BROADCOM DCSG Package Release: Ventura MR FW Package - Quanta - x86/ARM

ReleaseOrderPkg ID: *DCSG00366660*
Headline: *MR 7.14 - Full flash images for all Quanta boards (Package 51.14.0-3651)*
Package Type: *Ventura MR FW Package - Quanta - x86/ARM*
Package Version: *51.14.0-3651*
Date Generated: *Sep 24, 2020*

- **DCSG00352731 (ReleaseOrder) - Point Release: MR_FW_SAS3.5_7.14_FC - 5.140.00-3319 Firmware**
- **DCSG00343305 (ReleaseOrder) - Point Release: CtrlFw_Ph_15.0_Point_MR - 15.25.09.00 MR PL Release**
- **DCSG00011506 (ReleaseOrder) - GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS**
- **DCSG00010554 (ReleaseOrder) - Ventura Boot Block - 7.02.00.00-0021**
- **DCSG00297475 (ReleaseOrderPkg) - MR 7.14 Ventura BIOS Package 7.14.00.0_0x070E0202_07.14.06.02 (AARCH64/x64) - (Contains UEFI and HII - X64 Signed binary)**
  - **DCSG00297438 (ReleaseOrder) - MR 7.14 HEFU for Ventura and Aero 07.14.06.02 (AARCH64/x64) - Contains Signed X64 Binary**
  - **DCSG00297411 (ReleaseOrder) - MR 7.14 UEFI Driver For Ventura and Aero version 0x070E0202 (AARCH64/x64) - Signed X64 Binary**
  - **DCSG00077165 (ReleaseOrder) - MR 7.14 Legacy BIOS for Ventura and Aero v7.14.00.0**
  - **DCSG00011506 (ReleaseOrder) - GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS**
- **DCSG00350403 (ReleaseOrderPkg) - MR [7.14] Ventura SBR Package version 5.1400.00-0466**
  - **DCSG00348202 (ReleaseOrder) - Pre-Alpha Release: MR_RMC_SAS3.5_Ventura - 466 SBR_RMC**
  - **DCSG00136225 (ReleaseOrder) - Alpha Release: SBR_Bld_Tools - 1.03 SBR_TOOLS**
  - **DCSG00093483 (ReleaseOrder) - SPICO v1.08**
  - **DCSG00011506 (ReleaseOrder) - GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS**
  - **DCSG00010551 (ReleaseOrder) - HW Settings v1.17 - Add support for Harpoon + 25MHz**
  - **DCSG00010549 (ReleaseOrder) - PCE Settings v1.16 Update**
- **DCSG00366639 (ReleaseOrderPkg) - MR 7.14 NVData (5.1400.09-0002) for Quanta boards**
  - **DCSG00328631 (ReleaseOrder) - Point Release: MR_FW_SAS3.5_7.14_FC - 5.140.04-3286 NVDATA_XSD**
  - **DCSG00011506 (ReleaseOrder) - GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS**
  - **DCSG00007929 (ReleaseOrder) - SASPARSER: DCSG Re-Release 11.02.00.00**
  - **DCSG00320061 (HWBoardImageConfig) - Quanta_152D_8B00 QS3516B-32PD-R0156**
  - **DCSG00320059 (HWBoardImageConfig) - Quanta_152D_8B00_soem1 QS3516B-32PD-R0156**
  - **DCSG00320060 (HWBoardImageConfig) - Quanta_152D_8B00_soem2 QS3516B-32PD-R0156**
  - **DCSG00320062 (HWBoardImageConfig) - Quanta_152D_8B01 QS3516B-240PD-R0156**
  - **DCSG00320057 (HWBoardImageConfig) - Quanta_152D_8B01_soem1 QS3516B-240PD-R0156**
  - **DCSG00320058 (HWBoardImageConfig) - Quanta_152D_8B01_soem2 QS3516B-240PD-R0156**
- **Custom Image Table**

Point Release (DCSG00352731) - Firmware - 5.140.00-3319

ReleaseOrderID: DCSG00352731
Headline: Point Release: MR_FW_SAS3.5_7.14_FC - 5.140.00-3319 Firmware
Release Version: 5.140.00-3319
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_SAS3.5_7.14_FC
Release Type: Point
UCM Stream: MR_FW_SAS3.5_7.14_FC_Rel
Owner: dcsgccadm
Release Baseline: MR_FW_SAS3.5_7.14_FC-2020-09-14-5.140.00-3319_REL_1600112592@\MegaRAID
Release Date / Time: 2020-09-14 19:41:51.000000
Release Type: Point

Firmware Defects Fixed (11):

Defect ID: DCSG00319375
Headline: storcli show success for PDCache setting change on VD even though Cache setting of drive was not changed
Description Of Change: On receiving a pdcache setting change for VD, check if underlying drives support cache setting or not and fail command if any of the drives don't support write cache.
Issue Description: Firmware does VD level sanity checks and fails command only if VD level checks fail.
However, if setting failed on corresponding physical drives, the error was not propagated back to caller.
So command was showing success even in the disk setting failed.
Steps To Reproduce: Create VD on a PD that does not support write cache and try to set pdcache ON from storcli.

Defect ID: DCSG00335204
Headline: extend timeout for OOB command for SATA EPC enabled drive
Description Of Change: Check if a drive is SATA EPC enabled. Extend the timeout for a DCDB command from I2C OOB path for the EPC enabled drive.
This serves as an ER of temporary solution for SATA EPC handling until a PR is implemented for SATA EPC handling.
Issue Description: SATA EPC enabled drive can take a long time to spin up. When the drive is set into standby state without controller knowledge, new DCDB commands from OOB can take a long time and causing TM reset.
Steps To Reproduce: see reproduce steps

Defect ID: DCSG00351860
Headline: MR 7.14 Sept Point: pd_cache setting changes for nvme drives being handled incorrectly
Description Of Change: Changes made to skip the pd cache supported check for NVME drives.
Issue Description: For NVME drives the cache page setting is returning the same setting for all non-default pages including the changeable setting.
Steps To Reproduce: Try to set pdcache setting to ON a logical drive having NVME drives.

Defect ID: DCSG00119155
Headline: PL SATA: Sanitize operation is completed before actual completion from drive.
Description Of Change: During processing of completion of read log command, corrected the condition check to indicate sanitize is in progress.
Issue Description: When sanitize operation is in progress, PL internally sends sanitize status and read log ext commands to drive. During completion of read log ext, a wrong condition check indicates sanitize operation is not in progress and the command is completed.
Steps To Reproduce: 1. Convert all drives state form Spindown to spinup in the configuration
2. Start sanitize on only SATA HDD single drive, immediately observed the Firmware crash.

Defect ID: DCSG00139294
Headline: SATA only : Controller hang is observed due to recursive function call.
Description Of Change: Avoid starting of pended commands to SATA drive from completion functions of a command to avoid recursion.
Issue Description: Controller hang is observed with ATA pass through command followed by a pended command that fails.
At the completion of pass through command, PL starts the pended IOs if any.
If the pended IO is failed due to invalid CDB, then immediately completion function is called causing recursion.
This causes controller hang.
Steps To Reproduce: Install the FreeNAS and try to create ZFS pool(Storage -> Pools -> Add) of the direct attached SSDs.

- ATA command completes when there are IOs in pendlist.
- The pended IO has invalid CDB

Defect ID: DCSG00232962
Headline: Firmware fails to send Enclosure removal event to host when the enclosure is removed from the topology.
Description Of Change: Condition used for sending the enclosure removal event was incorrect in the latest code. Corrected the condition to send the enclosure removal event to host.
Issue Description: When the enclosure cable is pulled out firmware fails to send the Enclosure removal event to host. As a result, host driver throws a warning that "Received an add enclosure event for an enclosure that is already active" when the enclosure is connected back.
Steps To Reproduce: 1.Update the OS with the latest driver and controller to latest firmware.
2.Verify the driver is updated properly and enclosure with drives are discovered properly.
3.Now perform hot plug to the enclosure cable .
4.Observe "Received an add enclosure event for an enclosure that is already active" from driver event logger.

Defect ID: DCSG00311524
Headline: ExtManPage41 TX Values are not being applied / run by AERO SERDES
Description Of Change: Updated CSW M0 code to version 6790. M0 changes:
-Fix off by 1 error in setting PMU queue sizes. The hardware registers expects the last entry index to be written, not the number of entries.
-M0 to increase the delay for waiting for the semaphore from A15 (from 2msec to 5msec)

PL Changes
-Fixed bug where the PL/M0 CSW semaphore global flag was never cleared
-Added support for M02PL_REPORT_ERROR status ErrorCode of 0x7 (MSG_WAITING_SEMAPHORE) since the M0 sends this as a status message
-Added MemSyncs to the function used to send PMU messages from the PL to the CSW M0 to make sure the queue entry is flushed from cache before updating the write index.
Issue Description: The PL reads SerDes settings from NVDATA and sends them to the CSW M0 using PMU messages. Those messages were not reliably being transported, so updated settings may not be used.
Steps To Reproduce: Windows 2016
Scrutiny 25.0.5
Run Scrutiny, open AERO SI GUI.
Select SATA Drive
Look at Transmitt Settings Tab.
All values are still at their defaults of
C0 Cursor 27 --> Remain unchanged
Pre Cursor 0 --> Remain unchanged
Post Curson 6 --> Should be 12
Slew 1 --> Should be 0

Defect ID: DCSG00265811
Headline: 9460-8i faults repeatedly at fw\raid\utils.c
Description Of Change: - Added code to not fault near the boundary condition while building a PRP List
Issue Description: 9460-8i faults repeatedly at fw\raid\utils.c while just booting on an ARM server
Steps To Reproduce: - Create a R1 volume with 2 NVMe drives
- Reboot the server

Defect ID: DCSG00265980
Headline: [9440-8i+X86+MR7.13] SSD JBOD Drive state will change from (U-Up) to (D-Down/PowerSave) when they rmmod and insmod megaraid
Description Of Change: When a START STOP UNIT command is successfully completed from the host, check if the the power state for that PD is STOPPED, if it is update the power state to ACTIVE.
Issue Description: When the driver is unloaded, MR FW spins down the attached drives to save power. When the driver is re-loaded FW passes the sense data from the JBOD drives to the OS to do the recovery. The host sends a START STOP UNIT command to spin up the drives, but FW was never notified so the power state remained POWERSAVE
Steps To Reproduce: 1. Set Drive PD to JBOD
2. Storcli /c0 show
3. rmmod megaraid_sas.ko
insmod megaraid_sas.ko

4. storcli /c0 show

Defect ID: DCSG00314225
Headline: Controller fault on rebuild and IO
Description Of Change: oob status poll command should be added as a task, if FW get the command while OOB Config Cmd is in Progress..
Issue Description: Controller fault on rebuild while heavy IO was running. This is seems to happening because when i2c interrupt received for FOREIGN config, OOB Config cmd will be in Progress. While processing this command in interrupt context, OOB Poll request is received for log Get cmd.
LogGet scans all the events, if it takes more than 10ms FW adds to task to allow PL to run. FW checks if tasks are called from Interrupt (i.e IntNesting) before starting. If called from interrupt FW asserts.
Steps To Reproduce: 1.Create 2, RAID 1 volumes across 2 drives
2.Create GHS
3.Start Heavy IO to the RAID 1 volume (50 threads, 64k IO)
4.Offline one of the drives associated with the VD
5.While rebuild was happening on the drive and IO was running, controller had faulted.

Defect ID: DCSG00322186
Headline: FW is overriding the data length , present in the command frame header, with sizeof (MR_LD_ALLOWED_OPS_EXT)
Description Of Change: Changed the FW API code to use the size of the structure instead of size from the header for data copy.
Issue Description: FW was using size from the header for data copy.
Steps To Reproduce: 1. Boot to OS
2. Send MR_DCMD_LD_GET_ALLOWED_OPS using storelib

Firmware Enhancements Implemented (5):

EnhancementRequest ID: DCSG00298872
Headline: Adding critical events to a bad SAS/SATA drive that is consistently failing TM Reset
Description Of Change: When a drive consistently failing TM Reset, sending a critical event so that user intervention should take place.

EnhancementRequest ID: DCSG00306577
Headline: Add framework to inject correctable errors to endpoint in Atlas dev bst
Description Of Change: Error forwarding is enabled by the Host in synthetic UP and DS ports of the switch
1. Inject a Correctable Error condition in the Endpoint device
1. Verify that the host has logged the receipt of correctable error message from the EP.
2.Additionaly, the trace messages (if enabled) can be checked for the presence of

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EnhancementRequest ID: DCSG00341313
Headline: SCONS: Add IOP_SUBSYSTEM_ enums to assembly
Description Of Change: Modify generate_mpi_asm() script so it may find IOP_SUBSYSTEM_ defines

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EnhancementRequest ID: DCSG00342838
Headline: Support DEVICE_KEY_BASIS flags.
Description Of Change: Support DEVICE_KEY_BASIS flags.

Point Release (DCSG00343305) - MR PL-SCS Libs - 15.25.09.00

ReleaseOrderID: DCSG00343305
Headline: Point Release: CtrlFw_Ph_15.0_Point_MR - 15.25.09.00 MR PL Release
Release Version: 15.25.09.00
Product Org: SCS
Product Gen: SAS3.5
Product Family: ControllerFw
UCM Project: CtrlFw_Ph_15.0_Point_MR
Release Type: Point
UCM Stream: CtrlFw_Ph_15.0_Point_MR
Owner: dcsgccadm
Release Baseline: CtrlFw_Ph_15.0_Point_MR-2020-09-02-15.25.09.00_REL_1599041590@\SAS35
Release Date / Time: 2020-09-02 10:11:51.000000
Release Type: Point

MR PL-SCS Libs Defects Fixed (9):

Defect ID: DCSG00301666
Headline: BST: ELID update due to SAS-Address update on Blr Servers
Description Of Change: ELID is dependent on SAS address. Blr Servers are updated with valid SAS-Address. Requiring to update ELID's.
Issue Description: ELID's mismatch when sas-address got updated. Hence config file is updated with updated ELID
Steps To Reproduce: Run bst scripts with original config file to see ELID mismatch

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Defect ID: DCSG00305439
Headline: [BST] Remove the erase persistent test case from BST.
Description Of Change: Remove the erase persistent test case from BST
Issue Description: Persistent erase issued from scrutiny tool hangs some times leading to BST hang.
Steps To Reproduce: 1) Use the latest scripts and run the Activity bst.
2) Observe that some times BST hangs intermittently.

Defect ID: DCSG00312633
Headline: BST: Num Slots config file update for topology with Atlas Configuration
Description Of Change: Num Slots configuration file on server will be used to verify num slots information obtained from cli command. Which will also take care of the issue with Ph14 reporting extra slot count for Atlas switch
Issue Description: Currently Atlas-encl type 6 for Ph14 reports an extra slot. And the issue needs to be addressed for having a num slot config file for Ph14 separately.
Steps To Reproduce: Run the BST version 3E on Ph14 code and the slot count on Atlas is reported with extra slot.

Defect ID: DCSG00315471
Headline: BST: NumSlots fix for Ph14 &15 broke BST on other fw phases
Description Of Change: The condition calling for not considering fw-Phase 14 & 15 has been re-stated.
Issue Description: the statement written was not explicit enough
Steps To Reproduce: Run BST '3F' on Ph 16 & 17 to see the BST fail.

Defect ID: DCSG00319578
Headline: Incorrect slot count is present in config, for a BP connected to external card in BST server.
Description Of Change:
Corrected slot count the card.
Issue Description:
Incorrect slot count in config caused BST failure.
Steps To Reproduce:
Inspect config file.

Defect ID: DCSG00119155
Headline: PL SATA: Sanitize operation is completed before actual completion from drive.
Description Of Change: During processing of completion of read log command, corrected the condition check to indicate sanitize is in progress.
Issue Description: When sanitize operation is in progress, PL internally sends sanitize status and read log ext commands to drive. During completion of read log ext, a wrong condition check indicates sanitize operation is not in progress and the command is completed.
Steps To Reproduce: 1. Convert all drives state form Spindown to spinup in the configuration
2. Start sanitize on only SATA HDD single drive, immediately observed the Firmware crash.

Defect ID: DCSG00139294
Headline: SATA only : Controller hang is observed due to recursive function call.
Description Of Change: Avoid starting of pended commands to SATA drive from completion functions of a command to avoid recursion.
Issue Description: Controller hang is observed with ATA pass through command followed by a pended command that fails.
At the completion of pass through command, PL starts the pended IOs if any.
If the pended IO is failed due to invalid CDB, then immediately completion function is called causing recursion.
This causes controller hang.
Steps To Reproduce: Install the FreeNAS and try to create ZFS pool(Storage -> Pools -> Add) of the direct attached SSDs.

- ATA command completes when there are IOs in pendlist.
- The pended IO has invalid CDB

Defect ID: DCSG00232962
Headline: Firmware fails to send Enclosure removal event to host when the enclosure is removed from the topology.
Description Of Change: Condition used for sending the enclosure removal event was incorrect in the latest code. Corrected the condition to send the enclosure removal event to host.
Issue Description: When the enclosure cable is pulled out firmware fails to send the Enclosure removal event to host. As a result, host driver throws a warning that "Received an add enclosure event for an enclosure that is already active" when the enclosure is connected back.
Steps To Reproduce: 1.Update the OS with the latest driver and controller to latest firmware.
2.Verify the driver is updated properly and enclosure with drives are discovered properly.
3.Now perform hot plug to the enclosure cable .
4.Observe "Received an add enclosure event for an enclosure that is already active" from driver event logger.

Defect ID: DCSG00311524
Headline: ExtManPage41 TX Values are not being applied / run by AERO SERDES
Description Of Change: Updated CSW M0 code to version 6790. M0 changes:
-Fix off by 1 error in setting PMU queue sizes. The hardware registers expects the last entry index to be written, not the number of entries.
-M0 to increase the delay for waiting for the semaphore from A15 (from 2msec to 5msec)

PL Changes

-Fixed bug where the PL/M0 CSW semaphore global flag was never cleared
-Added support for M02PL_REPORT_ERROR status ErrorCode of 0x7 (MSG_WAITING_SEMAPHORE) since the M0 sends this as a status message
-Added MemSyncs to the function used to send PMU messages from the PL to the CSW M0 to make sure the queue entry is flushed from cache before updating the write index.

Issue Description: The PL reads SerDes settings from NVDATA and sends them to the CSW M0 using PMU messages. Those messages were not reliably being transported, so updated settings may not be used.

Steps To Reproduce: Windows 2016
Scrutiny 25.0.5
Run Scrutiny, open AERO SI GUI.
Select SATA Drive
Look at Transmitt Settings Tab.
All values are still at their defaults of
C0 Cursor 27 --> Remain unchanged
Pre Cursor 0 --> Remain unchanged
Post Curson 6 --> Should be 12
Slew 1 --> Should be 0

MR PL-SCS Libs Enhancements Implemented (3):

EnhancementRequest ID: DCSG00216341
Headline: [BST] Add the corrective action in BST scripts to check if SAS address is retained after persistent erase
Description Of Change: 1) Modify the BST scripts to exit if the adapter does not have valid SAS address.
2) If SAS address is valid, do a persistent erase and then reboot the controller.
3) Now check if SAS address is retained.

EnhancementRequest ID: DCSG00256443
Headline: BST: Add support for Drive Control Modules to cable breaker test cases.
Description Of Change:
Scripts will be able to issue commands for Drive control modules as part of Cable breaker tests.

EnhancementRequest ID: DCSG00268618
Headline: BST: Verify version control file from fw
Description Of Change: Version control file will be used to track the version verification by bst.

GCA Release (DCSG00011506) - MR_FW_BLD_TOOLS - 1.03

ReleaseOrderID: DCSG00011506
Headline: GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS
Release Version: 1.03
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_BLD_TOOLS
Release Type: GCA
UCM Stream: MR_FW_BLD_TOOLS_Rel
Owner: st887734
Release Baseline: MR_FW_BLD_TOOLS_Rel_2019-07-25@\MegaRAID
Release Date / Time: 2019-07-25 16:22:41.000000
Release Type: GCA

GCA Release (DCSG00010554) - BOOT_BLOCK - 7.02.00.00-0021

ReleaseOrderID: DCSG00010554
Headline: Ventura Boot Block - 7.02.00.00-0021
Release Version: 7.02.00.00-0021
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_BOOTBLOCK
Release Type: GCA
UCM Stream: MR_FW_BOOTBLOCK_Rel
Owner: st887734
Release Baseline: MR_FW_BOOTBLOCK_Rel_2019-07-24@\MegaRAID
Release Date / Time: 2019-07-24 17:36:17.000000
Release Type: GCA

ReleaseOrderPkg ID: *DCSG00297475*
Headline: *MR 7.14 Ventura BIOS Package 7.14.00.0_0x070E0202_07.14.06.02 (AARCH64/x64) - (Contains UEFI and HII - X64 Signed binary)*
Package Type: *MR 3516 Ventura ARM BIOS Package*
Package Version: *7.14.00.0_0x070E0202_07.14.06.02*
Date Generated: *Sep 24, 2020*

Point Release (DCSG00297438) - HEFU_HII - 07.14.06.02

ReleaseOrderID: DCSG00297438
Headline: MR 7.14 HEFU for Ventura and Aero 07.14.06.02 (AARCH64/x64) - Contains Signed X64 Binary
Release Version: 07.14.06.02
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_BIOS
UCM Project: MR_SAS_HEFU_HII_7.14
Release Type: Point
UCM Stream: MR_SAS_HEFU_HII_7.14_Patch
Owner: chgr
Release Baseline: MR_SAS_HEFU_HII_7.14_Patch_2020-07-17_07.14.06.02_Signed@\MegaRAID
Release Date / Time: 2020-07-17 07:35:53.000000
Release Type: Point

HEFU_HII Defects Fixed (1):

Defect ID: DCSG00242413
Headline: ShutOFF PTB - HII should pop-up a message reboot required
Description Of Change: When user turn off/on fw will retune reboot required. HII needs to handle the mfistatus reboot required.
Issue Description: PTB is controller property which can be enable/disable at HII.
PTB - Controller Management -> Controller Property -> PTB
PTB disabled from enable.- HII should return a pop-up message - "Operational has been completed and reboot required".
Attached the e-mail communication had with Dev team on this defect scenario,

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Steps To Reproduce: PTB is controller property which can be enable/disable at HII.
PTB - Controller Management -> Controller Property -> PTB
PTB disabled from enable.- HII should return a pop-up message - "Operational has been completed and reboot required".
Attached the e-mail communication had with Dev team on this defect scenario,

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HEFU_HII Enhancements Implemented (1):

EnhancementRequest ID: DCSG00297398
Headline: MR7.14 - Workaround for ARM server for GetTime() - HII
Description Of Change: The GetTime interface returns the time of the system RTC chip, and the function is internally bound to the server RTC chip hardware; the X86 platform RTC chip is integrated inside the South Bridge, directly accessed through IO, and the performance is good;
The RTC chip of the ARM server is designed outside the chip and accessed through I2C. The BIOS must compete with the BMC for I2C resources. The low I2C speed and other factors lead to deviations from X86 and the performance difference is very large; Raid new firmware is called frequently
The GetTime interface, the cumulative internal time consumed by the GetTime function causes the startup to slow down

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Point Release (DCSG00297411) - UEFI BSD Driver - 0x070E0202

ReleaseOrderID: DCSG00297411
Headline: MR 7.14 UEFI Driver For Ventura and Aero version 0x070E0202 (AARCH64/x64) - Signed X64 Binary
Release Version: 0x070E0202
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_BIOS
UCM Project: MR_UEFI_Drv_7.14
Release Type: Point
UCM Stream: MR_UEFI_Drv_7.14_Patch
Owner: chgr
Release Baseline: MR_UEFI_Drv_7.14_Patch_2020-07-17_0x070E0202_Signed@\MegaRAID
Release Date / Time: 2020-07-17 07:20:52.000000
Release Type: Point

GCA Release (DCSG00077165) - BIOS - 7.14.00.0

ReleaseOrderID: DCSG00077165
Headline: MR 7.14 Legacy BIOS for Ventura and Aero v7.14.00.0
Release Version: 7.14.00.0
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_BIOS
UCM Project: MR_SAS_BIOS_7.14
Release Type: GCA
UCM Stream: MR_SAS_BIOS_7.14_Rel
Owner: chgr
Release Baseline: MR_SAS_BIOS_7.14_Rel_2020-01-28_7_14_00_0@\MegaRAID
Release Date / Time: 2020-01-28 12:20:48.000000
Release Type: GCA

GCA Release (DCSG00011506) - MR_FW_BLD_TOOLS - 1.03

ReleaseOrderID: DCSG00011506
Headline: GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS
Release Version: 1.03
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_BLD_TOOLS
Release Type: GCA
UCM Stream: MR_FW_BLD_TOOLS_Rel
Owner: st887734
Release Baseline: MR_FW_BLD_TOOLS_Rel_2019-07-25@\MegaRAID
Release Date / Time: 2019-07-25 16:22:41.000000
Release Type: GCA

ReleaseOrderPkg ID: *DCSG00350403*
Headline: *MR [7.14] Ventura SBR Package version 5.1400.00-0466*
Package Type: *Ventura MR SBR Package - All*
Package Version: *5.1400.00-0466*
Date Generated: *Sep 24, 2020*

Pre-Alpha Release (DCSG00348202) - SBR_RMC - 466

ReleaseOrderID: DCSG00348202
Headline: Pre-Alpha Release: MR_RMC_SAS3.5_Ventura - 466 SBR_RMC
Release Version: 466
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_RMC_FW
UCM Project: MR_RMC_SAS3.5_VENTURA
Release Type: Pre-Alpha
UCM Stream: MR_RMC_SAS3.5_VENTURA_Rel
Owner: stewaldo
Release Baseline: stewaldo_MR_RMC_SAS3.5_VENTURA_Rel_466_2020-09-09@\MegaRAID
Release Date / Time: 2020-09-10 12:18:31.000000
Release Type: Pre-Alpha

SBR_RMC Defects Fixed (1):

Defect ID: DCSG00318961
Headline: Intermittent hang condition on repeated reboots
Description Of Change: RMC was getting stuck in a 'while' loop which was using the System Counter to measure a timeout. The failure was caused by a race condition which left the System Counter disabled, and therefore unable to reach its timeout tick count. The fix was to convert to a loop counter for a reasonable approximation of the timeout time.
Issue Description: Initial observation of a time out waiting for BAR init was shown to be a side effect of the controller being unresponsive.
Steps To Reproduce: This was found to be highly dependent on specific server/controller combinations, and could be repeated after hundreds of iterations of a simple warm reboot test, or cache offload with glitch test on the affected systems.

Alpha Release (DCSG00136225) - SBR_TOOLS - 1.03

ReleaseOrderID: DCSG00136225
Headline: Alpha Release: SBR_Bld_Tools - 1.03 SBR_TOOLS
Release Version: 1.03
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: SBR_Bld_Tools
Release Type: Alpha
UCM Stream: SBR_Bld_Tools_Rel
Owner: dcsgccadm
Release Baseline: SBR_Bld_Tools-2020-04-07-1.03_REL_1586312246@\MegaRAID
Release Date / Time: 2020-04-08 02:16:58.000000
Release Type: Alpha

SBR_TOOLS Defects Fixed (2):

Defect ID: DCSG00068041
Headline: SBR Build date and time corrected
Description Of Change: SBR Build date and time are now being correctly reported
Issue Description: SBR Build date and time were attached to the flash header so that they were read together rather than separately.
Steps To Reproduce: Using storelib, retrieve the flash components and see SBR build date and time entries overlap.

Defect ID: DCSG00108561
Headline: Clean up SBR Build Tools
Description Of Change: Fixed SBR build tools
Issue Description: SBR build tools were not functioning with build server.
Steps To Reproduce: N/A

GCA Release (DCSG00093483) - SBR_SPICO - 1.08

ReleaseOrderID: DCSG00093483
Headline: SPICO v1.08
Release Version: 1.08
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: SBR_Bld_Tools
Release Type: GCA
UCM Stream: SBR_Bld_Tools_Rel
Owner: st887734
Release Baseline: SBR_Bld_Tools_Rel_2020-02-21@\MegaRAID
Release Date / Time: 2020-02-21 21:02:20.000000
Release Type: GCA

GCA Release (DCSG00011506) - MR_FW_BLD_TOOLS - 1.03

ReleaseOrderID: DCSG00011506
Headline: GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS
Release Version: 1.03
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_BLD_TOOLS
Release Type: GCA
UCM Stream: MR_FW_BLD_TOOLS_Rel
Owner: st887734
Release Baseline: MR_FW_BLD_TOOLS_Rel_2019-07-25@\MegaRAID
Release Date / Time: 2019-07-25 16:22:41.000000
Release Type: GCA

Pre-Alpha Release (DCSG00010551) - SBR_HW - 1.17

ReleaseOrderID: DCSG00010551
Headline: HW Settings v1.17 - Add support for Harpoon + 25MHz
Release Version: 1.17
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: SBR_Bld_Tools
Release Type: Pre-Alpha
UCM Stream: SBR_Bld_Tools_Rel
Owner: st887734
Release Baseline: SBR_Bld_Tools_Rel_2019-07-24.659@\MegaRAID
Release Date / Time: 2019-07-24 17:14:25.000000
Release Type: Pre-Alpha

Point Release (DCSG00010549) - SBR_PCE - 1.16

ReleaseOrderID: DCSG00010549
Headline: PCE Settings v1.16 Update
Release Version: 1.16
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: SBR_Bld_Tools
Release Type: Point
UCM Stream: SBR_Bld_Tools_Rel
Owner: st887734
Release Baseline: SBR_Bld_Tools_Rel_2019-07-24.7403@\MegaRAID
Release Date / Time: 2019-07-24 17:07:29.000000
Release Type: Point

ReleaseOrderPkg ID: *DCSG00366639*
Headline: *MR 7.14 NVData (5.1400.09-0002) for Quanta boards*
Package Type: *Ventura MR NVDATA Package*
Package Version: *5.1400.09-0002*

Point Release (DCSG00328631) - NVDATA_XSD - 5.140.04-3286

ReleaseOrderID: DCSG00328631
Headline: Point Release: MR_FW_SAS3.5_7.14_FC - 5.140.04-3286 NVDATA_XSD
Release Version: 5.140.04-3286
Product Org: DCSG
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_SAS3.5_7.14_FC
Release Type: Point
UCM Stream: MR_FW_SAS3.5_7.14_FC_Rel
Owner: dcsgccadm
Release Baseline: MR_FW_SAS3.5_7.14_FC-2020-08-23-5.140.04-3286_REL_1598211562@\MegaRAID
Release Date / Time: 2020-08-23 19:38:54.000000
Release Type: Point

NVDATA_XSD Defects Fixed (558):

Defect ID: DCSG00009013
Headline: NVDATA in wrong location in MR release zip files
Description Of Change: Changed directories to the correct directory so the relative path in the zip file would be correct
Issue Description: The zip file was being created with the NVDATA at a bogus relative path:
../../../../../nvdata/nvdata.xsl
../../../../../nvdata/aero/sas3916A0.xsd
../../../../../nvdata/aero/sas3916A0Channel.xsd
../../../../../nvdata/aero/sas3916A0Channel8Phy.xsd
../../../../../nvdata/aero/sas3916A0_fpga.xsd
Steps To Reproduce: Build MR all release.

Defect ID: DCSG00010049
Headline: Aero: PL cannot handle very large SES Page 0Ah from Managed Switch SES for MPI SEP Request
Description Of Change: Extended PL's enclosure management to use IEEE chains to skip over data that is larger than its internal SES buffer. Add proper searching for slots associated with a Managed Switch.

Corrected PL's SES Page 0Ah translation for Manged Switch SES's to better translate a buffer inline.
Issue Description: PL cannot handle very large SES Page 0Ah from Managed Switch SES. This is especially true for processing an MPI SEP Request, where SES Page 0Ah needs to be translated inline.
Steps To Reproduce: Attach a Managed Switch (Atlas) to an Aero controller. The switch must be configured for a large number of devices.

Defect ID: DCSG00010071
Headline: pl: backend PCIe: legacy interrupt may not be serviced if interrupt mask fails
Description Of Change: Perform a timed retry of INTx handling if this case occurs.
Issue Description: If an endpoint or bridge generates a legacy (INTx) PCI interrupt and a config transaction sent to the entity by PL to read or mask the INTx fails, the entity's INTx will not be serviced. It may also cause the perceived state of the INTx to remain constant from that point on, causing the hardware interrupt that reports changes in the state of the INTx to not reassert.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00010189
Headline: Coverity detected unreachable code in IOP MCTP code
Description Of Change: Deleted condition that was unreachable in IOP MCTP code
Issue Description: A couple of conditions were unreachable in IOP MCTP code
Steps To Reproduce: None

Defect ID: DCSG00010317
Headline: Aero A0: Controller fault EC57 observed on doing individual lane break test on VendorX Gen4 NVMe drive
Description Of Change: Modified the root port hot reset initiation procedure to prevent cleanup failure.
Issue Description: During a test with IOs and individual lane breaks between the controller and direct attach gen4 NVMe drive, the controller faults with 0xEC57.
Steps To Reproduce: Connect a gen4 NVMe drive to the controller with a gen4 cable breaker in between. Run IOs and do individual lane breaks.

Defect ID: DCSG00010608
Headline: Aero: backend PCIe: disallow DPC for PCIe 3 and earlier specific vendor switches
Description Of Change: DPC will not be enabled on PCIe 3 and earlier specific vendor switches.
Issue Description: Downstream Port Containment has not been supported or tested with specific vendor PCIe 3 or earlier switches on the Gen 3.5 parts. In order to avoid the possibility of unexpected behavior if one of these switches is connected to Aero, disallow usage of DPC with them in order to maintain Ventura-level behavior.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00012363
Headline: UBM Auto HFC grouping fixes and debug print fixes
Description Of Change: Check HFCs for attachment to I2C BP type when grouping HFCs to avoid grouping of HFCs attaching to incorrect BP types. Fixed UBM and EM RB debug prints.
Issue Description: Ventura max x1 links supported per CSW is 4 and auto HFC grouping may not work when 1 quad from each CSW is used.
Incorrect HFC/connectors with SGPIO BP are grouped when auto HFC is enabled for 8 DFCs x1 config.
Fix UBM and EM RB debug prints.
Steps To Reproduce: Issues identified in dev testing

Defect ID: DCSG00012378
Headline: Aero: Various faults occur with PCIe clock configuration mismatch between Aero and managed switch (Atlas)
Description Of Change: Corrected locations that freed SMIDs to an MPI Device (in Atlas) to stop the timer.
Corrected handling of events to an MPI Device to not start a new Adapter Reset if one is in progress.
Corrected PL PCI Discovery Event Reply to not call back into PCI Discovery if event replay was called by it.
Issue Description: Various faults occur with PCIe clock configuration mismatch between Aero and managed switch (Atlas). Includes 0xEE2B (SMID freed while timer is running), 0xEE1A (Adapter Reset already in progress), and 0xEC02 (PCI Discovery reentered).
Steps To Reproduce: Mismatch the PCIe clocks between an Aero controller and a managed/Atlas switch.
Reboot the server over and over.

Defect ID: DCSG00012481
Headline: Aero: HW_SETTINGS_CHANGE PCIe PHY LF setting should be changed from 16 to 15
Description Of Change: Updated PSW Firmware Image to version 0x65D1
Issue Description: PTC Compliance Test Failures Occur Due to Aero Rejecting Requests to Use Preset 10 During 8 GT/sec and 16 GT/sec Equalization.
Default PHY register settings for P10 coefficients did not match default LF value, causing MAC to reject the request, as it did not satisfy coefficient rules.
Steps To Reproduce: Perform PTC Compliance Test

Defect ID: DCSG00012569
Headline: Unable to detect drives behind Sea controller during Windows installation
Description Of Change: AS part of Multi-VSES feature, more than one direct attached backplane can be connected to the controller. Have modified the Discovery Event Replay State machine to send Enclosure Add Event and SAS Topology Change List Event for each of the DA enclosure with their respective attached devices.
Issue Description: SAS topology change list event for direct attached devices didn't have correct enclosure handle associated causing drivers not discover the devices.

Steps To Reproduce: In a certain topology using Sea controller with more than one direct attached back planes of different types, attempt to install windows on a drive connected behind the controller.

Defect ID: DCSG00012605
Headline: Aero: Error on posting a SCSI IO request to Atlas SES can cause IO forever being pended
Description Of Change: When the error occurs posting the request, tell the MPI Device state machine code that an error occurred, which will trigger an Adapter Reset to the switch's MPI Device.
Issue Description: When posting a SCSI IO request to an Atlas/managed switch SES, an error upon posting can cause the IO to be forever being pended. The MPI Device is never reinitialized, and access to the SES stops working.
Steps To Reproduce: Attach an Atlas switch behind an Aero controller with a marginal link between the two. Run SCSI IOs to the managed switch SES.

Defect ID: DCSG00012617
Headline: Battery Learn schedule is not being reset to 90 days after a new battery chemID is installed.
Description Of Change: When a new battery is detected, postpone the learn cycle by 90 days.
Issue Description: The battery learn schedule is not being reset to 90 days after installing a new battery chemID.
Steps To Reproduce: Install a new battery chemID with the system off.
Boot system and review the FW log to show the new chemID was detected properly.
Notice the learn schedule did not reset to 90 days out.

Defect ID: DCSG00013239
Headline: SPILIB2: If the default clock divider is specified, there are excessive clock prints
Description Of Change: Modified algorithm so that init with DEFAULT clock divider actually changes parameter block
Issue Description: Excessive clock adjustment noted via debug prints from SPI 2.0
Steps To Reproduce: Initialize SPI with clock divider set to DEFAULT

Defect ID: DCSG00013387
Headline: pl: backend PCIe: debug prints
Description Of Change: Modified and added a few debug prints in the backend PCIe code.
Issue Description: In the backend PCIe code, there are a few debug prints that could be modified or added for ease of debug.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00014562
Headline: HW Workaround:Resizable BARs capability
Description Of Change: Since we don't need Resizable bars and there have been some system BIOS' that incorrectly set the capability, eliminate Resizable BAR capability from the chain.
Issue Description: On Aero, PCI SIG Compliance PCIECV 4.0 Test 1_45 (Resizable BAR) fails due to Bit 13 in the Resizable BAR Control Register remaining sticky across resets rather than defaulting to 0 after reset.
Steps To Reproduce: Run the new PCI SIG Compliance test

Defect ID: DCSG00015033
Headline: HIIM component is not listed
Description Of Change: While building the flash component details HIIM is added to the list
Issue Description: While building the flash component details HIIM is not added to the list
Steps To Reproduce: run storcli64.exe /c0 show all page

Defect ID: DCSG00016069
Headline: Aero: backend PCIe: 265D fault if PCIe Device Page 2 is read for a SES device
Description Of Change: Fixed a bug that caused a PCIe Device Page 2 access to an MPI SES device's DevHandle to proceed instead of being rejected.
Issue Description: If an Atlas switch with an enabled MPI device is attached to the HBA and an internal test application is run on the host system, a 265D fault occurs. It appears that the test application is attempting to read PCIe Device Page 2 with the MPI SES device's DevHandle.
Steps To Reproduce: Attach an Atlas switch to the HBA and run the offending test application.

Defect ID: DCSG00017353
Headline: Superfluous message for NVME IO with SGL
Description Of Change: Remove extra message
Issue Description: Remove extra message
Steps To Reproduce: These message would only print during NVME recovery for IO failure, therefore an NVME disk with medium errors would be needed

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Defect ID: DCSG00017381
Headline: SPILIB2: Windbond 16MB device fails to program
Description Of Change: Changed write command (0x32) properties so that it will not insert dummy cycles
Issue Description: Winbond 16MB device failed read-back test on first write
Steps To Reproduce: Download firmware with the spilib 20.00.01.00 onto a card with a Winbond 128 MegaBit part

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Defect ID: DCSG00017760
Headline: Avenger IOP: When CBB replies to NVSRAM Init PMU message, it returns FALSE
Description Of Change: Instead of checking the WIP bit once on NVSRAM init, wait for a timeout.
Issue Description: SPI NVSRAM init is failing due to WIP bit not clearing before the check is done.
Steps To Reproduce: Flash CBB/FMC from 00.15.00.00 - 00.15.02.00 on FPGA B348974 and observe SPI NVSRAM init failure. It does not fail on other FPGAs tried.

Defect ID: DCSG00018730
Headline: pl: backend PCIe: prevent switch rediscovery quirks
Description Of Change: Implemented path based rediscovery for backend PCIe switches.
Issue Description: When PL rediscovers a backend PCIe switch, all of the bridges within the switch and all of the endpoints attached to it are queried. This is not only inefficient but, if multiple devices are added to or removed from a switch in close succession, may also cause a race condition that defeats the port lockout timer.
Steps To Reproduce: Rediscover a PCIe switch attached to the device side of the ROC/IOC.

Defect ID: DCSG00018735
Headline: SPILIB 2.0: Custom Parts Write Parameters are Incorrect
Description Of Change: Modified parameters for some custom-made part's write commands to indicate no Dummy cycles
Issue Description: Inspection of parameter lists for these parts indicate the commands used have dummy bits set
Steps To Reproduce: Attempt to program these particular parts

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Defect ID: DCSG00019887
Headline: SPILIB: The SPI2 release zip contains SPI1 headers
Description Of Change: Modified path for SPI2 headers
Issue Description: Headers from old SPI library were being copied into to SPI2 release zips
Steps To Reproduce: Build SPI

Defect ID: DCSG00020839
Headline: Resolve rebase conflict
Description Of Change: Resolve rebase conflict
Issue Description: Resolve rebase conflict
Steps To Reproduce: Resolve rebase conflict

Defect ID: DCSG00021481
Headline: AeroMR GEN3 WIN,8 and 16 Drive SAS HDD, RAID0/RAID5/RAID6, 4K/8K RW, All QD.
Description Of Change: Reverted the PD queue depth in Aero to match Ventura's value.
Issue Description: The reported performance regression is related to an Aero only PD queue depth changed that occurred in ER ENHREQ1437148 (Merge RMW IOPs Performance POC into Aero Stream).
Steps To Reproduce: Run WIN,8 and 16 Drive SAS HDD, RAID0/RAID5/RAID6, 4K/8K RW, All QD and compare Aero to Ventura.

Defect ID: DCSG00022006
Headline: NVDATA Major version should be 0E00 for Phase 14
Description Of Change: Updated NVDATA Major version to 0E00
Issue Description: On the first NVDATA XSD file change of a phase, the major version is supposed to be updated to that phase.
Steps To Reproduce: Look at version

Defect ID: DCSG00022533
Headline: Atlas behind Aero IT: Fault code: 0x4000EDAC while running IOs and TMs.
Description Of Change: This was an inadvertent side effect of the fix for DCSG00013404.
Removing clearing the ChangeDetected flag in this case as this is unnecessary and the event generation code should already handle the not-reported-upward + change detected case properly.
Issue Description: 1.A switch and attached NVMe device are discovered but arent reported upward before the switch is pulled.
2.Both switch and device are moved to Delay Not Responding state. DMD timers are started.
3.Discovery repeatedly fails with link in bad state errors.
4.DMD timers expire.
5.Discovery of the switch fails again with a link in bad state error. The switch is transitioned to Not Responding state.
6.Since the switch wasnt reported upward and the Registered bit isnt set for switches, the DevMgr garbage collector hinting flag is set for the switch. The parent ports ChangeDetected flag is also cleared as there is no change to advertise upward.
7.Since the ChangeDetected flag is used to determine whether downstream device processing is needed and its now FALSE, DS device processing isnt performed, so the attached NVMe device isnt transitioned to Not Responding state.
8.When discovery completes, the DevMgr garbage collector runs and determines that the switch and attached device need to be removed.
9.It attempts to remove the NVMe device.
10.Since DS device processing wasnt performed, the device is still in Delay Not Responding state so an EDAC fault occurs.
Steps To Reproduce: Steps to Reproduce:

1. Flash the latest firmware 12.250.15.0 on Aero IT card (9500-16i)
2. Aero IT --> Atlas and UBM connected with 1 drive each.
3. Start IOs and TMs.
4. Now Power on the Atlas switch.
5. Observed FAULT.

Defect ID: DCSG00022705
Headline: pl: NVMe: maximum blocksize should be limited to 2 MB
Description Of Change: Limited the maximum NVMe device blocksize (LBA Data Size) allowed by NVMe init to 2 MB.
Issue Description: Since the NVMe IO breakup code supports a maximum NVMe device blocksize of 2 MB, the maximum blocksize allowed by NVMe init should be 2 MB instead of 2 GB.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00022999
Headline: Windows powershell shows 48 slots in single VSES mode
Description Of Change: Made a change in the VSES allocation code to always reserve the first VSES index for the direct attach enclosure/PCIe unmanaged switches and use other VSES indices for UBM.
Issue Description: In this configuration, there are 48 entries in the SES pages for the VSES even though there are only 16 direct attach phys.
Steps To Reproduce: Connect a UBM backplane to customer system and boot to Windows.

Defect ID: DCSG00023448
Headline: PL: Device removal event is not sent for hot removed end device
Description Of Change: Modified the check for whether a topology change list event entry is sent with NOT_RESPONDING status or not.
Issue Description: A device removal event is not sent for a hot removed end device. This is because of recent changes in PL device manager which broke the long existing event code to check for the device missing case.
Steps To Reproduce: Use customer system and backplane configuration. Populate all drive slots. In some cases, a hot remove will not result in a removal event being sent.

Defect ID: DCSG00023749
Headline: pl: NVMe: CFS not checked during handling of Abort Task
Description Of Change: Check an NVMe device's CFS bit when an Abort Task task management request is sent to it. If the CFS bit is set, fail the Abort Task request so that the issuer can escalate it to a device reset class TM.
Issue Description: If an NVMe device sets its Controller Fatal Status (CFS) bit, the NVMe specification suggests that it be handled by resetting the device. If an Abort Task task management request is issued to an NVMe device, PL should ensure that the device has not encountered a CFS condition before allowing the Abort Task to proceed; otherwise, the Abort Task could unexpectedly fail or time out.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00024038
Headline: pl: NVMe: controller reset shouldn't be issued if EN or RDY are 0
Description Of Change: If an NVMe device's Enable bit or Ready bit are found to have a value of 0 when issuing NVMe controller reset to the device, issue PCIe hot reset to it instead.
Issue Description: If an NVMe device's Enable bit or Ready bit are not set to 1 then controller reset can't be issued per NVMe specification: if CC.EN is 0 then there will be no transition from 1 to 0 and thus no controller reset, and if CC.EN is 1 but CSTS.RDY is 0 then setting EN to 0 has undefined results. This should not occur due to interlocks in PL subsystems that issue NVMe device resets, but it would be a good idea to check for this condition when issuing an NVMe controller reset to prevent a potential spec violation in the event that it does.

If the condition occurs, hot reset will be issued instead.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00024652
Headline: pl: Ventura/Mercator: device side PCIe link failure following adapter reset
Description Of Change: Worked around an issue that caused device side PCIe hardware to fail to establish a link following adapter reset.
Issue Description: After an adapter reset, device side PCIe links may take an unexpectedly long time to come up or may entirely fail to come up.
Steps To Reproduce: Perform adapter reset testing using Ventura with attached NVMe devices or PCIe switches.

Defect ID: DCSG00025523
Headline: Change 2WIRE_RESET and PERST GPIO signals logic level in NVDATA settings
Description Of Change: Fixed default and board xmls 2WIRE_RESET GPIO alternate source and master PERST CLAMP signal GPIO logic level
Issue Description: 2WIRE_RESET GPIO alternate source and master PERST CLAMP signal GPIO logic levels are setup incorrectly in the board NVDATA xml.
Steps To Reproduce: n/a

Defect ID: DCSG00026292
Headline: Increase EstimatedTimeBeforeSendingRequestFirmwareData to 10 mins
Description Of Change: Increase value of EstimatedTimeBeforeSendingRequestFirmwareData to 10 mins in the reply msg of UpdateComponent (0x14) command

Issue Description: Due to heavy IO, FW is taking more than 5 mins to complete MR_DCMD_CTRL_FLASH_FW_OPEN operation and did not send RequestFirmwareData (0x15) msg to UA within 3 mins as mentioned in the reply msg of UpdateComponent (0x14) command. UA waited for 3 mins + 1 mins(additional 60 secs as per spec) = 4 mins and then initiated CancelUpdate (0x1d).

Steps To Reproduce:
1. Connect Valvano-16i Controller to Whitley Server.
2. Connect Oberon UBM 4 Slot Backplane to Valvano-16i controller, Boot to OS
3. Connect SAS drives to all 4 slots of Oberon Backplane, create 97 VDs(Mix of single drive R0 and two drive R1 with WB , RA policies).
4. Run IO's on 97 VD's using VDbench.
5. From XCC, Start PLDM Firmware Update.
5. Observe that , PLDM Firmware update aborts with update status error.

Defect ID: DCSG00026516

Headline: FW - AMD2P Wave1 - UG bad drive is missing in MR 7.12 FW

Description Of Change:

Bad PD is failed in spinup state. DISM is marked completed on the bad PD after spinup retry. But due to recent firmware change the bad PD is not notified to RAID layer.
Fix is to use dismCleanupDone to ensure DISM is done for any given PD and further its get notified to RAID.

Issue Description: FW - AMD2P Wave1 - UG bad drive is missing in MR 7.12 FW

Steps To Reproduce:
1. Have one UG bad drive in the enclosure
2. Flash MR 7.10 FW and UG bad drive is coming properly in all app
3. Flash MR 7.12 FW and see that UG bad drive is missing completely in all apps
4. However in PL, it is listing that drive. Please refer the FW log
5. Flash MR 7.10 FW again and see that UG bad drive is coming properly

Please refer the FW log and attached mail for more reference.

Defect ID: DCSG00027855

Headline: pl: NVMe: Write Buffer parameters should be validated against FWUG

Description Of Change: Buffer Offset or Parameter List Length parameters that violate FWUG now cause the Write Buffer command to be failed.

Issue Description: The Buffer Offset and Parameter List Length parameters of a SCSI Write Buffer command sent to an NVMe device aren't validated against the Firmware Update Granularity (FWUG) value reported by the NVMe device.

Steps To Reproduce: Code inspection.

Defect ID: DCSG00027941

Headline: "iop show diag" output collection in CoreDump causes controller to hang

Description Of Change: Updated PL code to not allow adding new entries to the HW Trace-buffer if it is in the paused state

Issue Description: During "iop show diag" execution, we pause the HW Trace buffer to collect its contents. In this paused state, if a new entry is added, it will hang the controller.
CoreDump calls "iopFlashWrite" function to write the compressed HW Trace Buffer data to flash, this calls SPI Write API which caused the hang because it was trying to add debug messages to the paused trace buffer.

Steps To Reproduce: "fault" controller multiple times which will trigger the CoreDump collection multiple times.

Defect ID: DCSG00028298

Headline: Fault 4322 Observed On Sea 8i Board

Description Of Change: Code specific to 3808/3908 was modified to switch the clock to the serdes to the SAS clock which is always present instead of using the hardware default which requires a PDB clock to be present on the board.

Issue Description: The hardware defaults the back end serdes to PCIe mode which requires a valid PDB clock on the board. Code specific to the 3808/3908 8 phy boards requires a valid clock to be routed to the serdes. Since no clock was present, the code detected the error and faulted. The code worked fine on all other 8i phy boards because a PDB clock was present on those boards, but failed on a new board that did not provide the PDB clock input.

Steps To Reproduce: Initialize firmware on Sea 8i board intended for SAS/SATA only use that does not provide a PDB clock.

Defect ID: DCSG00028503

Headline: Application cannot find the CoreDump region size needed to erase the region

Description Of Change: Added new core dump region-specific checks to FW upload and FW download path. These will make sure that the application can use the existing MPI functions to find the region size and perform the erase operation

Issue Description: The new core dump specific checks were missing in FW Upload and Download path

Steps To Reproduce: Requested by ScruitnyCLI team

Defect ID: DCSG00030361

Headline: pl: backend PCIe: endpoint or switch is unexpectedly reset in a couple of error cases

Description Of Change: Ensure that a PL error tracking structure contains AER information before it is interpreted as AER information.

Suppress endpoint reset if an endpoint generates an Unsupported Request error.

Issue Description: If a PCIe memory write transaction is sent to the memory range downstream of a bridge that does not implement Advanced Error Reporting (AER) after the attached endpoint is disconnected, the entire switch is reset.

If a PCIe memory write transaction is sent to the memory range assigned to an endpoint after the endpoint is reset but before the reset condition has been handled, an additional device reset will occur.

Steps To Reproduce: Perform the described tests.

Defect ID: DCSG00031070

Headline: PL: Firmware is incorrectly acking spinup requests twice in a row

Description Of Change: Made a change in spinup request handling to keep track of which new spinup requests were acked, and not ack them again in the retry function.

Issue Description: Firmware is incorrectly acking spinup requests twice in a row, once when an entry is created for a new requests, and in the retry function in the same interrupt context.

Steps To Reproduce: Collect a log of PL spinning up drives.

Defect ID: DCSG00031501

Headline: Increase the number of Fast Training Sequences requested by Aero. (PL)

Description Of Change: Change number of Fast Training Sequences to 0xFF for root port.

Issue Description: When the ASPM L0s feature is enabled on a Link Partner, Aero may initiate recoveries during transitions from L0s to L0 state. This is due to Aero requesting a lower number of Fast Training Sequences than what is required by our receiver in order to achieve Sync during the transitions.

Steps To Reproduce:

When Upstream link to PDB from a drive link is enabled for ASPM L0s and at Gen2 rate, Aero goes into recovery often during the L0s to L0 transitions.
Make sure ASPM L0s is enabled on link.
Check the PCIe traces.

Defect ID: DCSG00031848

Headline: PL: NVMe: Remove MPI26_EVENT_PCIDEV_STAT_RC_SANITIZE_OPERATION_COMPLETED Temporary Event

Description Of Change: Instead of 'MPI26_EVENT_PCIDEV_STAT_RC_SANITIZE_OPERATION_COMPLETED' temporary event, we are now using 'MPI26_EVENT_PCIDEV_STAT_RC_ASYNC_NOTIFICATION' MPI event.

Issue Description: MPI26_EVENT_PCIDEV_STAT_RC_SANITIZE_OPERATION_COMPLETED MPI temporary event communicates the Sanitize complete asynchronous notification from the NVMe drive to MR using a new Event Reason Code "SANITIZE_OPERATION_COMPLETED (0x13)". MR FW is now Polling using Get Log page to check Sanitize Status. Hence, removing this MPI temporary event from PL FW code.

Steps To Reproduce: Initiate Sanitize on a NVMe drive.

Defect ID: DCSG00033003

Headline: Aero/Ventura: Fault 0xD203 - Trace Buffer Manager not in Extended mode when processing diagnostic requests.

Description Of Change: Modified API and internal sizes to match

Issue Description: The internal number of subsystems was smaller than the API number. This resulted in some of the associated arrays data being corrupted if variables nearby were initialized after the trace subsystem.

Steps To Reproduce: Increase the size of the trace subsystem array so that it matches the API size

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Defect ID: DCSG00033019

Headline: [Ventura] SAS/SATA direct attached drive is not listed when VSES disabled in nvata.
Description Of Change: Send the enclosure status change event for direct attached enclosure when vses is disabled.
Issue Description: Enclosure status change event is not sent by firmware to upper layers when vses disabled.
Steps To Reproduce: 1) Disable Vses in nvdata.
2) connect 1 direct attached sas/sata drive.
3) Flash any latest FW.
4) see that drive is listed in pl status but not listed in sg_scan.

Defect ID: DCSG00034100
Headline: Aero DBU Alpha : Driver sends KA , when one of the SMID pending on offline NVMe drive.
Description Of Change: Add logic to send response to host when the TM to a NVME drive based EPD is failed.
Issue Description: On host TM failure on a NVME based EPD, the drive was marked offline without sending response to host.
Host continued to issue TM's until a timeout triggered kill adapter from driver
Steps To Reproduce: Created a NVMe JBOD .
Create and take Snapshot for 8 VM's in a loop
After 5 minutes, NVMe drives enters into offline state.
After few minutes VMWARE driver sends the Kill Adapter (KA)..

Defect ID: DCSG00034356
Headline: Aero A0: Write and DC issues on NVMe drives running data integrity with XMEMCOPY==0 (new boot mode)
Description Of Change: Included DCSG00038206 which fixed a number of issues with ARM MMU related mapping
Also moved timing sensitive PL code and data into OCM
Issue Description: When running with SAS and NVME drives, timeouts and data corruption were observed after a few minutes to an hour under stress.
NOTE: With the normal boot mode (XMEMCOPY==1) these errors do not occur.
Steps To Reproduce: Modify NVDATA default mode from XMEMCOPY=1 to XMEMCOPY=0 in Manufacturing Page 11 and run large depth IO test to NVME for many hours

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Defect ID: DCSG00034467
Headline: [Aero] Upload request for the flash regions like CoreDump/Config1/Config2/SBR/CBB fails with LogInfo code: 0x30010416
Description Of Change: Updated code to return the correct status instead of returning failure.
Issue Description: The function "iopDetermineFwImageSize" was returning "ISTATUS_FAILURE" even when the region is valid and the size has been successfully determined.
Steps To Reproduce: Use Methrat "fwUpload" command to upload various FW regions on Aero.

Defect ID: DCSG00034534
Headline: Aero DBU Alpha: VMWARE OS reported Assert, while running IO's on NVM-E JBOD with DCMD
Description Of Change: During Task management (triggered from VSAN test), any FP diverted to MR FW was completed with status = MFI_STAT_SCSI_DONE_WITH_ERROR and extended status SCSI_GOOD. Change is return SS_CHECK, SN_ABORTED_COMMAND, SA_NO_SEN
Issue Description: Any IO failed with status = MFI_STAT_SCSI_DONE_WITH_ERROR and extended status SCSI_GOOD could be interpreted by VMWARE as good completion. the fix is fail the command with return SS_CHECK, SN_ABORTED_COMMAND, SA_NO_SEN, so OS retry the command later.
Steps To Reproduce: Installed VMWARE ESXi 6.7 U3 Beta OS on SATA pd.
Configured the one NVM-E driver as JBOD.
Performed the Creation, Snapshot of 8 VM'S
During which fired the DCMD command in loop with duration 60 sec.
After few minutes hit with Assert , reported the LSI signature in stack..
Attached the screenshot , fwlog.

Defect ID: DCSG00035015
Headline: Aero3: Uploading main firmware in XmemCopy=0 mode causes an abort
Description Of Change: Modified Aero firmware upload algorithm so that it temporarily unmaps flash code and maps SPI flash when associated regions are requested
Issue Description: Firmware aborts due to access to unmapped SPI flash area
Steps To Reproduce: Upload the main firmware area when XmemCopy==0

Defect ID: DCSG00035111
Headline: Ventura B0: 4 enclosures are created for 2 vSES in multi-UBM config in x8 mode
Description Of Change: Updated FW to limit Enclosure creation and grouping of backplanes only for the HBA connectors detected UBM backplanes.
Issue Description: Additional DA Enclosures (4) are created for multi-UBM config in x8 UBM HFC mode
Steps To Reproduce: With Man Page 46 bits [1:0] set to 1 to enable multi vSES for UBM.
Initialize FW with UBM configured to x8 HFC mode and verify vSES, Enclosure information.
Observe 4 DA Enclosure created instead of 2.

Defect ID: DCSG00035201
Headline: pl: port enable timeout when PCIe and backplane detection are disabled
Description Of Change: Fixed a bug that caused SAS discovery to be held off indefinitely in this case.
Issue Description: If device side PCIe functionality is disabled in Manufacturing Page 9 and backplane detection is disabled in Manufacturing Page 6, port enable times out.
Steps To Reproduce: Disable backplane detection in Manufacturing Page 6 and device side PCIe in Manufacturing Page 9 and bring up the HBA.

Defect ID: DCSG00035753
Headline: Do not create multiple EPDs if the command comes from a user request
Description Of Change: Before creating Enhanced Physical Drive array, check if the request was sent manually by the user. If user request and the PD does not match the drive passed into the function, firmware will skip array configuration
Issue Description: Firmware loops through all PD IDs to check for drives that are configurable as EPD and will create multiple arrays in one routine, however if a user sends the command to configure a specific drive as EPD, firmware should only create one array per PD reference.
Steps To Reproduce: use 2 controllers with same security setting.
1. on ctrl 1, set a SED drive to secure EPD.
2. write data on the secure EPD.
3. move the drive to ctrl 2, set the drive to EPD again.
4. change security key on ctrl 2.
5. write data to the secure EPD.
6. move the drive to ctrl 1.
7. foreign import the drive moved from ctrl 2 using the same security key on the ctrl 2.
8. try to set the imported SED UG drive to EPD.

Defect ID: DCSG00035771
Headline: MR7.13: FW hit "C0:Assertion failure in fw\ddf\ddfConfig.c at line 2403: 0" while doing cablepull/push to trigger auto rebuild
Description Of Change: When any ongoing DDF read is in progress on a drive, DDF RefCOD will be set in use. FW defers any other device insertion in the context of DDF reads until RefCOD is available.
Issue Description: Issue here is when DDF PD Read is in progress, DDF RefCOD is set in use. As a part of current PD DDF read, FW will execute next task picking up from TaskStartNext routine, until DDF read for the current requested PD is completed. Now in TaskStartNext context, let say we pick a task related to PD insertion, FW start to read DDF of new inserted PD using the same refCOD while there is previous read for another PD causing corruption of redCOD memory causing FW to crash.
Steps To Reproduce: Cascading two enclosures to Ventura controller running with FW package 2897.

Create the following steps:

Step Number: 1
Create 3 spanned arrays using 2 enclosures such that the first enclosure is in multipath and the second one is daisy chained without multipath path.

Step Number: 2
Array0: 4 drives R10 (1 drive from each span falls in first enclosure and 2nd drive from each span will fall in 2nd enclosure)
VD0 : 64KB,WT,DIO .
VD1 : 128KB,WB.
VD2 : 512KB,WT,DIO .
VD3 : 64KB,WB.

Step Number: 3
Step Details: Array1 : 8 drives R50 (3 PDs of each span falls on 1st enclosure and rest on other).
VD4 : 128KB,WT,DIO .
VD5 : 256KB,WB .
VD6 : 512KB,WT,DIO .
VD7 : 1024KB,WB .

VD8 : 64KB,WT,DIO .
VD9 : 1MB,WB.

Step Number: 4
Step Details: Array2 : 14 drives R60 (5 drives from each span fall on first enclosure and rest on another)
VD10: 64KB,WT,DIO .
VD11:128KB,WB .
VD12:64KB,WT,DIO .
VD13:128KB,WB .
VD14:256KB,WT,DIO .
VD15:512KB,WB .
VD16:1MB,WT,DIO.

Step Number: 5
Step Details: Run chaos on all the VDs with 10 threads on each.

Step Number: 6
Step Details: Use cable breaker and run cable pull/push script on second enclosure so that drives from second enclosure go off and start rebuilding when connection restored.
Give duration of cable pull/push of 5 mins and run overnight.

==> FW eventually hit ""C0:Assertion failure in fw\ddf\ddfConfig.c at line 2403: 0" while running step 6 above.

Defect ID: DCSG00035833
Headline: Disable DPM for IMR
Description Of Change: Disable the DPM for IMR controller
Issue Description: IMR controller does not have enough memory for DPM. So disable DPM for IMR
Steps To Reproduce: 1. Run Dev BST on iMR controller.
2. Observe "No memory for rh!" crash on the next boot-up.

Defect ID: DCSG00036613
Headline: pl: backend PCIe: Atlas switch may not be discovered
Description Of Change: Handle the absence of the vendor specific messaging capability structure as an allowed condition.

If this issue is encountered, it is also recommended to upgrade the switch firmware to a current version.
Issue Description: If an Atlas switch is connected to Aero and the Atlas switch's firmware does not support the vendor specific messaging capability, PCIe discovery will repeatedly fail to discover the switch.
Steps To Reproduce: Attach an Atlas synthetic mode switch running firmware without the described functionality to Aero.

Defect ID: DCSG00036696
Headline: pl: backend PCIe: 265D fault after deferred max payload size configuration
Description Of Change: Fixed a bug that caused an access of an invalid bridge structure in this scenario.
Issue Description: A 265D fault occurs following deferred max payload size configuration.
Steps To Reproduce: Connect a switch to the HBA and bring it up, then connect a device with a smaller max payload size than is supported by the switch's bridges to the switch.

Defect ID: DCSG00036947
Headline: Ventura_FW : Invalid slot id 255 shown for the PD in the PD Events when powercycle during reconstruction
Description Of Change: Following changes are done in as part of creating a ghost LD.
1) Any operation that is acting on the recon device Id (or related structures) which was referred from the recon structures in the NVRAM should be done only when that particular device is present.
2) If the recon device is not present, do not update the array information with valid recon device Id from the NVRAM, but update it with PD_INVALID.
Issue Description: While recon is in progress, if the system is shutdown and reconstruction drive is removed followed by boot up of the system, the ghost LD creation logic is assuming the recon drive is always present and changes the state of the drive to ONLINE. This is causing the state change events on the pd with invalid slot and enclosure numbers.
In addition to the above, MR FW is also updating the array information with a valid recon device Id(from the NVRAM) without checking the drive presence. This causes an issue for the auto-rebuild operation to kick in once the recon finishes and the original drive is put back.
Steps To Reproduce: 1. Have a Ventura controller with latest FW . Create 10GB R1 VD using PD1 , PD2.
2. Start reconstruction to R5 by adding PD3. Wait for reconstruction to complete 20%.
3. Power of the server(Hard shutdown) , remove PD2 where reconstruction is running and replace it with new drive(PD3)
4. Power on the server , reconstruction resumes , wait for Reconstruction complete.
5. Check the PD events in FW logs for the newly inserted Drive(PD3)
6. Invalid slot id 255 shown for the PD in the PD Events

Defect ID: DCSG00036996
Headline: Aero A0: Atlas switch (SRIS mode) not discovered with Elrond Ex1 config
Description Of Change: Update FW to allow PCIe support enabled for the non-UBM connector Phys when PCIe IO Unit 1 link config specifies SRIS support.
Issue Description: With UBM in the configuration, if other connectors BP_TYPE indicates SGPIO then PCIe support is disabled for the Phys routed on the connector.
Steps To Reproduce: With 9500-16i HBA, attach one of x8 connector quads to UBM backplane and other x8 quads to Atlas PCIe SW. Boot up the HBA and observe no Atlas SW discovered.

Defect ID: DCSG00037801
Headline: After executing "coredumo -erase" from ScrutinyCLI, flash offsets are not reset
Description Of Change: The code was updated to reset the flash offsets in the CoreDump Context data structure to start the next dump from the beginning of the flash region after the CoreDump region erase.
Issue Description: When the CoreDump region is erased, flash offsets in the CoreDump Context data structure are not reset.
Steps To Reproduce: 1. Have some dumps already available in the CoreDump region
2. Issue "coredump -erase" command from ScrutinyCLI
3. Generate the next dump and it will not be collected at the beginning of the flash region

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Defect ID: DCSG00037821
Headline: Backend PCIe link cfg may fail attaching to Ux2 UBM backplane
Description Of Change: Updated UBM link configuration to limit updating the link numbers for connector routed Phys links only.
Issue Description: Backend PCIe link configuration may fail attaching Ux2 UBM backplane to HBA ConnMod 2 and other connectors to non-UBM I2C mode.
Steps To Reproduce: Attach SAS3916 Eval Connector 2 to Ux2 UBM backplane and other connectors SAS JBOD.
Observe, no backend PCIe links configured and Uart PCIe link config cmd displays error "Backend PCIe support DISABLED at runtime (error 12)".

Defect ID: DCSG00037838
Headline: Need PL MPI Device data dumps in "pl dbg" for debug, i.e. "pl mpidev dbg"
Description Of Change: Compiled in the handler for the "pl mpidev dbg" call into the handler for "pl dbg"
Issue Description: Need PL MPI Device data dumps in "pl dbg" for debug, i.e. "pl mpidev dbg"
Steps To Reproduce: Issue "pl dbg" in UART CLI

Defect ID: DCSG00038206
Headline: Aero3: In XMEMCOPY==0 mode writes to config pages get overwritten on next reset
Description Of Change: Misc. fixes to make XMEMCOPY==0 mode compatible
Fixed auto-download algorithm. This caused the firmware to mistakenly believe that firmware was downgraded and would rewrite config pages on every reset.
Fixed firmware upload of config regions. In this mode the ARM MMU was getting confused and not doing Virtual to Physical translations properly.
This included switching to the previously used method of pre-allocating the areas which needed to be changed so table swaps were not necessary.
Fixed some currently unused firmware that disabled caching for the MMU
Added routines to test MMU tables to the CLI
Issue Description: Config pages were being rewritten on every reset.
Steps To Reproduce: Set XMEMCOPY=0 and reboot.
Writing to Manufacturing Page 9 persistent page
Reset
Read Manufacturing Page 9.

Defect ID: DCSG00038289
Headline: pl: backend PCIe: incorrect value written to Device Status/Control register during error handling
Description Of Change: Fixed the described bug.
Issue Description: When PL is clearing non-Advanced Error Reporting errors in a PCIe entity's Device Status register, some settings in the Device Control register are inadvertently cleared as well.
Steps To Reproduce: Perform device pull testing with an Atlas synthetic mode switch.

Defect ID: DCSG00038731
Headline: OS hangs while formatting VDs
Description Of Change: Increased the size of loop index variable to account for IO sizes with PRP Entries greater than 255.
Issue Description: An U8 index variable was used to loop through Prp Entries in an IO to create corresponding IEEE entries to work with DMA.
But when an 1MB IO was received with unaligned elements, the number or PRP entries was 256 causing the conversion loop to run indefinitely.
Steps To Reproduce: Attache two NVMe Ux2 UBM enclosures to 8i
Create max VDs per R0, R6, R5
Fast init
Start formatting VDs

Defect ID: DCSG00038959
Headline: PL: Controller not functional when booting up with 2 Ex1 UBMs in x8 mode
Description Of Change: In the direct attach enclosure creation code that groups HFCs together, made a change to account for this backplane configuration.
Issue Description: In the case of two Ex1 backplanes in x8 mode, the code to create direct attach enclosures can malfunction and get stuck in a loop, causing firmware to hang.
Steps To Reproduce: Attach two Ex1 backplanes in x8 mode and boot up the system.

Defect ID: DCSG00039024
Headline: Ventura B0: PCIe support disabled with UBM and Capella II switch in the topology
Description Of Change: Updated FW proper PCIe link number increment with various BP type attachments mixes to the HBA connectors.
Issue Description: When a non-UBM backplane or PCIe switch is mixed with a UBM BP in the topology, the PCIe link config update fails if HBA Connector 01 has the highest controller Phys routed.
Steps To Reproduce: With 9400-16i HBA, attach UBM to x8 connector quads and Capella-II PCIe switch to other x8 connector quads. Boot up the config and observe no PCIe switch discovered.

Defect ID: DCSG00039263
Headline: pl: NVMe: limit resource frame usage by NVMe IO breakup
Description Of Change: Limited the number of resource frames that may be allocated by NVMe read/write IO breakup.
Issue Description: NVMe read/write IO breakup may consume an excessive number of resource frames.
Steps To Reproduce: Connect 32 NVMe devices to the HBA and run high queue depth large IOs to them.

Defect ID: DCSG00039829
Headline: 9500 Channel board default I2C clock frequency higher than the spec specified
Description Of Change: Updated FW to calculate and set the appropriate clock period required for standard and fast I2C devices.
Issue Description: The 9500-16i channel board default I2C SCL freq probed to be 107.75kHz which exceeds to spec frequency range for standard I2C device.
Steps To Reproduce: Probe 9500-16i HBA I2C SCL line on HBA connector sideband and observe the SCL is around 107.75kHz.

Defect ID: DCSG00039850
Headline: PL Discovery debug prints for Expander Phys/Encl slot enumeration
Description Of Change: Added PL ring buffer prints for Expander Phys/Encl slot enumeration
Issue Description: Ring buffer prints needed for Expander Phys/Encl slot enumeration to aide with debug
Steps To Reproduce: n/a

Defect ID: DCSG00039857
Headline: avoid exception when booting up with more drives than supported.
Description Of Change: In the case that the system has more drives/devices than currently supported max, when user attempts to boot up without removing the extra drives, FW can proceed without exception.
Issue Description: The user has not fixed the extra drive issue yet, if proceed regardless of the critical boot message warning, hit a case causing array index out of bound.
Steps To Reproduce: Add extra drives, power cycle.

Defect ID: DCSG00040422
Headline: 0x6001 Fault while running IOs and cable pull test
Description Of Change: Added a flag to abort the missed IO at a later time when another TM gets started.
Issue Description: 0x6001 Fault occurs because an IO is not aborted by a Task Management. This happens because a TM can't be started when handling a Fast Path exception due to an out of resource condition. Because the TM is not started, the IO is not added to that TMs abort list and gets lost and is not aborted by subsequent TMs.
Steps To Reproduce: Run IOs and pull/push the cable between the controller and the topology

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Defect ID: DCSG00040869
Headline: iMR FW may crash if disabled in device manager when Microsoft OS boots and lock up
Description Of Change: This firmware crash cannot be avoided in this case since host memory is not available. Firmware changes were made to avoid additional crashes at snapdump and thereby avoid controller lockup. Additional code in the snapdump path checks if bus master on the controller is enabled and if it is not enabled FW will spin there to avoid other errors and lock up
Issue Description: OS disables bus mastering and memory enable then place iMR adapter in D3 power management state if the adapter is disabled by user in device manager.
iMR may attempt to access the host mem and triggers a CIB interrupt on that memory access (AXI2Shell access failed) that crashes FW with an asserts().
Snapdump uses host mem, so an attempt to create snapdump will cause additional crashes and lock up the controller
Steps To Reproduce: Disable iMR adapter in device manager.
Reboot OS (this is important, as OS will issue a hibernate DCMD when it it explicitly disabled by user from device manager, but will not do so when host OS reboots.)
Leave system idling.
If iMR FW does not hit assert() within 5 minutes, failure can be induced by accessing snapdump scratch buffer from megamon (di 0x00A00000 0x14)

Defect ID: DCSG00040937
Headline: PL: Remove all MPI 2.6 PCIe event handling and unexpected SAS events from managed switch's MPI Device
Description Of Change: Remove all MPI 2.6 PCIe event handling and unexpected SAS events from managed switch's MPI Device
Issue Description: A managed switch's MPI Device will not sent MPI 2.6 PCIe events, nor will send some MPI 2.6 SAS events.
Steps To Reproduce: None

Defect ID: DCSG00040939
Headline: PL: Adjust the MPI Device support check to only support Atlas's MPI Device
Description Of Change: Adjust the MPI Device support check to only support Atlas's MPI Device
Issue Description: The MPI Device support check in PL allows MPI Devices other than Atlas's
Steps To Reproduce: None

Defect ID: DCSG00040943
Headline: PL: Remove the using of an LMID frame as a request or reply frame to an MPI Device
Description Of Change: Removed code that could allocate and free and use an LMID frame as a request or reply frame to an MPI Device.
Issue Description: There is a compile time feature, which is currently disabled, to use an LMID frame as a request and reply frame to a downstream MPI Device (i.e. Atlas's MPI Device).

This is an obsolete feature, as there are too many sources of problems. So remove this feature from the code, which is no longer used.
Steps To Reproduce: None

Defect ID: DCSG00041605
Headline: Ventura B0: ISTWI Error observed during controller cable management initialization
Description Of Change: Modified FW to prevent certain Cable Mgmt. SM advancement in timer callback and allow advances in ISTWI callbacks.
Issue Description: With the ISTWI IO request callback break up support in IOP, the PL timer callback inadvertently advances the CableMgmt SM causing the SM send out ISTWI request without Bus reservation leading to accessing incorrect connectors SEEPROM's data.
Steps To Reproduce: Connect active cables to 9400-16e HBA and boot up. Observe the ISTWI error info dump in the uart.

Defect ID: DCSG00042025
Headline: Aero Alpha: FW hit assertion failure in fw\hw\debug\binTrc.c at line 1910: !((ext->remove.step > 0) && (ext->add.step > 0)) while OCR during long weekend
Description Of Change: Better accounting was added for free space to avoid growing into the next memory area.
Issue Description: There were cases where a snapdump would grow into the next memory area.
Steps To Reproduce: Run IO with an OCR loop. Each OCR will generate a snapdump.

Defect ID: DCSG00042060
Headline: Aero 7.13 PA1: Ondemand Snapdump does not capture PL Logs
Description Of Change: Update the Ondemand Snapdump function and dump all bitmap to include the PL dump function call
Issue Description: Encl debug dump support was recently added which added a new function in the Snapdump function table.
As a result PL function was shifted down changing its bit position
Steps To Reproduce: Capture run time snapdump with latest package.

Defect ID: DCSG00042890
Headline: Updated GoldenX to handle the CoreDump Region
Description Of Change: GoldenX code updated to handle the CoreDump Region and fill it with 0xFF in the final image
Issue Description: GoldenX code was not updated to handle the new CoreDump Region
Steps To Reproduce: Try to use goldenx with current phase 14 IT firmware

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Defect ID: DCSG00042965
Headline: Allow PCIe IO Unit page 1 link rate debug override option to override BP reported max link rate
Description Of Change: Updated FW to allow PCIe IO Unit page 1 debug override rate option to override the automatically detected rate with the value specified in PCIe IO Unit page 1 control flags.
Issue Description: PCIe IO Unit page 1 physical link rate debug override option allows the user to override the link rate settings automatically generated from UBM BP settings but it limits the speed to lesser of BP settings or debug override rate values.
Steps To Reproduce: None

Defect ID: DCSG00043038
Headline: Controller boot does not proceed after DISM
Description Of Change: Added safe guard in FW to avoid DMD handling if the device DISM is not complete.
Issue Description: DMD handling is added and expectation from PL is DMD events are not supposed to come during boot but it does not come in certain cases. FW does not handle this unexpected DMD events before DISM.
Steps To Reproduce: Do double dip

Defect ID: DCSG00043070
Headline: ExtTTYWrite will Infinite Loop if buff only Contains '\n\0'
Description Of Change: As messages are printed, they are scanned for \n characters to insert date/time prefixes. That code was updated to recognize single character prints for \n and \0.
Issue Description: Printing '\n' and '\0' characters resulted in infinite loops.
Steps To Reproduce: Build firmware that would execute these statements:

```
etprintf("%c", '\n')

etprintf("%c", '\0')
```

Defect ID: DCSG00043119
Headline: Coredump text files don't have file extensions
Description Of Change: Added ".txt" extension for the CLI output file generated by the coredump.
Issue Description: CoreDump added files to the zip without any extension.
Steps To Reproduce: Unzip coredump files. Click on one. Since there are no file extensions they are not pulled up on an editor.

Defect ID: DCSG00043379
Headline: Update OEM specific jbod bst script
Description Of Change: Removed wrong personality change at start of script. Also removed resume related changes.
Issue Description: Personality was getting changed to wrong mode in script.
Steps To Reproduce: Start jbod testing script.
Error occurs as wrong personality is changed.

Defect ID: DCSG00043514
Headline: Coverity Bugs in PL Enclosure Management Files
Description Of Change: Fixed the issues reported by Coverity tool
Issue Description: FW issues identified by Coverity code inspection tool
Steps To Reproduce: Coverity code inspection

Defect ID: DCSG00043549
Headline: 7.13 BST Failure: Data Abort During First Restore of COL BST
Description Of Change: Created temporary buffers for string manipulation routines to avoid permission faults to non-writable memory.
Issue Description: During first restore, a processor exception occurs.
Steps To Reproduce:
1. Run COL BST.
2. Observe processor exception on first restore.

Defect ID: DCSG00043589
Headline: Remove erroneous successful event if no foreign configuration is deleted at storcli command.
Description Of Change: check the number of PDs that got foreign config cleared, if it is 0, do not generate configuration cleared event.
Issue Description: An event of successful clear of foreign configuration is generated regardless of the actual clear status.
Steps To Reproduce: Use a locked drive, use storcli /c0/fall delete to try to delete foreign configure.

Defect ID: DCSG00043616
Headline: PL: SMP Timeouts During Expander Phy Reset Test
Description Of Change: Enable the DMA activate timeout interrupt in SAS Tx context manager and set the timeout to 1 second. For the interrupt handling, perform Tx transport cleanup so that the hardware is freed up to work on something else.
Issue Description: SAS Tx hardware can get stuck waiting on a SATA DMA activate FIS that is not coming. This can happen to all available SAS Tx units at once, which means nothing is being sent on the SAS wire, leading to SMP and IO timeouts.
Steps To Reproduce: Use a topology with cascaded expanders and only a x4 connection from controller to the first expander. Each expander should have a combination of SAS and SATA drives attached. Send SMP passthrough requests to the controller to reset random expander phys while running IO to the drives. SMP failure is expected at the test level.

Defect ID: DCSG00043746
Headline: Removing minimum capacitance check from the supercap code
Description Of Change: removing minimum capacitance check from the supercap code
Issue Description: Board group recommends removing minimum capacitance check from the supercap code.
This check has resulted in offload not being sustainable.
Steps To Reproduce: N/A

Defect ID: DCSG00043881
Headline: Bug in SerDes M0 Code U16RegDataFindReplace()
Description Of Change: A bug in the M0 code that manages the SerDes in the U16RegDataFindReplace() was fixed. Pull in new M0 code with fix.
Issue Description: U16RegDataFindReplace() was not masking data properly.
Steps To Reproduce: N/A. Found by code inspection.

Defect ID: DCSG00044316
Headline: Fix supercap/battery code so it process monitoring out of 2nd cpu core
Description Of Change: Add support to direct BBU monitoring to the 2nd CPU core.
Issue Description: Current code is running the monitoring out of primary cpu core, its resulting in performance degradation as its taking away from primary task processing.
Steps To Reproduce: Current BBU monitoring code is happening in primary CPU core.

Defect ID: DCSG00044331
Headline: coverity defect - non critical defects
Description Of Change: 1. MR FW incorrectly interpreting pliRegister return values. Use ISTATUS as the type.
2. If a host IO spans over 2TB size, FW may miss streaming detection as we were using U32 for LBA. Use U64 for LBA
Issue Description: 1. MR FW incorrectly interpreting return values from a device unregistration function. This is not an issue in the current implementation but using the right status data structure would avoid future errors.
2. Second issue was more on performance where if a host IO spans over 2TB size, FW may miss streaming detection as we were using U32 for LBA.
Steps To Reproduce: -

Defect ID: DCSG00045063
Headline: Aero MR7.13-PA2: PL Fault 0000d213 (Assertion failure in fw\dm\pl3.5\pliopi.c at line 1269) when running driver load/unload SAL script on RHEL 7.6 x64
Description Of Change: To switch back to normal (non extended) mode, MR FW shall do a control request with PLI_CTRL_REQ_OPERATION_TBM_RELEASE_EXT_BUFFER when driver shuts down.
Issue Description: The Aero DVT 9580-8i8e hit the PL Fault d213 when running the certified driver load/unload SAL script on RHEL 7.6 x64.
Steps To Reproduce: This issue can be easily reproduced by unloading the driver and reloading it back. In windows to reproduce the issue, do disable the controller and enable it back. This will result in unloading the driver and reloading it back

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Defect ID: DCSG00045441
Headline: Aero 7.13 PA1: Kill Adapter Snapdump does not capture Frame and other IO information
Description Of Change: Correct the Encl dump function entry in the SnapDumpTable to match the module base index.
Issue Description: Encl debug dump function was added in the middle of the dump function table which was causing wrong index calculation for driver OCR based snapdump case.
The driver index calculated was wrong which made it pick up function bitmap for ONFI and RMC only, resulting in not capturing all debug info.
Steps To Reproduce: Generate kill adapter based snapdump and check for the snapdump contents.

Defect ID: DCSG00045450
Headline: Aero A0: Fault D033 running IO + Expander Phy Link/Hard Resets to Expander phys
Description Of Change: Configure the IO accelerator (IOA) to SAS core queueing mechanism to use the threshold queuing mechanism.
Issue Description: A D033 or 7C55 fault is observed when running IO + expander phy resets. This is ultimately due a hang condition that occurs in the control queue queuing mechanism from the IO accelerator (IOA) to SAS core.
Steps To Reproduce: Use a mixed SAS/SATA topology behind a specific expander. Run IO to the drives and perform random phy resets on the expander phys.

Defect ID: DCSG00045474
Headline: FW crashed with Exception handler error at bios post while booting up with Multipath config
Description Of Change: BBU boot messages are converted to Cache Vault messages at reboot. These boot messages are static text in flash. FW logic was trying to convert these messages in flash which caused the crash. Logic is changed to copy the message in the local memory before converting them.
Issue Description: FW crashed with Exception handler error at bios post while booting up with Multipath config.
Steps To Reproduce: Just reboot the system and FW crashes with Exception handler error at bios post while booting up with Multipath config

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Defect ID: DCSG00046697
Headline: Remove 'thread 0 is reporting error' message
Description Of Change: Removing log message which is misleading.
Issue Description: We are reading the offload metadata block before we determine if its erased or not.
Because its erased this print is coming.
When a block is erased, the controller will report uncorrectable ECC error because the erase operations sets all bits to '1', and the ecc check bits are not set.
The ecc check bits are only set during program operation.
The "thread reporting error' should be removed.
Steps To Reproduce: After erasing all the blocks on the NAND flash part, do power cycle, and look for message in log.

Defect ID: DCSG00047643
Headline: Bug Fix In get CERT and While reading the certificate from the client
Description Of Change: Data type changed to account for buffer size.
Transfer length for get certificate is calculated based on input buffer size.
Issue Description: Internal issue discovered during code walk through
Steps To Reproduce: NA.

Defect ID: DCSG00047720
Headline: Lot of SES related prints in the FW log
Description Of Change: Masked the prints which doesn't add value to be displayed on the terminal log
Issue Description: A lot of SES related prints are seen on the terminal
Steps To Reproduce: Attach Aero MR adapter to Atlas and reboot

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Defect ID: DCSG00048021
Headline: Aero : Task Management timeout results in Kill Adapter while running IO's on 4K JBOD
Description Of Change: Break out of the EPD IO processing loop if TM is active on that EPD
Issue Description: EPD IO's are processed in a loop. If TM is active on EPD then IO is added back to host queue
But the loop logic runs till IO's are present in the host queue causing FW to loop indefinitely resulting in KA .
Steps To Reproduce: Create a 4K jbod on Aero card
Start a script to create 6 VM's and snapshot with a duration of 7200 sec.
After 5-10 minutes , kill adapter is seen.

Defect ID: DCSG00048491
Headline: Total Device count mismatch
Description Of Change: The variable is decremented as and when DISM is failed on the device.
Issue Description: gDevCount variable which reflects the total number of devices in the device list has been not accounted for failures in the context of DISM

Steps To Reproduce: On controller 1, enable persistent reservation on SAS drive following steps here -> https://www.thegeekdiary.com/understanding-linux-scsi-reservation/

Move the drive to controller 2 and restart the controller.

Defect ID: DCSG00048576
Headline: Patrol Read fails to run on all the online drives when iteration count > 1 and PR maxconcurrentpds < online-drive-count
Description Of Change: While starting patrol read operation, all eligible physical drives patrol read status is marked ready.
Issue Description: When patrol read is started on the controller, patrol read operation starts on only maximum allowed concurrent PDs and remaining online drives are ignored for patrol read operation.
Steps To Reproduce: Clear NVRAM.- Powercycle

Set PR maxconcurrentpds = 13 using storcli

Perform the test described in Reproduce Info . See if PR runs on the remaining 10 drives after the first 13 completes - Works as expected

wait for pr to completed on all 23 drives - PR Complete on all the 23 drives

repeat the test again without clearing NVRAM - PR starts only on first 13 drives and never kicks for the other 10 online drives .

Defect ID: DCSG00048634
Headline: PLDM FW UPDT component classification needs to be changed for MR ROP
Description Of Change: PLDM FW UPDT component classification. MR ROP includes all the FW, BIOS/UEFI in a single package. Hence, the classification should be 'Software Bundle(0x000D)'
Issue Description: PLDM FW UPDT component classification needs to be changed for MR ROP
Steps To Reproduce: 1. Wait for PLDM discovery.
2. Check the 'Firmware' section under MR card inventory.

Defect ID: DCSG00048692
Headline: iMR Ventura: R0 PD becomes UGUnsp instead of Online after system reboot.
Description Of Change: During drive insertion process at reboot when a drive is present in PD Fail History, this drive should be treated as bad drive and should not be counted for configurable PD count. FW logic was counting the drive present in PD Fail History for configurable PD count. This was causing Max allowed configurable PD count to exceed the limits and blocking good configured PDs to be part of the configuration.
Modified FW logic to bypass counting bad drives present in PD Fail History for configurable PD count.
Issue Description: The R0 PD created in step #4 becomes UGUnsp instead of staying Online after the system reboots in step #6.
Steps To Reproduce: TestCaseName: iMR : drive with DDF gets marked unsupported unconfigured bad in max 32 VD scenario
Description: When the supported configurable PD count is already filled and configured drives are added on top of this.
The added configured drive will get marked as unsupported and unconfigured bad so that the data on the drive is saved.

Step Number: 1
Step Details: Note: Keep maintain PD fail history ON and JBOD enabled.

Create 32 single drive R0.

Step Number: 2
Step Details: Create few JBODs

Step Number: 3
Step Details: Remove one of configured drive so that there are 31 VDs.

Step Number: 4
Step Details: Create another single drive R0 by undoing a JBOD.

Step Number: 5
Step Details: Trigger OCR.

Step Number: 6
Step Details: After OCR, insert back the removed drive.

Step Number: 7
Step Details: Remove another configured drive.
Step Expected Result: Unsupported drive becomes supported.

Step Number: 8
Step Details: Change the supported unconfigured bad drive to unconfigured good drive and import.
Step Expected Result: VD is imported.

Defect ID: DCSG00048725
Headline: Added Discovery Notify when controller boot up or reset.
Description Of Change: Full solution will be MR initiate Discovery Notify with NULL EID, BMC pick up this message and re-initiate MCTP discovery.
IT today is already issuing Discovery Notify while reset.
Issue Description: With Customer BMC, if controller do an OCR, BMC does not re-initiate MCTP discovery.
This results in OOB MCTP packet drop by MR FW.
Steps To Reproduce: 1. With OOB communication enabled, do OCR.
2. Issue any dcmd through OOB, seeing dcmd failed.

Defect ID: DCSG00048879
Headline: DMA test result status need to be corrected for OOB runs
Description Of Change: For the OOB runs there is no DMA tests involved. But the event got logged without checking any checks to prevent it.
Check added to prevent to logging the event for the diag test not run cases.
Issue Description: In the OOB Diag test runs, there is no test ran for DMA. But the event log shows incorrectly those DMA test were conducted.
Filter added to prevent such not correct event log.
Steps To Reproduce: 1. Here DMA test shows as test completed, if test completed then there should be corresponding counts.
2. Else if test completed count is 0, then stating passes successfully needs to be corrected.

Defect ID: DCSG00050349
Headline: PLDM FW UPDT component classification needs to be changed for MR ROP
Description Of Change: PLDM FW UPDT component classification. MR ROP includes all the FW, BIOS/UEFI in a single package. Hence, the classification should be 'Software Bundle(0x000D)'
Issue Description: PLDM FW UPDT component classification needs to be changed for MR ROP
Steps To Reproduce: 1. Wait for PLDM discovery.
2. Check the 'Firmware' section under MR card inventory.

Defect ID: DCSG00051124
Headline: IOP: Trace buffer image has extra "CFG string
Description Of Change: Corrected a check that incorrectly caused a 4th string set to be uploaded to the host's trace buffer when processing an MPI Diagnostic Buffer Post request. This happened to be old data for the CFGI strings.
Issue Description: Trace buffer image has extra "CFG string when uploaded to the host.
Steps To Reproduce: Register, release, and read a trace buffer using a host tool like ScrutinyCLI.

Defect ID: DCSG00051251
Headline: No Bad Phy reported after inserting a simulated Bad drive
Description Of Change: - Added code to force status page parsing from vSES if the page changes
- Added code to bypass bad phy reporting if the status of an element is UNKNOWN with invalid bit set in the phy descriptor

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Issue Description: No Bad Phy reported after inserting a simulated Bad drive

Steps To Reproduce: Windows 2016
Driver 7.713.04.00
FW package 2984

Attached UBM enclosure to DVT 16i
Insert a simulated Bad Phy drive
Wait for 10 mins to see the event

Defect ID: DCSG00051696

Headline: Retention test is not invalidating ONFI image immediatley after deallocating data cache

Description Of Change: When retention test is deallocating data cache, it should immediately invalidate the ONFI image.

Issue Description: There is a assertion when data cache is initialized because there is no memory available in data cache
This is happening because the Retention test is not freeing the data cache memory used for running the test.

Steps To Reproduce: (1) start retentiontest
(2) reboot
(3) there is an offload/restore.
(4) retentiontest is verified, and data cache is freed
(5) reboot
(6) there is a restore of the data cache back at step (3)
(7) retentiontest did not verify the data as flags were cleared on previous step (4) above. The data cache is not freed.
(8) There is an assertion during init cache because there is no memory available in data cache

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Defect ID: DCSG00052153

Headline: MR_7.13 PA2 DBU : Multiple VM's power on/shutdown on NVM-E result to Exception Handler Called for Processor Core = 0

Description Of Change: Pull in the chained MID for DMDouble buffer processing.

Issue Description: Since the chained MID is not pulled, data was transfer to wrong address causing an ASSERT.

Steps To Reproduce: As per e-mail communication extension of this defect fix DCSG00033062
Originally issue seen on 10 Hour , after defect fix issue run time extended to some more hour ..As per Dev analysis it need lot changes in the code path ..

This issue seen on VMWARE OS.
Created the R0 using four NVM-E drives with properties of WT/NORA/DI0/64KB
Run the script which create the VM's and perform the Power on/off with a different combination of CPU's and memory.
Simultaneously running attached DCMD script which performs vd policy change in a loop.
After 10 hour FW Crash with below lines..

ERROR: Exception Handler Called for Processor Core = 0
Data Abort exception handler was called
Exception due to executing THUMB instruction 0x7be0 at address 0x013bfb82
Exception due to data access at address 0x7000000f
Exception Reason: Translation Fault Level 2 LONG on Int READ
Exception Handler Return address 0x013bfc29

Current Program Mode Info:
CPSR = 800001d7
LR = f8401951
SP = 7fdd9f50
Processor Mode = Abort
Execution State = ARM
Asyn Abort Mask = 1
IRQ Mask = 1
FIQ Mask = 1

Defect ID: DCSG00052179

Headline: Sea 16e PCIe TX Compliance Test Failure

Description Of Change: Modified the build process to update the PSW firmware in the RMC to that which is stored in the binary file stored in the firmware project. This will ensure that both Aero and Sea are running the same firmware and provide and easier upgrade path.

Issue Description: The Protocol Test Compliance test was failing test 58-10 and 58-11 because the Sea controller was rejecting the P10 request during training/equalization.

Steps To Reproduce: Run the Protocol Test Compliance test from the PCI SIG.

Defect ID: DCSG00052207

Headline: move ETTY code from binTrc.c to extTTY.c

Description Of Change: Some ETTY code was moved from binTrc.c to extTTY.c.

Issue Description: There are naming conventions for firmware. This code needs to be moved to comply with the convention.

Steps To Reproduce: Source code inspection.

Defect ID: DCSG00052870

Headline: Flash Filesystem Refresh failed

Description Of Change: The code preforming the Flash Filesystem Refresh is modified to put all the blocks in free state in advance of the refresh.

Issue Description: The Flash Filesystem Refresh occurred because the system time changed by at least one year into future.
Flash Filesystem Refresh failed because there were not enough blocks in the free state.
All the blocks in the first and second offload region were in allocated state when the Flash Filesystem Refresh was requested, not leaving enough blocks available to perform the operation.

Steps To Reproduce: (1) kick off an offload by arming for offload then do cold reboot.
(2) change windows system time by at least one year in future
(3) warm reboot
(4) during next bootup, there is an assertion.

Defect ID: DCSG00052904

Headline: A lot of unexplained prints about PD Fail history seen in during FW boot

Description Of Change: Different offsets were generated for same nvram field due to run time padding of one of the structure within nvram structure. Added explicit padding in nvram to avoid different run time offsets for same field.

Issue Description: Run time padding was generating different offsets from different files for same nvram field. This was causing one word corruption in nvram.

Steps To Reproduce: * Select controller with macronix flash part.
* Boot and perform regular FW operations which generates lot of events. There should be atleast one erase/write to nor flash.
* Reboot
* Look for 'Nvram Checksum Invalid - Initializing' print during FW boot.

Defect ID: DCSG00053406

Headline: Fix Static Analysis reported issue #46175 in Aero Project

Description Of Change: Explicit casts were added when building a trace entry.

Issue Description: The static code analysis tool does not understand that the size values in the trace are always small. It believes an assignment will discard some bits.

Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00053409

Headline: Fix SPDM library for Get_Digest, Challenge.

Description Of Change: 1. Change Challenge Sig buffer size to allow ECDSA signature signing.
2. Correct Challenge signing buffer and size
3. Correct Digest response code.

Issue Description: Additional fix to make Get_Digest, Challenge working on SPDM library.

Steps To Reproduce: Issue get_digest or challenge from emulator, request fail by the SPDM library.

Defect ID: DCSG00053641

Headline: Allow secure PDs to be configured as Enhanced Physical Drive after PD is unlocked

Description Of Change: Clear EPD flag that does not allow drive to be auto configured after the PD is unlocked with correct security key

Issue Description: Firmware sets a bit to not allow drives to be auto configured as EPD if the configuration is foreign, so firmware must clear it if the PD is unlocked by way of the import command

Steps To Reproduce: use 2 controllers with same security setting.
1. on ctrl 1, set a SED drive to secure EPD

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2. move the drive to ctrl 2
3. change security key on ctrl 2
4. delete config on ctrl2
5. move the drive to ctrl 1, observe that PD is UGOOD Foreign
6. restart ctrl 1
7. foreign import the drive moved from ctrl 2 using the same security key on the ctrl 2
8. observe doNotAutoConfigureAsEPD flag is still set on that PD

Defect ID: DCSG00053674
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Update code so its not converting to narrower types.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00053709
Headline: smart recovery start pointer issue
Description Of Change: Program the new start pointer into offload wrapper following the condition when there was an adjustment.
Issue Description: When adjusting the smart recovery start pointer following smart recovery, the code is not programming new start pointer into offload wrapper.
Steps To Reproduce: inject smart recovery using megamon command
arm for offload
power cycle
arm for offload
power cycle
observe smart recovery start block using megamon command

Defect ID: DCSG00053711
Headline: Change boot loader version to 32 bit field
Description Of Change: Change boot loader version to a 32 bit field
Also add check for boot loader version for the expected supported version.
Issue Description: The boot loader version passed into firmware is 32 bit.
Firmware was copying the version passed into firmware into 8 bit fields.
Steps To Reproduce: Static Analysis Tool found the issue.

Defect ID: DCSG00053777
Headline: Fix Spdm Client logic
Description Of Change: 1. Fix tagowner bit for SPDM response.
2. Change logic to print buffer information.
Issue Description: Tag-owner bit of MCTP is not set correctly.
Steps To Reproduce: None

Defect ID: DCSG00054062
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Change field from U8 to U32
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue.

Defect ID: DCSG00054081
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Change field from U8 to U32
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue.

Defect ID: DCSG00054162
Headline: Fix Static Analysis reported issue #46155 #46132 #46115 in Aero Project
Description Of Change: The size types were made larger.
Issue Description: Some of the size types in the binary trace code are small due to the current print usage. The tool identified some inconsistencies with small and large types that could be a problem when printing long strings.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054386
Headline: Fix Static Analysis reported issue #46173 in Aero Project
Description Of Change: The current products only have 2 processors, so the value was casted. A static assert was added in case this code is reused in future products.
Issue Description: Static code analysis identified that a 4 byte processor id value was being assigned to a 2 byte field.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054389
Headline: Fix Static Analysis reported issue #46081 in Aero Project
Description Of Change: Casting was used to remove sign ambiguities.
Issue Description: The static code analysis tool pointed out a few inconsistent uses of signed and unsigned.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054500
Headline: Disable CoreDump when Flash device is not present
Description Of Change: During Coredump initialization, added a check to see if the flash device is present. If not, do not enable the coredump.
Issue Description: When there is no flash device present, core dump feature should not be enabled by the FW.
Steps To Reproduce: Load the FW on a board without the flash memory.

Defect ID: DCSG00054554
Headline: Fix Static Analysis reported issue 47315 in Aero Project
Description Of Change: Explicitly convert wider type unsigned short, to narrower type unsigned char.
Issue Description: Static analysis tool identified implicit conversion of an expression to a narrower type.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054556
Headline: Fix Static Analysis reported issue 47293 47290 47283 in Aero Project
Description Of Change: Make changes for the function parameters data type
Issue Description: integer_narrowing_conversion: pass the parameter data type U64 to U32 type
Steps To Reproduce: Run static code analysis tools

Defect ID: DCSG00054558
Headline: Fix Static Analysis reported issue 47281 47276 in Aero Project
Description Of Change: casting the input parameters to the right type.
Issue Description: Integer conversion value may be different than the original value, causing incorrect computations.
Steps To Reproduce: Run static code analysis tools

Defect ID: DCSG00054560
Headline: Fix Static Analysis reported issue 47268, 46980 46977 i in Aero Project. They are PD and LD variable defects
Description Of Change: Convert wider type, unsigned int, to raid typedefs
Issue Description: Static analysis tool identified implicit conversion of an expression to a narrower type.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054562
Headline: Fix Static Analysis reported issue of data type implicit conversion.
Description Of Change: Use explicit type conversion instead of implicit type conversion.
Issue Description: Data type mismatch causing implicit type conversion from u64 to uint.
Steps To Reproduce: Use Static Analysis Tool.

Defect ID: DCSG00054850
Headline: Fix Static Analysis reported issue 47110 47108 in Aero Project. They are VisionFirmwareDownload defects
Description Of Change: Explicitly convert wider type unsigned int to narrower type unsigned short.
Issue Description: Static analysis tool identified implicit conversion of an expression to a narrower type.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054851
Headline: Fix Static Analysis reported issue 46759 in Aero Project
Description Of Change: casting the input parameters to the right type.
Issue Description: Ulong conversion value may be different than the original value, causing incorrect computations.
Steps To Reproduce: Run static code analysis tools

Defect ID: DCSG00054852
Headline: Fix Static Analysis reported issue 46685 46283 46274 46111 in Aero Project
Description Of Change: casting the input parameters to the right type. casting U16 to uchar.
Issue Description: ushort conversion value may be different than the original value, causing incorrect computations.
Steps To Reproduce: Run static code analysis tools

Defect ID: DCSG00054864
Headline: Fix Static Analysis reported issue 46716 in Aero Project
Description Of Change: Casting was used to remove implicit integer conversion.
Issue Description: The static code analysis tool pointed out that there was a conversion to a narrower type without a cast.
Steps To Reproduce: Run static code analysis tools.

Defect ID: DCSG00054867
Headline: Offload was not sustainable
Description Of Change: The algorithm for determining the minimum voltage required for offload was modified.
The calculation for voltage drop as a result of the equivalent series resistance was incorrect.
An additional check on fully charge bit was added.
Issue Description: The voltage dropped below the minimum voltage required for offload.
Steps To Reproduce: The issue was reproduced at customer site. They did an initial learn cycle which succeeds, then after several boots it started failing.

Defect ID: DCSG00054923
Headline: SPILIB: New Version of Winbond SPI flash times out on write
Description Of Change: Modified reaction to the clearing of bits in the 4 byte parameter block.
Previously if the chip had a 4 byte parameter block but did not support 4 byte commands the library would fail the chip
The new action is to guess what kind of command to use using the size of the flash
Issue Description: SPILIB either used the wrong code (4 byte code) or failed the flash discovery entirely depending on the version of the library due to the addition of a 4 byte parameter block on a chip that does support 4 byte commands
Steps To Reproduce: Place the most recent revision of Winbond W25Q128JW chip on a Aero or Ventura board and attempt to initialized it
NOTE! Previous revisions of the same chip will work and currently there is no way to verify revisions of chips as it is expected they remain exactly the same.

Defect ID: DCSG00055385
Headline: Implicitly converting and expression to a narrower type
Description Of Change: Fixed static analysis tool issues flagged as "Implicitly converting and expression to a narrower type"
Also fixed a bug in the CoarseDelayCtrl calculation (struct member CrseCtrl was 4 bits in Ventura (mask with 0xF) - CrseCtrl is 5 bits in Aero and requires mask 0x1F.
Also, the mask and addition/subtraction was replaced with a ternary operator because the intent is to increment up to 0x1F and down to 0x0 (never past these).
Issue Description: issues flagged by static analysis tool
Steps To Reproduce: re-run static analysis tool

Defect ID: DCSG00055393
Headline: Make Challenge Buffer Include Get_Digest/Digest, Get_Cert/Cert
Description Of Change: Initially, challenge buffer with contiguous memory.
Logic is changed to support more flexible challenge buffer.
Challenge buffer also include digest/cert if both request is done when processing challenge request.
Issue Description: Issue Challenge request, only see version/cap/negotiate request/response include in the challenge buffer.
Steps To Reproduce: Issue Challenge request, only see version/cap/negotiate request/response include in the challenge buffer.

Defect ID: DCSG00055398
Headline: COL source code fixes in response to static analysis tool analysis
Description Of Change: miscellaeous fixes related to integer_narrowing_conversion
Issue Description: static analysis tool findings
Steps To Reproduce: run static analysis tool

Defect ID: DCSG00055415
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Update code so its not converting to narrower types.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00055451
Headline: Diagnostic test command memory allocation failure is not handled gracefully
Description Of Change: If diagnostic init command fail due to non-availability of scratch memory. Proper freeing up of the resources were not performed.
Issue Description: Firmware changes were made to handle diagnostic initialization failure.
Steps To Reproduce: Fail the diagnostic initialization and the test can be reproduced. Development team simulated this failure using test code and verified fix

Please follow reproduction steps of DCSG00048847 to test in the field

Observing Data Abort exception in the following scenario:
1. Create a R1 VD from host and start IOs using Chaos.
2. From OOB start StartSelfCheckDiagnostics for duration 300 seconds.
3. Observe that after around 240 seconds controller hits Data Abort exception

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Defect ID: DCSG00055790
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Changed all locally declared U32 parameters in this function to U16.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00055917
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Update code so its not converting to narrower types.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00056067
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Update code so its not converting to narrower types.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00056313
Headline: OEM DCMD error when executed SelfDiag test from OOB in I2C mode
Description Of Change: Enabled OOB controller self diagnostic test in I2C mode.
Issue Description: OOB controller self diagnostic test was blocked in FW in I2C mode, by designed until now. OEM requested it be enabled.
Steps To Reproduce: Set the controller OOB mode to I2C.
Enter to BMC shell and launch SLT.
Select: Controller Menu -> StartSelfCheckDiagnostics and enter 15 seconds as the test duration.

Observe that immediately: error 2 is seen .

Defect ID: DCSG00057140
Headline: MR_7.13 OEM :Assertion failure in fw\hw\pbam\serial.c at line 1614 observed while Create/delete Vd's with 4K drives
Description Of Change: Firmware changes made to avoid global variables being accessed from different cores at the same time.
Issue Description: We have noticed the Semaphore is initialized to zero in this issue and the function that causes the issue is called with out any processor synchronization. Global variables are accessed in the function from both the cores at the same time and that could cause unwanted results in the FW. We have done additional reviews of Semaphore implementation and its usage. It looks good so far and the reproduction of the issue is not happening in the same system where the issue happened.
Steps To Reproduce: 1) Create 16 Vd's R5 with 4 nos 4K drives WB
2)Create 16 Vd's R6 with 3 nos 512B SAS drives WB
3) Create 16 Vd's R1 with 2 nos 512B SAS drives WB
4) Start and Mount on all 48 VD's (chaos)
5) Start a script of create/delete 16 Vd's R0 with 1 Nos 4K drive
6) Start a script of JBOD create/delete of 5 drives
7) Start a script of CC and PR start/stop
{storcli64.exe /call stop pr
storcli64.exe /call/vall start cc force
timeout 90
storcli64.exe /call/vall stop cc
storcli64.exe /call start pr
timeout 5}

Defect ID: DCSG00057254
Headline: ED91 Fault while running IOs + OCR (controller reset) testing
Description Of Change: Made changes to read the link state from a different register that provides an accurate value. And updated the work around to included the missing step.
Issue Description: A HW workaround was determining the link state by reading a register that has been found to not always be accurate. In addition, part of the workaround was missing an important step in one code path. This was probably the real cause of the controller fault.
Steps To Reproduce: Run IOs while running a controller reset loop at the same time. If timings work out, the ED91 fault will occur.

Defect ID: DCSG00057268
Headline: PCIe OOB maxpacketsize value wrongly displayed from storcli application
Description Of Change: As part of OOB initialization firmware assigned the wrong PCIe OOB maxpacketsize value and causing this issue.
Made the required code changes and assigning the valid values.
Issue Description: As part of OOB initialization firmware assigned the wrong PCIe OOB maxpacketsize value and causing this issue.
Steps To Reproduce: 1 From Megamon execute below mentioned command
- Cn
- Call clear_nvram
2 Power cycle the system

Defect ID: DCSG00057795
Headline: Dev Defect to Fix Some Code Maintenance Issues
Description Of Change: Code changes were made to fix code review defects
Issue Description: Code review defects
Steps To Reproduce: NA

Defect ID: DCSG00057863
Headline: SPI controller hang
Description Of Change: A local copy of the NVRAM bbu properties structure will be maintained in DDR.
The supercap monitoring task is going to read from the DDR copy instead of NVRAM copy.
When changes are needed in that structure, then nvram intercore requests are sent to update the NVRAM copy.
Issue Description: The SPI controller hang when NVRAM access in 2nd CPU core is happens at same time when NOR FLASH access on first CPU core.
There is known issue on ventura where a potential hang in SPI controller could occur when multiple access's in nvram and flash happen at same time.
Steps To Reproduce: Cache offload test case ran over several days.

Defect ID: DCSG00058512
Headline: ePDS/JBODs not getting created and deleted properly in the test script. Also personality change code needs improvement.
Description Of Change: ePDs and Raid vds are added separately for jbod bst script. Also for both jbod and raid bsts personality check is made and then change is done if needed.
Issue Description: In bst scripts, for this OEM stream, same systems are used for both jbod and raid mode tests. Also both tests are supposed to be performed on every bst. Hence personality change (and a subsequent reboot) is required before start of each test to get the controller in correct personality.
Apart from this, in jbod test, there should be jbods (ePDs) as well as some raided virtual disks. Hence some drives are used for raid virtual drives and some should be added as ePDs.
Steps To Reproduce: Run the bst via ROPs.
Issues are seen in the script logs.

Defect ID: DCSG00058690
Headline: Invalid cache line caused exception
Description Of Change: skip cache line if it is invalid
Issue Description: When trying determine if need to pin a cache line, an invalid cache line caused exception.
Steps To Reproduce: Follow test steps.

Defect ID: DCSG00058905
Headline: Remove the 'NVCache device failed" message when there is no supercap
Description Of Change: For the message in question, a different API is used for inhibiting the "NVCache device failed' message when there is no supercap.
TTY History operations are now allowed when there is no supercap, previously not allowed.
BBU retention test will observe a different message when there is no supercap.
Issue Description: The request is to remove the "NVCache device failed' message when no supercap is present.
Its believed this message is misleading to the customer.
Steps To Reproduce: Remove supercap from board and power cycle system.
Observe messages in question.

Defect ID: DCSG00059689
Headline: Fix misspelling in print statement
Description Of Change: Fixed misspellings in print statement and comments throughout file
Issue Description: Misspelled Fault print was observed
Steps To Reproduce: Break into Megamon while IO is running and do not exit until 15 seconds before OCR occurs, usually ~3 min 45 seconds.
KA occurs and this message is in the TTY logs

Defect ID: DCSG00060769
Headline: On Linux: Unable to write SAS address update record to persistent region of the flash via sg_write_buffer
Description Of Change: In the logic handling GET_TARGET_PROP command, corrected the logic by using targetId as the input to this new function in question.
Issue Description: In the logic handling GET_TARGET_PROP command, a new function mistakenly used pd instead of targetId as input, failing the command.
Steps To Reproduce: Issue this command,

/usr/bin/sg_write_buffer -m1 -i 230 -l 786432 -o 16646144 -I sasrecord.bin /dev/sg1 -vvv

---

Defect ID: DCSG00060816
Headline: iMR hits exception after FW upgrade before OCR then do storcli /c0 get snapdump
Description Of Change: For iMR, bypassed the functions in sanpdump execution code which will cause exception when Symbol Table is not present.
Issue Description: When a new FW is flashed to the controller, Symbol Table is wiped out. There are few functions in iMR which will cause exception if Symbol Table is not present. These functions were getting called during "get snapdump".
Steps To Reproduce: 1. Upgrade/downgrade FW between different packages.
2. Without OCR, do storcli /c0 get snapdump.
This will hit exception.

Defect ID: DCSG00060912
Headline: MR_7.13_Aero_Alpha: SSD SATA SysPD's retain in spin-down state after quickboot and after VMFS file system creation.
Description Of Change: After Spinup recovery on EPD successfully completed on EPD, PD state was still spindown, send wrong information to apps.
On Spinup recovery for EPD,mark the PD state as active and updated led status if necessary.
Issue Description: After Spinup recovery on EPD successfully completed on EPD, PD state was still spindown, send wrong information to apps.
Steps To Reproduce: This issue seeen on VMWARE OS, while validating quick boot feature..
Installed the VMWARE 7.0 os behind the Ventura IMR card.
Aero card has 4 SSD SATA.. Configured those as -JBOD.
Performed the quick boot operation. Which performs the fast reboot of os, during which driver load/unload happens by sending shutdown command .
After quick boot, all 4 SSD SATA moved to spin down mode.

Defect ID: DCSG00060967
Headline: Aero_DBU_7.13_Alpha: On Demand Snapdump during IO SATA and SAS SSD result to driver issued KA
Description Of Change: During quick boot on VM ware, the trace buffer manager is stopped and started without the controller going through boot up.
As a result the release offset had a nonzero value which was causing wrong entry offset calculation causing infinite loop.
Fixed by, resetting the trace buffer release offset when the extended trace buffer mode is enabled.
Issue Description: Kill adapter seen on triggering on demand snapdump after quick boot.
Steps To Reproduce: Perform quick boot on VM ware.
Trigger multiple on-demand snapdump.
Firmware occasionally hangs causing kill adapter.

Defect ID: DCSG00061011
Headline: SPILIB 2.0: Initialization fails for Spansion 64MB part in serial mode
Description Of Change: Modified Quad Mode Bit algorithm so that the right bit is written and compared.
Added an RDID identifier for Winbond 128MBit parts for firmware downgrade processing
Issue Description: When the user requests the serial mode initialization in a later version of SPILIB 2.0, it fails to clear the QUAD bit and thus fails initialization.
This is due to code, ported from SPILIB 1.0 that doesn't shift the CSR bits to the appropriate position.
This will not be seen when not in serial mode as the QUAD bit will always appear to be set (it is looking at WEL)
Also note this does not affect non-Spansion parts as they use a single configuration byte on the write
Steps To Reproduce: Using IT firmware and the latest SPILIB 2.0 code, initialize a Spansion 64Mbit to use SERIAL mode twice and switch back to Quad twice. The ring buffer will indicate a mis-compare on the SERIAL mode transitions in some versions of firmware due to stack data.

Defect ID: DCSG00061066
Headline: Implicitly converting an expression to a narrower type
Description Of Change: Update code so its not converting to narrower types.
Issue Description: Implicitly converting an expression to a narrower type
Steps To Reproduce: Static Analysis Tool found the issue

Defect ID: DCSG00061087
Headline: Correct tagowner for Spdm Client MCTP code
Description Of Change: Correct tagowner for Spdm Client MCTP code
Issue Description: Since FW is always the SPDM target as of now, set the tagOwner to be always False.
TagOwner = False meaning this is responding side of SPDM traffic.
Steps To Reproduce: None

Defect ID: DCSG00061353
Headline: SPDM library to remove %s for any print as IT does not support %s print string.
Description Of Change: SPDM library to remove %s for any print as IT does not support %s print string.
Issue Description: IT does not support %s print string method
Steps To Reproduce: None

Defect ID: DCSG00061711
Headline: Increase the time wait time when quad mode bit gets written for write operation to complete.
Description Of Change: When changing from quad mode to serial mode, quad mode bit is written. Increase the timeout value for which we wait for this operation to complete.
Fix coding standard issue: Since operating mode is used before, use different name and capitalize first letter.
Issue Description: With insufficient wait time, flash init in serial mode would fail with WIP timeout.
Steps To Reproduce: With current timeout value, try to initialize spi flash in serial mode which was already set for quad mode operation before.

Defect ID: DCSG00061718
Headline: Addressing IT raise defects in SPDM library change.
Description Of Change: This is to address several IT developer raised question in code review
http://cmappsvr2:8181/ui#review:id=52191

Changes includes following:
1.Support similar function such as pldmiPrintNumArgsGet(PrintIndex, &noOfArguments) to client who use SPDM library.
2. Change SPDMLibClientDbgPrint to also support SPDM_DEBUG_FILTER.

Issue Description: Addressing IT raise defects in SPDM library change.
Steps To Reproduce: None.

Defect ID: DCSG00062252
Headline: Controller fault 0x1902 is seen while issuing locate command to NVMe drives
Description Of Change:
While processing SEP requests from timer context, ensure there's no existing SEP request under process.
Issue Description:
Single SES request from host would lead to duplicate requests getting generated to SEP device.
Steps To Reproduce:
1. Flash an Aero IT board with the latest firmware package i.e., 13.250.20.00
2. Do not flash any BIOS package.
3. Connect an Atlas switch attached NVMe drive to the adapter under test.
4. Connect an UBM attached NVMe drive to the adapter under test.
5. Launch UEFI shell, execute following storcli commands
"storcli.efi /c0/eall/sall stop locate"
"storcli.efi /c0/eall/sall start locate"

Defect ID: DCSG00062370
Headline: Adding SPDM filter in client code.
Description Of Change: Adding SPDM filter in client code.
Issue Description: Adding SPDM filter in client code.
Steps To Reproduce: None

Defect ID: DCSG00063139
Headline: Data Exception abort happening when function called to dump memory blocks
Description Of Change: Use page count for SOF/EOF metadata out of flash filesystem configuration instead of hardcoding page count to current running FW.
The memory allocations for SOF/EOF is moved to happen at a later points (1) after filesystem is read, (2) when filesystem is created.
Issue Description: The page count for SOF/EOF metadata in filesystem changed.
This change occurred during previous code analysis fix.
This page count change resulted in failing verifying SOF/EOF, and the corresponding memory allocations sizing are different when page count changed.
Steps To Reproduce: Flash FW using older release prior to changing page count.
Power cycle.
On next bootup flash new FW after page count changed.
Issue a couple OCR (online controller reset)
Issue a couple warm resets. (CNT^ALT^DEL)
On next bootup, ARM controller for offload by dirtying the data cache, or can do 'col arm'
Power cycle.
The assertion is hit.

Defect ID: DCSG00063197
Headline: MR 7.13 after set autoconfig jbod and securesed off found pd always on for both "sed enabled" and "secured" feature
Description Of Change: When the config clear command is received, re-provision secured Pd's by unlocking the drive before marking the PD as Unconfigured good.
Issue Description: Drive secured as a part of secure JBOD creation is not unlocked when the JBOD is deleted.
As a result, JBOD created after turning secure setting OFF, still has drive in secured state.
Steps To Reproduce: 1) Set Autoconfig to JBOD and securesed = ON
2) Create JBOD with SED drive
-> Drive secured and JBOD created.
3) Delete config
4) Set Autoconfig to JBOD securesed = OFF
5) Create JBOD with same drive
-> JBOD is created with drive that is still secured.

Defect ID: DCSG00063631
Headline: MR_7.13-DBU: Windows Driver: During Hibernation PL Fault 0000d213 is seen.
Description Of Change: Added logic to not send pli request if the Extended Trace Buffer is already turned on
Issue Description: During hibernate two MFI INIT commands are received back to back because of the additional hiber driver which causes firmware to try to start the extended trace buffer manager twice causing pl fault.
Steps To Reproduce: 1. Windows 2019 H2 64 bit OS installation on R0 VD
2. Upgrade the driver to 007.013.007 on MR ventura
3. Go to the startup button and click on the Hibernation option.
4. Hibernation starts but fails to resume.
5. PL Fault 0000d213 is seen in firmware logs.

Defect ID: DCSG00063929
Headline: "Add enclosure event for an enclosure that is already active" error message observed in Windows event logs
Description Of Change: Updated FW to suppress start of day Enclosure status change events when Auto port is enabled allowing Windows driver to consume only the Event replay Encl status events.
Issue Description: "Add enclosure event for an enclosure that is already active" error message observed in Windows event logs on Aero/Ventura HBA attached to UBM backplane with Auto Port Enable turned on. When Auto port enable is turned on, the FW sends SAS Enclosure status event during SOD and later during events replay and the duplicate set of Enclosure add events causes driver to log the error.
Steps To Reproduce: Attach 9400-16i HBA with Auto port enable in the NVDATA to UBM JBOD. Boot up to Windows OS and observe the "Add enclosure event for an enclosure that is already active" error message in the event log.

Defect ID: DCSG00065467
Headline: MR FW failed to arm offload when cache offload was expected to start
Description Of Change: The function that determines if the controller is 8i or 16i was using device ID from PCI Config space. A race condition was intermittently causing a hang. The solution is to get the 8i/16i information from CCR instead.
Issue Description: Various symptoms were observed, with a common occurrence being a timeout detected by RMC while waiting for the L1/L2 flush to complete.
Steps To Reproduce: The test was using ipmi to produce repeated SyLite resets. The failure was very intermittent, failing anywhere from less than 10 iterations, to more than 200.

Defect ID: DCSG00066110
Headline: iop show cfgspace doesn't work
Description Of Change: Removed the "iop show cfgspace" command. It didn't work and was redundant with "iop pci rdcfg".
Issue Description: When you type "iop show cfgspace", it is returning the info from "iop show cfg".
Steps To Reproduce: Type "iop show cfgspace" into the UART.

Defect ID: DCSG00066267
Headline: Coverity usability
Description Of Change: Unimportant messages were removed from the report files, and the significant messages are written to the terminal.
Issue Description: Unimportant messages are included in the Coverity report files.
Steps To Reproduce: Do a Coverity build. Inspect the terminal messages and report files.

Defect ID: DCSG00066476
Headline: BIOS private data being overwritten at init time when EPD and RAID VD are both used.

Description Of Change: In Legacy mode, when getting BIOS DCMD, if EPD is set, do not send fake response, which overwrite BIOS data in NVRAM.
Issue Description: BIOS private data may be overwritten at init time when EPD and RAID VD are both used.
Steps To Reproduce: In Legacy mode, set EPD as boot drive and add RAID 5 VDs. Reboot.

Defect ID: DCSG00066510
Headline: 7.13-Alpha Aero: Capturing multiple snapdumps via Megamon zcdump hang
Description Of Change: The zcdump code was refactored so that it now runs as a background task, which allows a delay between transfers. Other code is allowed to run so the UART buffers may drain.
Issue Description: The Snapdump downloads would hang or terminate prematurely. This resulted in corrupt zip files.
Steps To Reproduce: Get the controller into a state where it has multiple Snapdumps. On-demand Snapdumps will suffice. Then use the Megamon command "zcdump ff" to download all Snapdumps.

Defect ID: DCSG00066639
Headline: 7.13-Alpha Aero: Data Abort Exception on exiting Megamon at end of onDemand snapdumps capture via zcdump
Description Of Change: The resource leaks in the Snapdump code were fixed.
Issue Description: Resources are not available when browsing the HII panels because the Snapdump leaked them.
Steps To Reproduce: * Power on the server
* Trigger a snapdump from Megamon with SnapDumpDbgGlobalOnly
* Browse the Megaraid HII panels

Defect ID: DCSG00067276
Headline: Ventura MR 7.13 Alpha FW; Win/Lin -5.6% to 12% drop in SW, SR profile for IO Size-4K, 8K,16K, 32K QDs-4, 16,64,256 in RAID level - 0,1,5,6 for 1/4/16 workers - 12G SAS HDD DC/EC - 8D/16D/24D/64D
Description Of Change: Add branch predictor to the EPD checks in LD IO path.
Issue Description: EPD checks was causing some regression in the LD IO path. Adding a branch predictor helps control the efficiency of this check.
Steps To Reproduce: Compare HDD SAS Sequential Writes 4k and 8k high queue depth (greater than 16 QD) performance results between 7.12 and 7.13 on Ventura.

Defect ID: DCSG00068142
Headline: Zuma Beach: FW - Diagnostics failed for PD event observed when Drive Pull & Push operation is performed.
Description Of Change: Making this event conditional as it was expected following the drive pull by certain OEM.
Issue Description: This event is not a defect as such; it was added initially on OEMs' request.
Steps To Reproduce: Steps

1. Create 3 DGs of each 64 VDs and 48 VDs in one DG, totally 240 VDs
2. do drive pull n push operation, while operation is in progress check fw or LSA event logs
3. we observe 401=Diagnostics failed for PD 03(e0xfb/s6)

Defect ID: DCSG00068343
Headline: Add sense dump to the MPT Error dump
Description Of Change: Added code to dump sense data to the existing routine which is dumping the MPT error info
Issue Description: Add sense dump to the MPT Error dump
Steps To Reproduce: Not applicable

Defect ID: DCSG00068812
Headline: Copy paste and overflow errors in cache offload module
Description Of Change: Fixed the duplicate call and type casted to U64 to prevent data overflow
Issue Description: Copy-paste error - the same function is called twice and AND'ED together. Also, U32 was truncating the output potentially exceeding U32 range
Steps To Reproduce: Static analysis tool found the issue

Defect ID: DCSG00068814
Headline: Update checking in Scons for multiple Coverity scans
Description Of Change: Loops were added to allow multiple files to be scanned.
Issue Description: The build tools were only allowing a single file to be scanned.
Steps To Reproduce: Do a firmware build with Coverity.

Defect ID: DCSG00069084
Headline: Elrond Ex2 w/ SAS/SATA incorrect slot numbers after PD move to different slot
Description Of Change: In online controller reset(OCR) boot context, while moving the drives from one slot to another. New insertion processing is delayed until device missing delay is expired and old instance of drive in another slot is fully removed.
Issue Description: If MR controller is booted up in an OCR and when a drive is moved across different slots on UBM backplane, insertion of a drive is being completed in new slot before removal is processed in the FW.
Steps To Reproduce: Connect 9560-16i to Elrond Ex2 with SAS and/or SATA PDs
Move drives from slot 0/1 to slots 2/3

Defect ID: DCSG00071882
Headline: MR7.13 Alpha: SLT menu "(5) GetEnclosures List" always list slot numbers from 0
Description Of Change: Modifications made in the FW to fill correct slot offset information from enclosure info.
Issue Description: One of the enclosure's start slot offset is 1. But the FW is was sending slot offset value as zero to the application.
Steps To Reproduce: Use external enclosure has slots from 0 to 23 while the other has slots from 1 to 24.

run "(4) GetPhysicalDevicesList", storelibtest shows each drive with correct enclosure ID and slot number.
run "(5) GetEnclosures List", storelibtest shows slot numbers from 0 to 23 on both enclosures.

Defect ID: DCSG00072162
Headline: MR-7.13: Observing FW generated Snap dump with 0 bytes & no mention of Tigger time.
Description Of Change: The code to evaluate how much memory is available for a Snapdump was adjusted. It now handles both areas.
Issue Description: Early Snapdumps are stored in a temporary area. The code to evaluate how much memory is available was inspecting the usual Snapdump area.
Steps To Reproduce: Create an exception as early as possible in start-of-day.

Defect ID: DCSG00072257
Headline: WG: In presence of foreign configuration, DHSP's assigned to simple config DG's are not displayed
Description Of Change: When a configuration created by the FW upon request from the application, DDF data was populated before FW initializes dedicated hotspare details in data structures. This will result in updating Spare drive's DDF information with just hotspare information and will miss dedicated hotspare info. Firmware changes were made to initialize internal data structures with Global hotspare info before writing the DDF data to the spare drive.
Issue Description: Dedicated hot drives are getting converted to Global hot spare. This happens when a foreign configuration created or rebooting the system
Steps To Reproduce: a) Clear all configuration on the controller and reboot the system.
b) Create simple two drive R1 with one dedicated hotspare
c) Check the simple configuration details in controller console page, it would show the Simple config details along with dedicated hotspare
d) Add another r1 with two drives
e) Remove the drives used in step d. Create foreign configuration
f) Check simple configuration, notice that the simple configuration would not show the dedicated hotspare details in DG tab of CC page

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Defect ID: DCSG00072285
Headline: Updating the slot number with Phy order on the board.
Description Of Change: This defect is used to update slot numbering for all Aero controllers as per board layout.

Issue Description: Slot number are not updated as per board layout
Steps To Reproduce: Connect Aero controller to SGPIO backplane.

Defect ID: DCSG00072826
Headline: Duplicate slot IDs assigned for SAS/SATA drives on elrond Ex1 backplane when it is connected to 9405W 16i controller.
Description Of Change: Changed the manual HFC group settings in the 9405W NVDATA to auto to attempt the UBM backplane enumeration on all the connectors of same port.
Issue Description: UBM Backplane enumeration is not attempted on one of the connector of 9405W since it was grouped with other connector of same port.As a result, firmware uses default slot number from NVDATA and that conflicts with slot assignment done in other connector where the UBM backplane was detected successfully.
Steps To Reproduce: Connect NVME drives to 1-4 bays and SAS/SATA drives on 5-8 bays of an Elrond backplane.

Connect the Ex1 backplane to 9405W 16i controller using a SAS fanout cable.

Run the pl status console command and observe the output.

Defect ID: DCSG00072841
Headline: pl: firmware hang occurs in UBM command error case
Description Of Change: Fixed a bug that caused the described state machine to fail to advance.
Issue Description: If certain command errors occur within the UBM status and control state machine, the state machine will get stuck in an infinite loop.
Steps To Reproduce: Boot firmware with a UBM backplane attached to the HBA. While firmware is running, disconnect the UBM backplane and connect a different UBM backplane to the HBA.

Defect ID: DCSG00073978
Headline: Performance regression in various workloads due to code arrangement (4K SW QD=64 RAD6 1W for 24 SAS SSD and SR profile for small IO size in all QDs in 12G SAS HDD)
Description Of Change: The Ventura scatter file was organized so that the LD IO path is more tightly coupled and is more resilient to code changes.
Issue Description: MegaRAID saw regression in the LD IO path on Ventura due to veneers being created in the LD IO path after some PL code changes.
Steps To Reproduce: Run either of the following and compare 7.3 to 7.14 IOPs:
1. 4K sequential writes at queue depth (QD) 64 RAD5 for 24 SAS SSD (Linux)
2. Sequential reads with small IO size (less than 64K) in all QDs in 12G SAS HDD (Windows or Linux)

Defect ID: DCSG00074108
Headline: Check in SpdmDebug.h for IT
Description Of Change: Check in SpdmDebug.h for IT
Issue Description: IT is not printing directly to serial output.
So it needs to include SpdmDebug.h for ring buffer dump.
Steps To Reproduce: None

Defect ID: DCSG00074318
Headline: MR_7.13_Aero_Beta: After Quick Boot - Un-configured good SSD SATA drives moved to spindown state .
Description Of Change: unconfigured/HS (Hot Spare) ATA drives should spindown based on MFC enableSpinDownUnconfigured and disableSpinDownHS and not on shutdown. Change is avoid spindown on shutdown
Issue Description: All SATA SSD drives where spundown during shutdown to avoid drives doing background activity. background activity may cause drive corruption due to power-loss (from shutdown).to avoid this drives where spindown. On quick boot VMWARE environment or Windows coming out of stand unconfigured/HS are never spinned back. Since there is no valid user data on this drive state, we don't spindown those drives, rather the spindown action is based of MFC enableSpinDownUnconfigured and disableSpinDownHS settings..

Steps To Reproduce:
Connected the enclosure which has SSD SAS, SSD SATA, SAS HDD to Aero controller .
All drives are in Unconfigured good state and spinup state.
Performed the Quick boot -- (Quick boot works only on particular server , which is captured in test-case id)
After Quick boot observed the unconfigured good SATA SSD drives moved to Spindown state. Remaining drives retains at spinup state. Which has been verified on the Storcli App..
Which is not expected , as during quick boot SATA SSD drives moved to spindown state, so after quick boot drives should discovered with SpinUp state..

Defect ID: DCSG00074328
Headline: SPDM LIB: Need to include header file SpdmLibTypes.h in SpdmLibIFace.h
Description Of Change: Include header file SpdmLibTypes.h in SpdmLibIFace.h to remove compiler error due to unknown type SPDM_U32 when compile N2 Dev Int.
Issue Description: Compiler error due to unknown type SPDM_U32 when compile N2 Dev Int.
Steps To Reproduce: Compile N2 Dev Int.

Defect ID: DCSG00074348
Headline: Kill Adapter when Running RAID 5 RMW CTIO 4K Random Writes
Description Of Change: The nvram intercore request is brought back for the functions which perform 'arm and disarm for offload' operations.
It was removed in a recent activity; by way of DCSG00057863.
Issue Description: Nvram write access from 2nd cpu core resulted in kill adapter.
Steps To Reproduce: Running RAID 5 RMW CTIO 4K Random Writes

Defect ID: DCSG00074556
Headline: Change file name of SpdmDebug.h to SpdmDebugs.h . And Check in SpdmDebugs.h for IT
Description Of Change: Change file name of SpdmDebug.h to SpdmDebugs.h . And Check in SpdmDebugs.h for IT
Issue Description: IT is not printing directly to serial output.
So it needs to include "SpdmDebugs.h" for ring buffer dump.
"SpdmDebug.h" file name is no longer in use.
Steps To Reproduce: None

Defect ID: DCSG00074881
Headline: dmdiag Aladin MegaMon commands not working
Description Of Change: Enable Aladin support with build flag
Issue Description: After an aladin capture, the resulting data can be produced with this MegaMon command:
MegaMon0> dmdiag aladin dump ccr
and this was found not to be working.
Steps To Reproduce: MegaMon0> dmdiag aladin dump ccr

Defect ID: DCSG00074952
Headline: Build failed after MbedTLS new base line pulled
Description Of Change: Build failed after MbedTLS new base line pulled
Issue Description: Build failed after MbedTLS new base line pulled
Steps To Reproduce: Build failed after MbedTLS new base line pulled

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Defect ID: DCSG00075666
Headline: Backplane expose on/off setting is failing
Description Of Change: Send Bus scan event when the expose backplane setting changes, so that the driver can query the new device list
Issue Description: On expose backplane setting change the updated device list was not read by driver.
Steps To Reproduce: storclif64 /c0 set backplane expose=off
lsscsi -i ---> this still shows the enclosure

Defect ID: DCSG00076663
Headline: MR 7.13 Beta: Aero reports: Assertion failure heavy IO+Reconstruction+TM Reset

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Description Of Change: There are cases when command can be queued after processing, in that case do not process it again. Firmware change made to fix this issue

Issue Description: Firmware was processing host command multiple times and it causes link list of child commands to point to the parent command. Firmware safety checks detected this and asserted.

Steps To Reproduce: Running the certified script on config with 24 SATA drives sees the issue.
Step1: Create 2 drive R1, 3 drive R5, 15 EPD drives
Step2: Run Heavy IOs on all logical drive
Step3: Migrate 2 drive R1 to 4 drive R5
Step4: Run TM in a loop on JBOD drives.

Note : This issue is hard to reproduce without the script. Running TM as soon as you start the Migration is key to reproducing the issue consistently

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Defect ID: DCSG00076717

Headline: Some of SAS/SATA drives attached to OEM Aero HBA may not be reported to host

Description Of Change: Updated FW event reporting logic to iterate through Direct attached enclosure Phys list and send events for all of them.

Issue Description: Some of SAS/SATA drives attached OEM specific Aero HBA may not be reported to host. The Phys forming the direct attached enclosure are non-contiguous (eg., 0xF0FF) and the FW only sends topology change list events for a subset of Phys.

Steps To Reproduce: Attach OEM specific Aero HBA to JBOD with SAS/SATA, Boot up to Windows OS and observe only some of the drives in the Enclosure are reported.

Defect ID: DCSG00076783

Headline: pl: port enable is delayed when SAS/SATA devices are attached to a UBM backplane

Description Of Change: Start a port's PCIe hinting timer on UBM presence detect change only when the presence of a PCIe device is detected.

Issue Description: If SAS or SATA devices are attached to a UBM backplane, the PCIe hinting timers associated with the ports to which the devices are attached will always time out, causing port enable to be delayed by the PCIe hinting time limit.

Note that this issue was introduced in phase 15 and is not present in any GCA firmware version.

Steps To Reproduce: Connect an Elrond Ex1 backplane containing SAS or SATA devices to the HBA. Bring up firmware.

Defect ID: DCSG00076934

Headline: MR 7.14 : Storcli allows to set maxspinupdrive count to 255.

Description Of Change: Additional firmware checks added to avoid setting spinup drive count more than maximum drives supported

Issue Description: Controller info set function was not checking if the spin up drive count is more than maximum drives supported.

Steps To Reproduce: Using following command try to set spinup drive count to 255 and it should not be allowed
SYNTAX: storclif /cx set spinupdrivecount=255

Defect ID: DCSG00077263

Headline: PL: MS-SES with no Array Devices in Atlas SES causes 0x7200 fault

Description Of Change: Corrected a check meant to detect when no Array Devices are found in the SES's SES Page 1, which then transitions to copying SES Page 0Ah without any Array Device descriptors being translated.

Issue Description: MS-SES with no Array Devices in Atlas SES causes 0x7200 fault with a SES Page 0Ah read

Steps To Reproduce: Attach an Atlas managed switch with 0 Array Devices configured in the Atlas firmware or NVDATA.
Issue a SES Page 0Ah to the SES on the Managed Switch SES (MS-SES).

Defect ID: DCSG00077700

Headline: Mismatch between subsystem id in NVDATA and SBR for 9405-W 16i

Description Of Change: Changed the SBR subsystem ID to match that of NVDATA.

Issue Description: PCI subsystem ID in SBR not same as in NVDATA.

Steps To Reproduce: Flash 9405W-16i card with firmware concatenated nvdata for the same and notice the difference between PCI subsystem ID in SBR and NVDATA.

Defect ID: DCSG00077833

Headline: PTB bad address handling

Description Of Change: Add checking to the DCMD processing. Only DMA when the register DCMD has been received. This avoids using a bad address.

Issue Description: It is possible to disrupt the sequence of DCMDs, and cause DMA operations to fail.

Steps To Reproduce: Inject a preboot OCR after seeing the ptbUpdateState message for "registered". This will cause the controller to be reset. As it is re-initializing, the PTB DCMD will be skipped which causes a DMA to fail.

Defect ID: DCSG00077919

Headline: [SPDM] SPDM lib changed one of header file name , seeing compilation error in IT.

Description Of Change: Fixed in include file.

Issue Description: Seeing compilation error after pulling the SPDM lib new base line. (changed file name from : spdmdebug.h to spdmdebugs.h)

Steps To Reproduce: make aero

Defect ID: DCSG00077979

Headline: Additional Key Data field of Security Page 1 is missed in XSD definition

Description Of Change: Added the Additional Key Data field to security page 1 in master xsd

Issue Description: Additional Key Data field of Security Page 1 is missed in XSD definition

Steps To Reproduce: Not applicable

Defect ID: DCSG00078207

Headline: MR-7.13: FW - STP passthrough response Firmware does not send some ending bytes.

Description Of Change: Correct FW to send sizeof (FIS header) + 512 bytes response.

Issue Description: FW is not sending complete 512 bytes response back to host for OOB STP pass through.
FW is started with FIS header + response until 512 bytes is reached.
What really should happen is FW should send sizeof(FIS header) + 512 byte response total.

Steps To Reproduce: Compare output of host STP pass through Identify versus OOB STP pass through Identify output

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Defect ID: DCSG00078243

Headline: MR-7.13: FW - STP passthrough -FW sending ack before completely receiving all MCTP packets.

Description Of Change: 1. Change FW OOB STP handling to accept rest of mctp packet until full buffer size is received.
2. Detect FW have send acknowledgement for request and avoid sending duplicate acknowledgement.
3. Initial OOB Spdm message tag value to invalid. Otherwise, 2nd mctp traffic will match tag value of 0 and proceed to Spdm Process logic, result in exception.

Issue Description: 1. FW assume STP pass through request buffer to be only one MCTP packet.
This is not True since storelibtest use same buffer for request and response.
This results in later mctp packets to result in error, making mctp_driver and application to bail out.
2. FW is generating double MCTP acknowledgement which is wrong.
3. 2nd MCTP packet is going to OOB Spdm processing, result in exception.

Steps To Reproduce: Run STP pass through Identify through OOB in customer BMC environment.

Defect ID: DCSG00078508

Headline: AXI access error from TxDMA engine when certain errors occur during Task Management processing

Description Of Change: When a Task IU response is received and it was retried, do a cleanup of the TxDMA queue to prevent starting an unneeded TaskIU which would cause the AXI access error.

Issue Description: If issuing a Task IU to a device fails, a retry is made. In some errors, the first TaskIU made it to the drive. Firmware process the response frame assuming it was for the retry and completes the Task Management. If the 2nd Task IU is still on the TxDMA queue an AXI access error can occur because the memory representing the Task IU has changed when the TM completed.

Steps To Reproduce: The issue occurs when the connection goes away before receiving the ACK from the device. In this case, the error was the result of a noisy environment, no specific error injection was happening. A jammer could be used to cause this possibly.

Defect ID: DCSG00078563
Headline: MR7.13 Beta: Improve Config creation time to yield other traffic.
Description Of Change: replace DDF debug mprints with etty print to prevent logging wasting CPU cycles and yield to other task like oob traffic.And limit ddfdebug to error
Issue Description: OOB MCTP processing goes back seat, if there are DDF config creation print too much preventing other threads from execution.
Steps To Reproduce: Start to create and delete a large config on the controller in band.
Set SL debug level to 1 on OOB emulator.
Start FW download stress test through OOB SL/SLT.

Defect ID: DCSG00078806
Headline: locate LEDs state fails for odd slots on Ex2 backplane
Description Of Change: SES element control is check to route the LED request correctly.
Issue Description: locate LEDs state fails for odd # slots on Ex2 backplane
Steps To Reproduce: Connect 9580-16i to Elrond Ex2 with SAS/SATA drives.
Issue locate command to all slots.
Only even slots show locate LEDs (i.e. 0, 2, 4, 6)

Defect ID: DCSG00079022
Headline: cannot flash FW even after a warm reboot when followed by OOB FW flashing is interrupted
Description Of Change: clear any previous allocated cache memory for FW download purposes during SOD.
Issue Description: With ventura & Aero all cachemem are persistent memory.if previous FW download is incomplete and after re-system, memory will not cleared causing FW download failure due to memory allocation failure. Attached download address it.
Steps To Reproduce: Started FW flashing from OOB storelibtest.
Before FW flashing is completed, OOB storelibtest is killed.
Perform a warm reboot of the system.
Attempt to flash the FW using in band tool, ie. storcli.

Defect ID: DCSG00079268
Headline: Add a build option for Coverity MISRA_CAST to disable CWE-681
Description Of Change: Another Coverity option is used to disable the error.
Issue Description: Coverity checking around unsigned assignment is too strict.
Steps To Reproduce: Do a firmware build with Coverity.

Defect ID: DCSG00079486
Headline: 512B drive is assigned as DHSP for 4K DG
Description Of Change: Added check to prevent mismatch of sector size when assigned hot spare
Issue Description: Dedicated hot spare with sector size 512B was getting assigned to a drive group with 4k sector drives.
Steps To Reproduce: Create a R1 with a dedicated hot spare where the hot spare has a different sector size than the VD

Defect ID: DCSG00079652
Headline: Make it easy to query PTB wrap
Description Of Change: Add another flag to the "ptb" Megamon command to print only information about the PTB header.
Issue Description: "ptb -f" prints too much when the user is only interested in wrap.
Steps To Reproduce: Boot into the BIOS and browse our Megaraid panels. Then use "ptb -f" from Megamon.

Defect ID: DCSG00079654
Headline: Use NVRAM to save PTB information
Description Of Change: Code was added to save the location information in NVRAM. So it is available after OCR and the PTB can be collected.
Issue Description: The controller is storing the PTB location information in volatile memory. Since the location information is only registered once, it is lost after an OCR and the PTB cannot be collected later.
Steps To Reproduce: Power on a machine. After seeing the PTB registered print, inject an OCR from Megamon.

Defect ID: DCSG00079768
Headline: Fix SPDM routines name which are using same name as PLDM routines
Description Of Change: Fix SPDM routines name which are using same name as PLDM routines
Issue Description: Some routines used by SPDM module is having same name as PLDM routines.
This cause link error when building under PLDM stream.
Steps To Reproduce: None

Defect ID: DCSG00080256
Headline: (SATA Only) SCSI ATA Passthrough command with set feature command to set the drive in standby_y state sets it to standby_z state.
Description Of Change: For non data transfer commands do not convert sector count from number of bytes to number of sectors.
Issue Description: A SCSI ATA PAssthrough command send to SATA drive with 'byte block' bit set to 0 in flags field means that the transfer length value specified in sector count or features field on SCSI ATA Passthrough command is in number of bytes. For this case firmware converts the sector count from number of bytes to number of sectors before sending the ATA command to the drive, but this conversion is not required for non data transfer commands.
A Set features command send using SCSI ATA PAssthrough command with byte_block bit set to 0 results in incorrectly change the SectorCount field of ATA command and setting the drive in incorrect standby state.
Steps To Reproduce: To a SATA drive connected to the controller send a SCSI ATA Passthrough command with Set Features ATA command to set the drive in standby_y power state. After the completion of SCSI ATA PAssthrough, observe that the drive enters standy_z state instead.

Defect ID: DCSG00080298
Headline: PL Backend PCIe: 0xEE1A fault observed with bad clocked Aero and Atlas
Description Of Change: In case of error during MPI initialization, skip the MPI management state machine processing until adapter reset state machine completes
Issue Description: 0xEE1A fault is hit.
New adapter reset is started when already one in progress.
Steps To Reproduce: Boot the server with Aero in common clock mode connected to Atlas in SRIS mode.

Defect ID: DCSG00080749
Headline: Controller DPM (Drive Performance) returns some unacceptable numbers.
Description Of Change: There was an issue in FW for calculating response time in ns and micro seconds. Micro seconds calculation was overflowing beyond 32 bit boundary. Calculation has been changed to 64 bit. First us (microseconds) is calculated and from us, ns is getting calculated. This causes incorrect value for ns. Calculation for ns is changed to calculate ns directly.
Average Q-depth was initialized to 0, which was causing Q-depth calculation error. Initialization was changed to be initialized to the first value.
It seems there is an issue in storecli to display sectors read. If Sectors Read is large, storecli display is not correct. A defect for this can be created for storecli.
Response time display in storecli is just a number. An enhancement request can be created to display response time as range.
Issue Description: 1. Storcli /c0/ex/sx DPMstat type=RA (Running Average) returns Queue Depth=0 for any QD set to 16 or less in IOmeter.
Average Q-depth was initialized to 0, which was causing Q-depth error.
2. Storcli /c0/ex/sx DPMstat type=ext returns SR (or SW) as number of sectors (bytes) transferred but it over-flows and shows 255.
FW uses 64 bit memory to hold sectors read (SR) and Read Command Count. It seems storecli is using 32bit value for Sectors Read. For example in one instance, FW log shows SR=0000002feab00054 RC=bfab6 (785078).
For this storecli prints shows SR=255 and RC=785078. storecli shows a wrong value for the SR.
3. Storcli /c0/ex/sx DPMstat type=Hist returns response time =0 ns for 8222 commands. It is not acceptable to be 0 ns. A range of Response time should be given instead of a fixed number.
There was an issue in FW for calculating response time in ns and us (microseconds). Calculation was causing overflow beyond 32 bit value. Now caclulation is being doen as 64 bit data.
FW returns a value for the response time. This value implies a range. If value is 1ns. It means response time is between 1ns to 2ns. If value is 1us. It means range will be 1us to 10us.
Steps To Reproduce: Iometer settings are 256kB Seq. Read running for 3 Min. on a Jbod.
1 storcli /cx show dpm
2 storcli /cx start dpm
3 storcli /c0 delete dpmstat type=all
4 Start IOmeter for only one workload on a single jbod, 256kB Seq Read.
5 storcli /c0/ex/sx show dpmstat type= Lct / Hist / RA / Ext logfile=fn.txt
6 Repeat steps 3 to 5 for every run.
6 storcli /cx stop dpm

Defect ID: DCSG00080856
Headline: Fail to read device and link related counters from Page 250
Description Of Change: 1. Added the new pages (below) to the Config Page Routing Array to allow CFGI Lib route the request correctly.
a. Extended SAS Device Page 250
b. Extended Expander Page 250
c. Extended PCIe Device Page 250
d. Extended PCIe Switch Page 250
2. Updated "iop show cfg" command to dump the new pages
Issue Description: The application (ScrutinyCLI) cannot read the new pages added for Device and Link related counters
Steps To Reproduce: Read the new config pages:
a. Extended SAS Device Page 250
b. Extended Expander Page 250
c. Extended PCIe Device Page 250
d. Extended PCIe Switch Page 250

Defect ID: DCSG00081231
Headline: Use NVRAM to save PTB information
Description Of Change: Fields were defined to save PTB location information in NVRAM.
Issue Description: The controller is storing the PTB location information in volatile memory. Since the location information is only registered once, it is lost after an OCR and the PTB cannot be collected later.
Steps To Reproduce: Power on a machine. After seeing the PTB registered print, inject an OCR from Megamon.

Defect ID: DCSG00081243
Headline: Fix file names related to PTB
Description Of Change: The file names and paths were changed.
Issue Description: The content of the unit tests has increased. Rename some of the files to be more generic. Also, some of the libraries have been moved in 7.14 so some paths need to be adjusted.
Steps To Reproduce: Do a firmware build for unit test.

Defect ID: DCSG00081566
Headline: Avoid data exception when collecting early preboot snapdump
Description Of Change: Add checks to skip some data collection when the module is not ready to access
Issue Description: Avoid data exception when collecting early preboot snapdump
Steps To Reproduce: See reproduce steps

Defect ID: DCSG00081732
Headline: NVME Drives not getting discovered on inserting in Customer UBM3 x4 backplanes until OCR.
Description Of Change: As per new change during Start of day,firmware will de-assert HFC PERST# signal irrespective of the change source detected.
Issue Description: Currently the HFC PERST# signal is de-asserted only when there is no change source detected or drives installed in the UBM Backplane. During backplane enumeration the customer UBM backplane reports a different change source and hence the firmware fails to de-assert HFC PERST#. As a result NVME discovery fails after hot pug.
Steps To Reproduce: Connect the UBM3 X4 NVME Backplane on MR416i-a controller

Insert the NVME drive after the controller is up.

Observe that no drives discovered after hot plug.

Defect ID: DCSG00082524
Headline: NVMe device not discovered after disable-enable PCIe link in PCIe IO Unit page 1
Description Of Change: Enable hardware cleanup sequencing workaround done for Aero in Ventura as well.
Issue Description: If a Write Current of PCIe IO Unit Page 1 is used to set the PHY Disabled flags associated with an existing PCIe link following port enable, the link won't come up when the flags are later cleared. An adapter reset is needed to restore the link.
Similar issue was found in Aero as well for which fix was to modify sequencing of hardware cleanup steps in the link disabled case.
Steps To Reproduce: Disable PCIe link connected to an NVMe drive and then renable the link in PCIe IO Unit page 1. Observe that NVMe drive is not discovered after enabling the link again.

Defect ID: DCSG00082963
Headline: Aero: PswSbr.bin file is read only and causes an error when running the RMC script
Description Of Change: Modified perl script to not open the file as writable
Issue Description: Build fails when PswSbr.bin is read only
Steps To Reproduce: build Aero

Defect ID: DCSG00082970
Headline: Firmware faults while running a script to do drive push-pulls
Description Of Change: - Added code to check if cleanup has already happened when a timer expires in the spinup statemachine
Issue Description: Firmware faults while running a script to do drive push-pulls
Steps To Reproduce: TR71229
System: SMC AS -4023S-TRT (AMD cpu; 64GB RAM)

Ctrl: 9580-8i8e (8GB); pkg3126
Driver: 7.13.10 (win 2019)
UBM EX1 Backplane FW: 2.29
8 NVME pds

Wingman version: wingman 2.0 version 2020.01.28

Wingman Certified script DCSG00035513: NVMe_Pull_insert_PD_different_operations.json

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Defect ID: DCSG00082981
Headline: Use NVRAM to save PTB information -- API changes
Description Of Change: Comments were added about alignment and byte count restrictions for the location specified in MR_DCMD_CTRL_PREBOOT_TRACE_BUFFER. These restrictions allow the location information to be stored more efficiently in NVRAM.
Issue Description: The controller is storing the PTB location information in volatile memory. Since the location information is only registered once, it is lost after an OCR and the PTB cannot be collected later.
Steps To Reproduce: Power on a machine. After seeing the PTB registered print, inject an OCR from Megamon.

Defect ID: DCSG00083355
Headline: AeroMR: Win/Lin, Gen3, 4/8DC, 16EC, NVMe, 1/4/16W, RAID5, RW/OLTP, 4K/8k/16K/32K, QD=64/256, 8-40% Regression from RO3010 to ROP3102.
Description Of Change: Allow higher max queue depth for SSD drives and lower max queue depths for HDD drives.
Issue Description: PD max queue depth was increased since this helped SSD performance but it was later found to have a negative effect on HDD. Since lower queue depth negatively effects NVME, it was decided to have lower queue depth for HDD and higher queue depth for SSD.
Steps To Reproduce: 1. Create NVMe RAID5 (4, 8, or 16 drives)
2. Start Random Writes or OLTP with 4K,8k,16K, or 32K transfers with queue depth of 64 or 256
3. Compare performance between ROP3010 and 3102 (8-40% Regression)

Defect ID: DCSG00083594
Headline: pl: NVMe: D062 fault during NVMe init
Description Of Change: Increment the IO counter before enqueuing an LMID to the NVMe hardware, not afterward.
Issue Description: If a very fast NVMe device is attached or firmware is running unusually slow, a D062 fault may occur during NVMe init. This appears to be a side effect of the LBA 0 read added in phase 15.
Steps To Reproduce: Initialize several NVMe devices while console prints are being generated.

Defect ID: DCSG00083748
Headline: MFG Page 49/50/51 defines are not compiled
Description Of Change: MFG Page 49/50/51 are not defined within a macro.
Issue Description: MFG Page 49/50/51 defines are not compiled in CFGI build.
MFG Page 49/50/51 are defined under SPDM macro that is not enabled during CFGI build.
Steps To Reproduce: Not applicable

Defect ID: DCSG00084027
Headline: Fix Static Code analysis issue 101556 101555 101554
Description Of Change: Static code analysis fixes
Issue Description: Made sure variables used are right size and added type cast
Steps To Reproduce: NA

Defect ID: DCSG00084472
Headline: Junk character is display in OEM serial number
Description Of Change: Change FW behavior to only take 14 bytes as OEM serial number
Issue Description: FW was not enforcing the 14 byte length of the OEM serial number
Steps To Reproduce: Run "storcli /c0 show mfg"

Defect ID: DCSG00084540
Headline: Aero Pre-man string failure during looped testing
Description Of Change: While waiting for BAR init to complete, avoided calling ISR in tight while loop. Instead it will be called call every second. Changed the string that prints timeout to display that matches pre-manufacturing expected string
Issue Description: When FW waiting for BAR init to complete, UART logs are not getting transferred to the host system and it is lost. Also the string that prints timeout is printing function name instead of the string that pre-manufacturing test expected
Steps To Reproduce: This happens after cache offload / retention test was activated, then power off, then on following power up.

1) Storclif /c0/cv start retentiontest
2) We power off the pcie slot, but I would think pull plug to system to allow Data Retention to happen
3) Monitor the UART on the next system power up and see the strings.

We look for the following string to be dumped by the FW
In the failing log, we get:
T28: C0:extTTYImportSOD: importing, add
T88: C0:pceWaitForBARInitToComplete: Timed out waiting for BAR init

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Defect ID: DCSG00085845
Headline: Connector Name displayed as 'Unknown' in HII for NVMe drives behind Switch
Description Of Change: Populating the Connector Name Field in PCI Dev Page 0 for Switch attached device with the same Connector name as the Switch it is attached to.
Issue Description: The Connector Name Field in PCI Dev Page 0 for Switch attached device is not being populated.
Steps To Reproduce: 1. Connect a switch. Behind the swtich, connect a NVMe drive.
2. Launch HII application and go to Physical Disk Properties form. Verify the Connector Name field.

Defect ID: DCSG00086266
Headline: The first 32 characters of MPI defines should be unique
Description Of Change: Renamed the MPI defines related to Security pages such that the first 32 characters are unique
Issue Description: First 32 characters of MPI defines related to Security pages are not unique
Steps To Reproduce: Not applicable

Defect ID: DCSG00086774
Headline: Adjust the UART messages during Snapdump
Description Of Change: Prints were added after each data collection function. The prints include timing information.
Issue Description: The Snapdump prints need to clearly identify which data collection code has been run. This is needed to efficiently debug Snapdump bugs.
Steps To Reproduce: Generate an on-demand Snapdump, and observe the UART output.

Defect ID: DCSG00086898
Headline: Duplicate MPI Toolbox Tool Values in MPI temp
Description Of Change: Changed the drive recovery toolbox tool to a different value to avoid conflict.
Issue Description: Two different new MPI toolbox tool values were defined in mpi_temp.h. There's a conflict and one needs to be changed.
Steps To Reproduce: NA

Defect ID: DCSG00086932
Headline: Controller DPM type= hist does not save Response time properly which shows some conflicts.
Description Of Change: Running Average fields were initialized to 0. Initialized fields with first data after the test started.
Issue Description: Type=Hist shows conflicts with Max and average Response times
Steps To Reproduce: storcli /c0/ex/sx show dpmstat type= Hist
Match bin response time with average and max response times.

Defect ID: DCSG00087283
Headline: Fix static analysis issues
Description Of Change: Fix integer casting issues that were found by static analysis tool
Issue Description: Static analysis tool indicated integer casting issues
Steps To Reproduce: Run static analysis tool

Defect ID: DCSG00087285
Headline: Fix static analysis issues
Description Of Change: Fix integer casting issues that were found by static analysis tool
Issue Description: Static analysis tool indicated integer casting issues
Steps To Reproduce: Run static analysis tool

Defect ID: DCSG00088074
Headline: MR7.14 Beta: BMC-OOB-Update Controller Firmware SLT reports "Flash download already in progress"
Description Of Change: Fix is to introduce a timer to auto close Flash Context if FW does not see periodic MR_DCMD_CTRL_FLASH_DOWNLOAD every CTRL_FW_FLASH_STATE_DELAY (120 Sec) or FW Flash never move to the next state for CTRL_FW_FLASH_STATE_DELAY (120)seconds.
So if user inted to test Ctrl+C case, they can re-issue Ctrl FW Download after 120sec from previous Ctrl FW Flash.
Issue Description: If user bail out by doing Ctrl+C to abort storelibtest/storcli process in middle of Ctrl FW Flash.
FW FlashBuf and FlashInfo context is not properly clean due to application does not proceed to next Ctrl Flash Dcmd or do proper tear down.
Next time user again tries to flash, FW will return with Flash already in progress error.
Steps To Reproduce: Do oob Ctrl Flash dcmd, and Ctrl+C in middle of Ctrl FW flash.

Defect ID: DCSG00088148
Headline: controller DPM type=Ext returns wrong number of sectors.

Description Of Change: Modified logic to convert bytes into sectors.
Issue Description: controller DPM type=Ext returns wrong number of sectors. Instead of sectors, it returns in bytes.
Steps To Reproduce: Start DPM
Run Iometer 256KB QD 16 on a Jbod HDD for 3 Min.
Run DPMStat type=Ext
Check RC (Read commands) and convert to SR (Sectors Read) by mutiplying 256x1024/512

Defect ID: DCSG00092935
Headline: Phase 15 Coverity Bug Fixes
Description Of Change: Added appropriate fixes in code for the issues seen.
Issue Description: Identical code for different branches, Logically dead code, Logical vs Bitwise operator, unchecked return value, Uninitialized variable, unused variable, explicit null dereferenced issues seen in FW
Steps To Reproduce: Run coverity on Phase 15 stream

Defect ID: DCSG00093410
Headline: pl: NVMe: 265D fault in out of resource case
Description Of Change: Gate usage of the NVMe init context area with NVMe init state in addition to presence of the NVMe init LMID.
Issue Description: If the PL resource frame pool becomes exhausted such that allocation of a frame for NVMe init succeeds but allocation of a frame for usage with async notification fails, a 265D fault may occur.
Steps To Reproduce: Initialize NVMe devices during a persistent low resource condition.

Defect ID: DCSG00093660
Headline: pl: backend PCIe: resource leakage during direct attached event generation
Description Of Change: Do not allocate an LMID in this case unless an event is to be generated.
Issue Description: An LMID is allocated by the direct attached PCIe enclosure event generator but is not freed if no event is generated.
Steps To Reproduce: Perform a test that repeatedly causes PCIe discovery to run.

Defect ID: DCSG00093703
Headline: Updated CoreDump specific functions to run from OCM memory and enabled XMEMXOPY
Description Of Change: Moving various modules to OCM defeats the purpose of disabling XMEMCOPY. Re-enabling XMEMCOPY for now.
Issue Description: With 14.250.04.00 FW, XMemCopy is disabled, which will force the FW to run from flash. During CoreDump executing, the flash access can cause contention because CoreDump will be dumping data to the flash as well. This can cause a hang.
Steps To Reproduce: Use 14.250.04.00 and force a C0FFEE fault to trigger a coredump

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Defect ID: DCSG00094727
Headline: Coverity Defects
Description Of Change: Fixed coverity issues like out of bounds access, derefence after null check, missing break in switch.
Issue Description: Coverity found defects that includes out of bounds access, derefence after null check, missing break in switch
Steps To Reproduce: Not applicable

Defect ID: DCSG00094728
Headline: MR 7.14 : Unable to set controller properties with latest aero firmware pkg using storcli
Description Of Change: Additional logic added in the FW to check if NVRAM has spinupDriveCount setting more than PROFILE_MAX_PHYSICAL_DRIVES and if detected it will be updated to PROFILE_MAX_PHYSICAL_DRIVES.
Issue Description: spinupdrivecount set was allowed up to 0xff in FW older than ROP DCSG00092761. Defect DCSG00076934 fix added a check in the FW to check if applications setting spinupDriveCount more than PROFILE_MAX_PHYSICAL_DRIVES(240 in MR). Applications read spinupDriveCount set by the older FW and then use that structures to update any other controller properties. But the FW logic that check if spinupDriveCont more than PROFILE_MAX_PHYSICAL_DRIVES fails.
Steps To Reproduce: 1. Connect an aero card, preferably 9560-16i or 9580-8i8e card.
Flash 7.14 ROP older than DCSG00092761.
Set storclif /cx set spinupdrivecount=FF (This FW allows to set this value to FF)
2. Flash latest firmware on the controller. Package build : 52.14.0-3149 //DCSG00092761

3. Now, try to set controller properties like"

storcli64.exe /c0 set ocr = on/off
storcli64.exe /c0 set maintainpdfailhistory = on/off
storcli64.exe /c0 set unmap = on/off

Defect ID: DCSG00095243
Headline: FW creates R0 VD when HII: Enable/Disable Host LED Management For JBOD setting is toggled
Description Of Change: Add logic to not auto create R0 if already in R0 mode. R0 will be auto created only when mode is changed from non-R0 to R0.
Issue Description: Firmware was auto creating R0 on all UGood drives when Auto Config Set is received even for a property change from R0 mode.
Steps To Reproduce: 1. verify that controller's auto config setting is at raid 0.
2. in HII, verify that there are some UG drives available.
3. under HII Advanced Controller Management menu, toggle Enable/Disable Host LED Management for JBOD.

Defect ID: DCSG00096489
Headline: Fixing Coverity issues
Description Of Change: Added required changes to fix Coverity reported issues.
Issue Description: Coverity reported issues
Steps To Reproduce: Run Coverity

Defect ID: DCSG00096538
Headline: print correct variable during error condition
Description Of Change:
Updated variable being printed at the time error check fails.
Issue Description:
Incorrect variable was printed at the time of error.
Steps To Reproduce:
Code inspection.

Defect ID: DCSG00096545
Headline: Unitialized pointer was being accessed
Description Of Change:
Ensured pointer was initialized before access.
Issue Description:
Unitialized pointer was being accessed
Steps To Reproduce:
Code Inspection.

Defect ID: DCSG00096622
Headline: Aero_DBU_7.14_PA2: VMWARE Beta OS reported Assert during data under run.
Description Of Change: - Added code to send the proper status values when data under run happens
Issue Description: VMWARE Beta OS reported Assert during data under run.
Steps To Reproduce: This issue seen on vmware os 7.0 Beta On card Ventura IMR..
Created 4K drive as JBOD.

Run the script which performs -- creating 6 VM's and taking Snapshot for around 6 times..
After 1 Hour, it result in VMWare asserting

Defect ID: DCSG00096702
Headline: PBP hotplug drives showing dual sas address, instead of single sas address
Description Of Change: When the drive is removed, clear both present flags of the device from the persistence device table.
Issue Description: On PBP a drive is presented in app and to the user as single path with one SAS address.
This is not the case, as reported in this defect, after the drive is removed and reinserted.
The drive shows up as multipath with identical SAS addresses for both paths.
Steps To Reproduce: 1. connect drives to PBP controller; verify each drive is shown with one SAS address
2. pull out one of the drives; insert it back
3. check this drive's info via LSA or CLI; notice two SAS addresses are listed

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Defect ID: DCSG00096734
Headline: Controller Delete DPMStat Type=all does not reset QD.
Description Of Change: Made firmware change to reset CurrentIndex tracker to 0 during DPM Clear commands (DPM Delete Stat commands).
Issue Description: After running DPM test at lower Q-depth, stopping DPM test, deleting DPM statistics and running the DPM test at higher Q-depth does not calculate average Q-depth correctly. Firmware internal currentIndex tracker is not reset to 0 by deleting DPMStat. This causes starting Q-depth to be initialized to a lower value and hence overall average Q-depth remains lower.
Steps To Reproduce: 1. Start DPM
2. Run IOmeter SR256KB, QD 1 for 3 Min.
3. Collect DPM data.
4. Delete DPM Stat Type=all
5. Run IOmeter SR256KB QD 16 for 3 Min.
6. Collect DPM data and check QD. It should be 16 but it is much less.

Defect ID: DCSG00098168
Headline: Update log function to match API changes for event structure
Description Of Change: Remove the type casting in the log function for enclId and slotId pair.
Issue Description: After API changes, the type casting is no longer required.
Steps To Reproduce: see code.

Defect ID: DCSG00098345
Headline: pl: NVMe: E429 fault on register read failure
Description Of Change: Fixed a bug that caused an improper NVMe init state to be used by the NVMe init error handler.
Issue Description: If PL fails to read an NVMe device's CSTS register upon entry to the NVMe init state machine, an E429 fault will occur.
Steps To Reproduce: Initialize an NVMe device that is connected to the HBA thru a poor quality device side PCIe link.

Defect ID: DCSG00098596
Headline: Coverity found defect in SATA and Enclosure management modules.
Description Of Change: Removed out of bound access and NULL pointer dereference.
Issue Description: Coverity found defects like NULL pointer dereferencing and out of bound access in SATA and enclsoure management modules.
Steps To Reproduce: Not Applicable

Defect ID: DCSG00098787
Headline: Coverity found defect in MPI Device and FPE modules.
Description Of Change: Removed out of bound access, NULL pointer dereference and uninitialized variable usages.
Issue Description: Coverity found defects like NULL pointer dereferencing, out of bound access and uninitialized variable usages in MPI Device and FPE modules.
Steps To Reproduce: Not Appplicable

Defect ID: DCSG00099024
Headline: MR_7.14_DBU: FW & Storcli reported enclosure id's are mismatch for a NVM-E drive which has failed in nvmeinit
Description Of Change: from MptHandlePCIEDevStatusChgEvent, change an NVME INIT entry, if slot mapping is completed. if Slot mapping is not completed, added an NVME INIT entry after enclosure enumeration.
Issue Description: from MptHandlePCIEDevStatusChgEvent, change an NVME INIT entry, if slot mapping is completed. if Slot mapping is not completed, added an NVME INIT entry after enclosure enumeration. This will ensure that the slot id is properly populated.
Steps To Reproduce: Connected the Intel NVM-E drive behind the system motherboard.
Performed the Namespace deletion using Intel tool isdct . -- ./isdct delete -namespace 1 -intelssd 0
Poweroff the server.
Connected the drive to Elrond backplane which is connected to Aero card
Poweron the server. Fired the storcli command to get the NVME drive error list - It list the drive with enclid:slotid -- 272:2

EID:Slt RP RIP Reason Of Failure

272:2 Yes No Namespace count invalid

Fired the storcli command to repair the drive -- ./storcli64 /c0/e272/s2 start repair force -- IOCTL was successful .

At the sametime fw reported at the fwlog.

02/27/20 2:33:05: C0:EVT#430497-02/27/20 2:33:05: 618=NVMe Repair started on drive (e0x10/s2)
02/27/20 2:33:05: C0:NvmeInitFailDevListGetRepairStatus: Error! there is no entry of failed NVMe drive enclId 0xf9 slotId 0x2.

Even VSES id of Elrond backplane is 249 , which is seen storcli /c0 show -

Fired the storcli command to check the status, it throw an error message - NVMe repair is not in progress and command is in failure status.

It is confusing to user which is the enclosure id of Elrond.
if in-case fw reported enclosure id is correct, please move to storcli team..

Defect ID: DCSG00099273
Headline: 4K VD is set to boot device after foreign config import
Description Of Change: After an LD is imported, check if the target ID is the same as the boot target ID in NVRAM, and force the boot target ID to invalid if the PD has 4K sector size
Issue Description: boot Target ID saved in NVRAM is not cleared properly
Steps To Reproduce: 1. Create a situation where current selected boot device ID is identical to imported 4K VD ID.
2. Enter HII and change auto foreign config import setting.

Defect ID: DCSG00099487
Headline: Fix MR MPB2 copied length.
Description Of Change: Mpb2EntryLength include Mpb2Entry header + payload(this is the whole page size), previously FW was using incorrect length, which is short of 3 bytes.
Now FW copy the correct length so upper layer module would not result in false MAC.
Issue Description: User module who use MPB2 write is resulting in MAC comparison failure.
Steps To Reproduce: Issue write security page 0/1 and read the page back.

Defect ID: DCSG00099915
Headline: MR 7.14: Storcli: "Support NVMe Repair" is shown as "yes" in profile 10 and incorrect raid support displayed in profile 11 on iMR ventura
Description Of Change: Controller info NVME Repair flag was set to false for profiles that does not support NVME drive.
Controller info RAID level support flag settings modified to avoid unsupported raid levels.

Issue Description: Controller info NVME repair flag was set in the FW even when the profile does not support NVME drive
Controller info set raid level support flags irrespective of profile on all iMR controllers.

Steps To Reproduce: iMR Ventura controller with profile 10 (doesnt support NVME)
- Execute storcli /c0 show all
- Under "Supported Adapter Operations : below properties are displayed as:
  Support NVMe Repair = Yes-----"""INCORRECT""", as NMVe is not supported in profile 10. It should display as "No"

- Now change the profileid to 11.
- Reboot the system and boot to OS.
- Execute /c0 show profile

  Capabilities :
  ==========
  Supported Drives = SAS, SATA, NVMe
  RAID Level Supported = RAID0, RAID1(2 or more drives), RAID5, RAID00, RAID10(2 or more drives per span), RAID50--------"""INCORRECT""" as profile 11 support max of 2 drives, only R0 and R1 should be supported.

Defect ID: DCSG00100308
Headline: SBLIB: Change bool type to int type in API parameter to maintain compatibility
Description Of Change: Change bool type to int type in API parameter to maintain compatibility across platforms.
Issue Description: Compile firmware with a new API fails due to undefined function parameter.
Steps To Reproduce: Compile firmware with a new API fails due to undefined function parameter.

Defect ID: DCSG00101756
Headline: PCIe Switch Page 250 has NumPorts set to zero, and this page is not included in "iop show cfg all"
Description Of Change: - Updated PCIe Switch Page 250 Read function to populate the NumPorts field.
- Updated "iop show cfg all" dump to process PCIe Switch Page 250.
Issue Description: - PCIe Switch Page 250 Read function missing the NumPorts field update.
- PCIe Switch Page 250 processing is not done in "iop show cfg all" command
Steps To Reproduce: - Read PCIe Switch Page 250 from ScrutinyCLI
- Run "iop show cfg all" command.

Defect ID: DCSG00102153
Headline: Avoid controller firmware freeze due to one particular vendor's SATA TCGe drive behavior
Description Of Change: Added checking to ensure incremental progress is being made to process packet from TCGe drive from one particular Vendor
Issue Description: Controller hang triggered by short packet response from TCGe drive from one particular Vendor
Steps To Reproduce: Do pull then push of the drive, or will also occur if this particular drive inserted at bootup.

Defect ID: DCSG00102332
Headline: PH15 Scrutiny CLI: device c command output is not giving the details of the all the devices connected to the expander
Description Of Change: Added check to skip the expander dev-handles and continue searching for the end-device dev-handle. This will allow all the devices to be returned by the FW.
Issue Description: When the expander dev-handle is found, the FW will return INVALID_PAGE to the application which will indicate that there are no more devices available.
Steps To Reproduce: Create a topology where expander handle is in between the end-device handle and dump the Ext. SAS Device Page 250

Defect ID: DCSG00103063
Headline: Bug Fix for SPDM modules
Description Of Change: 1. Fix for Import CSR DCMD, FW is not copying full certificate from host
2. Key generation module should not init key in exit, module who use Generation Key Pair should init Key Pair after use.
Issue Description: 1. Fix for Import CSR DCMD, FW is not copying full certificate from host
2. Key generation module should not init key in exit, module who use Generation Key Pair should init Key Pair after use.
Steps To Reproduce: Use storelibtest to issue import CSR request

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Defect ID: DCSG00103123
Headline: SPDM: Fix issues in Certificate Slot Mgmt DCMD
Description Of Change: Fixed some issue in Slot Mgmt DCMD, it should read cert page, check if not sealed, then clear out Flags field, zero out Cert Chain field and write cert page.
Issue Description: Slot Mgmt DCMD does not read cert page in order to validate before invalidate it.
Steps To Reproduce: Use test version of StoreLibTest from APP team to issue Slot Mgmt DCMD.

Defect ID: DCSG00103208
Headline: [Aero] Application scanning for I2C devices on I2C bus hang when OOB configured to MCTP-PCIe mode
Description Of Change: Disable I2C core 4 when MCTP is disable or OOB set to MCTP-PCIe mode.
Issue Description: 1) I2C core 4 is initialized when OOB set to MCTP-PCIe mode.
2) I2C interrupts are handled but I2C requests are not processed leading to I2C timeouts in host and leading to retry.
Steps To Reproduce: 1) Connect multiple I2C devices on same I2C bus.(OEM server has this configuration)
2) Configure the controller to OOB MCTP-PCIe mode.
3) Run the application which will scan for I2C devices on the bus.
4) Observer that the application hangs.

Defect ID: DCSG00103799
Headline: Deleting file system during bst is not done using mrcli
Description Of Change: Now using mrcli function to delete the file system partitions created during BST.
Issue Description: mr class function is used to delete the file system partitions created during BST.
Steps To Reproduce: Start bst using the script.
Observe that script fails when file system is deleted.

Defect ID: DCSG00103807
Headline: iMR BST VDs are getting created with read ahead property set.
Description Of Change: Create VD with no ra property.
Issue Description: Creating VD with read ahead property set is not allowed in iMR controller.
Steps To Reproduce: run bst script for iMR controller.

Defect ID: DCSG00103860
Headline: Controller DPM overflows Write Count after 32 bits. As per document, it is supposed to be 64-bit number.
Description Of Change: Changed firmware logic to return write and read counts as 64 bit data.
Issue Description: Existing Firmware calculates write and read counts as 32 bit data instead of 64 bits.
Steps To Reproduce: Run Iometer 4kB Rand Write QD 256 overnight on SSD drive.
Get DPM data.
storcli /c0/e251/s9 show dpmstat type= ext will show this issue.

Defect ID: DCSG00103877
Headline: SPDM DCMD bug fix 03/04/20
Description Of Change: 1. Make FW Cert Write function PSecCertWriteCertChainConfigPage support Seal/Not Seal request form host
2. FW Cert Read function PSecCertReadCertChainConfigPage was returning Certificate data which is wrong.
  Purpose of this function is to read Certficate Page, it should return whole page to dcmd module.
3. Some fix with Export CSR dcmd PSecExportCsrDcmd provide incorrect input to PSecCsrConstructCsr.
4. Fix MR Config Page Get DCMD in order for host to get correct data on ExtManPage 49/50/51 and Security Page 0.
Issue Description: Some dcmd result in exception, result in incorrect data transfer from FW
Steps To Reproduce: Issue Storelibtest security related dcmd commands to FW

Defect ID: DCSG00103993
Headline: NVMe Init reports wrong failure error codes
Description Of Change: Added check in the NVMe Init state machine, if Identify Namespace command returns all zero in the response, then fail the NVMe initialization with "No Namespace 1" failure reason.
Issue Description: As per NVMe spec, if Identify Namespace command returns all zero in the response, that means the namespace is inactive or unallocated. In our current NVMe Init state machine, we do not have a check for this condition and fail the NVMe drive initialization with incorrect failure reason.
Steps To Reproduce: 1. Use nvme-cli to delete ns on one NVMe drive.
2. Use nvme-cli to detach ns on one NVMe drive.
3. Connect NVMe drives to Aero controller

Defect ID: DCSG00104982
Headline: Phase 15 Coverity Bug Fixes
Description Of Change: Added appropriate fixes in code for the issues seen
Issue Description: Identical code for different branches, Logically dead code, Logical vs Bitwise operator, unchecked return value, Uninitialized variable, unused variable, explicit null dereferenced issues seen in FW
Steps To Reproduce: Run coverity on phase15 stream

Defect ID: DCSG00105045
Headline: Phase 15 Coverity Bug Fixes
Description Of Change: The function was not support to return NULL, Fault in that case.
Issue Description: Deference null return value
Steps To Reproduce: Run coverity on phase15 stream

Defect ID: DCSG00105299
Headline: bst_jbod fails to change personality for iMR controller.
Description Of Change: Do not check for personality for iMR family of controllers.
Issue Description: iMR controller has only one personality and hence no personality change operation is supported on this controller.
Steps To Reproduce: run bst_jbod script on iMR controller.
Personality change operation fails as this is not a supported operation.

Defect ID: DCSG00106563
Headline: Updated the forceUpdate format in PLDM header generation Tool
Description Of Change: In PLDM Header generation tool , the way we read ForceUpdate(-fu=) option format was wrong ,corrected it.
Issue Description: ForceUpdateBit is not getting set in PLDM Header, because of which PLDM fw downgrade operation is not possible.
Steps To Reproduce: Generate PLDM header and observe FORCEUPDATE bit is not set in the header.

Defect ID: DCSG00107714
Headline: The last known successful learn time is reported as in Nov 11, 2000
Description Of Change: Removed SKIP_WAIT from the NvramIntercore request for BBU macro functions which update NVRAM parameters.
Fixed a unrelated static analysis tool issue.
Reverted function which enable/disable offload back to original code which called NvramIntercore directly within the function.
Issue Description: The NvramIntercore request is called with SKIP_WAIT when stack variable is being used. This only affects aero.
By the time NvramIntercore request is processed on 1st cpu core, the content of the stack variable on the 2nd cpu core had changed and garbage is being programmed to nvram.
Steps To Reproduce: Initiate a learn cycle.
Wait for the completion.
Use test tool to observe the results of the learn, and the last known successful learn time is giving Nov 11, 2000.

Defect ID: DCSG00108060
Headline: Firmware Fault on iMR while running IOs on 4K sector drives
Description Of Change: - Added code to initialize the context of an IO while releasing the frame to hardware
Issue Description: Firmware fault on iMR while running IOs on 4K sector drives
Steps To Reproduce: This issue is seen on vmware
Created 4K drive as JBOD.
Run the script which performs -- creating 6 VM's and taking Snapshot for around 6 times
After 20 minutes observed a FW FAULT.

Defect ID: DCSG00108246
Headline: Large topology of more than 500 drives cannot be supported on SAS 3.5 Channel Controllers
Description Of Change: Set the minimum number of Expanders and Enclosures supported in Manufacturing page 9 of NVDATA to 64 to support large topologies of upto 1024 drives. This change is done only for SAS/SATA only profiles.
Issue Description: In a recent change the minimum number of end devices was changed to 1024 in NVDATA for channel controllers for SAS/SATA only. The minimum number of expanders/enclosures were kept at 16 which resulted in not being able to support large topologies if minimum number of expanders were allocated.
Steps To Reproduce: Attach a large topology of more than 500 drives and 30 expanders to Aero controller. Observe that some drives and expanders are not discovered by the controller.

Defect ID: DCSG00108281
Headline: Observed PL Fault 0xEE17 when NVME drives connected via PCIe switch.
Description Of Change: Reverted new changes as the existing code is acceptable as per use cases.
Issue Description: Fault was added in new place to fix the coverity found defects like NULL pointer dereferencing.
Steps To Reproduce: Connect NVME drives to controller via PCIe switch.
Boot the controller.
Observe the 0xEE17 in the console.

Defect ID: DCSG00108408
Headline: SPDM: Don't fail APP request for import certificate in slot 2-7 with sealed flag set
Description Of Change: When APP sends Import Certificate DCMD for slot 2-7 with seal flag set, allow this request to go through for FW to handle it instead of failing request.
Issue Description: When APP sends Import Certificate DCMD for slot 2-7 with seal flag set, allow this request to go through for FW to handle it instead of failing request.
Steps To Reproduce: Use test version of storcli with spdm support:
storcli /cx import security spdm slotgroup=xx slot=yy file=filename [seal]

Defect ID: DCSG00108698
Headline: MR7.14 iMR snapdump start from ID 1 where MR start snapdump ID 0-- not consistent
Description Of Change: iMR code was adjusted to use zero as the Snapdump ID. This matches the MR code.
Issue Description: iMR and MR use different IDs for the first Snapdump. They need to be consistent.
Steps To Reproduce: Load the latest 7.14 ROPs on an MR and iMR. Collect on demand Snapdumps and compare the IDs in "storcli /c0 show snapdump" output.

Defect ID: DCSG00108800
Headline: Aero MR FW: While reconstruction process is running in the background, Firmware is allowing to change the behaviour mode from NONE to R0 with error message.
Description Of Change: Do not set the status to failed, if R0 creation fails as a part of Autoconfig set command.
R0 creation status is propagated only for the R0 execute once command.
Issue Description: Status was set to failed, when auto R0 creation failed due to active recon in progress, even though R0 mode was set successfully.
Steps To Reproduce: 1. Flash the latest firmware.
2. In Raid personality mode, Create a Raid 0 using LSA
3. Now Modify the drive group to Raid 1.
4. Reconstruction process started. While Background process is running, change the behaviour mode from "NONE" to "R0"
5. Observe Behaviour mode is updated to RO, with error message "Error code: 118, Operation is not possible"

Defect ID: DCSG00108848
Headline: Parallel PD Firmware hang once interrupted and restarted from SLT in OOB PCIe mode
Description Of Change: In the middle of the parallel fw pd update performed host application after the download completed application got abruptly terminated. There is 5 min timer reset added to handle the cleanup internally PD Firmware download module. This way the user retry the same operation will proceed to update the firmware on the next attempt. The issue earlier was incorrect check caused the reset was not triggered.
Issue Description: While preforming the parallel PD fw update using OOB, and in the middle of the operation if the host application terminated abruptly , even after retried the same command after 5 minutes the command fails always.
Steps To Reproduce: Start the SLT , perform parallel PD firmware download
while in the middle of download, kill the SL by pressing Ctrl+C.

Restart the SLT and perform parallel PD firmware download.

Observe the message as:

Fw download is not allowed on this PD

Defect ID: DCSG00109053
Headline: PL Fault 0000e40e while booting OS with bad NVMe drive
Description Of Change: Add a check in the beginning of NVMe Initialization state machine for the validity of Device Base Address.
Issue Description: Due to faulty device FW skips device configuration and Device Base Address remains INVALID.
Steps To Reproduce: Boot to OS with a bad NVMe drive behind the controller.

Defect ID: DCSG00109086
Headline: MR7.14 PA2 - Unable to collect zcdump once hitting PL Fault. FW keeps looping back to PL Fault again.
Description Of Change: The assert code was corrected such that Megamon cannot be exited. Correcting this causes zcdump to always run in the foreground.
Issue Description: PL faults are not invoking Megamon correctly. Firmware cannot continue execution after a PL fault, so the user must be blocked from exiting Megamon.
Steps To Reproduce: Inject a PL fault by inserting a bad NVMe drive to x4 NVMe UBM enclosure, and boot to OS.

Defect ID: DCSG00109315
Headline: [SPDM] Fix compilation #include "iopPlatSecCertMgMt.h" case sensitive issue
Description Of Change: Fixed file name (case sensitive)
Issue Description: file name case sensitive issue. In Windows build working fine and in Linux seeing problem.
Steps To Reproduce: make aero

Defect ID: DCSG00109367
Headline: Fix for the value of a controller status bit: Support PD firmware download
Description Of Change: Change the status bit input to match the name/description.
Issue Description: Currently, the value provided to Support PD firmware download is not matching the name.
Steps To Reproduce: StorCLI to run show all.

Defect ID: DCSG00109936
Headline: 7.14 PA2 (DBU) LSA WG: No option to change the behavior mode for the Ventura controller.
Description Of Change: Set the multi behavior supported bit in Ventura Raid personality
Issue Description: Multi behavior supported bit was not set for Ventura Raid personality, hence LSA was not showing the setting.
Steps To Reproduce: 1. Have Ventura card in the config.
2. Install latest LSA on linux.
3. Click on Personality Management option.
4. Observe no option to change the behavior mode.

Defect ID: DCSG00110319
Headline: OEM board: SAS drives the link speed is shown as unknown
Description Of Change: In updating link speed of a multipath device, add additional checks for negotiated logical link rate of both phys to be certain that both paths are active.

Issue Description: In updating link speed of a multipath device, existing logic assumes if a path is present it is also active. This does not work in a topology involving a Pismo Beach Plus board, where a dual ported drive connected via the expander functions as a single ported drive.
Steps To Reproduce: 1. Connect SAS drives (HDD n SSD) to PBP controller.
2. Do Push n Pull Operation
3. Observe in Drive Property that for SAS drive link speed is shown as unknown

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Defect ID: DCSG00111382
Headline: MR 7.14 PA2 - Aero firmware asserted at taskman.c at line 361 during R5 SED creation
Description Of Change: Timer is added to the command appropriately if timer is missing on the command when DM queue issues the command.
Issue Description: PD clear command may be blocked by the FW if a drive is in recovery mode and queued in to DM wait queue. Current firmware is not starting the timer on this command when these commands were re-issues. Drive could end up not responding to these commands and it may get stuck at the PL layer. As the timer is missing on the command, FW could not issue a TM request. These chain of event will cause IO traffic block and driver killing/resetting the controller.
Steps To Reproduce: 1. Enable SED on Aero controller
2. Create R0 and R5 VDs with SED enabled using LSA

Defect ID: DCSG00111753
Headline: SPDM : BMC Emulator System is halting at POST with latest FW pkg 2.14.0-3226 with Zumabeach controller.
Description Of Change: FW now allows DCMD SET CTRL TIME to go through for minimal capability mode.
Issue Description: With SPDM policy implementation FW is boot up with minimal capability mode, which
FW will fail mostly any set dcmd. This included DCMD SET CTRL TIME.
Due to Firmware fail this dcmd, boot up process stuck in post.
Steps To Reproduce: With latest ROP, boot up the system.

Defect ID: DCSG00111965
Headline: Aero_DBU_714: On Cavium (ThunderX2(R) CPU CN9975 v2.1 @ 2.20GHz) ARM server with Ubuntu OS, Aero discovery fails with megasas_init_fw
Description Of Change: Firmware was updated to handle multiple BAR updates occurring at the same time.
Issue Description: Firmware crashes due to multiple BAR updates.
Steps To Reproduce: Boot a Cavium Arm server with an Aero controller, the latest 7.14 code, and Ubuntu 18.04.

Defect ID: DCSG00112203
Headline: Fix Bus Master Enable handling in Snapdump related to DCSG00040869
Description Of Change: The Snapdump code was updated. When bus master enable is off, the Snapdump is discarded, and the controller is reset.
Issue Description: The controller needs to be reset after bus master enable has been toggled. If firmware tries to collect a Snapdump before the controller has been reset, additional errors will occur.
Steps To Reproduce: Boot into Windows. Disable the iMR controller in devmgr. Reboot. Soon after windows is booted, iMR will crash.

Defect ID: DCSG00112274
Headline: Aero SPDM Policy: Add Nvram flag to enable/disable SPDM feature in megamon
Description Of Change: FW now introduce another flag enableSPDM in nvram.
By default, enableSPDM flag will start with 0, so next ROP, SPDM by default is disabled.
If testers want to enable SPDM.
Please do megamon>EnableSPDM or megamon> DisableSPDM and reboot/ocr.
The flag is stored into Nvram and read back in next reboot/OCR.
So that SPDM Policy module can change to SPDM enable/disable mode.

Issue Description: Customer have requested a ROP build with SPDM disable.
While internal test team may want to test a lot of feature with SPDM enable such as host application SPDM related commands.
However, it is hard to maintain two ROP with two different XML.

Steps To Reproduce: None

Defect ID: DCSG00112303

Headline: PL NVMe : NVMe repair operation fails with metadata

Description Of Change: If metadata size(MS) of existing LBAF is non zero, find different LBAF for the given logical block size which has metadata size(MS) set to 0.

Issue Description: The issue is during recovery if logical block is of size 512 or 4K, existing LBAF is used for format without checking metadata size(MS) of LBAF.
Since the metadata size is non zero for LBAF, again NVMe initialization fails.

Steps To Reproduce: 1. Format namespace to lbaf with metadata using nvme-cli.
2. Connect to Aero controller, NVMe init error reported correctly.
3. Start repair operation using storcli, repair fails.

Defect ID: DCSG00113527

Headline: Fix iMR save code in create small dumps

Description Of Change: The code to save to NVRAM was added.

Issue Description: It was noticed that small dump isn't working for iMR because the save to NVRAM code is missing there. This small dump code is only used for internal testing.

Steps To Reproduce: The easiest way to reproduce this is to run "call SnapDumpDbgCreateSmallDump" from Megamon.

Defect ID: DCSG00113697

Headline: NVMe Init Error List has drive entry missing when multiple Bad PDs are inserted

Description Of Change: Added check in the FW while reporting device as part of the PCI device discovery, if the the Drive has already completed initialization and failed, then FW will not report this device as part of PCI Topology change event list.

Issue Description: While reporting the device as part of the PCI device discovery, the FW is not checking if the device has completed Initialization and has failed Initialization. FW goes ahead reports this device which has failed initialization as part of PCI Topology change event list and hence the device is not getting added into the NVME Init error list.

Steps To Reproduce: Insert two or more PDs with NVMe Init error

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Defect ID: DCSG00114179

Headline: pl: NVMe: EC0E fault after drive pull during NVMe init

Description Of Change: Fixed a couple of bugs related to cleanup of NVMe init with a pending Namespace Not Ready retry.

Issue Description: If NVMe init is in progress, a Namespace Not Ready retry is pending for the namespace readiness read, and the associated NVMe device is pulled, the NVMe init session may not be cleaned up properly. This causes an EC0E fault when the device is unregistered.

Steps To Reproduce: Perform device add/removal testing with NVMe devices that report readiness before the namespace is ready.

Defect ID: DCSG00114774

Headline: PL : 0x7008 fault seen when booting the bad clocked controller connected to Atlas

Description Of Change: IO to Managed Switch SES device is pended if pend flag is set and the IO is not from the pend list.

Issue Description: The IO to Managed Switch SES device that was expected to be pended is being added to control queue.

Steps To Reproduce: Boot the server with Aero in common clock mode connected to Atlas in SRIS mode.

Defect ID: DCSG00115555

Headline: Printing vd_id for jbods in iMR raises script error.

Description Of Change: Now not printing vd_id in iMR controller testing script.

Issue Description: Accessing vd_id for iMR controller (in jbod bst script) causes script error.

Steps To Reproduce: Running jbod bst script on iMR controller raises error.

Defect ID: DCSG00117767

Headline: MR_7.14 PA2 DBU: FW received the KA, while running IO with IOCTL command in a loop

Description Of Change: Abort the fast path IO's in the context of the abort task TM, diverted to firmware.

Issue Description: Fast path IO's diverted to firmware were not handled in abort task sequence, causing TM to be retried twice before being escalated to reset.
This recovery sequence was sometimes taking more than abort TM timeout causing driver to issue kill adapter.

Steps To Reproduce: Install the VMWARE 7.0 OS on system mother board of Dell AMD Gen-4 system.
Created one NVM-E JBOD - 1.455 TB NVMe SSD N N 512B SAMSUNG MZWLL1T6HEHP-00003 .
Performed the creation of 6 VM's . Performed the creation of 6 Snapshot and deletion in a loop with a duration of 10200sec
Concurrently running attached storcli scrpt in a loop.
After two hours observed the Kill adapter ..

Defect ID: DCSG00118659

Headline: Snapdumps are discarded unnecessarily when flashing a new ROP

Description Of Change: The code was adjusted so that the SBR/CBB version is also considered in the decision to discard Snapdumps.

Issue Description: Snapdumps are only supposed to be cleared when the SBR/CBB are flashed. However, Snapdumps are being cleared for ROPs with the same SBR/CBB.

Steps To Reproduce: * Flash an ROP. Eg 3224.
* Boot up and create an on-demand Snapdump.
* Flash another ROP with the same SBR. Eg 3230.
* Do a storcli /c0 show snapdump to observe that the Snapdump has been discarded.

Defect ID: DCSG00119529

Headline: SPDM_FW : Import certificate should fail for the slots for which already certificates are imported and sealed

Description Of Change: Added change in firmware to check if firmware receives Import Cert DCMD or Export CSR DCMD, check if cert slot request is already used or sealed, reject DCMD.

Issue Description: Firmware didn't reject Import Cert DCMD to the sealed cert slot or used cert slot.

Steps To Reproduce: Import the security slot with seal command.

storclif64.exe /c0 import security spdm slotgroup=0 slot=5 file=certchain.der seal

Import is successful.

Try to import the same slot with same command.
Import succeeds, where import should not be allowed as slot is sealed from first Import cmd.

Defect ID: DCSG00120091

Headline: MR FW Assertion failure in snapdump module

Description Of Change: If Expected SD Image count is not matching with Existing one Scan the NAND Flash for SD Images and update count accordingly

Issue Description: MR FW Asserted is because of there is mismatch between Snapdump Image Count and Snapdump Images written to NAND flash . This seems to be very corner case where Snapdump Image written to NAND but Count did not update because Reboot Happen before updating the Valid Snapdump Image count in NAND.

Steps To Reproduce: Create Secured R1 VD with NVMe OPAL
- Start Migrate from R1 to 4 x PD R6
- Remove 1 PD from R1 DG
- Assertion detected as expected.
- Reboot System
- Force into preboot Utilities
- C, and Y to continue from HII
- FW Crash

Defect ID: DCSG00120588

Headline: pl: NVMe: unexpected NVMe init failure if LBA 0 is inaccessible

Description Of Change: If the LBA 0 read that is performed to check namespace readiness during NVMe init fails with an error other than Namespace Not Ready or if the Namespace Not Ready retry time limit expires, allow NVMe init to proceed as if the LBA 0 read had succeeded.

Issue Description: If LBA 0 on an NVMe device cannot be read for some reason, NVMe init will unexpectedly fail. Note that this issue was introduced in phase 15 and is not in a GCA release.
Steps To Reproduce: Attempt to initialize an NVMe device that is security locked.

Defect ID: DCSG00120976
Headline: (SATA Only) SCSI ATA Passthrough command with data transfer fails.
Description Of Change: Get the byteblock field from SCSI ATA passthrough flag correctly so the sector count is set with right value in ATA FIS sent to drive.
Issue Description: While checking the byteblock flag in SCSI ATA passthrough command, fw was always setting the value to 0 resulting in incorrect translation of Sector count field in ATA FIS sent to drive.
Steps To Reproduce: Use hdparam to send fw download command to a SATA drive. The command will fail.

Defect ID: DCSG00121768
Headline: SPILIB 2.0: Cypress 256Mbit SPI Flash Is Not Supported
Description Of Change: Added Cypress 256Mbit SPI Flash to supported device array
Issue Description: Cypress 256MBit SPI Flash was not ported from SPILIB 1.0 to 2.0 (left out of the supported devices array)
Steps To Reproduce: Host boot and program a board with a Cypress 256MBit Part on it

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Defect ID: DCSG00121827
Headline: MR 7.14 PA2 DBU : SLT_OOB : Get enclosure element data throws 8017 error code for UBM backplane.
Description Of Change: 1) For Virtual SES device, Sense data is not returned properly to host&OOB applications on completion for MFI commands.
2) PCE Oob completion state is pre-maturely free command, before return sense data.
Issue Description: This is Virtual SES device, it doesnt support temperature element page. Further this device might not have capability to read temperature/fan speed etc. hence its return sense data, 5/26/0 (unsupported/invalid field). This data is not properly returned to host applications.
Steps To Reproduce: 1. Connect a UBM backplane along with an enclosure to the aero controller on BMC_OOB setup.

[In this case the setup was (PCIe_OOB)]

2. Go to enclosure menu and select option 10 which is "get enclosure element data"
3. For enclosure we get the data properly, but for UBM we could see error code 0x8017.

PFA storelibdebug.txt and fw logs for the same.

```
                    ...ENCLOSURE MENU...
                     ---------------------
(1) Get Enclosure Config Information    (2) Get Enclosure Status
(3) Set Enclosure Element Data          (4) Locate Enclosure
(5) Shutdown Enclosure                  (6) Get Enclosure Status_Ex
(7) Get Enclosure Element Data

0 TO QUIT. Invalid option to return to Previous Menu
Currently selected controller = 0
Please enter choice :7
        Enter Enclosure Device Id      251

Please select the element type(0-Temp, 1-Voltage, 2-Current) : (default = 0)
        Enter element index(zero based) 0

ProcessLibCommand Successful. Get Element data is shown below.
Element Type: Temperature
Element Index: 0
High critical value: 85
Low critical value: 18
High Warning value: 85
Low Warning value: 18

Press ENTER to continue


                    ...ENCLOSURE MENU...
                     ---------------------
(1) Get Enclosure Config Information    (2) Get Enclosure Status
(3) Set Enclosure Element Data          (4) Locate Enclosure
(5) Shutdown Enclosure                  (6) Get Enclosure Status_Ex
(7) Get Enclosure Element Data

0 TO QUIT. Invalid option to return to Previous Menu
Currently selected controller = 0
Please enter choice :7
        Enter Enclosure Device Id      250

Please select the element type(0-Temp, 1-Voltage, 2-Current) : (default = 0)
        Enter element index(zero based) 0


GetEnclElement : ProcessLibCommandCall failed; rval = 0x8017
```

Defect ID: DCSG00121852
Headline: Aero_scrutinycli: "Device -c" command output is not matching with the firmware cli parameter values in Aero behind atlas configuration.
Description Of Change: Fixed Extended PCIe Switch Page 250 to populate the port descriptors correctly.
Added Ext PCIe Device Page 250 for MPI-SES device exported by PCIe-Switch.
Issue Description: Extended PCIe Switch Page 250 not correctly populated
Steps To Reproduce: Read Extended PCIe Switch Page 250 after connecting Atlas Switch

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Defect ID: DCSG00126744
Headline: SPDM_FW : SPDM commands are failing in OOB SL/SLT on Trinity M6 servers.
Description Of Change: Add additional logic in resume to check if oobCmdState is in sending state (this state is indicated after dcmd command processing), before sending back dcmd response data.
Issue Description: Storelibtest use single buffer for request/response for manufacturing SPDM commands.
If buffer is large enough, Resume OOB command is used.
For OOB Read/Write command, if the read flag is set, FW always assume when receiving resume, dcmd process is already completed.
This is not the correct assumption. This results in while still transferring data for large request, FW thought dcmd is already finished and starts to copy back dcmd response data.
Steps To Reproduce: Under OOB environment, use storelibtest to issue Read Security Page 0 Slot 0.
Storelibtest timeout or result in error.

Defect ID: DCSG00127828
Headline: Asserts from interrupt handlers are not working properly
Description Of Change: The print code now disables interrupts in its locking code to avoid nesting.
Issue Description: Code executing in system mode was interrupted in the middle of a print. Inside the interrupt handler, firmware tried to print again.
Steps To Reproduce: Power on a Cavium Arm server with Aero, the latest 7.14 code, and Ubuntu 18.04.

Defect ID: DCSG00129498
Headline: NVMe repair command fails with 'No drive support for recovery' loginfo
Description Of Change: Before exiting the NVMe Init which failed while parsing the Identify Controller Data structure (CNS 0x1), made sure that firmware parses the complete structure and stores this information which will be used later in the NVMe recovery state machine.
Issue Description: Firmware fails the NVMe Init of the drive before parsing and storing the complete data received as part of Indentify Controller Command (CNS 0x1). This data like 'NameSpace Managment is Supported' & 'Format NVM is Supported' is used during the NVMe recovery state machine.
Steps To Reproduce: 1. Connect an NVMe drive with no namespace count 0
2. Attempt to run storcli /c0/ex/sx start repair force command

---

Defect ID: DCSG00131485
Headline: Invalidate slot not working for IT SPDM
Description Of Change: Added improvement to existing validation handling for SPDM TOOL BOX commands:
1) Export CSR:
- Reject command if slot request is already in use or seal

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2) Import Cert:
- Reject command if slot request is already in use or seal
  - if there is no cert data in slot 0 and 1, cfgiMpb2Read function returns ISTATUS_MPB2_ENTRY_NOT_PRESENT. Based on this error, FW will allow IMPORT command.
3) Slot Mgmt:
- Reject command if slot request is already seal
- Reject command if slot request does not exist

Issue Description: Import is successful for already sealed slot(for eg : slot5) , import should be blocked as already slot is configured .
Also for sealed slot it should not be allowed to import.

Steps To Reproduce: Trigger Export , Import and Slot management commands from stolcli

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Defect ID: DCSG00131571
Headline: Aero A0: External cards do not support PCIe and SRIS by default
Description Of Change:
Enabled NVMe support by default for external cards.
Issue Description:
NVMe support was disabled for external cards.
Steps To Reproduce:
inspect partial XML for external Aero cards.

Defect ID: DCSG00131574
Headline: (SATA Only) MODE SELECT (6|10) to SATA drive with DEXCPT set fails if DEXCPT is already set.
Description Of Change: Don't send enable/disable Smart feature set to the SATA drive if it is already set to desired value and complete the SCSI Mode Select command with success.
Issue Description: SCSI Mode Select command with DEXCPT (disable exceptions) to a SATA drive that supports SMART feature set results in ATA command to disable SMART. In case the SMART feature is already disabled on the drive, then sending another disable SMART command by controller was resulting in command being failed by the drive which in turn fails the SCSI mode select command.
Steps To Reproduce: Send SCSI mode select command with page code 0x1C (information exception) and DEXCPT bit set. First time the command will be successful, second time onward the command will be failed with check condition.

Defect ID: DCSG00132639
Headline: [Aero] Fault 0xA03 observed when updating FW with a bad NVMe drive in the topology
Description Of Change: Do not cleanup NVMe initialization Mid when Initialization failed with timeout.
Issue Description: when NVMe init is failed with timeout, we do clean up and clear the NVMe initialization Mid as invalid
NVMe Initialization timeout triggers TM (TaskManagement) which tries to free the same Mid again, leading to 0xA03 fault.
Steps To Reproduce: 1. Put a bad NVMe drive in the topology which will fail the NVMe initilization.
2 Upgrade the FW to 14.250.13.00 FW.
3.Here update is successful but seeing the fault 0xA03 in FW and driver logs.
4.After updating the FW controller is not seen in the OS.

Defect ID: DCSG00134207
Headline: PL backend PCIe: PL fault 0xD308 is observed with Aero and Atlas connected in bad clock environment
Description Of Change: When handling PCIe error events in MPI event handling function, do not start MPI initialization if device is found missing.
Issue Description: The fault indicates MPI device initialization is in progress during DMD(Device missing delay) cancel handling.
When DMD is started, flag to indicate MPI initialization in progress is set to 0.
But when handling PCIe error events, MPI init is started and the flag is set again.
Now the device comes back and while cancelling DMD the fault is hit as the flag indicates MPI init is in progress.
Steps To Reproduce: Boot the server with Aero and Atlas connected in bad clock environment.

Defect ID: DCSG00134669
Headline: Index out of range is observed for print in ring buffer logs
Description Of Change: The maximum debugh string variable is intialized with appropriate value.
Issue Description: The maximum debug string variable which is compared against every index to ensure the index is in the range is set to 1 less than the max value.
This leads to misleading print index out of range for the last debug string.
Steps To Reproduce: Read security pages from persistent region.
Observe index out of range print in ring buffer logs.

Defect ID: DCSG00134906
Headline: Failed NVMe drive repair start command does not get report back properly
Description Of Change: Apply the mask to IOCStatus to get the IOCstatus properly.
Issue Description: The repair start command got failure status from PL, but it did not get propagate correctly to StorCLI.
Steps To Reproduce: Inspect code of NVMeRepairStartReply.

Defect ID: DCSG00137138
Headline: Fix PD initialization abort issue on non secure erase SATA SSD
Description Of Change: Do not block the abort if there is no secure erase active.
Issue Description: Trying to stop a SATA SSD init, but failed.
Steps To Reproduce: See reproduce steps.

Defect ID: DCSG00138244
Headline: MR 7.14 Alpha: Unexpected OCR caught by automation, FW update issue
Description Of Change: FW will not have this timer active before calling FlashWrite.
If somehow FlashWrite return failure, FW should restart timer to track the case if application does not send a close on it.

The fix only address the issue from FW exception.
It is observed that script sends an update with OFU. However, script still bail out saying it doesn't expect an OCR.
FW is working as expected (no exception) after this fix.
If still hitting script issue after this fix, script developer may want to dig further on this.
Issue Description: MR_DCMD_CTRL_FLASH_FW_FLASH, on top of this case, FW start 2min timer, but FlashWrite trigger multiple TtyFlashErase.
Eventually, this exhausted the timer while FlashWrite still have not returned. And FW auto close flash context.
Result in exception once FlashWrite return.
Steps To Reproduce: Issue flash FW ROP, script detect extra OCR.

Defect ID: DCSG00138303
Headline: PD FW Download support bit is repurposed to FW Download in progress
Description Of Change: Use the adapter status bit for support PD FW download to repurpose it for FW Download in Progress.
Issue Description: Currently the adapter status bit for support PD FW download is used by StorCLI in two places, support FW Download and download in progress, which is a conflict.
Steps To Reproduce: StorCLI show all.

Defect ID: DCSG00139362
Headline: A8: Aero MR 7.14: Intermittent issue: Assertion failure in fw\raid\taskman.c at line 361 , when tried to start IO's on SAS SSD 24 expander connect RAID5 RW Windows 2019
Description Of Change: Properly initialized some global variables so that multi processor NVRAM logic functions properly.
Issue Description: When running IO's on SAS SSD 24 expander connect, RAID5 RW, on Windows 2019, IO's hang, and a Kill Adapter results.

Found while running the performance test suite.
Steps To Reproduce: Intermittent issue:

Found while running the performance test suite for RAID5 Random write.

1) Connect 24 SAS SSD drives with 2 expanders.
2) Create 3 R5 VD's wit WT, NoRA andt Strip=64
3) storcli.exe /c0 set cc=off

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4) storcli.exe /c0 set patrolread=off
5) storcli.exe /c0 set alarm=off
6) storcli.exe /c0/vall set autobgi=off
7) storcli.exe /c0 set ds=off type=4
8) Goto diskmgmt and initialize volumes.
9) Now launch IOMeter and we hit Assertion failure

Defect ID: DCSG00139459
Headline: Crucial assert print is missing from Snapdump
Description Of Change: The missing eTTY code was added.
Issue Description: One of the paths through the print code was missing eTTY.
Steps To Reproduce: Boot up the controller. Force an assert to occur. Any assert will suffice. This can be done with Megamon. Compare the prints on the Uart and eTTY.

Defect ID: DCSG00139682
Headline: The test tool does not reflect correct bad block count when additional bad blocks are added
Description Of Change: When bad block is registered then update bad block counter in nvram.
For warm reboot case, then update the nvram with bad block count as well as other static info in same structure.
This fix is to handle the case when nvram is cleared. The information in same request will be updated to contain correct info, such as controller count, chip count, and device name.
Issue Description: The test tool does not reflect correct bad block count when additional bad blocks are added.
Additional bad blocks are added using debug monitor.
After bad blocks are added, then the test tool is still reporting the previous count.
A warm reboot still shows same results.
Only a cold reboot will result in the correct bad block count.
Steps To Reproduce: Use test tool to dump the bad block counters
Add bad block using debug monitor
Verify updated counters using test tool.
Warm reboot, then verify counters with test tool

Defect ID: DCSG00148775
Headline: NVMe devices VPD page 83 NAA descriptor may conflict with EUI64 ID reported
Description Of Change: Modified FW to report the VPD page 83 NAA descriptor for NVMe devices in new format in MS-SES synthesized SES Page 0Ah by reversing the EUI64 and converting to NAA to prevent the VPD ID collisions.
Issue Description: VPD83 page for NVMe devices report EUI64 ID and EUI64 is modified for NAA descriptor for associating NVMe devices with MS-SES Synthesized SES Page 0Ah. There are some NVMe devices which report EUI64 with upper nibble already set to NAA value (03h) and FW modifying EUI64 upper nibble for other devices seems to cause VPD83 ID collisions.
Steps To Reproduce: Install NVMe devices behind managed switch which is attached to MR HBA and boot up.

Defect ID: DCSG00148922
Headline: Fix unintended update of BBM Long size.
Description Of Change: When handling illegal mpt request, do not update BBM long size if the result will become 0.
Issue Description: BBM Long size set to zeor unexpectedly and causing write long at puncturing an LBA with 0 transfer length.
Steps To Reproduce: Run test set up with drives with UNCOR not supported.

Defect ID: DCSG00149010
Headline: MR_7.14 Alpha DBU: VMWARE reported IOMMU fault detected for vmhba3(Ventura IMR).
Description Of Change: Rearrange the command Completion resource clean-up, so we are cleaning
1) Post response frame
2) Chained/SGE mids
3) Free host Mids
Issue Description: During Command completion, freed lmid resource was accessed. This resulted in an indeterminate behavior.
Steps To Reproduce: Run heavy IO with MFI & MPT IO mixture.

Defect ID: DCSG00150120
Headline: 7.14 SPDM client code fix: Enable Route By ID for all the packet.
Description Of Change: FW will use tgtID now to route SPDM response back to BMC.
Issue Description: While helping customer to test their BMC on SPDM commands, root cause this bug that cause packet is not routed correctly.
Steps To Reproduce: Use customer system with customer BMC to issue SPDM get_version commands.

Defect ID: DCSG00150282
Headline: Correct SPDM python script StepsToRun.txt, remove redundant bmc.tar.bz2 file.
Description Of Change: With latest DCSG00134284 BMC image Alpha Release: BMC_EMUL - 00.02.00.00 Firmware
Python script can run directly with default emulator _S50Mctpd process.
So remove all the bmc.tar.bz2 dependency
Issue Description: With latest DCSG00134284 BMC image Alpha Release: BMC_EMUL - 00.02.00.00 Firmware
Python script can run directly with default emulator _S50Mctpd process.
So remove all the bmc.tar.bz2 dependency
Steps To Reproduce: None

Defect ID: DCSG00150798
Headline: SCSI Passthrough format command on unconfigured good drive causes kill adpater
Description Of Change: Outstanding commands on un-configured good drives are terminated after 35 seconds, when command block is pending within firmware.
Issue Description: When the format command is pending on a un-configured good drive, firmware is not terminating commands while command block is pending.
Steps To Reproduce: 1. Using storelibtest issue SCSI format on unconfigured good drive
2. While format is pending, create a raid volume on different drive. (After 35 seconds hang in application, VD create command completes and within FW format DCDB command terminates).

Defect ID: DCSG00151556
Headline: Applications displays incorrect PD count with SATA drive in enclosure on multi-path configuration
Description Of Change: Enclosure structure bit are updated according to reflect the drive count appropriately in each path of enclosure.
Issue Description: When SATA drive is connected in multipath configuration, PD count and device IDs are not correctly reflected in each path of enclosure.
Steps To Reproduce: 1. Connect an Aero controller to the system.
2. Connect an enclosure in multipath.
3. Keep some SATA drives in the enclosure.
4. Flash latest MR FW package on the system.
5. Launch SLT -> Main Menu -> Option 3 and then press 5

Defect ID: DCSG00151683
Headline: MR_7.14 Alpha DBU: Ventura iMR FW received a command "getCdbPtrAndTargetId: Invalid cmd fa", it result to KA on VMWARE OS.
Description Of Change: During skinny host memory poll command copy to SRAM, reinitialize the CRDs that were copied from. So this freed CRD could be safely re-used.
Issue Description: During skinny host memory poll command copy to SRAM, reinitialize the CRDs that were copied from. So this freed CRD could be safely re-used.
Steps To Reproduce: run Vmware DDV tool.

Defect ID: DCSG00152618
Headline: Aero Host Application Loading Changes to Support CTRL-R
Description Of Change: Updated a flash base address and a flash header offset needed in order for Aero to support loading the CTRL-R application.
Issue Description: Various flash base address and flash header offset updates are needed in order for Aero to support loading the CTRL-R application, and will be fixed via this defect.
Steps To Reproduce: N/A

Defect ID: DCSG00152802
Headline: Fix assert in etty debug code
Description Of Change: Code was added to acquire the lock.
Issue Description: There is locking that is required to print. A portion of the code was not holding the lock while printing.
Steps To Reproduce: Flash different ROPs to test loading new firmware.

Defect ID: DCSG00153860
Headline: Upto 90% performance drop with expander attached configuration.
Description Of Change: A flag added to check if the hardware workaround to force the dma grouping to be expander based was applied to a particular SAS core. In case the flag is set always return true for the function that checks if hardware workaround is required or not.
Issue Description: Due to an hardware bug, if there are more than 1 expander attached to same SAS core the dma group setting of device based dma group (each device with its own dma group) may lead to performance drop. To overcome that a hardware workaround was added where if all 8 phys of a SAS core are not attached to a single expander, then the dma grouping was forced to be expander based (same dma group for all devices attached to expander).
However in case the expander is attached after first port enable, there is a chance that one connector (4 phys) is attached after a few seconds. This can cause the above hardware workaround to be applied to some devices and not applied to devices discovered later and also incorrectly set the dma port limit for the expander causing a significant performance drop.
Steps To Reproduce: 1. Attach an expander with 32 SATA drives to the controller.
2. Disable all controller facing phys of the expander (wait till all devices are removed).
3. Enable the controller facing phys of the expander one by one with a small pause between enabling two phys.
4. Run write IOs performance test to the SATA drives and observe a performance drop.

Defect ID: DCSG00166684
Headline: OOB : Controller is not discovering thru OOB Storelibtest in pcie mode on loading /unloading SLT multiple times.
Description Of Change: Now, once OOB_GetStatus or OOB_HandleGetPollCmd is processed, set oob command state to SEND.
So the follow up resume will transfer dcmd response data and free the command.
Issue Description: OOB_GetStatus dcmd resume is not working correctly after earlier changes from
DCSG00126744 "SPDM_FW : SPDM commands are failing in OOB SL/SLT on Trinity M6 servers."
Since FW change handling resume command to only process dcmd response when oob command state is SEND.
Steps To Reproduce: Have a CISCO Aero controller on CISCO 1U Trinity system with latest FW .
Login to BMC terminal. Launch SLT .
Storelib loads, verify the controller info. Do some OOB stress operations.
Unload the SLT.
Repeat load/unload SLT several times.
In some point of time , SLT fails to discover and exits with " no controller found " message.

Defect ID: DCSG00167682
Headline: Running format on a EPD once one has started is causing a KA.
Description Of Change: When drive reports sense key LUN_NOT_READY, device spinup recovery is performed only on few SCSI ASCQ codes.
Issue Description: While running format on multiple EPD or JBOD drives, host is issuing commands like read capacity. This is causing the drives to report sense code 2/4/4 and firmware is issuing device spinup recovery and eventually kill adapter happens.
Steps To Reproduce: 1. Create an EPD or JBOD
2. Start format on multiple drives
3. While format is in progress, issue read capacity SCSI command

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Defect ID: DCSG00181406
Headline: Fix error handling in traceTool.py
Description Of Change: The typo was corrected.
Issue Description: There's a typo in a variable name. So a python error occurs instead of printing a useful error message and exiting.
Steps To Reproduce: Add an empty print statement to the firmware (mprintf();), and do a compile.

Defect ID: DCSG00212038
Headline: MR 7.14 Beta: OCR did not complete appropriately and assert didn't print properly
Description Of Change: The function call was corrected to also pass the data arguments.
Issue Description: Part of the firmware that reads user input from the Uart passes a printf string with conversion specifications, but not the data arguments to format. So firmware uses random values from the stack as the data arguments. This causes firmware to occassionally crash.
Steps To Reproduce: Run an OCR and repeatedly break into Megamon during start-of-day.

Defect ID: DCSG00212751
Headline: Fix mistaken warning of drive degradation detection messages
Description Of Change: check the recovery time spent correctly against non-zero preset limit.
Issue Description: Every time a medium error is handled, such drive degradation message shows up.
Steps To Reproduce: Follow reproduce step for ME injection and start CC.

Defect ID: DCSG00214223
Headline: iMR boot stuck in creating slot mapping
Description Of Change: Disable the debug flag for slotmapping and phyDes print.
Issue Description: iMR controller cannot boot into OS and stuck in creating slot mapping.
Steps To Reproduce: See reproduce step.

Defect ID: DCSG00214265
Headline: Correct Sblib Int make sure ER 110403 and ER 166877 are present
Description Of Change: Correct Sblib Int make sure ER 110403 and ER 166877 changes are present
Issue Description: baseline 05/01 is from sy727730, baseline 03/22 from Phillip.
But there was another delivery on 0403 from Chenna, SECUREBOOT_LIB_INT does not auto-create baseline with that.
This delivery is from 131835 with ER 110403.

This defect is used to check latest sblib_Int have changes from ER 11403 and ER DCSG00166877 (latest change).
Steps To Reproduce: None

Defect ID: DCSG00215378
Headline: MR 7.14 Beta: Assertion failure in fw\raid\mpthostcmd.c at line 3213: crd->mptReqDesc.Default.SMID
Description Of Change: undo iMR IOMMU error issue (DCSG00149010), changes that made to order of freeing LMID, SMID and chained MIDS logic during completion path.
Issue Description: As part of iMR IOMMU error issue (DCSG00149010), changes were made to order of freeing LMID, SMID and chained MIDS logic during completion path. These changes were abruptly affecting commands that are currently processed leading to command failing with different errors.
Steps To Reproduce: Have hit this twice. System was able to recover from it during first hit as OCR was still turned on. Seems like there were more than one OCR before I realized something was amiss.

Script is running TMs and drive pulls to aero behind atlas on atlas eval/validation boards with 16 drives each.

Next step, while dev looks at logs, is to determine if it is TMs or drive pulls, or the combination that is causing the issue.

Defect ID: DCSG00215388
Headline: Correct Sblib Int make sure ER 110403 and ER 166877 are present (2)
Description Of Change: Port sblib.c change from ER 110403 again.
Correct minor logic from ER 166877.
Issue Description: sblib.c does not have change from ER 110403.
Steps To Reproduce: None

Defect ID: DCSG00215476
Headline: MR7.14 Beta: Firmware hit exception stuck while IOs and rebooting, causing no controller found

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Description Of Change: Additional checking was added to make sure the contents of this field is used appropriately.
Issue Description: There is a per IO data structure with a large union. One of the fields is used differently when media errors occur. However, firmware was not accounting for this which led to a crash.
Steps To Reproduce: Inject media errors into a drive with IO running and reboot.

Defect ID: DCSG00216908
Headline: NVRAM changes for supporting dynamic recon ghost tgtId
Description Of Change: Added new flags to maintain recon ghost tgtId across FW resets
Issue Description: NVRAM changes for supporting dynamic recon ghost tgtId
Steps To Reproduce: Not applicable.

Defect ID: DCSG00225935
Headline: PL SATA only : SATA init timeout observed due to drive taking longer to respond to sanitize status ext
Description Of Change: During SATA initialization, issue check power mode and then sanitize status ext is issued only if check power mode fails.
As per SATA specification, if sanitize is in progress drive will fail check power mode.
Issue Description: Sata initialization timeout is set to 3 seconds. As part of SATA initialization, PL sends sanitize status ext to check if sanitize is in progress on the drive.
As certain drives fail to respond to santize status within 3s and takes longer to respond, multiple SATA initialization timeouts are observed leading to drive reset.
Its obseved that drives take longer to respond when the drive is in standby state.
Steps To Reproduce: - Drive is in standby state
- power on the drive

Note:
This issue is observed only with certain drive models.

Defect ID: DCSG00225977
Headline: Implicitly error when converting an expression to a narrower type
Description Of Change: Typecast to U16 for a field containing last sector size.
Typecast to U32 for a field containing the block number.
Typecast to U16 for a input parameter to function containing the page count.
Issue Description: various errors reported by static analysis tool
Steps To Reproduce: static analysis tool was used to find these errors

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Defect ID: DCSG00231422
Headline: PL NVMe : PCI task management is not getting completed.
Description Of Change: During FPE pend queue clean up, scan through the pended mids for TM marker mid.
If TM marker mid submitted to FPE for control queue clean up is found, then resubmit the mid to FPE
after the pend queue clean up(when the pend queue is empty).
Issue Description: During PCI TM hardware queue clean up, marker mid is submitted to fast path engine.
The expectation is we get an exception for marker mid and TM advances to the next state.
But the marked mid is getting added to hardware device pend queue and later moved to PL pend queue.
Due to this, TM is not advancing to next state and not getting completed.
Steps To Reproduce: Raid operations are performed, IOs are started and drives are pulled.
Due to some device related error, internal task management is triggered.
This task management does not get completed.

Defect ID: DCSG00234826
Headline: NVDATA XSD in MR is out of sync from the latest spec
Description Of Change: Update NVDATA to include new IOUnitPage11 information
Issue Description: IOUnitPage11 does not have the latest fields.
Steps To Reproduce: check page details.

Defect ID: DCSG00234837
Headline: PL fault 0xE40E observed accessing unconfigured MPI backend device registers through CLI cmd
Description Of Change: Added check in FW to ensure MPI Device memory mapped register address is initialized for dumping register info else the register dump is skipped.
Issue Description: During PCIe SW MPI device enumeration; if UART command CLI is executed to dump MPI device register information it will lead to 0xE40E fault. The FW faults to prevent uninitialized/ unconfigured device memory mapped registers.
Steps To Reproduce: During PCIe SW MPI device enumeration, issue pl mpidev dbg or initiate Storcli get snapdump command and observe the FW faults with 0xE40E.

Defect ID: DCSG00234911
Headline: Merge conflict issues
Description Of Change: With the last delivery found there were bunch of code missed out which causing compilation errors
Issue Description: With the last delivery found there were bunch of code missed out which causing compilation errors
Steps To Reproduce: compilation error.

Defect ID: DCSG00243819
Headline: Secure SED and SES Management ctrl properties are toggling after changing autoconfig from None to JBOD and vice versa.
Description Of Change: Megaraid params page is updated with appropriate default settings for secure SED and SES management bit in Nvdata
Issue Description: Secure SED and SES management bits are not matching with defaults.
Steps To Reproduce: Set the 9580-16i controller factory default using storcli - Storcli64 /c0 set factory defaults and reboot.
Check the default settings using storcli - Storcli64 /c0 show autoconfig.

Defect ID: DCSG00290593
Headline: NVMe Init Error: Device with no namespaces shows 'Namespace count Invalid' as Unrecoverable Error
Description Of Change: Modified the PL FW to make sure that the Namespace Management feature flag from its internal structures are referenced only after it is populated using the Identify controller response.
Issue Description: Before setting the flag that a drive with invalid namespaces is recoverable or not, PL FW checks if the drive supports Namespace Management feature. If the Namespace Management feature is not supported then we mark the drive as not recoverable. In this case the drive had the Namespace Management feature enabled, but the PL FW was referencing this feature flag from its internal structure even before populating the same using the Identify controller response and there by marking the the drive as not recoverable.
Steps To Reproduce: 1. Delete all the Namespaces on a NVMe drive
2. Connect the drive behind PERC controller and boot up.
3. Observe NVMe init error reporting status in HII and PERCCLI

Defect ID: DCSG00297592
Headline: [9440-8i + MR7.14 ARM/X86] Auto config RAID0 in HII didnot work as expected
Description Of Change: Fixed an Auto Configure retrieval parameter for iMR.
Issue Description: In MegaRAID MR7.14, HII add one menu "Auto config RAID0".
But when there are Unconfigured Good drive connected to controller, and choose "Auto config RAID0", it doesn't work as expected. No drives are configured as RAID0. Also there is error message "The requested commands has invalid arguments".
Steps To Reproduce: Launch HII and check Configuration Management menu.

Defect ID: DCSG00307042
Headline: API clarification for large io support
Description Of Change: The description of Large IO feature bits was corrected.
Issue Description: In the comments, the description of the support bits for the Large IO feature is misleading.
Steps To Reproduce: This issue was found by inspection.

Defect ID: DCSG00312453
Headline: [9440-8i + MR7.14 + ARM] Controller hit Fatal error when doing drives hard reset test by storelibtest
Description Of Change: Free spin up buffer after the drive spin up completes
Issue Description: A spin buffer used during spin up state machine was not freed, causing controller to run out of memory when multiple drives went through spin up recovery in a loop.
Steps To Reproduce: Issue hard reset on multiple drives in a loop, while running IO's on them.

Defect ID: DCSG00312708
Headline: [MR3508+MR7.14 +X86] Controller is seen with Fatal error by unknown reason unexpectedly (XH628 V5's 3508 mem.c issue)
Description Of Change: Additional checking was added to the DCMD processing firmware. Processing will stop early when inconsistencies are found. This prevents over writing adjacent memory and asserting.

However, this does not explain the malformed DCMD. Since the issue cannot be reliably reproduced, further progress is not possible at this time. To make future debug easier, additional debug is being included.
Issue Description: A malformed DCMD was processed by firmware. This caused the firmware to allocate a smaller buffer than was needed. Firmware then over wrote an adjacent data structure. This led to an assert in the memory management firmware.
Steps To Reproduce: This issue has not been reliably reproduced. However, it is known to fail with 35xx controllers and the 7.14 GCA ROP.

Defect ID: DCSG00318971
Headline: 9460-16i MR FW marks Zoned Out PHYs as bad PHYs
Description Of Change: Changed MR FW to not mark PHYs as bad if status indicates that device access is not allowed.
Issue Description: Zoned Out PHYs are no more accessible to MR FW until it gets zoned In.
Expander sets status as access not allowed for these Zoned Out PHYs.
MR FW marks this Zoned Out PHYs as BAD without checking whether access is allowed or not.
Ideally this PHYs won't be accessible to MR Controller and shouldn't be marked as bad.
Steps To Reproduce: Expander with T10 zoning enabled, MR FW marks Zoned Out PHYs as bad PHYs.

Defect ID: DCSG00322761
Headline: Atlas Behind Aero BST is not working as the correct XML file is not copied.
Description Of Change: The correct XML file is copied.
Issue Description: Atlas Behind Aero BST is not working as the correct XML file is not copied.
Steps To Reproduce: Run the Atlas behind Aero BST.

Defect ID: DCSG00013123
Headline: VSES may not report valid SES Page 0Ah elements for one of quads attached elements in a UBM backplane.
Description Of Change: VSES may not report valid SES Page 0Ah elements for one of quads attached elements in a UBM backplane. In a UBM backplane configured for x8 HFC I2C mode with HBA attached have the quads BP type report as I2C by default, then the Firmware's may not properly configure the HFC groups. This leads to VSES marking the HFC connector group attached elements as invalid.
Issue Description: 1) Connect MR OEM HBA to OEM UBM 10 bay backplane
2) Install 8 NVMe drives to UBM DFCs 0-7
3) Reboot to HII and observe only 4 NVMe drives listed.
Steps To Reproduce: Modified the FW logic to configure the UBM HFC grouping appropriately for this configuration.

Defect ID: DCSG00013397
Headline: pl: discovery failure if PCIe backplane detection is disabled
Description Of Change: Fixed a bug that caused some of the port enable time initialization to be blocked when backplane detection is disabled.
Issue Description: If PCIe backplane detection is disabled, port enable will time out and attached devices will not be discovered.
Steps To Reproduce: Bring up firmware on a Ventura eval board.

Defect ID: DCSG00014628
Headline: pl: NVMe: fix a couple of debug issues related to unique identifiers
Description Of Change: Fixed the unique identifier printing in the 'pl pci prot' console command and added debug prints for the mismatch cases.
Issue Description: Some of the unique identifier information is printed incorrectly by the 'pl pci prot' diag console command. Debug of unique identifier mismatch cases would be difficult without debug prints that are generated in those cases.
Steps To Reproduce: Code inspection.

Defect ID: DCSG00012487
Headline: Aero A0: vSES is created even for managed Atlas (Ibanez) switch
Description Of Change: Eliminated case where an empty VSES was created for Atlas as we no longer support unmanaged Atlas switches
Issue Description: A Phantom VSES was created due to old logic left in the code
Steps To Reproduce: Connect two EX1 UBM enclosures and one Atlas Ibanez switch

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Defect ID: DCSG00014510
Headline: Scrutiny GUI clear option fails to reset the PCIe error counters.
Description Of Change: Added the support for clearing PCIe error counters in MPI IO unit message handler.
Issue Description: PCIe link error clear operation is not handled in MPI IO unit message handler. Hence the clear PCIe link error operation fails from scruitny GUI.
Steps To Reproduce: 1. Load the HBA with latest latest firmware
2. Introduce PCIe link errors by cable/drive hot plug
3. Using clear option try to clear the PCIe error counts.
4. Read the link error using Read phy error option.
5. Observe that still we are able to see the Correctable error count in the PCIe error window.

Defect ID: DCSG00015943
Headline: pl: backend PCIe: IO halt following temporary device removal
Description Of Change: Place modified port status information in the PCIe Topology Change List event on successful rediscovery following repeated event generation when the device is in the Delay Not Responding state.
Issue Description: If an NVMe device is disconnected from the HBA and is then reconnected before its Device Missing Delay timer expires, the initial rediscovery of the device fails for a reason other than Config Retry Status (e.g. the PCIe link happens to be in recovery when discovery runs), and neither the width nor the speed of the PCIe link change before the device is successfully rediscovered, the PCIe Topology Change List event entry describing the device will contain port status information that may be unexpected by the host driver. This may cause the host driver to refuse to resume IOs to the device.
Steps To Reproduce: Perform link break testing with NVMe devices under Linux.

Defect ID: DCSG00013404
Headline: Aero: NVMe: device not removed if init fails and it then goes missing
Description Of Change: Fixed a bug that caused unreported device cleanup to not occur in the described case.
Issue Description: If an NVMe device is attached, NVMe initialization fails with an error that causes NVMe init to be retried but it doesn't fail a sufficient number of times that PL gives up on initializing the device, and the device is then pulled, the PL structures associated with the device aren't cleaned up after its device missing delay timer expires.
Steps To Reproduce: Induce errors while performing NVMe device push/pull testing.

Defect ID: DCSG00019925
Headline: pl: backend PCIe: 'pl pci dbgall' causes ring buffer spam
Description Of Change: Disable good path config transaction ring buffer prints while handling these diag console commands.
Issue Description: When backend PCIe debug logs are dumped with 'pl pci dbgall' or 'pl dbg', 1024 ring buffer prints are generated per PCIe entity due to the config space reads that occur during these diag commands. This may cause useful prints to be ejected from the PL ring buffer in favor of the non-useful config space read prints.
Steps To Reproduce: Issue 'pl pci dbgall' and then examine the PL ring buffer dump.

Defect ID: DCSG00017373
Headline: Multiple VSES created on SAS only 8-Slot UBM backplane with duplicate slot assignments
Description Of Change: Fixed incorrect reference of CSW core index by FW with SAS only FW attaching to UBM backplane.
Issue Description: Multiple VSES may be created on SAS only 8-Slot UBM backplane with duplicate slot assignments.
Steps To Reproduce: Attach 94xx-16i HBA to SAS only 8-slot UBM backplane and boot up to OS. Observe multiple VSES instances created with duplicate slot number assigned to drive slots.

Defect ID: DCSG00014455
Headline: pl: NVMe: unexpected task management halt may occur
Description Of Change: Clear the device's config transaction error status before performing path analysis following Device Missing Delay timer expiration with a hot reset TM outstanding to the device.

Fixed a bug that caused the timer restart to be applied to outstanding hot reset TMs for all NVMe devices, not just the device for which the triggering event occurred.
Issue Description: If a task management request that issues hot reset to an NVMe device is outstanding and a discovery failure due to a temporary condition (e.g. link in bad state) occurs after the device's Device Missing Delay timer expires, the task management request may be unexpectedly halted.

If task management requests that issue hot reset are issued to multiple NVMe devices, an internal timer may be unexpectedly restarted for all of the task management requests after one of the NVMe devices is rediscovered. This could cause an unexpected internal timeout and subsequent TM halt.
Steps To Reproduce: Perform simultaneous device add/removal testing with several NVMe devices.

Defect ID: DCSG00021412
Headline: Aero: Powered cycled managed switch SES can become inaccessible
Description Of Change: Extended the IO quiescing to handle more than 32 PCI devices.

Corrected the location that checks if an MPI attached device is hidden and was incorrectly failing for a managed switch SES.
Issue Description: Having more than 28 NVMe/PCIe devices configured in ManPage9 with a in powered cycled managed switch results in its SES (Atlas's SES) becoming inaccessible.

When the switch is powered back on the firmware will quiesce IOs on the root port, but this only accounts for 32 PCIe Devices and not the additional ones generated by MPI Device support.

A secondary issue was a check in PL for IOs to the managed switch SES, which was checking the wrong location if it is supposed to be a hidden MPI attached device. This caused a different error to be passed once the quiescing issue stopped occurring.
Steps To Reproduce: Configured NVDATA's ManPage9 to have more than 28 PCI Devices. Attach many NVMe drives.

Attach a managed switch with drives attached to the switch.

Power cycle the switch off (long enough to cause the switch to be removed) and back on.

Try to send IOs to the Atlas SES (whether through IOP or host).

Defect ID: DCSG00022691
Headline: UBM Link Config may fail for HBA connector with Phys routed spans CSWs
Description Of Change: Updated fw to allow link configuration for connector with Phys routed spanning CSW attaching to UBM backplane.
Issue Description: Ventura chip supports max 4 x1 links per CSW and FW checks for Phys on the HBA connector to be within a CSW for max x1 link configuration. Some Aero custom board designs have single connector routing 12 Phys, spanning CSW and this check causes backend PCIe link configuration to fail.
Steps To Reproduce: Using OEM x12 board with NVDATA setup for x12 connector lane mapping attached to UBM backplane.
Boot up the FW and observe backend PCIe support disabled for the Phys routed on x12 connector.

Defect ID: DCSG00019315
Headline: 0x6231 Fault during Sata Task Management
Description Of Change: Added a check to make sure a timer is still running before attempting to stop it
Issue Description: The SATA Task Management code was attempting to stop a timer for an aborted IO that was already stopped.
Steps To Reproduce: Run repeated multipath failover w/ I/O
Booted with 2 enclosures attached. Then removed SAS drives and put SATA in one enclosure and shutoff the other.
Also added the 2nd path and then started test.

Defect ID: DCSG00012593
Headline: pl: NVMe: E425 fault after vendor specific device firmware update
Description Of Change: Made two changes to PL's NVMe unique identifier validation behavior:

1. During an NVMe init session, if an NVMe device presents unique identifiers that differ from those that it presented during a previous NVMe init session, cause the device to be reported missing. After it is removed, rediscover it as a new device. The faults that previously occurred on unique identifier validation failure will no longer occur.

2. Add a flag that allows NVMe unique identifier validation to be disabled by the user: Manufacturing Page 11 AddlFlags2 bit 8. The default setting is 0 (unique identifier validation enabled).
Issue Description: When the firmware on a vendor specific NVMe device is updated, an E425 fault occurs after the device reset that is performed following the firmware update. It appears that the Namespace NGUID reported by the device is changing after the firmware update.
Steps To Reproduce: Update firmware on a vendor specific NVMe device.

Defect ID: DCSG00022805
Headline: pl: backend PCIe: EC5B fault
Description Of Change: If this condition occurs, do not attempt to configure a backend PCIe component unless PCIe Discovery has granted permission to configure it.
Issue Description: If PCIe Discovery runs and bypasses enumeration for a switch attached endpoint because the associated downstream port lockout timer has not yet expired, PCIe Device Manager will nonetheless attempt to configure the endpoint if the timer expires within the timing window between the start of the current discovery session and when DevManager is called to configure the topology attached to the given root port. If the endpoint is attached to an Atlas synthetic mode switch, this may cause an EC5B fault.
Steps To Reproduce: Perform device add/removal testing with an Atlas switch and attached NVMe devices.

Defect ID: DCSG00023764
Headline: Ventura B0: Incorrect VSES associated to unmanaged PCIe SW enclosure
Description Of Change: Fixed FW to associate appropriate VSES device to right enclosure
Issue Description: On a 9400-16 attached to unmanaged PCIe SW and to UBM backplane, boot up FW to observe vSES with drives associated from both switch and UBM.
Steps To Reproduce: 1. Connect 9400-16i to Capella II switch with NVMe drives
2. Connect 9400-16i to UBM backplane with SAS/NVMe drives
3. Boot system to SLES
4. Observe incorrect VSES to end device mapping from UART and storCli

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Defect ID: DCSG00018823
Headline: On Locating PD's,LED's are not blinking for drives connected to customer specific SGPIO Backplane.
Description Of Change: Updated Firmware to use slot number for SGPIO LED translation.
Issue Description: Existing code was using Phy number for SGPIO translation instead of corresponding slot number. Hence the firmware writes the LED update pattern to incorrect offset of SGPIO Port config register. As a result locate PD fails on the SGPIO backplane.
Steps To Reproduce: 1. Connect few drives to the SGPIO Backplane.
2. Connect SGPIO Backplane to HBA.
3. Boot to OS, From Storcli run PD locate command on all drives connected to Backplane.
4. Observe that LED's are not blinking after running PD Locate command.

Defect ID: DCSG00024555
Headline: Ventura B0: vSES goes missing after the first controller reset on UBM Ex1 in x8 HFC config
Description Of Change: Fixed UBM backplane enclosure attached Phymask creation logic to include Phys from all the HBA connectors attached to UBM backplane.
Issue Description: UBM attached device and VSES gets same slot number which prevent OS driver in adding to the VSES to device list during adapter reset.
Steps To Reproduce: Connect UBM x1 backplane in x8 HFC mode with SAS drives. Boot up to Windows OS, issue sg_scan command and vSES device listed.
Reset the controller using storCLI and issue sg_scan again, observe vSES device missing.

Defect ID: DCSG00020917
Headline: Channel SAS3.5 HBAs cannot support published PD limits when loaded with SAS/SATA-only FW image

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Description Of Change: Changed the RESOURCE_TARGETS Minimum to 1024 in Mfg. Page 9 in the NVDATA for Ventura, Marlin and Aero channel boards. This was done only for the SAS/SATA profiles to match Fury numbers. This will cause the firmware to always allocate 1024 targets.

Issue Description: The published supported number of devices is 1024. However, the NVDATA made it allocate between 128 and 1024 targets depending on memory availability.

Steps To Reproduce: Load up firmware and read the Actual field for RESOURCE_TARGETS in Mfg. Page 9 and notice it may be below 1024.

Defect ID: DCSG00022778

Headline: Aero-3: Serdes parameters from NVDATA are not sent to Serdes

Description Of Change: Added code to copy backend serdes settings from NVDATA and send them to the M0 processor that controls the serdes. Updated NVDATA with the default serdes values previously used. Updated M0 code with fixes to the messages to get and set serdes parameters.

Issue Description: The code to copy serdes settings from Mfg. Page 40/41 in NVDATA had not been enabled yet for Aero.

Steps To Reproduce: N/A

Defect ID: DCSG00026333

Headline: Ventura B0: vSES not reported in Windows 2019 on certain UBM backplane config

Description Of Change: Fixed the UBM Enclosure total Slots calculation based on starting slot number and max slot number assignment.

Issue Description: vSES device may not be reported in Windows 2019 on UBM backplanes with non-contiguous slot numbers.

Steps To Reproduce: Connect to UBM enclosure with non-contiguous slot numbering and boot to Windows 2019.
Issue sg_scan -s command and observe vSES not reported.

Defect ID: DCSG00023081

Headline: Backplane detection never completes leading to discovery timeout.

Description Of Change: Within the backplane detection state machine for connectors in a group that are in waiting state for other connector to complete detection, mark the detection complete for connectors connected to VPP type B backplane and are in I2C Polling state to check for drive presence.

Issue Description: During backplane detection out of 4 connectors two connectors 1 and 3 are found to be connected to VPP type B backplane and other two connectors 2 and 4 as per NVADATA setting are added to group waiting for backplane detection to complete on connectors 1 and 3. However for VPP type B backplane, the backplane detection state machine enters the I2C Polling state (to poll for drive presence) as the final state instead of detection complete state. So the backplane detection for connector 2 and 4 never completes.

Steps To Reproduce: Connect VPP type B backplane to the controller to connectors 1 and 3 and set NVDATA so that connector 2 and 4 are part of group with connector 1 and 3. Observe that initial discovery times out due to backplane detection never completing.

Defect ID: DCSG00027593

Headline: PL: Fault 0xD033 During Drive Pull Testing

Description Of Change: Added a check to validate the device handle and return a failure status if it's not valid.

Issue Description: A PLI interface function was called to start a SATA passthrough request, but with an invalid device handle of 0xffff. PL firmware was not validating the device handle. It passed the bad device handle to FPE manager code, resulting in a 0xD033 fault due to a bad memory access.

Steps To Reproduce: On customer system, connect SAS and SATA drives without an expander, and perform the following steps:
1. Pull 4 drives
2. Wait 90 seconds
3. Push 4 drives
4. Wait 90 seconds
5. Repeat.

Defect ID: DCSG00026985

Headline: Fault 0x265d seen when the UBM FRU I2C read size configured to 2 bytes.

Description Of Change: Skipped the printing of received data if the buffer address used is not DWORD aligned.

Issue Description: Misaligned I2C buffer print causes the data abort fault 0x265D due to smaller size chunks data size read in I2C transaction.

Steps To Reproduce: Configure the UBM FRU I2C read size to 2 byte in the NVDATA.

Attach an UBM Backplane to HBA and boot.

Defect ID: DCSG00030914

Headline: PL : PL fault 0x7C41 is observed

Description Of Change: Clear the FW context of internally generated IO used for sending SEP requests at completion.

Issue Description: PL fault 0x7C41 indicates that the message frame address is not in the allocated pool.
At IO completion on error, if the firmware context flags indicate its an internal IO, then PL tries to call the callback registered. During this time, we obseve fault since the message frame address is NULL.

While completing internal IOs generated for creating SEP request, the FW context of the message frame is not cleared. When the same mid is reused, due to stale data from previous use, PL misinterprets the host IO as an internal one and tries to access invalid data.

Steps To Reproduce: Run IOs on DA-SEP system and ensure some IOs hit error path.

Defect ID: DCSG00032146

Headline: NVMe crypto erase sanitize command is issued in restricted completion mode

Description Of Change: Set AUSE bit in DWORD10 of sanitize Admin NVMe command. This is to issue sanitize command in unrestricted completion mode.

Issue Description: Crypto erase Sanitize command is issued in restricted completion mode.

Steps To Reproduce: Not reproducible.

Defect ID: DCSG00032157

Headline: PL improperly cleaning up and recovering from hot resetting MPI Device (i.e. reinitializing MPI Device failing)

Description Of Change: When PL is reconfiguring an MPI Device because it seems to have lost its settings, added code to clear the MPI Device to reset the state management to initiate MPI Initialization, and clear out resources associated with the MPI Doorbell.

Removed code that hides the managed switch's SES when the MPI Device is not yet initialized (this is like NVMe).

Make sure to reflect the presence of the MPI Device in PCIe Device Page 0 even when it is not yet fully initialized (MPI Initialization).

Removed code that could disable the FPE timer against IOs to the managed switch SES so they can be properly cleaned up when the IOs are lost under some IOP confiugrations.

Added code to properly clean-up when there are no frames for managed switch SES's SES Page 0Ah translation (occurred after the MPI Device came back).

Issue Description: Unable to access the SES through an MPI Device in a managed switch (Atlas) when multiple managed switches are attached with heavy IO load and multiple hot resets are issued to both root ports.

Steps To Reproduce: Perform multiple hot resets to the root port of an MPI Device in a managed switch, but have enough activity and additional devices being discovered to miss the MPI Device has gone missing.
This will typically require two managed switches, both of which are receiving hot resets.

Have IO running to the SES attached to the MPI Device immediately after reinitializing the MPI Device.

Defect ID: DCSG00027826

Headline: Cache data is lost after server power pull running IO on R5 and R6

Description Of Change: Force MR FW to set DRAM size to 4GB if 4GB to 8GB Migration is pending and cache was Dirty in previous boot.

Issue Description: MR FW is not handling 4GB to 8GB Migration gracefully.

Steps To Reproduce: Flash 4GB Firmware
Create R5 and R6 and init
Start testio
Flash 8GB DRAM Firmware on top of 4GB Firmware
After a couple minutes check for wj. If wj entries are present, pull power to system and restore.
Upon boot up, HII will display cache data was lost.

Defect ID: DCSG00032952

Headline: PL 0x4E00 fault occurs when Task Management Device Resets are issued to different manged switch SESes at the same time

Description Of Change: Added additional checks on the Task Management completion for TMs to MPI attached devices, like a managed switch SES, to make sure the frames are to the matching MPI Device.

Removed context clearing of TMs that find a matching frame on the Enclosure Management Queue. This allows other Task Management states to more easily match child frames to the top-frame on the Enclosure Management Queue.

Also corrected a problem where the reply free frame pool's can overlap between MPI Devices, which required proper offset calculations into the reply free frame pool for each MPI Device.

Issue Description: PL 0x4E00 fault occurs when Task Management Device Resets are issued to different manged switch SESes (MSSES) at the same time.

The first Task Management's completion tries to clean-up the second Task Management's frame to the MSSES's MPI Device.

Steps To Reproduce: Cause the IOP/MR or host driver to issue a Task Management Device Reset to two managed switch SESes at the same time.

Defect ID: DCSG00038775
Headline: pl: Ventura/Mercator: device side PCIe link failure following adapter reset
Description Of Change: On top of the fix added in DCSG00024652, added additional delay between asserting a modules, Module Specific Reset bit and clearing it.
Issue Description: After an adapter reset, device side PCIe links may take an unexpectedly long time to come up or may entirely fail to come up.
Steps To Reproduce: Perform adapter reset testing using Ventura with attached NVMe devices or PCIe switches.

Defect ID: DCSG00036978
Headline: UBM BP product revision version mismatch b/w SES Page 01 and SCSI Inquiry output
Description Of Change: Update the Product Revision Field in the SES Page 01 with the UBM Image version, if UBM backplane is connected to the controller and NVData indicates to override the product revision field with UBM Image Version value.
Issue Description: UBM BP revision version is different b/w SCSI Inquiry command and in SES Page 01
Steps To Reproduce: Execute sg_ses --page=0x01 <device> and sg_inq <device> command for the vSES device.

Defect ID: DCSG00025534
Headline: Dev Defect -Firmware asserted in ONFI module on OCR with Pinned cache.
Description Of Change: If controller supports COL Single Image feature, Skip ONFI Descriptor preparation in OCR and Pinned cache scenario.
Issue Description: If controller boots with Pinned cache, Device Health Manager should load and wait until User acknowledgment. In this case, Option ROM is not loaded, But System continued to OS and Driver loaded while Controller is waiting for removal of pinned cache. Driver issued OCR since controller is not responding after couple of seconds.MR FW tried to prepare ONFI descriptors on OCR, which caused the Assertion.
If Controller has Pinned cache and supports COL Single Image, MR FW should prepare ONFI for next Offload only when user acknowledges the Pinned cache Critical boot message from Device Health Manager.

Please Refer attached Write up for more details.

Steps To Reproduce: Installed RHEL 8 OS on Raid1_VD on BOSS controller (boot mode: UEFI)
Had acontroller in Raid Mode, Created Raid1_VD (size 50gb) via HII.
Booted to OS and Created Ext4 FS and then ran IO, using IO monkey (3.14.17) for around 15 mins (Parameters: t100, b512 f64)
Then stopped the IO, powered off the system
Replaced with an PERC controller in EHBA Mode. Then powered on the system.
Note1: It took 30 mins to boot to HII. Entered into HII.
Here selected Boot device as Boss controller and then allowed to continue normal boot.
Note2: it took around 40 mins to boot to OS.
Logged into OS , OS was hung, when checked in TTY log Montask was seen.

Defect ID: DCSG00032425
Headline: Debug message prints for controller that do not support NVMe.
Description Of Change: This is expected for the controller that do not support NVMe. Changed mprintf() to etprintf().
Issue Description: Debug message prints for controller that do not support NVMe.
Steps To Reproduce: Look for debug error message in FW log

Defect ID: DCSG00024573
Headline: Add debug code to enable debug fake flash error for OEM
Description Of Change: Added debug code to enable fake flash error for OEM for MR7.10
Issue Description: Add the debug fake flash error code to MR7.10
Steps To Reproduce: 1. ei enableDebugFakeFlash 1
2. eb debugFakeFlashError 0

Defect ID: DCSG00034489
Headline: Locate PD fail on SGPIO enclosure when GroupId is disabled in Nvdata.
Description Of Change: Updated Firmware to use phy number for SGPIO LED translation.
Issue Description: Existing code was using Phy number for SGPIO translation, when groupId is disabled we are using slot number to update LED pattern to incorrect offset of SGPIO Port config register as a result locate PD fails on the SGPIO backplane
Steps To Reproduce: 1) Connect the controller to SGPIO backplane.
2) Disable the GroupId in Manpage12 flags section of nvdata.
3) Issue the locate command on any drive.
4) Observe the locate fails.

Defect ID: DCSG00038944
Headline: Controller Cache lost is seen while running 200-loop Cache Offload Test
Description Of Change: Code change addresses below issues:
* Fix battery monitoring hole between primary and secondary during boot up.
* Increase the minimum amount of charge required to perform successful Cache Offload. These levels are mentioned by OEM in their latest spec.
* Fix next cycle time variable assignment so that monitoring always occurs every 5 secs.
Issue Description: Battery monitoring was not done by secondary core every 5 seconds.
FW had incorrect minimum charge value to perform successful cache offload.
Steps To Reproduce: Run long iteration cache offload test.

Defect ID: DCSG00022886
Headline: [Aero]Remove NVMe support for SAS/SATA profile only
Description Of Change: [Aero]Remove NVMe support for SAS/SATA profile only
Issue Description: NVMe is enabled in SAS/SATA profile ROM.
Steps To Reproduce: Update Aero card with latest SAS/SATA profile and check PLStatus.
You can see NVMe is enabled.

Defect ID: DCSG00039310
Headline: CPLD Version is not shown with CLI show all command
Description Of Change: CTRL_INFO(cpld.userCodeDefinition) is not populated with CPLD data, so was not printing it.
Issue Description: When running the CLI show all command the CPLD Version is not shown, the field is blank.
Steps To Reproduce: 1. Run CLI show all command
2) Check CPLD Version in the output

Defect ID: DCSG00031186
Headline: [Aero] Change the Manpage 7 Phy to Connector settings and Disable NVMe support in ManPage9
Description Of Change: NVDATA changes to
1) Disable NVMe support in channel 16e card.
2) Connector to Phy mappings in ManPage 7.
Issue Description: ManPage 7 is not as per Board Schematics.
NVMe is enabled for channel 16e card.
Steps To Reproduce: NA

Defect ID: DCSG00042497
Headline: BSOD when running CoreDump with Aero connected to Atlas switch
Description Of Change: Updated FW code to not use invalid-index to access the array during the "pl dbg" capture.
Issue Description: During the CoreDump collection, FW tries to access the array with invalid index and we see recursive faults
Steps To Reproduce: Force Coredump with Atlas connected to Aero controller.

Defect ID: DCSG00045528
Headline: Quotes present in NVDATA XMLs
Description Of Change: Remove the quotes.
Issue Description: The Ventura XMLs have "Broadcom" in the headers. The XML parser used for ROP builds can't handle the quotes.
Steps To Reproduce: Build a Ventura ROP.

Defect ID: DCSG00045593
Headline: PL: Initial MPI driver error injection can cause the Managed Switch's SES to not be exposed to OS
Description Of Change: Deleted the code that cleared the MPI Initialization in progress flag when an error is hit during MPI Initialization.

This prevents the PCI Discovery events from going up until the Managed Switch SES is initially found.
Issue Description: An initial error injection into PL's MPI driver can cause the Managed Switch's SES to not be exposed to OS. The add event is disrupted and never reissued.
Steps To Reproduce: Cause an error during MPI initialization of a Managed Switch's MPI Device that causes MPI Initialization to fail and then be retried later.

This was synthesized via the MPI Driver Error Injection feature in PL (compile time feature that is not available by default)

Defect ID: DCSG00045385
Headline: Ventura B0: Device discovery fails on 9400-16e
Description Of Change: Modified the FW to change the cable mgmt. SM to appropriate state on an SEEPROM I2C read failure.
Issue Description: Device discovery may fail on 9400-16e. When passive cable is used, the I2C read of SEEPROM fails and an earlier fix that prevents the retry of the I2C request from PL timer context leading to discovery failure.
Steps To Reproduce: On 9400-16e HBA running 13.250.11.00 FW and connect Expander Enclosure with passive cable. Observe no Expander attached devices are discovered.

Defect ID: DCSG00039865
Headline: Controller crashes in certain cases when sending multiple NVME pass through commands
Description Of Change: when releasing the PRP list, release the correct memory address.
Issue Description: when application sends NVME pass through commands with data length more than 4K, FW allocates PRP list frame and when releasing it ended up releasing incorrect memory pointer which causes corruption and leading to crash. This issue will only be seen with NVME pass through with length more than 4k.
Steps To Reproduce: send NVME pass through command with data length more than 4K and issue multiple times.

Defect ID: DCSG00033753
Headline: PL: Blind retries by MegaRAID FW when PL is in out of resource condition results in IOs to MS-SES exhausting retries
Description Of Change: Altered PL to pend the IO when an LMID is needed but not available.
Also changed PL to allow the Managed Switch SES layer to manage its Sense Buffer (an LMID) so the lower MPI Driver layer will not try to free it. This reduces the surface area for IOs translated by the MS-SES layer to hit low resource conditions.
Issue Description: Blind retries by MegaRAID FW when PL returns an insufficient resource error for IOs to a Managed Switch SES result in MegaRAID FW exhausting its retries. This is because higher layer firmware is retrying immediately and not giving time for any other task to run.
Steps To Reproduce: Have all of the LMIDs that PL uses be exhausted.
Cause a layer above, like MegaRAID FW/IOP or the host send a request to a MS-SES.

Defect ID: DCSG00044296
Headline: U.2 Drives Not Discovered on OEM backplane
Description Of Change: As this system supports both SAS/SATA and NVMe drives, following are the changes made:

1. Revert to earlier NVDATA configured for Tri-mode BP mgmt. with additional (Param3) settings to enable RefClk without BP_TYPE check.
2. MR FW read the AltDSel flag settings of the sideband signals used for cable decoding from NVDATA, save of the AltDSel settings.
3. Change the AltDSel settings for these GPIOs to 00 (GPIO) and read the GPIOs state.
4. Revert the AltDSel of the cable detect GPIOs to NVDATA/Saved settings.
5. When PL initializes, based on override settings the RefClk is enabled always. This will allow FW to work for SAS/SATA and NVMe configs.
6. Change the GPIO as input and read it during OOB along with the NVDATA flags change

Issue Description: The changes made to NVDATA v18 are not intended for tri-mode backplane and focused only for SAS/SATA. Because of the new nvdata changes, the NVMe drives were not getting detected.
Steps To Reproduce: OEM used Package version 50.9.1-2830 with NVMe drives in the configuration and the drives were not discovered on boot up.

Defect ID: DCSG00036763
Headline: PL: TM Device Reset to NVMe drive under out of LMID condition can cause Data Abort Exception to the processor
Description Of Change: Corrected a stack variable to always be seeded with the invalid value.

Corrected both FX Core flushing and NVMe Flush code to only mark a specifically tracked critical MID when the critical frame is successfully allocated.

Added fault codes for critical frame allocation failures for FX Core, NVMe Flush, and TM Task Abort to SAS drive.

Added a new custom CLI command to fake a specifically tracked critical LMID is already in use, clear its in use flag, and report the value of the tracking variables.
Issue Description: A TM Device Reset to NVMe drive when PL is under an out of LMID condition can cause Data Abort Exception to the processor. This also requires a critical LMID used by FX Core flushes, NVMe Flushes, and Task Abort UIs to SAS Drives to be already in use by one of those tasks. A NULL pointer is unintentionally accessed because a check that is expected to fail due to a known invalid value does not.
Steps To Reproduce: Attach 16+ NVMe drives to a switch. Attach the switch to an Aero controller.
Run very large IO that requires breakup by PL, i.e. larger than the MDTS of the NVMe drives.
Run PL and IOP code that do not throttle IO breakup's resource allocation.

Defect ID: DCSG00043821
Headline: Aero: backend PCIe: link failure following link down
Description Of Change: Modified Aero protocol cycler dwell timer settings to prevent an issue where one or more lanes in a PCIe link becomes unsynchronized from the others.
Issue Description: If a device side PCIe link goes down, it may not come up again when it is restored.
Steps To Reproduce: Perform direct attached link break, device pull, and device/switch power cycle testing with Aero.

Defect ID: DCSG00048027
Headline: UBM: Incorrect slot number enumerated for a DFC on 3 x4 DFCs UBM config
Description Of Change: Updated FW to properly enumerate the slot numbers for connectors in UBM HFC group.
Issue Description: During UBM Auto HFC grouping, the FW skips the connector group config update and slot enumeration as both the connectors in the group were of same BP type (UBM) but at different states.
Steps To Reproduce: Using a customer specific UBM backplane with 3 x4 DFCs attached to 9400-16i HBA on C0/C1/C3. Observe incorrect slot number enumerated for C3 attached device.

Defect ID: DCSG00039322
Headline: Firmware version is blank and Macronix controller not being displayed in Raid manangement utilities
Description Of Change: Don't Include and ignore Secondary/CBB or SBR Components in while building components from Flash memory
Issue Description: Firmware version is blank and Macronix controller not being displayed in Raid manangement utilities
Steps To Reproduce: Use storcli show all or HII to see Firmware version string

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Defect ID: DCSG00047664
Headline: Hard/SoftSecure Firmware unexpectedly flashes successfully on controllers.

Description Of Change: MR FW Blocks Image flashing based on Device ID.Device ID field is different for Aero soft secure (0X10E1) and Hard secure(0x10E2)
Firmware should block Firmware flashing based on device ID for Aero

Issue Description: OEM is able to flash soft secure Images on Hard secure aero boards.

Steps To Reproduce: Flash soft secure Image on Hard secure board or vice versa.

Defect ID: DCSG00047928

Headline: "iop show cfg all" command captured by core-dump is zero

Description Of Change: 1. Reduced the memory footprint of zlib. This will help other CLI commands to allocate the memory if needed
2. During "iop show cfg all", if the memory allocation fails use the CFGI-Scratch buffer memory area, if available.

Issue Description: During the "iop show cfg all" execution, the memory needed for storing the config-page temporarily is failing to be allocated.

Steps To Reproduce: 1.Using Fault command from Scrutiny CLI, trigger soft fault on the running firmware.
2. Execute below command to upload contents of flash to a file.
coredump -ul -f <filename>
3. Coredump data is generated in a zip file.
4. Unzip the file and notice that "iop show cfg all" capture is not showing any config page data

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Defect ID: DCSG00050675

Headline: Fix ring buffer decoder's slowness with decoding a trace buffer

Description Of Change: Cached the size of the trace buffer file and used the cached version instead. This file should never change in size during processing.

A mostly empty 5MB trace buffer went from 1067 seconds to the end of the decoding down to 43s.
A fully 5MB trace buffer went from 1067 seconds down to 35s.

Issue Description: Fix ring buffer decoder's slowness. Decoding a trace buffer suddenly slowed down despite no code changes to the tool.

Either newer Windows versions or new anti-virus versions are penalizing repetitive requests to get the size of a file.

This call added 1ms of time.

Steps To Reproduce: Decode a trace buffer using the ring buffer decoder.

Defect ID: DCSG00050201

Headline: [Aero][PLDM] FW version reported wrongly to BMC(Board Management Controller) over out of band

Description Of Change: Remove the extra colon from the firmware version.

Issue Description: Firmware Version is not properly formatted, extra colon appears in firmware version.

Steps To Reproduce: 1) Flash the latest firmware on controller.
2) Observe the firmware version in board management controller portal.
3) An extra colon(:) appears in the beginning of firmware version.

Defect ID: DCSG00050182

Headline: pl: NVMe: Select field used during NVMe init without verifying support

Description Of Change: Verify that the Select field is supported before using it during NVMe initialization.

Issue Description: During NVMe initialization, PL may set the Get Features (Select) field to a value other than Current without first checking if the device supports the Select field.

Steps To Reproduce: Code inspection.

Defect ID: DCSG00050164

Headline: Aero: backend PCIe: link failure after PCIe IO Unit Page 1 link disable

Description Of Change: Modified sequencing of hardware cleanup steps in the link disabled case on Aero.

Issue Description: If a Write Current of PCIe IO Unit Page 1 is used to set the PHY Disabled flags associated with an existing PCIe link following port enable, the link won't come up when the flags are later cleared. An adapter reset is needed to restore the link.

Steps To Reproduce: Use the PHY Disabled flags in PCIe IO Unit Page 1 to disable an existing PCIe link on Aero.

Defect ID: DCSG00044028

Headline: pl: NVMe: Drive Firmware update fails on mode 0xE

Description Of Change: Added a debug print instead of failing the write buffer command.

Issue Description: Currently PL firmware will not send the firmware image download command to the drive if data length of write buffer command is less or it is not multiple of reported drive FWUG value.
Hence the drive firmware update fails from storcli.

Steps To Reproduce: Insert the NVME drive on UBM backplane.
Using storcli execute mode E drive firmware update command .
Observe the results from storcli console.

Defect ID: DCSG00042446

Headline: Drive Discovery failed with Port Hot-swap on Aero16e controller

Description Of Change: Fixed NVData to reflect correct Phy-ReceptacleID mapping in Manpage7.

Issue Description: The Phy-ReceptacleID mapping in Manpage7 was incorrect.

Steps To Reproduce: 1. On 16e HBA Port-0, connected enclosure drives. Drives discovered successfully.
2. Hot swapped cable to Port-3 on the HBA, Drives failed to discover in the FW and as well in the OS.

Defect ID: DCSG00048993

Headline: Automatic Copyback operation fails from Hotspare

Description Of Change: The issue was caused due to PD post processing occurring on the inserted drive twice. The first call causes copyback to start and the second aborts the copyback operation. There should only be one PD post process operation run in this scenario. The fix is to not call PD post processing when drive has been unlocked when drives are attempted to be unlocked.

Issue Description: When drive is inserted into original slot, copyback starts but is aborted soon after.

Steps To Reproduce: 1. With EKMS/SEKM security configured and enabled, create a secure 3PD R5 VD (with SED Drives)
2. Create a DHS drive using an SED drive and assign it to the R5's DG.
3. Pull a member PD from the R5 and verify rebuild starts and completes on DHS.
4. wait for 3 min
5. Re-insert pulled member PD. Automatic copyback should start and complete.

Defect ID: DCSG00049508

Headline: Unable to create a new security key (LKM) after deleting the security key

Description Of Change: For certain OEM with EKMS, key is not always stored in SRAM. When key is required, it is requested from an EKM server. In this case, lock key cannot be considered failed if key is removed from controller.

Issue Description: After deleting the security key and attempting to create a new security key, an error stating a key already exists is returned.

Steps To Reproduce: 1. delete the security key
2. attempt to create a new security key

Defect ID: DCSG00052268

Headline: pl: backend PCIe: 'pl pci devlnk' is missing from the 'pl dbg' dump

Description Of Change: Added 'pl pci devlnk' data to the 'pl dbg' dump.

Issue Description: The "pl pci devlnk" diag console command is used to obtain the negotiated link width and speed of every device and bridge in the topology, which is useful for debugging link and performance issues. It appears that this information isn't printed by "pl dbg" which is the usual means of obtaining detailed PL debug information.

Steps To Reproduce: Examine the "pl dbg" data.

Defect ID: DCSG00048607

Headline: PH14 Windows Driver: on 2016,19H2 OS,Getting BSOD for fault command

Description Of Change: 1. Updated CMM handling to enable controller reset before calling the completion function.
2. In case of CoreDump timeout call CMM command completion function so that adapter reset can be enabled

Issue Description: 1. The issue happens when the CoreDump times out during "pl dbg" execution.
During "pl dbg" execution, the adapter reset is disabled

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2. Once the coredump times out, the command execution is aborted and zip is saved in the flash and FW is faulted
3. Driver than issues diag reset to bring the adapter in the operational state, but since the reset is disabled, the adapter never reset itself

Steps To Reproduce: 1. Connect a topology which can cause the "pl dbg" to take a long time to dump (> 15 seconds)
2. Trigger the coredump by faulting the controller

Defect ID: DCSG00051990

Headline: Number of initiators gets decremented to 0xFF

Description Of Change: Add/Remove initiator entry to initiator table if SSPInitiator is set in the open address frame.

Issue Description: SSPInitiator set in the open address frame is checked only for incrementing the number of initiators but not for adding the entry to table.
In one of the scenarios, entry is added to initator table even though SSPInitiator is not set. But the number of initiators is not incremented.
When this entry is removed, the number of intiators is decremented to negative value as it was not incremented while adding.

Steps To Reproduce: Two HBAs first port has nothing connected to them.
The second ports are directly cabled to each other.

All ports are configured in initiator mode via SAS IO Unit page 1 as SSPTarg, SMPInit, STPInit, and SSPInit.
To go to target mode on a port, do a diag reset, and configure the port as SSPTarg, SMPInit, and STPInit (removing SSPInit).
To go back to initiator mode do a diag reset, and then set up SAS IO Unit page 1 accordingly

Transit from initiator to target, to initiator, and then back to target mode on the local port.
After the last transition to target mode, the remote port which is in initiator mode, reports the overflow of 255.

Defect ID: DCSG00053379

Headline: Back out changes of ER DCSG00029633 that limits VSES devices to 2

Description Of Change: The changes done in ER DCSG00029633 is reversed to revert the number of VSES devices support to the original implementation.

Issue Description: ER DCSG00029633 limited the VSES device instances support in PL to max 2 but OEM's new UBM backplane server configurations require support for more than 2 VSES devices.

Steps To Reproduce: None

Defect ID: DCSG00051937

Headline: MR firmware does not parse PL CLI commands that are tagged as RESTRICTED correctly

Description Of Change: Updated the code to handle RESTRICTED commands properly

Issue Description: The PL has a small set of its PL CLI commands that are tagged as restricted. The MR firmware when parsing the PL CLI structures does not correctly handle the RESTRICTED tag correctly. As a consequence, the restricted PL CLI are not able to be executed when attempting a "dmdaig pl ..." CLI comand on the megamon prompt.

Steps To Reproduce: Attempt to execute the following megamon command:

MegaMon0> dmdiag pl pci reset 0x0017

Notice that the help for the command is printed out rather than the command being executed.

Defect ID: DCSG00052343

Headline: Cache Data Not recovered event not seen after 63 loops of cache offload with double dip.

Description Of Change: Some OEMs have Battery instead of Supercap. Firmware checking for Supercap and Supercap state of Health and returning without ONFI region for next next Offload.

For this OEM, Firmware should not check Supercap status.

Issue Description: Some OEMs have Battery instead of Supercap. Firmware checking for Supercap and Supercap state of Health and returning without ONFI region for next next Offload.

Steps To Reproduce: Run SAL Script for case test run DCSG00038904

Defect ID: DCSG00054655

Headline: MCTP: SenseData not available for a failed command sent over OOB.

Description Of Change: While transferring data in error case, set transfer length to the minimum of data length in the request and transfer length field updated by PL.
This ensures the data transferred does not exceed the response length.

Issue Description: The response length in MCTP request for a SCSI command includes data length and sense data length.
The sense data is placed after the command data. The data length field in the request indicates how much data
is expected.In case of error, the data transferred field updated by PL is used as data length to transfer the data.
If the transfer length field updated by PL exceeds response length, it causes overrun.
Due to this there is no space to transfer the sense data,
as the whole response length is consumed by data. As a result, sense data is not transfered.

Steps To Reproduce: Drive firmware upgrade with controller firmware upgrade in BMC with OEM drive connected

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Defect ID: DCSG00057124

Headline: scattered file changes to include some debug prints and also minor change to debug print

Description Of Change: scattered file changes to include some debug prints and minor change to debug print

Issue Description: some of the section related to debug prints were not specified in scattered file.

Steps To Reproduce: Enable macro PL_FEATURE_EM_SFF_TA1005_UBM_DEBUG_PRINT and try to build.

Defect ID: DCSG00056083

Headline: FW is stuck in an infinite reboot loop after uncorrectable ECC errors detected

Description Of Change: Initialize local variables before using them

Issue Description: MR FW is not Clearing resetAdapter and resetRequired bit fields before writing value in to MFI Door bell register when FW halts with Fault code. MR FW requested system to reboot because of garbage value in this case and then Firmware entered infinite loop.

Steps To Reproduce: s
Start IOs
Break into the debugger and use the function to create multiple uncorrectable ECC errors...
"call validate_ecc_handling 48"
Break out and the FW will halt
Reboot the server
- Upon rebooting the FW reports the below output and the server post reports that the FW is in Fault State and that a system reset is required. System will reboot now...

Note: The FW repeats this in an infinite loop until a full power cycle is performed, but the post does not indicate ECC errors, or that a Power Cycle is required.

*** ECC Error(un-correctable), addr=0x0000000020000000 ***
*** data=0x0000000000000000 syndrome=0x00000004 badBit=0x000000ff sourceId=0x00000144
MSS error interrupt status = 0x00000020

haltwithfaultcode faultcode 81
!!! Firmware halted. Fault code = 0x81 !!!

!!! Power Cycle Required !!!

Defect ID: DCSG00048699

Headline: PL: Over 250+ power cycles of managed switch (Atlas) causes an associated SES to be inaccessible

Description Of Change: Corrected the code to detect the wrap needed when preallocating a single Device Handle.

Issue Description: A Device Handle preallocation done for managed switch SESes has incorrect wrap handling of Device Handles when on a boundary condition and only preallocating a single Device Handle.

Steps To Reproduce: Power cycle or connect-disconnect a managed switch for 250+ cycles.
Reproduction time is cut proportionally for each managed switch attached that is also cycled.

Defect ID: DCSG00058770

Headline: Firmware asserts during customer specific UBM Backplane enumeration.

Description Of Change: Changed the logic for configuring the link for the quad where the enumeration is failed.

Issue Description: When one of the quad in a x8 is connected to UBM that enumerated successfully and other quad to UBM its enumeration is failed, quad that enumeration failed is not selected for configuring the link and stays in same state of enclosure state machine. As a result PL is not completing the discovery on both quads and firmware is not receiving discovery complete event from PL and Firmware asserts.

Steps To Reproduce: 1.Connect a customer specific UBM backplane which fails during UBM FRU or UBM controller enumeration to one of the quad in a x8 slim SAS connector.
2.Connect a working UBM backplane to other quad of x8 slim SAS connector.
3.Boot the controller and observe the assert in RAID IOP stack.

Defect ID: DCSG00059594
Headline: Ventura; Add code to prevent downgrade from phase 14 to previous phases for winbond
Description Of Change: Added code that will prevent downgrade of firmware to previous revisions when one of there is a SPI part that requires a later revision of SPI Library
Issue Description: An OEM changed their SPI FLASH Part such that it was incompatible with older versions of SPI Library
Steps To Reproduce: Replace a working version of the given SPI Flash with the newer one

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Defect ID: DCSG00061349
Headline: Incorrect Man page 7 Phy-Slot mapping set for 9500-xx channel HBAs
Description Of Change: Fixed Man Page 7 Phys to slot numbering for 9500-xx boards NVDATA.
Issue Description: Slot numbering of devices reversed on 9500-16i DVT board attached to SGPIO backplane using SlimLine-x8to-Dual Mini-SAS-HDx4 cable
Steps To Reproduce: Attach SGPIO backplane with no group ID support to 9500-16i IT HBA and observe the slot numbers being reversed for the Phys

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Defect ID: DCSG00054949
Headline: PL: 2 Atlases in single MPT mode with 2 host ports each will have drives on one switch not mapped to that Atlas's SES Page 0Ah
Description Of Change: Start with an Atlas FW that supported the per-Atlas WWID feature, as well as some other commands like querying for the ELI and Port Mask configuration.

Added code to set the enclosure type to PCIe SES when an Atlas is found right away instead of deferring.
Added code to better track per enclosure whether it needs to stretch across ports or switches as well as a related counter.
Added code to decrement the enclosure's port counter when switches are removed.
Adjusted the Slot Number of a switch enclosure at the end of MPI Initialization when a managed switch SES is found, but only do this the first time it is found.
Changed the switch-to-enclosure information translation code to consider whether the enclosure crosses ports/switches and adjust the Start Slot and Number of Slots for MPI Enclosure Page 0 accordingly.

Issue Description: Attach 2 Atlases in single MPT mode with 2 host ports each will have drives on one switch not mapped to that Atlas's SES Page 0Ah.
Steps To Reproduce: Attach 2 Atlases in single MPT mode with 2 host ports each behind an Aero controller. Attach drives to the Atlas.

Defect ID: DCSG00059302
Headline: Toolbox clean command sent to clean flash fails.
Description Of Change: Added code to erase the new coredump flash region and removed the code to erase old region type.
Issue Description: A new flash region was added in phase 14 to store the coredump. This region was using a previously unused region. However the toolbox clean command handler was not updated to erase the newly added region and it was still trying to erase the old region type which did not exist so the toolbox clean command was getting failed.
Steps To Reproduce: Issue erase all command using storcli, observe that the toolbox clean command fails.

Defect ID: DCSG00061635
Headline: pl: backend PCIe: switch rediscovery fails with certain switch configurations
Description Of Change: Fixed the described issues. Note that the first issue was introduced in phase 14 and is not present in a GCA build.
Issue Description: If a backend PCIe switch lacks a downstream port with device number 0, the upstream port's bus configuration isn't reprogrammed during switch rediscovery. This causes rediscovery of the switch to repeatedly fail.

If a switch is placed into Delay Not Responding state when a Device Missing Delay timer expiration has occurred for an attached device, the Device Missing Delay timer expiration isnt handled when downstream device processing occurs.

Steps To Reproduce: Perform switch upstream link break testing with a switch that does not have a downstream port at device number 0.

Defect ID: DCSG00026003
Headline: BP and EPD LEDs are not exposed to the host if Slot 0 is configured as an EPD
Description Of Change: Instead of using devHandle filled in PL frame to extract device id , the original device id (filled by driver) is used to retry the command. Thus now the correct device id for enclosure/ backplane is used.
Issue Description: In pl frame the device handle is filled as 0xFFFF. When this is used to extract device id for backplane the offset is overshooting the maximum number of elements present in the array. The array having device id to device handle table is defined for only Maximum Device Handles. When accessing 0xFFFF element this is some undefined memory access giving some junk data. In this case it returns value 0.
Now device id =0 is used for subsequent processing of command i.e. deciding whether to retry the command or now. In the system there is ePD with deviceid=0. FW does not allow commands for ePD to be retried. Hence the command is not retired since deviceid has incorrect value of 0x0 pointing to ePD.
Steps To Reproduce: Have ePD with device id =0.
Enable JBOD host led management
Issue the powershell command to show BP details (Get-StorageEnclosure | fl) - No Info Shown
Use Server manager to attempt Toggle drive light on both EPDs - FAILS
Now delete the EPD with devid 0
Repeat powershell command - BP Info shown correctly
Repeat test to toggle drive light with server manager - WORKS

Defect ID: DCSG00063530
Headline: PL: PCIe switch discovery can cause processor exception when setting enclosure information
Description Of Change: Corrected the use of a variable that may not be initialized with an in range value.
Issue Description: Variable used in array access can be uninitialized and cause an address access that is not mapped. Problem does not show up in IT firmware, likely due to compilation differences or memory mapping layout differences.
Steps To Reproduce: Attach Atlas to an Aero RAID controller and perform Port Enable.

Defect ID: DCSG00055795
Headline: No Access Allowed' not set on VDs and UG drives when Host LED Mgmt on Non-RAID Disks is enabled.
Description Of Change: Allowing Enclosure Status diagnostic page 0x02 to be modified for OEM controller. This modification is to set RAID slots status as No Access Allowed . This was blocked earlier for this OEM.
Issue Description: The issue occurs because for specific OEM controller , modifying RAID slots status is not modified. The status page allows operation to the RAID slots.
Steps To Reproduce: 1. Enable Host LED Mgmt on Non-RAID Disks from HII
2. Boot to OS
3. Create VD on a PD
4. Check SES page A to get the element index for the slot PD is in
5. Check the status of the element in step 4 in SES page 2. It is set to OK instead of 'No Access allowed'
6. Attempt to blink the PD using 'sg_ses /dev/sg<ses_id> -p 0x2 --index=<index_id> --set=ident'. Command succeeds.

Defect ID: DCSG00058973
Headline: Undefined Instruction exception handler was called
Description Of Change: The code for the final buffer transition was rearranged. Instead of doing some of the transition at the top, and the rest at the bottom of the module, all transition is done at the top so there is no window for a print to occur.
Issue Description: Prints are buffered in a few places. When the code is transitioning between these places, care must not be taken to print while the data structures are not consistent.
Steps To Reproduce: Reset the controller with the tty-log-in-flash setting. Turning on debug to increase the volume of prints increases the likelihood of failure.

Defect ID: DCSG00058474
Headline: Assertion failure in fw\dm\pl3.5\pliopi.c - During drive push pull and reboot
Description Of Change: A check needs to be added, where before issuing smart poll, FW will check if removal pending flag is set then skip that drive
Issue Description: There seems to be a race condition in MR FW between when a drive is removed and when smart poll is issued to it. once the drive removal process starts among other things FW sets a removal pending flag, invalidates the devhandle, notify RAID module about its removal and then mark the drive as unconfigured bad. Between this a narrow window exits where if SMART poll is issued then there is all likelihood that MR FW will issue a command to PL with invalid dev handle.
Steps To Reproduce: Verify multiple drive type push/pull and reboot actions don't cause the FW or PL to fault.
With Dtabs attached and Sas HDD and SSD, SATA HDD and SSD start script to push/pull drives with reboot
After several loops : Assertion failure in fw\dm\pl3.5\pliopi.c

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Defect ID: DCSG00062820
Headline: PERC 10.5 - The personality behavior=None is allowed to be set and should be blocked in eHBA mode.
Description Of Change: When FW receive with autoconfig option as user configur, FW will reject as command is not allowed
Issue Description: In eHBA mode, the user can set the personality behavior=None . This should not be allowed and be blocked to be consistent with previous programs behavior. When the behavior is set to None, this prevents the user from being able to create EPDs.

Steps To Reproduce: 1. Switch to eHBA mode.
2. change the personality behavior to None. cli64 /c0 set personality behavior=None

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Defect ID: DCSG00061406
Headline: Aero A0: In Windows OS redundant disks detected when controller connected to Elrond Ex1
Description Of Change: When sending SAS Topology Change List event during event replay, the direct attached enclosure attached Phys may have holes (eg., 0xF0FF). So start from the beginning to find the last PhyIdx else duplicate device add event may be sent for same device with different Encl Handle. If the Port Phys are managed by two enclosures then separate SAS Topology Change List events are sent for each of the Encl and attached Phys/devices.
Issue Description: UBM Ex1 enclosure attached devices being see twice.
Steps To Reproduce: Attach OEM specific controller to Elrond Ex1 enclosure. Boot Windows and notice that Windows Disk Managment and Device manager show each device twice.

Defect ID: DCSG00055371
Headline: Aero: Firmware Download should return success with loginfo indicating POR is necessary
Description Of Change: When completing a firmware download request, added code to set a loginfo value of IOP_LOGINFO_CODE_IMAGE_REQUIRES_POR (0x412) in the reply message, to indicate that a power on reset (POR) is required.
Issue Description: Currently, in the case that the firmware image has different keys and a key update is required, there is no indication to the host that a key update is pending and a power on reset (POR) is required.
Steps To Reproduce: Sign an Aero firmware image with different keys than normal and do a firmware download operation. No indication is given at the host level that a key update is pending.

Defect ID: DCSG00062527
Headline: PowerCycle Server after re-purposing controller by ClearNVRAM causes controller not found
Description Of Change: changed the "delete nvram" routine to not generate a snapdump
Issue Description: "delete nvram" command was generating a snapdump where it is not necessary and during reboot the FW re-initializes the ONFI flash because of the "delete nvram" causing a cache data loss message
Steps To Reproduce: Run "storcli /c0 delete nvram" with supercap attached and reboot server

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Defect ID: DCSG00058891
Headline: MR:Config Loss seen for rebooting server after Deleting Logical disk with OS on JBOD installed.
Description Of Change: In LD deletion path, FW tries to read the DDF data from EPD PD leads to an issue.
Added the condition check to skip reading DDF data from EPD Lds.
Issue Description: Issue happening only if we create one JBOD first and then 2 partial Vds. When we tried to delete the one partial Vd its deleting both Vds.
We are not seeing the issue if partial Vds created first then JBOD. If first LD number is EPD drive then only the issue occurs.
Steps To Reproduce: Test case:
- Create the JBOD
- Create the 2 partial R0 VDs using single drive.
- Delete any one partial VD
- Reboot the server, across reboot observed both config last.

Defect ID: DCSG00063924
Headline: pl: NVMe: incorrect sense key is returned for Access Denied NVMe status
Description Of Change: Return DATA PROTECT sense key in this case.
Issue Description: If an NVMe device fails a command with an Access Denied (0x86) status code, the SCSI sense key returned by PL for the IO is ILLEGAL REQUEST (0x5). It should be DATA PROTECT (0x7).
Steps To Reproduce: Send read/write IOs to a security locked NVMe device.

Defect ID: DCSG00062701
Headline: 0xD101 Fault observed running non-RW IOs to NVMe devices with drive push-pull
Description Of Change: Updated FW to clear the IO context area used during the start of the PCIe IOs.
Issue Description: FW may fault with 0xD101 running non-RW IOs to NVMe devices with drive hot removal and insertion. An IO flag used for FW RW IOs is left out on completion and when the same MID used for non-RW IO leads to double completion due to flag set causing the FW fault 0xD101.
Steps To Reproduce: On 9500-16i HBA attached to UBM backplane with NVMe devices
Run IOs to the drives and perform rapid removal/reinsertion and observe FW fault 0xD101

Defect ID: DCSG00065411
Headline: The personality behavior=JBOD is allowed to be set and should be blocked in eHBA mode.
Description Of Change: When FW receive with autoconfig option as user configure (EPD Passthrough) FW will reject as command is not allowed
Issue Description: In eHBA mode, the user can set the personality behavior=JBOD. This should not be allowed and be blocked to be consistent with previous programs behavior.
Steps To Reproduce: 1. Switch to eHBA mode.
2. change the personality behavior to None. cli64 /c0 set personality behavior=JBOD

Defect ID: DCSG00068694
Headline: Incomplete foreign configuration when importing LKM into EKMS environment
Description Of Change: In order to rekey a drive MR FW requires both the old key and the new key. In this case, due to removal of key caching from SRAM, the new key has been cleared and is not present on the controller. This causes the rekey to fail and as a result, the config is not able to be imported.

The fix is to request the EKM server for the controller key during import sequence while using escrow key.
Issue Description: Unable to import an LKM secured volume into an EKMS secured environment. Import fails with "Incomplete foreign configuration"
Steps To Reproduce: 1. Create EKMS secured R5 VD on local EKMS system
2. Create LKM secured R1 VD on secondary (LKM) system
3. Remove both secured Vds are reboot local system back into Windows OS
4. Insert both VDs (EKMS secured and LKM secured) into local (EKMS) system.
5. Import EKMS VS (It should already be unlocked, but foreign)
6. Unlock secured LKM VD (in this case I incorrectly specified the key the first time and unlock failed dut to bad key)
7. Verify LKM VD is now unlocked (Used good passphrase key) and import it. Import fails

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Defect ID: DCSG00069395
Headline: PERC 10.5 FW version missing in /c0 show and Hii
Description Of Change: Listing HIIA component is skipped as it is not needed
Issue Description: Firmware version is Blank in HII and the field is missing in OS with CLI show command
Steps To Reproduce: Boot to HII
Enter Controller Management
Firmware Version is blank

Defect ID: DCSG00071775
Headline: Cryptographic Erase cannot be executed on drives that do support Format NVM but not Sanitize
Description Of Change: As per NVMe spec, Bit 2 of FNA should be checked to determine if the drive supports crypto erase. MR FW was using Bit 1 to make this determination.
The fix is to check Bit 2, which if set it means that the drive supports crypto erase.
Issue Description: Cryptographic Erase cannot be executed on drives that do support Format NVM but not Sanitize
FNA should be set to 4 in order for cryptographic erase to be supported.
Steps To Reproduce: 1. Boot SUT with NVMe drives
2. Go to HII
3. Observe that under PD operations, PD erase is displayed but not cryptographic erase
4. Boot to OS
5. Attempt crypto erase using CLI. Observe that the operation fails.

Defect ID: DCSG00054906
Headline: Aero: pl: SATA device may not link up following a link down
Description Of Change: Pulled in an updated CSW firmware image containing a fix for an issue that caused the SERDES to become stuck at an improper speed. This issue caused SATA OOB signaling to repeatedly fail following a link down.

Issue Description: If the link between an Aero/Sea HBA and a direct attached SATA device goes down, it may not come up again until the HBA is reset.

Steps To Reproduce: Perform link reset or link break testing with direct attached SATA devices.

Defect ID: DCSG00072635

Headline: [9361-8i MR6.14] storcli return with error when set patrolread mode

Description Of Change: MR FW has been changed to set max possible value for PR property "max concurrent PD" in Get PR property path, if it has invalid value.

Issue Description: Max possible value to be configured for PR property "max concurrent PD" has been changed in 6.14 FW (it was max PD in old FW and it is max configured PD in new FW).
So PR property "max concurrent PD" initialized as "max PD" when user does factory reset with old FW and it's value remain same after upgrading the new FW, value is invalid now with respect to this new FW. Later if user tries to set any of the PR property, then FW fails it because "max concurrent PD" has invalid value.

Steps To Reproduce:
1. storcli /c0 download file= MR6.12GCAFW.rom noverchk
2. reboot, and issue,
   a) storcli /c0 set patrolread=on mode=manual <<<< this is working fine
   b) storcli /c0 set patrolread=on mode=auto <<<< this is working fine
   c) storcli /c0 show patrolread <<<< to make sure the mode is auto now
3. power cycle the system with controller.
4. storcli /c0 download file= MR6.14FW.rom
5. reboot, and issue storcli /c0 set patrolread=on mode=manual <<<< this is NOT working now

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Defect ID: DCSG00067176

Headline: SAS9341-8i board encounters 'Previous configuration completely missing at boot' error

Description Of Change: MR FW has changed as below :-
1. Restore config sequence number before writing the first header itself (May be primary or secondary based upon the whichever header having the error)
2. Update config sequence number in NVRAM only after first header is written and before writing second header.

Issue Description: Power cycling the system while MR FW initialization where FW is writing the secondary header is in progress, causing secondary header error, so in next boot FW writes the secondary errors first. Before writing secondary header it didn't restore the sequence number and written anchor written sequence number -1 to secondary header and NVRAM both and while writing primary header it restored the sequence number and updated the correct seq to primary header. This causing sequence number mismatch in NVRAM and primary header when FW tries to read the configs, hence MR FW found this as missing config.

Steps To Reproduce: The test steps are:
-First boot into the OS and create the RAID0 VDs with storcli tool.
-Then start the unexpected power loss stress test. Customer just suddenly unplug the AC power during the test.
-There is no IO running to the VDs during the test.

Defect ID: DCSG00069689

Headline: FW exception when get snapdump is initiated

Description Of Change: If the OOB communication method is I2C, then not dumping the PLDM module related data structure as part of snapdump data collection.

Issue Description: When OOB communication method is I2C, Fw tries to dump the PLDM module related data structure. In I2C mode PLDM FW services are not registered and leads to FW exception.

Steps To Reproduce: In I2C mode execute the storcli.exe /cx get snapdump command

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Defect ID: DCSG00069029

Headline: Not able to enable JBOD property in Ventura controllers

Description Of Change: Unused legacy feature bits being removed

Issue Description: When the FW halt with fault code in some scenarios, one of the unused legacy feature bit is being set which causes the JBOD property set to be blocking

Steps To Reproduce: 1. Connect 16i ventura controller to OEM server.
2. Boot to HII, try to enable JBOD property on RAID 930-8i and RAID 930-16i controllers from storcli.
3. Observe that command fails with error Invalid arguments.

Defect ID: DCSG00059007

Headline: For an OEM - Unable to pause Patrol read via perccli

Description Of Change: Updated code to check for prd->active flag instead of prd->msgActive for a valid pause operation.

Issue Description: Not able to pause patrol read.

Steps To Reproduce: C:\>app_name.exe /c0 start pr
Observe successful start.
C:\>app_name.exe /c0 pause pr
Observe Failure wit error code 50.
Note: This error happens intermittently, so try this several times.

Defect ID: DCSG00071784

Headline: Moving Controller From Single VSES config to a multi-VSES config causes issues in windows OS.

Description Of Change: The firmware workaround to the driver issue includes
1. For UBM backplanes always start enclosure handle numbering from 2, since enclosure handle 1 has some specific handling in windows driver.
2. On completing the discovery before reply to port enable, if the controller was initiated by BIOS. The firmware will go through the driver persistence mapping config page and compare it with current enclosure configuration. In case a mismatch is found the complete driver persistence mapping page will be deleted.

Issue Description: Based on the enclosure configuration windows driver creates a persistent mapping of enclosures and devices and writes that mapping into a config page on the controller. On subsequent boot up the driver reads this config page to create the persistent target id of the devices. If a controller is moved from one configuration with single direct attached enclosure to another with multiple direct attached enclosure and if there is a conflict between the persistent mapping config page and current configuration it may lead to some issues in OS while creating the device mapping.

Since inbox driver can not be changed, this issue needs a workaround in firmware.

Steps To Reproduce: Connect a controller in a system with single backplane and boot to Windows OS with inbox driver. Take the same controller and move it to a system with more than one backplanes of different types connected to controller and boot to Windows OS with inbox driver. Sometimes an OS crash is observed.

Defect ID: DCSG00078212

Headline: NVMe drives not discovered and Event replay in enclosure slot mapping not working as expected.

Description Of Change: During PCIe device discovery instead of checking if enclosure handle 1 is allocated or not, added a check to see if direct attach enclosure initialization is complete or not.

Changed event replay function to move to direct attach slot ordering state after adding first direct attached enclosure.

Issue Description: In a recent change the enclosure handle for UBM backplanes will start from 2 instead of 1. However the PCIe discovery had a check to see if enclosure handle 1 is allocated or not before starting the discovery. This was leading the PCIe discovery to never start.

Also during event replay it moves to direct attach slot ordering state only after adding enclosure handle 1 add event is sent to host. So in cases there is no enclosure handle 1 allocated, it will not move to slot ordering state and will sent event in default phy order.

Steps To Reproduce: Attach a NVMe device behind a UBM backplane to the controller. Observe that the NVMe device is not discovered and PCIe discovery never completes.

Set direct attach enclosure slot ordering for event replays in nvdata but still the devices are not added in slot order.

Defect ID: DCSG00075900

Headline: Attempting to enable Host LED Management option fails in HII.

Description Of Change: Allowing specific permissible parameters to be changed for the personality. Instead of earlier code where there was a blanket blocking of set operation.

Issue Description: In code any Auto-configure set operation was blocked for this controller in this personality. Hence when application was trying to set Host LED Management parameter (which is a property of autoconfigure parameters), this operation was getting blocked.

Steps To Reproduce: 1. Set factory defaults and boot into HII
2. Go to the Controller Management -> Advanced Controller Management Menu and look for the Host LED Management selection.
3. Changing this property fails.

Defect ID: DCSG00079271

Headline: The personality behavior=None is allowed to be set.

Description Of Change: Performing check for OEM and personality at correct place and returning status before any non-permissible parameters are set.

Issue Description: Check and return status is done incorrectly. Hence parameters which should not be changed in given behaviour mode are getting modified.

Steps To Reproduce: 1. Switch to eHBA mode.
2. change the personality behavior to None. Command status shown is operation not possible.
3. But in code status operation not possible is returned from incorrect place.

Defect ID: DCSG00078527

Headline: Autoconfigure R0 is allowed to be set when this should be disabled and only allow the immediate command.
Description Of Change: FW will block to set autoconfigure R0 in RAID mode and JBOD mode when Auto config with set DCMD is received.
Issue Description: The cli autoconfigure R0 command is going through successfully and setting the personality behavior to single drive R0. This should be blocked.
Steps To Reproduce: 1. Run cli64 /c0 set autoconfig=r0
2. run cli64 /c0 show personality to see the mode changed.

Defect ID: DCSG00040960
Headline: logGet: Found invalid event at e82858c4 pe 1411
Description Of Change: Harden the check by having additional SeqNo range validation while searching the flash offset for a valid event entry.
Issue Description: When searching for a valid event from beginning of a flash block, as per logs invalid offset is being returned in spite of length, code and CRC values of EVENT_PACKED for validations.
As a result the Seqno which is used to reference the the event is going outside the acceptable range which causes firmware to print the invalid event.
Steps To Reproduce: Media Error recovery Scripts runs through following steps on R1, R5, R6, R10, R50, R60
1.Create VD (cli.exe /c0 add vd type=raid1 Size=2000MB drives=252:1,252:2 pdcache=default wb ra direct Strip=256)
2.Fast Init
3.Full Init
4.Run IO using 'testio.exe -f\\.\PhysicalDrive1 -b256k -x 999m -q -p89'
5.Wait for testio to complete
6.Flush cache by changing VD cache policy to WT and the change it back to WB
7.Make the VD transition offline so that the controller marks it inconsistent (causing BGI to run)8. 'diskio.exe -f\\.\PhysicalDrive1 -Q -b256k -i2 -r70 -s0 -t64 -x1g'
8.Puncture 25 LBAs. For each LBA
9.Wait for BGI to start

Defect ID: DCSG00072261
Headline: For an OEM - eHBA mode - FW stuck in reset loop when Recon target drive goes missing during OCR
Description Of Change: Updated code to check for Recon LD Id before calling Pin Cache related functions.
Issue Description: For an OEM - eHBA mode - FW stuck in reset loop when Recon target drive goes missing during OCR
Steps To Reproduce: Steps:
Move controller to EHBA mode
Delete the config (VDs and EPDs)
Create 2PD R1
Start a Recon to R0 by adding 1PD
During the Recon, start an OCR and pull the target drive while the controller is in the middle of the OCR
FW never recovers

Defect ID: DCSG00077812
Headline: In RAID personality autoconfig off mode should not be displayed
Description Of Change: Off mode was present because of supportEPDWithAutoConfigOff value is set to TRUE. HII is uses this bit to display the option.
supportEPDWithAutoConfigOff should be FALSE in case of RAID/JBOD personality on Ventura Controllers and TRUE in Aero RAID personality
Issue Description: In HII Main Menu->Controller Management->Advanced Controller Management -> Manage Controller Mode, Off mode is present. It should not be shown.
Steps To Reproduce: Controller in RAID personality.
Go to HII preboot utility.
Go to Main Menu->Controller Management->Advanced Controller Management -> Manage Controller Mode.
Off mode is present

Defect ID: DCSG00079651
Headline: Auto R0 Available in eHBA mode, Fails when selected
Description Of Change: Now setting autoconfig parameter for not allowing executing once option for eHBA personality.
Issue Description: autoconfig parameter is not set correctly for allowing executing once option for eHBA personality.
Steps To Reproduce: Boot to Hii
Main Menu > Configuration Menu >
Select Auto Configure R0 (Confirm, Yes)

Receive error message:

The requested operation is not possible.

Defect ID: DCSG00079695
Headline: Fix code for proper use of patrol-read active and msgActive flags
Description Of Change: Updated the code path of profile change to use the appropriate patrol-read flag and pause status.
Issue Description: Fix code for proper use of patrol-read active and msgActive flags
Steps To Reproduce: This defect is very difficult to hit as the window of error is very small.
It will only happen if personality change is issued while PR is running and threshold exceeds.

Defect ID: DCSG00080240
Headline: NVMe Sanitize completion path and print message modifications
Description Of Change: Made changes to prints in TTY log and completion path for Sanitize command for NVMe drives
Issue Description: Made changes to prints in TTY log and completion path for Sanitize command for NVMe drives
Steps To Reproduce: Boot system and observe TTY logs

Defect ID: DCSG00081229
Headline: Autoconfig paramter Set Auto R0 Mode is not set correctly for eHBA personality.
Description Of Change: Now setting auto configure parameters correctly for eHBA personality and appropriate controllers.
Issue Description: For eHBA personality and controllers autoconfigure Auto R0 Mode parameter is not correctly set. Hence when apps are querying for this variable a wrong value is sent to apps.
Steps To Reproduce: 1. Controller should be in eHBA personality
2. Boot to HII application
2. Go to Main Menu -> Controller Management ->Advanced Controller Management.
3. App now sends a get command and wrong value is sent to application.

Defect ID: DCSG00074490
Headline: Unable to secure EPD in EKM mode after reporvisioning
Description Of Change: Securing of EPDs is blocked in EKM mode as per customer requirements
Issue Description: Securing of EPDs should have been blocked in EKM mode but was allowed to succeed. It has now been blocked.
Steps To Reproduce: Create EPD and attempt to secure it in EKM mode.

Defect ID: DCSG00077969
Headline: Incorrect slot mapping on UBM backplane with additional DFCs support
Description Of Change: FW to skip UBM DFC slot enumeration for controller Phys if slot is enumerated already.
Issue Description: When a single HBA connector quad is attached to a UBM backplane that supports additional DFCs (e.g. 4 x4 DFCs), the FW uses same set of Phys in the quad for slot enumeration on the additional DFCs, leading to incorrect slot mapping.
Steps To Reproduce: Attach 9500-16i HBA connector quad with static connector grouping in NVDATA to a UBM backplane supporting 4 x4 DFCs and boot up the system, observe incorrect slot number enumerated for the connector quad Phys.

Defect ID: DCSG00082201
Headline: Fault 0x6109 while running IOs and device remove test.
Description Of Change: The check to see if dma queue is disabled changed to match the hardware specification to include dequeue wait state.
Issue Description: When a device is removed or added back a Task management is run to reset the drive and abort all outstanding IOs to the drive. For the hardware cleanup state of task management firmware disables the DMA queue, after some delay firmware checks if the dma queue is disabled or not. If it is not disabled fw faults.

This check however was checking if all the dma state machines are in disabled state, but as per hardware specification one of the state can be in a 'dequeu wait' state and dma queue can still be marked as disabled.

Steps To Reproduce: Attach a few SAS SATA drives to controller and run heavy IOs while also removing attaching devices. After running this test for multiple hours sometime firmware fault 0x6109 is observed.

Defect ID: DCSG00081077
Headline: DHSP to GHSP is generating duplicate alerts
Description Of Change: Generate event only if drive is spare.
Issue Description: GHSP is generating same event twice when VD is deleted.
Steps To Reproduce: 1. Create a VD
2. Assign a DHS
3. Delete the VD
4. Check the alerts

Defect ID: DCSG00083472
Headline: Allowed Cfg Options does not show support for SINGLE_PD_R0 option
Description Of Change: When Application send get Autoconfig option command, FW was not sending R0 option. Fix is to send R0 option.
Issue Description: AllowedCfgOptions does not show support for SINGLE_PD_R0 when Application sends command to get Autoconfig options

Steps To Reproduce: 1. Boot to HII application
2. Go to Main Menu -> Controller Management ->Advanced Controller Management.
3. App now sends a get auto config command, FW sends incorrect value

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Defect ID: DCSG00069091
Headline: VSES SES Page 02h reports Unknown (06h) Element Status for some Array device elements in a wide DFC slot
Description Of Change: Updated VSES to report Not Available (07h) status in Page 02h for Array device additional Element/Phys in a wide (x2, x4) DFC slot when one or more Phys of the DFC has a device linked up.
Issue Description: On a UBM backplane with x2 and x4 DFC, VSES status Page 02h reports Unknown (06h) element status for unconnected Phys of SAS/SATA drives. This may cause discovery delay with RAID FW due to Bad/no-linkup retry, leading to longer time for new PD discovery.
Steps To Reproduce: On x2/x4 DFC UBM backplane with SAS/SATA drive installed in the slot, boot up the system and read VSES status Page 02h . Observe element status code Unknown 06h reported for additional elements/Phys of the DFC.

Defect ID: DCSG00078678
Headline: Ventura: The host PCIe link width may be narrower than expected
Description Of Change: Ensure the CSW_PCIEPCS_REG01_G2_REALIGN_GATE is set at SOD and on any exception that modifies the associated register
Issue Description: The host or device PCIe links width may be narrower than expected
Within the PCS logic provided by APD, the reset value of the G2_REALIGN_GATE signal (SBus register offset 0x1 in PCS, bit [9]) is a 0, whereas it was specified to reset to 1. This bug results in the PCIe "auto realignment feature" being disabled by default. This feature is considered to be required by DCSG as it compensates for temporal marginality within the data stream provided by the SerDes to the PCS
Steps To Reproduce: Only occurs in one OEM specific server's slot

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Defect ID: DCSG00084525
Headline: VSES - SES page not set correctly for Front adapters
Description Of Change: - Removed OEM related checks introduced in an ER, this way the behavior is now in parity with channel
- The OEM front adapters have their ports in descending order for the first connector, and in this case the element Index and slot Number is not one to one mapping. For this issue, the change involved sending bay Number (which is the true physical slot) as a parameter for slot Index instead of element Index in a function which checks if a given drive in a slot is a Raided volume or not.
Issue Description: - Removed OEM related checks introduced in an ER, this way the behavior is now in parity with channel
- Also made changes to send the true slot number which check if the given drive in a slot is a raided volume or not
Steps To Reproduce: 1) On a Front adapter; Windows 2019
2) set controller mode to eHBA and enable Host LED management
3) create a VD on disk in slot 0
4) all other disks non-raid
5) start locate on VD disk in slot 0 using perccli
6) Dump SES 0x2 and 0xA with utility (sg_utils/sg_ses)
7) For a given element check and verify the values of Status, Identify, SAS address
8) Cross verify with CLI application

Defect ID: DCSG00084535
Headline: SMART trip drive LED not blinking for specific OEM controllers
Description Of Change: Modified code to set predFail field in SCSI Device Control Command on Predictive failure
Issue Description: MR FW is not Setting predFail field in SCSI Device Control Command on Predictive failure. OEM Check was overwritten with CSET#DCSG00026840 changes.
Steps To Reproduce: 1) Insert SMART Tripped drive on Huracan 3.5x8 system
2) Predictive failed event appears within 5 minutes
3) Backplane LED does not blink Predictive Fail pattern

Defect ID: DCSG00087745
Headline: SEKM: Cannot Secure VD once VD is created
Description Of Change: MR FW does not cache controller key always. When controller key is not present in controller and user attempts to secure an LD, the operation was unsuccessful. The fix is to request controller key from external server when user attempts to secure an LD. Once the key is obtained, the LD can be secured.
Issue Description: Cannot Secure VDs on OEM controllers with SEKM enabled with the perccli command
Steps To Reproduce: 1. Create a non-Secure VD on SED.
2. Run the command:
cli /cx/dx set security=on

Defect ID: DCSG00080809
Headline: Patrol read (and CC) causing OS boot failure on media error correction
Description Of Change: Delay resuming the patrol read on boot up till the handshake with the OS is complete
Issue Description: With multiple uncorrectable media errors injected into VD (between 1000-2200 media errors) the patrol read resumed on boot up enters error correction and recovery logic which causes the host IO's to starve resulting in delayed boot up.
Steps To Reproduce: As part of a test we inject quite a lot of media errors into a VD (between 1000-2200 media errors) then start patrol read and reset the system. Upon the next boot after the controller has initialized it resumes patrol read and error correction. This causes a huge performance hit to all storage in the system including any storage that is not connected to the RAID controller and results in boot times up to 10 minutes.

Defect ID: DCSG00077835
Headline: For an OEM, Install of RHEL 8.0 using NVME PD R0 fails. It will error out during the creation of the UEFI partition
Description Of Change: Updated code to set optimalTransferLengthGranularity <= optimalTransferLength .
The field optimalTransferLengthGranularity is used by the kernel to set the min-io-size.
Issue Description: This issue is seen because optimalTransferLengthGranularity > optimalTransferLength.
Steps To Reproduce: Have a NVME setup on a 10 Bay Server
Created an R0 and fast init it.
Start the RHEL 8.0 installation
During the creation of the partition it will error out on "creating efi on /dev/sda1"

Defect ID: DCSG00096508
Headline: Some of the drives not listed under Widows OS Disk Management.
Description Of Change: Set the Port's enclosure handle same as device's enclsoure handle when a new device is discovered.
Issue Description: While reporting the device add event to host, the enclosure handle is set to the enclosure handle or the Port for that device. In some cases the Port's enclosure handle is not correctly set which may lead to device being added to incorrect enclosure and widnows driver not adding that device in OS.
Steps To Reproduce: Connect 3 out of 4 connectors to a UBM backplane and attach drives in the backplane. Some of the drives will not be added to OS Disk management.

Defect ID: DCSG00091414

Headline: Complete config missing boot message shown for NON-RLM case

Description Of Change: When RLM is in progress a critical OEM-specific message is issued ; but in the non-RLM case a non-critical generic boot message is issued.

Issue Description: For normal complete config missing as well as PD and VD missing cases, FW should not stop during boot in pause on error boot mode.

Steps To Reproduce: 1) controller in RAID mode
2) create R1 VD and no other drives configured
3) shutdown the system
4) remove the two drive R1 VD and boot system

Defect ID: DCSG00098242

Headline: Critical Boot messages not being handled properly during OCR

Description Of Change: For certain OEM , if RLM is in progress the desired behavior is to process boot messages immediately even for chip reset cases. This is because OEM wants MR FW to fault when there are critical boot messages pending, so that user is forced to shut down and fix the issue that caused the critical boot message to be issued.

Issue Description: 1) Create a R0 VD
2) start RLM on VD by adding two disks
3) OCR the controller
4) after controller starts reset pull the drives out
5) controller OCRs and crashes on reboot error is shown
6) shutdown, insert disks back into system, and boot
7) RLM VD missing, user is unable to import VD

Steps To Reproduce: 1) Create a SDR0 VD
2) start RLM on VD by adding two disks
3) OCR the controller
4) after controller starts reset pull the drives out
5) controller OCRs and crashes on reboot error is shown
6) shutdown, insert disks back into system, and boot
7) RLM VD missing, user is unable to import VD

Defect ID: DCSG00101763

Headline: Utility not providing an VD task to encrypt a VD (post creation)

Description Of Change: LDallowedOps secure was being incorrectly being set to 0 based on if controller key was present in controller SRAM. However, OEM's EKMS solution does not always store key in SRAM.
The change was to not check for key's presence if key caching is disabled.

Issue Description: MR_LD_ALLOWED_OPS.secure to be set to zero incorrectly when controller key is not cached.

Steps To Reproduce: 1. create an encryption key
2. create a normal VD with SED disks
3. now go to the virtual disk's task's - where you dont find any task to encrypt that VD

Defect ID: DCSG00096587

Headline: Aero config import from file fails with EPD-JBOD drives

Description Of Change: Added support to parse config data to detect and import EPD's in addition to raid VD's.

Issue Description: EPD information is included in the config information that is returned as a part of save/get config.
But when restore/set is done, EPD's were filtered before sending to firmware as add config does not support EPD.
This was causing config creation to fail as arrayref's were not adjusted during EPD removal.

Steps To Reproduce: 1. Make the first slot drive to JBOD; (slot 0 drive)
storcli /c0/e252/s0 set jbod
2. Create a RAID 0 VD with the last 2 slot drives; (slot 6 & 7 drives)
storcli /c0 add vd drives=252:6-7
3. Save the RAID config file
storcli /c0 get config file=config1.file
4. Delete the RAID config
storcli /c0 delete config
5. Import the config file. --> failed.
storcli /c0 set config file=config1.file

Defect ID: DCSG00074378

Headline: [Aero][AutoPort Enable] Erase persistent config pages is not retaining the VPD and sas address

Description Of Change: Do not create MPB until real sas address is programmed.

Issue Description: MPB is created as part of port enable even without configuring the real sas address.

Steps To Reproduce: 1) Enable auto port enable in nvdata and create a FW image.
2) Do a clean erase of the flash.
3) Flash the image prepared in step 1.
4) set the sas address using storcli (storcli /cx set sasadd = <>)
5) upload the MPB and see if MPB has sas address (storcli /cx get mpb file =<>)
6) Do a persistent page clean and see if sas address is not retained.

Defect ID: DCSG00111498

Headline: Change adapterOperations5.supportNvmeWidths to 0 as NVME is not supported

Description Of Change: Change supportNvmeWidths to FALSE for OEM specific controllers

Issue Description: Following needs to be set to 0 ci->adapterOperationExt.adapterOperations5.supportNvmeWidths

Steps To Reproduce: Connect NVME drives and verify it properties

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Defect ID: DCSG00103998

Headline: PL: Removal of NVMe Drive that Failed NVMe Init Doesn't Work Correctly

Description Of Change: For NVMe devices that have failed initialization and have gone missing, do the internal PL device missing delay task management, even if the device is not registered with upper software layers.

Issue Description: In order to process removal of an NVMe drive that failed initialization, MegaRAID relies on PL doing an internal task management target reset when the device goes missing. This was not occurring in some cases.

Steps To Reproduce: Use an NVMe drive that will fail NVMe init with a potentially recoverable reason. After init, pull the drive.

Defect ID: DCSG00111423

Headline: Dev-Defect: Incorrect default autoconfig parameters are returned for non zero confmode

Description Of Change: Updated code to set SES Mgmt to FW for an OEM if conf-mode is EPD Pass-through.

Issue Description: N/A - Issue discovered during code inspection.

Steps To Reproduce: N/A - Issue discovered during code inspection.

Defect ID: DCSG00108094

Headline: Expander attached devices not reported to host if enclosure slot ordering is enabled in event replay.

Description Of Change: Set the enclosure add event replayed flag after setting state to enclosure slot order state in event replay state machine.

Issue Description: The event replay state machine was setting the enclosure add event sent flag right after sending the enclosure add event. However before setting the state to enclosure slot order state it was checking to see if enclosure add event is sent or not this was to check if it was the first time the event replay state machine was handling this enclosure since in second round it needs to move to a different state to report missing devices. Since the flag was already set it was directly moving to report missing devices and device add events were skipped.

Steps To Reproduce: Set enclosure slot ordering during event replay bit in nvdata and attach an expander with some devices attached. Observe the device add event for expander attached device are not reported.

Defect ID: DCSG00104151

Headline: MR Ventura FW in JBOD mode still allows security erase by hdparm

Description Of Change: SATA securiy feature set passthrough commands will blocked on all drives in process dcdb path.

Issue Description: SATA_SECURITY_* commands are sent to a SATA drive in passthrough path (DCDB or STP). SATA securiy feature set passthrough commands need to be blocked on all drives in DCDB path, this is already blocked in process stp path.

Steps To Reproduce: #hdparm --user-master u --security-set-pass 123456 /dev/sda

Customer sees set security feature set command via hdparm fails in Invader but passes in Ventura.

Defect ID: DCSG00112320
Headline: VSES page 02h reports incorrect status for linkup failed array device element on certain UBM slots
Description Of Change: Updated FW to parse all the HFCs attached to the UBM in determining the DFC slot drive presence for SES element status reporting.
Issue Description: VSES diag page 02h reports an UNKNOWN (06h) element status for link failed Array Device element status present in a slot. In a UBM backplane managing more than one HFC, incorrect element status is reported for link failed array device elements attaching to the HFCs in the group.
Steps To Reproduce: On a UBM backplane with UBM controller managing more than one HFC, attach a link failed drive to a DFC slot routed to a HFC in the group. Observe, VSES diag page 02h reporting NOT_INSTALLED (05h) status instead of UNKNOWN (06h) status for the link failed element.

Defect ID: DCSG00118666
Headline: Dev-defect: Reset SES Mgmt flags after the reboot (not in the same boot) when personality changed to RAID.
Description Of Change: Updated code to reset SES mgmt related flags after the reboot.
Issue Description: In JBOD, with SES Mgmt enabled, if the user changes the personality to RAID and changes it back to JBOD, SES Mgmt related flags will be reset.
Steps To Reproduce: In JBOD personality, enabled SES Mgmt related option.
Change personality to RAID.
Change it back to JBOD.
Observe SES Mgmt related option and reset.

Defect ID: DCSG00119569
Headline: CLI allows auto configure R0 immediate command in ePD pass-through mode
Description Of Change: Now not allowing any R0 auto-configure command when in ePD passthrough mode.
Issue Description: Currently even in ePD passthrough mode, R0 auto configure is allowed. This should not be allowed.
Steps To Reproduce: 1) Change to auto configure mode EPD-PT via CLI
2) Run cli command to set R0 autoconfig immediate command.
3) Command completes successfully. R0 VDs created on Unconfigured Good drives.

Defect ID: DCSG00119796
Headline: Dev-defect Use of OEM check in a function not correct.
Description Of Change: Removed non-functional code as the caller of the function overwrites the variable set by this code.
Issue Description: Dev-defect Use of OEM check in a function not correct.
Steps To Reproduce: N/A -- Discovered during code walk through

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Defect ID: DCSG00060347
Headline: NVMe devices VPD page 83 NAA descriptor may conflict with EUI64 ID reported
Description Of Change: Modified FW to report the VPD page 83 NAA descriptor for NVMe devices in new format by reversing the EUI64 and converting to NAA to prevent the VPD ID collisions.
Issue Description: VPD83 page for NVMe devices report EUI64 ID and EUI64 modified for NAA descriptor for associating NVMe devices with SES Page 0Ah. There are some NVMe device which report EUI64 with upper nibble already set to NAA value (03h) and FW modifying EUI64 upper nibble for some of the devices seems to cause VPD83 ID collisions.
Steps To Reproduce: Install NVMe devices to OEM specific UBM backplane attached to MR HBA and boot up. Observe duplicate slot numbers reported for the attached devices due to VPD83 ID collision.

Defect ID: DCSG00126872
Headline: SPDM: Attestation failed with wrong Nonce values
Description Of Change: Since SPDM Challenge command requires 32-byte nonce, Security Page 0 & 1 requires 64-bytes nonce, Nonce function changed to be more flexible. Now it will accommodate any none size up to PSEC_MAX_NONCE_SIZE=64bytes.
Issue Description: Nonce function fixed to 64 byte nonce (PSEC_MAX_NONCE_SIZE=64bytes),
Steps To Reproduce: run SPDM attestation

Defect ID: DCSG00111492
Headline: Direct attached PFA drive - LED is neither ON nor Blinking
Description Of Change: SES array element bits are updated for predictive failure case. This enables the legacy backplane set appropriate LED.
Issue Description: LED activity is not seen on predictive failure drive.
Steps To Reproduce: 1. Flash 7.12 GCA firmware(DCSG00058494) on a 9460-8i controller.
2. Connect a predictive failure drive without expander to a backplane whose LEDs are controlled through SGPIO.
3. Using storcli, send "show all" command to the predictive failure drive.
4. The storcli output should show "Predictive Failure Count" >= 1
5. The error LED in the backplane of the predictive failure drive will be neither ON nor blinking.

Defect ID: DCSG00113492
Headline: autoconfig field is not set to None when firmware is upgraded to current programme package
Description Of Change: Now checking whether current autoconfig option is not an allowed option in RAID personality. If it is so then autoconfig option is switched to default case of None.
Issue Description: There is no check on allowed autoconfig options for RAID personality. Hence when user upgrades from prior programme , wrong autoconfig option (R0) is allowed.
Steps To Reproduce: 1. flash controller with 50.9.4 firmware
2. set autoconfigure mode to R0
3. Flash 51.13.0 firmware and reboot
4. after reboot check autoconfig settings, autoconfig is set to R0

Defect ID: DCSG00132764
Headline: COL Failure on AC cycle
Description Of Change: This change is specific to Single COL Image. Set flashEraseRequired in NVRAM to TRUE only when ONFI erase is required(single Image and ONFI Flash has Valid Image on it and there is no Pinned cache present).
Issue Description: MR FW is setting flashEraseRequired=TRUE and this flag should be cleared as part of Preparing ONFI for next offload.
Steps To Reproduce: Reboot the system with Dirty Cache and then Power Cycle. COL will be triggered on Power Failure.Firmware reports cache lost even though COL is successful.

Defect ID: DCSG00212797
Headline: Observed Data Corruption during IO stress test.
Description Of Change: SGL translation worked fine after correcting the logic for fetching the next SGL in a IO request.
Issue Description: SGL translation was failing for Read/Write IOs during stress test. That resulted data corruption.
Steps To Reproduce: Update latest Firmware on 9560-16i board.

Run Stress test.

Observe the "Data Miscompare" error.

Defect ID: DCSG00149932
Headline: CurrentControllerMode Value is Showing "null" instead Of "RAID"
Description Of Change: For iMR controller support personality change is set to only get the personality.
Issue Description: For iMR controller support personality change was set as not supported. This caused the applications to no show the current controller mode.
Steps To Reproduce: Check Controller Properties & Verify CurrentControllerMode->it is showing null instead of RAID.

Defect ID: DCSG00147889
Headline: Disable break mirror support
Description Of Change: Disable break mirror support
Issue Description: Disable break mirror support
Steps To Reproduce: - Flash FW
- break mirror still works

Defect ID: DCSG00104797
Headline: Foreign configuration import fails after rekey operation.
Description Of Change: Changed scratch pad read size from fixed 50 bytes for opal drive to actual length.
Issue Description: Foreign configuration import fails after rekey operation.
Steps To Reproduce: 1) Create a R1 and R5
2) Remove the R1 and R5 drives.
3) Perform a rekey operation to rotate the keys.
4) Reinsert the R1 and R5 VDs and Attempt to import the VDs.

Defect ID: DCSG00081483
Headline: Secured EPD IO Error = media is write protected after continuous PushPull within 2 seconds
Description Of Change: IOs which are fired before the drive gets unlocked were being failed, which in turn caused the application to stop.
The change is to unlock the drive as part of recovery so that these IOs are not failed.
Issue Description: When IOs are run onto LKM secured OPAL NVMe drives and the drives are push-pulled within 2 seconds, IOs are stopped and IO application reports media is write protected.
Steps To Reproduce: - secured EPD with OPAL NVMe drive
- run chaos to secured EPD
- remove and reinsert EPD in continous loop in 2 seconds

Defect ID: DCSG00165400
Headline: NVMe Identify Controller sent over OOB fails with MFI_STAT_INVALID_CMD
Description Of Change: Nvme encapsulated frame changed to refer MFI_NVME_ENCAPSULATED structure to retrieve correct Opcode.
Issue Description: Nvme command was referring against the NVME_CMD_DWORD0 struct that is reserved for data returned from command, due to this opcode was not matching with the white list and through up invalid command.
Steps To Reproduce: Send the NVMe Identify Controller command over OOB

Defect ID: DCSG00118646
Headline: Auto Cfg Parameters Changed is not generated when host led management is changed.
Description Of Change: Now logging event for any parameter being changed.
Issue Description: Event is not generated because the event logged only when auto configure option was changed.
Steps To Reproduce: 1. Boot server with controller in auto configure none mode.
2. Go to Controller Management -> Advanced Controller Management.
3. Click on 'Enable Host LED Management of Non-RAID Disks'
4. Check OS application for events generated.

Defect ID: DCSG00119468
Headline: Cli utility allows auto config option when it is not supported
Description Of Change: Now checking for allowed valid parameters when a set command is received. Hence when set command is sent with a non changeable paramater set , invalid parameter status is returned.
Issue Description: Firmware is not checking for allowed parameter for auto config behaviour mode none . Hence command wrongly goes through.
Steps To Reproduce: 1. Boot SUT in default auto configure mode - Off
2. Run CLI command to enable automatic secure drives.
3. Command completes successfully

Defect ID: DCSG00127771
Headline: AUTOCFG parameters- EPDParams is set incorrectly for NONE/OFF mode
Description Of Change: Now setting the EPDParams correctly for None/Off mode
Issue Description: All EPDParams are cleared to 0 for NONE/OFF mode.
Steps To Reproduce: When ePD are created in None/Off mode the params are not set correctly.

Defect ID: DCSG00119480
Headline: MR controller resets
Description Of Change: 1.TTYLogInFlash is supposed to be copy of MFCD.ttyLogInFlash. This should have not been changed. But when tty logging to flash was to be blocked, for configuration related command over sideband, TTYLogInFlash was cleared and then later restored with MFCD.ttyLogInFlash. In between this, if TTY Read DCMD is issued, it would cause DATA TLB error, as FW didnt initialize the read buffers properly when TTYLogInFlash is cleared.
Solution is to define a new flag which specifically disables writing of tty to flash. Instead of changing TTYLogInFlash for sideband config command, FW should use this new variable instead to control the same outcome.
2.Ifdef flag to compile out the local buffer read for TTY read DCMD for iMR is removed.
Issue Description: 1.TTYLogInFlash was getting cleared while config commands came through sideband/OOB from BMC. This caused the TTY Read DCMD to have flash read buffer addresses set to 0, causing DATA TLB error on iMR controllers. On MR controllers this would cause TTY Read DCMD to send data from local buffer when TTYLogInFlash is disabled or from flash when TTYLogInFlash is enabled, thus log will have garbled up. This issue is affecting both iMR and MR. On iMR it leads to montask and OCR. On MR the tty log will be messed up.
2.On iMR controllers code to read from local buffer in case TTYLogInFlash was disabled at compile time. This caused the issue as well. On MR controllers this issue is not there.
Steps To Reproduce: To repro, use sideband utility to send collect command to collect
Also send command to read config at the same.

Defect ID: DCSG00134946
Headline: FW not checking bound on tty read DCMD, leading to send tty log twice.
Description Of Change: Bound check for the size of the request offset and making sure the actual read pointer points to valid flash address.
Issue Description: FW is not bound checking for the request virtual offset from the application. Also FW calculates the actual read offset from flash based on virtual offset plus read pointer from flash. The offset due to circular buffer nature of tty log, can land in the area between start and read pointer in case of wrap around case, when tty log in flash is full. This causes FW to send old tty log form flash multiple times.
Steps To Reproduce: 1. Enable pcidebug to log lot of tty messages, while IO is running.
2. Now collect tty dump via sideband.
3. after few retries tty dump will have same log messages twice in what is read.

Defect ID: DCSG00130055
Headline: Unsupported drive LED Solid Green on Rear Backplane - LED flashing green expected
Description Of Change: Update Required SES Control page field to blink LED
Issue Description: Firmware is not Updating Required SES Control page field to blink LED for unsupported drive.
Steps To Reproduce: Insert NVME drive on OEM specific SAS/SATA Controller.

Defect ID: DCSG00219908
Headline: [Aero/Ventura]Allow the backplane detection state machine to retry the FRU detection.
Description Of Change: Allow the backplane detection state machine to retry the FRU detection.
Issue Description: Backplane FRU data was not ready by the time controller tries to read FRU.
Steps To Reproduce: 1) Connect the HBA card to OEM Backplane with 10 slots which has all bay SAS/SATA support.
2) Connect drives in slots 0,1.
3) Perform DC cycle and observe that ODD cycles detect drives and Even DC cycles does not detect drives.

Defect ID: DCSG00151021
Headline: [Aero/Ventura] Unused phys are managed by VSes in SGPIO BP mode
Description Of Change: Avoid unused phys getting marked as SGPIO managed elements.
Issue Description: When 8i controller is mimicked as 4i by masking few phys in nvdata and connected to SGPIO backplane,
VSes still considers the unused phys as SGPIO managed elements.
Vses Enclosure diag page had entries for unused phys and allows SES_DIAG command to write to enclosure diag pages.
Steps To Reproduce: 1) Select a controller which has unused phys (iMR 4i controller)
2) Send the SEND_DIAGNOSTIC command for unused phys(4-7) to mark them faulty.
3) See that Phy getting marked as bad in applications.

Defect ID: DCSG00215315
Headline: Auto Configure EPD-PT set fails when sent with MR_AUTO_CFG_PARAMETER received from firmware for Auto configure Off mode
Description Of Change: Initialize epdParams appropriately for auto configure OFF mode.
Issue Description: Default settings for EPDParams for NONE/OFF is set as "0", instead it should be set as "B8" which is same as "epd-PT" mode.
Steps To Reproduce: Enable AutoConfigDebug debug flag.
Load HII Manage Controller Page for auto config OFF mode.
Observe that the log show all the EPD related params as 0.

Expected: The following flags should be set to 1.
disableErrorRecovery, disablePinnedCache, epdParams.MRIEMode and dontFailPDOnError

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Defect ID: DCSG00171248
Headline: Expander_FW : Expander FW upgrade or downgrade through CIMC is not getting reflected on host applications
Description Of Change: This issue caused because of the Inquire command update is not happened after CUB EXP firmware update and reset happened. There is a logic already present issue Inquiry command after received unit attention from the SES device. But upon successful response received with new inquiry data received were not getting update in the current global SES PD information structures.
Issue Description: After the SES CUB FW update reset device received Unit Attention to Firmware. This unit attention triggered to update the new inquiry data from the device. But these new data was not updated to the global PD structures to reflect immediately.
Steps To Reproduce: 1.The issue can be recreated on LagunaBeach+ or Madeira systems.
2.Pick either phase 9 or Phase 11 latest expander Binaries.
3.Take one version previous expander version for upgrading or downgrading.
4.Note Expander FW version in LSA or Storcli (storcli /c0/ex show) before upgrading or downgrading.
5.After the upgrade through CIMC or SASEXP the new versions are not getting reflected in host applications.
6.After the OCR the same is reflected.

Defect ID: DCSG00107743
Headline: FW faults during driver unload and load process
Description Of Change: Fixed in Firmware by gracefully handling the oob commands during driver unload and load timing window
Issue Description: During the driver unload and load timing window, the oob commands local memory is getting corrupted.
This causes the FW fault when the memory validation happens for the oob command during completion
Steps To Reproduce: Perform the AC cycle test with MR driver unload and load for iMR adapter.
Read the Adapter or PD info from StorCLI. But, the iMR adapter is not visible in the host.

Defect ID: DCSG00220882
Headline: MR7.15 PA: FW gets hung while generating snapdump through MegaMon call SnapDumpDbgGlobalOnly
Description Of Change: The Snapdump error handling code was improved. Conditions were added so that it handles an assert within a data collection function.
Issue Description: The test case gets the controller into a state where DMA operations fail. The tester then triggers a Snapdump. The DMA failures cause a Snapdump data collection function to fail.
This exposes a bug in the Snapdump error handling. The Snapdump code is supposed to close the partial zip file and restore printing. It fails to do this.
Steps To Reproduce: 1. Boot in MR7.15 FW in Linux OS with MR7.15 driver.
2. Enable device order by firmware.
3. Reboot.
4. Downgrade to a MR7.14 FW. Use noverchk if needed to force the downgrade.
5. Reboot to OS and try to access the controller.
6. Enter MegaMon and try to generate a snapdump.

Defect ID: DCSG00136092
Headline: [NVMe] SCSI log sense command timeouts seen while running 1MB IOs to NVMe drive
Description Of Change: For translation of SCSI log sense command allocate local buffer based on the page size of the NVMe log page to read. Instead of allocating a large buffer that can accommodate all supported log pages.
Issue Description: 1. There is a stream of host IOs with data size more than the MDTS size of the drives.
2. This requires PL to break up the IO in MDTS size chunks. To do this PL needs to allocate memory from its PCI dynamic memory buffer.
3. While these IOs are running MR periodically sends a non RW IO SCSI Log sense to read the information exception logs page.
4. To translate SCSI Log Sense command PL needs to allocate 1K memory from the PCI dynamic buffer. This fails due to resource crunch, and the non RW IO gets added to Pend Queue.
5. Since RW IO translation requires a lesser amount of memory (512B), if there are any RW IOs in the pend queue they get started but the SCSI Log sense command keeps getting pended to the tail of the pend queue eventually leading to its timeout.
Steps To Reproduce: 1. Attach 2-3 NVMe drives that have very low MDTS (128K).
2. Run large size IO (1MB) to the drives.
3. Periodically send SCSI Log Sense command to read Information Exception log page to the drive.

Defect ID: DCSG00124592
Headline: [9460-8i+MR7.12 Patch+X86] Use script to upgrade Huawei-made SAS SSD firmware underneath 9460-8i (7.9, 7.11, and 7.12) will fail
Description Of Change: Allow the OEM 0xC1 download command to be the issued to the restricted device by allocation a restricted frame for it, so that it is not blocked in Wait Queue.
Issue Description: OEM command 0xC1 was blocked in Wait Queue as the device was restricted due to firmware download.
Eventually issuing it out of order was causing drive to return sense code making drive to go to shielded state failing download process.
Steps To Reproduce:
1. sleep 2s
2. storcli /cx/ex/sx download src=FW
3. sleep 2s
4. issue SCSI pass-through command (0xC1, 0x26, 0x0, 0x0, 0x0, 0x0) to activate via storlibtest
5. sleep 10s
6. storcli /cx/ex/sx download src=FW <<<< fails here, error code 45 device busy or unexpected error occurred
7. sleep 10s
8. check see if new FW(3232) have been updated using storcli /cx/ex/sx show all.

Defect ID: DCSG00113956
Headline: In JBOD profile, set VD Write Cache to AWB shows success even though WB Supported is set to NO
Description Of Change: Set Write policy as FALSE if the profile does not support write back, so that the request to set cache to write back or always write back is failed.
Issue Description: In JBOD personality request to set write back cache on VD is not applied as the mode does not support write back cache. The VD is reverted to write through but the failure is not notified to application causing app to show success.
Steps To Reproduce: 1.Set controller mode to JBOD personality and profileid=20. and reboot to make it take effect.
2.create VD;
3.use storcli /cx/vx set wrcache=AWB to set VD write Cache to AWB.

Defect ID: DCSG00224879
Headline: NvmeAdmin: 'Exception handler called' observed while converting drive to Non RAID preceded by Export Log from OM
Description Of Change: Updated the PRP free function to free all the PRPs.
Issue Description: PRP free function was not freeing all the PRPs
Steps To Reproduce: 1. Using a utility, do a Nvme Admin commands for get log (error) on a drive that supports 255(FF) max-error-entries.
2. After few minutes execute "Convert to Non RAID disks" option on other Vendor drives or different Toshiba drive.
3. Observes Controller Exception Handler errors

Defect ID: DCSG00120410
Headline: Correct Nvme Double Buffer module for multiple double buffer cases.
Description Of Change: According to SPEC, change Nvme Double Buffer handling to following cases:
1. Only one 4kb double buffer is needed => only PRP1 entry is used (a)
2. Only two 4kb double buffer is needed => PRP1 and PRP2 used as pure PRP entry (b). Validate Nvme identify with 4136 host buffer length. Compared storelibtest log output for option (1) versus option (2) with 4136 host buffer length. They are same result except with more zeroes at the end which is expected.
3. More than two 4kb double buffer is needed => PRP1 as pure PRP, PRP2 as PRP list (c) Issue Nvme Identify with 8300 byte host buffer. This still yields in FW fault as drive seems to see PRP list as buffer address instead of pointer to buffer address for Identify Command.
Case 3, there will be another record to block or trim down bunch of Admin commands with larger than SPEC defined size received from host.
Issue Description: Nvme Double Buffer currently categorized into two cases:
1. Only single 4k buffer is used. FW use PRP1 as pure PRP entry.
2. Multiple 4k buffers are used. FW use PRP1 as pure PRP entry and PRP2 as PRP List.
This does not fully comply with the Nvme SPEC.

Following is posted from Nvme SPEC.
If CDW0.PSDT is set to 00b, then the definition of this field is: 39:32
PRP Entry 2 (PRP2): This field:
a) is reserved if the data transfer does not cross a memory page boundary.
b) specifies the Page Base Address of the second memory page if the data transfer crosses exactly one memory page boundary. E.g.,:
i. the command data transfer length is equal in size to one memory page and the offset portion of the PBAO field of PRP1 is non-zero or
ii. the Offset portion of the PBAO field of PRP1 is equal to zero and the command data transfer length is greater than one memory page and less than or equal to two memory pages in

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size.
c) is a PRP List pointer if the data transfer crosses more than one memory page boundary. E.g.,:
i. the command data transfer length is greater than or equal to two memory pages in size but the offset portion of the PBAO field of PRP1 is non-zero or
ii. the command data transfer length is equal in size to more than two memory pages and the Offset portion of the PBAO field of PRP1 is equal to zero.

31:24
PRP Entry 1 (PRP1): This field contains the first PRP entry for the command or a PRP List pointer depending on the command.

Steps To Reproduce: Using storelibtest to issue Nvme Admin Identify command with larger than 4k host buffer.
And observe FW faulted.

```
        ...NVME Encap Passthru Menu...
                ----------------
(1) NVME Identify (2) Any NVME Encap Passthru

0 TO QUIT. Invalid option to return to Previous Menu
Please enter choice : 2


Enter NVMe Device Id (DEC) --> 08
Enter Time Out Value (DEC) --> 30
Enter NVMe Encapsulated Command Length (MAX = 128) (DEC) --> 64
Enter 64 NVMe cmd in Hex ---> encapsulatedNVMeCmd[0] = 0x06
encapsulatedNVMeCmd[1]  [39]  = 0x0.
encapsulatedNVMeCmd[40] = 0x01
encapsulatedNVMeCmd[41] - [63] = 0x0
Enter NVMe Error Response Allocation Length (MAX = 32) (DEC) --> 32
Enter NVMe Encapsulated Flags (DEC) --> 50
Enter Cmd Direction (0->no data transfer, 1->transfer from host, 2->transfer to host, 3->transfer both to and from the host (DEC) -
Enter NVMe Response Data Length (DEC) --> 4136
```

Defect ID: DCSG00239272
Headline: supportEPDWithAutoConfigOff supported bit is set as 1
Description Of Change: Now setting the supported bit to 0
Issue Description: This is not a user configurable parameter . hence supported bit should be 0
Steps To Reproduce: 1. Enable 'eb AutoConfigDebug 1'
2. Go to HII->Controller Management -> Advanced Controller Management -> Manage Controller Mode
3. Observe TTY log

Defect ID: DCSG00243152
Headline: Out of bound memory access when assigning dma group for controller devices.
Description Of Change: Added a check to see if SAS core number goes beyond actual number of SAS cores then do not perform any operation.
Issue Description: For controller devices the port number is set to invalid value 0x1F the SAS core number is calculated as port/(numphys per SAS core) which gives the value 3 and this is used in an array while setting the dma group which only has 3 elements.
Steps To Reproduce: Not applicable.

Defect ID: DCSG00236990
Headline: [9440-8i+MR7.12/7.13/7.14Beta2+ARM] controller FW printed Assertion failure in fw\cpu\arm\exceptions.c at line 1006: 0 during fio issue verify(2F) commands to sas hdd(JBOD)
Description Of Change: Verify MPT request Sub-type for Sys-PD and skip the check for Unaligned request check for LD IO that access LD structure causing a data abort.
Any Unaligned request for Sys-PD will be handled by Drive and not MR FW.
Issue Description: Unaligned request check intended for LD IO path was causing Data abort on SYS PD IO request handling.
Steps To Reproduce: create JBOD on iMR and run fio Butterfly seek pattern.

Defect ID: DCSG00227153
Headline: CTRL_MFC_DEFAULTS_SET DCMD returning error when controller is in eHBA mode
Description Of Change: MR_MAX_AUTO_CFG_OPTIONS defines the max possible autocfg option value
autocfgOption cannot take more than value MR_MAX_AUTO_CFG_OPTIONS for Megaraid
Issue Description: DCMD CTRL_MFC_DEFAULTS_SET as a result of cli sent to controller in eHBA mode return an error.
Steps To Reproduce: 1. Configure Controller in eHBA mode
2. Using SDM send DCMDMFC_DEFAULTS_SET

Defect ID: DCSG00243849
Headline: Low risk temporary solution for preventing duplicate target Ids
Description Of Change: Reconstruction is blocked when the target Id needed for reconstruction is already in use
Issue Description: When reconstruction is requested with an existing volume having a target Id of 239 on MR or 31 on iMR, Firmware will start reconstruction with a duplicate target Id causing corruption of structures managing the hardware divert engine.
Steps To Reproduce: 1. Create volumes until a target Id of 239 on MR or 31 on iMR gets allocated
2. Start recon to create duplicate target Ids

Defect ID: DCSG00238473
Headline: MR_7.15: Driver load/unload result to Assertion failure in fw\hw\debug\ptb.c at line 618: 0 on Aero card
Description Of Change: The PTB code was updated to handle back-to-back loads of the operating system driver.
Issue Description: The PTB code is notified when the operating system driver is loaded. However, this code had difficulty handling back-to-back loads, and correctly asserted.
Steps To Reproduce: Load and unload the operating system driver in a loop.

Defect ID: DCSG00238510
Headline: MR_7.15: User disabled PTB not reflected, hence PTB.txt is part of OnDemand SnapDump
Description Of Change: Corrections were made to firmware so that the setting is stored correctly in persistent memory.
Issue Description: When the user disables PTB, the new setting is passed to firmware. However, firmware is not storing it correctly. So the setting reverts.
Steps To Reproduce: Boot into HII, and disable the PTB. Boot into the operating system and collect an on-demand Snapdump. Open up the Snapdump and it will erroneously contain a PTB file.

Defect ID: DCSG00241021
Headline: MR_7.15: PTB switch to Enabled and Save. No PoP up message reboot required/PTB.txt not part of Snapdump.
Description Of Change: The firmware that handles the setting change was updated. It will now return a different status when a reboot is required. This causes HII to display the popup at the appropriate times.
Issue Description: Since the reboot popup is missing, it's possible to continue booting the server. Any snapdumps that are created will be missing the PTB file even PTB has been re-enabled.
Steps To Reproduce: Boot into HII. Disable PTB. Continue booting into the operating system. Reboot the server. Enter HII again and enable PTB. At this point, there should be a pop up saying that a reboot is required. However, that is missing and the user is allowed to continue booting into the operating system.

Defect ID: DCSG00212592
Headline: MR7.14: Controller Bios never sent the printing-has-completed DCMD
Description Of Change: Firmware was updated to recognize cases where the Bios and firmware do not synchronize before operating system boot. This avoids logging PTB data later that is not helpful.
Issue Description: Some UEFI implementations do not fully support events. The MR PTB implementation requires events. Since an event callback was not made, Broadcom Bios and controller firmware did not synchronize before operating system boot. This led to unhelpful data being included in a subsequent Snapdump in the PTB file.
Steps To Reproduce: Run a reboot test with 7.14 code.

Defect ID: DCSG00255330
Headline: Last LDBBM entry in the list is not cleared after VD Deletion
Description Of Change: Cleared last LDBBM entry after VD deletion.
Issue Description: VD deletion doesn't clear last LDBBM entry in the list causing potential data corruption if recon happen, and ghost LD target ID matches the last LD that the LDBBM belonged to. For Aero/Venture, the last LDBBM is only cleared when last LD is deleted, which will not suffice.
Steps To Reproduce: 1. Create max possible 64 VDs, first 62 VDs are R0 and last two are fast path capable R5 WT NRA Direct VDs.
2. Injected X number of medium errors on 2 PDs at the same LBA that were part of last R5 VD63
3. Run read IOs on last R5 VD63

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4. Delete 1st R0 VD0,
5. Start migrating second last R5 VD62 to R6,
6. FW removes divert node entries for regular VD63 accidentally

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Defect ID: DCSG00099330
Headline: Controller crash and resets on attempt to boot to windows OS
Description Of Change: Now handling the case wherein reverse calculation produces an abnormally larger targetID. When this happens firmware fails the command back to host so that controller does not crash.
Expectation is that after boot up user will update to latest driver so that there is no compatibility issue and all features are functioning properly.
Issue Description: The issue happens because of the OS has inbox driver which is not of the current generation. Hence the current controller firmware and this old inbox driver version are having compatibility issues.
When host sends commands to enclosure directly, the old driver sends the command with targetId filled in message frame.
However the latest drivers have different mechanism/calculation to fill this targetId. Current firmware handles this calculation and can uses the re calculated target Id. However when firmware receives command from old driver this reverse calculation to get the targetID produces an abnormally large number. When this garbage targetID is used further , it causes illegal memory access.
Steps To Reproduce: Upon beginning attempt to boot to windows OS, Driver does not load and system enters OCR state.

Defect ID: DCSG00113486
Headline: VSES: Incorrect linkup failed elements status reported on certain slots of the UBM backplane
Description Of Change: As an interim solution, the reporting of array device slot elements present but not linking up will be disabled for OEM specific UBM backplanes and in future phases, the UBM DFC Array device element status code will used for reporting the status of device not managed by the HBA.
Issue Description: VSES features reporting the status of Array device slot elements that are present in a slot but not discovered by the PL through "UNKNOWN" 6h element status code. On certain OEM UBM backplane, the failed to linkup element status is reported incorrectly on certain slots.
Steps To Reproduce: On OEM specific UBM backplane, install NVMe drives in slots attached to host.
Connect OEM specific MR RAID adapter and boot up.
Observe, MR FW registering Bad Phy AEN event on the slots attached to Host.

Defect ID: DCSG00253426
Headline: UNMAP support is blocked and disabled
Description Of Change: Enable the UNMAP support in FW
Issue Description: UNMAP appears to be not working for SSD VDs in MegaRAID
When the SSD is configured as JBOD, UNMAP works
When the same SSD is configured in an R0, UNMAP does not work.
Steps To Reproduce: 1. Use a SAS SSD to create unmap capable RAID0
2. In Linux issue the following command: unmap -l 1 -n 512 -vf /dev/sdx
3. Issue will happen "unmap Fixed format, current: sense key: illegal request"

Defect ID: DCSG00258471
Headline: Dev-Defect - PRP-List overwritten in Double-Buffer-Copy-To-Host for response size > 8K
Description Of Change: Update the relevant code to update ptrPrpList only once.
Issue Description: For a response size of > 8K, Admin data returned to the host app will be incorrect.
Steps To Reproduce: None. This was discovered during code inspection

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Defect ID: DCSG00286358
Headline: ventura build issue with PL PCI DEVICE feature disabled
Description Of Change: Added PCI related code under the PL PCI DEVICE feature macro
Issue Description: ventura build issue with PL PCI DEVICE feature disabled
Steps To Reproduce: make all

Defect ID: DCSG00298128
Headline: As part of the Device Add\Removal Event, the enclosure handle passed on by the PL FW to the upper layer is incorrect.
Description Of Change: PL FW will be modified to determine the ParentDevHandle using the Port Number instead Phy Number associated with the discovered device.
Issue Description: PL FW determines the ParentDevHandle associated with a direct attached device using a static logic. When devices boot up in Phy order basis, the ParentDevHandle is correct. When the devices do not boot up in Phy order basis, due to dynamic Port Number assignment, ParentDevHandle assignment yields incorrect value, which results in passing incorrect enclosure handle associated with the device.
Steps To Reproduce: 1. Connect Multiple UBM backplanes to controller there by creating a Multi-vSES topology.
2. Hot Plug the devices which share same SAS core with the devices from the other UBM.

Defect ID: DCSG00243834
Headline: MR FW not responding to resume within 3 seconds
Description Of Change: Fix is that if there is a config command over OOB is pending, and interrupt nesting happens, then FW will process the I2C (OOB) interrupt in the interrupt context itself. Any new command will be added as a task to be processed later.
Issue Description: If an I2c (OOB) interrupt happens while FW is processing another interrupt (interrupt nesting) then FW adds a task to handle that interrupt later. It seems during config creation due to FW been processing other task, the I2C (OOB) task take long time to before starting processing, and in this case was beyond 3 second thus BMC timing out.
Steps To Reproduce: Ran the script to create 240 VDs.
Script ran and created a job to create 240 VDs
Job is getting as "Completed with Errors"

Defect ID: DCSG00297794
Headline: 9440-8i System black screen and hang during S4 + CC stress
Description Of Change: Device recovery state machine in firmware is updated with appropriate return status from spin up recovery state machine.
Issue Description: Drive spin up fails during device recovery.
Steps To Reproduce: Issue hibernate on OEM work station, when the drives are spun down.

Defect ID: DCSG00297806
Headline: After loading aero driver, the VD of the controller cannot be listed
Description Of Change: Handling in FW not to assert when bar update request came for pcie devices if backend pcie already disabled
Issue Description: Assertion seen when the bar update request came for backend pcie devices
Steps To Reproduce: Load MR driver when SAS/SATA only backplane is connected to controller on windows

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Defect ID: DCSG00221279
Headline: MR 7.15: Invalid Arguments error seen while setting config file w.r.t JBODs from Storcli.
Description Of Change: Extend logic to create config structure per EPD and create one EPD at a time.
Issue Description: For manual EPD creation, logic was added to update arraycount only for PD passed by user and skip rest of PD in bitmap. However same logic was not added when creating config structure causing offset error for import case with multiple EPD's.
Steps To Reproduce: 1. Connect an Aero controller to the system.
2. Flash latest MR 7.15 firmware (FW Package Build = 52.15.0-3334)
3. Copy latest Cli on the system.
4. Create mutiple EPD's and save config.
5) Delete config.
6) Restore config with the saved file.

NVDATA_XSD Enhancements Implemented (323):

EnhancementRequest ID: DCSG00007471
Headline: Allow host utils to manage CSWs individually in the presence of UBM
Description Of Change: Allow host to change the PCIe link config of Phys in link at the CSW level when UBM backplane is used in the configuration. The PCIe IO Unit page 0 link flag MPI26_PCIEIOUNIT0_LF_CFG_SRC_BACKPLANE is set for all the Phys in a CSW when subset of CSW Phys link config source is UBM.

EnhancementRequest ID: DCSG00007512
Headline: Ventura/Aero: Get debug file array sizes via a API variable for CFGI and PL
Description Of Change: This allows firmware to eliminate pl-specific build paths and debug information, cleaning up the interface

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EnhancementRequest ID: DCSG00007514
Headline: [Aero][Pldm] Clean PLDM make files
Description Of Change: Remove the invalid references in PLDM make files.

EnhancementRequest ID: DCSG00007958
Headline: Create a new firmware image that provides an AVSO setting of 0.997V
Description Of Change: Added lines to makefiles that build an alternate firmware image for Ventura.
This firmware image contains an RMC that sets the AVSO to 0.997V.
For customers that desire this AVSO setting, they must use this new raw firmware as the basis for their complete image.

EnhancementRequest ID: DCSG00007993
Headline: Add support for managed switch (Atlas) WWID in Vendor Specific Extended Capability
Description Of Change: Added function to send commands and recieve reply from Atlas using vendor specific extended capability(VSEC).
During PCI discovery, obtain WWID from switch and use the same as enclosure logical ID.
Number of slots in the enclosure is set to the number of downstream ports obtained from switch using VSEC messaging.

EnhancementRequest ID: DCSG00008045
Headline: Update PLI Spec
Description Of Change: - Updated spec from latest source code
- Removed AHCI
- Added Marlin & Aero family chips
- Changed Avago to Broadcom
- Misc. minor fixes

EnhancementRequest ID: DCSG00008046
Headline: Create method to give verbose fault code descriptions
Description Of Change: Created a Protocol Layer fault and error code document similar to controller firmware error code document.
Made current one line descriptions of error/fault code as 'brief' descriptions.
Added template for 'detailed' description for error and fault codes.
Added PL error codes and PLI document creation for MR PL Lib build script.

EnhancementRequest ID: DCSG00008197
Headline: Aero: Add permissions to access additional registers for Scrutiny
Description Of Change: Added R/W access to registers starting at 0xFFE14000 for 0x100 bytes

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EnhancementRequest ID: DCSG00008208
Headline: Create PLI interrupt handler timestamp log
Description Of Change: Timestamp log added in PLI interrupt handlers to record time when the interrupt handler is called.
The log has last 10 entries for each PLI interrupt handler.
Added CLI command to dump it and added the command to "pl dbg"

EnhancementRequest ID: DCSG00008993
Headline: Update summary release notes
Description Of Change: Added new AVSO image, Aero UART speed change and NVMe drive detection issue.

EnhancementRequest ID: DCSG00009002
Headline: pl: backend PCIe: enhance robustness of PCIe-related MPI event generation
Description Of Change: Provide the PCIe-related MPI event generators with a larger selection of resource frames to reduce the likelihood of allocation failure.

EnhancementRequest ID: DCSG00009014
Headline: SPILIB(2): SPI Library based upon API 2.0
Description Of Change: Updated SPI Library based upon the API 2.0 documentation.
Eliminates support for host-based peeking and poking
Uses bit-fields for easier support
Uses many less device register writes and should be much faster in slow CPU's

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EnhancementRequest ID: DCSG00009402
Headline: Aero/Ventura: Misc debug fixes and enhancements
Description Of Change: Fix GPIO writing and dumping for GPIOB on Crusader
Fix header on unread VSES page 2
Add additional debug prints for UBM

EnhancementRequest ID: DCSG00010053
Headline: Aero: Add limited support for IEEE SGL chains that point to DDR memory for Managed Switch SES
Description Of Change: Add limited support for IEEE SGL chains that point to DDR memory for Managed Switch SESes (attached via an MPI Device). Only one chain is allowed per MPI Device. This is to enable the few use-cases that perform better with re-using a buffer as a bit-bucket buffer to skip unneeded data (i.e. MPI SCSI Enclosure Processor Request).

These SGEs must use the IOCCTL define (MPI26_IEEE_SGE_FLAGS_IOCCTL_ADDR) for the Data Location Address Space field.
Any SG Chains must use the MPI IEEE define (MPI26_IEEE_SGE_FLAGS_NSF_MPI_IEEE) for the Next Segment Format field.

Only 4 scatter gather entries are allowed in the translated chain segment. Larger numbers of SGEs may be supported in the future.

An MPI SCSI IO frame with IT firmware allows for 2 SGEs, one of them points to this translated chain segment.
So 5 SGEs pointing to data buffers can be used.

EnhancementRequest ID: DCSG00010069
Headline: Add PERST# clamp to nvdata
Description Of Change: Added PERST# clamp entry for GPIO
Modified ISTWI entries for UBM
Added entries for I2C OOB

EnhancementRequest ID: DCSG00010274

Headline: Aero: Add yet more ranges for scrutiny signal integrity
Description Of Change: Added PDB2 and PDB3

EnhancementRequest ID: DCSG00010293
Headline: Aero/Ventura: Integrate SPILIB 2.0 into IT firmware
Description Of Change: Made necessary changes to allow firmware to use the SPILIB 1.0 or 2.0 API's on a build option basis

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EnhancementRequest ID: DCSG00010302
Headline: Update Sasparser path in additional files
Description Of Change: Location of SASParser moved in new DB2.

EnhancementRequest ID: DCSG00010543
Headline: Aero: check in ACM-enabled partial file for Sea eval board
Description Of Change: Checked in the partial NVDATA file that enables Active Cable Management on the Sea eval board that was generated while debugging a recent issue.

EnhancementRequest ID: DCSG00010679
Headline: Aero/Ventura: Add auto-downgrade algorithm
Description Of Change: When the major nvdata version of the backup region is less than the major nvdata version of the main firmware region, this firmware will automatically erase the config areas, eliminating the need for the host to do so. Therefore, if the user saves all of the necessary manufacturing data in the MPB, it will perform an effective downgrade of the firmware with appropriate factory parameters.

EnhancementRequest ID: DCSG00011488
Headline: NVMe Device PCIe Configuration Space Access DCMD
Description Of Change: Implemented a mechanism for OEM to access NVME PCIe information.

EnhancementRequest ID: DCSG00011555
Headline: pl: backend PCIe: allow override of backplane link config for debug
Description Of Change: Added flags in PCIe IO Unit Page 1 to enable override of the automatically generated backend PCIe link configuration for debug.

EnhancementRequest ID: DCSG00011562
Headline: pl: update combo serdes library
Description Of Change: Integrated the latest version of the Gen 3.5 (Ventura/Mercator) SERDES library with PL.

EnhancementRequest ID: DCSG00012208
Headline: Ventura: Fix OEM DeviceSpecific fields
Description Of Change: Fixed lane masks for OEM device specific fields

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EnhancementRequest ID: DCSG00012331
Headline: [Aero][Pldm] Print Implementation
Description Of Change: 1) IT interface exposes the print interface to PLDM lib.
2) Any prints in PLDM lib is done via this print interface.

EnhancementRequest ID: DCSG00012454
Headline: pl: backend PCIe: check in some plugfest diag console code
Description Of Change: Checked in some diag console code that was written to collect information for the recent NVMe plugfest. It's compiled out by default.

EnhancementRequest ID: DCSG00012583
Headline: Add new MR Event to notify user of PCIe hot reset fail
Description Of Change: Log new MR event if hot reset of PCIe device fails.

EnhancementRequest ID: DCSG00012641
Headline: SPILIB: Modify Spilib 2.0 print settings to allow some prints in INFO
Description Of Change: Make it so minimal prints are done at INFO level

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EnhancementRequest ID: DCSG00013067
Headline: SES Access Control - prevent access to DA-SEP
Description Of Change: SES Access Control - prevent access to DA-SEP for OEM Mercury

The Parent PR ID is SCGCQ01936065 (older database)

EnhancementRequest ID: DCSG00013345
Headline: Diagnostic command changes via OOB
Description Of Change: The design philosophy is to re-use existing infrastructure for the diagnostic commands and enable them for the OOB. After some careful thoughts we excluded any API changes or call back functionality per the software architect team. The most important thing in this design to be able to successfully differentiate between the commands coming from the in-band compared to the out of the band interface. The goal will be the re-use of the existing diagnostic functionality so that differentiation will help in excluding tests such as DMA from diagnostics. We do not have on-board memory available during running of the out of band diagnostic commands.

1. A new flag shall be defined in the CMD_INFO structure called is OOBCmd:1 to differentiate between an in-band and out of band command.
2. A new argument is defined for MfiCmdIssueLocal() function. The argument have the flag isOOBCmd as the third parameter of type Boolean. It is the callers responsibility to setup the flag accurately, when calling the function, MfiCmdIssueLocal(). The new defined parameter in the function is shown as follows:

MfiCmdIssueLocal(MFI_CMD *mf, CMD_DONE_FUNC func, boolean isOOBCmd)

The above approach provides a comprehensive mechanism for even a new OOB handler. It re-uses the existing design logic and ensures, that even if the logic is changed the design will remain the same.

EnhancementRequest ID: DCSG00013352
Headline: SPILIB2: Eliminate address mask for Avenger Compatibility
Description Of Change: Eliminated mask and altered method of determine whether to use base/size passed in by user
User must now zero both DcrAddressBase and DcrRegionSize if they wish to use default data.

EnhancementRequest ID: DCSG00014014
Headline: Ventura: Fix OEM Page7 Data
Description Of Change: The dual x4 card does not have interleaved phys, normalized the connector information

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EnhancementRequest ID: DCSG00014521
Headline: Update FW code to Disable SafeMode Boot on OCR using NVDATA.
Description Of Change: Provide an option to the OEMs to enable/disable disableSafeModeOnOcr at their discretion at the time of NVDATA creation.

EnhancementRequest ID: DCSG00014564
Headline: pl: NVMe: RTD3 Entry Latency shutdown timing
Description Of Change: PL now reports each NVMe device's shutdown latency in PCIe Device Page 2 and utilizes it when performing NVMe shutdown.

EnhancementRequest ID: DCSG00014807
Headline: Disable Active Cable Mgmt. IntL GPIO configuration from default NVDATA
Description Of Change: Disables Active Cable Mgmt. IntL GPIO configuration from default NVDATA.

EnhancementRequest ID: DCSG00015055
Headline: Aero/Ventura: Add capability to return UNKNOWN status in SES, page 2, when link is down yet presence detected
Description Of Change: In order to detect bad slots in an enclosure a new element status will be returned by VSES, UNKNOWN (6), when the back-plane signals a device is present and yet the link is not yet up.

EnhancementRequest ID: DCSG00015057
Headline: Queue Depth Change for SAS Drives (fix for SAS SMR TSF performance)
Description Of Change: NVDATA contains the field SASNarrowMaxQueueDepth which is currently set to 0x100 (256). Lower it to a value that does not exceed the queue depth of known SMR drives 0x80 (128) so that they do not return Task Set Full. This is updated in the Ventura & Aero family XSD files.

Note that the SASNarrowMaxQueueDepth field is used for all narrow SAS devices, it is not only for SMR drives. This will lower the max queue depth we will send to all narrow SAS drives.

EnhancementRequest ID: DCSG00015120
Headline: Aero: Update to SECUREBOOT Librrary 2.01.00.00
Description Of Change: This allows firmware to verify hash signatures before the component header is completely written.
Thus a reset at precisely the right time will no longer allow unsigned images to run.

EnhancementRequest ID: DCSG00015603
Headline: Update IOP debug prints to replace %x with an appropriate modifier
Description Of Change: When the print macro that expanded %x prints to %08x prints was turned off, it was found that many IOP debug prints lacked proper formatting. Went through the debug prints and modified prints to have proper formatting when needed.

EnhancementRequest ID: DCSG00016416
Headline: pl: NVMe: fail NVMe init if device requires too much power
Description Of Change: If an NVMe device requires more power than can be supplied by the backplane to which it is attached, fail NVMe init to prevent the device from being used.

EnhancementRequest ID: DCSG00017357
Headline: CSET Port of EnhancementRequest DCSG00017357: Support dynamic BAR changes from host OS without performing a controller reset.
Description Of Change: Original ER did not make the cut-off for CC split between 7.13 and 7.14.
As the result, original ER is now in 7.14. This CSET backports it to 7.13.

EnhancementRequest ID: DCSG00017456
Headline: Add Attention Button for drive removal support for traditional PCIe Hotplug in PCIe switches
Description Of Change: Added Attention Button for drive remove support for traditional PCIe Hotplug from PCIe switches.

This is to enable managed switches to indicate when they need IO to devices to quiesce for manage switch firmware update. Once firmware was updated the Power Indicator for each switch Downstream Port to OFF, then the managed switch will know all IO to those devices are quiesced. If a drive is not quiescing within 1 second, then firmware will issue a secondary bus reset to the drive to force quiescing.

Once all Downstream Ports with IOs are quiesced, the managed switch will be free to perform the operation it needs in regards to IO quiescing.

EnhancementRequest ID: DCSG00018257
Headline: Multi-Chemistry BMU support
Description Of Change: MR FW support for different battery chemistries added.

EnhancementRequest ID: DCSG00018268
Headline: pl: backend PCIe: add ring buffer printing of PL-initiated transaction data
Description Of Change: Added functionality to allow PL-initiated PCIe config space transaction data and memory space transaction data to be logged to the PL ring buffer for debug. It's disabled by default.

EnhancementRequest ID: DCSG00018437
Headline: Ventura/Mercator: backend PCIe: enhance robustness of PCIe port status tracking
Description Of Change: Modified the device side PCIe port status tracking mechanism to improve robustness in the presence of conditions that cause PCIe discovery to run frequently, such as unstable PCIe links.

EnhancementRequest ID: DCSG00018758
Headline: pl: backend PCIe: modify default PCIe device missing delay setting
Description Of Change: The default value of the DMDReportPCIe field in PCIe IO Unit Page 1 is now 8 seconds.

EnhancementRequest ID: DCSG00019322
Headline: Add bitmap support to reduce command block time during 240 auto create R0 and avoid firmware reset
Description Of Change: Implement bitmap model batch R0 creation in auto R0 path. This will make the logical drive creation fast.

EnhancementRequest ID: DCSG00019356
Headline: Single PLDM fw update file that covers all controllers from that series
Description Of Change:
1. Changes in pldm-hdr tool
2. Follow up with SCM people for release-script changes
3. Identify method to be used by ROP to generate single PLDM image
4. Identify the folder/location for single PLDM image
5. Test it - check with the customer if current BMC has the capability

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EnhancementRequest ID: DCSG00019848
Headline: Active State Power Management (ASPM) feature support for backend PCIe links

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Description Of Change: Active State Power Management (ASPM) feature support is added for backed PCIe links.
Feature is disabled for now.

EnhancementRequest ID: DCSG00019927
Headline: Added tests for 2TB and larger Drives and VDs
Description Of Change: This is part1 of two parts

1. Script searches for four 2TB+ drives in the system and saves them in a drive pool for 2TB tests

2. Creates R5 VD that crosses the 2TB boundary for normal Init, IO, Rebuild, tests

3. Creates a 2.1TB R50 VD using small drives, if possible

Currently this test runs longer than desired, so a part2 was created to address run time for BST

EnhancementRequest ID: DCSG00020112
Headline: SnapDump Enhancement : Enable Extended Trace Buffer by default in MR - implementation
Description Of Change: Implemented code changes enabling Cuda's trace buffer manager in extended mode by default in MR.

EnhancementRequest ID: DCSG00020567
Headline: MPI 2.6: Add additional IOC_State (CoreDump) to allow firmware to dump debug logs without being reset by host.
Description Of Change: Allow the FW to collect the debug information (e.g. pl dbg) when a Fault occurs.
Add a new IOC state called CoreDump to inform the driver that the FW is dumping the debug information and avoid the diag-reset.

EnhancementRequest ID: DCSG00020911
Headline: Remove Obsolete Config Pages
Description Of Change: Removed these obsolete config pages from NVDATA XSDs and code:
ManPage4
ManPage18

EnhancementRequest ID: DCSG00020928
Headline: Request for DPMstat support in MegaRAID SAS 3.5 controllers
Description Of Change: Modify code to make DPM stat works for MR 3.5 Controller

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EnhancementRequest ID: DCSG00020978
Headline: Restrict In band /Out of band NVMe PT IO path to only Mgmt cmds
Description Of Change: Only following pass through management commands will be allowed for NVMe drives:
1. NVMe Identify
2. NVMe Get Log Page
3. NVMe MI Send
4. NVMe MI Receive
5. NVMe Get Feature
6. NVMe Set Feature
7. NVMe Change Definition

For all other commands, MR firmware will return error code MFI_STAT_INVALID_CMD (0x01)

MR firmware logic has been changed to restrict NVMe commands to only above set.

EnhancementRequest ID: DCSG00022062
Headline: Handle SATA/NVME DMD
Description Of Change: Scope of this ER is to describe the MegaRAID Design of how Sata and NVME drive removal and insertion done within DMD (Device Missing Delay) is handled in Firmware. Device Missing Delay is a time window where PL does not notify MegaRAID until certain time expires. This is typically a glitch case where drive link goes down and comes back within DMD window.

EnhancementRequest ID: DCSG00022459
Headline: Preserve RMC ring buffer contents if metadata is corrupted
Description Of Change: When corrupt metadata is detected in the SEEPROM, try to establish reasonable head and tail pointers, and display those contents. Only erase the entire SEEPROM when requested via MegaMon, "rmc init"

EnhancementRequest ID: DCSG00022793
Headline: Change all BBU messages to CacheVault for controllers using non-battery solution
Description Of Change: MR code changes are required for changing all event BBU messages and boot time messages BBU messages to Cache Vault messages. These changes will be done under a compile time define #ENERGY_PACK_EVT_STR. MR FW will use internal logic to update these message depending on customer. Following type of message change will be done:
1. Event/Boot Messages that refer to the COL solution - the ONFI/circuit/supercap in total - will use the term "CacheVault". Battery solution uses terms BBU, NVChache.
2. Term "Battery" will be replaced by term "Energy Pack" in Cache Vault solution.

EnhancementRequest ID: DCSG00023086
Headline: IOC FW need to capture Optical Cable's vendor serial number (vendor SN) so driver will be able to read it via MPI spec
Description Of Change: Added Vendor Serial number to the output of the CLI command "pl acm".
This info can be fetched over MPI by using the ToolboxCLI command and reading the output.

EnhancementRequest ID: DCSG00023671
Headline: Added CoreDump collection on IT-FW fault
Description Of Change: When the IT-FW faults:
1. It will collect the out of FW-CLI commands (e.g. "pl dbg", "iop show diag" etc.) to a newly created CoreDump Flash Region.
2. Added a new CoreDump IOC state to inform the driver that IOC is collecting debug data
3. This feature can be disabled via ManPage11

EnhancementRequest ID: DCSG00023737
Headline: pl: backend PCIe: reconfiguration of PCIe address space without adapter reset
Description Of Change: PL now supports some device side PCIe memory address space reconfiguration scenarios without performing an adapter reset.

EnhancementRequest ID: DCSG00023770
Headline: API changes needed for DPMstat support in MegaRAID SAS 3.5 controllers
Description Of Change: API changes needed for DPMstat support in MegaRAID SAS 3.5 controllers. This one is changed based upon POC API change SCGCQ02138624

EnhancementRequest ID: DCSG00024640
Headline: MPI 2.6: Header file changes associated with Revision 2.6.9 of the specification
Description Of Change: Make all necessary header changes to accommodate new proposals and items found during doc review.

EnhancementRequest ID: DCSG00025793

Headline: Aero/Ventura IT: Optimize space by accessing non-IO path data directly from FLASH

Description Of Change: Modified build process and boot code so that two sections of the image may optionally reside in FLASH
1) Some code and constant data
2) Extended images
3) Added checks to properly protect regions of flash from being erased or modified when FW is runnin gout of them.
This saves memory which may be used for other purposes

EnhancementRequest ID: DCSG00026309

Headline: Ventura/Aero: Add Ext. Man Page 48 to store CoreDump options

Description Of Change: 1. Added Ext Man Page 48 to store the CoreDump CLI commands
2. Updated FW to remove the duplicate CFGI files and set the correct include path in the make file

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EnhancementRequest ID: DCSG00026455

Headline: Change Aero default UART speed to 921600

Description Of Change: Update NVDATA XSD, firmware default and bootloader default UART speed to 921600 for Aero.

EnhancementRequest ID: DCSG00027013

Headline: PLDM: Integrate PLDM debug infrastructure with snapdump

Description Of Change: - Integration of PLDM debug infrastructure with Sanpdump
- Implements required debug routines for platform MCTP module that is being used to communicate with PLDM Lib.

EnhancementRequest ID: DCSG00027043

Headline: Defines and Implements debug routines

Description Of Change: Defines and Implements debug routines

EnhancementRequest ID: DCSG00027432

Headline: MS-SES: Enabling translating devices in SES Page 0Ah from managed switch with non-unique BDFs

Description Of Change: Enabling translating devices in SES Page 0Ah from managed switch (Atlas) with non-unique BDFs.

A device listed in the SES NVMe Port Descriptor needs to be matched against an internal device via:
1) BDF
2) Physical Slot Number/Slot

This enables managed switches that manage multiple switches (Atlas's multiple host port feature) to have SES Page 0Ah translate correctly for devices seen across multiple switches, but use one SES.

The major limitation is we cannot have:
1. Multiple physical Atlases
2. With multiple host ports
3. All configured with a single SES/MPI Device

This will be alleviated when there is managed switch/Atlas FW that supports a WWID for each physical Atlas.

EnhancementRequest ID: DCSG00027926

Headline: Integrate MPI 2.6.9 headers into Ventura/Aero code

Description Of Change: Update MPI 2.6 baseline to be the 2.6.9 release and made required code changes.

EnhancementRequest ID: DCSG00029633

Headline: Limit VSES device instances support to max 2

Description Of Change: Note: The changes done in this ER is reversed by DCSG00053379 which reverts the number of VSES devices support to the original implementation.

EnhancementRequest ID: DCSG00029636

Headline: Determine UBM DFC drive type installed based on IFDET# and PRSNT# signals support implemented

Description Of Change: Enhance the identification of DFC drive type installed based on PRSNT#, IFDET# and IFDET2# signals reported in the UBM controller additional capabilities as certain UBM Backplanes designs only support few of them.

EnhancementRequest ID: DCSG00031051

Headline: For new CoreDump feature, set IOC-Capabilities "CoreDump" bit based on ManPage11 value only

Description Of Change: Use only ManPage11 Additional-Flags2 enable-CoreDump field to set the bit in IOC-Capabilities field

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EnhancementRequest ID: DCSG00031340

Headline: PL support for reporting UBM Backplane Number

Description Of Change: Option to report UBM Backplane Number in Enclosure Page 0.

EnhancementRequest ID: DCSG00032147

Headline: Update GetEnclList/GetEnclListExt API behavior to support backplanes and SES devices where the device startslot is other than 0. - PR SCGCQ02198300

Description Of Change: Traditionally, slotOffset is holding the array element index of the first valid entry in SES page 0xA. This is incorrect and does not accurately represent the start slot number if the slot number is something other than 0.

Changes that are done are as follows, and these changes are to address the issue where the start slot is something other than 0.

MR_ENCL_INFO.slotCount = number of array device elements from SES page 01h for SES, number of valid array device elements from SES page 0Ah for VSES
MR_ENCL_INFO.slotOffset = LOWEST slot number assigned to a valid array device element from SES Page 0Ah for VSES
LOWEST slot number assigned to a valid array device element from MR PD LIST for other SES (where slot number comes from SES or MPI)
MR_ENCL_INFO.pdCount = holds number of drives present in the enclosure.
MR_ENCL_INFO.pdIdList array subscript. a simple array , the entries [0..slotCount-1] will be considered valid
The slot number of the first entry in this list is MR_ENCL_INFO.slotOffset
The slot count for a PD in the array is calculated by slotNumber = arraySubscript + MR_ENCL_INFO.slotOffset

This assumes that slot numbers are sequential.

EnhancementRequest ID: DCSG00032992

Headline: ESR Max Threshold check is not required for Aero

Description Of Change: ESR stands for equivalent series resistance.

It was determined by the board group that the current supercap manager is far more accurate in voltage settings and energy available calculations when compared to previous generation, that this ESR check is not required as it will artificially shorten the supercap EOL (end-of-life).

EnhancementRequest ID: DCSG00033543

Headline: Aero/Ventura IT: NVDATA Changes to enable FLASH execution mode

Description Of Change: This disables OCM copy mode and increases resources to the phase 14 specified minimums

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EnhancementRequest ID: DCSG00033552

Headline: Aero: Unmap SPI areas that are virtually mapped to code areas

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Description Of Change: This enhances the original flash-code execution algorithm. It prevents accidental accesses by unmapping SPI flash areas associated with code. It also modifies linker and build options to ensure data is linked to expected locations.

EnhancementRequest ID: DCSG00034259
Headline: Integrate MPI 2.6.10 headers into Ventura/Aero code.
Description Of Change: Update MPI 2.6 baseline to be the 2.6.10 release and made required code changes.

EnhancementRequest ID: DCSG00035135
Headline: Optimizing LIBZ Make
Description Of Change: Added LIBZ objects to the make dependency path so that they are not built every time

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EnhancementRequest ID: DCSG00035455
Headline: Automate version update stage in release process
Description Of Change:
This activity automates version updation stage during release process.

EnhancementRequest ID: DCSG00035457
Headline: Release Automation: Automate state transitions for ReleaseOrder
Description Of Change:
Release script will,
- Verify all activities attached to RO are in closed or equivalent state.
- Verify correct archive files have been checked-in against RO change set.

EnhancementRequest ID: DCSG00035867
Headline: Aero3: Enable XmemCopy Mode
Description Of Change: Choose to execute the entire firmware image from OCM to simplify initial test

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EnhancementRequest ID: DCSG00036523
Headline: MR SBLIB: Update MR to handle SBLIB 2.01.00.00 change
Description Of Change: Update MR to handle SBLIB 2.01.00.00 due to SCGCQ02175169 change.

EnhancementRequest ID: DCSG00036604
Headline: Megamon commands enabled for testing mbedtls library
Description Of Change: Integrated the mbedtls library and add test megamon commands for verification.

EnhancementRequest ID: DCSG00036689
Headline: New Event added when drive unique ID changes.
Description Of Change: User needs to be notified when FW detect a physical drive unique id changes either via DMD path or PD FW update.

EnhancementRequest ID: DCSG00036693
Headline: MR: Single MPI support on Atlas
Description Of Change: Added code to reduce the delay when cables are missing between Aero and Atlas.

EnhancementRequest ID: DCSG00037053
Headline: Aero3: Harden Managed Switch SES (Atlas) SES Page 0Ah translation with error injection framework
Description Of Change: Implementation of error injection framework for managed switch SES.
New command "pl msses test" created to inject errors at different instances and scenarios.

EnhancementRequest ID: DCSG00037325
Headline: Update Version descriptors for standard inquiry data of SATA and vSES devices
Description Of Change: Updated the version descriptors in the standard inquiry data of SATA and vSES devices as per the SPC spec including the SAS-3, SPL-3 and SES-3 version descriptors.

EnhancementRequest ID: DCSG00037855
Headline: SPDM: Test the Library Integration. UT framework in MR Megamon
Description Of Change: The new SPDM library integrated with the FW. enabled few different commands to debug separately some of these commands provided in the SPDM library.

EnhancementRequest ID: DCSG00038937
Headline: API changes for changing all BBU messages to CacheVault.
Description Of Change: API changes are required for changing all event BBU messages to CacheVault. These changes will be done under a compile time flag #ENERGY_PACK_EVT_STR. This flag will be used to define all the Cache Vault event messages for controllers with Cache Vault. All the applications which use eventmsg.h file for their event message must define flag ENERGY_PACK_EVT_STR to get Cache Vault messages. Applications which depend on the event messages sent by FW, do not have to do anything. Applications which use their own message file need to make necessary changes in their message file.
1. Event/Boot Messages that refer to the COL solution - the ONFI/circuit/supercap in total - will use the term "CacheVault". Battery solution uses terms BBU/ NVChache.
2. Messages that refer solely to the SuperCap will use the term "Energy Pack".Term "Battery" will be replaced by term "Energy Pack" in Cache Vault solution.
3. Term "Battery/Memory" will be replaced by term "CacheVault in Cache Vault solution.

EnhancementRequest ID: DCSG00039439
Headline: SPDM: Coding: MR FW MCTP Handler (SPDM Request & Response)
Description Of Change: Spdm Library Client files will be under /fw/spdmlibclient/ directory.
The files under /fw/spdmlibclient/ should implement client responsible routines defined by SPDM library.
This include all the function defined by API SpdmLibClientIFace.h such as SPDMLibClientCompleteReq.
Or buidling SPDM library message to be processed by SPDM library (SPDMLibProcessReq).

For MCTP related routine,
SpdmMctp.c and SpdmMctp.h are used for MCTP traffic related routine.

Implmentation:

Following section describes how client should implement MCTP routines for SPDM library:
1.SPDMLibClientProcessReq: Based on the MCTP packet received, client should check for SOM and EOM bit set. SOM bit indicate the packet is the starting packet for upper layer (either SPDM/PLDM/VDM). Client should check MsgType on the packet with SOM bit set. Allocate enough buffer to hold the SPDM command, right now the buffer is hard coded to 4k. If the packet received is with SOM bit set only, client needs to wait for additional packets to be received before it passes the SPDM request to the library. Client is responsible to keep track the current offset of data payload received on each MCTP packet, and copy the incoming packet to correct offset into the SPDM request buffer. For requests that take more than one MCTP packet, SPDM requestor is responsible to generate correct MCTP sequence number in increment of one (sequence number is from 0-3) in order for the client to build the data correctly. Out of order MCTP sequence number will be dropped at the client side. Only when a packet is received with EOM bit, then the incoming transfer SPDM request is complete. Then, the client builds the SPDM_REQUEST from client context and call SPDM library through SPDMLibClientProcessReq to process SPDM traffic.

2.SPDMLibClientCompleteReq: Client should implement this routine for SPDM library to send the response back to requestor. Client first will copy the response into local buffer from SPDM response pSPDMResMsg with SPDMMsgSz size. In additional, client generates MsgType field, MCTP header field, and PCI header field based on each SPDM response payload length in one MCTP packet. The client may split the response into multiple MCTP packet if the response is larger than a single MCTP payload (64 byte) and send SPDM response back to requester one by one. For multiple MCTP packets response, correct SOM/EOM bit and MCTP sequence number need to be generated by the client routine. This is to ensure SPDM requester knows how to read and build the complete SPDM response.

Test:
For compile to test, place all SPDM library .c .h file under /fw/spdmlibclient for easy compile to test.

Test with emulator python module to generate SPDM GET_VERSION, GET_CAP, NEGO_ALGORIGHTM.
Make sure emulator get correct response back.

GET_VERSION/GET_CAP/NEGO_ALGO is basic SPDM request/response. It only involves one 64byte MCTP packet for request and response. More complicated tests needs to be done when traffic is of larger size such as GET_CERTIFICATE, CHALLENGE.

EnhancementRequest ID: DCSG00039443
Headline: SPDM: Coding: Implement SPDM Commands (SPDM Lib Shell & Client of SPDM Lib)
Description Of Change: SPDM Commands (SPDM Shell): Get Cap, Get Ver, Neg Algo are implemented in the SPDM Lib. SCM team and Stephen have put it in ClearCase fwlibs repository.

Implemented client code in MegaRAID FW as client to SPDM Lib to allow SPDM Lib to handle additional SPDM cmds: Get Certificate, Get Digest, Challenge.
The Client Debug Print function is also implemented in MR Firmware to allow SPDM Lib to log messages to UART or serial port console for debugging.

Implemented MegaMon command to test out the main sign data functions in SPDM Lib and SPDM client code.

EnhancementRequest ID: DCSG00039844
Headline: Platform related configuration changes updation
Description Of Change: Configuration file change according to the platform usage modifications done.

EnhancementRequest ID: DCSG00040165
Headline: API change to support 1. OEM specific UBM Back planes, and 2. Smart Battery state
Description Of Change: Added

```
MR_ENCL_SUBTYPE_DU2BB = 8,        // OEM specific enclosure sub-type
MR_ENCL_SUBTYPE_DU3BB = 9,        // OEM specific enclosure sub-type
```

Updated
MR_BBU_STATUS_BAD_FOR_SMARTBATTERY to 0x0008060B

EnhancementRequest ID: DCSG00040462
Headline: Reserve frames for backend PCIe activities
Description Of Change: - Added code to reserve a set of frames for backend PCIe activities and implemented new APIs to alloc/free frames from this pool

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EnhancementRequest ID: DCSG00041624
Headline: Aero-3: Add debug prints to display SerDes Tx parameters
Description Of Change: Add code to break up the TxCM1CP1CO field into bits so it's easier to compare NVDATA settings to the format giving by the analog team.

EnhancementRequest ID: DCSG00042002
Headline: Add MR Register access to PDB0b, PDB1b and CCR Subset
Description Of Change: Added Following register access that are additionally requested.

```
0000_0000_FC80_0000    0000_0000_FCBF_FFFF    4 MB    PDB0b Registers    Read/Write
0000_0000_FCC0_0000    0000_0000_FCFF_FFFF    4 MB    PDB1b Registers    Read/Write
0000_0000_FFE1_4080    0000_0000_FFE1_40BC    60(0x3C) CCR: SW MXS (SubSet))
```

EnhancementRequest ID: DCSG00042561
Headline: OEM Stream Merge to Channel stream
Description Of Change: OEM Stream Merge to Channel stream

EnhancementRequest ID: DCSG00042985
Headline: Update MR API mr_drv.h to modify field for RTTRace_header
Description Of Change: Converted PortName Field in RTTRACE Header to Single U16 PortNumber. PortNumber will be a Unique Number generated fromStorPortGetSystemPortNumber. This will help us to differentiate adapters based on PortNumber which will be unique for each adapter. Converted the unused space to reserved so that it can used for Future use.

EnhancementRequest ID: DCSG00043318
Headline: Scons build tool modification to append multi NVDATA binary
Description Of Change: Need to modify the CreateCbbRomBld in AvngBinTools to append an NVDATA extended image header for a multi NVDATA binary

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EnhancementRequest ID: DCSG00043884
Headline: Enhance medium error test cases : please refer to CLCA for defect SCGCQ01996272
Description Of Change: Enhance medium error handling
Description: IO complete without error
This is to enhance medium error test cases for CLCA defect for SCGCQ01996272: When there are drives with medium error, and IO is sent to medium error LBA range. FW enters medium error handling path for that LDBBM entries are created.
When once again IO is sent to same LBA range with LDBBM entry, in one of the immediate read IO path the IO is not completed back to the host, which cause kill adapter
So this test case is to issue two rounds of read to make sure we handle the IO path that read comes to the LBA when ldbbm exist

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EnhancementRequest ID: DCSG00044714
Headline: updated BST script to run the 2TB+ drive tests in 90-100 minutes (previously would have taken hours)
Description Of Change: run 2TB+ R50 VD in a new step (and limit LBA range to the upper fastinit region)

EnhancementRequest ID: DCSG00045139
Headline: Automate Build Job and Release Job Submission Process
Description Of Change: This ER will:
1. Open CM Portal
2. Submit Build Job for IT Firmware and MR PL Lib
3. Validate Build Job completion
4. Initiate Release Job and fill in Release details.
5. Submit Release Job and validate release job completion.

EnhancementRequest ID: DCSG00045448
Headline: Resolving the compilation conflicts while integrating the library with FW
Description Of Change: Found few redefinition of type variables and needs to be modified to compile it properly.

EnhancementRequest ID: DCSG00045470
Headline: Resolving the compilation conflicts while integrating the library with FW
Description Of Change: Found few redefinition of type variables and needs to be modified to compile it properly.

EnhancementRequest ID: DCSG00045604
Headline: Provide Configurability For SPDM Library
Description Of Change: Added a separate header file to provide configurability for the library.

EnhancementRequest ID: DCSG00047716
Headline: Config file changes to including prints
Description Of Change: Config file changed to include the prints enable.

EnhancementRequest ID: DCSG00047741
Headline: Correcting the print function configuration
Description Of Change: Debug functions with prints redirecting to the firmware defined prints.

EnhancementRequest ID: DCSG00048463
Headline: PLDM - Calculate PLDM package header checksum as per DSP0267_1.0.1 specification
Description Of Change: PLDM package header checksum was calculated wrongly which was causing PLDM Type 5 firmware update failure due to CRC error at OEM end.

Calculate the PLDM package header checksum as mentioned in DSP0267_1.0.1 specification.

"For this specification, CRC-32 algorithm with the polynomial x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1 (same as the one used by IEEE 802.3) shall be used for the integrity checksum computation. The CRC computation involves processing a byte at a time with the least significant bit first."

EnhancementRequest ID: DCSG00048670
Headline: Aero multi-party signing partial signing of images
Description Of Change: Added support to secureSign.exe, HSM server controller scripts, CQ schema and PHP WebSvc scripts to support partial signing of an image with a customer publickey. Added new CLI argument '-partialSignCustKey' to secureSign.exe to enable this behavior along with new field "customerPublicKey" and form control in CQ schema to define the customer publickey.

EnhancementRequest ID: DCSG00050115
Headline: FW should reflect PD cache setting changes on EPD
Description Of Change: Firmware need additional code changes to make Cache Setting flags updated when an EPD cache setting is changed by an application.

MegaRAID Firmware is process EPD MODE_SELECT_6 (0x15) command through DCDB path. When a MODE_SELECT_6 (0x15) command is completed for an EPD device through DCDB path firmware will start a task to check if cache setting is changed. If any changes were detected then firmware will read new cache settings from the drive and update its data structures.

Any drive cache setting changes within the firmware is done in a command blocked environment. So this new task also will be executed after command blocked. Command block will be released after completion of the task.

In order to keep the implementation simple, current cache setting sync functions when an EPD created will be mostly used and code repetition will be avoided

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EnhancementRequest ID: DCSG00050640
Headline: pl: backend PCIe: PCIe Hinting
Description Of Change: Added a feature similar to SATA Hinting for use with device side PCIe devices and switches.

EnhancementRequest ID: DCSG00051200
Headline: Add support for C++/CPP compile for libspdm
Description Of Change: Add support for C++/CPP compile for libspdm

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EnhancementRequest ID: DCSG00051225
Headline: Atlas drives connected to an OEM controller behind Atlas PCI switch SMART polling 10s interval
Description Of Change: For a specific OEM set the smart polling value to 10s for all the drives behind Atlas switches.

EnhancementRequest ID: DCSG00051246
Headline: OOB diagnostic Test Improvments
Description Of Change: 1. Currently if we run OOB from the inband and also initiate a diagnostic from Out of band there can be case where the second command can never get the command block. Design has been added to fail the second diagnostic command if the first one is outstanding and return a error status. Diagnostic command in general, block all commands until they are complete. A flag has been added that becomes true as soon as the in-band diagnostic is in progress. This fails if there is any incoming OOB diagnostic command that is initiated. The global flag is then cleared after the inband diagnostic command is completed.

2. DMA test skipped but reported to the applications for OOB : For oob test events are now skipped for both pass and fail for DMA test.

3. 180 seconds change in the APP - FW added a maximum diagnostic command time of 180 internally and fails the command with invalid status. The Mr.h is updated to reflected the mbox time in seconds to make it clear for the user on maximum diagnostic time.

EnhancementRequest ID: DCSG00051277
Headline: MPI changes to configure backend ASPM
Description Of Change: MPI changes to configure backend ASPM in PCIe IO unit page 0 , PCIe IO unit Page 1 , PCIE device page 0 and PCIe switch page 1.

EnhancementRequest ID: DCSG00051715
Headline: SPDM: Enable SPDM LIB support by default & improve the check for buffer size of ECDSA signature buffer which contains integer R and S in der format
Description Of Change: - Enable compiler flag F_SPDM_LIB_SUPPORT to enable SPDM LIB code and MR Client code by default.
- Improve the check for buffer size of ECDSA signature buffer which contains R and S in der format in SPDM client code.

EnhancementRequest ID: DCSG00051793
Headline: Cache bypass tuning on Aero
Description Of Change: Tune cache bypass for Aero for performance optimization.

EnhancementRequest ID: DCSG00051824
Headline: Improve cable breaker mechanism for PERC bst
Description Of Change: Included quarch system related commands directly in the script rather than using extra module.

EnhancementRequest ID: DCSG00053828
Headline: Added "pl serdes tx" and "pl serdes rx" command
Description Of Change: Added the options to dump the TX and RX Serdes parameters for Ventura and Aero.

EnhancementRequest ID: DCSG00054194
Headline: API change OOB Self Diagnostics Design Improvements
Description Of Change: MaxDiagTime Change will require the following changes:
- FW change in progress to fail the command if > maxDiagTime.
- MR API and SL API comment change required for maxDiagTime so users have the visibility to see the maximum Diagnostic time limit.
- First thing to deliver the Mr.h file to Suma. Suma to take the baseline and update the SL API.

EnhancementRequest ID: DCSG00054211

Headline: Serial mode support for S25FL512S SPI flash part

Description Of Change: Added support for serial mode operation for spi flash S25FL512S part.
Due to conflict on command code usage, now nvsram and spi flash use separate array for command properties.

EnhancementRequest ID: DCSG00054553

Headline: Python SPDM scripts for Get_Version,Get_Capability, Nego_Algo, Get_Certificate, Get_Digest, Challenge

Description Of Change: Check in include all python files needed for Get_Version,Get_Capability, Nego_Algo, and
advance SPDM command: Get_Certificate, Get_Digest, Challenge to work in emulator environment.

Document wise, please check attached AeroSPDMDesignNote-v0.7.
Section 21 UNIT TEST BMC EMULATOR &PYTHON SCRIPTSUPPORT

For steps on how to use SPDM python scripts, check StepsToRun.txt

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EnhancementRequest ID: DCSG00054557

Headline: MbedTLS: Explicitly make enumerator value of enum type to 4-byte value

Description Of Change: Added last enumerator and set it to 4-byte integer value in MbedTLS enum type mbedtls_ecp_group_id to explicitly
make each enumerator a 4-byte value (Note: MbedTLS already treats enumerator as a 4-byte value by default).
This way, any consumer or client code base integrates MbedTLS Lib and uses this enum type mbedtls_ecp_group_id
will treat its enumerator as a 4-byte value.

EnhancementRequest ID: DCSG00054920

Headline: Tool to help managing ROP package_type

Description Of Change: Tools to used to managing creation of Ventura package type, that distributes ROPs in different custom firmware packages.

EnhancementRequest ID: DCSG00054950

Headline: NVMe Drive Repair command processing

Description Of Change: Added code to process drive repair commands from the host

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EnhancementRequest ID: DCSG00054970

Headline: NVMe Drive Init failure Error Reporting.

Description Of Change: 1) On insertion of NVME drive with namespace issue or format issue, maintain a internal list of failure.
2) Provide above failure data to applications through DCMD..

EnhancementRequest ID: DCSG00054971

Headline: Preboot Trace Buffer [PTB] for Ventura/Aero - MR Firmware

Description Of Change: Add support for the Preboot Trace Buffer. This feature allows prints from UEFI/HII code running on the host to be included in a Snapdump.

EnhancementRequest ID: DCSG00055071

Headline: Release Automation: Validate FW Header post Package Creation

Description Of Change: This ER will:
1. Download the package created post successful run of Release Job.
2. Unzip the FW files from the package.
3. Validate the FW headers to check if it is updated with the correct Release Version.

EnhancementRequest ID: DCSG00055387

Headline: pl: NVMe: update Block Limits VPD page translation

Description Of Change: Made a couple of minor edits to the Block Limits VPD page translation. There should be no externally visible changes.

EnhancementRequest ID: DCSG00055420

Headline: Tools to help analyze NVDATA ROP

Description Of Change: This tool will
1. renames the full and partial xml files of a Ventura NVDATA ROP from CQ_ID.xml to PnP_ID.xml
2. if full xml does not exists = partial NVDATA failed to build, do not rename, thus the remaining partial xml with CQ_ID.xml name are "failed-to-build" ones.

Since PnP_ID is persistent, user can compare NVDATA ROP of different releases by the top-level folder name.

The workflow is
Unzip MR_FW_SAS3.5_7.0_NVDATA_Pkg-5.1200.00-0013-DCSG00048296
Unzip MR_FW_SAS3.5_7.0_NVDATA_Pkg--DCSG00019689
CQ2PnP.py FW_SAS3.5_7.0_NVDATA_Pkg-5.1200.00-0013-DCSG0004829
CQ2PnP.py MR_FW_SAS3.5_7.0_NVDATA_Pkg--DCSG00019689
Wnmerge or beyond compare the two folders.

This tool can be EOL'd when NVDATA ROP are built with PnPID name or when partial NVDATA.xml are in Clear Case.

EnhancementRequest ID: DCSG00055427

Headline: Adding Events Handling for NVMe Drive Init Error reporting/Repair

Description Of Change: Add event handling for NVMe Drive Init errors and repair. Log events at different points of reporting and repairs.

EnhancementRequest ID: DCSG00055563

Headline: PL: NVMe Drive Repair

Description Of Change: Implemented the NVMe repair/recovery feature in PL, which can be used to fix certain conditions that cause PL NVMe init to fail, making the drive inaccessible from upper layers. The
feature is accessed via an MPI toolbox request sent through the PLI interface.

The conditions this feature is intended to recover:
- No namespaces exist
- Namespace 1 not present or not attached
- Namespace is formatted with EEDP or non-zero metadata size, or an unsupported sector size.

Commands implemented for the toolbox request:
- Start recovery on DevHandle.
- Check if recovery is in progress on DevHandle.
- Abort recovery in progress on Devhandle.

EnhancementRequest ID: DCSG00055566

Headline: NVMe Drive Init failure Error Reporting

Description Of Change: 1.Permanent Failure Reason code will be published as part of new field in PCIe Device Page 0.
2.FW will publish if the error is recoverable or not as part of new field in PCIe Device Page 0.
3.If the error is recoverable, FW will publish what recovery method needs to be used as part of new field in PCIe Device Page 0.
4.Added new Toolbox tool framework to:
a) Initiate Recovery of NVMe drive which failed initialization.
b) Get the status of the Ongoing drive recovery.
c) Abort an ongoing recovery.
5.Enhanced FW handling of NVMe drive initialization by adding check for PCIe address space allocation before starting NVMe Init state machine.

EnhancementRequest ID: DCSG00055878

Headline: Additional FDE type for Ruby SED support

Description Of Change: Add FDE type for Ruby SED support

EnhancementRequest ID: DCSG00056703
Headline: Reduce rebuild delay for SSDs
Description Of Change: A rebuild delay 100 milliseconds, depending on rebuild rate and the number of host commands issued, is too long for SSDs. Modified the rebuild delay to 100 microseconds instead of 100 milliseconds.

EnhancementRequest ID: DCSG00056834
Headline: Providing Link and Device Related Counters
Description Of Change: Added below pages:
1. Extended SAS Device Page 250
2. Extended Expander Page 250
3. Extended PCIe Device Page 250
4. Extended PCIe Switch Page 250

Below counters were added to the above pages:
1. Phy Change count
2. Link Rate Change Count
3. TM Count

EnhancementRequest ID: DCSG00058083
Headline: OEM ROMB design support
Description Of Change: Add custom board design support

EnhancementRequest ID: DCSG00058089
Headline: Modify board support package for custom boards
Description Of Change: Modify board support package for custom boards

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EnhancementRequest ID: DCSG00058148
Headline: Do not update timeout value for a DCDB issued by host on JBOD.
Description Of Change: For system PDs, timeout value for DCDBs is limited to 90 seconds, if the application specifies time out value more than 90 seconds. This limitation is removed in the code for MR controllers. And if the command block is pending for more than 35 seconds, DCDB commands are aborted and failed back to application.

EnhancementRequest ID: DCSG00058202
Headline: Modify package options for custom distribution of fir,ware binary
Description Of Change: Modify package options for custom distribution of fir,ware binary

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EnhancementRequest ID: DCSG00058537
Headline: Aero/Ventura: Enable easier debug when SPI FLASH is bad
Description Of Change: Added in misc places to check for flash before reading it
Ported iop spiflash init function to SPILIB2 so users could get a ring buffer on failure

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EnhancementRequest ID: DCSG00059001
Headline: Shrink MbedTLS library size
Description Of Change: This ER starts with basic MbedTLS files client (MR) needed to for signing certificate, generating hash from buffer.
Base on those file, try to add more MbedTLS files to still have the code compile.
This reduce redundant files needed for MbedTLS. Thus, reduce release library size for MbedTLS.

Files started with pk.c, pkparse.c, sha256.c, ecdsa.c (these are 1st layer of file MR need from Spdm.c) and keep adding file when seeing undefined symbol.
Following is the best achievable size without changing content of MbedTLS file.
make libmbedtls --release result in 395KB (previously was 757KB).

EnhancementRequest ID: DCSG00060323
Headline: SPDM library: Adding PLDM print module style.
Description Of Change: This ER covers the change to have SPDM print to work like PLDM print module.
Such that, SpdmDebug.c SpdmDebug.h is generated by python script when building.
And client (MR) will get input based on printIndex to indicate which string client project will print with additional arguments.

The changes will be from SPDM library and Client Code changes.
This ER covers the change for SPDM library.

EnhancementRequest ID: DCSG00060325
Headline: SPDM Client Code Change: Adding PLDM print module style
Description Of Change: This ER covers the change to have SPDM print module to work like PLDM.
Such that, SpdmDebug.c SpdmDebug.h is generated by python script when building.
And client (MR) will get input based on printIndex to indicate which string client project is printing along with additional arguments.

The changes will be from SPDM library and Client Code changes.
This ER covers the change for SPDM client code (MR).

EnhancementRequest ID: DCSG00060350
Headline: Coverity improvements
Description Of Change: A build target was added to our Scons file so that developers can easily run Coverity tests before checking in changes.

EnhancementRequest ID: DCSG00060384
Headline: MbedTLS Lib: disable file system related functions & enable memory allocation and prints functions to be compiled in CPP environment
Description Of Change: There are file system related calls (fopen, fclose, sys_io, fseek, etc.) in MbedTLS Lib which are not used in MR and IT Firmware, disable file system related calls in MbedTLS Lib.

This change also saves about 5 Kbytes of code space.

EnhancementRequest ID: DCSG00060636
Headline: Add official support for New Winbond and Macroix Flash chips and block downgrade to older firmware versions
Description Of Change: The following changes are added:

1) add environment variable to stamp official support for Macronix and New Winbond Flash Chip
2) Block downgrade to older firmware versions on these flash chips
3) Maintain downgrade support to previous version on Winbond chips.

EnhancementRequest ID: DCSG00060670
Headline: Add support for TCG Enterprise SED drives that require Packet.SessionNumber to be zero for Open, Close, Config, Sync
Description Of Change: update Packet.SessionNumber to be zero in the cases specified by the TCG Enterprise spec starting with Version 1.00 Revision 2.00 and later. Some drives claining TCG Enterprise 1.01 support do not even enforce this requirement.

EnhancementRequest ID: DCSG00060688
Headline: pl: backend PCIe: examine BAR attributes following endpoint/switch reset
Description Of Change: When rediscovering a backend PCIe topology, PL now compares the current size and attributes of BARs of components that are found to be unconfigured against those that were determined during the previous discovery.

EnhancementRequest ID: DCSG00060713
Headline: Preboot Trace Buffer [PTB] for Ventura/Aero - MR API
Description Of Change: Defines a new DCMD for the implementation of the Preboot Trace Buffer. This DCMD can be used to:
* Register the location of trace buffer with firmware.
* Inform firmware that tracing into the buffer has completed.

EnhancementRequest ID: DCSG00060737
Headline: SPDM: Implementation: Implement CDI generation and ECDSA Key Pair generation
Description Of Change: 1) Generate CDI:
CDI = HMAC(SRK, 16-byte mfg data || security setting || advanced security setting)
Generate HMAC data: 16-byte mfg data, security setting and advanced security setting.
Use ApSha hardware and input HMAC data and specify to use SRK to compute CDI.

2) Call Mbed TLS functions and input CDI value to generate ECDSA key pair.

EnhancementRequest ID: DCSG00060758
Headline: Check-in generate HBICList script
Description Of Change: Check in the support for generating HBICList from FW RO.

EnhancementRequest ID: DCSG00061091
Headline: No Longer Close Flash for Error Cases
Description Of Change: With the current design, if the firmware flash was unsuccessful, firmware returns a MFI status indicating the error and closes the flash. However applications try to close the flash again, and this fails because flash is no longer opened. Updated firmware to check that the flash return code is OK before closing the flash.

EnhancementRequest ID: DCSG00061410
Headline: Check in HwBoardImageConfig's partial xml files into Clear Case
Description Of Change: Check in HwBoardImageConfig's partial xml files into Clear Case

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EnhancementRequest ID: DCSG00063680
Headline: XSD and NVDATA changes to support SPDM manufacturing and Security pages
Description Of Change: Added extended manufacturing page 49, 50 and 51 in XSD
Added new extended page type Security and defined security page 0 and 1 in XSD.
Added related MPI structures and definitions.

All these pages have information related to SPDM.
MFg Page 49 indicates the attestation policy to the firmware
MFg Page 50 indicates the the supported algorithms to the firmware
MFg Page 51 indicates the supported measurement algorithms to the firmware.
Security page 0 is used to store the certificates.
Security page 1 is used to store the encrption keys.

EnhancementRequest ID: DCSG00063687
Headline: MbedTLS lib integration with IT FW
Description Of Change: MbedTLS lib integration with IT FW

EnhancementRequest ID: DCSG00063688
Headline: Added SPDM lib to IT FW code base and handle MCTP VDM SPDM commands
Description Of Change: 1.Include SPDM .a file which is compiled in CPP.
2. Add required header files.
3. IT FW code changes to handle SPDM commands which are coming from BMC and pass to SPDM lib.
4. SPDM lib interface functions (including print).

EnhancementRequest ID: DCSG00063690
Headline: CDI & Key Generation source integration with IT FW
Description Of Change: Added CDI ,HMAC, Nonce & Key Generation API's

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EnhancementRequest ID: DCSG00063691
Headline: [Aero IT SPDM] Attestation policy at the boot-up time.
Description Of Change: 1) Check if the certificate & key are in proper state and update Spdm status flags accordingly.
2) Based on the spdm flags, platform(IOP) should take respective action of either blocking or unblocking inband/outband request.

EnhancementRequest ID: DCSG00063692
Headline: [Aero] [SPDM] Support Export Certificate Signing Request command
Description Of Change: 1) Integrate platform with Mbed TLS library and generate CSR.
2) Fill CSR required data for Export command
3) Integrate the tool box with CSR interface.

EnhancementRequest ID: DCSG00063755
Headline: Aero+Cub Multi-path improvements
Description Of Change: Multi ported drives discovered with same SAS address configuration is supported. Filtered our the error messages and critical event logs and firmware error logs. Also load balancing module modified to distribute the devices connected between SAS core connection port instead of path it connected logic.

EnhancementRequest ID: DCSG00063756
Headline: Multi-path/Multi-port message filtering
Description Of Change: Multi-path/Multi-port message filtering. That covers code implementation and development testing.

EnhancementRequest ID: DCSG00065857
Headline: Implement to change i2c messages to etty
Description Of Change: Implement to change i2c messages to etty. Move all OOB_debug prints to etty of i2cOOBMgmt.c for MR.

EnhancementRequest ID: DCSG00065881
Headline: API change to support ISE completion status
Description Of Change: Added MR_PD_PROGRESS.previous.operation.erase and MR_PD_PROGRESS.previous.status in order to populate the completion status of ISE operation for particular application.

EnhancementRequest ID: DCSG00066113
Headline: Add support for custom design
Description Of Change: Change NVDATA to support custom design.

EnhancementRequest ID: DCSG00066845
Headline: Release Automation: create Aero IT FW only Release Order Package
Description Of Change:
Release scripts will create a new Release order package and include it's component Release orders and Board configurations.

EnhancementRequest ID: DCSG00066920
Headline: Aero SAS Performance Enhancement on AMD Rome
Description Of Change: Set IOC_CFG_MFG_PG11_ADDLFLAGS_PCIE_RELAXED_ORDERING in ManPage11 of NVDATA.

EnhancementRequest ID: DCSG00066934
Headline: Add dev test suite directory and scripts.
Description Of Change: Implemented Dev BST Suite and also added scripts for some ERs

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EnhancementRequest ID: DCSG00067411
Headline: MBEDTLS LIB: Implementation: Use CDI to generate ECDSA key pair
Description Of Change: Add functions in Mbed TLS LIB to get CDI value from MR Firmware and enable other functions to use CDI to generate ECDSA key pair.

EnhancementRequest ID: DCSG00068355
Headline: MR API changes - Support new DCMD for Platform Security SPDM
Description Of Change: Added the following DCMD commands to the API
1. Added MR_DCMD_CTRL_PSEC_EXPORT_CSR
2. Added MR_DCMD_CTRL_PSEC_IMPORT_CER
3. Added MR_DCMD_CTRL_PSEC_SLOT_MGMT

EnhancementRequest ID: DCSG00068675
Headline: MBEDTLS LIB: Rename sha256.h header file to avoid conflict with MR FW sha256.h header file
Description Of Change: Mbed TLS Lib uses its own SHA256 implementation and includes header file sha256.h in source code. MR FW uses its own SHA256 implementation and includes header file mrsha256.h (originally, MR FW used sha256.h but this file was renamed to mrsha256.h). IT FW uses its own SHA256 implementation and includes header file sha256.h.

When we build Aero FW for MR, there is no conflict as expected.

Since IT FW uses sha256.h so when IT FW team build Aero FW for IT with Mbed TLS, the build fails due to sha256.h conflict.

Per discussion with IT FW team and Architecture team, we decided to rename sha256.h in Mbed TLS Lib to something like mbedtlssha256.h, this way we can tell different sha256.h from various platforms.

EnhancementRequest ID: DCSG00068680
Headline: SPILIB2: Add support for Macronix MX25U25691G part
Description Of Change: This enhancement adds new internal features which allow for commands to have 0, 8 or 24 bits of dummy cycle/ MX25U25691G requires the addition of a new 0xEC command which has 24 bits of dummy cycles.

EnhancementRequest ID: DCSG00068681
Headline: SPDM: Implementation: Rename sha256.h header file to avoid conflict with MR FW sha256.h header file
Description Of Change: Mbed TLS Lib uses its own SHA256 implementation and includes header file sha256.h in source code. MR FW uses its own SHA256 implementation and includes header file mrsha256.h (originally, MR FW used sha256.h but this file was renamed to mrsha256.h). IT FW uses its own SHA256 implementation and includes header file sha256.h.

When we build Aero FW for MR, there is no conflict as expected.

Since IT FW uses sha256.h so when IT FW team build Aero FW for IT with Mbed TLS, the build fails due to sha256.h conflict.

Per discussion with IT FW team and Architecture team, we decided to rename sha256.h in Mbed TLS Lib to something like mbedtlssha256.h, this way we can tell different sha256.h from various platforms.

EnhancementRequest ID: DCSG00069168
Headline: SPDM: Implementation: Implement Subject Name validation for CSR (Certfificate Signing Request) and CSR generation
Description Of Change: Implement functions to take in subject distinguished name string with its length, and CSR buffer and its length for CSR construction, validate parameters and construct CSR in DER format, sign CSR, and return CSR with actual length.

EnhancementRequest ID: DCSG00069245
Headline: PL logic to create VSES instances per Backplane number
Description Of Change: Modified the VSES creation logic by grouping the FRUs attached to UBM backplanes with same BP type or FRUs on a backplane with same backplane number.

EnhancementRequest ID: DCSG00069942
Headline: MBEDTLS: Implementation: Implement Subject Name validation for CSR (Certfificate Signing Request) and CSR generation
Description Of Change: Implement functions to take in subject distinguished name string with its length, and CSR buffer and its length for CSR construction, validate parameters and construct CSR in DER format, sign CSR, and return CSR with actual length.

EnhancementRequest ID: DCSG00069955
Headline: Updated BST scripts for latest controller
Description Of Change: Updated scripts and modified scripts to suit the latest controller type.

EnhancementRequest ID: DCSG00069982
Headline: Add SasSerdesCtl0_7 registers to pl serdes
Description Of Change: For debug of an issue, HW has asked for a dump of SasSerdesCtl0_7, but they are not part of pl serdes. Add them so they are there in the future.

EnhancementRequest ID: DCSG00070917
Headline: Ventura/Aero: Update SPI flash test to print better failure information
Description Of Change: Updated the output so that the offset and data of the error are printed

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EnhancementRequest ID: DCSG00071066
Headline: Define MR_SAS_PHY_CONNECTION.currentSpeed when no devices are connected
Description Of Change: Added a new value to the MR_SAS_PHY_CONNECTION enum to indicate an unknown speed.

EnhancementRequest ID: DCSG00071534
Headline: MR API: NVME Drive Init Error Report and Repair for Aero/Ventura
Description Of Change: MR API changes for handling NVME Drive Init Error Report and Repair for Aero/Ventura
1. Added two DCMDs to get init error and start repair commands.
2. Added new events for NVME init error reporting and repair
3. Added new MFI status codes for NVME init error reporting and repair

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EnhancementRequest ID: DCSG00071626
Headline: PL: Support Managed Switch (Atlas) slot range VSEC command for its single MPT mode
Description Of Change: Support the Managed Switch (Atlas) slot range VSEC (Vendor Specific Extension Capability) command for Atlas's single MPT mode.

This enables PL to properly setup the slot information of an enclosure of managed switch without having all of the upstream ports of the Atlas connected. This is done by getting the slot range data via a VSEC register set from an upstream bridge of the managed switch. Any upstream bridge on an Atlas upstream port will provide the same data.

This is only important for Atlas's single MPT mode because it needs one enclosure across switches in the Atlas. Without this mode, PL is able to collect the data on a per-switch basis within a physical Atlas.

EnhancementRequest ID: DCSG00071652
Headline: pl: NVMe: handle Namespace Not Ready error during NVMe init
Description Of Change: If an NVMe device throws a Namespace Not Ready error while the device is being initialized, handle it by retrying the failed command.

EnhancementRequest ID: DCSG00072397
Headline: Populate currentSpeed for SAS Phys
Description Of Change: Added code to populate currentSpeed for SAS Phys

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EnhancementRequest ID: DCSG00072481
Headline: MBEDTLS LIB: Implement version scheme
Description Of Change: Implement version scheme in MBED TLS LIB will include:
- Define version number, version string
- Implement functions to return version number and version string

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EnhancementRequest ID: DCSG00072483
Headline: SPDM LIB: Implement version scheme
Description Of Change: Implement version scheme in SPDM LIB will include:
- Define version number, version string
- Implement functions to return version number and version string

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EnhancementRequest ID: DCSG00072590
Headline: UpdateVersion tool to change and update version information in ClearCase
Description Of Change: Added utility to perform version updates based on config file. Log output will be available to know the progress made. Supports a debug mode that will give more detailed log on user provided data and further details from server.

EnhancementRequest ID: DCSG00072780
Headline: Include new field cannotSetMode in MR_AUTO_CFG_PARAMETER structure.
Description Of Change: In order to resolve backward compatibility issue, solution is to introduce a new bit cannotSetMode to the existing MR_AUTO_CFG_PARAMETER structure. This would represent an action to indicate applications that the AutoConfig R0 feature cannot be set.

EnhancementRequest ID: DCSG00074400
Headline: pl: SATA: vendor specific ATA Standby handling
Description Of Change: Modified the Test Unit Ready SCSI command translation so that it returns Good SCSI status when a SATA device is in the ATA Standby_y state.

This behavior is disabled by default. It can be enabled by setting bit 12 of the AddlFlags2 field in Manufacturing Page 11.

EnhancementRequest ID: DCSG00075028
Headline: SPDM: Implement Cert HMAC, Cert Key, Key HMAC, KEK, Nonce, AES decryption/encryption of key storage
Description Of Change: Implement functions to:
- Generate MAC key, and MAC for Cert Config Page
- Generate MAC key, MAC, KEK for Key Config Page
- Encrypt and decrypt Key Config Page

EnhancementRequest ID: DCSG00075871
Headline: pl: NVMe: handle Namespace Not Ready error during NVMe init (part 2)
Description Of Change: Send a Read command to LBA 0 at the end of NVMe init to ensure that the namespace is ready before allowing NVMe init to complete.

EnhancementRequest ID: DCSG00076512
Headline: [Aero][SPDM] IOP framework to support CFGI Reads and Writes
Description Of Change: 1) New MPB2 region is introduced as part of MPB now.
2) IOP to redirect read and writes of certificates to MPB 2.
3) Support the new toolbox command to write the certificates and key to MPB2.

EnhancementRequest ID: DCSG00077215
Headline: Signing Linux executables via GPG method in HSM
Description Of Change: With this implementation, Linux executables can be signed using GPG way of signing in HSM.

We have created client secureSignGPG tool which would accept public key id and filename to be signed and signs the executables and downloads the signed executable, signature file,and public key.

EnhancementRequest ID: DCSG00077909
Headline: Add NVMe drive init failure condition tracking list
Description Of Change: Implement the tracking list for NVMe Init failed drives, which store Init errors and repair status.

EnhancementRequest ID: DCSG00077941
Headline: Add Aero/Sea Info to Ventura Summary Release Notes
Description Of Change: In the past, we created a separate summary release notes document for Aero/Sea. Now that they are all GCAing together, add all the Aero/Sea info to the Ventura document.

EnhancementRequest ID: DCSG00077966
Headline: CFGI Integration for MR
Description Of Change: 1. Integrate new CFGI for MR (integrate MPB2 read/write into MR's MPB implementation dm_cfg_mpb xx layer).
2. Provide interface for Security Page0/1 read/write, some of this may falls into either config region or MPB2 region.
3. Provide access to read ExtManPage 49/50/51 for SPDM policy related attributes.

Testing Scenario:
1. Verify Write to Security Page 0 slot 2-7, reboot, able to read back Security Page 0 slot 2-7 data. (Verify Config Region is working correctly).
2. With no entries in MPB entry, add MPB2 entry, reboot, should be able to read back MPB2 entry. (Verify Security Page 0 Slot 0-1, Security Page 1 writing/reading is working.
3. With existing entry in MPB1, validate code can handle adding/updating MPB2 entry. And Read MPB2 content back successfully after reboot. MPB1 content should not be affected.
4. Validate if MPB1/MPB2 region is erased, MR should be able to get the data back from MPB1 backup region (Original MR's MPB2 region for backup).
5. Downgrade testing, with MPB2 entries present, downgrade to 7.13, add/update MPB1 entries, this should trigger a Flash Erase of MPB1 region. Upgrade back to 7.14 code, validate Security Page 0/1 data still present.

EnhancementRequest ID: DCSG00079183
Headline: Revert the algorithm which determine if offload is sustainable
Description Of Change: In a recent activity, the algorithm was changed to use max voltage instead of min voltage in the Vesr calculation.
This activity is reverting back that change, suggested by the hardware team.
The fully charge check was added in the original activity, and that is the fix for the original issue.

EnhancementRequest ID: DCSG00079238
Headline: Update Sea Channel XMLs to PCI Device ID 0xE6
Description Of Change: The hardware controls the lower 2 bits of the PCI Device ID and will set them depending on configurable vs. hard secure. So we previously put PCI Device ID 0xE4 in the XML files. Since this isn't a valid ID, it has been confusing people. Also, even though it's not in the XML, the packaging process uses the PCI Device ID in the HwBoardImageConfig to select the correct BIOS image when building full flash images. So just change them all to 0xE6 (Hard Secure) since that is what will be shipped.

EnhancementRequest ID: DCSG00079737
Headline: Support Vision FW signing
Description Of Change: Support Vision FW signing

EnhancementRequest ID: DCSG00080714
Headline: Add output to RMC log to indicate image is for debug use
Description Of Change: Modified RMC ring buffer parser to look for debug flags and enhanced log output to display it.

EnhancementRequest ID: DCSG00081168
Headline: Avenger support for the LIBSPDM
Description Of Change: Add Avenger support for the LIBSPDM. Requires to change the certificate lengths to 4k instead of 64K. Without this linker scripts needed to change for fpga compile.

In the production code the certificates will be read from Config Pages.

EnhancementRequest ID: DCSG00082166
Headline: SECUREBOOT_LIB: Move hardware touch (ApSha HASH & HMAC and OTP eFuse Read) from MR SPDM code to Secure Boot Lib
Description Of Change: - Move hardware touch (ApSha HASH & HMAC and OTP eFuse Manufacturing Data Read) from MR SPDM code to Secure Boot Lib
- Add APIs for ApSha HASH & HMAC and OTP eFuse Manufacturing Data Read in Secure Boot Lib for the client code to use.
- MR SPDM code will use this code, and IT FW will also can use this code.

EnhancementRequest ID: DCSG00082170
Headline: SPDM: Move hardware touch (ApSha HASH & HMAC and OTP eFuse Read) from MR SPDM code to Secure Boot Lib
Description Of Change: - Move hardware touch (ApSha HASH & HMAC and OTP eFuse Manufacturing Data Read) from MR SPDM code to Secure Boot Lib
- Add APIs for ApSha HASH & HMAC and OTP eFuse Manufacturing Data Read in Secure Boot Lib for the client code to use.
- MR SPDM code will use this code, and IT FW will also can use this code.

EnhancementRequest ID: DCSG00082841
Headline: Aero: Change XMEMCOPY default to disabled in Aero
Description Of Change: Setting XMEMCOPY in Man Page 11 to zero will cause firmware to execute certain sections of code out of flash and leave constant data in flash. This is done to offset the performance hit tied to features with large code size.

EnhancementRequest ID: DCSG00082978
Headline: Check in XSD for new security page ExtManPage 49/50/51, Security Page 0/1
Description Of Change: Check in XSD for new security page ExtManPage 49/50/51, Security Page 0/1

EnhancementRequest ID: DCSG00083082
Headline: pl: backend PCIe: add debug print for a discovery failure case
Description Of Change: Added a PCIe discovery debug print for new device check failure status.

EnhancementRequest ID: DCSG00083856
Headline: CM Utility to perform automated Deliver and Rebase actions
Description Of Change: Utilities are generated for performing automated deliver and rebase actions on configured streams. Utility will perform and forced merge option for any conflict scenarios. utilities can be added as a separate read-only component to the project/stream. Created wiki page with usage information for developers.

EnhancementRequest ID: DCSG00086663
Headline: MISC changes for NVMe drive repair
Description Of Change: MISC changes for NVMe drive repair found during dev testing

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EnhancementRequest ID: DCSG00086765
Headline: SECUREBOOT_LIB: Move SRK and CCR eFuse register access functions to SBLIB
Description Of Change: Move SRK and CCR eFuse register access functions from MR FW to SBLIB.
Added APIs in SBLIB for the client code to call these new SBLIB functions

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EnhancementRequest ID: DCSG00086780
Headline: FW SAS MEGA API:Change MR_EVT_CTRL_FLASH_DISALLOWED_SB_KEY_CHANGE_PENDING event from Info to Warning
Description Of Change: Updated MR_EVT_CTRL_FLASH_DISALLOWED_SB_KEY_CHANGE_PENDING and MR_EVT_CTRL_SB_SOFT_SECURE_MODE events from INFO to WARNING.

EnhancementRequest ID: DCSG00087564
Headline: MBEDTLS LIB: Change large local variable memory allocation from the stack to dynamic memory allocation from the heap
Description Of Change: IT FW team integrated MbedTLS Lib into their code base and run into issue related to stack overflow. There are several functions related to CSR and Certificate we have identified in MbedTLS Lib that declare local variables with large storage on the stack. As an example, function mbedtls_x509write_csr_der() declares local array variable with 3 KB storage on the stack. MR FW has larger stack memory and does not run into stack overflow issue.

Change large local variable memory allocation from the stack to dynamic memory allocation from the heap. This is to accommodate IT FW as IT FW has smaller stack size than MR FW.

EnhancementRequest ID: DCSG00091314
Headline: [SPDM]SBlib upgrade to 2.02
Description Of Change: Update SBlib to latest release which has SPDM related API's (CDI and HMAC)

EnhancementRequest ID: DCSG00091315
Headline: Release Automation: Submit auto-BST jobs
Description Of Change:
Automation scripts will initiate BST jobs for release binaries, monitor progress and update results.

EnhancementRequest ID: DCSG00092779
Headline: Security page 0 and page 1 - Wrapper
Description Of Change: Added wrapper functions to call the security page 0 read and write.

EnhancementRequest ID: DCSG00093331
Headline: MR API: update field in event structure.
Description Of Change: Adjust field data size in the substructure enclIdSlotIdPair in MR_EVT_DETAIL.

EnhancementRequest ID: DCSG00093342
Headline: Improve RMC debug image indicator
Description Of Change: Implement unique Register File value for debug RMC image

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EnhancementRequest ID: DCSG00094677
Headline: Release Automation: Integrate utility for deliver/rebase into release scripts.
Description Of Change:
Release scripts can perform deliver/rebase operation on repository at the time of release.

EnhancementRequest ID: DCSG00096299
Headline: SPDM: Implement Security Page Wrapper for reading/writing key page
Description Of Change: Implement Security Page Wrapper for reading/writing key page.

EnhancementRequest ID: DCSG00097417
Headline: SPDM_LIBRARY: Change for SPDM Policy Implementation
Description Of Change: This covers the following:
1.SPDM lib will get runtime SpdmStatus from client to determine if it can proceed to process Get_Cert/Get_Digest/Challenge.
If under minimum cap mode, library only allows to run Get_Version/Get_Cap/Nego_Algo
2.SPDM lib will get runtime SpdmStatus and set corresponding SpdmStatus after Challenge is done.
If Authentication require/active flag is set, clear those flag after Spdm Library receive Challenge.
3. SPDM lib will get Asym and Hash Algorithm from client when processing negotiate_algorithm.
4. SPDM lib will get Nonce from client for Challenge Response.

EnhancementRequest ID: DCSG00098359
Headline: 7.14 MR: Change for SPDM Policy Implementation
Description Of Change: This covers the following:
1. Covers the boot up logic to read ExtManPage49 to define SPDM policy.
This include logging corresponding event.
2. Covers the case of both certificate page and key page not present, and issue to generate key pair based on ExtManPage50 define algorithm.
3. Implement failure logic DCMD for cases of Minimal Capability Mode.
4. Implement new SPDM LIB client routines needed for SPDM library.

EnhancementRequest ID: DCSG00098752
Headline: SEA IT TRNG HW enable
Description Of Change: Implemented TRNG init and Random number generator functions

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EnhancementRequest ID: DCSG00101901
Headline: Add support to build Avenger specific sbr image.
Description Of Change: Add support to build Avenger specific sbr image.

Aero needs SPICO image, but Avenger doesn't need it. Add new function create_sbr_image_avng() to take care of it.

EnhancementRequest ID: DCSG00102973
Headline: Avenger IOP: Scons scripts update for firmware versioning
Description Of Change: Scripts update for firmware versioning

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EnhancementRequest ID: DCSG00103023
Headline: Coverity Upgrade Aero Build to latest version
Description Of Change: Scons changes were made so that the Coverity version number is no longer hardcoded in some paths.

EnhancementRequest ID: DCSG00103227
Headline: [Aero SPDM] XSD changes to support SPDM version in a new manufacturing page
Description Of Change: 1) SPDM versions supported need to be kept track of.
2) Add the support to store the SPDM versions to new Manufacturing Page.

EnhancementRequest ID: DCSG00105005
Headline: Certificate read and Write wrapper functions & Slot management
Description Of Change: 1. Certificate read and Write wrapper functions.
2. Slot & group management
3. Key page wrapper calling in SPDM commands.

EnhancementRequest ID: DCSG00105230
Headline: Modify generate HBICList script
Description Of Change: Modify python script that support for generating HBICList from FW RO.

EnhancementRequest ID: DCSG00105430
Headline: Implement changes to secureSign signing tool and infrastructure to support mixed list of PublicKeys that are from SCGCQ and DCSG.
Description Of Change: Implement changes to secureSign signing tool and infrastructure to support mixed list of PublicKeys that are from SCGCQ and DCSG.

EnhancementRequest ID: DCSG00106306
Headline: FW SAS PVT API : A mechanism to get supported device protocols for each controller form factor
Description Of Change: Added MPI2_MR_PARAMS_PAGE_0.ctrlDisplayType

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EnhancementRequest ID: DCSG00106380
Headline: MR API changes - Support new Provisional bit in CTRL INFO and new MFI status for Platform Security SPDM
Description Of Change: MR API changes:

1) A new bit in CTRL INFO to tell APP when controller is in provisional mode

2) A new MFI status MFI_STAT_OK_PSEC_CERT_NOT_PRESENT to tell APP
certificate at slot xx is not yet present.

3) The existing MR_DCMD_CTRL_PSEC_EXPORT_CSR in MR API, add a comment to indicate the subject name string "rSubName"
is a null terminated string, and subject name length "rSubNameLen" include string plus null terminator.

EnhancementRequest ID: DCSG00106381
Headline: SPDM: Add support for new bit CTRL INFO and new MFI status in MR API
Description Of Change: Add support in MR FW for new MR API changes: Support new Provision bit in controller info and new MFI status for Platform Security SPDM:

1) During boot up, check if controller is in certificate provision mode, set certificate provision mode bit in controller info to
let APP know.

2) When APP issues Get Config Page DCMD to request certificate for a slot (Broadcom manufacturing slots 0 and 1) that is not yet present in MPB2 region,
FW will return MFI status MFI_STAT_OK_PSEC_CERT_NOT_PRESENT to tell APP certificate requested slot is not yet present.

EnhancementRequest ID: DCSG00108514
Headline: XSD change adding SPDM new page ExtManPage 52 for SPDM Version
Description Of Change: XSD change adding SPDM new page ExtManPage 52 for SPDM Version

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EnhancementRequest ID: DCSG00108534
Headline: XSD : Need a mechanism to get supported device protocols for each controller form factor
Description Of Change: Added new field ctrlDisplayType in MrParamsPage0

EnhancementRequest ID: DCSG00108545
Headline: Aero: Add support for SPDM ExtManPage 52
Description Of Change: Aero: Add support for SPDM ExtManPage 52

EnhancementRequest ID: DCSG00112317
Headline: NVRAM Aero SPDM Policy: Add Nvram flag to enable/disable SPDM feature in megamon
Description Of Change: Customer have requested a ROP build with SPDM disable.
While internal test team may want to test a lot of feature with SPDM enable such as host application SPDM related commands.
However, it is hard to maintain two ROP with two different XML SPDM page definition.
FW now introduce another flag enableSPDM in nvram.
By default, enableSPDM flag will start with 0, so next ROP, SPDM by default is disabled.
If testers want to enable SPDM and test manufacturing SPDM commands.
Please do megamon>EnableSPDM or megamon> DisableSPDM and reboot/ocr.
The flag is stored into Nvram and read back in next reboot/OCR.
So that SPDM Policy module can change to SPDM enable/disable mode.

EnhancementRequest ID: DCSG00125616
Headline: UCM Action tool feature to support rebase using latest baseline
Description Of Change: Added option to support rebase on latest baseline from parent stream.

EnhancementRequest ID: DCSG00129388
Headline: Implemented change to use FTP instead of UNC for upload / download of unsigned / signed artifacts to workaround firewall issue.
Description Of Change: Implemented change to use FTP instead of UNC for upload / download of unsigned / signed artifacts to workaround firewall issue.

EnhancementRequest ID: DCSG00131581
Headline: Update createSasversion.exe to use getCreds
Description Of Change: Update createSasversion.exe to use getCreds

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EnhancementRequest ID: DCSG00134416
Headline: MR API: Change event class for SPDM events
Description Of Change: Updated event error classifications to better-reflect true meaning. The following changes were made:

MR_EVT_CTRL_PSEC_CERT_SLOT_UPDATED	Change from EC_C to EC_I
MR_EVT_CTRL_PSEC_CERT_SLOT_INVALIDATED	Change from EC_C to EC_I
MR_EVT_CTRL_PSEC_CERT_SLOT_SEALED	Change from EC_C to EC_I
MR_EVT_CTRL_PSEC_CERT_IMPORT_FAILED	Change from EC_I to EC_C
MR_EVT_CTRL_PSEC_KEYPAIR_BAD	Change from EC_I to EC_C

EnhancementRequest ID: DCSG00134638
Headline: BST script change for single PLDM image removal
Description Of Change: Avoid BST scripts picking the PLDM image to flash for Host BST

EnhancementRequest ID: DCSG00137059
Headline: Ctrl - H support for pkg - secure Image flash validation
Description Of Change: Secure Image flash to include new module signature verification added.

EnhancementRequest ID: DCSG00139069
Headline: Enhance OEMs Dev BST scripts
Description Of Change: - Handle EPD and VD combinations
- Different Order of creation and deletions
- With BGOPs, IOs, Offline, Rebuild etc

EnhancementRequest ID: DCSG00140236
Headline: SPILIB 2.0: Add capability to support Winbond Parts with Factory Quad bit Disabled
Description Of Change: Added QE bit setting logic for Winbond Parts, specifically ones with part number not ending in "IQ"

EnhancementRequest ID: DCSG00141730
Headline: XSD changes Disk labels need to be tied to fixed physical ports in order

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Description Of Change: exposeToHostDeviceOrder is set 4 for OEMs.

EnhancementRequest ID: DCSG00143847
Headline: Add support for signing MegaRAID Legacy BIOS CU Images (CTLR) images
Description Of Change: Add support for signing MegaRAID Legacy BIOS CU Images (CTLR) images

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EnhancementRequest ID: DCSG00151058
Headline: API changes to expose MR_AUTO_CFG_PARAMETER for NONE mode
Description Of Change: Modified the DCMD to expose MR_AUTO_CFG_PARAMETER for NONE mode

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EnhancementRequest ID: DCSG00152322
Headline: Enhance OEMs Dev BST scripts for driver upgrade and downgrade
Description Of Change: - Handle Driver upgrade and downgrade combinations along with oob traffic

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EnhancementRequest ID: DCSG00166877
Headline: Aero SPDM Sblib change: provide sblib interface to disable specified HW debug port.
Description Of Change: During boot up, SBR will mask on all HW debug port disable bits.
And MR boot up code by default enable HW debug port through _main->SbLibInit->sbliEnableDebug (clear all HW debug ports bits).
Later after SPDM config pages is up, MR needs to disable specified HW debug port.
Current Sblib only have interface to enable all HW debug port.
Thus, Sblib needs to provide interface to disable specified HW debug port:
SBLI_STATUS sbliDisableDebug(U8 DebugPortDisableBitMask)
Where BitMask is using flags from sbliDef.h:
/*Expose HALI_DEBUG_PORT_DISABLES flags through SBLI API for MR/IT use to disable HW debug port*/
#define SBLI_CCR_DEBUG_PORT_SDB_DISABLE (1 << 2)
#define SBLI_CCR_DEBUG_PORT_JTAG_DISABLE (1 << 1)
#define SBLI_CCR_DEBUG_PORT_MDIO_DISABLE (1 << 0)

EnhancementRequest ID: DCSG00167313
Headline: Add new security events
Description Of Change: Two new security events are added.
MR_EVT_CTRL_LOCK_KEY_EKM_MODE_ENTERPRISE
MR_EVT_CTRL_LOCK_KEY_EKM_FAILURE_ENTERPRISE

EnhancementRequest ID: DCSG00171040
Headline: Updated personality change testing scripts to BST suite
Description Of Change: Updated test scripts to include personality change and PD erase testing in BST suite.

EnhancementRequest ID: DCSG00214352
Headline: SMART Polling Improvement- API Changes
Description Of Change: Define New Controller Properties structure (MR_CTRL_PROP_2) to expand new controller fields.

EnhancementRequest ID: DCSG00218726
Headline: Addition of atlas_bst scripts
Description Of Change: Added test scripts to run BST for Atlas

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EnhancementRequest ID: DCSG00218900
Headline: XSD :Add New fields 'predFailPollDAInterval' and 'predFailPollInterval' in MPI2_MR_PARAMS_PAGE_0
Description Of Change: Add new fields 'predFailPollDAInterval' and 'predFailPollInterval' in MPI2_MR_PARAMS_PAGE_0

EnhancementRequest ID: DCSG00222915
Headline: API change to add DCMD MR_DCMD_CTRL_LOCK_KEY_SECRET_KEY_APPLY and associated MFI STAT
Description Of Change: Added DCMD MR_DCMD_CTRL_LOCK_KEY_SECRET_KEY_APPLY to enter Boot time password
Added MFI STATs for above DCMD

EnhancementRequest ID: DCSG00223408
Headline: MR PVT API :Update mr_configpage.h file for New fields 'predFailPollDAInterval' and 'predFailPollInterval' in MPI2_MR_PARAMS_PAGE_0
Description Of Change: Update mr_configpage.h file for New fields 'predFailPollDAInterval' and 'predFailPollInterval' in MPI2_MR_PARAMS_PAGE_0

EnhancementRequest ID: DCSG00226081
Headline: SPDM python script: Support to build Challenge buffer with multiple GET_CERTIFICATE/CERTIFICATE_RESPONSE
Description Of Change: Current SPDM_LIB builds M1 challenge buffer with only one pair of Get_Certficate request/ Certificate Response.
So if BMC/emulator use multiple pairs of get_cert/cert_response to fetch CertificateChain.der, M1 buffer only contains the last pair of get_cert/cert_resp portion.
SPDM_LIB currently uses a static buffer possible to build M1 byte buffer to sign.
Change: In order to support multiple pairs of get_cert/cert_resp, emulator python script needs to keep track of all get_cert/cert_response and build M2 buffer with all the get_cert/cert_response pair.

EnhancementRequest ID: DCSG00226286
Headline: Preboot Trace Buffer [PTB] for Ventura/Aero - add a switch - MR API
Description Of Change: A new field was added to MR_SNAPDUMP_PROPERTIES. This controls whether the PTB feature is enabled, or disabled.

EnhancementRequest ID: DCSG00228248
Headline: Preboot Trace Buffer [PTB] for Ventura/Aero - add a switch - nvram
Description Of Change: A field was added so that PTB can be disabled in Snapdump.

EnhancementRequest ID: DCSG00229416
Headline: New MFI Stat for the updated recon behavior
Description Of Change: Added 2 new MFI stats

MFI_STAT_RECON_INPROG = 0xAB, /* Requested operation is not possible because of an active Reconstruction */
MFI_STAT_FW_ACTIVATION_PENDING = 0xAC, /* Failed to start the requested operation as FW activation is pending */

EnhancementRequest ID: DCSG00231443
Headline: MR7 API: Add package incompatibility reporting
Description Of Change:
Added 2 new fields,

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1. MR_CTRL_INFO.adapterOperations6.supportPackageIncompatibilityReporting
2. MR_CTRL_INFO.adapterStatus2.packageStampMismatchError

EnhancementRequest ID: DCSG00234319
Headline: Added power cycle tests in Atlas AutoBST
Description Of Change: Added power cycle tests in Atlas AutoBST. The number of power cycles to be run can be provided as argument to reset_atlas_using_apc.py e.g reset_atlas_using_apc.py 5

EnhancementRequest ID: DCSG00234348
Headline: Atlas BST:- USD integration
Description Of Change: 1. Write Unit Specific data with Invalid binary (RegionType is header != 30)- It should fail.
2. Write Unit specific data with Valid binary (RegionType in header == 30)- It should pass.
3. Reboot Atlas
- Reboot RDK and HOST in case of RDK platform.
- Reboot Host in case of HBA platform.
4. Ping the host and check if its up.
5. Once host is up, dump flashtable.
6. Check flashtable dump to see if 'UNIT DATA' region is VALID.

EnhancementRequest ID: DCSG00234391
Headline: BST setup with Channel HBA + Elrond
Description Of Change: BST setup with Channel HBA + Elrond

EnhancementRequest ID: DCSG00234646
Headline: Implement customSign.exe CLI wrapper utility to help customers sign with their private key
Description Of Change: Implement customSign.exe CLI wrapper utility to help customers sign with their private key

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EnhancementRequest ID: DCSG00237302
Headline: Make necessary changes to atlas_bst in valscripts to enable BST for Nvidia stream
Description Of Change: -Added virtual_atlas_config -Added VIRTUAL_ATLAS_SMOKE_TEST -Modified hba_config, Lenovo_config, rdk_config, run_bst, reset_atlas_using_apc, common_lib, SerialLib to enable BST for Nvidia stream without disturbing BST for other systems.

EnhancementRequest ID: DCSG00246317
Headline: SMART Polling Improvement - API Changes
Description Of Change: Define New Controller Properties structure (MR_CTRL_PROP_2) to expand new controller fields.

EnhancementRequest ID: DCSG00253665
Headline: Added drive push pull tests
Description Of Change: Added test scripts to
1. Push all the drives and verify all drives are detected in Host
2. Pulled few drives and verify that pulled drives are not detected

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EnhancementRequest ID: DCSG00253672
Headline: Add Atlas Behind Aero Setup in Atlas AutoBST
Description Of Change: Added scripts to include Atlas Behind Aero setup in AutoBST.

EnhancementRequest ID: DCSG00256271
Headline: To add return status MFI_STAT_OK_REBOOT_REQUIRED to MR_DCMD_LD_SET_PROPERTIES in mr.h
Description Of Change: The following return status has been added to the status list for the dcmd:

status: MFI_STAT_OK_REBOOT_REQUIRED
dcmd: MR_DCMD_LD_SET_PROPERTIES

EnhancementRequest ID: DCSG00257777
Headline: MFI SMP Port Num API changes
Description Of Change: Made API changes needed to support Port number for MFI SMP Commands.

EnhancementRequest ID: DCSG00265215
Headline: BST script modification due to change in RO content
Description Of Change: 1. Copy the XML from a new zipped folder created for BST
2. Modification of DS ports due to changes in device connection

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EnhancementRequest ID: DCSG00272230
Headline: MR PVT API: Add singlePortMultipathFeatures to MPI2_MR_PARAMS_PAGE_0
Description Of Change: MR PVT API: Add singlePortMultipathFeatures to MPI2_MR_PARAMS_PAGE_0

EnhancementRequest ID: DCSG00278286
Headline: NVDATA change for Ruby SED support
Description Of Change: Update MR Parameter Page 0 with Ruby SED related field

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EnhancementRequest ID: DCSG00278424
Headline: MR PVT API :Update mr_configpage.h file for Ruby SED support
Description Of Change: add a new field for Ruby SED in MPI2_MR_PARAMS_PAGE_0

EnhancementRequest ID: DCSG00282675
Headline: XSD: Add New field 'parityReadCacheBypass' in MPI2_MR_PARAMS_PAGE_0 for PR DCSG00237022
Description Of Change: Update MR Parameter Page 0 with parityReadCacheBypass related field.

EnhancementRequest ID: DCSG00282676
Headline: MegaAPI: Add API Controller Properties and MFCD for ParityReadCacheBypass (PR: DCSG00237022)
Description Of Change: Add API Controller Properties and MFCD for ParityReadCacheBypass (PR: DCSG00237022)

EnhancementRequest ID: DCSG00284472
Headline: PvtAPI: Add new field 'parityReadCacheBypass' in MPI2_MR_PARAMS_PAGE_0 for PR DCSG00237022
Description Of Change: Add new field 'parityReadCacheBypass' in mr_configpage.h for MPI2_MR_PARAMS_PAGE_0 (PR DCSG00237022).

EnhancementRequest ID: DCSG00292323
Headline: MR API: reclassify MR_EVT_CTRL_FW_VALID_SNAPDUMP_AVAILABLE as informational
Description Of Change: In MR FW, the following event has been classified as critical; to downgrade it to informational.

MR_EVT_CTRL_FW_VALID_SNAPDUMP_AVAILABLE

EnhancementRequest ID: DCSG00301780
Headline: Disable custom image build for HBA BST
Description Of Change: Disable custom image build for HBA BST

EnhancementRequest ID: DCSG00310657
Headline: XSD : Add New field 'singlePortMultipathFeatures' in MPI2_MR_PARAMS_PAGE_0
Description Of Change: XSD : Add New field 'singlePortMultipathFeatures' in MPI2_MR_PARAMS_PAGE_0 PR# DCSG00242971

EnhancementRequest ID: DCSG00313996
Headline: Make updating the embedded key(step 1) of securesign optional.
Description Of Change: Added CLI argument '-noembed' which turns off the logic to embed the public key hash of the latest or customer key in the FW bin.

EnhancementRequest ID: DCSG00314237
Headline: Add noembed support to signtools
Description Of Change: Embedded public is used only in APP image. Remove this in other modules.

EnhancementRequest ID: DCSG00315798
Headline: SPDM python script: Add handling to manage actual certificate certain for Aero with depth=4
Description Of Change: Aero Controller will support certificate chain with depth = 4. CM team will generate this certificate chain. Add handling in Python SPDM scripts to test certificate with depth=4.

Actual certificate chain with depth=4 is shown below:

Root CA Cert - ECDSA (NIST CURVE) P-521, SHA2-512 - level 0

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Intermediate CA Cert - ECDSA (NIST CURVE) P-384, SHA2-384 - level 1

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Model CA Cert - ECDSA (NIST CURVE) P-256, SHA2-256 - level 2

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Cisco Device Cert - ECDSA (NIST CURVE) P-256, SHA2-256 - level 3

DEPTH = 4

Note:
The handling for hardcoded certificate with depth = 3 is still kept in case we still want to test with hardcoded certificate with depth=3.

EnhancementRequest ID: DCSG00324772
Headline: Set disablePdDegradedMedia in all XSDs
Description Of Change: Set disablePdDegradedMedia in all XSDs

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EnhancementRequest ID: DCSG00035830
Headline: Change the default behaviour of LED management for ePDs
Description Of Change: OEM has requested the default behaviour of LED management for ePDs.

Changes related to this is to disable host management of ePD LED by default. And provide an option for user to enable the same.

EnhancementRequest ID: DCSG00040356
Headline: AutoCfg Execute Once option is modified.
Description Of Change: To achieve this apps are changing our direction to find out the allowed configuration for execute-once . Hence certain autocfg related code is modified to support these new features/ behaviours.

EnhancementRequest ID: DCSG00026421
Headline: Preserve EPT-PT as boot device after reboot.
Description Of Change: Updated code to set boot device when ePDs are created if boot device is not set.

EnhancementRequest ID: DCSG00024579
Headline: OOB Passthrough Command Restrictions
Description Of Change: Restrict out-of-band (OOB) pass through commands from reading or writing user data.

EnhancementRequest ID: DCSG00041659
Headline: Add NVME Init failure prints.
Description Of Change: Updated FW to print NVME Init failure events.

EnhancementRequest ID: DCSG00025207
Headline: Multi-Chemistry BMU support
Description Of Change: MR FW support for different battery chemistries added.

EnhancementRequest ID: DCSG00034355
Headline: Removal of key caching from SRAM
Description Of Change: MR FW deletes key once it completes key related operations. Keys are not stored in controller memory.

EnhancementRequest ID: DCSG00064583
Headline: Aero SAS Performance Enhancement on AMD Rome as part of PR
Description Of Change: set IOC_CFG_MFG_PG11_ADDLFLAGS_PCIE_RELAXED_ORDERING in ManPage11of NVdata

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EnhancementRequest ID: DCSG00014871
Headline: Remove informational prints from tty log
Description Of Change: Changed requested prints to conditional prints

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EnhancementRequest ID: DCSG00068257
Headline: Increase timeout value for Revert Tper commands to support drives from new drive vendor
Description Of Change: Increased timeout value in MR FW to allow completion of Revert Tper commands.

EnhancementRequest ID: DCSG00076595
Headline: Enable DST in NVMe Cmd Filtering
Description Of Change: Allow NVME_ADMIN_CMD_OPCODE_DEVICE_SELF_TEST as a NVMe PT commands in DCMD.

EnhancementRequest ID: DCSG00056745
Headline: In pre boot environment, if IO's received greater than 1MB reject the command with correct error status and not to Assert
Description Of Change: In pre-boot environment if MR FW gets a IO greater than 1MB, MR FW will reject the command with sense information SN_ILLEGAL_REQUEST, SA_INVALID_FIELD_IN_CDB and MFI status as MFI_STAT_SCSI_IO_FAILED.

EnhancementRequest ID: DCSG00054917
Headline: Allow FW to reprovision UBAD drives
Description Of Change: MR FW will now allow reprovisioning of unconfigured bad drives.

EnhancementRequest ID: DCSG00054919
Headline: FW should treat copyback start as import success in case of secured drives.
Description Of Change: In case there is a drive that is inserted on which copyback operation needs to be initiated but is keyed to a different key than the current controller key; then the drive needs to be imported with the drive's key. During this import sequence, the drive is first rekeyed to the controller key and then MR FW checks if copyback can be initiated.If copyback can be initated, it is. MR FW would previously return MFI_STAT_FOREIGN_CONFIG_INCOMPLETE - this is not a desirable user experience. Instead now, MR FW tracks if a drive was rekeyed and if copyback was initated it returns MFI_STAT_OK.

EnhancementRequest ID: DCSG00073908
Headline: Include new field Auto Config Parameter structure to indicate that AutoConfig R0 property cannot be set .
Description Of Change: Firmware would hard code the newly included bit to 1 for this OEM only and will not be made as configurable parameter.
This bit can only be retrieved using get operation auto configure command.
Supported fields command/operation should not be used to retrieve this bit value.

EnhancementRequest ID: DCSG00056769
Headline: Treat PD missing for RLM only as critical
Description Of Change: For specific OEM,
- Any PD that is undergoing RLM and is missing during boot will be considered as a critical event.
- Will issue boot messages when controller is in eHBA mode
- Edited certain boot messages for clarity

EnhancementRequest ID: DCSG00072757
Headline: Change to BMU update process for power loss recovery
Description Of Change: - If BMU is in ROM mode during boot, then send exit ROM command
- Clear NVRAM batId field before any BMU update and repopulate the field once BMU updates successfully

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EnhancementRequest ID: DCSG00062819
Headline: EnhancementRequest DCSG00062819: SPDM: Implementation: DCMD Commands addition for Export/Import CSR
Description Of Change: Implemented the DCMD commands to handle the Export Import and management commands for platform security feature.Also added a way to test this through debugger.

EnhancementRequest ID: DCSG00078835
Headline: Advertise certain Secure Boot Properties using a config page for Application to be able to display it
Description Of Change: Added a new Config Page: IO Unit Page 12 to share below Secure Boot Properties for Application's to be able to display it:
1. Secure Boot Enabled
2. Controller in Soft Secure Mode
3. Controller in Hard Secure Mode
4. Key Update Pending
5. Remaining Secure Boot Key Slots
6. Total Key Slots

EnhancementRequest ID: DCSG00057696
Headline: Secure drive Crypto erase behavior change
Description Of Change: Crypto erase should not been allowed to start on JBOD drives. Because JBODs are pass-through devices, no controller background operations should be allowed when OS is managing it. Hence, Crypto erase needs to be disallowed on Ventura JBOD drives.

EnhancementRequest ID: DCSG00082984
Headline: Monitoring Drive Performance and Predictive Failure feature to be removed for certain OEM
Description Of Change: Disabled the feature for certain OEM

EnhancementRequest ID: DCSG00098356
Headline: Unblock the ability to secure EPDs via SEKM
Description Of Change: MR FW will allow securing of EPDs using EKMS/SEKM

EnhancementRequest ID: DCSG00109563
Headline: This ER is to allow exposing of active internal expander based backplane to host for jbod LED management.

Description Of Change: A new bit is added in enclosure information structure in firmware. This bit indicates whether the direct attached backplane is expander based or not.

When enclosure is first detected and added, firmware queries for enclosure page 0.
This enclosure page 0 contains information indicating whether the enclosure is expander based or not. This information is present in enclosure page 0-> Flags.
If this flag is set in enclosure page0 , then it means that backplane is expander based. And the newly added bit in enclosure information structure is set to TRUE (for expander based backplanes only).
This bit helps differentiate between active (expander based) and passive (SEP based) internal backplanes.

If user chooses to allow host to access backplane then only expander based internal backplane are allowed to be exposed to host.

EnhancementRequest ID: DCSG00108508
Headline: Need a mechanism to get supported device protocols for each controller form factor
Description Of Change: Based on configured NVDATA value, MR FW sets deviceInterface and Profile information

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EnhancementRequest ID: DCSG00112013
Headline: Initialize and persist SES management related flags when personality change from HBA to RAID
Description Of Change: Updated code to initialize and persist SES management related flags when personality change from HBA to RAID for an OEM

EnhancementRequest ID: DCSG00115404
Headline: MR FW feature to dump battery FRU data
Description Of Change: Implement the feature to dump Battery FRU Bytes in TTY Log.

EnhancementRequest ID: DCSG00120440
Headline: Restore Factory Default doesn't prompt user to reboot the system after being performed
Description Of Change: MR Firmware will now return MFI_STAT_OK_REBOOT_REQUIRED for successful completion of DCMD MR_DCMD_CTRL_SET_FACTORY_DEFAULTS.

EnhancementRequest ID: DCSG00053656
Headline: Support for NVMe Firmware Download when the image size exceeds the SNTL Transfer limitation.
Description Of Change: Added support for breaking a single write buffer firmware download request in to multiple NVMe commands and send them to NVMe controller without overlapping.

EnhancementRequest ID: DCSG00143569
Headline: Disable hardware debug ports
Description Of Change: Disable debug ports to avoid any vulnerability and extra security to block accessing debug ports.
ExtManpage49 bits 10:8 in Flags variable used for debug ports disable.
IOC_CFG_EXT_MFG_49_FLAGS_MDIO_PORT_DISABLE // bit -8
IOC_CFG_EXT_MFG_49_FLAGS_JTAG_PORT_DISABLE // bit -9
IOC_CFG_EXT_MFG_49_FLAGS_SDB_PORT_DISABLE // bit -10

Note :To revert back debug ports, use good FW and enable above bits in ExtManpage49 bits 10:8 in Flags variable ,
flash the FW.

EnhancementRequest ID: DCSG00216966
Headline: Execute once Auto configure option needs to be allowed for EPD-PT behaviour mode for certain controllers.
Description Of Change: Auto configure executeOnce option was blocked in certain controllers for EPD-PT auto configure behaviour mode. Now this is allowed. However please note this is still not allowed in controllers having eHBA personality.

EnhancementRequest ID: DCSG00183076
Headline: Support bit for "cannotExecuteOnce" autoconfig parameter needs to be set as 0 for all configure modes
Description Of Change: Support bit for "cannotExecuteOnce" autoconfig parameter is set to 0 for all configure modes

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EnhancementRequest ID: DCSG00227036
Headline: Preboot Trace Buffer [PTB] for Ventura/Aero - add a switch - MR firmware
Description Of Change: A field was added to Snapdump properties so that PTB can be disabled from HII.

EnhancementRequest ID: DCSG00312222
Headline: Snap-dump Enhancement - remove unnecessary duplicate prints
Description Of Change: In funtion FlashEvaluateBQMI()
- Commented out a print as it does not provide any useful information when flashing a component.
- Even though its commented I have added additional information to dump flash header component name.

In funtion PersonalityGetRAIDSubDevId()
- Commented out a print as it does not provide any useful information on controller boot.

GCA Release (DCSG00011506) - MR_FW_BLD_TOOLS - 1.03

ReleaseOrderID: DCSG00011506
Headline: GCA Release: MR_FW_BLD_TOOLS - 1.03 MR_FW_BLD_TOOLS
Release Version: 1.03
Product Org: MegaRAID
Product Gen: SAS3.5
Product Family: MR_FW
UCM Project: MR_FW_BLD_TOOLS
Release Type: GCA
UCM Stream: MR_FW_BLD_TOOLS_Rel
Owner: st887734
Release Baseline: MR_FW_BLD_TOOLS_Rel_2019-07-25@\MegaRAID
Release Date / Time: 2019-07-25 16:22:41.000000
Release Type: GCA

Beta Release (DCSG00007929) - SASPARSER - 11.02.00.00

ReleaseOrderID: DCSG00007929
Headline: SASPARSER: DCSG Re-Release 11.02.00.00
Release Version: 11.02.00.00
Product Org: SCS
Product Gen: SAS3.5
Product Family: ControllerFw
UCM Project: SASPARSER
Release Type: Beta
UCM Stream: SASPARSER_Int
Owner: rclegg
Release Baseline: SASPARSER_7_12_2019@\FWUTIL
Release Date / Time: 2019-07-15 16:06:51.000000
Release Type: Beta

HWBoardImageConfig: (DCSG00320061) - Quanta_152D_8B00 QS3516B-32PD-R0156

hwBoardImgCfgId:	DCSG00320061
Config Name:	Quanta_152D_8B00 QS3516B-32PD-R0156
Board Number:	QS-3516B-R5-PD32
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B00
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5014
NVDATA XSD Name:	LSISAS3516.xsd

HWBoardImageConfig: (DCSG00320059) - Quanta_152D_8B00_soem1 QS3516B-32PD-R0156

hwBoardImgCfgId:	DCSG00320059
Config Name:	Quanta_152D_8B00_soem1 QS3516B-32PD-R0156
Board Number:	QS-3516B-R5-PD32
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B00
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5015
NVDATA XSD Name:	LSISAS3516.xsd

HWBoardImageConfig: (DCSG00320060) - Quanta_152D_8B00_soem2 QS3516B-32PD-R0156

hwBoardImgCfgId:	DCSG00320060
Config Name:	Quanta_152D_8B00_soem2 QS3516B-32PD-R0156
Board Number:	QS-3516B-R5-PD32
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B00
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5015
NVDATA XSD Name:	LSISAS3516.xsd

HWBoardImageConfig: (DCSG00320062) - Quanta_152D_8B01 QS3516B-240PD-R0156

hwBoardImgCfgId:	DCSG00320062
Config Name:	Quanta_152D_8B01 QS3516B-240PD-R0156
Board Number:	QS-3516B-R6-PD240
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B01
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5014
NVDATA XSD Name:	LSISAS3516.xsd

HWBoardImageConfig: (DCSG00320057) - Quanta_152D_8B01_soem1 QS3516B-240PD-R0156

hwBoardImgCfgId:	DCSG00320057
Config Name:	Quanta_152D_8B01_soem1 QS3516B-240PD-R0156
Board Number:	QS-3516B-R6-PD240
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B01
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5015
NVDATA XSD Name:	LSISAS3516.xsd

HWBoardImageConfig: (DCSG00320058) - Quanta_152D_8B01_soem2 QS3516B-240PD-R0156

hwBoardImgCfgId:	DCSG00320058
Config Name:	Quanta_152D_8B01_soem2 QS3516B-240PD-R0156
Board Number:	QS-3516B-R6-PD240
PCB Internal Name:	Talladega
Customer Account:	Quanta
Vendor ID:	1000
Device Id:	0014
Sub-System Vendor Id:	152D
Sub-System Device Id:	8B01
FW Image Type:	MR
NVDATA ProductId:	MRROMB
NVDATA Minor Version:	5015
NVDATA XSD Name:	LSISAS3516.xsd

Custom Images:

Full Flash Images:				
File Path:	Check Sum 8-Bit:	Check Sum 16-Bit:	MD5 CheckSum:	Size (bytes):
customImages\8B00-16i\8B00-16i_NOPAD\8B00-16i_nopad.rom	2BCB CF8D	183E 1FC8	700F9F3C40803F7FA5D5AE68B304710A	7,340,032
customImages\8B01-16i\8B01-16i_NOPAD\8B01-16i_nopad.rom	2BCB D0C0	183F 9C7E	413C23150BF8F6F2DE2DD89E909E977B	7,340,032
customImages\8B01-16i\8B01-16i_32MB\8B01-16i_32MB.rom	BA3B D168	1777 0EB5	BAD035C5056AFDC51D3C6A8E047E555B	33,554,432
customImages\8B01-16i\8B01-16i_16MB\8B01-16i_16MB.rom	BB3B D119	17F7 1A5A	E0CD21A3B57251249ED8A221845424E7	16,777,216
customImages\8B00-16i\8B00-16i_32MB\8B00-16i_32MB.rom	BA3B CEBA	1776 B360	92EF22C6BA13F0518D30493A1F1F0FEF	33,554,432
customImages\8B00-16i\8B00-16i_16MB\8B00-16i_16MB.rom	BB3B CF06	17F6 8CD3	71726A8BCD21925B0B6DA8436CC75F15	16,777,216