

ReleaseOrder ID: SCGCQ02083305

Headline: Point Release: SASFW_Intruder_Phase_16.0 - 16.00.09.00 IT/IR Release

Release Version: 16.00.09.00

UCM Project: SAS3.5FW_MASTER_DEV

Sub UCM Project: SASFW_Intruder_Phase_16.0

UCM Stream: SASFW_Intruder_Phase_16.0_Rel

Release Type: Point

State: Open

Release Baseline: SASFW_Intruder_Phase_16.0-2019-03-22-16.00.09.00_REL_1553274213@
SAS_CTRL_FW

Release Date:

Date Generated: Mar 22, 2019

Defects Fixed (3):

ID: SCGCQ02064802 (Port Of Defect SCGCQ01963394)

Headline: PL Spinup: Firmware Takes a Long Time to Grant Spinup to Some Drives/Phys

Description Of Change: Fixed the spinup queue entries to be a fully functional linked list, rather than an array. This allows for spinup requests to be serviced in the order they were received from hardware, even in cases where entries are being re-used. When an entry is invalidated, it's moved to the end of the queue.

Issue Description: PL firmware may take a long time to grant spinup to some drives. In the case of SATA drives, this can lead to the drives not being discovered within the port enable/first discovery timeout. This happens because in cases where entries on the PL spinup queue are re-used (multiple spinups on some phys), spinup requests may not be serviced in the order they were received.

Steps To Reproduce: This was seen with 16 direct attach SATA drives, MaxTargetSpinup value of 2, and SpinupDelay value of 6 seconds.

ID: SCGCQ02065660 (Port Of Defect SCGCQ01969521)

Headline: PL : Task management timeout is observed if the task management type is invalid

Description Of Change: In task management, added handling to fail the task management if the task management type is invalid.

Issue Description: Server hang and reboot observed if the task management type is invalid

Steps To Reproduce: Issue task management with invalid task management type to SAS drive

ID: SCGCQ02078155 (Port Of Defect SCGCQ02066816)

Headline: IOP: Interrupts to Host Are Incorrectly Masked Leading to IO and TM Timeouts

Description Of Change: In the config trap code for the PCIe Device Status and Control register, when checking the InitiateFunctionLevelReset bit, qualify on the byte-enable bit for that byte.

Issue Description: Phase 16 implemented a FW workaround for a HW issue with handling Function Level Resets (FLR). The implementation had a hole whereby it could falsely detect an FLR request. As part of the FLR process, FW disables interrupts which will be re-enabled on FLR completion. Since this is a false detection, no FLR occurs thus interrupts are never re-enabled. This results in IO/Task Management timeouts, and propagated error recovery of the HBA.

Steps To Reproduce: Perform a PCI config write directed at the HBA as follows:
- Offset 0x70 (PCIe Device Status and Control)
- Byte enable bits set only for the two upper bytes (Status)
- Bit 15 set (InitiateFunctionLevelReset)

Interrupts to the host will be masked, causing all outstanding requests to timeout from the host perspective.

Enhancements Implemented (1):

ID: SCGCQ02082632

Headline: PL Serdes: Add Nvdata Option to Enable Rx EQ Adaption for SATA

Description Of Change: Added an NVDATA option to enable RX EQ adaption in the serdes for direct connect SATA drives. It's in Manufacturing Page 40, FeatureFlags, bit 2 (mask 0x04). A value of 0 for this bit is the existing behavior (no adaption for SATA). To enable RX EQ adaption for SATA, set this bit to 1.