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SSBLOG SECTION

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SSBLOG05-90 Byte27 = 81 (CHK3) Byte28-31
SSBLOG05-90 (1) Byte28 = 00/01/10/11/20/21/22/23/40/41/42/43/50/51/52/53/54/55/ 58/59/5A/5B/5C/5D/60/61/62/63/80/81/82/83/84/90/91/A0/A1/A2/A3/F0
SSBLOG05-100 Byte27 = 81 (CHK3) Byte40-7F Detail
SSBLOG05-100 (1) Byte28 = 80
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SSBLOG05-260 (5) Byte28 = 84
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SSBLOG05-340 (7) Byte28 = 10/11/50-55/58-5D/60-63
SSBLOG05-380 (8) Byte28 = A3
SSBLOG05-420 (9) Byte28 = A0
SSBLOG05-460 (10) Byte28 = A1
SSBLOG05-500 (11) Byte28 = A2
SSBLOG05-540 (12) Byte28 = 90
SSBLOG05-580 (13) Byte28 = 91
SSBLOG05-620 (14) Byte28 = 00
SSBLOG05-660 (15) Byte28 = F0

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SSBLOG05-700 • Byte27 = 84 (CHK4)
SSBLOG05-710 Byte27 = 84 (CHK4) Byte28-31
SSBLOG05-710 (1) Byte28 = 20/21/22/23/24/25 (FC IFB CHK4 – PCI 0 ~ 5 Error1)
Byte28 = 28/29/2a/2b/2c/2d (FC IFB CHK4 – PCI 0 ~ 5 Error2)
Byte28 = 30/31/32/33/34/35 (FC IFB CHK4 – FC Protocol 0 ~ 5 Error)
Byte28 = 36/37/38/39 (FC IFB CHK4 – LRP 0 ~ 3 Error)
Byte28 = 3a (FC IFB CHK4 – No HW Error)
SSBLOG05-720 (2) Byte28 = 40/41/42/43/44/45 (SAS IFB CHK4 – PCI 0 ~ 5 Error1)
Byte28 = 48/49/4a/4b/4c/4d (SAS IFB CHK4 – PCI 0 ~ 5 Error2)
Byte28 = 50/51/52/53/54/55 (SAS IFB CHK4 – FC Protocol 0 ~ 5 Error)
Byte28 = 56/57/58/59 (SAS IFB CHK4 – LRP 0 ~ 3 Error)
Byte28 = 5a (SAS IFB CHK4 – No HW Error)
SSBLOG05-740 Byte27 = 84 (CHK4) Byte40-7F Detail
SSBLOG05-740 (1) Byte28 = 20/40
SSBLOG05-860 (2) Byte28 = 21/41
SSBLOG05-980 (3) Byte28 = 22/42
SSBLOG05-1100 (4) Byte28 = 23/43
SSBLOG05-1220 (5) Byte28 = 24/44
SSBLOG05-1340 (6) Byte28 = 25/45
SSBLOG05-1460 (7) Byte28 = 28/48
SSBLOG05-1580 (8) Byte28 = 29/49
SSBLOG05-1700 (9) Byte28 = 2A/4A
SSBLOG05-1820 (10) Byte28 = 2B/4B
SSBLOG05-1940 (11) Byte28 = 2C/4C
SSBLOG05-2060 (12) Byte28 = 2D/4D
SSBLOG05-2180 (13) Byte28 = 30/50
SSBLOG05-2300 (14) Byte28 = 31/51
SSBLOG05-2420 (15) Byte28 = 32/52
SSBLOG05-2540 (16) Byte28 = 33/53
SSBLOG05-2660 (17) Byte28 = 34/54
SSBLOG05-2780 (18) Byte28 = 35/55
SSBLOG05-2900 (19) Byte28 = 36/56
SSBLOG05-3020 (20) Byte28 = 37/57
SSBLOG05-3140 (21) Byte28 = 38/58
SSBLOG05-3260 (22) Byte28 = 39/59
SSBLOG05-3380 (23) Byte28 = 3A/5A

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SSBLOG05-3500 • Byte27 = 89 & Byte0D Bit2 = 1 (MAIN Blade CHK2)
SSBLOG05-3510 Byte27 = 89 (MAIN Blade CHK2) Byte28-31 Detail
SSBLOG05-3510 (1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15
SSBLOG05-3520 (2) Byte28 = 08/0c/18/1c
SSBLOG05-3530 Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail
SSBLOG05-3530 (1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15
SSBLOG05-3570 (2) Byte28 = 08/0c/18/1c
SSBLOG05-3610 • Byte27 = 8B (DRR CHK2)
SSBLOG05-3620 Byte27 = 8B (DRR CHK2) Byte28-31 Detail
SSBLOG05-3620 (1) Byte28 = 00/01/02/03/10/11/12/13
SSBLOG05-3630 (2) Byte28 = 08/0c/18/1c
SSBLOG05-3640 Byte27 = 8B (DRR CHK2) Byte40-7F Detail
SSBLOG05-3640 (1) Byte28 = 00/01/02/03/10/11/12/13
SSBLOG05-3680 (2) Byte28 = 08/0c/18/1c
SSBLOG05-3720 • Byte27 = 8C (SVP Detected Failure : SVP(PC))
SSBLOG05-3740 Byte27 = 8C (SVP Detected Failure : SVP(PC)) error information detailed
SSBLOG05-3740 (1) Logical inconsistency / HEAP / File / LAN / Windows failure / SVP forced reboot or maintenance failure / Router failure / Disable SVP reboot / Stop SSB overwrite / Stop SSBS overwrite / Flash memory failure / Battery failure / Delay of time / Warning of a stack / Single task error / SVP launcher error / SVP reboot / SVP reboot (WSAENOBUF) / IP address setting error / Subnet mask setting error / Virus detection error / SVP environment error / Situation observation error / Dummy PS/Off starting (normal)
SSBLOG05-3760 (2) CUDG detected error
SSBLOG05-3800 (3) BOOT detected error

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SSBLOG05-3860 • Byte27 = 8E (CHK1)
SSBLOG05-3860 Byte27 = 8E (CHK1) Byte28-31 Detail
SSBLOG05-3860 (1) Byte28 = 20
SSBLOG05-3870 (2) Byte28 = 21
SSBLOG05-3880 (3) Byte28 = 22/23/24/25
SSBLOG05-3890 (4) Byte28 = 30
SSBLOG05-3900 (5) Byte28 = 40
SSBLOG05-3910 (6) Byte28 = 41/42/43
SSBLOG05-3920 (7) Byte28 = 44/45
SSBLOG05-3930 (8) Byte28 = 47
SSBLOG05-3940 (9) Byte28 = 50/51/52
SSBLOG05-3950 (10) Byte28 = 60/61/62/63/64/65/66/67/68
SSBLOG05-3960 (11) Byte28 = 80/81
SSBLOG05-3970 Byte27 = 8E (CHK1) Byte40-7F Detail
SSBLOG05-3970 (1) Byte28 = 20/40
SSBLOG05-4000 (2) Byte28 = 21
SSBLOG05-4030 (3) Byte28 = 22/23/24/25
SSBLOG05-4060 (4) Byte28 = 30
SSBLOG05-4090 (5) Byte28 = 41/43/47/51/52
SSBLOG05-4120 (6) Byte28 = 42/50
SSBLOG05-4150 (7) Byte28 = 44/45
SSBLOG05-4180 (8) Byte28 = 60
SSBLOG05-4220 (9) Byte28 = 61
SSBLOG05-4260 (10) Byte28 = 62
SSBLOG05-4300 (11) Byte28 = 63
SSBLOG05-4340 (12) Byte28 = 64
SSBLOG05-4380 (13) Byte28 = 65
SSBLOG05-4420 (14) Byte28 = 66
SSBLOG05-4460 (15) Byte28 = 67
SSBLOG05-4500 (16) Byte28 = 68
SSBLOG05-4540 (17) Byte28 = 80/81
SSBLOG05-4570 • Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (WCHK1)
SSBLOG05-4580 Byte27 = 8E & Byte34:bit4-7=5 (CHK1B Reset)
SSBLOG05-4580 Byte27 = 81 & Byte34:bit4-7=3 (CHK3 Reset)
SSBLOG05-4580 Byte27 = 84 & Byte34:bit4-7=5 (CHK4 Reset)
SSBLOG05-4610 Byte27 = 8E & Byte34:bit4-7=6 (DKC Internal Reset)
SSBLOG05-4640 Byte27 = 8E & Byte34:bit4-7=8 (Force Reset)
SSBLOG05-4660 Byte27 = 8E & Byte34:bit4-7=9 (Logical Inconsistency Reset)
SSBLOG05-4680 • Byte27 = 8F (Logical Inconsistency)
SSBLOG05-4700 • Byte27 = 9F (Trace data/Log data)
SSBLOG05-4730 • Byte27 = EC (Environment Monitor Detected Failure : Controller Environment Failure)
SSBLOG05-4760 • Byte27 = EE (Environment Monitor Detected DB Failure)

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SSBLOG05-4790 • Byte27 = F1 (Micro-program Detected Cache Failure)
SSBLOG05-4810 • Byte27 = F2 (CACHE ERR)
SSBLOG05-4820 Byte27 = F2 (CACHE ERR) Byte28-2C, 30 Detail
SSBLOG05-4830 Byte27 = F2 (CACHE ERR) Byte40-47 Detail
SSBLOG05-4830 (1) Byte30 = x‘10’ : MPDMA(W1) error status
SSBLOG05-4840 (2) Byte30 = x‘30’ , x‘40’ , x‘50’ , x‘60’ , x‘70’ , x‘80’ : DMA(W2) error status
SSBLOG05-4850 (3) Byte30 = x‘90’, x‘A0’, x‘B0’, x‘C0’: DRR(W2) error status
SSBLOG05-4860 Byte27 = F2 (CACHE ERR) Byte50-5F Detail
SSBLOG05-4870 Byte27 = F2 (CACHE ERR) Byte60-7F Detail
SSBLOG05-4870 (1) If Byte50:(b2= ‘1’ or b3=‘1’) then CM00 or CM01 error
SSBLOG05-4870 (2) If Byte51:(b2= ‘1’ or b3=‘1’) then CM10 or CM11 error
SSBLOG05-4870 (3) If Byte52:(b2= ‘1’ or b3=‘1’) then CM20 or CM21 error
SSBLOG05-4870 (4) If Byte53:(b2= ‘1’ or b3=‘1’) then CM30 or CM31 error
SSBLOG05-4880 • Byte27 = F5 (Remote Copy Paths Removed / Restored)
SSBLOG05-4900 • Byte27 = FA (NVS Terminated)
SSBLOG05-4920 • Byte27 = FB (TrueCopy for Pair suspend)
SSBLOG05-4940 • Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support)
SSBLOG05-4950 Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information
SSBLOG05-4950 (1) Byte28 = 02 : Cache Memory correctable error
SSBLOG05-4970 (2) Byte28 = 84 : HMA correctable error
SSBLOG05-4990 (3) Byte28 = 40 : Abnormal DC Voltage control warning
SSBLOG05-5000 (4) Byte28 = 41 : Abnormal CEMODE warning
SSBLOG05-5010 (5) Byte28 = 42 : Abnormal CEDT warning
SSBLOG05-5020 (6) Byte28 = C0 : SFP (Tachyon) warning
SSBLOG05-5040 (7) Byte28 = 45 : Battery warning
SSBLOG05-5070 (8) Byte28 = 46 : CFM warning
SSBLOG05-5100 (9) Byte28 = 48 : MPPK Abnormal temperature warning
SSBLOG05-5110 (10) Byte28 = 49 : PK Abnormal temperature warning
SSBLOG05-5130 (11) Byte28 = 43 : Forced volatile reboot warning
SSBLOG05-5140 (12) Byte28 = 47 : CFM Config warning
SSBLOG05-5170 (13) Byte28 = 4A : MAIN Blade FAN warning

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SSBLOG05-5200	• Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 81/82/84 (FPC Detected Failure)
SSBLOG05-5230	• Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 83 (Drive Detected Failure)
SSBLOG05-5250	• Byte36: bit0-3 = E & Byte26: bit4-7 = 1 (Drive Detected Failure)
SSBLOG05-5270	• Byte26: b4-7 = F & Byte3C = F1 (DKC SIM)
SSBLOG05-5300	• Byte26: b4-7 = F & Byte3C = F2 (CACHE SIM)
SSBLOG05-5330	• Byte26: b4-7 = F & Byte3C = FE (Device SIM)
SSBLOG05-5350	• Byte26: b4-7 = F & Byte3C = FF (MEDIA SIM)

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1. Introduction

The internal SSB information is presented as either 24-byte compatibility SSB format or 32-byte SSB format.The internal SSB is divided into the following 3 sections:

(1) Internal SSB common information
This 32 byte information is used for SSB management, and same for all formats.

(2) Format-dependent information
This is 32 bytes information defined by format of 128 byte internal SSB information .

(3) Internal SSB individual information
This is 64 byte information, and package format is free. This information is supplementary set, When error information of format-dependent information is not enough .

NOTE: The byte offset in SSB logs is described in hexadecimal number.

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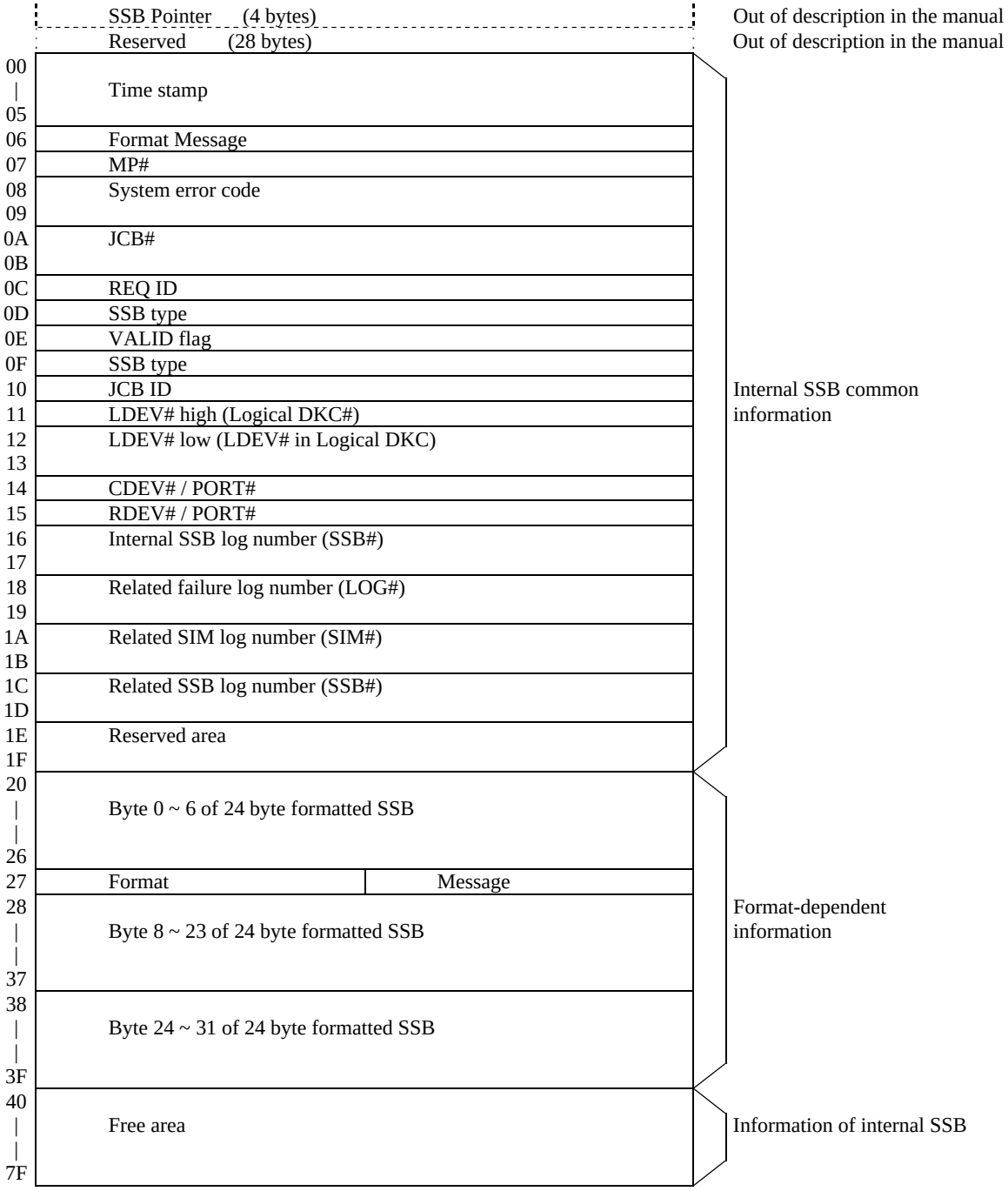

Fig. 1-1 Outline of 24-byte Format Internal SSB

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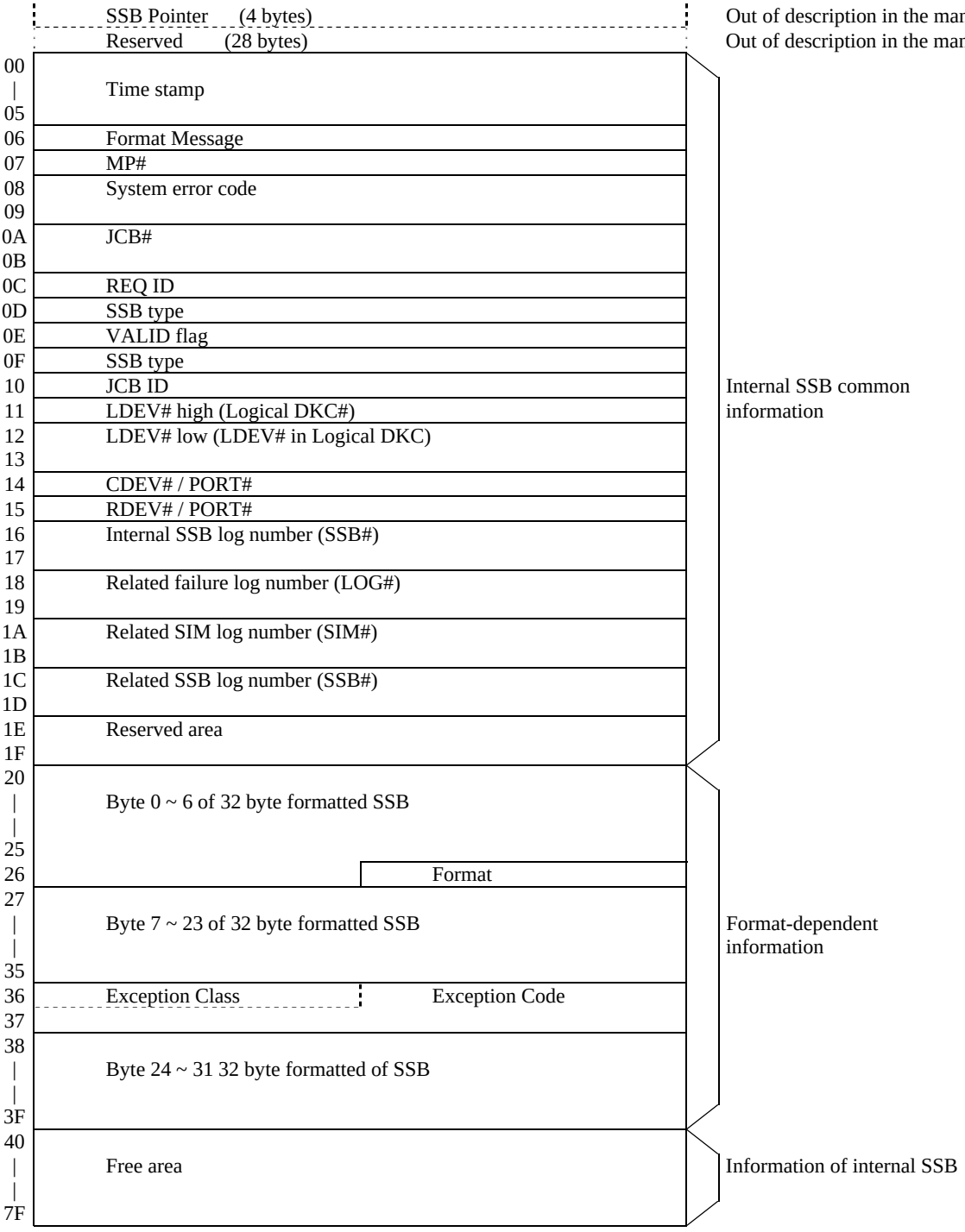

Fig. 1-2 Outline of 32-byte Format Internal SSB

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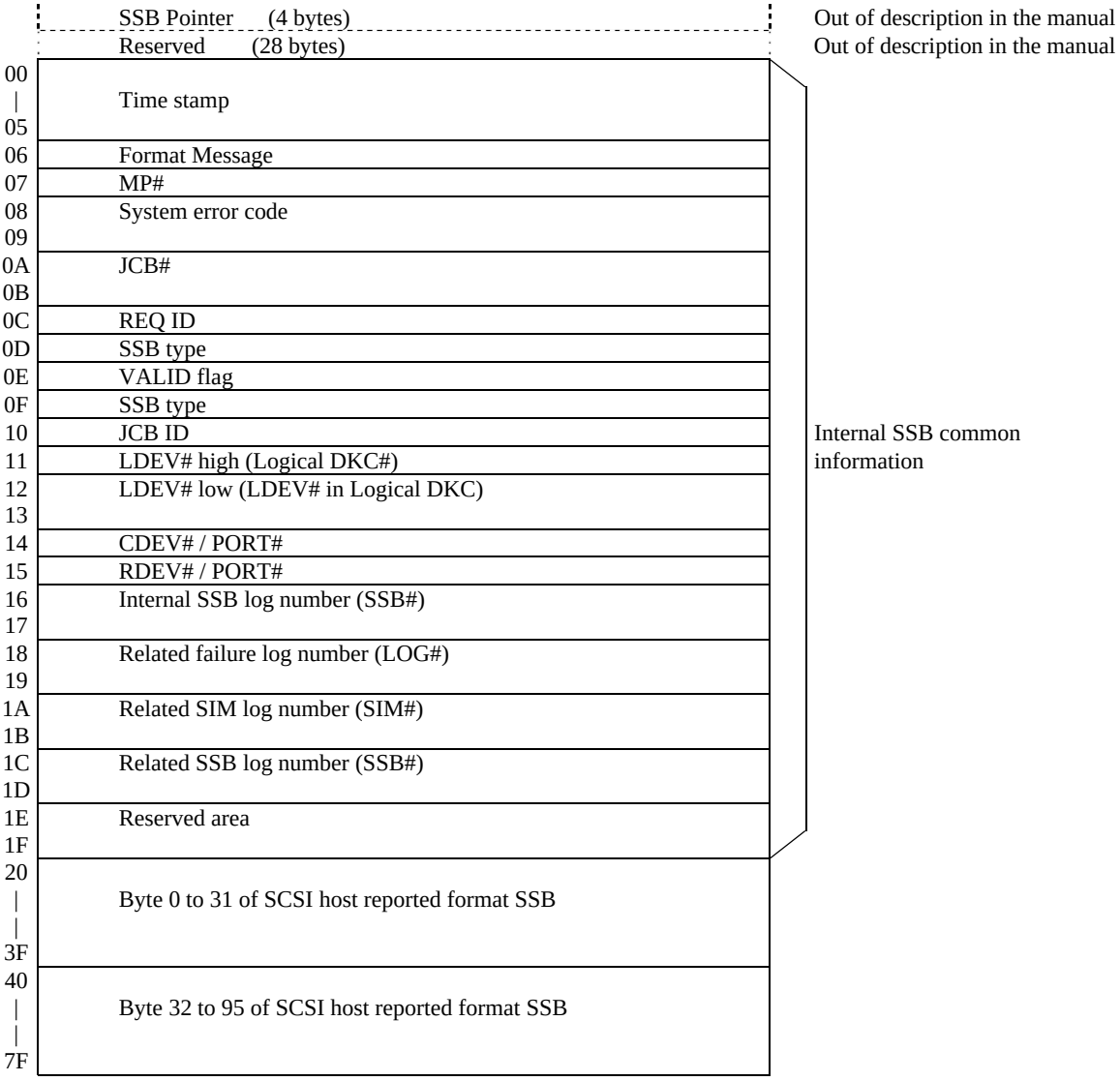

Fig. 1-3 Overview of SCSI Host Report Format Internal SSB

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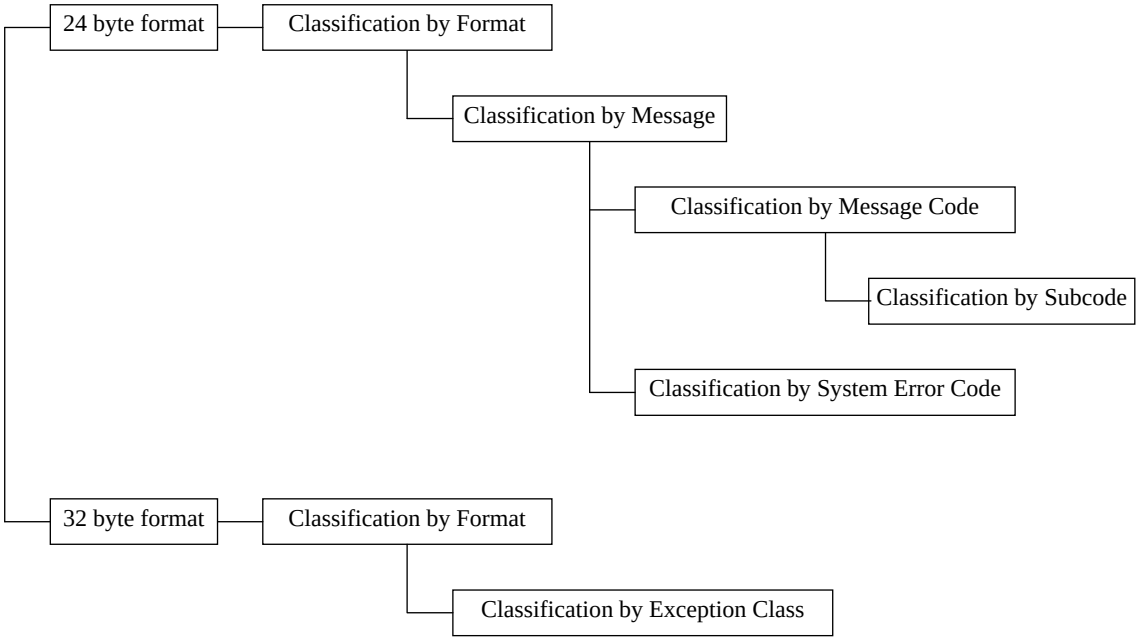
2. Classification of Internal SSB

The internal SSB is devided roughly into 24 byte format and 32 byte format. The further classification (The search method for SSB table) is shown Fig. 2-1.

The outline is below.



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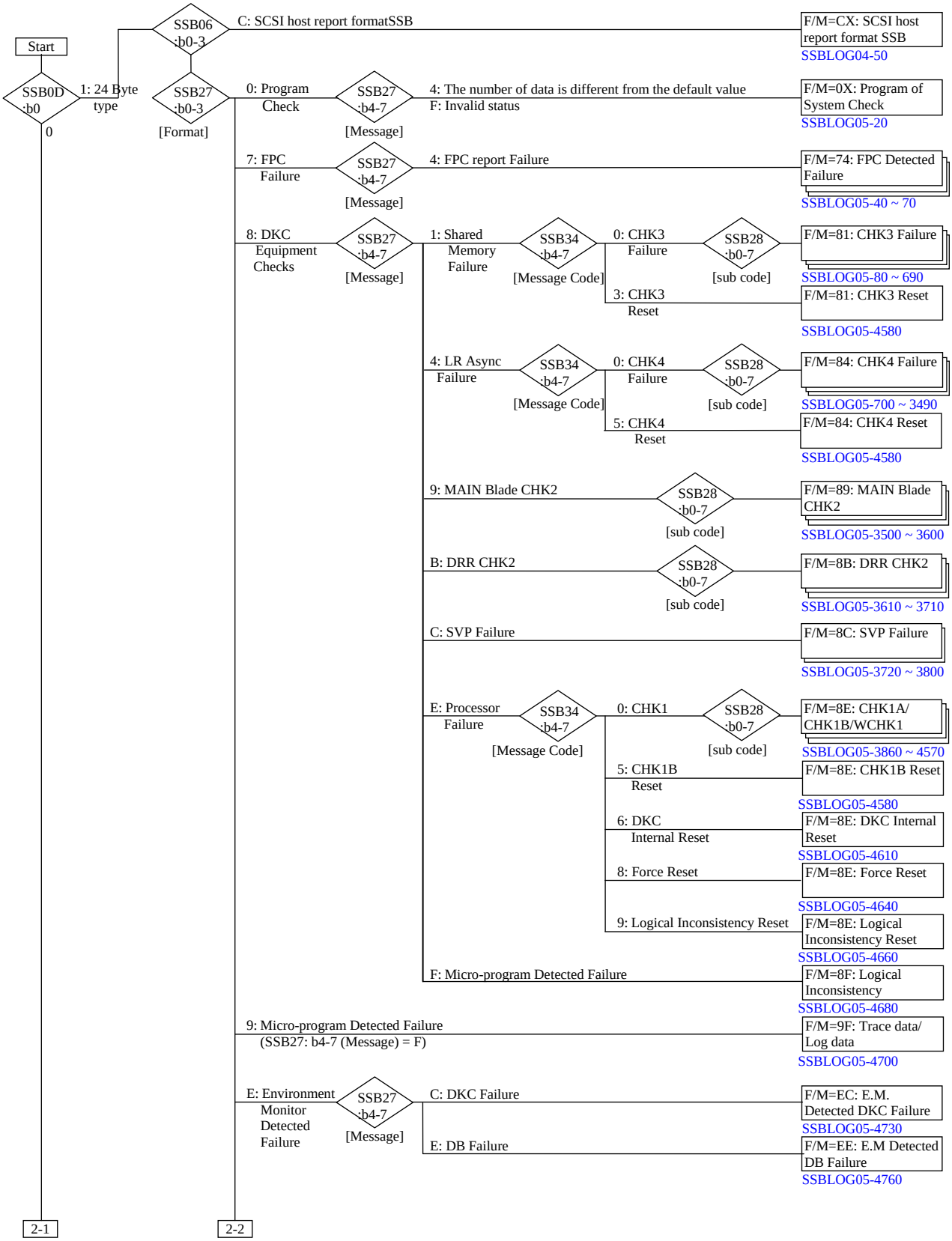

Fig. 2-1 Search method for SSB tables (1/2)

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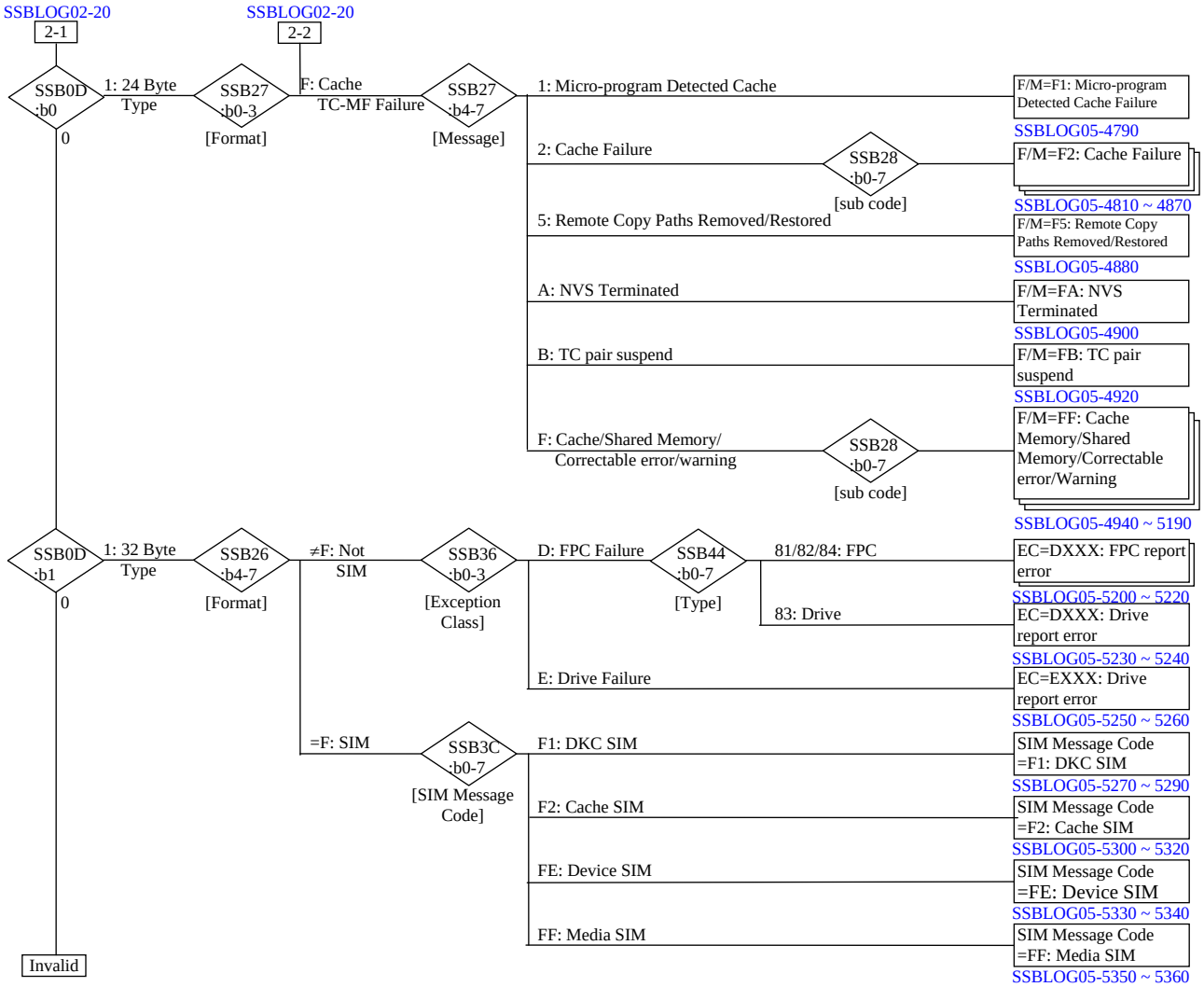

Fig. 2-1 Search method for SSB tables (2/2)

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3. Common information description

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	No Display log
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Format-Dependent Information							
3F								
40	Internal SSB Information							
7F								

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Common Information (1/2)

Byte	Bit	Meaning	Remarks
00 ~ 05		Time stamp The time error occurred (The time maked internal SSB)	
06		Format Message	
07		Processor number (Internal ID) x‘00’ ~ x‘0F’	
08 ~ 09		System error code	
	0 ~ 7	Module ID	
	8 ~ 15	Routine ID	
0A ~ 0B		JCB#	
0C		REQ ID	
0D		SSB type	
	0	24 byte type flag 0: Invalid 1: 24 byte type SSB	
	1	32 byte type flag 0: Invalid 1: 32 byte type SSB	
	2	Flag for SCSI host processor detected the error 0: Invalid 1: SSB detected by SCSI host processor	
	3	Remote copy flag 0: Invalid 1: Remote copy valid	
	4	Separately stored log flag 0: General log 1: Separately stored log	
	5	Host report flag 0: Pending 1: Reported	
	6	SVP report flag 0: Pending 1: Reported	
	7	Forcible log flag 0: Normal 1: Forcibly ejected log (store in DKC beyond a definite period of time)	
0E		Valid flag	
	0	LDEV number valid or invalid 0: Invalid 1: Valid	
	1	PDEV number valid or invalid 0: Invalid 1: Valid	
	2	SSB number valid or invalid 0: Invalid 1: Valid	
	3	Related failure log number valid or invalid 0: Invalid 1: Valid	

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Common Information (2/2)

Byte	Bit	Meaning	Remarks
0E		Valid flag	
	4	Related SIM log number valid or invalid 0: Invalid 1: Valid	
	5	Related SSB log number valid or invalid 0: Invalid 1: Valid	
	6	PK information valid or invalid 0: Invalid 1: Valid	
	7	No display log valid or invalid 0: Display log 1: No display log	
0F		SSB type	
	0	Reserved	
	1	RCU SIM flag 0: Invalid 1: RCU SIM flag	
	2	PORT number valid or invalid 0: Valid 1: Invalid	
	3 ~ 7	Reserved	
10		JCB ID	
11		LDEV# high (Logical DKC#)	
12 ~ 13		LDEV# low (LDEV# in Logical DKC)	
14		CDEV# / PORT#	
15		RDEV# / PORT#	
16 ~ 17		Internal SSB log number	
18 ~ 19		Related Failure log number	
1A ~ 1B		Related SIM log number	
1C ~ 1D		Related SSB log number	
1E ~ 1F		Reserved area	

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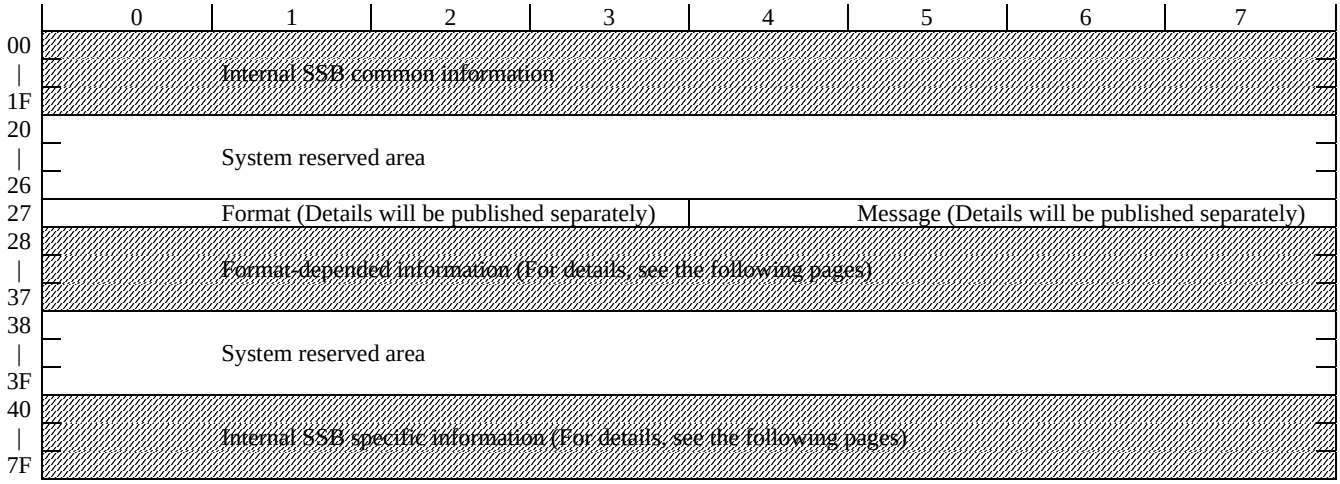
4. Host SSB information and internal SSB format-depended information description

4.1 24-byte type SSB



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Format and Message

Format	Message	Meaning
0 (Program/ System check)	0 ~ 3	Not used
	4	The number of data is different from the default value
	5 ~ E	Not used
	F	Invalid status
1 ~ 6	0 ~ F	Not used
7	0 ~ 3	Not used
	4	FPC report error
	5 ~ F	Not used
8	0	Not used
	1	Shared memory failure
	2 ~ 3	Not used
	4	IFB failure
	5 ~ 8	Not used
	9	MAIN Blade failure
	A	Not used
	B	DRR failure
	C	SVP failure
	D	Power failure
	E	Processor failure
	F	Micro-program detected error (Logical Inconsistency)
9	0 ~ E	Not used
	F	Micro-program detected error (Trace data/Log data)
E	0 ~ B	Not used
	C	Environmental monitor detected DKC failure
	D	Not used
	E	Environmental monitor detected DB failure
	F	Not used
F	0	Not used
	1	Micro-program detected cache failure
	2	Cache failure
	3 ~ 4	Not used
	5	Remote Copy Paths Removed/Restored
	6 ~ 9	Not used
	A	NVS terminated
	B	TrueCopy for Mainframe Pair suspend
	C ~ E	Not used
	F	Cache/SFP/HMA warning

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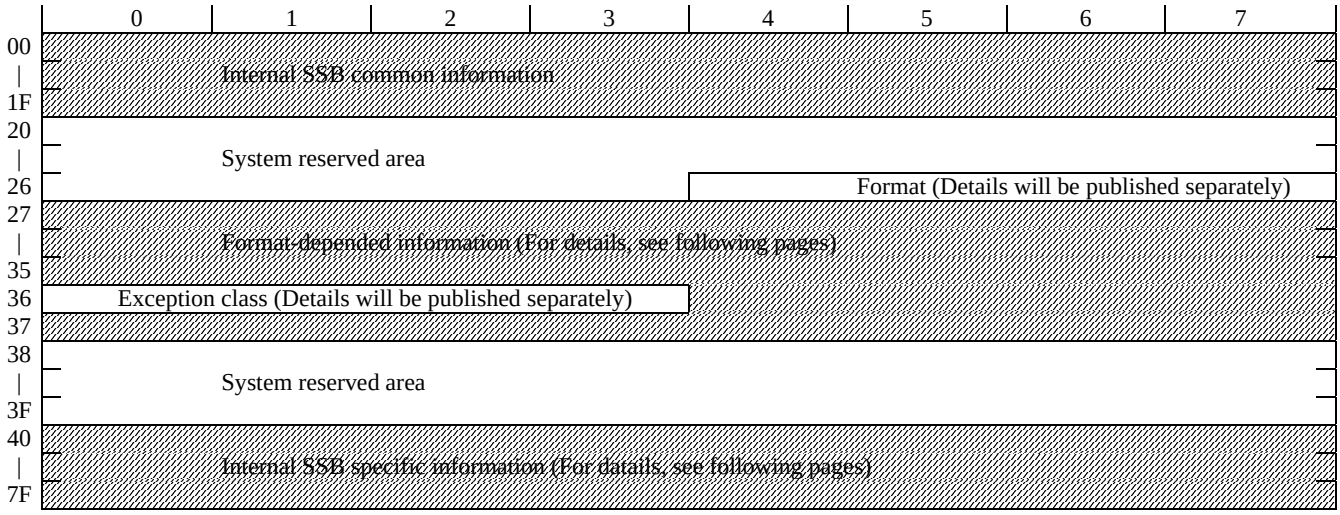
4.2 32-byte type SSB



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Exception Class (Byte36: bit0-3) and Format (Byte26: bit4-7)

Exception class	Format	Meaning
0	0 ~ F	Not used
2	0 ~ E	Not used
	F	DKC SIM
3	0 ~ E	Not used
	F	DKC SIM
4	0 ~ E	Not used
	F	Media SIM
5	0 ~ E	Not used
	F	DEVICE SIM/Media SIM (ORM detected)
6	2 ~ F	Not used
C	0 ~ E	Not used
	F	DKC SIM
D	0	Not used
	1	FPC report error / Drive report error
	0 ~ E	Not used
	F	DKC SIM
E	0	Not used
	1	Drive report error
	2 ~ E	Not used
	F	DEVICE SIM
F	0 ~ E	Not used
	F	DKC SIM/CACHE SIM

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4.3 SCSI host report format SSB

	0	1	2	3	4	5	6	7
00 | 1F	Internal SSB common information (*1)							
20	Information byte valid	Error code (0x7)						
21	Segment No (0)							
22	File mark (0)	ECM (0)	ILI (0)	Not used	Sense key			
23 | 26	Information byte							
27	Additional sense data length (0x58)							
28 | 2B	Command specific information							
2C 2D	Sense code							
2E	Field Replaceable Unit (0)							
2F	Sense key specific information	Sense key specific information						
30 31								
32 | 7F	Additional sense data valid	Additional sense data						

*1: 0xCX (X=sense key) is set to byte 7 (log type low-order byte). SSB on SVP is indicated as F/M=CX.

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Details of SCSI host report format SSB information

Byte	Bit	Description	Setting	Remarks
20	0	Information byte valid/invalid 0: Invalid 1: Valid	OPEN command Control	
	1 ~ 7	Error code (0x7) Indicates an I/O process error.		
21		Segment No. (0)		
22	0	File Mark (0)		
	1	ECM (0)		
	2	ILI (0)		
	3	No use		
	4 ~ 7	Sense key: For more details, see “sense keys list”.		
23 ~ 26		Information bytes: LBA related to sense key if information byte is valid.		
27		Additional sense data length (0x58) Indicates sense data length after byte 8 or later.		
28 ~ 2B		Command specific information		
2C ~ 2D		Sense codes: For more details, see “sense codes list”.		
2E		Field Replaceable Unit (0)		
2F ~ 31	0	Sense key specific information valid/invalid 0: Invalid 1: Valid		
	1 ~ 17	Sense key specific information		
32 ~ 7F	0	Additional sense data valid/invalid 0: Invalid 1: Valid	Error detection source	
	1 ~ END	Additional sense data		

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Sense Keys List

Sense key	Description
0	NO SENSE
1	RECOVERED ERROR
2	NOT READY
3	MEDIUM ERROR
4	HARDWARE ERROR
5	ILLIGAL REQUEST
6	UNIT ATTENTION
7	DATA PROTECT
8	BLANK CHECK (No use)
9	VENDER UNIQUE
A	COPY ABORTED
B	ABORTED COMMAND
C	EQUAL (No use)
D	VOLUME OVERFLOW
E	MISCOMPARE
F	(RESERVED)

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5. Format-depended information description

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Byte27 = 04 (The number of data is different from the default value) / 0F (Invalid status) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Hostreport	SVP report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘0’)				Message (x‘X’ : X ≠ 8/A)			
28	Command code (for F/M ≠ 0F) / Reason code (for F/M=0F)							
29	Detail failure information 1							
2A								
2B								
2C								
2D	SSID of mate storage system (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID							
31	Routine ID							
32	Package number							
33	Detail failure information 2							
34	SSID of self storage system							
35								
36	Symptom code (x‘0F0X’) (X=Message code)							
37								
38	Log and message congtrol (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 04 (The number of data is different from the default value) / 0F (Invalid status) (2/2)

	0	1	2	3	4	5	6	7
40 | 55	Not used							
56	Module ID (detected the error)							
57	Routine ID (detected the error)							
58 | 7F	Not used							

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Byte27 = 74 & Byte40: Bit7 = 0 (FPC Detected Failure: DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PK type		MP#					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HST REP	HST REP	EXPLS
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘7’)				Message (x‘4’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Not used							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Exception code (x‘DYZZ’) (Y: CDEV number, ZZ: RDEV number)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 74 & Byte40: Bit7 = 0 (FPC Detected Failure: DSP) (2/2)

	0	1	2	3	4	5	6	7
40		SSB edit format (x‘00’)						
41		Not used						
42		CDB information						
|								
|								
4B								
4C		(x‘AB’)						
4D		(x‘CD’)						
4E		CMD BLK#						
4F		Data transfer end flag						
50		I/O status						
51								
52		PDEV status						
53								
54		LOOP status						
55								
56								
57								
58		Frame Manager status						
59								
5A								
5B								
5C		TL status						
5D								
5E								
5F								
60		I/O issued status 1						
61								
62		I/O issued status 2						
63								
64		Not use						
65								
66								
67								
68		JOB require info						
69								
6A								
6B								
6C		Data transfer status						
6D								
6E								
6F								
70		Not used						
|								
|								
7F								

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Byte27 = 74 & Byte40: Bit7 = 1 (FPC Detected Failure: FBP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PK type		MP#					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HST REP	HST REP	EXPLS
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘7’)				Message (x‘4’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Not used							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Exception code (x‘DYZZ’) (Y: CDEV number, ZZ: RDEV number)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 74 & Byte40: Bit7 = 1 (FPC Detected Failure: FBP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format (x'01')							
41	Not used							
42								
43								
44	ERQ index							
45								
46								
47								
48	IMQ index							
49								
4A								
4B								
4C	I/O request information							
4D								
4E								
4F								
50	FPC Config/Control register							
51								
52								
53								
54	FPC Status register							
55								
56								
57								
58	FM Configuration register							
59								
5A								
5B								
5C	FM Status register							
5D								
5E								
5F								
60	FM Link Status1 register							
61								
62								
63								
64	FM Link Status2 register							
65								
66								
67								
68	FCA register 1							
69								
6A								
6B								
6C	FCA register 2							
6D								
6E								
6F								
70	FPC PCI register							
71								
72	AL_PA							
73								
74	FPC Config command							
75								
76								
77								
78	Fibre status							
79								
7A								
7B								
7C	Fibre error outbreak count							
7D								
7E								
7F								

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Byte27 = 81 (CHK3)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM		Reserved				
10	JCB ID							
11	LDEV# (Logical DKC#)							
12	LDEV# (GDEV#)							
13								
14	CDEV#							
15	RDEV#							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘1’)			
28	Subcode (See following pages)							
29	Hardware information (See following pages)							
|								
|								
31								
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	PCB number				Message code (x‘0’)			
35	SSID of self storage system							
36	Symptom code (x‘FF81’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Reserved							
3E								
3F								
40	Hard information (See following pages)							
|								
|								
7F								

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Byte27 = 81 (CHK3) Byte28-31

(1) Byte28 = 00/01/10/11/20/21/22/23/40/41/42/43/50/51/52/53/54/55/58/59/5A/5B/5C/5D/
60/61/62/63/80/81/82/83/84/90/91/A0/A1/A2/A3/F0

	0	1	2	3	4	5	6	7
28	Subcode (x‘00’ or x‘01’ or x‘10’ or x‘11’ or x‘20’ or x‘21’ or x‘22’ or x‘23’ or x‘40’ or x‘41’ or x‘42’ or x‘43’ or x‘50’ or x‘51’ or x‘52’ or x‘53’ or x‘54’ or x‘55’ or x‘58’ or x‘59’ or x‘5A’ or x‘5B’ or x‘5C’ or x‘5D’ or x‘60’ or x‘61’ or x‘62’ or x‘63’ or x‘80’ or x‘81’ or x‘82’ or x‘83’ or x‘84’ or x‘90’ or x‘91’ or x‘A0’ or x‘A1’ or x‘A2’ or x‘A3’ or x‘F0’)							
29	INT0_HMA_STATUS B3							
	Not used	Module Number			CL Number	Not used	Not used	IX Mode
2A	INT0_HMA_STATUS:B1							
	LSI Revision							
2B	LRP_HMA_INFO_TABLE00:B2							
	Not used	Not used	P5 path STATUS	P4 path STATUS	P3 path STATUS	P2 path STATUS	P1 path STATUS	P0 path STATUS
2C	LRP_HMA_INFO_TABLE00:B1							
	CM13 STATUS	CM03 STATUS	CM12 STATUS	CM02 STATUS	CM11 STATUS	CM01 STATUS	CM10 STATUS	CM00 STATUS
2D	LRP_HMA_INFO_TABLE00:B0							
	E1 path STATUS	E0 path STATUS	I1 path STATUS	I0 path STATUS	Not used	Not used	Not used	PON HMA STATUS
2E	INT0_INTSTS0:B3							
	INT CHK1B	LRP4 CHK1B	LRP3-0 CHK1B	SWIF CHK1B	BARB CHK1B	IARB CHK1B	EARB CHK1B	IXARB CHK1B
2F	INT0_INTSTS0:B2							
	PARB CHK1B	XD CHK1B	DXC CHK1B	DXA CHK1B	DRR CHK1B	MPDMA DMAMB CHK1B	DMA CHK1B	RGA CHK1B
30	INT0_INTSTS0:B1							
	FMT CHK1B	BRAM BCOM SH CHK1B	SMC CHK1B	SMBUS CHK1B	CHK4	CHK3	CHK2	WARN
31	INT0_INTSTS0:B0							
	Not used	Not used	MBOX INT	LRP4 INT	LRP3 INT	LRP2 INT	LRP1 INT	LRP0 INT

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Byte27 = 81 (CHK3) Byte40-7F Detail
(1) Byte28 = 80 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	SMC_ERRSTS_OWNMP:B2							
	Not used	E Micro Error	Not used	Not used	Not used	X CPLError	D CPLError	E CPLError
45	SMC_ERRSTS_OWNMP:B0							
	Not used	Not used	Not used	Not used	CRG CHK1	X CHK1	D CHK1	E CHK1
46	SMC_ERRSTS_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	X Warning	D Warning	E Warning
47	SMC_ERRSTS_OWNMP:B6							
	Not used	Not used	Not used	Not used	Not used	X Slave Error	D Slave Error	E Slave Error
48	SMC_CHK3_ERRLOG_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	ECTL NP MULTI Micro Error	ECTL BNDRY Error	ECTL INVDST Error
49	SMC_CHK3_ERRLOG_OWNMP:B6							
	ECTL PREGWT Micro Error	ECTL INDWT Micro Error	ECTL INDRD Micro Error	ECTL ATM Micro Error	ECTL INV CMD Error	ECTL PCODE Error	ECTL SM ACC Error	ECTL ADR INV Error
4A	SMC_CHK3_ERRLOG_OWNMP:B5							
	Not used	Not used	Not used	Not used	Not used	XCTL AUTOCHK TOV Error	XCTL WTCHKRD Error	XCTL AUTOCHK Error
4B	SMC_CHK3_ERRLOG_OWNMP:B4							
	XCTL AUTOCHK STS Error	Not used	Not used	XCTL MERSTS X Error	XCTL ErrorSTS X Error	XCTL CPL TOV Error	XCTL CPL FRCTOV Error	XCTL CPL STS Error
4C	SMC_CHK3_ERRLOG_OWNMP:B3							
	Not used	Not used	Not used	Not used	DCTL AUTOCHK TOV Error	Not used	DCTL WTCHKRD Error	DCTL AUTOCHK Error
4D	SMC_CHK3_ERRLOG_OWNMP:B2							
	DCTL AUTOCHK STS Error	Not used	Not used	Not used	Not used	DCTL CPL FRCTOV Error	DCTL CPL TOV Error	DCTL CPL STS Error
4E	SMC_CHK3_ERRLOG_OWNMP:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4F	SMC_CHK3_ERRLOG_OWNMP:B0							
	Not used	Not used	Not used	Not used	Not used	ECTL CPL FRCTOV Error	ECTL CPL TOV Error	ECTL CPL STS Error

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Byte27 = 81 (CHK3) Byte40-7F Detail
(1) Byte28 = 80 (2/4)

	0	1	2	3	4	5	6	7
50	SMC_ECTL_DSTADR_LOG:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ErrorLog FLG
51	SMC_ECTL_DSTADR_LOG:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
52	SMC_ECTL_DSTADR_LOG:B5							
	Destination Address ACC			Destination Address IX	Destination Address MDL			
53	SMC_ECTL_DSTADR_LOG:B4							
	Destination Address [B4]							
54	SMC_ECTL_DSTADR_LOG:B3							
	Destination Address [B3]							
55	SMC_ECTL_DSTADR_LOG:B2							
	Destination Address [B2]							
56	SMC_ECTL_DSTADR_LOG:B1							
	Destination Address [B1]							
57	SMC_ECTL_DSTADR_LOG:B0							
	Destination Address [B0]							
58	SMC_ECTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
59	SMC_ECTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
5A	SMC_ECTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
5B	SMC_ECTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
5C	SMC_ECTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
5D	SMC_ECTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
5E	SMC_ECTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
5F	SMC_ECTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(1) Byte28 = 80 (3/4)

	0	1	2	3	4	5	6	7
60	SMC_ECTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
61	SMC_ECTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
62	SMC_ECTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
63	SMC_ECTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
64	SMC_ECTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
65	SMC_ECTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
66	SMC_ECTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
67	SMC_ECTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							
68	SMC_ECTL_DAT_LOG:B7							
	Data Log [B7]							
69	SMC_ECTL_DAT_LOG:B6							
	Data Log [B6]							
6A	SMC_ECTL_DAT_LOG:B5							
	Data Log [B5]							
6B	SMC_ECTL_DAT_LOG:B4							
	Data Log [B4]							
6C	SMC_ECTL_DAT_LOG:B3							
	Data Log [B3]							
6D	SMC_ECTL_DAT_LOG:B2							
	Data Log [B2]							
6E	SMC_ECTL_DAT_LOG:B1							
	Data Log [B1]							
6F	SMC_ECTL_DAT_LOG:B0							
	Data Log [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(1) Byte28 = 80 (4/4)

	0	1	2	3	4	5	6	7
70	SMC_DCTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
71	SMC_DCTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
72	SMC_DCTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
73	SMC_DCTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
74	SMC_DCTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
75	SMC_DCTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
76	SMC_DCTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
77	SMC_DCTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							
78	SMC_DCTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
79	SMC_DCTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
7A	SMC_DCTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
7B	SMC_DCTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
7C	SMC_DCTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
7D	SMC_DCTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
7E	SMC_DCTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
7F	SMC_DCTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(2) Byte28 = 81 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 Error NO5 REPAFEINT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	MPDMA_MD_ENABLE:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	MPDMA_MD_ENABLE:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	MPDMA_MD_ENABLE:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
47	MPDMA_MD_ENABLE:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DMA EN
48	MPDMA_MD_REPAFE:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
49	MPDMA_MD_REPAFE:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO6 REPAFE	Error NO5 REPAFE
4A	MPDMA_MD_REPAFE:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Error NO4 REPAFE
4B	MPDMA_MD_REPAFE:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO2 REPAFE	Error NO1 REPAFE
4C	MPDMA_MD_STS_W5_LOG:B3							
	STS W5 Log							
4D	MPDMA_MD_STS_W5_LOG:B2							
	STS W5 Log							
4E	MPDMA_MD_STS_W5_LOG:B1							
	STS W5 Log							
4F	MPDMA_MD_STS_W5_LOG:B0							
	STS W5 Log							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(2) Byte28 = 81 (2/4)

	0	1	2	3	4	5	6	7
50	MPDMA_MD_ERR_ST09:B3							
	STS W1 Error2							
51	MPDMA_MD_ERR_ST09:B2							
	STS W1 Error2							
52	MPDMA_MD_ERR_ST09:B1							
	STS W1 Error2							
53	MPDMA_MD_ERR_ST09:B0							
	STS W1 Error2							
54	MPDMA_MD_ERR_ST10:B3							
	STS W1 Error2							
55	MPDMA_MD_ERR_ST10:B2							
	STS W1 Error2							
56	MPDMA_MD_ERR_ST10:B1							
	STS W1 Error2							
57	MPDMA_MD_ERR_ST10:B0							
	STS W1 Error2							
58	MPDMA_MD_ERR_ST11:B3							
	STS W1 Error3							
59	MPDMA_MD_ERR_ST11:B2							
	STS W1 Error3							
5A	MPDMA_MD_ERR_ST11:B1							
	STS W1 Error3							
5B	MPDMA_MD_ERR_ST11:B0							
	STS W1 Error3							
5C	MPDMA_MD_ERR_ST12:B3							
	STS W1 Error3							
5D	MPDMA_MD_ERR_ST12:B2							
	STS W1 Error3							
5E	MPDMA_MD_ERR_ST12:B1							
	STS W1 Error3							
5F	MPDMA_MD_ERR_ST12:B0							
	STS W1 Error3							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(2) Byte28 = 81 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	Reserved							
61	Reserved							
	Reserved							
62	Reserved							
	Reserved							
63	Reserved							
	Reserved							
64	Reserved							
	Reserved							
65	Reserved							
	Reserved							
66	Reserved							
	Reserved							
67	Reserved							
	Reserved							
68	Reserved							
	Reserved							
69	Reserved							
	Reserved							
6A	Reserved							
	Reserved							
6B	Reserved							
	Reserved							
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(2) Byte28 = 81 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(3) Byte28 = 82 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	DXC_REP_ERROR ::DXC0 :B3							
	LOG-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
45	DXC_REP_ERROR ::DXC1 :B3							
	LOG-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
46	DXC_REP_ERROR ::DXC2 :B3							
	LOG-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
47	DXC_REP_ERROR ::DXC3 :B3							
	LOG-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
48	DXC_ERROR_1 ::DXC0 :B3							
	LENGTH OVER	BE Error	AREA Error	STEP OVER	CMD Error	ACC Error	SMC Error	Not used
49	DXC_ERROR_1 ::DXC0 :B2							
	ACC DIMM0 Error	ACC DIMM1 Error	Not used	ACC REFRDY Error	Not used	Not used	Not used	WLST Error
4A	DXC_ERROR_1 ::DXC1 :B3							
	LENGTH OVER	BE Error	AREA Error	STEP OVER	CMD Error	ACC Error	SMC Error	Not used
4B	DXC_ERROR_1 ::DXC1 :B2							
	ACC DIMM0 Error	ACC DIMM1 Error	Not used	ACC REFRDY Error	Not used	Not used	Not used	WLST Error
4C	DXC_ERROR_1 ::DXC2 :B3							
	LENGTH OVER	BE Error	AREA Error	STEP OVER	CMD Error	ACC Error	SMC Error	Not used
4D	DXC_ERROR_1 ::DXC2 :B2							
	ACC DIMM0 Error	ACC DIMM1 Error	Not used	ACC REFRDY Error	Not used	Not used	Not used	WLST Error
4E	DXC_ERROR_1 ::DXC3 :B3							
	LENGTH OVER	BE Error	AREA Error	STEP OVER	CMD Error	ACC Error	SMC Error	Not used
4F	DXC_ERROR_1 ::DXC3 :B2							
	ACC DIMM0 Error	ACC DIMM1 Error	Not used	ACC REFRDY Error	Not used	Not used	Not used	WLST Error

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Byte27 = 81 (CHK3) Byte40-7F Detail
(3) Byte28 = 82 (2/4)

	0	1	2	3	4	5	6	7
50	DXC_SMC_ERR_LOG0 ::DXC0 :B3							
	SMC Error1							
51	DXC_SMC_ERR_LOG0 ::DXC0 :B2							
	SMC Error1							
52	DXC_SMC_ERR_LOG0 ::DXC0 :B1							
	SMC Error0							
53	DXC_SMC_ERR_LOG0 ::DXC0 :B0							
	SMC Error0							
54	DXC_LRP_ERR_LOG0 ::DXC0 :B3							
	Not used	Not used	Not used	LRP Error1				
55	DXC_LRP_ERR_LOG0 ::DXC0 :B2							
	Not used	Not used	Not used	LRP Error1				
56	DXC_LRP_ERR_LOG0 ::DXC0 :B1							
	Not used	Not used	Not used	LRP Error0				
57	DXC_LRP_ERR_LOG0 ::DXC0 :B0							
	Not used	Not used	Not used	LRP Error0				
58	DXC_XD_ERR_LOG ::DXC0 :B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
59	DXC_XD_ERR_LOG ::DXC0 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5A	DXC_XD_ERR_LOG ::DXC0 :B1							
	XD Error							
5B	DXC_XD_ERR_LOG ::DXC0 :B0							
	XD Error							
5C	DXC_SMC_ERR_LOG0 ::DXC1 :B3							
	SMC Error1							
5D	DXC_SMC_ERR_LOG0 ::DXC1 :B2							
	SMC Error1							
5E	DXC_SMC_ERR_LOG0 ::DXC1 :B1							
	SMC Error0							
5F	DXC_SMC_ERR_LOG0 ::DXC1 :B0							
	SMC Error0							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(3) Byte28 = 82 (3/4)

	0	1	2	3	4	5	6	7
60	DXC_LRP_ERR_LOG0 ::DXC1 :B3							
	Not used	Not used	Not used	LRP Error1				
61	DXC_LRP_ERR_LOG0 ::DXC1 :B2							
	Not used	Not used	Not used	LRP Error1				
62	DXC_LRP_ERR_LOG0 ::DXC1 :B1							
	Not used	Not used	Not used	LRP Error0				
63	DXC_LRP_ERR_LOG0 ::DXC1 :B0							
	Not used	Not used	Not used	LRP Error0				
64	DXC_XD_ERR_LOG ::DXC1 :B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	DXC_XD_ERR_LOG ::DXC1 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	DXC_XD_ERR_LOG ::DXC1 :B1							
	XD Error							
67	DXC_XD_ERR_LOG ::DXC1 :B0							
	XD Error							
68	DXC_SMC_ERR_LOG0 ::DXC2 :B3							
	SMC Error1							
69	DXC_SMC_ERR_LOG0 ::DXC2 :B2							
	SMC Error1							
6A	DXC_SMC_ERR_LOG0 ::DXC2 :B1							
	SMC Error0							
6B	DXC_SMC_ERR_LOG0 ::DXC2 :B0							
	SMC Error0							
6C	DXC_LRP_ERR_LOG0 ::DXC2 :B3							
	Not used	Not used	Not used	LRP Error1				
6D	DXC_LRP_ERR_LOG0 ::DXC2 :B2							
	Not used	Not used	Not used	LRP Error1				
6E	DXC_LRP_ERR_LOG0 ::DXC2 :B1							
	Not used	Not used	Not used	LRP Error0				
6F	DXC_LRP_ERR_LOG0 ::DXC2 :B0							
	Not used	Not used	Not used	LRP Error0				

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Byte27 = 81 (CHK3) Byte40-7F Detail
(3) Byte28 = 82 (4/4)

	0	1	2	3	4	5	6	7
70	DXC_XD_ERR_LOG ::DXC2 :B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	DXC_XD_ERR_LOG ::DXC2 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	DXC_XD_ERR_LOG ::DXC2 :B1							
	XD Error							
73	DXC_XD_ERR_LOG ::DXC2 :B0							
	XD Error							
74	DXC_SMC_ERR_LOG0 ::DXC3 :B3							
	SMC Error1							
75	DXC_SMC_ERR_LOG0 ::DXC3 :B2							
	SMC Error1							
76	DXC_SMC_ERR_LOG0 ::DXC3 :B1							
	SMC Error0							
77	DXC_SMC_ERR_LOG0 ::DXC3 :B0							
	SMC Error0							
78	DXC_LRP_ERR_LOG0 ::DXC3 :B3							
	Not used	Not used	Not used	LRP Error1				
79	DXC_LRP_ERR_LOG0 ::DXC3 :B2							
	Not used	Not used	Not used	LRP Error1				
7A	DXC_LRP_ERR_LOG0 ::DXC3 :B1							
	Not used	Not used	Not used	LRP Error0				
7B	DXC_LRP_ERR_LOG0 ::DXC3 :B0							
	Not used	Not used	Not used	LRP Error0				
7C	DXC_XD_ERR_LOG ::DXC3 :B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7D	DXC_XD_ERR_LOG ::DXC3 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7E	DXC_XD_ERR_LOG ::DXC3 :B1							
	XD Error							
7F	DXC_XD_ERR_LOG ::DXC3 :B0							
	XD Error							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(4) Byte28 = 83 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	RGARB_REQGNT_MONI:B3							
	Not used	Not used	STS GNT			Not used	STS GNT	
45	RGARB_REQGNT_MONI:B2							
	STS GNT				Not used	STS GNT		
46	RGARB_REQGNT_MONI:B1							
	Not used	Not used	STS REQ			Not used	STS REQ	
47	RGARB_REQGNT_MONI:B0							
	STS REQ				Not used	STS REQ		
48	RGARB_ACSADR_MONI_CRT:B3							
	ACS REG							
49	RGARB_ACSADR_MONI_CRT:B2							
	ACS REG							
4A	RGARB_ACSADR_MONI_CRT:B1							
	ACS REG							
4B	RGARB_ACSADR_MONI_CRT:B0							
	ACS REG							
4C	RGARB_CHK_LOG_ALL:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	RGARB_CHK_LOG_ALL:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	ALL RXDT PER W RDT	ALL RXDT PER MPNO
4E	RGARB_CHK_LOG_ALL:B1							
	ALL MST REQOFF	ALL RXDT PER Error	ALL RXDT PER FUNC	ALL RXDT PER WRBE	ALL RXDT PER ADR	ALL RXDT PER WDT	ALL RXDT PER RDT	ALL RXDT CMPCHK
4F	RGARB_CHK_LOG_ALL:B0							
	ALL VALID CHK	ALL XR RSV	ALL XR WRBE	ALL PENC GNTZERO	ALL PENC GNTEX	ALL SEQ PTY	ALL SEQ ENC	ALL SEQ DEC

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Byte27 = 81 (CHK3) Byte40-7F Detail
(4) Byte28 = 83 (2/4)

	0	1	2	3	4	5	6	7
50	RGARB_ACSADR_MONI_OLD:B3							
	ACS REG							
51	RGARB_ACSADR_MONI_OLD:B2							
	ACS REG							
52	RGARB_ACSADR_MONI_OLD:B1							
	ACS REG							
53	RGARB_ACSADR_MONI_OLD:B0							
	ACS REG							
54	Reserved							
	Reserved							
55	Reserved							
	Reserved							
56	Reserved							
	Reserved							
57	Reserved							
	Reserved							
58	Reserved							
	Reserved							
59	Reserved							
	Reserved							
5A	Reserved							
	Reserved							
5B	Reserved							
	Reserved							
5C	Reserved							
	Reserved							
5D	Reserved							
	Reserved							
5E	Reserved							
	Reserved							
5F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(4) Byte28 = 83 (3/4)

	0	1	2	3	4	5	6	7
60	XREG_MCERR_ALLLOG:B3							
	RAIF RGARB CMP	RAIF TIMEOUT WT	RAIF TIMEOUT RD	Not used	Not used	Not used	Not used	Not used
61	XREG_MCERR_ALLLOG:B2							
	Not used	Not used	Not used	Not used	LRP3 ILLEGAL ACS	LRP2 ILLEGAL ACS	LRP1 ILLEGAL ACS	LRP0 ILLEGAL ACS
62	XREG_MCERR_ALLLOG:B1							
	XD ILLEGAL ACS	SHC ILLEGAL ACS	IX0 ILLEGAL ACS	IX1 ILLEGAL ACS	IA0 ILLEGAL ACS	IA1 ILLEGAL ACS	UNK ILLEGAL ACS	Not used
63	XREG_MCERR_ALLLOG:B0							
	MP7 ILLEGAL ACS	MP6 ILLEGAL ACS	MP5 ILLEGAL ACS	MP4 ILLEGAL ACS	MP3 ILLEGAL ACS	MP2 ILLEGAL ACS	MP1 ILLEGAL ACS	MP0 ILLEGAL ACS
64	XREG_MCERR_HDLOG0_0:B3							
	HED LOG							
65	XREG_MCERR_HDLOG0_0:B2							
	HED LOG							
66	XREG_MCERR_HDLOG0_0:B1							
	HED LOG							
67	XREG_MCERR_HDLOG0_0:B0							
	HED LOG							
68	XREG_MCERR_HDLOG0_1:B3							
	HED LOG							
69	XREG_MCERR_HDLOG0_1:B2							
	HED LOG							
6A	XREG_MCERR_HDLOG0_1:B1							
	HED LOG							
6B	XREG_MCERR_HDLOG0_1:B0							
	HED LOG							
6C	XREG_MCERR_HDLOG0_2:B3							
	HED LOG							
6D	XREG_MCERR_HDLOG0_2:B2							
	HED LOG							
6E	XREG_MCERR_HDLOG0_2:B1							
	HED LOG							
6F	XREG_MCERR_HDLOG0_2:B0							
	HED LOG							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(4) Byte28 = 83 (4/4)

	0	1	2	3	4	5	6	7
70	XREG_MCERR_HDLOG0_3:B3							
	HED LOG							
71	XREG_MCERR_HDLOG0_3:B2							
	HED LOG							
72	XREG_MCERR_HDLOG0_3:B1							
	HED LOG							
73	XREG_MCERR_HDLOG0_3:B0							
	HED LOG							
74	XREG_MCERR_LOG0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
75	XREG_MCERR_LOG0:B2							
	RAIF RGARB CMP	RAIF TIMEOUT WT	RAIF TIMOUT RD	Not used	Not used	Not used	Not used	Not used
76	XREG_MCERR_LOG0:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
77	XREG_MCERR_LOG0:B0							
	RAIF RGARB CMP	RAIF TIMEOUT WT	RAIF TIMOUT RD	Not used	Not used	Not used	Not used	Not used
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(5) Byte28 = 84 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	XD_CTL_CHK3_MPx:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	XD_CTL_CHK3_MPx:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	XD_CTL_CHK3_MPx:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
47	XD_CTL_CHK3_MPx:B0							
	Not used	Not used	Not used	Not used	Not used	MPTRASH	MPMYRD	RREG
48	XD_RREGX_CHK3_INT:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
49	XD_RREGX_CHK3_INT:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4A	XD_RREGX_CHK3_INT:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4B	XD_RREGX_CHK3_INT:B0							
	WSETERR	NOHITADR STOP	DRXLRC	ERXLRC	PNPTO	RCHKS	WCHKS	RREG WR NOHIT
4C	XD_RREGX_CHK3_STS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	XD_RREGX_CHK3_STS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4E	XD_RREGX_CHK3_STS:B1							
	Not used	EP	CPLSTS	ID	LEN	REQID	NEQCPLD	NEQTAG
4F	XD_RREGX_CHK3_STS:B0							
	Not used	Not used	Not used	Not used	Not used	CPLTO	IX	NOHITADR

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Byte27 = 81 (CHK3) Byte40-7F Detail
(5) Byte28 = 84 (2/4)

	0	1	2	3	4	5	6	7
50	XD_RREGX_WRADR0:B3							
	A31	A30	A29	A28	A27	A26	A25	A24
51	XD_RREGX_WRADR0:B2							
	A23	A22	A21	A20	A19	A18	A17	A16
52	XD_RREGX_WRADR0:B1							
	A15	A14	A13	A12	A11	A10	A9	A8
53	XD_RREGX_WRADR0:B0							
	A7	A6	A5	A4	A3	A2	A1	A0
54	XD_RREGX_WRADR1:B3							
	LMA15	LMA14	LMA13	LMA12	LMA11	LMA10	LMA9	LMA8
55	XD_RREGX_WRADR1:B2							
	LMA7	LMA6	LMA5	LMA4	LMA3	LMA2	LMA1	LMA0
56	XD_RREGX_WRADR1:B1							
	ACC2	ACC1	ACC0	IX	MD3	MD2	MD1	MD0
57	XD_RREGX_WRADR1:B0							
	CL	A38	A37	A36	A35	A34	A33	A32
58	XD_RREGX_RDADR0:B3							
	A31	A30	A29	A28	A27	A26	A25	A24
59	XD_RREGX_RDADR0:B2							
	A23	A22	A21	A20	A19	A18	A17	A16
5A	XD_RREGX_RDADR0:B1							
	A15	A14	A13	A12	A11	A10	A9	A8
5B	XD_RREGX_RDADR0:B0							
	A7	A6	A5	A4	A3	A2	A1	A0
5C	XD_RREGX_RDADR1:B3							
	LMA15	LMA14	LMA13	LMA12	LMA11	LMA10	LMA9	LMA8
5D	XD_RREGX_RDADR1:B2							
	LMA7	LMA6	LMA5	LMA4	LMA3	LMA2	LMA1	LMA0
5E	XD_RREGX_RDADR1:B1							
	ACC2	ACC1	ACC0	IX	MD3	MD2	MD1	MD0
5F	XD_RREGX_RDADR1:B0							
	CL	A38	A37	A36	A35	A34	A33	A32

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Byte27 = 81 (CHK3) Byte40-7F Detail
(5) Byte28 = 84 (3/4)

	0	1	2	3	4	5	6	7
60	XD_RREGX_STS2:B3							
	LRC							
61	XD_RREGX_STS2:B2							
	LRC							
62	XD_RREGX_STS2:B1							
	ERR	Not used	Not used	Not used	Not used	Not used	Not used	RD
63	XD_RREGX_STS2:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	END
64	XD_RREGX_SEQSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	XD_RREGX_SEQSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	XD_RREGX_SEQSTS:B1							
	ST N							
67	XD_RREGX_SEQSTS:B0							
	ST							
68	Reserved							
	Reserved							
69	Reserved							
	Reserved							
6A	Reserved							
	Reserved							
6B	Reserved							
	Reserved							
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(5) Byte28 = 84 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(6) Byte28 = 20/21/22/23/40/41/42/43 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	XARB_RX_PCK_ERR0:B3							
	Not used	RXSEQ0 QENC Error	RXSEQ0 Q Parity Error	PCI ECC DETECT	RXBLK ECRC Error	Not used	RXHDBUF WTPT Parity Error	Not used
45	XARB_RX_PCK_ERR0:B2							
	Not used	RXNDBUF WTPT Parity Error	RXHDIX Parity Error	Not used	RXDT WTADR Parity Error	RXSEQ0 TCNT Parity Error	RXNHIX Parity Error	RCRC CMP Parity Error
46	XARB_RX_PCK_ERR0:B1							
	P2C SEQ DEC Error	P2C SEQ ENC Error	P2C SEQ Parity Error	P2C CNT Parity Error	RX Parity Error	RXNDBUF ING Parity Error	RXDTIX DTCMP Parity Error	RXDTIX WADR Parity Error
47	XARB_RX_PCK_ERR0:B0							
	TAGxTMR SEQ Parity Error	TAGxTMR ENC Error	TAGxTMR GP Error	BACNT GP Error	RX PCK CHK4TOP	RX PCK CHK1TOP	RX PCK WRN TOP	Not used
48	XARB_TX_PCK_ERR0:B3							
	TXHD RDPT Parity Error	TXNH RDPT Parity Error	TXNH WTPT Parity Error	TXND RDPT Parity Error	BETY Error	CDETY Error	CHETY Error	NDETY Error
49	XARB_TX_PCK_ERR0:B2							
	NHETY FRC Error	PDETY FRC Error	PHETY FRC Error	QETY FRC Error	LINKERR	TXSEQ0 QE Error	TXSEQ0 Q Parity Error	P2C SEQ D Error
4A	XARB_TX_PCK_ERR0:B1							
	P2C SEQ E Error	P2C SEQ Parity Error	TXDT RDADR Parity Error	P2C CNT Parity Error	TXHDOX Parity Error	TXDTOX Parity Error	TXNHIX Parity Error	TXNHOX Parity Error
4B	XARB_TX_PCK_ERR0:B0							
	LINKERR	TXNDBUF WTPT Parity Error	STOPREQ Parity Error	TX Error GP Error	TXSEQ0 TCNT Parity Error	Not used	XFBCNT GP Error	XFQCNT Parity Error
4C	XARB_TX_PCK_ERR1:B3							
	ICNT Parity Error	TXHDDT A Parity Error	TXHDDT E Parity Error	Not used	ICNT NP Parity Error	NPHDBUF Parity Error	TXDTBUF Parity Error	TXNDBUF Parity Error
4D	XARB_TX_PCK_ERR1:B2							
	CHCNT Parity Error	NHCNT Parity Error	PHCNT Parity Error	CDCNT Parity Error	NDCNT Parity Error	PDCNT Parity Error	TXDTBUF ADR Error	TXDTBUF UNC Error
4E	XARB_TX_PCK_ERR1:B1							
	FCTMR SEQ Parity Error	FCTMR SEQ ENC Error	FCTMR GP Error	FCTMR TO Error	Not used	Not used	Not used	Not used
4F	XARB_TX_PCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN TOP	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(6) Byte28 = 20/21/22/23/40/41/42/43 (2/4)

	0	1	2	3	4	5	6	7
50	XARB_RX_UCK_ERR0:B3							
	RXHDBUF RDPT Parity Error	RXDTBUF ADR Error	RXDTBUF UNCOR	RXNHBUF RDPT Parity Error	RXNDBUF RDPT Parity Error	RXDT RDADR Parity Error	RXHDOX Parity Error	WCRC CMP Parity Error
51	XARB_RX_UCK_ERR0:B2							
	RXNHOX Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error	C2P CNT Parity Error	SWTX DEC Error	SWTX DLRC G Error
52	XARB_RX_UCK_ERR0:B1							
	SWTX DT L GP Error	SWTX ENC Error	SWTX HLRC G Error	Not used	SWTX TOCNT GP Error	SWTX TOCNT TO	SWTX WDCNT GP Error	Not used
53	XARB_RX_UCK_ERR0:B0							
	ARBSEQ QDEC Error	ARBSEQ QENC Error	ARBSEQ Q Parity Error	RXNHBUF WTPT Parity Error	MRG ECC ADR Error	MRG ECC UNCOR	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
54	XARB_RX_UCK_ERR1:B3							
	MRGBUF DTCNT Parity Error	MRGBUF TMR Parity Error	XFCNT GP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	RXNHBUF OVER	Not used	Not used
55	XARB_RX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
56	XARB_RX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
57	XARB_RX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN TOP	Not used
58	XARB_TX_UCK_ERR0:B3							
	SWRX DEC Error	SWRX DLRCTIM G Error	SWRX DLRC G Error	SWRX ENC Error	SWRX HLRC G Error	SWRX SW DT GP Error	SWRX SW VLD G Error	SWRX TOCNT GP Error
59	XARB_TX_UCK_ERR0:B2							
	SWRX TOCNT TO	SWRX TX Error G Error	SWRX WDCNT GP Error	TXHDBUF WTPT Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error
5A	XARB_TX_UCK_ERR0:B1							
	C2P CNT Parity Error	TXDTBUF WTADR Parity Error	TXHDIX Parity Error	Not used	TXNHCNT Parity Error	SWRX REQOFF Error	SWRX SW HD Parity Error	DATCNT Parity Error
5B	XARB_TX_UCK_ERR0:B0							
	DIV ECC ADR Error	DIV ECC CRCT Error	DIV ECC UNCOR	CPLSEQ QDEC Error	CPLSEQ QENC Error	CPLSEQ Q Parity Error	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
5C	XARB_TX_UCK_ERR1:B3							
	CDICNT Parity Error	CPLSEQ DTCNT Parity Error	XFCNT GP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	MIC CHK1 Error	TXDTIX DTCMP Parity Error	TXDTIX WACMP Parity Error
5D	XARB_TX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5E	XARB_TX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5F	XARB_TX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN TOP	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(6) Byte28 = 20/21/22/23/40/41/42/43 (3/4)

	0	1	2	3	4	5	6	7
60	XARBRG_ERR_STS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
61	XARBRG_ERR_STS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WARNING STATUS
62	XARBRG_ERR_STS:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK4 ERROR STATUS
63	XARBRG_ERR_STS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK1B ERROR STATUS
64	XARBRG_CRG_EXPCAPINT:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	XARBRG_CRG_EXPCAPINT:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	XARBRG_CRG_EXPCAPINT:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
67	XARBRG_CRG_EXPCAPINT:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CRG EXPCAP INT
68	XARBRG_AHB0_SEQERRSTS:B3							
	AHBSEQ ST							
69	XARBRG_AHB0_SEQERRSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	XARBRG_AHB0_SEQERRSTS:B1							
	Not used	Not used	Not used	ERROR STATUS		Not used	ERROR STATUS	
6B	XARBRG_AHB0_SEQERRSTS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ERROR STATUS
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(6) Byte28 = 20/21/22/23/40/41/42/43 (4/4)

	0	1	2	3	4	5	6	7
70	XARBRG_PRGERR_C1BSTS2:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	XARBRG_PRGERR_C1BSTS2:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	XARBRG_PRGERR_C1BSTS2:B1							
	ZPEX DLM ECC Error REP	ZPEX DLM ECC Error NOR	ZPEX TLM ECC Error TX0	ZPEX TLM ECC Error RX0	ZPEX TLM PARITY Error	ZPEX TLM PARITY Error RX0	ZPEX TLM PARITY Error STOP	ZPEX TLM PARITY Error TX0
73	XARBRG_PRGERR_C1BSTS2:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ZPEX ERR INJECC Error
74	XARBRG_PRGERR_C1BSTS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
75	XARBRG_PRGERR_C1BSTS1:B2							
	Not used	Not used	TLM FCPTC Error	TLM ROVF Error	TLM PTLP Error	TLM MFTLP Error	TLM ECRC Error	TLM UR Error
76	XARBRG_PRGERR_C1BSTS1:B1							
	Not used	Not used	DLM SURPRISE DW Error	DLM PTC Error	DLM TLP Error	DLM DLLP Error	DLM REPLAY RO Error	DLM REPLAY TO Error
77	XARBRG_PRGERR_C1BSTS1:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	PLM RECIEVER Error
78	XARBRG_PRGLINK_C1BSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
79	XARBRG_PRGLINK_C1BSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	XARBRG_PRGLINK_C1BSTS:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7B	XARBRG_PRGLINK_C1BSTS:B0							
	Not used	Not used	Not used	Not used	PLM LTSSM Error	PLM LINK Training Error	DLM VC0 EN Error	DLM DL UP Error
7C	XARBRG_PRGERR_RXSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7D	XARBRG_PRGERR_RXSTS:B2							
	Not used	Not used	Not used	TLM TX0 Error	Not used	Not used	Not used	TLM RX0 Error
7E	XARBRG_PRGERR_RXSTS:B1							
	Not used	TLM RX0 STS						
7F	XARBRG_PRGERR_RXSTS:B0							
	TLM MFTLP CODE							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(7) Byte28 = 10/11/50-55/58-5D/60-63 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	XARB_RX_PCK_ERR0:B3							
	Not used	RXSEQ0 QENC Error	RXSEQ0 Q Parity Error	PCI ECC DETECT	RXBLK ECRC Error	Not used	RXHDBUF WTPT Parity Error	Not used
45	XARB_RX_PCK_ERR0:B2							
	Not used	RXNDBUF WTPT Parity Error	RXHDIX Parity Error	Not used	RXDT WTADR Parity Error	RXSEQ0 TCNT Parity Error	RXNHIX Parity Error	RCRC CMP Parity Error
46	XARB_RX_PCK_ERR0:B1							
	P2C SEQ DEC Error	P2C SEQ ENC Error	P2C SEQ Parity Error	P2C CNT Parity Error	RX Parity Error	RXNDBUF ING Parity Error	RXDTIX DTCMP Parity Error	RXDTIX WADR Parity Error
47	XARB_RX_PCK_ERR0:B0							
	TAGxTMR SEQ Parity Error	TAGxTMR ENC Error	TAGxTMR GP Error	BACNT GP Error	RX PCK CHK4TOP	RX PCK CHK1TOP	RX PCK WRN TOP	Not used
48	XARB_TX_PCK_ERR0:B3							
	TXHD RDPT Parity Error	TXNH RDPT Parity Error	TXNH WTPT Parity Error	TXND RDPT Parity Error	BETY Error	CDETY Error	CHETY Error	NDETY Error
49	XARB_TX_PCK_ERR0:B2							
	NHETY FRC Error	PDETY FRC Error	PHETY FRC Error	QETY FRC Error	LINKERR	TXSEQ0 QE Error	TXSEQ0 Q Parity Error	P2C SEQ D Error
4A	XARB_TX_PCK_ERR0:B1							
	P2C SEQ E Error	P2C SEQ Parity Error	TXDT RDADR Parity Error	P2C CNT Parity Error	TXHDOX Parity Error	TXDTOX Parity Error	TXNHIX Parity Error	TXNHOX Parity Error
4B	XARB_TX_PCK_ERR0:B0							
	LINKERR	TXNDBUF WTPT Parity Error	STOPREQ Parity Error	TX Error GP Error	TXSEQ0 TCNT Parity Error	Not used	XFBCNT GP Error	XFQCNT Parity Error
4C	XARB_TX_PCK_ERR1:B3							
	ICNT Parity Error	TXHDDT A Parity Error	TXHDDT E Parity Error	Not used	ICNT NP Parity Error	NPHDBUF Parity Error	TXDTBUF Parity Error	TXNDBUF Parity Error
4D	XARB_TX_PCK_ERR1:B2							
	CHCNT Parity Error	NHCNT Parity Error	PHCNT Parity Error	CDCNT Parity Error	NDCNT Parity Error	PDCNT Parity Error	TXDTBUF ADR Error	TXDTBUF UNC Error
4E	XARB_TX_PCK_ERR1:B1							
	FCTMR SEQ Parity Error	FCTMR SEQ ENC Error	FCTMR GP Error	FCTMR TO Error	Not used	Not used	Not used	Not used
4F	XARB_TX_PCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN TOP	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(7) Byte28 = 10/11/50-55/58-5D/60-63 (2/4)

	0	1	2	3	4	5	6	7
50	XARB_RX_UCK_ERR0:B3							
	RXHDBUF RDPT Parity Error	RXDTBUF ADR Error	RXDTBUF UNCOR	RXNHBUF RDPT Parity Error	RXNDBUF RDPT Parity Error	RXDT RDADR Parity Error	RXHDOX Parity Error	WCRC CMP Parity Error
51	XARB_RX_UCK_ERR0:B2							
	RXNHOX Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error	C2P CNT Parity Error	SWTX DEC Error	SWTX DLRC G Error
52	XARB_RX_UCK_ERR0:B1							
	SWTX DT L GP Error	SWTX ENC Error	SWTX HLRC G Error	Not used	SWTX TOCNT GP Error	SWTX TOCNT TO	SWTX WDCNT GP Error	Not used
53	XARB_RX_UCK_ERR0:B0							
	ARBSEQ QDEC Error	ARBSEQ QENC Error	ARBSEQ Q Parity Error	RXNHBUF WTPT Parity Error	MRG ECC ADR Error	MRG ECC UNCOR	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
54	XARB_RX_UCK_ERR1:B3							
	MRGBUF DTCNT Parity Error	MRGBUF TMR Parity Error	XFCNT GP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	RXNHBUF OVER	Not used	Not used
55	XARB_RX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
56	XARB_RX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
57	XARB_RX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN TOP	Not used
58	XARB_TX_UCK_ERR0:B3							
	SWRX DEC Error	SWRX DLRCTIM G Error	SWRX DLRC G Error	SWRX ENC Error	SWRX HLRC G Error	SWRX SW DT GP Error	SWRX SW VLD G Error	SWRX TOCNT GP Error
59	XARB_TX_UCK_ERR0:B2							
	SWRX TOCNT TO	SWRX TX Error G Error	SWRX WDCNT GP Error	TXHDBUF WTPT Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error
5A	XARB_TX_UCK_ERR0:B1							
	C2P CNT Parity Error	TXDTBUF WTADR Parity Error	TXHDIX Parity Error	Not used	TXNHCNT Parity Error	SWRX REQOFF Error	SWRX SW HD Parity Error	DATCNT Parity Error
5B	XARB_TX_UCK_ERR0:B0							
	DIV ECC ADR Error	DIV ECC CRCT Error	DIV ECC UNCOR	CPLSEQ QDEC Error	CPLSEQ QENC Error	CPLSEQ Q Parity Error	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
5C	XARB_TX_UCK_ERR1:B3							
	CDICNT Parity Error	CPLSEQ DTCNT Parity Error	XFCNT GP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	MIC CHK1 Error	TXDTIX DTCMP Parity Error	TXDTIX WACMP Parity Error
5D	XARB_TX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5E	XARB_TX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5F	XARB_TX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN TOP	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(7) Byte28 = 10/11/50-55/58-5D/60-63 (3/4)

	0	1	2	3	4	5	6	7
60	XARBRG_ERR_STS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
61	XARBRG_ERR_STS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WARNING STATUS
62	XARBRG_ERR_STS:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK4 ERROR STATUS
63	XARBRG_ERR_STS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK1B ERROR STATUS
64	XARBRG_CRG_EXPCAPINT:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	XARBRG_CRG_EXPCAPINT:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	XARBRG_CRG_EXPCAPINT:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
67	XARBRG_CRG_EXPCAPINT:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CRG EXPCAP INT
68	XARBRG_AHB0_SEQERRSTS:B3							
	AHBSEQ ST							
69	XARBRG_AHB0_SEQERRSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	XARBRG_AHB0_SEQERRSTS:B1							
	Not used	Not used	Not used	ERROR STATUS		Not used	ERROR STATUS	
6B	XARBRG_AHB0_SEQERRSTS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ERROR STATUS
6C	XARBRG_AHB1_SEQERRSTS:B3							
	AHBSEQ ST							
6D	XARBRG_AHB1_SEQERRSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6E	XARBRG_AHB1_SEQERRSTS:B1							
	Not used	Not used	Not used	ERROR STATUS		Not used	ERROR STATUS	
6F	XARBRG_AHB1_SEQERRSTS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ERROR STATUS

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Byte27 = 81 (CHK3) Byte40-7F Detail
(7) Byte28 = 10/11/50-55/58-5D/60-63 (4/4)

	0	1	2	3	4	5	6	7
70	XARBRG_PRGERR_C1BSTS2:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	XARBRG_PRGERR_C1BSTS2:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	XARBRG_PRGERR_C1BSTS2:B1							
	ZPEX DLM ECC Error REP	ZPEX DLM ECC Error NOR	ZPEX TLM ECC Error TX0	ZPEX TLM ECC Error RX0	ZPEX TLM PARITY Error	ZPEX TLM PARITY Error RX0	ZPEX TLM PARITY Error STOP	ZPEX TLM PARITY Error TX0
73	XARBRG_PRGERR_C1BSTS2:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ZPEX ERR INJECC Error
74	XARBRG_PRGERR_C1BSTS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
75	XARBRG_PRGERR_C1BSTS1:B2							
	Not used	Not used	TLM FCPTC Error	TLM ROVF Error	TLM PTLP Error	TLM MFTLP Error	TLM ECRC Error	TLM UR Error
76	XARBRG_PRGERR_C1BSTS1:B1							
	Not used	Not used	DLM SURPRISE DW Error	DLM PTC Error	DLM TLP Error	DLM DLLP Error	DLM REPLAY RO Error	DLM REPLAY TO Error
77	XARBRG_PRGERR_C1BSTS1:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	PLM RECIEVER Error
78	XARBRG_PRGLINK_C1BSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
79	XARBRG_PRGLINK_C1BSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	XARBRG_PRGLINK_C1BSTS:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7B	XARBRG_PRGLINK_C1BSTS:B0							
	Not used	Not used	Not used	Not used	PLM LTSSM Error	PLM LINK Training Error	DLM VC0 EN Error	DLM DL UP Error
7C	XARBRG_PRGERR_RXSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7D	XARBRG_PRGERR_RXSTS:B2							
	Not used	Not used	Not used	TLM TX0 Error	Not used	Not used	Not used	TLM RX0 Error
7E	XARBRG_PRGERR_RXSTS:B1							
	Not used	TLM RX0 STS						
7F	XARBRG_PRGERR_RXSTS:B0							
	TLM MFTLP CODE							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(8) Byte28 = A3 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	INT1_MAILBOX_INT_STATUS0:B3							
	MBOX INT MP31	MBOX INT MP30	MBOX INT MP29	MBOX INT MP28	MBOX INT MP27	MBOX INT MP26	MBOX INT MP25	MBOX INT MP24
45	INT1_MAILBOX_INT_STATUS0:B2							
	MBOX INT MP23	MBOX INT MP22	MBOX INT MP21	MBOX INT MP20	MBOX INT MP19	MBOX INT MP18	MBOX INT MP17	MBOX INT MP16
46	INT1_MAILBOX_INT_STATUS0:B1							
	MBOX INT MP15	MBOX INT MP14	MBOX INT MP13	MBOX INT MP12	MBOX INT MP11	MBOX INT MP10	MBOX INT MP9	MBOX INT MP8
47	INT1_MAILBOX_INT_STATUS0:B0							
	MBOX INT MP7	MBOX INT MP6	MBOX INT MP5	MBOX INT MP4	MBOX INT MP3	MBOX INT MP2	MBOX INT MP1	MBOX INT MP0
48	INT1_MAILBOX_ABT_STATUS0:B3							
	MBOX ABT MP31	MBOX ABT MP30	MBOX ABT MP29	MBOX ABT MP28	MBOX ABT MP27	MBOX ABT MP26	MBOX ABT MP25	MBOX ABT MP24
49	INT1_MAILBOX_ABT_STATUS0:B2							
	MBOX ABT MP23	MBOX ABT MP22	MBOX ABT MP21	MBOX ABT MP20	MBOX ABT MP19	MBOX ABT MP18	MBOX ABT MP17	MBOX ABT MP16
4A	INT1_MAILBOX_ABT_STATUS0:B1							
	MBOX ABT MP15	MBOX ABT MP14	MBOX ABT MP13	MBOX ABT MP12	MBOX ABT MP11	MBOX ABT MP10	MBOX ABT MP9	MBOX ABT MP8
4B	INT1_MAILBOX_ABT_STATUS0:B0							
	MBOX ABT MP7	MBOX ABT MP6	MBOX ABT MP5	MBOX ABT MP4	MBOX ABT MP3	MBOX ABT MP2	MBOX ABT MP1	MBOX ABT MP0
4C	INT1_MAILBOX_CTL_MP00:B3							
	MAILBOX EN	MP NUM						
4D	INT1_MAILBOX_CTL_MP00:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4E	INT1_MAILBOX_CTL_MP00:B1							
	COPY							
4F	INT1_MAILBOX_CTL_MP00:B0							
	OPCODE							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(8) Byte28 = A3 (2/4)

	0	1	2	3	4	5	6	7
50	INT1_IDMA_STATUS:B3							
	STATUS ENABLE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
51	INT1_IDMA_STATUS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
52	INT1_IDMA_STATUS:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
53	INT1_IDMA_STATUS:B0							
	INTDMA RX STS	Not used	Not used	ERR END STS4	ERR END STS3	ERR END STS2	ERR END STS1	ERR END STS0
54	LRPDS_MBOX_TX0:B3							
	MBOX LM ADR							
55	LRPDS_MBOX_TX0:B2							
	MBOX LM ADR							
56	LRPDS_MBOX_TX0:B1							
	MBOX LM ADR							
57	LRPDS_MBOX_TX0:B0							
	MBOX LM ADR							
58	LRPDS_MBOX_TX1:B3							
	MBOX TX1							
59	LRPDS_MBOX_TX1:B2							
	MBOX TX1							
5A	LRPDS_MBOX_TX1:B1							
	MBOX TX1							
5B	LRPDS_MBOX_TX1:B0							
	MBOX TX1							
5C	LRPDS_MBOX_TX2:B3							
	MBOX TX2							
5D	LRPDS_MBOX_TX2:B2							
	MBOX TX2							
5E	LRPDS_MBOX_TX2:B1							
	MBOX TX2							
5F	LRPDS_MBOX_TX2:B0							
	MBOX TX2							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(8) Byte28 = A3 (3/4)

	0	1	2	3	4	5	6	7
60	LRPDS_MBOX_TX3:B3							
	MBOX TX3							
61	LRPDS_MBOX_TX3:B2							
	MBOX TX3							
62	LRPDS_MBOX_TX3:B1							
	MBOX TX3							
63	LRPDS_MBOX_TX3:B0							
	MBOX TX3							
64	LRPDS_HMA_STS:B3							
	Not used	Module number			CL Number	Not used	Not used	IX Mode
65	LRPDS_HMA_STS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	LRPDS_HMA_STS:B1							
	LSI REV							
67	LRPDS_HMA_STS:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	LRPDS_STATUS0:B3							
	LRP STS31	LRP STS30	LRP STS29	LRP STS28	LRP STS27	LRP STS26	LRP STS25	LRP STS24
69	LRPDS_STATUS0:B2							
	LRP STS23	LRP STS22	LRP STS21	LRP STS20	LRP STS19	LRP STS18	LRP STS17	LRP STS16
6A	LRPDS_STATUS0:B1							
	LRP STS15	LRP STS14	LRP STS13	LRP STS12	LRP STS11	LRP STS10	LRP STS9	LRP STS8
6B	LRPDS_STATUS0:B0							
	LRP STS7	LRP STS6	LRP STS5	LRP STS4	LRP STS3	LRP STS2	LRP STS1	LRP STS0
6C	LRPDS_FLAG0 ::LRP4 :B3							
	LRP4 FLAG0							
6D	LRPDS_FLAG0 ::LRP4 :B2							
	LRP4 FLAG0							
6E	LRPDS_FLAG0 ::LRP4 :B1							
	LRP4 FLAG0							
6F	LRPDS_FLAG0 ::LRP4 :B0							
	LRP4 FLAG0							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(8) Byte28 = A3 (4/4)

	0	1	2	3	4	5	6	7
70		LRPDS_FLAG0	::LRP0 :B3					
				LRP0 FLAG0				
71		LRPDS_FLAG0	::LRP0 :B2					
				LRP0 FLAG0				
72		LRPDS_FLAG0	::LRP0 :B1					
				LRP0 FLAG0				
73		LRPDS_FLAG0	::LRP0 :B0					
				LRP0 FLAG0				
74		LRPDS_FLAG0	::LRP1 :B3					
				LRP1 FLAG0				
75		LRPDS_FLAG0	::LRP1 :B2					
				LRP1 FLAG0				
76		LRPDS_FLAG0	::LRP1 :B1					
				LRP1 FLAG0				
77		LRPDS_FLAG0	::LRP1 :B0					
				LRP1 FLAG0				
78		LRPDS_FLAG0	::LRP2 :B3					
				LRP2 FLAG0				
79		LRPDS_FLAG0	::LRP2 :B2					
				LRP2 FLAG0				
7A		LRPDS_FLAG0	::LRP2 :B1					
				LRP2 FLAG0				
7B		LRPDS_FLAG0	::LRP2 :B0					
				LRP2 FLAG0				
7C		LRPDS_FLAG0	::LRP3 :B3					
				LRP3 FLAG0				
7D		LRPDS_FLAG0	::LRP3 :B2					
				LRP3 FLAG0				
7E		LRPDS_FLAG0	::LRP3 :B1					
				LRP3 FLAG0				
7F		LRPDS_FLAG0	::LRP3 :B0					
				LRP3 FLAG0				

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Byte27 = 81 (CHK3) Byte40-7F Detail
(9) Byte28 = A0 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	SMC_ERRSTS_OWNMP:B2							
	Not used	E Micro Error	Not used	Not used	Not used	X CPL Error	D CPL Error	E CPL Error
45	SMC_ERRSTS_OWNMP:B0							
	Not used	Not used	Not used	Not used	CRG CHK1	X CHK1	D CHK1	E CHK1
46	SMC_ERRSTS_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	X Warning	D Warning	E Warning
47	SMC_ERRSTS_OWNMP:B6							
	Not used	Not used	Not used	Not used	Not used	X Slave Error	D Slave Error	E Slave Error
48	SMC_CHK3_ERRLOG_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	ECTL NP MULTI Micro Error	ECTL BNDRY Error	ECTL INVDST Error
49	SMC_CHK3_ERRLOG_OWNMP:B6							
	ECTL PREGWT Micro Error	ECTL INDWT Micro Error	ECTL INDRD Micro Error	ECTL ATM Micro Error	ECTL INV CMD Error	ECTL PCODE Error	ECTL SM ACC Error	ECTL ADR INV Error
4A	SMC_CHK3_ERRLOG_OWNMP:B5							
	Not used	Not used	Not used	Not used	Not used	XCTL AUTOCHK TOV Error	XCTL WTCHKRD Error	XCTL AUTOCHK Error
4B	SMC_CHK3_ERRLOG_OWNMP:B4							
	XCTL AUTOCHK STS Error	Not used	Not used	XCTL MERSTS X Error	XCTL ErrorSTS X Error	XCTL CPL TOV Error	XCTL CPL FRCTOV Error	XCTL CPL STS Error
4C	SMC_CHK3_ERRLOG_OWNMP:B3							
	Not used	Not used	Not used	Not used	DCTL AUTOCHK TOV Error	Not used	DCTL WTCHKRD Error	DCTL AUTOCHK Error
4D	SMC_CHK3_ERRLOG_OWNMP:B2							
	DCTL AUTOCHK STS Error	Not used	Not used	Not used	Not used	DCTL CPL FRCTOV Error	DCTL CPL TOV Error	DCTL CPL STS Error
4E	SMC_CHK3_ERRLOG_OWNMP:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4F	SMC_CHK3_ERRLOG_OWNMP:B0							
	Not used	Not used	Not used	Not used	Not used	ECTL CPL FRCTOV Error	ECTL CPL TOV Error	ECTL CPL STS Error

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Byte27 = 81 (CHK3) Byte40-7F Detail
(9) Byte28 = A0 (2/4)

	0	1	2	3	4	5	6	7
50	SMC_ECTL_DSTADR_LOG:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ErrorLog FLG
51	SMC_ECTL_DSTADR_LOG:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
52	SMC_ECTL_DSTADR_LOG:B5							
	Destination Address ACC			Destination Address IX	Destination Address MDL			
53	SMC_ECTL_DSTADR_LOG:B4							
	Destination Address [B4]							
54	SMC_ECTL_DSTADR_LOG:B3							
	Destination Address [B3]							
55	SMC_ECTL_DSTADR_LOG:B2							
	Destination Address [B2]							
56	SMC_ECTL_DSTADR_LOG:B1							
	Destination Address [B1]							
57	SMC_ECTL_DSTADR_LOG:B0							
	Destination Address [B0]							
58	SMC_ECTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
59	SMC_ECTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
5A	SMC_ECTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
5B	SMC_ECTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
5C	SMC_ECTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
5D	SMC_ECTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
5E	SMC_ECTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
5F	SMC_ECTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(9) Byte28 = A0 (3/4)

	0	1	2	3	4	5	6	7
60	SMC_ECTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
61	SMC_ECTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
62	SMC_ECTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
63	SMC_ECTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
64	SMC_ECTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
65	SMC_ECTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
66	SMC_ECTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
67	SMC_ECTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							
68	SMC_ECTL_DAT_LOG:B7							
	Data Log [B7]							
69	SMC_ECTL_DAT_LOG:B6							
	Data Log [B6]							
6A	SMC_ECTL_DAT_LOG:B5							
	Data Log [B5]							
6B	SMC_ECTL_DAT_LOG:B4							
	Data Log [B4]							
6C	SMC_ECTL_DAT_LOG:B3							
	Data Log [B3]							
6D	SMC_ECTL_DAT_LOG:B2							
	Data Log [B2]							
6E	SMC_ECTL_DAT_LOG:B1							
	Data Log [B1]							
6F	SMC_ECTL_DAT_LOG:B0							
	Data Log [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(9) Byte28 = A0 (4/4)

	0	1	2	3	4	5	6	7
70	SMC_DCTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
71	SMC_DCTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
72	SMC_DCTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
73	SMC_DCTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
74	SMC_DCTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
75	SMC_DCTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
76	SMC_DCTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
77	SMC_DCTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							
78	SMC_DCTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
79	SMC_DCTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
7A	SMC_DCTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
7B	SMC_DCTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
7C	SMC_DCTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
7D	SMC_DCTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
7E	SMC_DCTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
7F	SMC_DCTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(10) Byte28 = A1 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	MPDMA_MD_REPAFE:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	MPDMA_MD_REPAFE:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO6 REPAFE	Error NO5 REPAFE
46	MPDMA_MD_REPAFE:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Error NO4 REPAFE
47	MPDMA_MD_REPAFE:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO2 REPAFE	Error NO1 REPAFE
48	MPDMA_MD_ERR_ST09:B3							
	STS W1 Error2							
49	MPDMA_MD_ERR_ST09:B2							
	STS W1 Error2							
4A	MPDMA_MD_ERR_ST09:B1							
	STS W1 Error2							
4B	MPDMA_MD_ERR_ST09:B0							
	STS W1 Error2							
4C	MPDMA_MD_ERR_ST10:B3							
	STS W1 Error2							
4D	MPDMA_MD_ERR_ST10:B2							
	STS W1 Error2							
4E	MPDMA_MD_ERR_ST10:B1							
	STS W1 Error2							
4F	MPDMA_MD_ERR_ST10:B0							
	STS W1 Error2							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(10) Byte28 = A1 (2/4)

	0	1	2	3	4	5	6	7
50	MPDMA_MD_ERR_ST11:B3							
	STS W1 Error3							
51	MPDMA_MD_ERR_ST11:B2							
	STS W1 Error3							
52	MPDMA_MD_ERR_ST11:B1							
	STS W1 Error3							
53	MPDMA_MD_ERR_ST11:B0							
	STS W1 Error3							
54	MPDMA_MD_ERR_ST12:B3							
	STS W1 Error3							
55	MPDMA_MD_ERR_ST12:B2							
	STS W1 Error3							
56	MPDMA_MD_ERR_ST12:B1							
	STS W1 Error3							
57	MPDMA_MD_ERR_ST12:B0							
	STS W1 Error3							
58	MPDMA_MD_ERR_ST13:B3							
	SEQ Error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
59	MPDMA_MD_ERR_ST13:B2							
	X E1 E00 NOTIDLE	X E1 E01 SEM Error33	PRM OUT LOW	PRM OUT HIGH	MSK SADR 8B CNT	MSK DADR0 8B CNT	MSK DADR1 8B CNT	Not used
5A	MPDMA_MD_ERR_ST13:B1							
	STSS Error2 SUMMARY	STS 32B	Not used	Not used	Not used	Not used	Not used	Not used
5B	MPDMA_MD_ERR_ST13:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5C	MPDMA_MD_ERR_ST14:B3							
	SWRX SEQ Error	E03 WDCNT	E04 TOCNT TO	E05 TOCNT	E06 DT	E07 HLRC NEQ	E08 DLRC NEQ	E09 HED
5D	MPDMA_MD_ERR_ST14:B2							
	E10 NPCNT	E11 PCCNT	E12 DLRCTIM	E13 VLD	E14 REQ	Not used	Not used	TX ErrorSTS
5E	MPDMA_MD_ERR_ST14:B1							
	SWTX SEQ Error	E03 WDCNT	E04 TOCNT TO	E05 TOCNT	E06 DT	E07 HLRC NEQ	E08 DLRC NEQ	RX ErrorSTS
5F	MPDMA_MD_ERR_ST14:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(10) Byte28 = A1 (3/4)

	0	1	2	3	4	5	6	7
60	MPDMA_MD_ERR_ST15:B3							
	BFS0 SEQ Error	BFS1 SEQ Error	BFS2 SEQ Error	BFS3 SEQ Error	BFS4 SEQ Error	BFS5 SEQ Error	BFS6 SEQ Error	BFS7 SEQ Error
61	MPDMA_MD_ERR_ST15:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
62	MPDMA_MD_ERR_ST15:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
63	MPDMA_MD_ERR_ST15:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
64	MPDMA_MD_ERR_ST16:B3							
	DRXCMD SEQ Error	BF PTR CNT Parity Error	RCMD NUM CNT Parity Error	Not used	BM ZAN SBLK Parity Error	BMPTN FD Parity Error	DIV DLEN D10 8BB Parity Error	ZAN REQ DLEN 8BB Parity Error
65	MPDMA_MD_ERR_ST16:B2							
	BF DLEN 8BB Parity Error	CFW DLEN 8BB Parity Error	HDR TAG W18 Parity Error	P SADR 8B CNT Parity Error	RDREQ HDR D Parity Error	Not used	Not used	Not used
66	MPDMA_MD_ERR_ST16:B1							
	TMR0 SEQ Error	TMR1 SEQ Error	TMR2 SEQ Error	TMR3 SEQ Error	TMR4 SEQ Error	TMR5 SEQ Error	TMR6 SEQ Error	TMR7 SEQ Error
67	MPDMA_MD_ERR_ST16:B0							
	TOCNT0 PERR	TOCNT1 PERR	TOCNT2 PERR	TOCNT3 PERR	TOCNT4 PERR	TOCNT5 PERR	TOCNT6 PERR	TOCNT7 PERR
68	MPDMA_MD_ERR_ST18:B3							
	RXCMP SEQ Error	HDR P CNT Parity Error	REQHD Parity Error	BF S TH 8BB Parity Error	CMPHD DLEN 8BB Parity Error	Not used	Z CMPHD DLEN 8BB Parity Error	Z PRM LEN CMP 8BB Parity Error
69	MPDMA_MD_ERR_ST18:B2							
	Z REQHD DLEN 8BB Parity Error	Q Error OR	Q Error SEM	X Error UR	F1 D00 D Parity Error	F1 D08 D Parity Error	F1 D10 D Parity Error	F1 D18 D Parity Error
6A	MPDMA_MD_ERR_ST18:B1							
	FDDT W4 Parity Error	FDDT W5 Parity Error	FDDT W6 Parity Error	Not used	ZAN DLEN B 8B Parity Error	ZAN BF DLEN 8BB Parity Error	ZAN CMP DLEN 8BB Parity Error	ZAN PRM DLEN 8BB Parity Error
6B	MPDMA_MD_ERR_ST18:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6C	MPDMA_MD_ERR_ST20:B3							
	RXDCL SEQ Error A	RXDCL SEQ Error B	RXDCL SEQ Error C	RXDCL SEQ Error D	Not used	Not used	Not used	Not used
6D	MPDMA_MD_ERR_ST20:B2							
	X A Error SEM	X A Error UR	Q B T10 SFT CNT Parity Error	Q C Error UR	Q C T10 SFT CNT Parity Error	Q D Error UR	Q D T10 SFT CNT Parity Error	Not used
6E	MPDMA_MD_ERR_ST20:B1							
	ZAN BF DLEN 8BB Parity Error	OCRC OUT Parity Error	GEN OCRC DT Parity Error	GENDT LRC4B Parity Error	Not used	Not used	BADR CNT Parity Error	BF INDT Parity Error
6F	MPDMA_MD_ERR_ST20:B0							
	F2 D00 DIF CHKD Parity Error	F2 D08 DIF CHKD Parity Error	F2 D10 DIF CHKD Parity Error	F2 D18 DIF CHKD Parity Error	FDDT W4 Parity Error	FDDT W5 Parity Error	FDDT W6 Parity Error	BF PTR CNT Parity Error

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Byte27 = 81 (CHK3) Byte40-7F Detail
(10) Byte28 = A1 (4/4)

	0	1	2	3	4	5	6	7
70	MPDMA_MD_ERR_ST21:B3							
	E1 E00 FDBKDT Parity Error	E1 E01 GENRTAG Parity Error	E1 E02 CHKRTAG Parity Error	Not used	Not used	Not used	Not used	Not used
71	MPDMA_MD_ERR_ST21:B2							
	E1 00 DBV BNCNT	E1 01 DBV BLCNT	E1 02 DBV LRC	E1 03 DBV TLRC	E1 04 DBV HD	Not used	Not used	Not used
72	MPDMA_MD_ERR_ST21:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
73	MPDMA_MD_ERR_ST21:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
74	MPDMA_MD_ERR_ST23:B3							
	DTXCMD SEQ Error	TMR SEQ Error	SEQDTX CHK Error	Not used	Not used	Not used	Not used	Not used
75	MPDMA_MD_ERR_ST23:B2							
	ZAN PRM DLEN 8BB	ZAN BF DLEN 8BB	ZAN RLEN 2B 8BB	BF PTR CNT	BADRCNT	UNCRERR	ADRERR	DT F1 DI CHK
76	MPDMA_MD_ERR_ST23:B1							
	HDR TAG W1B	P DADR 8B CNT	Not used	WREQ HDR W32B D	Not used	CMPHD L	Not used	Not used
77	MPDMA_MD_ERR_ST23:B0							
	Error CPLD NOT SC	Error CPL NOT SC	Error HED	Error NOT CPL CPLD	TOCNT	T OVER	REQ DLEN 8BB	Error ACSCNT CHK
78	MPDMA_MD_ERR_ST24:B3							
	DTXCMD SEM Error	DTXCMD UR Error	T10 SFT CNTCHK	OCRC NOT EQL	OCRC OUT	LRC NOT EQL	GENDT LRC4B	Not used
79	MPDMA_MD_ERR_ST24:B2							
	E1 E00 FBDKDT	Not used	E1 E02 CHKRTAG	Not used	Not used	Not used	Not used	Not used
7A	MPDMA_MD_ERR_ST24:B1							
	E3 04 RTAG0 NOT EQL	E3 05 RTAG1 NOT EQL	E3 06 RTAG2 NOT EQL	E3 07 RTAG3 NOT EQL	E3 08 WRSEQ	E3 0A ATAG00 NOT EQL	E3 0B ATAG01 NOT EQL	E3 E0C CRC NOT EQL
7B	MPDMA_MD_ERR_ST24:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7C	MPDMA_MD_ERR_ST26:B3							
	SWRX SEQ Error	E03 WDCNT	E04 TOCNT TO	E05 TOCNT	E06 DT	E07 HLRC NEQ	E08 DLRC NEQ	E09 HED
7D	MPDMA_MD_ERR_ST26:B2							
	E10 NPCNT	E11 PCCNT	E12 DLRCTIM	E13 VLD	E14 REQ	Not used	Not used	TX ErrorSTS
7E	MPDMA_MD_ERR_ST26:B1							
	SWTX SEQ Error	E03 WDCNT	E04 TOCNT TO	E05 TOCNT	E06 DT	E07 HLRC NEQ	E08 DLRC NEQ	RX ErrorSTS
7F	MPDMA_MD_ERR_ST26:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(11) Byte28 = A2 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	XD_CTL_CHK3_MPx:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	XD_CTL_CHK3_MPx:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	XD_CTL_CHK3_MPx:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
47	XD_CTL_CHK3_MPx:B0							
	Not used	Not used	Not used	Not used	Not used	MPTRASH	MPMYRD	RREG
48	XD_RREGX_CHK3_INT:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
49	XD_RREGX_CHK3_INT:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4A	XD_RREGX_CHK3_INT:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4B	XD_RREGX_CHK3_INT:B0							
	WSET Error	NOHIT ADR STOP	DRXLRC	ERXLRC	PNPTO	RCHKS	WCHKS	RREG WR NOHIT
4C	XD_RREGX_CHK3_STS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	XD_RREGX_CHK3_STS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4E	XD_RREGX_CHK3_STS:B1							
	Not used	EP	CPLSTS	ID	LEN	REQID	NEQCPLD	NEQTAG
4F	XD_RREGX_CHK3_STS:B0							
	Not used	Not used	Not used	Not used	Not used	CPLTO	IX	NOHIT ADR

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Byte27 = 81 (CHK3) Byte40-7F Detail
(11) Byte28 = A2 (2/4)

	0	1	2	3	4	5	6	7
50	XD_RREGX_WRADR0:B3							
	A31	A30	A29	A28	A27	A26	A25	A24
51	XD_RREGX_WRADR0:B2							
	A23	A22	A21	A20	A19	A18	A17	A16
52	XD_RREGX_WRADR0:B1							
	A15	A14	A13	A12	A11	A10	A9	A8
53	XD_RREGX_WRADR0:B0							
	A7	A6	A5	A4	A3	A2	A1	A0
54	XD_RREGX_WRADR1:B3							
	LMA15	LMA14	LMA13	LMA12	LMA11	LMA10	LMA9	LMA8
55	XD_RREGX_WRADR1:B2							
	LMA7	LMA6	LMA5	LMA4	LMA3	LMA2	LMA1	LMA0
56	XD_RREGX_WRADR1:B1							
	ACC2	ACC1	ACC0	IX	MD3	MD2	MD1	MD0
57	XD_RREGX_WRADR1:B0							
	CL	A38	A37	A36	A35	A34	A33	A32
58	XD_RREGX_RDADR0:B3							
	A31	A30	A29	A28	A27	A26	A25	A24
59	XD_RREGX_RDADR0:B2							
	A23	A22	A21	A20	A19	A18	A17	A16
5A	XD_RREGX_RDADR0:B1							
	A15	A14	A13	A12	A11	A10	A9	A8
5B	XD_RREGX_RDADR0:B0							
	A7	A6	A5	A4	A3	A2	A1	A0
5C	XD_RREGX_RDADR1:B3							
	LMA15	LMA14	LMA13	LMA12	LMA11	LMA10	LMA9	LMA8
5D	XD_RREGX_RDADR1:B2							
	LMA7	LMA6	LMA5	LMA4	LMA3	LMA2	LMA1	LMA0
5E	XD_RREGX_RDADR1:B1							
	ACC2	ACC1	ACC0	IX	MD3	MD2	MD1	MD0
5F	XD_RREGX_RDADR1:B0							
	CL	A38	A37	A36	A35	A34	A33	A32

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Byte27 = 81 (CHK3) Byte40-7F Detail
(11) Byte28 = A2 (3/4)

	0	1	2	3	4	5	6	7
60	XD_RREGX_STS2:B3							
	LRC							
61	XD_RREGX_STS2:B2							
	LRC							
62	XD_RREGX_STS2:B1							
	Error	Not used	Not used	Not used	Not used	Not used	Not used	RD
63	XD_RREGX_STS2:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	END
64	XD_RREGX_SEQSTS:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	XD_RREGX_SEQSTS:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	XD_RREGX_SEQSTS:B1							
	ST N							
67	XD_RREGX_SEQSTS:B0							
	ST							
68	Reserved							
	Reserved							
69	Reserved							
	Reserved							
6A	Reserved							
	Reserved							
6B	Reserved							
	Reserved							
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(11) Byte28 = A2 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(12) Byte28 = 90 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	SMC_ERRSTS_OWNMP:B2							
	Not used	E Micro Error	Not used	Not used	Not used	X CPL Error	D CPL Error	E CPL Error
45	SMC_ERRSTS_OWNMP:B0							
	Not used	Not used	Not used	Not used	CRG CHK1	X CHK1	D CHK1	E CHK1
46	SMC_ERRSTS_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	X Warning	D Warning	E Warning
47	SMC_ERRSTS_OWNMP:B6							
	Not used	Not used	Not used	Not used	Not used	X Slave Error	D Slave Error	E Slave Error
48	SMC_CHK3_ERRLOG_OWNMP:B7							
	Not used	Not used	Not used	Not used	Not used	ECTL NP MULTI Micro Error	ECTL BNDRY Error	ECTL INVDST Error
49	SMC_CHK3_ERRLOG_OWNMP:B6							
	ECTL PREGWT Micro Error	ECTL INDWT Micro Error	ECTL INDRD Micro Error	ECTL ATM Micro Error	ECTL INV CMD Error	ECTL PCODE Error	ECTL SM ACC Error	ECTL ADR INV Error
4A	SMC_CHK3_ERRLOG_OWNMP:B5							
	Not used	Not used	Not used	Not used	Not used	XCTL AUTOCHK TOV Error	XCTL WTCHKRD Error	XCTL AUTOCHK Error
4B	SMC_CHK3_ERRLOG_OWNMP:B4							
	XCTL AUTOCHK STS Error	Not used	Not used	XCTL MERSTS X Error	XCTL ErrorSTS X Error	XCTL CPL TOV Error	XCTL CPL FRCTOV Error	XCTL CPL STS Error
4C	SMC_CHK3_ERRLOG_OWNMP:B3							
	Not used	Not used	Not used	Not used	DCTL AUTOCHK TOV Error	Not used	DCTL WTCHKRD Error	DCTL AUTOCHK Error
4D	SMC_CHK3_ERRLOG_OWNMP:B2							
	DCTL AUTOCHK STS Error	Not used	Not used	Not used	Not used	DCTL CPL FRCTOV Error	DCTL CPL TOV Error	DCTL CPL STS Error
4E	SMC_CHK3_ERRLOG_OWNMP:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4F	SMC_CHK3_ERRLOG_OWNMP:B0							
	Not used	Not used	Not used	Not used	Not used	ECTL CPL FRCTOV Error	ECTL CPL TOV Error	ECTL CPL STS Error

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Byte27 = 81 (CHK3) Byte40-7F Detail
(12) Byte28 = 90 (2/4)

	0	1	2	3	4	5	6	7
50	SMC_ECTL_DSTADR_LOG:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ErrorLog FLG
51	SMC_ECTL_DSTADR_LOG:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
52	SMC_ECTL_DSTADR_LOG:B5							
	Destination Address ACC			Destination Address IX	Destination Address MDL			
53	SMC_ECTL_DSTADR_LOG:B4							
	Destination Address [B4]							
54	SMC_ECTL_DSTADR_LOG:B3							
	Destination Address [B3]							
55	SMC_ECTL_DSTADR_LOG:B2							
	Destination Address [B2]							
56	SMC_ECTL_DSTADR_LOG:B1							
	Destination Address [B1]							
57	SMC_ECTL_DSTADR_LOG:B0							
	Destination Address [B0]							
58	SMC_ECTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
59	SMC_ECTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
5A	SMC_ECTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
5B	SMC_ECTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
5C	SMC_ECTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
5D	SMC_ECTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
5E	SMC_ECTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
5F	SMC_ECTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(12) Byte28 = 90 (3/4)

	0	1	2	3	4	5	6	7
60	SMC_ECTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
61	SMC_ECTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
62	SMC_ECTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
63	SMC_ECTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
64	SMC_ECTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
65	SMC_ECTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
66	SMC_ECTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
67	SMC_ECTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							
68	SMC_ECTL_DAT_LOG:B7							
	Data Log [B7]							
69	SMC_ECTL_DAT_LOG:B6							
	Data Log [B6]							
6A	SMC_ECTL_DAT_LOG:B5							
	Data Log [B5]							
6B	SMC_ECTL_DAT_LOG:B4							
	Data Log [B4]							
6C	SMC_ECTL_DAT_LOG:B3							
	Data Log [B3]							
6D	SMC_ECTL_DAT_LOG:B2							
	Data Log [B2]							
6E	SMC_ECTL_DAT_LOG:B1							
	Data Log [B1]							
6F	SMC_ECTL_DAT_LOG:B0							
	Data Log [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(12) Byte28 = 90 (4/4)

	0	1	2	3	4	5	6	7
70	SMC_DCTL_HDR_LOG_H:B7							
	Not used	Header Log FMT		Header Log TYPE				
71	SMC_DCTL_HDR_LOG_H:B6							
	Header Log 0/1DW [B6]							
72	SMC_DCTL_HDR_LOG_H:B5							
	Header Log 0/1DW [B5]							
73	SMC_DCTL_HDR_LOG_H:B4							
	Header Log 0/1DW [B4]							
74	SMC_DCTL_HDR_LOG_H:B3							
	Header Log 0/1DW [B3]							
75	SMC_DCTL_HDR_LOG_H:B2							
	Header Log 0/1DW [B2]							
76	SMC_DCTL_HDR_LOG_H:B1							
	Header Log 0/1DW [B1]							
77	SMC_DCTL_HDR_LOG_H:B0							
	Header Log 0/1DW [B0]							
78	SMC_DCTL_HDR_LOG_L:B7							
	Header Log 2/3DW [B7]							
79	SMC_DCTL_HDR_LOG_L:B6							
	Header Log 2/3DW [B6]							
7A	SMC_DCTL_HDR_LOG_L:B5							
	Header Log 2/3DW [B5]							
7B	SMC_DCTL_HDR_LOG_L:B4							
	Header Log 2/3DW [B4]							
7C	SMC_DCTL_HDR_LOG_L:B3							
	Header Log 2/3DW [B3]							
7D	SMC_DCTL_HDR_LOG_L:B2							
	Header Log 2/3DW [B2]							
7E	SMC_DCTL_HDR_LOG_L:B1							
	Header Log 2/3DW [B1]							
7F	SMC_DCTL_HDR_LOG_L:B0							
	Header Log 2/3DW [B0]							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(13) Byte28 = 91 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	MPDMA_MD_ENABLE:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	MPDMA_MD_ENABLE:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	MPDMA_MD_ENABLE:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
47	MPDMA_MD_ENABLE:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DMA EN
48	MPDMA_MD_REPAFE:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
49	MPDMA_MD_REPAFE:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO6 REPAFE	Error NO5 REPAFE
4A	MPDMA_MD_REPAFE:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Error NO4 REPAFE
4B	MPDMA_MD_REPAFE:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Error NO2 REPAFE	Error NO1 REPAFE
4C	MPDMA_MD_STS_W5_LOG:B3							
	STS W5 Log							
4D	MPDMA_MD_STS_W5_LOG:B2							
	STS W5 Log							
4E	MPDMA_MD_STS_W5_LOG:B1							
	STS W5 Log							
4F	MPDMA_MD_STS_W5_LOG:B0							
	STS W5 Log							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(13) Byte28 = 91 (2/4)

	0	1	2	3	4	5	6	7
50		MPDMA_MD_ERR_ST09:B3						
				STS W1 Error2				
51		MPDMA_MD_ERR_ST09:B2						
				STS W1 Error2				
52		MPDMA_MD_ERR_ST09:B1						
				STS W1 Error2				
53		MPDMA_MD_ERR_ST09:B0						
				STS W1 Error2				
54		MPDMA_MD_ERR_ST10:B3						
				STS W1 Error2				
55		MPDMA_MD_ERR_ST10:B2						
				STS W1 Error2				
56		MPDMA_MD_ERR_ST10:B1						
				STS W1 Error2				
57		MPDMA_MD_ERR_ST10:B0						
				STS W1 Error2				
58		MPDMA_MD_ERR_ST11:B3						
				STS W1 Error3				
59		MPDMA_MD_ERR_ST11:B2						
				STS W1 Error3				
5A		MPDMA_MD_ERR_ST11:B1						
				STS W1 Error3				
5B		MPDMA_MD_ERR_ST11:B0						
				STS W1 Error3				
5C		MPDMA_MD_ERR_ST12:B3						
				STS W1 Error3				
5D		MPDMA_MD_ERR_ST12:B2						
				STS W1 Error3				
5E		MPDMA_MD_ERR_ST12:B1						
				STS W1 Error3				
5F		MPDMA_MD_ERR_ST12:B0						
				STS W1 Error3				

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Byte27 = 81 (CHK3) Byte40-7F Detail
(13) Byte28 = 91 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	Reserved							
61	Reserved							
	Reserved							
62	Reserved							
	Reserved							
63	Reserved							
	Reserved							
64	Reserved							
	Reserved							
65	Reserved							
	Reserved							
66	Reserved							
	Reserved							
67	Reserved							
	Reserved							
68	Reserved							
	Reserved							
69	Reserved							
	Reserved							
6A	Reserved							
	Reserved							
6B	Reserved							
	Reserved							
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(13) Byte28 = 91 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(14) Byte28 = 00 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
46	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
47	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
48	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
49	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
4A	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
4B	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
4C	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
4D	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4E	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4F	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B

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Byte27 = 81 (CHK3) Byte40-7F Detail
(14) Byte28 = 00 (2/4)

	0	1	2	3	4	5	6	7
50	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
51	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
52	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
53	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B
54	INT0_INT_STATUS4:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
55	INT0_INT_STATUS4:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
56	INT0_INT_STATUS4:B1							
	INT DRR3 CHK2	INT DRR2 CHK2	INT DRR1 CHK2	INT DRR0 CHK2	Not used	Not used	INT DMAMB1 CHK2	INT DMAMB0 CHK2
57	INT0_INT_STATUS4:B0							
	Not used	Not used	INT DMA5 CHK2	INT DMA4 CHK2	INT DMA3 CHK2	INT DMA2 CHK2	INT DMA1 CHK2	INT DMA0 CHK2
58	INT0_INT_STATUS5:B3							
	Not used	Not used	Not used	INT LRP4 WRN	INT LRP3 WRN	INT LRP2 WRN	INT LRP1 WRN	INT LRP0 WRN
59	INT0_INT_STATUS5:B2							
	Not used	Not used	Not used	INT FDMA4 WRN	INT FDMA3 WRN	INT FDMA2 WRN	INT FDMA1 WRN	INT FDMA0 WRN
5A	INT0_INT_STATUS5:B1							
	INT DRR3 WRN	INT DRR2 WRN	INT DRR1 WRN	INT DRR0 WRN	INT MPDMA1 WRN	INT MPDMA0 WRN	INT DMAMB1 WRN	INT DMAMB0 WRN
5B	INT0_INT_STATUS5:B0							
	Not used	Not used	INT DMA5 WRN	INT DMA4 WRN	INT DMA3 WRN	INT DMA2 WRN	INT DMA1 WRN	INT DMA0 WRN
5C	INT0_INT_STATUS6:B3							
	Not used	Not used	Not used	Not used	Not used	INT BARB WRN	INT IARB1 WRN	INT IARB0 WRN
5D	INT0_INT_STATUS6:B2							
	INT EARB1 WRN	INT EARB0 WRN	INT IXARB1 WRN	INT IXARB0 WRN	INT PARB3 WRN	INT PARB2 WRN	INT PARB1 WRN	INT PARB0 WRN
5E	INT0_INT_STATUS6:B1							
	Not used	Not used	Not used	Not used	Not used	INT BARBREG WRN	INT IARB1REG WRN	INT IARB0REG WRN
5F	INT0_INT_STATUS6:B0							
	INT EARB1REG WRN	INT EARB0REG WRN	INT IXARB1REG WRN	INT IXARB0REG WRN	INT PARB3REG WRN	INT PARB2REG WRN	INT PARB1REG WRN	INT PARB0REG WRN

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Byte27 = 81 (CHK3) Byte40-7F Detail
(14) Byte28 = 00 (3/4)

	0	1	2	3	4	5	6	7
60	INT0_INT_STATUS7:B3							
	DC UPDOWN WRN	TX FAULT	PCI CORE WARN	Not used	INT XD WRN	INT BRAM WRN	INT BCOM WRN	INT SMC WRN
61	INT0_INT_STATUS7:B2							
	Not used	Not used	Not used	INT REG2 WRN	INT DXA3 WRN	INT DXA2 WRN	INT DXA1 WRN	INT DXA0 WRN
62	INT0_INT_STATUS7:B1							
	INT DXC3 MICRO	INT DXC2 MICRO	INT DXC1 MICRO	INT DXC0 MICRO	INT DXC3 WRN	INT DXC2 WRN	INT DXC1 WRN	INT DXC0 WRN
63	INT0_INT_STATUS7:B0							
	INT DXC3 WRN DIMM1	INT DXC2 WRN DIMM1	INT DXC1 WRN DIMM1	INT DXC0 WRN DIMM1	INT DXC3 WRN DIMM0	INT DXC2 WRN DIMM0	INT DXC1 WRN DIMM0	INT DXC0 WRN DIMM0
64	INT0_INT_STATUS10:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	INT0_INT_STATUS10:B2							
	Not used	INT XD CHK4	INT IXARB1REG CHK4	INT IXARB1 CHK4	Not used	INT XD CHK4	INT IXARB0REG CHK4	INT IXARB0 CHK4
66	INT0_INT_STATUS10:B1							
	Not used	INT XD CHK4	INT PARB3REG CHK4	INT PARB3 CHK4	Not used	INT XD CHK4	INT PARB2REG CHK4	INT PARB2 CHK4
67	INT0_INT_STATUS10:B0							
	Not used	INT XD CHK4	INT PARB1REG CHK4	INT PARB1 CHK4	Not used	INT XD CHK4	INT PARB0REG CHK4	INT PARB0 CHK4
68	INT0_INT_STATUS11:B3							
	Not used	Not used	Not used	INT XD CHK4	Not used	Not used	Not used	Not used
69	INT0_INT_STATUS11:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	INT BARBREG CHK4	INT BARB CHK4
6A	INT0_INT_STATUS11:B1							
	Not used	Not used	INT IARB1REG CHK4	INT IARB1 CHK4	Not used	Not used	INT IARB0REG CHK4	INT IARB0 CHK4
6B	INT0_INT_STATUS11:B0							
	Not used	Not used	INT EARB1REG CHK4	INT EARB1 CHK4	Not used	Not used	INT EARB0REG CHK4	INT EARB0 CHK4
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(14) Byte28 = 00 (4/4)

	0	1	2	3	4	5	6	7
70	DXC_REP_ERROR ::DXC0 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
71	DXC_REP_ERROR ::DXC0 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	DXC_REP_ERROR ::DXC0 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
73	DXC_REP_ERROR ::DXC0 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
74	DXC_REP_ERROR ::DXC1 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
75	DXC_REP_ERROR ::DXC1 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	DXC_REP_ERROR ::DXC1 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
77	DXC_REP_ERROR ::DXC1 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
78	DXC_REP_ERROR ::DXC2 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
79	DXC_REP_ERROR ::DXC2 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	DXC_REP_ERROR ::DXC2 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7B	DXC_REP_ERROR ::DXC2 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7C	DXC_REP_ERROR ::DXC3 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
7D	DXC_REP_ERROR ::DXC3 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7E	DXC_REP_ERROR ::DXC3 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7F	DXC_REP_ERROR ::DXC3 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 81 (CHK3) Byte40-7F Detail
(15) Byte28 = F0 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_CHK3_STS_MPx:B3							
	FRC CHK3	Not used	Not used	Not used	REG2 CHK3 INT	REG2 CHK3	REG0 CHK3 INT	REG0 CHK3
41	INT0_INT_CHK3_STS_MPx:B2							
	Not used	Not used	Not used	SMC SLAVE CHK3	SMC CHK3 INT	SMC CHK3	XD CHK3 INT	XD CHK3
42	INT0_INT_CHK3_STS_MPx:B1							
	MPDMA1 CHK3 INT	MPDMA1 CHK3	MPDMA0 CHK3 INT	MPDMA0 CHK3	DXC3 CHK3 LOGRAM	DXC2 CHK3 LOGRAM	DXC1 CHK3 LOGRAM	DXC0 CHK3 LOGRAM
43	INT0_INT_CHK3_STS_MPx:B0							
	DXC3 CHK3 DIMM1	DXC3 CHK3 DIMM0	DXC2 CHK3 DIMM1	DXC2 CHK3 DIMM0	DXC1 CHK3 DIMM1	DXC1 CHK3 DIMM0	DXC0 CHK3 DIMM1	DXC0 CHK3 DIMM0
44	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
46	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
47	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
48	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
49	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
4A	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
4B	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
4C	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
4D	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4E	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4F	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B

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Byte27 = 81 (CHK3) Byte40-7F Detail
(15) Byte28 = F0 (2/4)

	0	1	2	3	4	5	6	7
50	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
51	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
52	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
53	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B
54	INT0_INT_STATUS4:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
55	INT0_INT_STATUS4:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
56	INT0_INT_STATUS4:B1							
	INT DRR3 CHK2	INT DRR2 CHK2	INT DRR1 CHK2	INT DRR0 CHK2	Not used	Not used	INT DMAMB1 CHK2	INT DMAMB0 CHK2
57	INT0_INT_STATUS4:B0							
	Not used	Not used	INT DMA5 CHK2	INT DMA4 CHK2	INT DMA3 CHK2	INT DMA2 CHK2	INT DMA1 CHK2	INT DMA0 CHK2
58	INT0_INT_STATUS5:B3							
	Not used	Not used	Not used	INT LRP4 WRN	INT LRP3 WRN	INT LRP2 WRN	INT LRP1 WRN	INT LRP0 WRN
59	INT0_INT_STATUS5:B2							
	Not used	Not used	Not used	INT FDMA4 WRN	INT FDMA3 WRN	INT FDMA2 WRN	INT FDMA1 WRN	INT FDMA0 WRN
5A	INT0_INT_STATUS5:B1							
	INT DRR3 WRN	INT DRR2 WRN	INT DRR1 WRN	INT DRR0 WRN	INT MPDMA1 WRN	INT MPDMA0 WRN	INT DMAMB1 WRN	INT DMAMB0 WRN
5B	INT0_INT_STATUS5:B0							
	Not used	Not used	INT DMA5 WRN	INT DMA4 WRN	INT DMA3 WRN	INT DMA2 WRN	INT DMA1 WRN	INT DMA0 WRN
5C	INT0_INT_STATUS6:B3							
	Not used	Not used	Not used	Not used	Not used	INT BARB WRN	INT IARB1 WRN	INT IARB0 WRN
5D	INT0_INT_STATUS6:B2							
	INT EARB1 WRN	INT EARB0 WRN	INT IXARB1 WRN	INT IXARB0 WRN	INT PARB3 WRN	INT PARB2 WRN	INT PARB1 WRN	INT PARB0 WRN
5E	INT0_INT_STATUS6:B1							
	Not used	Not used	Not used	Not used	Not used	INT BARBREG WRN	INT IARB1REG WRN	INT IARB0REG WRN
5F	INT0_INT_STATUS6:B0							
	INT EARB1REG WRN	INT EARB0REG WRN	INT IXARB1REG WRN	INT IXARB0REG WRN	INT PARB3REG WRN	INT PARB2REG WRN	INT PARB1REG WRN	INT PARB0REG WRN

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Byte27 = 81 (CHK3) Byte40-7F Detail
(15) Byte28 = F0 (3/4)

	0	1	2	3	4	5	6	7
60	INT0_INT_STATUS7:B3							
	DC UPDOWN WRN	TX FAULT	PCI CORE WARN	Not used	INT XD WRN	INT BRAM WRN	INT BCOM WRN	INT SMC WRN
61	INT0_INT_STATUS7:B2							
	Not used	Not used	Not used	INT REG2 WRN	INT DXA3 WRN	INT DXA2 WRN	INT DXA1 WRN	INT DXA0 WRN
62	INT0_INT_STATUS7:B1							
	INT DXC3 MICRO	INT DXC2 MICRO	INT DXC1 MICRO	INT DXC0 MICRO	INT DXC3 WRN	INT DXC2 WRN	INT DXC1 WRN	INT DXC0 WRN
63	INT0_INT_STATUS7:B0							
	INT DXC3 WRN DIMM1	INT DXC2 WRN DIMM1	INT DXC1 WRN DIMM1	INT DXC0 WRN DIMM1	INT DXC3 WRN DIMM0	INT DXC2 WRN DIMM0	INT DXC1 WRN DIMM0	INT DXC0 WRN DIMM0
64	INT0_INT_STATUS10:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	INT0_INT_STATUS10:B2							
	Not used	INT XD CHK4	INT IXARB1REG CHK4	INT IXARB1 CHK4	Not used	INT XD CHK4	INT IXARB0REG CHK4	INT IXARB0 CHK4
66	INT0_INT_STATUS10:B1							
	Not used	INT XD CHK4	INT PARB3REG CHK4	INT PARB3 CHK4	Not used	INT XD CHK4	INT PARB2REG CHK4	INT PARB2 CHK4
67	INT0_INT_STATUS10:B0							
	Not used	INT XD CHK4	INT PARB1REG CHK4	INT PARB1 CHK4	Not used	INT XD CHK4	INT PARB0REG CHK4	INT PARB0 CHK4
68	INT0_INT_STATUS11:B3							
	Not used	Not used	Not used	INT XD CHK4	Not used	Not used	Not used	Not used
69	INT0_INT_STATUS11:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	INT BARBREG CHK4	INT BARB CHK4
6A	INT0_INT_STATUS11:B1							
	Not used	Not used	INT IARB1REG CHK4	INT IARB1 CHK4	Not used	Not used	INT IARB0REG CHK4	INT IARB0 CHK4
6B	INT0_INT_STATUS11:B0							
	Not used	Not used	INT EARB1REG CHK4	INT EARB1 CHK4	Not used	Not used	INT EARB0REG CHK4	INT EARB0 CHK4
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 81 (CHK3) Byte40-7F Detail
(15) Byte28 = F0 (4/4)

	0	1	2	3	4	5	6	7
70	DXC_REP_ERROR ::DXC0 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
71	DXC_REP_ERROR ::DXC0 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	DXC_REP_ERROR ::DXC0 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
73	DXC_REP_ERROR ::DXC0 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
74	DXC_REP_ERROR ::DXC1 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
75	DXC_REP_ERROR ::DXC1 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	DXC_REP_ERROR ::DXC1 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
77	DXC_REP_ERROR ::DXC1 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
78	DXC_REP_ERROR ::DXC2 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
79	DXC_REP_ERROR ::DXC2 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	DXC_REP_ERROR ::DXC2 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7B	DXC_REP_ERROR ::DXC2 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7C	DXC_REP_ERROR ::DXC3 :B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
7D	DXC_REP_ERROR ::DXC3 :B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7E	DXC_REP_ERROR ::DXC3 :B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7F	DXC_REP_ERROR ::DXC3 :B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 84 (CHK4)

	0	1	2	3	4	5	6	7
00 | 05	Time stamp							
06	Format Message							
07	Processor ID							
08 | 09	System error code							
0A | 0B	JCB#							
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK Information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	Reserved					
10	JCB ID							
11	LDEV#high (Logical DKC#)							
12 | 13	LDEV#low (LDEV# in DKC)							
14	CDEV#							
15	RDEV#							
16 | 17	SSB log number							
18 | 19	Related failure log number							
1A | 1B	Related SIM log number							
1C | 1D	Related SSB log number							
1E	Reserved							
1F	SCB							
20 | 26	Reserved							
27	Format (x‘8’)				Message (x‘4’)			
28	Subcode (See following pages)							
29 | 31	Detail information (See following pages)							
32	Module ID							
33	Routine ID							
34	PCB number (*1)				Message code (x‘0’)			
35	SSID of self storage system (low)							
36 | 37	Symptom code (x‘FF84’)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A | 3B	Configuration information							
3C	Not used							
3D | 3F	Reserved							
40 | 7F	Hardwre information (See following pages)							

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Byte27 = 84 (CHK4) Byte28-31

(1) Byte28 = 20/21/22/23/24/25 (FC IFB CHK4 – PCI 0 ~ 5 Error1)
Byte28 = 28/29/2a/2b/2c/2d (FC IFB CHK4 – PCI 0 ~ 5 Error2)
Byte28 = 30/31/32/33/34/35 (FC IFB CHK4 – FC Protocol 0 ~ 5 Error)
Byte28 = 36/37/38/39 (FC IFB CHK4 – LRP 0 ~ 3 Error)
Byte28 = 3a (FC IFB CHK4 – No HW Error)

	0	1	2	3	4	5	6	7
28	Subcode (x‘20’ or x‘21’ or x‘22’ or x‘23’ or x‘24’ or x‘25’ : FC IFB CHK4 – PCI 0 ~ 5 Error1) Subcode (x‘28’ or x‘29’ or x‘2a’ or x‘2b’ or x‘2c’ or x‘2d’ : FC IFB CHK4 – PCI 0 ~ 5 Error2) Subcode (x‘30’ or x‘31’ or x‘32’ or x‘33’ or x‘34’ or x‘35’ : FC IFB CHK4 – FC Protocol 0 ~ 5 Error) Subcode (x‘36’ or x‘37’ or x‘38’ or x‘39’ : FC IFB CHK4 – LRP 0 ~ 3 Error) Subcode (x‘3a’ : FC IFB CHK4 – No HW Error)							
29	INT0_HMA_STATUS (b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM(0)	(RSV)	(RSV)	IX MODE
2A	INT0_HMA_STATUS (b15 – 08)							
	HMA REV(7)	HMA REV(6)	HMA REV(5)	HMA REV(4)	HMA REV(3)	HMA REV(2)	HMA REV(1)	HMA REV(0)
2B	LRP_INFO_TABLE04 (b23 – 16)							
	(RSV)	(RSV)	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
2C	LRP_INFO_TABLE04 (b15 – 08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
2D	LRP_INFO_TABLE04 (b7 – 0)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	(RSV)	(RSV)	(RSV)	HMA EN
2E	INT_STATUS0 (b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2F	INT_STATUS0 (b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
30	INT_STATUS0 (b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
31	INT_STATUS0 (b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B

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Byte27 = 84 (CHK4) Byte28-31

(2) Byte28 = 40/41/42/43/44/45 (SAS IFB CHK4 – PCI 0 ~ 5 Error1)
Byte28 = 48/49/4a/4b/4c/4d (SAS IFB CHK4 – PCI 0 ~ 5 Error2)
Byte28 = 50/51/52/53/54/55 (SAS IFB CHK4 – FC Protocol 0 ~ 5 Error)
Byte28 = 56/57/58/59 (SAS IFB CHK4 – LRP 0 ~ 3 Error)
Byte28 = 5a (SAS IFB CHK4 – No HW Error)

	0	1	2	3	4	5	6	7
28	Subcode (x‘40’ or x‘41’ or x‘42’ or x‘43’ or x‘44’ or x‘45’ : SAS IFB CHK4 – PCI 0 ~ 5 Error1) Subcode (x‘48’ or x‘49’ or x‘4a’ or x‘4b’ or x‘4c’ or x‘4d’ : SAS IFB CHK4 – PCI 0 ~ 5 Error2) Subcode (x‘50’ or x‘51’ or x‘52’ or x‘53’ or x‘54’ or x‘55’ : SAS IFB CHK4 – FC Protocol 0 ~ 5 Error) Subcode (x‘56’ or x‘57’ or x‘58’ or x‘59’ : SAS IFB CHK4 – LRP 0 ~ 3 Error) Subcode (x‘5a’ : SAS IFB CHK4 – No HW Error)							
29	INT0_HMA_STATUS (b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM(0)	(RSV)	(RSV)	IX MODE
2A	INT0_HMA_STATUS (b15 – 08)							
	HMA REV(7)	HMA REV(6)	HMA REV(5)	HMA REV(4)	HMA REV(3)	HMA REV(2)	HMA REV(1)	HMA REV(0)
2B	LRP_INFO_TABLE04 (b23 – 16)							
	(RSV)	(RSV)	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
2C	LRP_INFO_TABLE04 (b15 – 08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
2D	LRP_INFO_TABLE04 (b7 – 0)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	(RSV)	(RSV)	(RSV)	HMA EN
2E	INT_STATUS0 (b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2F	INT_STATUS0 (b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
30	INT_STATUS0 (b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
31	INT_STATUS0 (b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(1) Byte28 = 20/40 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(2) Byte28 = 21/41 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(3) Byte28 = 22/42 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(4) Byte28 = 23/43 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(5) Byte28 = 24/44 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(6) Byte28 = 25/45 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(7) Byte28 = 28/48 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(8) Byte28 = 29/49 ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(9) Byte28 = 2A/4A ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(10) Byte28 = 2B/4B ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(11) Byte28 = 2C/4C ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0 (bit31 -24)							
	Reserved	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRC ERR	Reserved	RXHDBUF WTPT PERR	Reserved
41	HMA: XARB_RX_PCK_ERR0 (bit23 -16)							
	Reserved	RXNDBUF WTPT PERR	RXHDIX PERR	Reserved	RXDT WTADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RCRC CMP PERR
42	HMA: XARB_RX_PCK_ERR0 (bit15 -08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	P2C CNT PERR	RX PERR	RXNDBUF INGPERR	RXDTIX DTCMP PERR	RXDTIX WADR PERR
43	HMA: XARB_RX_PCK_ERR0 (bit07 -00)							
	TAGxTMR SEQ PERR	TAGxTMR ENCERR	TAGxTMR GPERR	BACNT GPERR	RX_PCK CHK4TOP	RX_PCK CHK1TOP	RX_PCK WRN_TOP	Reserved
44	HMA: XARB_PCI_ECC_RCV (bit31 -24)							
	PCI ECC RCV	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARB_PCI_ECC_RCV (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: XARB_PCI_ECC_RCV (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: XARB_PCI_ECC_RCV (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: XARB_TAGXTMR_GPERR (bit31 -24)							
	TAG0 TMR GPERR	TAG1 TMR GPERR	TAG2 TMR GPERR	TAG3 TMR GPERR	TAG4 TMR GPERR	TAG5 TMR GPERR	TAG6 TMR GPERR	TAG7 TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR (bit23 -16)							
	TAG8 TMR GPERR	TAG9 TMR GPERR	TAG10 TMR GPERR	TAG11 TMR GPERR	TAG12 TMR GPERR	TAG13 TMR GPERR	TAG14 TMR GPERR	TAG15 TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR (bit15 -08)							
	TAG16 TMR GPERR	TAG17 TMR GPERR	TAG18 TMR GPERR	TAG19 TMR GPERR	TAG20 TMR GPERR	TAG21 TMR GPERR	TAG22 TMR GPERR	TAG23 TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR (bit07 -00)							
	TAG24 TMR GPERR	TAG25 TMR GPERR	TAG26 TMR GPERR	TAG27 TMR GPERR	TAG28 TMR GPERR	TAG29 TMR GPERR	TAG30 TMR GPERR	TAG31 TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit31 -24)							
	TAG0TMR SEQ EERR	TAG1TMR SEQ EERR	TAG2TMR SEQ EERR	TAG3TMR SEQ EERR	TAG4TMR SEQ EERR	TAG5TMR SEQ EERR	TAG6TMR SEQ EERR	TAG7TMR SEQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit23 -16)							
	TAG8TMR SEQ EERR	TAG9TMR SEQ EERR	TAG10TMR SEQ EERR	TAG11TMR SEQ EERR	TAG12TMR SEQ EERR	TAG13TMR SEQ EERR	TAG14TMR SEQ EERR	TAG15TMR SEQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit15 -08)							
	TAG16TMR SEQ EERR	TAG17TMR SEQ EERR	TAG18TMR SEQ EERR	TAG19TMR SEQ EERR	TAG20TMR SEQ EERR	TAG21TMR SEQ EERR	TAG22TMR SEQ EERR	TAG23TMR SEQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR (bit07 -00)							
	TAG24TMR SEQ EERR	TAG25TMR SEQ EERR	TAG26TMR SEQ EERR	TAG27TMR SEQ EERR	TAG28TMR SEQ EERR	TAG29TMR SEQ EERR	TAG30TMR SEQ EERR	TAG31TMR SEQ EERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR (bit31 -24)							
	TAG0TMR SEQ PERR	TAG1TMR SEQ PERR	TAG2TMR SEQ PERR	TAG3TMR SEQ PERR	TAG4TMR SEQ PERR	TAG5TMR SEQ PERR	TAG6TMR SEQ PERR	TAG7TMR SEQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR (bit23 -16)							
	TAG8TMR SEQ PERR	TAG9TMR SEQ PERR	TAG10TMR SEQ PERR	TAG11TMR SEQ PERR	TAG12TMR SEQ PERR	TAG13TMR SEQ PERR	TAG14TMR SEQ PERR	TAG15TMR SEQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR (bit15 -08)							
	TAG16TMR SEQ PERR	TAG17TMR SEQ PERR	TAG18TMR SEQ PERR	TAG19TMR SEQ PERR	TAG20TMR SEQ PERR	TAG21TMR SEQ PERR	TAG22TMR SEQ PERR	TAG23TMR SEQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR (bit07 -00)							
	TAG24TMR SEQ PERR	TAG25TMR SEQ PERR	TAG26TMR SEQ PERR	TAG27TMR SEQ PERR	TAG28TMR SEQ PERR	TAG29TMR SEQ PERR	TAG30TMR SEQ PERR	TAG31TMR SEQ PERR
54	HMA: XARB_TAGXTMR_TOERR (bit31 -24)							
	TAG0TMR TO ERR	TAG1TMR TO ERR	TAG2TMR TO ERR	TAG3TMR TO ERR	TAG4TMR TO ERR	TAG5TMR TO ERR	TAG6TMR TO ERR	TAG7TMR TO ERR
55	HMA: XARB_TAGXTMR_TOERR (bit23 -16)							
	TAG8TMR TO ERR	TAG9TMR TO ERR	TAG10TMR TO ERR	TAG11TMR TO ERR	TAG12TMR TO ERR	TAG13TMR TO ERR	TAG14TMR TO ERR	TAG15TMR TO ERR
56	HMA: XARB_TAGXTMR_TOERR (bit15 -08)							
	TAG16TMR TO ERR	TAG17TMR TO ERR	TAG18TMR TO ERR	TAG19TMR TO ERR	TAG20TMR TO ERR	TAG21TMR TO ERR	TAG22TMR TO ERR	TAG23TMR TO ERR
57	HMA: XARB_TAGXTMR_TOERR (bit07 -00)							
	TAG24TMR TO ERR	TAG25TMR TO ERR	TAG26TMR TO ERR	TAG27TMR TO ERR	TAG28TMR TO ERR	TAG29TMR TO ERR	TAG30TMR TO ERR	TAG31TMR TO ERR
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	HMA: XARB_TX_PCK_ERR0 (bit31 -24)							
	TXHDBUF RDPT PERR	TXNHBUF RDPT PERR	TXNHBUF WTPT PERR	TXNDBUF RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0 (bit23 -16)							
	NHETY ERR	PDETY ERR	PHETY ERR	QETY ERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0 (bit15 -08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDTBUF RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0 (bit07 -00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	Reserved	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1 (bit31 -24)							
	ICNT_PERR	TXHDDT APERR	TXHDDT EPERR	Reserved	ICNT NPPERR	NPHDBUF PERR	TXDTBUF PERR	TXNDBUF PERR
61	HMA: XARB_TX_PCK_ERR1 (bit23 -16)							
	CHCNT PERR	NHCNT PERR	PHCNT PERR	CDCNT PERR	NDCNT PERR	PDCNT PERR	TXDTBUF ADRERR	TXDTBUF UNCERR
62	HMA: XARB_TX_PCK_ERR1 (bit15 -08)							
	FCTMR SEQ PERR	FCTMR SEQ ENCERR	FCTMR GPERR	FCTMR TOERR	Reserved	Reserved	Reserved	Reserved
63	HMA: XARB_TX_PCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN_TOP	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	HMA: XARB_RX_UCK_ERR0 (bit31 -24)							
	RXHDBUF RDPT PERR	RXDTBUF ADR ERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDT RDADR PERR	RXHDOX PERR	WCRC CMP PERR
69	HMA: XARB_RX_UCK_ERR0 (bit23 -16)							
	RXNHOX PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0 (bit15 -08)							
	SWTX DT_L GPERR	SWTX ENCERR	SWTX HLRC GERR	Reserved	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	Reserved
6B	HMA: XARB_RX_UCK_ERR0 (bit07 -00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1 (bit31 -24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	RXNHBUF OVER RUN	Reserved	Reserved
6D	HMA: XARB_RX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: XARB_RX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	HMA: XARB_RX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN_TOP	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARB_TX_UCK_ERR0 (bit31 -24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW_DT GPERR	SWRX SW_VLD GERR	SWRX TOCNT GPERR
71	HMA: XARB_TX_UCK_ERR0 (bit23 -16)							
	SWRX TOCNT TO	SWRX TX_ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	Reserved	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
72	HMA: XARB_TX_UCK_ERR0 (bit15 -08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	Reserved	TXNHCNT PERR	SWRX REQOFF ERR	SWRX SW_HD PERR	DATCNT PERR
73	HMA: XARB_TX_UCK_ERR0 (bit07 -00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
74	HMA: XARB_TX_UCK_ERR1 (bit31 -24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	MIC CHK1ERR	TXDTIX DTCMP PERR	TXDTIX WACMP PERR
75	HMA: XARB_TX_UCK_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	HMA: XARB_TX_UCK_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: XARB_TX_UCK_ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN_TOP	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARBREG_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XARBREG_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WARNING STATUS
42	HMA: XARBREG_ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK4 ERROR STATUS
43	HMA: XARBREG_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CHK1B ERROR STATUS
44	HMA: XARBREG_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XARBREG_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL WRN	PCIREG ERRREG WRN	PCIREG LINK WRN
46	HMA: XARBREG_ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIREG INTCTL CHK4ERR	PCIREG ERRREG CHK4ERR	PCIREG LINK CHK4ERR
47	HMA: XARBREG_ERR1 (bit07 -00)							
	ADRCMP CHK1B ERR	SYNC CHK1B ERR	REGIF CHK1B ERR	AHBIF1 CHK1B ERR	AHBIF0 CHK1B ERR	Reserved	PCIREG ERRREG CHK1BERR	PCIREG LINK CHK1BERR
48	HMA: XARBREG_INTCTL_MSG_REQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XARBREG_INTCTL_MSG_REQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: XARBREG_INTCTL_MSG_REQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG_MSG_TX_TYPE(1:0)	
4B	HMA: XARBREG_INTCTL_MSG_REQ (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG MSG TX_REQ
4C	HMA: XARBREG_INTCTL_EXP_INT (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	HMA: XARBREG_INTCTL_EXP_INT (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	HMA: XARBREG_INTCTL_EXP_INT (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XARBREG_INTCTL_EXP_INT (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CRG EXPCAP INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK4	ZPEX_DLM ECCERR NORCHK4	ZPEX_TLM ECCERR TX0CHK4	ZPEX_TLM ECCERR RX0CHK4	ZPEX_TLM PERRALLOC CHK4	ZPEX_TLM PERR RX0CHK4	ZPEX_TLM PERR STOPCHK4	ZPEX_TLM PERR TX0CHK4
53	HMA: XARBREG_ERRREG ZPEX_ERR0 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK4	ZPEX_DLM ECCRECOV NORCHK4	ZPEX_TLM ECCRECOV TX0CHK4	ZPEX_TLM ECCRECOV RX0CHK4	Reserved	Reserved	ZPEX_ERR INJECC RECOVCHK4	ZPEX_ERR INJECC ERRCHK4
54	HMA: XARBREG_ERRREG ERR0 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK4	TLM RX0 ERR HK4	Reserved	Reserved	Reserved	TLM TX0 ERRCHK4
55	HMA: XARBREG_ERRREG ERR0 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERR CHK4	TLM ROVF ERR CHK4	TLM PTLP ERR CHK4	TLM MFTLP ERR CHK4	TLM ECRC ERR CHK4	TLM UR ERR CHK4
56	HMA: XARBREG_ERRREG ERR0 (bit15 -08)							
	Reserved	Reserved	SURPRISE DWERR CHK4	DLM PTC ERR CHK4	DLM TLP ERR CHK4	DLM DLLP ERR CHK4	DLM REPLAY_RO ERR CHK4	DLM REPLAY_TO ERR CHK4
57	HMA: XARBREG_ERRREG ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERR CHK4
58	HMA: XARBREG LINK ERR0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XARBREG LINK ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XARBREG LINK ERR0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	HMA: XARBREG LINK ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK4	PLM LINKTR ERR CHK4	DLM VC0_EN ERR CHK4	DLM DL_UP ERR CHK4
5C	HMA: ADRCMPPTY ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: ADRCMPPTY ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: ADRCMPPTY ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	HMA: ADRCMPPTY ERR (bit07 -00)							
	Reserved	ADR CMPERROR b6	ADR CMPERROR b5	Reserved	ADR CMPERROR b3	Reserved	ADR CMPERROR b1	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: SYNC ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: SYNC ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: SYNC ERR (bit15 -08)							
	AHBREGEN AMSET ERR	AHBREGEN BMCLR ERR	Reserved	Reserved	Reserved	ASREGVLD AMSET ERR	RGIFEN BMCLR ERR	ASREGEN BMCLR ERR
63	HMA: SYNC ERR (bit07 -00)							
	AHBREG VLDBMCLR ERR	AHBREG ENAMSET ERR	Reserved	Reserved	Reserved	ASREG VLDBMCLR ERR	RGIFEN AMSET ERR	ASREGEN AMSET ERR
64	HMA: RGIF ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: RGIF ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	HMA: RGIF ERR (bit15 -08)							
	Reserved	Reserved	Reserved	TIMER PARITY ERR	SEQ TMOUT ERR	SEQ PARITY ERR	Reserved	SEQ ENC ERR
67	HMA: RGIF ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
68	HMA: AHBIF0 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
69	HMA: AHBIF0 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	HMA: AHBIF0 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6B	HMA: AHBIF0 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR
6C	HMA: AHBIF1 ERR (bit31 -24)							
	AHBSEQ STATUS(07:00)							
6D	HMA: AHBIF1 ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: AHBIF1 ERR (bit15 -08)							
	Reserved	Reserved	Reserved	SEQ TIMER PERR	SEQ TMOUT ERR	Reserved	SEQ ENC ERR	SEQ PERR
6F	HMA: AHBIF1 ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	HW ERR

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XARBREG ERRREG ZPEX_ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit15 -08)							
	ZPEX_DLM ECCERR REPCHK1B	ZPEX_DLM ECCERR NORCHK1B	ZPEX_TLM ECCERR TX0CHK1B	ZPEX_TLM ECCERR RX0CHK1B	ZPEX_TLM PERRALLOC CHK1B	ZPEX_TLM PERR RX0CHK1B	ZPEX_TLM PERR STOPCHK1B	ZPEX_TLM PERR TX0CHK1B
73	HMA: XARBREG_ERRREG ZPEX_ERR1 (bit07 -00)							
	ZPEX_DLM ECCRECOV REPCHK1B	ZPEX_DLM ECCRECOV NORCHK1B	ZPEX_TLM ECCRECOV TX0CHK1B	ZPEX_TLM ECCRECOV RX0CHK1B	Reserved	Reserved	ZPEX_ERR INJECC RECOCHK1B	ZPEX_ERR INJECC ERRCHK1B
74	HMA: XARBREG_ERRREG ERR1 (bit31 -24)							
	Reserved	Reserved	RX0 STATUS ERRCHK1B	TLM RX0 ERRCHK1B	Reserved	Reserved	Reserved	TLM TX0 ERRCHK1B
75	HMA: XARBREG_ERRREG ERR1 (bit23 -16)							
	Reserved	Reserved	TLM FCPTC ERRCHK1B	TLM ROVF ERRCHK1B	TLM PTLP ERRCHK1B	TLM MFTLP ERRCHK1B	TLM ECRC ERRCHK1B	TLM UR ERRCHK1B
76	HMA: XARBREG_ERRREG ERR1 (bit15 -08)							
	Reserved	Reserved	SURPRISE DW_ERR CHK1B	DLM PTC ERRCHK1B	DLM TLP ERRCHK1B	DLM DLLP ERRCHK1B	DLM REPLAY_RO ERRCHK1B	DLM REPLAY_TO ERRCHK1B
77	HMA: XARBREG_ERRREG ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLM RECEIVER ERRCHK1B
78	HMA: XARBREG LINK ERR1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	HMA: XARBREG LINK ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	HMA: XARBREG LINK ERR1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	HMA: XARBREG LINK ERR1 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	PLM LTSSM ERRCHK1B	PLM LINKTR ERRCHK1B	DLM VC0_EN ERRCHK1B	DLM DL_UP ERRCHK1B
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: ZCORE_LINKSTS (bit31 -24)							
	LINK AUTO BW STS	LINK BW MANAG STS	DLL LINK ACTIVE	SLOT CLK CONFIG	LINK TRAINING	Reserved	NEGO LINK WIDTH(05:04)	
41	HMA: ZCORE_LINKSTS (bit23 -16)							
	NEGO LINK WIDTH(03:00)				CURRENT LINK SPD(03:00)			
42	HMA: ZCORE_LINKSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	LINK AUTO INT EN	LINK BW MANAG INT EN	HW AUTO WIDTH DISABLE	Reserved
43	HMA: ZCORE_LINKSTS (bit07 -00)							
	EXTEND SYNCH	COMMON CLK CONFIG	RETRAIN LINK	LINK DISABLE	READ COMP BOUND	Reserved	ASPM CTL(01:00)	
44	HMA: ZCORE_LANEERRSTS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: ZCORE_LANEERRSTS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: ZCORE_LANEERRSTS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: ZCORE_LANEERRSTS (bit07 -00)							
	LANE ERR STS BIT(07:00)							
48	HMA: ZCORE_ERR_DETCT_ENB (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: ZCORE_ERR_DETCT_ENB (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVE ERR DETCT EN
4A	HMA: ZCORE_ERR_DETCT_ENB (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	POISONED REQ TLP HANDLING	FC ERR DETCT EN1	CFG IO REQ ERR DETCT EN	FC-UPDT TO EN
4B	HMA: ZCORE_ERR_DETCT_ENB (bit07 -00)							
	Reserved	RCB ERR DETCT EN	INTX MSG TLP ERR DETCT EN	BYTE EN ERR DETCT EN	MEM ACC ADR BUND ERR EN	FC ERR DETCT EN0	FC RCV OF DETCT EN	CA DETCT EN
4C	HMA: ZCORE_ERR_STAT_CNT0 (bit31 -24)							
	POISONDE TLP ERR CNT(07:00)							
4D	HMA: ZCORE_ERR_STAT_CNT0 (bit23 -16)							
	ECRC ERR CNT(07:00)							
4E	HMA: ZCORE_ERR_STAT_CNT0 (bit15 -08)							
	FC UPDATE TIMEOUT ERR CNT(07:00)							
4F	HMA: ZCORE_ERR_STAT_CNT0 (bit07 -00)							
	RECEIVER ERR CNT(07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: ZCORE_ERR_STAT_CNT1 (bit31 -24)							
	REPLAY TIMER TIMEOUT ERR CNT(07:00)							
51	HMA: ZCORE_ERR_STAT_CNT1 (bit23 -16)							
	REPLAY NUM ROLLOVER ERR CNT(07:00)							
52	HMA: ZCORE_ERR_STAT_CNT1 (bit15 -08)							
	BAD DLLP ERR CNT(07:00)							
53	HMA: ZCORE_ERR_STAT_CNT1 (bit07 -00)							
	BAD TLP ERR CNT(07:00)							
54	HMA: ZCORE_ERR_STAT_CNT2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: ZCORE_ERR_STAT_CNT2 (bit23 -16)							
	RX NG DEFRAMING PATTERN BUFF OVERFLOW CNT(07:00)							
56	HMA: ZCORE_ERR_STAT_CNT2 (bit15 -08)							
	RX NG DEFRAMING PATTERN EVENT CNT(07:00)							
57	HMA: ZCORE_ERR_STAT_CNT2 (bit07 -00)							
	RX NAK DLLP CNT							
58	HMA: ZCORE_LTSSM_STS (bit31 -24)							
	PIPE POWER STS(01:00)		CURRENT DEV POWER STS(01:00)		Reserved		CURRENT LINK POWER STS(02:00)	
59	HMA: ZCORE_LTSSM_STS (bit23 -16)							
	Reserved	EXT LTSSM SUB STATE(02:00)			Reserved		LTSSM SUB-SUB STATE(02:00)	
5A	HMA: ZCORE_LTSSM_STS (bit15 -08)							
	Reserved	TX OS CODE(02:00)			Reserved		RX OS CODE(02:00)	
5B	HMA: ZCORE_LTSSM_STS (bit07 -00)							
	Reserved	LTSSM SUB STATE(02:00)			LTSSM STATE(03:00)			
5C	HMA: ZCORE_PLM_REPORT_PORT0 (bit31 -24)							
	LANE1 RECEIVER DISPARITY ERR CNT(03:00)				LANE1 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5D	HMA: ZCORE_PLM_REPORT_PORT0 (bit23 -16)							
	LANE1 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE1 8B/10B DECODER ERR CNT(03:00)			
5E	HMA: ZCORE_PLM_REPORT_PORT0 (bit15 -08)							
	LANE0 RECEIVER DISPARITY ERR CNT(03:00)				LANE0 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
5F	HMA: ZCORE_PLM_REPORT_PORT0 (bit07 -00)							
	LANE0 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE0 8B/10B DECODER ERR CNT(03:00)			

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: ZCORE_PLM_REPORT_PORT1 (bit31 -24)							
	LANE3 RECEIVER DISPARITY ERR CNT(03:00)				LANE3 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
61	HMA: ZCORE_PLM_REPORT_PORT1 (bit23 -16)							
	LANE3 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE3 8B/10B DECODER ERR CNT(03:00)			
62	HMA: ZCORE_PLM_REPORT_PORT1 (bit15 -08)							
	LANE2 RECEIVER DISPARITY ERR CNT(03:00)				LANE2 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
63	HMA: ZCORE_PLM_REPORT_PORT1 (bit07 -00)							
	LANE2 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE2 8B/10B DECODER ERR CNT(03:00)			
64	HMA: ZCORE_PLM_REPORT_PORT2 (bit31 -24)							
	LANE5 RECEIVER DISPARITY ERR CNT(03:00)				LANE5 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
65	HMA: ZCORE_PLM_REPORT_PORT2 (bit23 -16)							
	LANE5 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE5 8B/10B DECODER ERR CNT(03:00)			
66	HMA: ZCORE_PLM_REPORT_PORT2 (bit15 -08)							
	LANE4 RECEIVER DISPARITY ERR CNT(03:00)				LANE4 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
67	HMA: ZCORE_PLM_REPORT_PORT2 (bit07 -00)							
	LANE4 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE4 8B/10B DECODER ERR CNT(03:00)			
68	HMA: ZCORE_PLM_REPORT_PORT3 (bit31 -24)							
	LANE7 RECEIVER DISPARITY ERR CNT(03:00)				LANE7 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
69	HMA: ZCORE_PLM_REPORT_PORT3 (bit23 -16)							
	LANE7 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE7 8B/10B DECODER ERR CNT(03:00)			
6A	HMA: ZCORE_PLM_REPORT_PORT3 (bit15 -08)							
	LANE6 RECEIVER DISPARITY ERR CNT(03:00)				LANE6 ELASTIC BUFFER UNDERFLOW CNT(03:00)			
6B	HMA: ZCORE_PLM_REPORT_PORT3 (bit07 -00)							
	LANE6 ELASTIC BUFFER OVERFLOW CNT(03:00)				LANE6 8B/10B DECODER ERR CNT(03:00)			
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(12) Byte28 = 2D/4D ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL0_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL0_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL0_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL0_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL0_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL0_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL0_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL0_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL0_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL0_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL0_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL0_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL0_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL0_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL0_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL0_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL0_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL0_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL0_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL0_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL0_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL0_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL0_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL0_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL0_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL0_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL0_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL0_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL0_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL0_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL0_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL0_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL0_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL0_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL0_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL0_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL0_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL0_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL0_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL0_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL0_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL0_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL0_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL0_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL0_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL0_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL0_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL0_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL0_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL0_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL0_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL0_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL0_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL0_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL0_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL0_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL0_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL0_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL0_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL0_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL0_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL0_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL0_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL0_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL0_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL0_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL0_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL0_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL0_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL0_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL0_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL0_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL0_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL0_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL0_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL0_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL0_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL0_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL0_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL0_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL0_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL0_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL0_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL0_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL0_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL0_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL0_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL0_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL0_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL0_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL0_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL0_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL0_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL0_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL0_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL0_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL0_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL0_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL0_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL0_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL0_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL0_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL0_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL0_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL0_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL0_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL0_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL0_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL0_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL0_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL0_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL0_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL0_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL0_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL0_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL0_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL0_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL0_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL0_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL0_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL0_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL0_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL0_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL0_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL0_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL0_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL0_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL0_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ00_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ00_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ00_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ00_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ01_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ01_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ01_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ01_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ02_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ02_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ02_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ02_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ03_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ03_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ03_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ03_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(13) Byte28 = 30/50 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL1_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL1_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL1_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL1_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL1_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL1_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL1_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL1_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL1_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL1_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL1_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL1_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL1_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL1_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL1_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL1_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL1_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL1_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL1_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL1_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL1_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL1_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL1_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL1_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL1_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL1_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL1_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL1_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL1_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL1_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL1_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL1_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL1_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL1_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL1_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL1_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL1_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL1_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL1_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL1_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL1_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL1_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL1_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL1_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL1_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL1_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL1_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL1_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL1_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL1_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL1_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL1_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL1_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL1_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL1_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL1_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL1_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL1_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL1_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL1_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL1_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL1_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL1_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL1_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL1_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL1_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL1_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL1_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL1_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL1_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL1_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL1_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL1_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL1_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL1_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL1_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL1_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL1_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL1_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL1_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL1_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL1_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL1_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL1_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL1_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL1_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL1_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL1_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL1_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL1_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL1_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL1_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL1_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL1_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL1_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL1_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL1_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL1_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL1_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL1_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL1_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL1_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL1_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL1_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL1_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL1_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL1_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL1_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL1_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL1_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL1_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL1_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL1_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL1_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL1_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL1_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL1_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL1_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL1_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL1_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL1_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL1_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL1_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL1_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL1_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL1_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL1_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL1_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ04_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ04_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ04_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ04_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ05_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ05_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ05_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ05_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ06_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ06_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ06_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ06_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ07_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ07_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ07_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ07_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(14) Byte28 = 31/51 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL2_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL2_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL2_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL2_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL2_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL2_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL2_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL2_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL2_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL2_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL2_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL2_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL2_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL2_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL2_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL2_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL2_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL2_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL2_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL2_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL2_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL2_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL2_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL2_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL2_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL2_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL2_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL2_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL2_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL2_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL2_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL2_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL2_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL2_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL2_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL2_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL2_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL2_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL2_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL2_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL2_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL2_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL2_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL2_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL2_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL2_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL2_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL2_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL2_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL2_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL2_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL2_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL2_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL2_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL2_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL2_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL2_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL2_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL2_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL2_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL2_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL2_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL2_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL2_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL2_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL2_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL2_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL2_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL2_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL2_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL2_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL2_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL2_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL2_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL2_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL2_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL2_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL2_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL2_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL2_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL2_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL2_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL2_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL2_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL2_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL2_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL2_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL2_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL2_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL2_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL2_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL2_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL2_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL2_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL2_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL2_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL2_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL2_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL2_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL2_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL2_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL2_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL2_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL2_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL2_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL2_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL2_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL2_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL2_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL2_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL2_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL2_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL2_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL2_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL2_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL2_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL2_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL2_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL2_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL2_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL2_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL2_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL2_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL2_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL2_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL2_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL2_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL2_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ08_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ08_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ08_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ08_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ09_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ09_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ09_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ09_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ0A_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ0A_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ0A_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ0A_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ0B_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ0B_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ0B_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ0B_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(15) Byte28 = 32/52 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL3_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL3_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL3_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL3_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL3_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL3_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL3_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL3_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL3_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL3_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL3_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL3_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL3_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL3_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL3_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL3_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL3_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL3_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL3_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL3_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL3_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL3_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL3_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL3_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL3_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL3_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL3_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL3_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL3_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL3_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL3_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL3_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL3_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL3_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL3_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL3_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL3_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL3_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL3_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL3_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL3_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL3_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL3_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL3_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL3_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL3_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL3_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL3_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL3_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL3_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL3_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL3_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL3_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL3_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL3_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL3_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL3_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL3_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL3_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL3_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL3_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL3_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL3_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL3_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL3_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL3_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL3_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL3_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL3_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL3_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL3_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL3_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL3_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL3_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL3_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL3_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL3_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL3_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL3_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL3_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL3_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL3_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL3_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL3_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL3_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL3_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL3_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL3_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL3_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL3_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL3_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL3_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL3_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL3_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL3_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL3_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL3_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL3_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL3_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL3_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL3_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL3_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL3_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL3_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL3_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL3_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL3_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL3_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL3_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL3_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL3_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL3_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL3_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL3_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL3_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL3_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL3_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL3_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL3_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL3_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL3_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL3_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL3_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL3_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL3_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL3_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL3_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL3_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ0C_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ0C_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ0C_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ0C_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ0D_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ0D_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ0D_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ0D_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ0E_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ0E_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ0E_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ0E_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ0F_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ0F_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ0F_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ0F_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(16) Byte28 = 33/53 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL4_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL4_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL4_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL4_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL4_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL4_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL4_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL4_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL4_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL4_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL4_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL4_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL4_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL4_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL4_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL4_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL4_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL4_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL4_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL4_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL4_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL4_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL4_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL4_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL4_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL4_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL4_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL4_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL4_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL4_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL4_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL4_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL4_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL4_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL4_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL4_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL4_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL4_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL4_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL4_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL4_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL4_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL4_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL4_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL4_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL4_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL4_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL4_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL4_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL4_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL4_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL4_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL4_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL4_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL4_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL4_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL4_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL4_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL4_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL4_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL4_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL4_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL4_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL4_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL4_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL4_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL4_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL4_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL4_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL4_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL4_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL4_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL4_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL4_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL4_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL4_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL4_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL4_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL4_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL4_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL4_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL4_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL4_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL4_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL4_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL4_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL4_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL4_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL4_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL4_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL4_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL4_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL4_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL4_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL4_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL4_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL4_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL4_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL4_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL4_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL4_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL4_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL4_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL4_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL4_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL4_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL4_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL4_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL4_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL4_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL4_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL4_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL4_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL4_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL4_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL4_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL4_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL4_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL4_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL4_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL4_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL4_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL4_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL4_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL4_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL4_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL4_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL4_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ10_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ10_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ10_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ10_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ11_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ11_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ11_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ11_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ12_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ12_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ12_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ12_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ13_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ13_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ13_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ13_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(17) Byte28 = 34/54 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL5_TABLE00 (bit31 -24)							
	PROTOCOL0 INFO03 (07:00)							
41	HMA: LRP_PROTOCOL5_TABLE00 (bit23 -16)							
	PROTOCOL0 INFO02 (07:00)							
42	HMA: LRP_PROTOCOL5_TABLE00 (bit15 -08)							
	PROTOCOL0 INFO01 (07:00)							
43	HMA: LRP_PROTOCOL5_TABLE00 (bit07 -00)							
	PROTOCOL0 INFO00 (07:00)							
44	HMA: LRP_PROTOCOL5_TABLE04 (bit31 -24)							
	PROTOCOL0 INFO07 (07:00)							
45	HMA: LRP_PROTOCOL5_TABLE04 (bit23 -16)							
	PROTOCOL0 INFO06 (07:00)							
46	HMA: LRP_PROTOCOL5_TABLE04 (bit15 -08)							
	PROTOCOL0 INFO05 (07:00)							
47	HMA: LRP_PROTOCOL5_TABLE04 (bit07 -00)							
	PROTOCOL0 INFO04 (07:00)							
48	HMA: LRP_PROTOCOL5_TABLE08 (bit31 -24)							
	PROTOCOL0 INFO0B (07:00)							
49	HMA: LRP_PROTOCOL5_TABLE08 (bit23 -16)							
	PROTOCOL0 INFO0A (07:00)							
4A	HMA: LRP_PROTOCOL5_TABLE08 (bit15 -08)							
	PROTOCOL0 INFO09 (07:00)							
4B	HMA: LRP_PROTOCOL5_TABLE08 (bit07 -00)							
	PROTOCOL0 INFO08 (07:00)							
4C	HMA: LRP_PROTOCOL5_TABLE0C (bit31 -24)							
	PROTOCOL0 INFO0F (07:00)							
4D	HMA: LRP_PROTOCOL5_TABLE0C (bit23 -16)							
	PROTOCOL0 INFO0E (07:00)							
4E	HMA: LRP_PROTOCOL5_TABLE0C (bit15 -08)							
	PROTOCOL0 INFO0D (07:00)							
4F	HMA: LRP_PROTOCOL5_TABLE0C (bit07 -00)							
	PROTOCOL0 INFO0C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL5_TABLE10 (bit31 -24)							
	PROTOCOL0 INFO13 (07:00)							
51	HMA: LRP_PROTOCOL5_TABLE10 (bit23 -16)							
	PROTOCOL0 INFO12 (07:00)							
52	HMA: LRP_PROTOCOL5_TABLE10 (bit15 -08)							
	PROTOCOL0 INFO11 (07:00)							
53	HMA: LRP_PROTOCOL5_TABLE10 (bit07 -00)							
	PROTOCOL0 INFO10 (07:00)							
54	HMA: LRP_PROTOCOL5_TABLE14 (bit31 -24)							
	PROTOCOL0 INFO17 (07:00)							
55	HMA: LRP_PROTOCOL5_TABLE14 (bit23 -16)							
	PROTOCOL0 INFO16 (07:00)							
56	HMA: LRP_PROTOCOL5_TABLE14 (bit15 -08)							
	PROTOCOL0 INFO15 (07:00)							
57	HMA: LRP_PROTOCOL5_TABLE14 (bit07 -00)							
	PROTOCOL0 INFO14 (07:00)							
58	HMA: LRP_PROTOCOL5_TABLE18 (bit31 -24)							
	PROTOCOL0 INFO1B (07:00)							
59	HMA: LRP_PROTOCOL5_TABLE18 (bit23 -16)							
	PROTOCOL0 INFO1A (07:00)							
5A	HMA: LRP_PROTOCOL5_TABLE18 (bit15 -08)							
	PROTOCOL0 INFO19 (07:00)							
5B	HMA: LRP_PROTOCOL5_TABLE18 (bit07 -00)							
	PROTOCOL0 INFO18 (07:00)							
5C	HMA: LRP_PROTOCOL5_TABLE1C (bit31 -24)							
	PROTOCOL0 INFO1F (07:00)							
5D	HMA: LRP_PROTOCOL5_TABLE1C (bit23 -16)							
	PROTOCOL0 INFO1E (07:00)							
5E	HMA: LRP_PROTOCOL5_TABLE1C (bit15 -08)							
	PROTOCOL0 INFO1D (07:00)							
5F	HMA: LRP_PROTOCOL5_TABLE1C (bit07 -00)							
	PROTOCOL0 INFO1C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL5_TABLE20 (bit31 -24)							
	PROTOCOL0 INFO23 (07:00)							
61	HMA: LRP_PROTOCOL5_TABLE20 (bit23 -16)							
	PROTOCOL0 INFO22 (07:00)							
62	HMA: LRP_PROTOCOL5_TABLE20 (bit15 -08)							
	PROTOCOL0 INFO21 (07:00)							
63	HMA: LRP_PROTOCOL5_TABLE20 (bit07 -00)							
	PROTOCOL0 INFO20 (07:00)							
64	HMA: LRP_PROTOCOL5_TABLE24 (bit31 -24)							
	PROTOCOL0 INFO27 (07:00)							
65	HMA: LRP_PROTOCOL5_TABLE24 (bit23 -16)							
	PROTOCOL0 INFO26 (07:00)							
66	HMA: LRP_PROTOCOL5_TABLE24 (bit15 -08)							
	PROTOCOL0 INFO25 (07:00)							
67	HMA: LRP_PROTOCOL5_TABLE24 (bit07 -00)							
	PROTOCOL0 INFO24 (07:00)							
68	HMA: LRP_PROTOCOL5_TABLE28 (bit31 -24)							
	PROTOCOL0 INFO2B (07:00)							
69	HMA: LRP_PROTOCOL5_TABLE28 (bit23 -16)							
	PROTOCOL0 INFO2A (07:00)							
6A	HMA: LRP_PROTOCOL5_TABLE28 (bit15 -08)							
	PROTOCOL0 INFO29 (07:00)							
6B	HMA: LRP_PROTOCOL5_TABLE28 (bit07 -00)							
	PROTOCOL0 INFO28 (07:00)							
6C	HMA: LRP_PROTOCOL5_TABLE2C (bit31 -24)							
	PROTOCOL0 INFO2F (07:00)							
6D	HMA: LRP_PROTOCOL5_TABLE2C (bit23 -16)							
	PROTOCOL0 INFO2E (07:00)							
6E	HMA: LRP_PROTOCOL5_TABLE2C (bit15 -08)							
	PROTOCOL0 INFO2D (07:00)							
6F	HMA: LRP_PROTOCOL5_TABLE2C (bit07 -00)							
	PROTOCOL0 INFO2C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL5_TABLE30 (bit31 -24)							
	PROTOCOL0 INFO33 (07:00)							
71	HMA: LRP_PROTOCOL5_TABLE30 (bit23 -16)							
	PROTOCOL0 INFO32 (07:00)							
72	HMA: LRP_PROTOCOL5_TABLE30 (bit15 -08)							
	PROTOCOL0 INFO31 (07:00)							
73	HMA: LRP_PROTOCOL5_TABLE30 (bit07 -00)							
	PROTOCOL0 INFO30 (07:00)							
74	HMA: LRP_PROTOCOL5_TABLE34 (bit31 -24)							
	PROTOCOL0 INFO37 (07:00)							
75	HMA: LRP_PROTOCOL5_TABLE34 (bit23 -16)							
	PROTOCOL0 INFO36 (07:00)							
76	HMA: LRP_PROTOCOL5_TABLE34 (bit15 -08)							
	PROTOCOL0 INFO35 (07:00)							
77	HMA: LRP_PROTOCOL5_TABLE34 (bit07 -00)							
	PROTOCOL0 INFO34 (07:00)							
78	HMA: LRP_PROTOCOL5_TABLE38 (bit31 -24)							
	PROTOCOL0 INFO3B (07:00)							
79	HMA: LRP_PROTOCOL5_TABLE38 (bit23 -16)							
	PROTOCOL0 INFO3A (07:00)							
7A	HMA: LRP_PROTOCOL5_TABLE38 (bit15 -08)							
	PROTOCOL0 INFO39 (07:00)							
7B	HMA: LRP_PROTOCOL5_TABLE38 (bit07 -00)							
	PROTOCOL0 INFO38 (07:00)							
7C	HMA: LRP_PROTOCOL5_TABLE3C (bit31 -24)							
	PROTOCOL0 INFO3F (07:00)							
7D	HMA: LRP_PROTOCOL5_TABLE3C (bit23 -16)							
	PROTOCOL0 INFO3E (07:00)							
7E	HMA: LRP_PROTOCOL5_TABLE3C (bit15 -08)							
	PROTOCOL0 INFO3D (07:00)							
7F	HMA: LRP_PROTOCOL5_TABLE3C (bit07 -00)							
	PROTOCOL0 INFO3C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRP_PROTOCOL5_TABLE40 (bit31 -24)							
	PROTOCOL0 INFO43 (07:00)							
41	HMA: LRP_PROTOCOL5_TABLE40 (bit23 -16)							
	PROTOCOL0 INFO42 (07:00)							
42	HMA: LRP_PROTOCOL5_TABLE40 (bit15 -08)							
	PROTOCOL0 INFO41 (07:00)							
43	HMA: LRP_PROTOCOL5_TABLE40 (bit07 -00)							
	PROTOCOL0 INFO40 (07:00)							
44	HMA: LRP_PROTOCOL5_TABLE44 (bit31 -24)							
	PROTOCOL0 INFO47 (07:00)							
45	HMA: LRP_PROTOCOL5_TABLE44 (bit23 -16)							
	PROTOCOL0 INFO46 (07:00)							
46	HMA: LRP_PROTOCOL5_TABLE44 (bit15 -08)							
	PROTOCOL0 INFO45 (07:00)							
47	HMA: LRP_PROTOCOL5_TABLE44 (bit07 -00)							
	PROTOCOL0 INFO44 (07:00)							
48	HMA: LRP_PROTOCOL5_TABLE48 (bit31 -24)							
	PROTOCOL0 INFO4B (07:00)							
49	HMA: LRP_PROTOCOL5_TABLE48 (bit23 -16)							
	PROTOCOL0 INFO4A (07:00)							
4A	HMA: LRP_PROTOCOL5_TABLE48 (bit15 -08)							
	PROTOCOL0 INFO49 (07:00)							
4B	HMA: LRP_PROTOCOL5_TABLE48 (bit07 -00)							
	PROTOCOL0 INFO48 (07:00)							
4C	HMA: LRP_PROTOCOL5_TABLE4C (bit31 -24)							
	PROTOCOL0 INFO4F (07:00)							
4D	HMA: LRP_PROTOCOL5_TABLE4C (bit23 -16)							
	PROTOCOL0 INFO4E (07:00)							
4E	HMA: LRP_PROTOCOL5_TABLE4C (bit15 -08)							
	PROTOCOL0 INFO4D (07:00)							
4F	HMA: LRP_PROTOCOL5_TABLE4C (bit07 -00)							
	PROTOCOL0 INFO4C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_PROTOCOL5_TABLE50 (bit31 -24)							
	PROTOCOL0 INFO53 (07:00)							
51	HMA: LRP_PROTOCOL5_TABLE50 (bit23 -16)							
	PROTOCOL0 INFO52 (07:00)							
52	HMA: LRP_PROTOCOL5_TABLE50 (bit15 -08)							
	PROTOCOL0 INFO51 (07:00)							
53	HMA: LRP_PROTOCOL5_TABLE50 (bit07 -00)							
	PROTOCOL0 INFO50 (07:00)							
54	HMA: LRP_PROTOCOL5_TABLE54 (bit31 -24)							
	PROTOCOL0 INFO57 (07:00)							
55	HMA: LRP_PROTOCOL5_TABLE54 (bit23 -16)							
	PROTOCOL0 INFO56 (07:00)							
56	HMA: LRP_PROTOCOL5_TABLE54 (bit15 -08)							
	PROTOCOL0 INFO55 (07:00)							
57	HMA: LRP_PROTOCOL5_TABLE54 (bit07 -00)							
	PROTOCOL0 INFO54 (07:00)							
58	HMA: LRP_PROTOCOL5_TABLE58 (bit31 -24)							
	PROTOCOL0 INFO5B (07:00)							
59	HMA: LRP_PROTOCOL5_TABLE58 (bit23 -16)							
	PROTOCOL0 INFO5A (07:00)							
5A	HMA: LRP_PROTOCOL5_TABLE58 (bit15 -08)							
	PROTOCOL0 INFO59 (07:00)							
5B	HMA: LRP_PROTOCOL5_TABLE58 (bit07 -00)							
	PROTOCOL0 INFO58 (07:00)							
5C	HMA: LRP_PROTOCOL5_TABLE5C (bit31 -24)							
	PROTOCOL0 INFO5F (07:00)							
5D	HMA: LRP_PROTOCOL5_TABLE5C (bit23 -16)							
	PROTOCOL0 INFO5E (07:00)							
5E	HMA: LRP_PROTOCOL5_TABLE5C (bit15 -08)							
	PROTOCOL0 INFO5D (07:00)							
5F	HMA: LRP_PROTOCOL5_TABLE5C (bit07 -00)							
	PROTOCOL0 INFO5C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRP_PROTOCOL5_TABLE60 (bit31 -24)							
	PROTOCOL0 INFO63 (07:00)							
61	HMA: LRP_PROTOCOL5_TABLE60 (bit23 -16)							
	PROTOCOL0 INFO62 (07:00)							
62	HMA: LRP_PROTOCOL5_TABLE60 (bit15 -08)							
	PROTOCOL0 INFO61 (07:00)							
63	HMA: LRP_PROTOCOL5_TABLE60 (bit07 -00)							
	PROTOCOL0 INFO60 (07:00)							
64	HMA: LRP_PROTOCOL5_TABLE64 (bit31 -24)							
	PROTOCOL0 INFO67 (07:00)							
65	HMA: LRP_PROTOCOL5_TABLE64 (bit23 -16)							
	PROTOCOL0 INFO66 (07:00)							
66	HMA: LRP_PROTOCOL5_TABLE64 (bit15 -08)							
	PROTOCOL0 INFO65 (07:00)							
67	HMA: LRP_PROTOCOL5_TABLE64 (bit07 -00)							
	PROTOCOL0 INFO64 (07:00)							
68	HMA: LRP_PROTOCOL5_TABLE68 (bit31 -24)							
	PROTOCOL0 INFO6B (07:00)							
69	HMA: LRP_PROTOCOL5_TABLE68 (bit23 -16)							
	PROTOCOL0 INFO6A (07:00)							
6A	HMA: LRP_PROTOCOL5_TABLE68 (bit15 -08)							
	PROTOCOL0 INFO69 (07:00)							
6B	HMA: LRP_PROTOCOL5_TABLE68 (bit07 -00)							
	PROTOCOL0 INFO68 (07:00)							
6C	HMA: LRP_PROTOCOL5_TABLE6C (bit31 -24)							
	PROTOCOL0 INFO6F (07:00)							
6D	HMA: LRP_PROTOCOL5_TABLE6C (bit23 -16)							
	PROTOCOL0 INFO6E (07:00)							
6E	HMA: LRP_PROTOCOL5_TABLE6C (bit15 -08)							
	PROTOCOL0 INFO6D (07:00)							
6F	HMA: LRP_PROTOCOL5_TABLE6C (bit07 -00)							
	PROTOCOL0 INFO6C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRP_PROTOCOL5_TABLE70 (bit31 -24)							
	PROTOCOL0 INFO73 (07:00)							
71	HMA: LRP_PROTOCOL5_TABLE70 (bit23 -16)							
	PROTOCOL0 INFO72 (07:00)							
72	HMA: LRP_PROTOCOL5_TABLE70 (bit15 -08)							
	PROTOCOL0 INFO71 (07:00)							
73	HMA: LRP_PROTOCOL5_TABLE70 (bit07 -00)							
	PROTOCOL0 INFO70 (07:00)							
74	HMA: LRP_PROTOCOL5_TABLE74 (bit31 -24)							
	PROTOCOL0 INFO77 (07:00)							
75	HMA: LRP_PROTOCOL5_TABLE74 (bit23 -16)							
	PROTOCOL0 INFO76 (07:00)							
76	HMA: LRP_PROTOCOL5_TABLE74 (bit15 -08)							
	PROTOCOL0 INFO75 (07:00)							
77	HMA: LRP_PROTOCOL5_TABLE74 (bit07 -00)							
	PROTOCOL0 INFO74 (07:00)							
78	HMA: LRP_PROTOCOL5_TABLE78 (bit31 -24)							
	PROTOCOL0 INFO7B (07:00)							
79	HMA: LRP_PROTOCOL5_TABLE78 (bit23 -16)							
	PROTOCOL0 INFO7A (07:00)							
7A	HMA: LRP_PROTOCOL5_TABLE78 (bit15 -08)							
	PROTOCOL0 INFO79 (07:00)							
7B	HMA: LRP_PROTOCOL5_TABLE78 (bit07 -00)							
	PROTOCOL0 INFO78 (07:00)							
7C	HMA: LRP_PROTOCOL5_TABLE7C (bit31 -24)							
	PROTOCOL0 INFO7F (07:00)							
7D	HMA: LRP_PROTOCOL5_TABLE7C (bit23 -16)							
	PROTOCOL0 INFO7E (07:00)							
7E	HMA: LRP_PROTOCOL5_TABLE7C (bit15 -08)							
	PROTOCOL0 INFO7D (07:00)							
7F	HMA: LRP_PROTOCOL5_TABLE7C (bit07 -00)							
	PROTOCOL0 INFO7C (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ③ (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XD_ERQ14_ERR_F0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	HMA: XD_ERQ14_ERR_F0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	HMA: XD_ERQ14_ERR_F0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
53	HMA: XD_ERQ14_ERR_F0 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
54	HMA: XD_ERQ15_ERR_F1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	HMA: XD_ERQ15_ERR_F1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	HMA: XD_ERQ15_ERR_F1 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
57	HMA: XD_ERQ15_ERR_F1 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
58	HMA: XD_ERQ16_ERR_F2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	HMA: XD_ERQ16_ERR_F2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	HMA: XD_ERQ16_ERR_F2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5B	HMA: XD_ERQ16_ERR_F2 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1
5C	HMA: XD_ERQ17_ERR_F3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	HMA: XD_ERQ17_ERR_F3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: XD_ERQ17_ERR_F3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	DP SEQ	ETX SEQ	DNA SEQ	DN2 SEQ
5F	HMA: XD_ERQ17_ERR_F3 (bit07 -00)							
	DN WRN	DN STS	DN REQID	DN CPLID	DN SEQ	DN TO3	DN TO2	DN TO1

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(18) Byte28 = 35/55 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: INT0_INT_STATUS0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: INT0_INT_STATUS0 (bit23 -16)							
	Reserved	Reserved	Reserved	INT INT CHK1B	Reserved	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	HMA: INT0_INT_STATUS0 (bit15 -08)							
	Reserved	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Reserved	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	HMA: INT0_INT_STATUS0 (bit07 -00)							
	Reserved	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Reserved	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	HMA: LRPn_CTL (bit31 -24)							
	START (07:00)							
45	HMA: LRPn_CTL (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_CTL (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_CTL (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: LRPn_STS (bit31 -24)							
	ACT	ERRSTP	Reserved	ERR	WRN	Reserved	DGWAIT	DGPASS
49	HMA: LRPn_STS (bit23 -16)							
	SEQ (07:00)							
4A	HMA: LRPn_STS (bit15 -08)							
	Now ADR (15:08)							
4B	HMA: LRPn_STS (bit07 -00)							
	Now ADR (07:00)							
4C	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit31 -24)							
	JUMPADR_LOG1 (15:08)							
4D	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit23 -16)							
	JUMPADR_LOG1 (07:00)							
4E	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit15 -08)							
	JUMPADR_LOG0 (15:08)							
4F	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit07 -00)							
	JUMPADR_LOG0 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit31 -24)							
	JUMPADR_LOG3 (15:08)							
51	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit23 -16)							
	JUMPADR_LOG3 (07:00)							
52	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit15 -08)							
	JUMPADR_LOG2 (15:08)							
53	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit07 -00)							
	JUMPADR_LOG2 (07:00)							
54	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit31 -24)							
	JUMPADR_LOG5 (15:08)							
55	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit23 -16)							
	JUMPADR_LOG5 (07:00)							
56	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit15 -08)							
	JUMPADR_LOG4 (15:08)							
57	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit07 -00)							
	JUMPADR_LOG4 (07:00)							
58	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit31 -24)							
	JUMPADR_LOG7 (15:08)							
59	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit23 -16)							
	JUMPADR_LOG7 (07:00)							
5A	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit15 -08)							
	JUMPADR_LOG6 (15:08)							
5B	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit07 -00)							
	JUMPADR_LOG6 (07:00)							
5C	HMA: LRPn_ERR0 (bit31 -24)							
	ALUCMP ERR	SEQE ERR	TIMOUT	0JUMP	TIMER PERR	X2PERR	X1PERR	X0PERR
5D	HMA: LRPn_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: LRPn_ERR0 (bit15 -08)							
	Reserved	Reserved	CSAD ECC	CSUC ECC	CSODTP	CSOADP	CSIDTP	CSIADP
5F	HMA: LRPn_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR1 (bit31 -24)							
	DSO_LRP	DSO_DMA	DSO_XR	DSO_PPCI	Reserved	DSI_LRP	DSI_XR	DSI_PPCI
61	HMA: LRPn_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR1 (bit15 -08)							
	DS OAW3	DS OAW2	DS OAW1	DS OAW0	DS OUNCW3	DS OUNCW2	DS OUNCW1	DS OUNCW0
63	HMA: LRPn_ERR1 (bit07 -00)							
	DSOADP	DSODTP	Reserved	DSIADP	DSIDTPW3	DSIDTPW2	DSIDTPW1	DSIDTPW0
64	HMA: LRPn_PCIRX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	MEMDRP	ECCCRE	ECCADR
65	HMA: LRPn_PCIRX_ERR (bit23 -16)							
	Reserved	Reserved	RAMOP	RAMINP	TXADRP	SEQENC	SEQDEC	RDTO
66	HMA: LRPn_PCIRX_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
67	HMA: LRPn_PCIRX_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
68	HMA: LRPn_FPCI_RX_MODE (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	ECCINH	SEQRES	SEQERR
69	HMA: LRPn_FPCI_RX_MODE (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	SWBSYOF	SWFRST	SWSTOP	SWERST
6A	HMA: LRPn_FPCI_RX_MODE (bit15 -08)							
	SWRX_TIMER VAL (15:08)							
6B	HMA: LRPn_FPCI_RX_MODE (bit07 -00)							
	SWRX_TIMER VAL (07:00)							
6C	HMA: LRPn_PCITX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRPn_PCITX_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: LRPn_PCITX_ERR (bit15 -08)							
	Reserved	LENP	H8P	H423P	PENDP	ECNTP	DTP	ADRP
6F	HMA: LRPn_PCITX_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	SEQ	TIMOUT	STS	CPTY	OVRUN

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRPn_FPCI_TX_SEQ (bit31 -24)							
	RX SW SEQ STS (07:00)							
71	HMA: LRPn_FPCI_TX_SEQ (bit23 -16)							
	RX SEQ STS (07:00)							
72	HMA: LRPn_FPCI_TX_SEQ (bit15 -08)							
	TX SW SEQ STS (07:00)							
73	HMA: LRPn_FPCI_TX_SEQ (bit07 -00)							
	TX SEQ STS (07:00)							
74	HMA: LRPn_FCTL_ERR (bit31 -24)							
	CSLRC	CSLCNT1	CSLCNT2	CSLSEQ	CSLTOP	CSLTOUT	CSLXCTP	CSLBKP
75	HMA: LRPn_FCTL_ERR (bit23 -16)							
	CSLADRP	CSLDTP	DXBASP	LRPADP	DXERR	Reserved	Reserved	Reserved
76	HMA: LRPn_FCTL_ERR (bit15 -08)							
	XRDXDP	XRDXAP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: LRPn_FCTL_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	HMA: LRPn_FCTL_CSLD_BANK (bit31 -24)							
	EN	Reserved	Reserved	LINE3 BANK (04:00)				
79	HMA: LRPn_FCTL_CSLD_BANK (bit23 -16)							
	EN	Reserved	Reserved	LINE2 BANK (04:00)				
7A	HMA: LRPn_FCTL_CSLD_BANK (bit15 -08)							
	EN	Reserved	Reserved	LINE1 BANK (04:00)				
7B	HMA: LRPn_FCTL_CSLD_BANK (bit07 -00)							
	EN	Reserved	Reserved	LINE0 BANK (04:00)				
7C	HMA: LRPn_FCTL_CSLD_SEQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	HMA: LRPn_FCTL_CSLD_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	HMA: LRPn_FCTL_CSLD_SEQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	HMA: LRPn_FCTL_CSLD_SEQ (bit07 -00)							
	SEQ STS (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRPn_FIF_DXLRP_ERR (bit31 -24)							
	RDCPL	DTOP	DTIP	SEQ	BEERR	ADRERR	TIM2	TIM3
41	HMA: LRPn_FIF_DXLRP_ERR (bit23 -16)							
	TXHLRC	TXDT	TXTO	TXTOTO	TXWCNT	TXENC	TXDEC	TXDLRC
42	HMA: LRPn_FIF_DXLRP_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
43	HMA: LRPn_FIF_DXLRP_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
44	HMA: LRPn_FIF_XRPCI_ERR (bit31 -24)							
	ADRP	DTOP	DTIP	SEQ	BEP	TIMOV	STS	Reserved
45	HMA: LRPn_FIF_XRPCI_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_FIF_XRPCI_ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_FIF_XRPCI_ERR (bit07 -00)							
	ADRP	WDTP	WBEP	RDTP	WSEL	RSEL	CMP	SEQ
48	HMA: LRPn_FIF_SEQ (bit31 -24)							
	XR SEQ STS (07:00)							
49	HMA: LRPn_FIF_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: LRPn_FIF_SEQ (bit15 -08)							
	DXBF SEQ STS (07:00)							
4B	HMA: LRPn_FIF_SEQ (bit07 -00)							
	FIFLRP SEQ STS (07:00)							
4C	HMA: LRP_FIF_STS (bit31 -24)							
	XR ERR STS (15:08)							
4D	HMA: LRP_FIF_STS (bit23 -16)							
	XR ERR STS (07:00)							
4E	HMA: LRP_FIF_STS (bit15 -08)							
	DX SWTX SEQ (07:00)							
4F	HMA: LRP_FIF_STS (bit07 -00)							
	DX SWRX SEQ (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_FIF_DXBF_ADRLOG (bit31 -24)							
	DXBF_ADRLOG (31:24)							
51	HMA: LRP_FIF_DXBF_ADRLOG (bit23 -16)							
	DXBF_ADRLOG (23:16)							
52	HMA: LRP_FIF_DXBF_ADRLOG (bit15 -08)							
	DXBF_ADRLOG (15:08)							
53	HMA: LRP_FIF_DXBF_ADRLOG (bit07 -00)							
	DXBF_ADRLOG (07:00)							
54	HMA: LRPn_FIF_XR_ADRLOG (bit31 -24)							
	XR_ADRLOG (bit31 -24)							
55	HMA: LRPn_FIF_XR_ADRLOG (bit23 -16)							
	XR_ADRLOG (bit23 -16)							
56	HMA: LRPn_FIF_XR_ADRLOG (bit15 -08)							
	XR_ADRLOG (bit15 -08)							
57	HMA: LRPn_FIF_XR_ADRLOG (bit07 -00)							
	XR_ADRLOG (bit07 -00)							
58	HMA: LRPn_FIF_PCI_HD4_LOG (bit31 -24)							
	FMT	FMT	FMT	TYP	TYP	TYP	TYP	TYP
59	HMA: LRPn_FIF_PCI_HD4_LOG (bit23 -16)							
	Reserved	TC	TC	TC	Reserved	ATTR	Reserved	TH
5A	HMA: LRPn_FIF_PCI_HD4_LOG (bit15 -08)							
	TD	EP	ATTR	ATTR	AT	AT	LEN	LEN
5B	HMA: LRPn_FIF_PCI_HD4_LOG (bit07 -00)							
	LEN	LEN	LEN	LEN	LEN	LEN	LEN	LEN
5C	HMA: LRPn_FIF_PCI_HD8_LOG (bit31 -24)							
	CMPBUS# (07:00)							
5D	HMA: LRPn_FIF_PCI_HD8_LOG (bit23 -16)							
	CMPSOURCE DEV# (07:00)							
5E	HMA: LRPn_FIF_PCI_HD8_LOG (bit15 -08)							
	ST	ST	ST	BMC	BCNT	BCNT	BCNT	BCNT
5F	HMA: LRPn_FIF_PCI_HD8_LOG (bit07 -00)							
	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR_STS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: LRPn_ERR_STS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR_STS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	HMA: LRPn_ERR_STS (bit07 -00)							
	FIFXRPCI	FIFDXLRP	FCTL	FPCITX	FPCIRX	Reserved	ERR1	ERR0
64	HMA: LRP4 DS HMA INFO 0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: LRP4 DS HMA INFO 0 (bit23 -16)							
	Reserved	Reserved	Ppath5 STS	Ppath4 STS	Ppath3 STS	Ppath2 STS	Ppath1 STS	Ppath0 STS
66	HMA: LRP4 DS HMA INFO 0 (bit15 -08)							
	CM13 STS	CM03 STS	CM12 STS	CM02 STS	CM11 STS	CM01 STS	CM10 STS	CM00 STS
67	HMA: LRP4 DS HMA INFO 0 (bit07 -00)							
	Epath1 STS	Epath0 STS	Ipath1 STS	Ipath0 STS	Reserved	Reserved	Reserved	HMA STS
68	HMA: LRP4 DS HMA INFO 1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	HMA: LRP4 DS HMA INFO 1 (bit23 -16)							
	Reserved	Reserved	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
6A	HMA: LRP4 DS HMA INFO 1 (bit15 -08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
6B	HMA: LRP4 DS HMA INFO 1 (bit07 -00)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	Reserved	Reserved	Reserved	HMA EN
6C	HMA: LRP4 DS HMA INFO 23 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRP4 DS HMA INFO 23 (bit23 -16)							
	Reserved	Reserved	Ppath5 INT	Ppath4 INT	Ppath3 INT	Ppath2 INT	Ppath1 INT	Ppath0 INT
6E	HMA: LRP4 DS HMA INFO 23 (bit15 -08)							
	CM13 INT	CM03 INT	CM12 INT	CM02 INT	CM11 INT	CM01 INT	CM10 INT	CM00 INT
6F	HMA: LRP4 DS HMA INFO 23 (bit07 -00)							
	Epath1 INT	Epath0 INT	Ipath1 INT	Ipath0 INT	Reserved	Reserved	Reserved	HMA INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: INT1_MAILBOX_INT_STATUS0 (bit31 -24)							
	MBOX INT MP31	MBOX INT MP30	MBOX INT MP29	MBOX INT MP28	MBOX INT MP27	MBOX INT MP26	MBOX INT MP25	MBOX INT MP24
71	HMA: INT1_MAILBOX_INT_STATUS0 (bit23 -16)							
	MBOX INT MP23	MBOX INT MP22	MBOX INT MP21	MBOX INT MP20	MBOX INT MP19	MBOX INT MP18	MBOX INT MP17	MBOX INT MP16
72	HMA: INT1_MAILBOX_INT_STATUS0 (bit15 -08)							
	MBOX INT MP15	MBOX INT MP14	MBOX INT MP13	MBOX INT MP12	MBOX INT MP11	MBOX INT MP10	MBOX INT MP09	MBOX INT MP08
73	HMA: INT1_MAILBOX_INT_STATUS0 (bit07 -00)							
	MBOX INT MP07	MBOX INT MP06	MBOX INT MP05	MBOX INT MP04	MBOX INT MP03	MBOX INT MP02	MBOX INT MP01	MBOX INT MP00
74	HMA: INT1_MAILBOX_ABT_STATUS0 (bit31 -24)							
	MBOX ABT MP31	MBOX ABT MP30	MBOX ABT MP29	MBOX ABT MP28	MBOX ABT MP27	MBOX ABT MP26	MBOX ABT MP25	MBOX ABT MP24
75	HMA: INT1_MAILBOX_ABT_STATUS0 (bit23 -16)							
	MBOX ABT MP23	MBOX ABT MP22	MBOX ABT MP21	MBOX ABT MP20	MBOX ABT MP19	MBOX ABT MP18	MBOX ABT MP17	MBOX ABT MP16
76	HMA: INT1_MAILBOX_ABT_STATUS0 (bit15 -08)							
	MBOX ABT MP15	MBOX ABT MP14	MBOX ABT MP13	MBOX ABT MP12	MBOX ABT MP11	MBOX ABT MP10	MBOX ABT MP09	MBOX ABT MP08
77	HMA: INT1_MAILBOX_ABT_STATUS0 (bit07 -00)							
	MBOX ABT MP07	MBOX ABT MP06	MBOX ABT MP05	MBOX ABT MP04	MBOX ABT MP03	MBOX ABT MP02	MBOX ABT MP01	MBOX ABT MP00
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ③ (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(19) Byte28 = 36/56 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: INT0_INT_STATUS0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: INT0_INT_STATUS0 (bit23 -16)							
	Reserved	Reserved	Reserved	INT INT CHK1B	Reserved	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	HMA: INT0_INT_STATUS0 (bit15 -08)							
	Reserved	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Reserved	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	HMA: INT0_INT_STATUS0 (bit07 -00)							
	Reserved	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Reserved	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	HMA: LRPn_CTL (bit31 -24)							
	START (07:00)							
45	HMA: LRPn_CTL (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_CTL (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_CTL (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: LRPn_STS (bit31 -24)							
	ACT	ERRSTP	Reserved	ERR	WRN	Reserved	DGWAIT	DGPASS
49	HMA: LRPn_STS (bit23 -16)							
	SEQ (07:00)							
4A	HMA: LRPn_STS (bit15 -08)							
	Now ADR (15:08)							
4B	HMA: LRPn_STS (bit07 -00)							
	Now ADR (07:00)							
4C	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit31 -24)							
	JUMPADR_LOG1 (15:08)							
4D	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit23 -16)							
	JUMPADR_LOG1 (07:00)							
4E	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit15 -08)							
	JUMPADR_LOG0 (15:08)							
4F	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit07 -00)							
	JUMPADR_LOG0 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit31 -24)							
	JUMPADR_LOG3 (15:08)							
51	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit23 -16)							
	JUMPADR_LOG3 (07:00)							
52	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit15 -08)							
	JUMPADR_LOG2 (15:08)							
53	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit07 -00)							
	JUMPADR_LOG2 (07:00)							
54	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit31 -24)							
	JUMPADR_LOG5 (15:08)							
55	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit23 -16)							
	JUMPADR_LOG5 (07:00)							
56	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit15 -08)							
	JUMPADR_LOG4 (15:08)							
57	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit07 -00)							
	JUMPADR_LOG4 (07:00)							
58	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit31 -24)							
	JUMPADR_LOG7 (15:08)							
59	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit23 -16)							
	JUMPADR_LOG7 (07:00)							
5A	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit15 -08)							
	JUMPADR_LOG6 (15:08)							
5B	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit07 -00)							
	JUMPADR_LOG6 (07:00)							
5C	HMA: LRPn_ERR0 (bit31 -24)							
	ALUCMP ERR	SEQE ERR	TIMOUT	0JUMP	TIMER PERR	X2PERR	X1PERR	X0PERR
5D	HMA: LRPn_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: LRPn_ERR0 (bit15 -08)							
	Reserved	Reserved	CSAD ECC	CSUC ECC	CSODTP	CSOADP	CSIDTP	CSIADP
5F	HMA: LRPn_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR1 (bit31 -24)							
	DSO_LRP	DSO_DMA	DSO_XR	DSO_PPCI	Reserved	DSI_LRP	DSI_XR	DSI_PPCI
61	HMA: LRPn_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR1 (bit15 -08)							
	DS OAW3	DS OAW2	DS OAW1	DS OAW0	DS OUNCW3	DS OUNCW2	DS OUNCW1	DS OUNCW0
63	HMA: LRPn_ERR1 (bit07 -00)							
	DSOADP	DSODTP	Reserved	DSIADP	DSIDTPW3	DSIDTPW2	DSIDTPW1	DSIDTPW0
64	HMA: LRPn_PCIRX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	MEMDRP	ECCCRE	ECCADR
65	HMA: LRPn_PCIRX_ERR (bit23 -16)							
	Reserved	Reserved	RAMOP	RAMINP	TXADRP	SEQENC	SEQDEC	RDTO
66	HMA: LRPn_PCIRX_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
67	HMA: LRPn_PCIRX_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
68	HMA: LRPn_FPCI_RX_MODE (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	ECCINH	SEQRES	SEQERR
69	HMA: LRPn_FPCI_RX_MODE (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	SWBSYOF	SWFRST	SWSTOP	SWERST
6A	HMA: LRPn_FPCI_RX_MODE (bit15 -08)							
	SWRX_TIMER VAL (15:08)							
6B	HMA: LRPn_FPCI_RX_MODE (bit07 -00)							
	SWRX_TIMER VAL (07:00)							
6C	HMA: LRPn_PCITX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRPn_PCITX_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: LRPn_PCITX_ERR (bit15 -08)							
	Reserved	LENP	H8P	H423P	PENDP	ECNTP	DTP	ADRP
6F	HMA: LRPn_PCITX_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	SEQ	TIMOUT	STS	CPTY	OVRUN

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRPn_FPCI_TX_SEQ (bit31 -24)							
	RX SW SEQ STS (07:00)							
71	HMA: LRPn_FPCI_TX_SEQ (bit23 -16)							
	RX SEQ STS (07:00)							
72	HMA: LRPn_FPCI_TX_SEQ (bit15 -08)							
	TX SW SEQ STS (07:00)							
73	HMA: LRPn_FPCI_TX_SEQ (bit07 -00)							
	TX SEQ STS (07:00)							
74	HMA: LRPn_FCTL_ERR (bit31 -24)							
	CSLRC	CSLCNT1	CSLCNT2	CSLSEQ	CSLTOP	CSLTOUT	CSLXCTP	CSLBKP
75	HMA: LRPn_FCTL_ERR (bit23 -16)							
	CSLADRP	CSLDTP	DXBASP	LRPADP	DXERR	Reserved	Reserved	Reserved
76	HMA: LRPn_FCTL_ERR (bit15 -08)							
	XRDXDP	XRDXAP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: LRPn_FCTL_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	HMA: LRPn_FCTL_CSLD_BANK (bit31 -24)							
	EN	Reserved	Reserved	LINE3 BANK (04:00)				
79	HMA: LRPn_FCTL_CSLD_BANK (bit23 -16)							
	EN	Reserved	Reserved	LINE2 BANK (04:00)				
7A	HMA: LRPn_FCTL_CSLD_BANK (bit15 -08)							
	EN	Reserved	Reserved	LINE1 BANK (04:00)				
7B	HMA: LRPn_FCTL_CSLD_BANK (bit07 -00)							
	EN	Reserved	Reserved	LINE0 BANK (04:00)				
7C	HMA: LRPn_FCTL_CSLD_SEQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	HMA: LRPn_FCTL_CSLD_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	HMA: LRPn_FCTL_CSLD_SEQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	HMA: LRPn_FCTL_CSLD_SEQ (bit07 -00)							
	SEQ STS (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRPn_FIF_DXLRP_ERR (bit31 -24)							
	RDCPL	DTOP	DTIP	SEQ	BEERR	ADRERR	TIM2	TIM3
41	HMA: LRPn_FIF_DXLRP_ERR (bit23 -16)							
	TXHLRC	TXDT	TXTO	TXTOTO	TXWCNT	TXENC	TXDEC	TXDLRC
42	HMA: LRPn_FIF_DXLRP_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
43	HMA: LRPn_FIF_DXLRP_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
44	HMA: LRPn_FIF_XRPCI_ERR (bit31 -24)							
	ADRP	DTOP	DTIP	SEQ	BEP	TIMOV	STS	Reserved
45	HMA: LRPn_FIF_XRPCI_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_FIF_XRPCI_ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_FIF_XRPCI_ERR (bit07 -00)							
	ADRP	WDTP	WBEP	RDTP	WSEL	RSEL	CMP	SEQ
48	HMA: LRPn_FIF_SEQ (bit31 -24)							
	XR SEQ STS (07:00)							
49	HMA: LRPn_FIF_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: LRPn_FIF_SEQ (bit15 -08)							
	DXBF SEQ STS (07:00)							
4B	HMA: LRPn_FIF_SEQ (bit07 -00)							
	FIFLRP SEQ STS (07:00)							
4C	HMA: LRP_FIF_STS (bit31 -24)							
	XR ERR STS (15:08)							
4D	HMA: LRP_FIF_STS (bit23 -16)							
	XR ERR STS (07:00)							
4E	HMA: LRP_FIF_STS (bit15 -08)							
	DX SWTX SEQ (07:00)							
4F	HMA: LRP_FIF_STS (bit07 -00)							
	DX SWRX SEQ (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_FIF_DXBF_ADRLOG (bit31 -24)							
	DXBF_ADRLOG (31:24)							
51	HMA: LRP_FIF_DXBF_ADRLOG (bit23 -16)							
	DXBF_ADRLOG (23:16)							
52	HMA: LRP_FIF_DXBF_ADRLOG (bit15 -08)							
	DXBF_ADRLOG (15:08)							
53	HMA: LRP_FIF_DXBF_ADRLOG (bit07 -00)							
	DXBF_ADRLOG (07:00)							
54	HMA: LRPn_FIF_XR_ADRLOG (bit31 -24)							
	XR_ADRLOG (bit31 -24)							
55	HMA: LRPn_FIF_XR_ADRLOG (bit23 -16)							
	XR_ADRLOG (bit23 -16)							
56	HMA: LRPn_FIF_XR_ADRLOG (bit15 -08)							
	XR_ADRLOG (bit15 -08)							
57	HMA: LRPn_FIF_XR_ADRLOG (bit07 -00)							
	XR_ADRLOG (bit07 -00)							
58	HMA: LRPn_FIF_PCI_HD4_LOG (bit31 -24)							
	FMT	FMT	FMT	TYP	TYP	TYP	TYP	TYP
59	HMA: LRPn_FIF_PCI_HD4_LOG (bit23 -16)							
	Reserved	TC	TC	TC	Reserved	ATTR	Reserved	TH
5A	HMA: LRPn_FIF_PCI_HD4_LOG (bit15 -08)							
	TD	EP	ATTR	ATTR	AT	AT	LEN	LEN
5B	HMA: LRPn_FIF_PCI_HD4_LOG (bit07 -00)							
	LEN	LEN	LEN	LEN	LEN	LEN	LEN	LEN
5C	HMA: LRPn_FIF_PCI_HD8_LOG (bit31 -24)							
	CMPBUS# (07:00)							
5D	HMA: LRPn_FIF_PCI_HD8_LOG (bit23 -16)							
	CMPSOURCE DEV# (07:00)							
5E	HMA: LRPn_FIF_PCI_HD8_LOG (bit15 -08)							
	ST	ST	ST	BMC	BCNT	BCNT	BCNT	BCNT
5F	HMA: LRPn_FIF_PCI_HD8_LOG (bit07 -00)							
	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR_STS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: LRPn_ERR_STS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR_STS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	HMA: LRPn_ERR_STS (bit07 -00)							
	FIFXRPCI	FIFDXLRP	FCTL	FPCITX	FPCIRX	Reserved	ERR1	ERR0
64	HMA: LRP4 DS HMA INFO 0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: LRP4 DS HMA INFO 0 (bit23 -16)							
	Reserved	Reserved	Ppath5 STS	Ppath4 STS	Ppath3 STS	Ppath2 STS	Ppath1 STS	Ppath0 STS
66	HMA: LRP4 DS HMA INFO 0 (bit15 -08)							
	CM13 STS	CM03 STS	CM12 STS	CM02 STS	CM11 STS	CM01 STS	CM10 STS	CM00 STS
67	HMA: LRP4 DS HMA INFO 0 (bit07 -00)							
	Epath1 STS	Epath0 STS	Ipath1 STS	Ipath0 STS	Reserved	Reserved	Reserved	HMA STS
68	HMA: LRP4 DS HMA INFO 1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	HMA: LRP4 DS HMA INFO 1 (bit23 -16)							
	Reserved	Reserved	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
6A	HMA: LRP4 DS HMA INFO 1 (bit15 -08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
6B	HMA: LRP4 DS HMA INFO 1 (bit07 -00)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	Reserved	Reserved	Reserved	HMA EN
6C	HMA: LRP4 DS HMA INFO 23 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRP4 DS HMA INFO 23 (bit23 -16)							
	Reserved	Reserved	Ppath5 INT	Ppath4 INT	Ppath3 INT	Ppath2 INT	Ppath1 INT	Ppath0 INT
6E	HMA: LRP4 DS HMA INFO 23 (bit15 -08)							
	CM13 INT	CM03 INT	CM12 INT	CM02 INT	CM11 INT	CM01 INT	CM10 INT	CM00 INT
6F	HMA: LRP4 DS HMA INFO 23 (bit07 -00)							
	Epath1 INT	Epath0 INT	Ipath1 INT	Ipath0 INT	Reserved	Reserved	Reserved	HMA INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: INT1_MAILBOX_INT_STATUS0 (bit31 -24)							
	MBOX INT MP31	MBOX INT MP30	MBOX INT MP29	MBOX INT MP28	MBOX INT MP27	MBOX INT MP26	MBOX INT MP25	MBOX INT MP24
71	HMA: INT1_MAILBOX_INT_STATUS0 (bit23 -16)							
	MBOX INT MP23	MBOX INT MP22	MBOX INT MP21	MBOX INT MP20	MBOX INT MP19	MBOX INT MP18	MBOX INT MP17	MBOX INT MP16
72	HMA: INT1_MAILBOX_INT_STATUS0 (bit15 -08)							
	MBOX INT MP15	MBOX INT MP14	MBOX INT MP13	MBOX INT MP12	MBOX INT MP11	MBOX INT MP10	MBOX INT MP09	MBOX INT MP08
73	HMA: INT1_MAILBOX_INT_STATUS0 (bit07 -00)							
	MBOX INT MP07	MBOX INT MP06	MBOX INT MP05	MBOX INT MP04	MBOX INT MP03	MBOX INT MP02	MBOX INT MP01	MBOX INT MP00
74	HMA: INT1_MAILBOX_ABT_STATUS0 (bit31 -24)							
	MBOX ABT MP31	MBOX ABT MP30	MBOX ABT MP29	MBOX ABT MP28	MBOX ABT MP27	MBOX ABT MP26	MBOX ABT MP25	MBOX ABT MP24
75	HMA: INT1_MAILBOX_ABT_STATUS0 (bit23 -16)							
	MBOX ABT MP23	MBOX ABT MP22	MBOX ABT MP21	MBOX ABT MP20	MBOX ABT MP19	MBOX ABT MP18	MBOX ABT MP17	MBOX ABT MP16
76	HMA: INT1_MAILBOX_ABT_STATUS0 (bit15 -08)							
	MBOX ABT MP15	MBOX ABT MP14	MBOX ABT MP13	MBOX ABT MP12	MBOX ABT MP11	MBOX ABT MP10	MBOX ABT MP09	MBOX ABT MP08
77	HMA: INT1_MAILBOX_ABT_STATUS0 (bit07 -00)							
	MBOX ABT MP07	MBOX ABT MP06	MBOX ABT MP05	MBOX ABT MP04	MBOX ABT MP03	MBOX ABT MP02	MBOX ABT MP01	MBOX ABT MP00
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ③ (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(20) Byte28 = 37/57 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: INT0_INT_STATUS0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: INT0_INT_STATUS0 (bit23 -16)							
	Reserved	Reserved	Reserved	INT INT CHK1B	Reserved	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	HMA: INT0_INT_STATUS0 (bit15 -08)							
	Reserved	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Reserved	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	HMA: INT0_INT_STATUS0 (bit07 -00)							
	Reserved	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Reserved	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	HMA: LRPn_CTL (bit31 -24)							
	START (07:00)							
45	HMA: LRPn_CTL (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_CTL (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_CTL (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: LRPn_STS (bit31 -24)							
	ACT	ERRSTP	Reserved	ERR	WRN	Reserved	DGWAIT	DGPASS
49	HMA: LRPn_STS (bit23 -16)							
	SEQ (07:00)							
4A	HMA: LRPn_STS (bit15 -08)							
	Now ADR (15:08)							
4B	HMA: LRPn_STS (bit07 -00)							
	Now ADR (07:00)							
4C	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit31 -24)							
	JUMPADR_LOG1 (15:08)							
4D	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit23 -16)							
	JUMPADR_LOG1 (07:00)							
4E	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit15 -08)							
	JUMPADR_LOG0 (15:08)							
4F	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit07 -00)							
	JUMPADR_LOG0 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit31 -24)							
	JUMPADR_LOG3 (15:08)							
51	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit23 -16)							
	JUMPADR_LOG3 (07:00)							
52	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit15 -08)							
	JUMPADR_LOG2 (15:08)							
53	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit07 -00)							
	JUMPADR_LOG2 (07:00)							
54	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit31 -24)							
	JUMPADR_LOG5 (15:08)							
55	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit23 -16)							
	JUMPADR_LOG5 (07:00)							
56	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit15 -08)							
	JUMPADR_LOG4 (15:08)							
57	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit07 -00)							
	JUMPADR_LOG4 (07:00)							
58	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit31 -24)							
	JUMPADR_LOG7 (15:08)							
59	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit23 -16)							
	JUMPADR_LOG7 (07:00)							
5A	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit15 -08)							
	JUMPADR_LOG6 (15:08)							
5B	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit07 -00)							
	JUMPADR_LOG6 (07:00)							
5C	HMA: LRPn_ERR0 (bit31 -24)							
	ALUCMP ERR	SEQE ERR	TIMOUT	0JUMP	TIMER PERR	X2PERR	X1PERR	X0PERR
5D	HMA: LRPn_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: LRPn_ERR0 (bit15 -08)							
	Reserved	Reserved	CSAD ECC	CSUC ECC	CSODTP	CSOADP	CSIDTP	CSIADP
5F	HMA: LRPn_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR1 (bit31 -24)							
	DSO_LRP	DSO_DMA	DSO_XR	DSO_PPCI	Reserved	DSI_LRP	DSI_XR	DSI_PPCI
61	HMA: LRPn_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR1 (bit15 -08)							
	DS OAW3	DS OAW2	DS OAW1	DS OAW0	DS OUNCW3	DS OUNCW2	DS OUNCW1	DS OUNCW0
63	HMA: LRPn_ERR1 (bit07 -00)							
	DSOADP	DSODTP	Reserved	DSIADP	DSIDTPW3	DSIDTPW2	DSIDTPW1	DSIDTPW0
64	HMA: LRPn_PCIRX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	MEMDRP	ECCCRE	ECCADR
65	HMA: LRPn_PCIRX_ERR (bit23 -16)							
	Reserved	Reserved	RAMOP	RAMINP	TXADRP	SEQENC	SEQDEC	RDTO
66	HMA: LRPn_PCIRX_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
67	HMA: LRPn_PCIRX_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
68	HMA: LRPn_FPCI_RX_MODE (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	ECCINH	SEQRES	SEQERR
69	HMA: LRPn_FPCI_RX_MODE (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	SWBSYOF	SWFRST	SWSTOP	SWERST
6A	HMA: LRPn_FPCI_RX_MODE (bit15 -08)							
	SWRX_TIMER VAL (15:08)							
6B	HMA: LRPn_FPCI_RX_MODE (bit07 -00)							
	SWRX_TIMER VAL (07:00)							
6C	HMA: LRPn_PCITX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRPn_PCITX_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: LRPn_PCITX_ERR (bit15 -08)							
	Reserved	LENP	H8P	H423P	PENDP	ECNTP	DTP	ADRP
6F	HMA: LRPn_PCITX_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	SEQ	TIMOUT	STS	CPTY	OVRUN

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRPn_FPCI_TX_SEQ (bit31 -24)							
	RX SW SEQ STS (07:00)							
71	HMA: LRPn_FPCI_TX_SEQ (bit23 -16)							
	RX SEQ STS (07:00)							
72	HMA: LRPn_FPCI_TX_SEQ (bit15 -08)							
	TX SW SEQ STS (07:00)							
73	HMA: LRPn_FPCI_TX_SEQ (bit07 -00)							
	TX SEQ STS (07:00)							
74	HMA: LRPn_FCTL_ERR (bit31 -24)							
	CSLRC	CSLCNT1	CSLCNT2	CSLSEQ	CSLTOP	CSLTOUT	CSLXCTP	CSLBKP
75	HMA: LRPn_FCTL_ERR (bit23 -16)							
	CSLADRP	CSLDTP	DXBASP	LRPADP	DXERR	Reserved	Reserved	Reserved
76	HMA: LRPn_FCTL_ERR (bit15 -08)							
	XRDXDP	XRDXAP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: LRPn_FCTL_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	HMA: LRPn_FCTL_CSLD_BANK (bit31 -24)							
	EN	Reserved	Reserved	LINE3 BANK (04:00)				
79	HMA: LRPn_FCTL_CSLD_BANK (bit23 -16)							
	EN	Reserved	Reserved	LINE2 BANK (04:00)				
7A	HMA: LRPn_FCTL_CSLD_BANK (bit15 -08)							
	EN	Reserved	Reserved	LINE1 BANK (04:00)				
7B	HMA: LRPn_FCTL_CSLD_BANK (bit07 -00)							
	EN	Reserved	Reserved	LINE0 BANK (04:00)				
7C	HMA: LRPn_FCTL_CSLD_SEQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	HMA: LRPn_FCTL_CSLD_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	HMA: LRPn_FCTL_CSLD_SEQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	HMA: LRPn_FCTL_CSLD_SEQ (bit07 -00)							
	SEQ STS (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRPn_FIF_DXLRP_ERR (bit31 -24)							
	RDCPL	DTOP	DTIP	SEQ	BEERR	ADRERR	TIM2	TIM3
41	HMA: LRPn_FIF_DXLRP_ERR (bit23 -16)							
	TXHLRC	TXDT	TXTO	TXTOTO	TXWCNT	TXENC	TXDEC	TXDLRC
42	HMA: LRPn_FIF_DXLRP_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
43	HMA: LRPn_FIF_DXLRP_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
44	HMA: LRPn_FIF_XRPCI_ERR (bit31 -24)							
	ADRP	DTOP	DTIP	SEQ	BEP	TIMOV	STS	Reserved
45	HMA: LRPn_FIF_XRPCI_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_FIF_XRPCI_ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_FIF_XRPCI_ERR (bit07 -00)							
	ADRP	WDTP	WBEP	RDTP	WSEL	RSEL	CMP	SEQ
48	HMA: LRPn_FIF_SEQ (bit31 -24)							
	XR SEQ STS (07:00)							
49	HMA: LRPn_FIF_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: LRPn_FIF_SEQ (bit15 -08)							
	DXBF SEQ STS (07:00)							
4B	HMA: LRPn_FIF_SEQ (bit07 -00)							
	FIFLRP SEQ STS (07:00)							
4C	HMA: LRP_FIF_STS (bit31 -24)							
	XR ERR STS (15:08)							
4D	HMA: LRP_FIF_STS (bit23 -16)							
	XR ERR STS (07:00)							
4E	HMA: LRP_FIF_STS (bit15 -08)							
	DX SWTX SEQ (07:00)							
4F	HMA: LRP_FIF_STS (bit07 -00)							
	DX SWRX SEQ (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_FIF_DXBF_ADRLOG (bit31 -24)							
	DXBF_ADRLOG (31:24)							
51	HMA: LRP_FIF_DXBF_ADRLOG (bit23 -16)							
	DXBF_ADRLOG (23:16)							
52	HMA: LRP_FIF_DXBF_ADRLOG (bit15 -08)							
	DXBF_ADRLOG (15:08)							
53	HMA: LRP_FIF_DXBF_ADRLOG (bit07 -00)							
	DXBF_ADRLOG (07:00)							
54	HMA: LRPn_FIF_XR_ADRLOG (bit31 -24)							
	XR_ADRLOG (bit31 -24)							
55	HMA: LRPn_FIF_XR_ADRLOG (bit23 -16)							
	XR_ADRLOG (bit23 -16)							
56	HMA: LRPn_FIF_XR_ADRLOG (bit15 -08)							
	XR_ADRLOG (bit15 -08)							
57	HMA: LRPn_FIF_XR_ADRLOG (bit07 -00)							
	XR_ADRLOG (bit07 -00)							
58	HMA: LRPn_FIF_PCI_HD4_LOG (bit31 -24)							
	FMT	FMT	FMT	TYP	TYP	TYP	TYP	TYP
59	HMA: LRPn_FIF_PCI_HD4_LOG (bit23 -16)							
	Reserved	TC	TC	TC	Reserved	ATTR	Reserved	TH
5A	HMA: LRPn_FIF_PCI_HD4_LOG (bit15 -08)							
	TD	EP	ATTR	ATTR	AT	AT	LEN	LEN
5B	HMA: LRPn_FIF_PCI_HD4_LOG (bit07 -00)							
	LEN	LEN	LEN	LEN	LEN	LEN	LEN	LEN
5C	HMA: LRPn_FIF_PCI_HD8_LOG (bit31 -24)							
	CMPBUS# (07:00)							
5D	HMA: LRPn_FIF_PCI_HD8_LOG (bit23 -16)							
	CMPSOURCE DEV# (07:00)							
5E	HMA: LRPn_FIF_PCI_HD8_LOG (bit15 -08)							
	ST	ST	ST	BMC	BCNT	BCNT	BCNT	BCNT
5F	HMA: LRPn_FIF_PCI_HD8_LOG (bit07 -00)							
	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR_STS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: LRPn_ERR_STS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR_STS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	HMA: LRPn_ERR_STS (bit07 -00)							
	FIFXRPCI	FIFDXLRP	FCTL	FPCITX	FPCIRX	Reserved	ERR1	ERR0
64	HMA: LRP4 DS HMA INFO 0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: LRP4 DS HMA INFO 0 (bit23 -16)							
	Reserved	Reserved	Ppath5 STS	Ppath4 STS	Ppath3 STS	Ppath2 STS	Ppath1 STS	Ppath0 STS
66	HMA: LRP4 DS HMA INFO 0 (bit15 -08)							
	CM13 STS	CM03 STS	CM12 STS	CM02 STS	CM11 STS	CM01 STS	CM10 STS	CM00 STS
67	HMA: LRP4 DS HMA INFO 0 (bit07 -00)							
	Epath1 STS	Epath0 STS	Ipath1 STS	Ipath0 STS	Reserved	Reserved	Reserved	HMA STS
68	HMA: LRP4 DS HMA INFO 1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	HMA: LRP4 DS HMA INFO 1 (bit23 -16)							
	Reserved	Reserved	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
6A	HMA: LRP4 DS HMA INFO 1 (bit15 -08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
6B	HMA: LRP4 DS HMA INFO 1 (bit07 -00)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	Reserved	Reserved	Reserved	HMA EN
6C	HMA: LRP4 DS HMA INFO 23 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRP4 DS HMA INFO 23 (bit23 -16)							
	Reserved	Reserved	Ppath5 INT	Ppath4 INT	Ppath3 INT	Ppath2 INT	Ppath1 INT	Ppath0 INT
6E	HMA: LRP4 DS HMA INFO 23 (bit15 -08)							
	CM13 INT	CM03 INT	CM12 INT	CM02 INT	CM11 INT	CM01 INT	CM10 INT	CM00 INT
6F	HMA: LRP4 DS HMA INFO 23 (bit07 -00)							
	Epath1 INT	Epath0 INT	Ipath1 INT	Ipath0 INT	Reserved	Reserved	Reserved	HMA INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: INT1_MAILBOX_INT_STATUS0 (bit31 -24)							
	MBOX INT MP31	MBOX INT MP30	MBOX INT MP29	MBOX INT MP28	MBOX INT MP27	MBOX INT MP26	MBOX INT MP25	MBOX INT MP24
71	HMA: INT1_MAILBOX_INT_STATUS0 (bit23 -16)							
	MBOX INT MP23	MBOX INT MP22	MBOX INT MP21	MBOX INT MP20	MBOX INT MP19	MBOX INT MP18	MBOX INT MP17	MBOX INT MP16
72	HMA: INT1_MAILBOX_INT_STATUS0 (bit15 -08)							
	MBOX INT MP15	MBOX INT MP14	MBOX INT MP13	MBOX INT MP12	MBOX INT MP11	MBOX INT MP10	MBOX INT MP09	MBOX INT MP08
73	HMA: INT1_MAILBOX_INT_STATUS0 (bit07 -00)							
	MBOX INT MP07	MBOX INT MP06	MBOX INT MP05	MBOX INT MP04	MBOX INT MP03	MBOX INT MP02	MBOX INT MP01	MBOX INT MP00
74	HMA: INT1_MAILBOX_ABT_STATUS0 (bit31 -24)							
	MBOX ABT MP31	MBOX ABT MP30	MBOX ABT MP29	MBOX ABT MP28	MBOX ABT MP27	MBOX ABT MP26	MBOX ABT MP25	MBOX ABT MP24
75	HMA: INT1_MAILBOX_ABT_STATUS0 (bit23 -16)							
	MBOX ABT MP23	MBOX ABT MP22	MBOX ABT MP21	MBOX ABT MP20	MBOX ABT MP19	MBOX ABT MP18	MBOX ABT MP17	MBOX ABT MP16
76	HMA: INT1_MAILBOX_ABT_STATUS0 (bit15 -08)							
	MBOX ABT MP15	MBOX ABT MP14	MBOX ABT MP13	MBOX ABT MP12	MBOX ABT MP11	MBOX ABT MP10	MBOX ABT MP09	MBOX ABT MP08
77	HMA: INT1_MAILBOX_ABT_STATUS0 (bit07 -00)							
	MBOX ABT MP07	MBOX ABT MP06	MBOX ABT MP05	MBOX ABT MP04	MBOX ABT MP03	MBOX ABT MP02	MBOX ABT MP01	MBOX ABT MP00
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ③ (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(21) Byte28 = 38/58 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: INT0_INT_STATUS0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: INT0_INT_STATUS0 (bit23 -16)							
	Reserved	Reserved	Reserved	INT INT CHK1B	Reserved	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	HMA: INT0_INT_STATUS0 (bit15 -08)							
	Reserved	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Reserved	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	HMA: INT0_INT_STATUS0 (bit07 -00)							
	Reserved	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Reserved	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	HMA: LRPn_CTL (bit31 -24)							
	START (07:00)							
45	HMA: LRPn_CTL (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_CTL (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_CTL (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	HMA: LRPn_STS (bit31 -24)							
	ACT	ERRSTP	Reserved	ERR	WRN	Reserved	DGWAIT	DGPASS
49	HMA: LRPn_STS (bit23 -16)							
	SEQ (07:00)							
4A	HMA: LRPn_STS (bit15 -08)							
	Now ADR (15:08)							
4B	HMA: LRPn_STS (bit07 -00)							
	Now ADR (07:00)							
4C	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit31 -24)							
	JUMPADR_LOG1 (15:08)							
4D	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit23 -16)							
	JUMPADR_LOG1 (07:00)							
4E	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit15 -08)							
	JUMPADR_LOG0 (15:08)							
4F	HMA: LRPn_JUMP_ADR_LOG_0_1 (bit07 -00)							
	JUMPADR_LOG0 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ① (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit31 -24)							
	JUMPADR_LOG3 (15:08)							
51	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit23 -16)							
	JUMPADR_LOG3 (07:00)							
52	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit15 -08)							
	JUMPADR_LOG2 (15:08)							
53	HMA: LRPn_JUMP_ADR_LOG_2_3 (bit07 -00)							
	JUMPADR_LOG2 (07:00)							
54	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit31 -24)							
	JUMPADR_LOG5 (15:08)							
55	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit23 -16)							
	JUMPADR_LOG5 (07:00)							
56	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit15 -08)							
	JUMPADR_LOG4 (15:08)							
57	HMA: LRPn_JUMP_ADR_LOG_4_5 (bit07 -00)							
	JUMPADR_LOG4 (07:00)							
58	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit31 -24)							
	JUMPADR_LOG7 (15:08)							
59	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit23 -16)							
	JUMPADR_LOG7 (07:00)							
5A	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit15 -08)							
	JUMPADR_LOG6 (15:08)							
5B	HMA: LRPn_JUMP_ADR_LOG_6_7 (bit07 -00)							
	JUMPADR_LOG6 (07:00)							
5C	HMA: LRPn_ERR0 (bit31 -24)							
	ALUCMP ERR	SEQE ERR	TIMOUT	0JUMP	TIMER PERR	X2PERR	X1PERR	X0PERR
5D	HMA: LRPn_ERR0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	HMA: LRPn_ERR0 (bit15 -08)							
	Reserved	Reserved	CSAD ECC	CSUC ECC	CSODTP	CSOADP	CSIDTP	CSIADP
5F	HMA: LRPn_ERR0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR1 (bit31 -24)							
	DSO_LRP	DSO_DMA	DSO_XR	DSO_PPCI	Reserved	DSI_LRP	DSI_XR	DSI_PPCI
61	HMA: LRPn_ERR1 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR1 (bit15 -08)							
	DS OAW3	DS OAW2	DS OAW1	DS OAW0	DS OUNCW3	DS OUNCW2	DS OUNCW1	DS OUNCW0
63	HMA: LRPn_ERR1 (bit07 -00)							
	DSOADP	DSODTP	Reserved	DSIADP	DSIDTPW3	DSIDTPW2	DSIDTPW1	DSIDTPW0
64	HMA: LRPn_PCIRX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	MEMDRP	ECCCRE	ECCADR
65	HMA: LRPn_PCIRX_ERR (bit23 -16)							
	Reserved	Reserved	RAMOP	RAMINP	TXADRP	SEQENC	SEQDEC	RDTO
66	HMA: LRPn_PCIRX_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
67	HMA: LRPn_PCIRX_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
68	HMA: LRPn_FPCI_RX_MODE (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	ECCINH	SEQRES	SEQERR
69	HMA: LRPn_FPCI_RX_MODE (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	SWBSYOF	SWFRST	SWSTOP	SWERST
6A	HMA: LRPn_FPCI_RX_MODE (bit15 -08)							
	SWRX_TIMER VAL (15:08)							
6B	HMA: LRPn_FPCI_RX_MODE (bit07 -00)							
	SWRX_TIMER VAL (07:00)							
6C	HMA: LRPn_PCITX_ERR (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRPn_PCITX_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	HMA: LRPn_PCITX_ERR (bit15 -08)							
	Reserved	LENP	H8P	H423P	PENDP	ECNTP	DTP	ADRP
6F	HMA: LRPn_PCITX_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	SEQ	TIMOUT	STS	CPTY	OVRUN

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: LRPn_FPCI_TX_SEQ (bit31 -24)							
	RX SW SEQ STS (07:00)							
71	HMA: LRPn_FPCI_TX_SEQ (bit23 -16)							
	RX SEQ STS (07:00)							
72	HMA: LRPn_FPCI_TX_SEQ (bit15 -08)							
	TX SW SEQ STS (07:00)							
73	HMA: LRPn_FPCI_TX_SEQ (bit07 -00)							
	TX SEQ STS (07:00)							
74	HMA: LRPn_FCTL_ERR (bit31 -24)							
	CSLRC	CSLCNT1	CSLCNT2	CSLSEQ	CSLTOP	CSLTOUT	CSLXCTP	CSLBKP
75	HMA: LRPn_FCTL_ERR (bit23 -16)							
	CSLADRP	CSLDTP	DXBASP	LRPADP	DXERR	Reserved	Reserved	Reserved
76	HMA: LRPn_FCTL_ERR (bit15 -08)							
	XRDXDP	XRDXAP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	HMA: LRPn_FCTL_ERR (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	HMA: LRPn_FCTL_CSLD_BANK (bit31 -24)							
	EN	Reserved	Reserved	LINE3 BANK (04:00)				
79	HMA: LRPn_FCTL_CSLD_BANK (bit23 -16)							
	EN	Reserved	Reserved	LINE2 BANK (04:00)				
7A	HMA: LRPn_FCTL_CSLD_BANK (bit15 -08)							
	EN	Reserved	Reserved	LINE1 BANK (04:00)				
7B	HMA: LRPn_FCTL_CSLD_BANK (bit07 -00)							
	EN	Reserved	Reserved	LINE0 BANK (04:00)				
7C	HMA: LRPn_FCTL_CSLD_SEQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	HMA: LRPn_FCTL_CSLD_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	HMA: LRPn_FCTL_CSLD_SEQ (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	HMA: LRPn_FCTL_CSLD_SEQ (bit07 -00)							
	SEQ STS (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ② (1/4)

	0	1	2	3	4	5	6	7
40	HMA: LRPn_FIF_DXLRP_ERR (bit31 -24)							
	RDCPL	DTOP	DTIP	SEQ	BEERR	ADRERR	TIM2	TIM3
41	HMA: LRPn_FIF_DXLRP_ERR (bit23 -16)							
	TXHLRC	TXDT	TXTO	TXTOTO	TXWCNT	TXENC	TXDEC	TXDLRC
42	HMA: LRPn_FIF_DXLRP_ERR (bit15 -08)							
	Reserved	RXREQ	RXVLD	RXDLRC	RXPCCNT	RXNPCNT	RXHED	RXDLRC
43	HMA: LRPn_FIF_DXLRP_ERR (bit07 -00)							
	RXHLRC	RXDTP	RXTO	RXTOTO	RXWDCNT	RXENC	RXDEC	Reserved
44	HMA: LRPn_FIF_XRPCI_ERR (bit31 -24)							
	ADRP	DTOP	DTIP	SEQ	BEP	TIMOV	STS	Reserved
45	HMA: LRPn_FIF_XRPCI_ERR (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	HMA: LRPn_FIF_XRPCI_ERR (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	HMA: LRPn_FIF_XRPCI_ERR (bit07 -00)							
	ADRP	WDTP	WBEP	RDTP	WSEL	RSEL	CMP	SEQ
48	HMA: LRPn_FIF_SEQ (bit31 -24)							
	XR SEQ STS (07:00)							
49	HMA: LRPn_FIF_SEQ (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	HMA: LRPn_FIF_SEQ (bit15 -08)							
	DXBF SEQ STS (07:00)							
4B	HMA: LRPn_FIF_SEQ (bit07 -00)							
	FIFLRP SEQ STS (07:00)							
4C	HMA: LRP_FIF_STS (bit31 -24)							
	XR ERR STS (15:08)							
4D	HMA: LRP_FIF_STS (bit23 -16)							
	XR ERR STS (07:00)							
4E	HMA: LRP_FIF_STS (bit15 -08)							
	DX SWTX SEQ (07:00)							
4F	HMA: LRP_FIF_STS (bit07 -00)							
	DX SWRX SEQ (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ② (2/4)

	0	1	2	3	4	5	6	7
50	HMA: LRP_FIF_DXBF_ADRLOG (bit31 -24)							
	DXBF_ADRLOG (31:24)							
51	HMA: LRP_FIF_DXBF_ADRLOG (bit23 -16)							
	DXBF_ADRLOG (23:16)							
52	HMA: LRP_FIF_DXBF_ADRLOG (bit15 -08)							
	DXBF_ADRLOG (15:08)							
53	HMA: LRP_FIF_DXBF_ADRLOG (bit07 -00)							
	DXBF_ADRLOG (07:00)							
54	HMA: LRPn_FIF_XR_ADRLOG (bit31 -24)							
	XR_ADRLOG (bit31 -24)							
55	HMA: LRPn_FIF_XR_ADRLOG (bit23 -16)							
	XR_ADRLOG (bit23 -16)							
56	HMA: LRPn_FIF_XR_ADRLOG (bit15 -08)							
	XR_ADRLOG (bit15 -08)							
57	HMA: LRPn_FIF_XR_ADRLOG (bit07 -00)							
	XR_ADRLOG (bit07 -00)							
58	HMA: LRPn_FIF_PCI_HD4_LOG (bit31 -24)							
	FMT	FMT	FMT	TYP	TYP	TYP	TYP	TYP
59	HMA: LRPn_FIF_PCI_HD4_LOG (bit23 -16)							
	Reserved	TC	TC	TC	Reserved	ATTR	Reserved	TH
5A	HMA: LRPn_FIF_PCI_HD4_LOG (bit15 -08)							
	TD	EP	ATTR	ATTR	AT	AT	LEN	LEN
5B	HMA: LRPn_FIF_PCI_HD4_LOG (bit07 -00)							
	LEN	LEN	LEN	LEN	LEN	LEN	LEN	LEN
5C	HMA: LRPn_FIF_PCI_HD8_LOG (bit31 -24)							
	CMPBUS# (07:00)							
5D	HMA: LRPn_FIF_PCI_HD8_LOG (bit23 -16)							
	CMPSOURCE DEV# (07:00)							
5E	HMA: LRPn_FIF_PCI_HD8_LOG (bit15 -08)							
	ST	ST	ST	BMC	BCNT	BCNT	BCNT	BCNT
5F	HMA: LRPn_FIF_PCI_HD8_LOG (bit07 -00)							
	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT	BCNT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ② (3/4)

	0	1	2	3	4	5	6	7
60	HMA: LRPn_ERR_STS (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	HMA: LRPn_ERR_STS (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	HMA: LRPn_ERR_STS (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	HMA: LRPn_ERR_STS (bit07 -00)							
	FIFXRPCI	FIFDXLRP	FCTL	FPCITX	FPCIRX	Reserved	ERR1	ERR0
64	HMA: LRP4 DS HMA INFO 0 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	HMA: LRP4 DS HMA INFO 0 (bit23 -16)							
	Reserved	Reserved	Ppath5 STS	Ppath4 STS	Ppath3 STS	Ppath2 STS	Ppath1 STS	Ppath0 STS
66	HMA: LRP4 DS HMA INFO 0 (bit15 -08)							
	CM13 STS	CM03 STS	CM12 STS	CM02 STS	CM11 STS	CM01 STS	CM10 STS	CM00 STS
67	HMA: LRP4 DS HMA INFO 0 (bit07 -00)							
	Epath1 STS	Epath0 STS	Ipath1 STS	Ipath0 STS	Reserved	Reserved	Reserved	HMA STS
68	HMA: LRP4 DS HMA INFO 1 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	HMA: LRP4 DS HMA INFO 1 (bit23 -16)							
	Reserved	Reserved	Ppath5 EN	Ppath4 EN	Ppath3 EN	Ppath2 EN	Ppath1 EN	Ppath0 EN
6A	HMA: LRP4 DS HMA INFO 1 (bit15 -08)							
	CM13 EN	CM03 EN	CM12 EN	CM02 EN	CM11 EN	CM01 EN	CM10 EN	CM00 EN
6B	HMA: LRP4 DS HMA INFO 1 (bit07 -00)							
	Epath1 EN	Epath0 EN	Ipath1 EN	Ipath0 EN	Reserved	Reserved	Reserved	HMA EN
6C	HMA: LRP4 DS HMA INFO 23 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	HMA: LRP4 DS HMA INFO 23 (bit23 -16)							
	Reserved	Reserved	Ppath5 INT	Ppath4 INT	Ppath3 INT	Ppath2 INT	Ppath1 INT	Ppath0 INT
6E	HMA: LRP4 DS HMA INFO 23 (bit15 -08)							
	CM13 INT	CM03 INT	CM12 INT	CM02 INT	CM11 INT	CM01 INT	CM10 INT	CM00 INT
6F	HMA: LRP4 DS HMA INFO 23 (bit07 -00)							
	Epath1 INT	Epath0 INT	Ipath1 INT	Ipath0 INT	Reserved	Reserved	Reserved	HMA INT

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ② (4/4)

	0	1	2	3	4	5	6	7
70	HMA: INT1_MAILBOX_INT_STATUS0 (bit31 -24)							
	MBOX INT MP31	MBOX INT MP30	MBOX INT MP29	MBOX INT MP28	MBOX INT MP27	MBOX INT MP26	MBOX INT MP25	MBOX INT MP24
71	HMA: INT1_MAILBOX_INT_STATUS0 (bit23 -16)							
	MBOX INT MP23	MBOX INT MP22	MBOX INT MP21	MBOX INT MP20	MBOX INT MP19	MBOX INT MP18	MBOX INT MP17	MBOX INT MP16
72	HMA: INT1_MAILBOX_INT_STATUS0 (bit15 -08)							
	MBOX INT MP15	MBOX INT MP14	MBOX INT MP13	MBOX INT MP12	MBOX INT MP11	MBOX INT MP10	MBOX INT MP09	MBOX INT MP08
73	HMA: INT1_MAILBOX_INT_STATUS0 (bit07 -00)							
	MBOX INT MP07	MBOX INT MP06	MBOX INT MP05	MBOX INT MP04	MBOX INT MP03	MBOX INT MP02	MBOX INT MP01	MBOX INT MP00
74	HMA: INT1_MAILBOX_ABT_STATUS0 (bit31 -24)							
	MBOX ABT MP31	MBOX ABT MP30	MBOX ABT MP29	MBOX ABT MP28	MBOX ABT MP27	MBOX ABT MP26	MBOX ABT MP25	MBOX ABT MP24
75	HMA: INT1_MAILBOX_ABT_STATUS0 (bit23 -16)							
	MBOX ABT MP23	MBOX ABT MP22	MBOX ABT MP21	MBOX ABT MP20	MBOX ABT MP19	MBOX ABT MP18	MBOX ABT MP17	MBOX ABT MP16
76	HMA: INT1_MAILBOX_ABT_STATUS0 (bit15 -08)							
	MBOX ABT MP15	MBOX ABT MP14	MBOX ABT MP13	MBOX ABT MP12	MBOX ABT MP11	MBOX ABT MP10	MBOX ABT MP09	MBOX ABT MP08
77	HMA: INT1_MAILBOX_ABT_STATUS0 (bit07 -00)							
	MBOX ABT MP07	MBOX ABT MP06	MBOX ABT MP05	MBOX ABT MP04	MBOX ABT MP03	MBOX ABT MP02	MBOX ABT MP01	MBOX ABT MP00
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ③ (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ③ (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ③ (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(22) Byte28 = 39/59 ③ (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ① (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XD_CTL_CHK4_ERQ (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	HMA: XD_CTL_CHK4_ERQ (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
42	HMA: XD_CTL_CHK4_ERQ (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
43	HMA: XD_CTL_CHK4_ERQ (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
44	HMA: XD_CTL_CHK4_MSG (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	HMA: XD_CTL_CHK4_MSG (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
46	HMA: XD_CTL_CHK4_MSG (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
47	HMA: XD_CTL_CHK4_MSG (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
48	HMA: XD_CTL_CHK4_TRASH (bit31 -24)							
	MOW COT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	HMA: XD_CTL_CHK4_TRASH (bit23 -16)							
	DEV5 FUNC3	DEV5 FUNC2	DEV5 FUNC1	DEV5 FUNC0	DEV4 FUNC3	DEV4 FUNC2	DEV4 FUNC1	DEV4 FUNC0
4A	HMA: XD_CTL_CHK4_TRASH (bit15 -08)							
	DEV3 FUNC3	DEV3 FUNC2	DEV3 FUNC1	DEV3 FUNC0	DEV2 FUNC3	DEV2 FUNC2	DEV2 FUNC1	DEV2 FUNC0
4B	HMA: XD_CTL_CHK4_TRASH (bit07 -00)							
	DEV1 FUNC3	DEV1 FUNC2	DEV1 FUNC1	DEV1 FUNC0	DEV0 FUNC3	DEV0 FUNC2	DEV0 FUNC1	DEV0 FUNC0
4C	HMA: XD_CTL_CHK4_MONI (bit31 -24)							
	M7C1 TRASH	M6C1 TRASH	M5C1 TRASH	M4C1 TRASH	M3C1 TRASH	M2C1 TRASH	M1C1 TRASH	M0C1 TRASH
4D	HMA: XD_CTL_CHK4_MONI (bit23 -16)							
	M7C0 TRASH	M6C0 TRASH	M5C0 TRASH	M4C0 TRASH	M3C0 TRASH	M2C0 TRASH	M1C0 TRASH	M0C0 TRASH
4E	HMA: XD_CTL_CHK4_MONI (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	HMA: XD_CTL_CHK4_MONI (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	TR OTHER MOD	TR OWN MOD	MSG	ERQ

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ① (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ① (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XD_DTX_TLOG_B0 (bit31 -24)							
	TRASH LOG B0 (31:24)							
61	HMA: XD_DTX_TLOG_B0 (bit23 -16)							
	TRASH LOG B0 (23:16)							
62	HMA: XD_DTX_TLOG_B0 (bit15 -08)							
	TRASH LOG B0 (15:08)							
63	HMA: XD_DTX_TLOG_B0 (bit07 -00)							
	TRASH LOG B0 (07:00)							
64	HMA: XD_DTX_TLOG_B1 (bit31 -24)							
	TRASH LOG B1 (31:24)							
65	HMA: XD_DTX_TLOG_B1 (bit23 -16)							
	TRASH LOG B1 (23:16)							
66	HMA: XD_DTX_TLOG_B1 (bit15 -08)							
	TRASH LOG B1 (15:08)							
67	HMA: XD_DTX_TLOG_B1 (bit07 -00)							
	TRASH LOG B1 (07:00)							
68	HMA: XD_DTX_TLOG_B2 (bit31 -24)							
	TRASH LOG B2 (31:24)							
69	HMA: XD_DTX_TLOG_B2 (bit23 -16)							
	TRASH LOG B2 (23:16)							
6A	HMA: XD_DTX_TLOG_B2 (bit15 -08)							
	TRASH LOG B2 (15:08)							
6B	HMA: XD_DTX_TLOG_B2 (bit07 -00)							
	TRASH LOG B2 (07:00)							
6C	HMA: XD_DTX_TLOG_B3 (bit31 -24)							
	TRASH LOG B3 (31:24)							
6D	HMA: XD_DTX_TLOG_B3 (bit23 -16)							
	TRASH LOG B3 (23:16)							
6E	HMA: XD_DTX_TLOG_B3 (bit15 -08)							
	TRASH LOG B3 (15:08)							
6F	HMA: XD_DTX_TLOG_B3 (bit07 -00)							
	TRASH LOG B3 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ① (4/4)

	0	1	2	3	4	5	6	7
70	HMA: XD_DTX_TLOG_B4 (bit31 -24)							
	TRASH LOG B4 (31:24)							
71	HMA: XD_DTX_TLOG_B4 (bit23 -16)							
	TRASH LOG B4 (23:16)							
72	HMA: XD_DTX_TLOG_B4 (bit15 -08)							
	TRASH LOG B4 (15:08)							
73	HMA: XD_DTX_TLOG_B4 (bit07 -00)							
	TRASH LOG B4 (07:00)							
74	HMA: XD_DTX_TLOG_B5 (bit31 -24)							
	TRASH LOG B5 (31:24)							
75	HMA: XD_DTX_TLOG_B5 (bit23 -16)							
	TRASH LOG B5 (23:16)							
76	HMA: XD_DTX_TLOG_B5 (bit15 -08)							
	TRASH LOG B5 (15:08)							
77	HMA: XD_DTX_TLOG_B5 (bit07 -00)							
	TRASH LOG B5 (07:00)							
78	HMA: XD_DTX_TLOG_B6 (bit31 -24)							
	TRASH LOG B6 (31:24)							
79	HMA: XD_DTX_TLOG_B6 (bit23 -16)							
	TRASH LOG B6 (23:16)							
7A	HMA: XD_DTX_TLOG_B6 (bit15 -08)							
	TRASH LOG B6 (15:08)							
7B	HMA: XD_DTX_TLOG_B6 (bit07 -00)							
	TRASH LOG B6 (07:00)							
7C	HMA: XD_DTX_TLOG_B7 (bit31 -24)							
	TRASH LOG B7 (31:24)							
7D	HMA: XD_DTX_TLOG_B7 (bit23 -16)							
	TRASH LOG B7 (23:16)							
7E	HMA: XD_DTX_TLOG_B7 (bit15 -08)							
	TRASH LOG B7 (15:08)							
7F	HMA: XD_DTX_TLOG_B7 (bit07 -00)							
	TRASH LOG B7 (07:00)							

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ② (1/4)

	0	1	2	3	4	5	6	7
40	CHK4 INT MSG WD0 (bit31 -24)							
	EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	CHK4 INT MSG WD0 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
42	CHK4 INT MSG WD0 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
43	CHK4 INT MSG WD0 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
44	CHK4 INT MSG WD1 (bit31 -24)							
	INT CHK1B	LRP4 CHK1B	LRP3-0 CHK1B	SWIF CHK1B	BARB CHK1B	IARB CHK1B	EARB CHK1B	IXARB CHK1B
45	CHK4 INT MSG WD1 (bit23 -16)							
	PARB CHK1B	XD CHK1B	DXC CHK1B	DXA CHK1B	DRR CHK1B	MPDMA DMAMB CHK1B	DMA CHK1B	RGA CHK1B
46	CHK4 INT MSG WD1 (bit15 -08)							
	FMT CHK1B	BRAM BCOM SH CHK1B	SMC CHK1B	SMBUS CHK1B	CHK4	CHK3	CHK2	WARN
47	CHK4 INT MSG WD1 (bit07 -00)							
	Reserved	Reserved	MBOX INT	LRP4 INT	LRP3 INT	LRP2 INT	LRP1 INT	LRP0 INT
48	CHK4 INT MSG WD2 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	CHK4 INT MSG WD2 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	CHK4 INT MSG WD2 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4B	CHK4 INT MSG WD2 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4C	CHK4 INT MSG WD3 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	CHK4 INT MSG WD3 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	CHK4 INT MSG WD3 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	CHK4 INT MSG WD3 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ② (2/4)

	0	1	2	3	4	5	6	7
50	CHK4 INTERRUPT VECTOR (bit31 -24)							
	INT VECTOR NUM (31:24)							
51	CHK4 INTERRUPT VECTOR (bit23 -16)							
	INT VECTOR NUM (23:16)							
52	CHK4 INTERRUPT VECTOR (bit15 -08)							
	INT VECTOR NUM (15:08)							
53	CHK4 INTERRUPT VECTOR (bit07 -00)							
	INT VECTOR NUM (07:00)							
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ② (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ② (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ③ (1/4)

	0	1	2	3	4	5	6	7
40	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
41	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
42	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
43	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
44	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
48	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ③ (2/4)

	0	1	2	3	4	5	6	7
50	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
53	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
54	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
56	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
57	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
58	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ③ (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
62	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
63	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
64	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
67	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 84 (CHK4) Byte40-7F Detail

(23) Byte28 = 3A/5A ③ (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
73	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
77	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 89 & Byte0D Bit2 = 1 (MAIN Blade CHK2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK Information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	Reserved					
10	JCB ID							
11	LDEV#high (Logical DKC#)							
12	LDEV#low (LDEV# in DKC)							
13								
14	CDEV#							
15	RDEV#							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27		Format (x'8')			Message (x'9')			
28	Subcode (See following pages)							
29	Detail Information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Reserved							
33								
34	Module ID 1							
35	Routine ID 1							
36	Module ID 2							
37	Routine ID 2							
38	Master Path Number							
39	SCSI Initiator ID							
3A	SCSI Target ID							
3B	Logical Unit Number							
3C	SCSI Command Code							
3D	Reserved							
3E								
3F								
40	Detail Information (See following pages)							
|								
|								
7F								

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Byte27 = 89 (MAIN Blade CHK2) Byte28-31 Detail

(1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15

	0	1	2	3	4	5	6	7
28	Subcode (x‘00’ or x‘01’ or x‘02’ or x‘03’ or x‘04’ or x‘05’ : MAIN Blade CHK2 – DMA Error) Subcode (x‘10’ or x‘11’ or x‘12’ or x‘13’ or x‘14’ or x‘15’ : MAIN Blade CHK2 – DMA Timeout)							
29	INT_STATUS0 (b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2A	INT_STATUS0 (b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
2B	INT_STATUS0 (b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
2C	INT_STATUS0 (b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B
2D	INT_STATUS4 (b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2E	INT_STATUS4 (b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2F	INT_STATUS4 (b15 – 08)							
	DRR3 CHK2	DRR2 CHK2	DRR1 CHK2	DRR0 CHK2	(RSV)	(RSV)	DMAMB1 CHK2	DMAMB0 CHK2
30	INT_STATUS4 (b07 – 00)							
	(RSV)	(RSV)	DMA5 CHK2	DMA4 CHK2	DMA3 CHK2	DMA2 CHK2	DMA1 CHK2	DMA0 CHK2
31	HMA_STATUS (b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM(0)	(RSV)	(RSV)	IX MODE

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Byte27 = 89 (MAIN Blade CHK2) Byte28-31 Detail

(2) Byte28 = 08/0c/18/1c

	0	1	2	3	4	5	6	7
28	Subcode (x‘08’ or x‘0c’) Subcode (x‘18’ or x‘1c’)			MAIN Blade CHK2 DMA IPath Error MAIN Blade CHK2 DMA Timeout				
29	INT_STATUS0 (b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2A	INT_STATUS0 (b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
2B	INT_STATUS0 (b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
2C	INT_STATUS0 (b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B
2D	INT_STATUS4 (b15 – 08)							
	DRR3 CHK2	DRR2 CHK2	DRR1 CHK2	DRR0 CHK2	(RSV)	(RSV)	DMAMB1 CHK2	DMAMB0 CHK2
2E	INT_STATUS4 (b07 – 00)							
	(RSV)	(RSV)	DMA5 CHK2	DMA4 CHK2	DMA3 CHK2	DMA2 CHK2	DMA1 CHK2	DMA0 CHK2
2F	INT_STATUS1 (b23 – 16)							
	(RSV)	(RSV)	BARBREG CHK1B	BARB CHK1B	IARB1REG CHK1B	IARB1 CHK1B	IARB0REG CHK1B	IARB0 CHK1B
30	DMA Number							
	DMA0 = 0x00 DMA1 = 0x01 DMA2 = 0x02 DMA3 = 0x03 DMA3 = 0x04 DMA3 = 0x05							
31	HMA_STATUS (b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM(0)	(RSV)	(RSV)	IX MODE

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15 (1/4)

	0	1	2	3	4	5	6	7
40	HMA_STATUS (bit31 -24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM(0)	(RSV)	(RSV)	IX MODE
41	HMA_STATUS (bit23 -16)							
	MP CHK CODE 0x41							
42	HMA_STATUS (bit15 -08)							
	LSI REV							
43	HMA_STATUS (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
44	DM_ERR_ST13 (bit31 -24)							
	DM_CP SEQERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	DM_ERR_ST13 (bit23 -16)							
	DM_CP NOTIDLE ERR	DM_CP SEMERR	DM_CP PRM PERR(1)	DM_CP PRM PERR(0)	DM_CP SADRCNT PERR	DM_CP DADR0CNT PERR	DM_CP DADR1CNT PERR	Reserved
46	DM_ERR_ST13 (bit15 -08)							
	DM_CP STSS PERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
47	DM_ERR_ST13 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
48	DM_ERR_ST14 (bit31 -24)							
	DM_RX_SWR SEQERR	DM_RX_SWR WDCNT PERR	Reserved	DM_RX_SWR TOCNT PERR	Reserved	Reserved	Reserved	Reserced
49	DM_ERR_ST14 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	DM_ERR_ST14 (bit15 -08)							
	DM_RX_SWT SEQERR	DM_RX_SWT WDCNT PERR	Reserved	DM_RX_SWT TOCNT PERR	DM_RX_SWT DT PERR	DM_RX_SWT HLRC ERR	DM_RX_SWT DLRC ERR	Reserved
4B	DM_ERR_ST14 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4C	DM_ERR_ST15 (bit31 -24)							
	DM_RX BFS0 SEQERR	DM_RX BFS1 SEQERR	DM_RX BFS2 SEQERR	DM_RX BFS3 SEQERR	DM_RX BFS4 SEQERR	DM_RX BFS5 SEQERR	DM_RX BFS6 SEQERR	DM_RX BFS7 SEQERR
4D	DM_ERR_ST15 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	DM_ERR_ST15 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4F	DM_ERR_ST15 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DM_RX_CMD RAC PERR	DM_RX_CM D HPC PERR

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15 (2/4)

	0	1	2	3	4	5	6	7
50	DM_ERR_ST16 (bit31 -24)							
	DM_RX_CMD SEQERR	DM_RX_CMD BP PERR	DM_RX_CMD RCNC PERR	DM_RX_CMD BS PERR	DM_RX_CMD BZS PERR	DM_RX_CMD BMP PERR	DM_RX_CMD DDLEN PERR	DM_RX_CMD RDLEN PERR
51	DM_ERR_ST16 (bit23 -16)							
	DM_RX_CMD BDLEN PERR	DM_RX_CMD CDLEN PERR	DM_RX_CMD HTAG PERR	DM_RX_CMD SADR PERR	DM_RX_CMD HDR PERR	DM_RX_CMD DCMP PERR	Reserved	DM_RX_CMD ZDLEN PERR
52	DM_ERR_ST16 (bit15 -08)							
	DM_RX_CMD TMR0 SEQERR	DM_RX_CMD TMR1 SEQERR	DM_RX_CMD TMR2 SEQERR	DM_RX_CMD TMR3 SEQERR	DM_RX_CMD TMR4 SEQERR	DM_RX_CMD TMR5 SEQERR	DM_RX_CMD TMR6 SEQERR	DM_RX_CMD TMR7 SEQERR
53	DM_ERR_ST16 (bit07 -00)							
	DM_RX_CMD TOCNT0 PERR	DM_RX_CMD TOCNT1 PERR	DM_RX_CMD TOCNT2 PERR	DM_RX_CMD TOCNT3 PERR	DM_RX_CMD TOCNT4 PERR	DM_RX_CMD TOCNT5 PERR	DM_RX_CMD TOCNT6 PERR	DM_RX_CMD TOCNT7 PERR
54	DM_ERR_ST18 (bit31 -24)							
	DM_RX_CMP SEQERR	DM_RX_CMP HSELCNT PERR	DM_RX_CMP RQHD PERR	DM_RX_CMP BS PERR	DM_RX_CMP DCMP PERR	Reserved	DM_RX_CMP ZRQHD PERR	DM_RX_CMP ZDCMP PERR
55	DM_ERR_ST18 (bit23 -16)							
	DM_RX_CMP ZRLEN PERR	DM_RX_CMP DRXCMP SEQERR	DM_RX_CMP DRXCMP MERR	DM_RX_CMP DRXCMP URERR	DM_RX_CMP W0DT PERR	DM_RX_CMP W1DT PERR	DM_RX_CMP W2DT PERR	DM_RX_CMP W3DT PERR
56	DM_ERR_ST18 (bit15 -08)							
	DM_RX_CMP W4DT PERR	DM_RX_CMP W5DT PERR	DM_RX_CMP W6DT PERR	Reserved	DM_RX_CMP ZDLEN PERR	DM_RX_CMP ZBDLEN PERR	DM_RX_CMP ZCDLEN PERR	DM_RX_CMP ZPDLEN PERR
57	DM_ERR_ST18 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	DM_RX_CMP BPC PERR	DM_RX_CMP RLEN PERR	DM_RX_CMP RDLEN PERR	DM_RX_CMP ZRQHDCMP PERR
58	DM_ERR_ST20 (bit31 -24)							
	DM_RX_DCL A SEQERR	DM_RX_DCL B SEQERR	DM_RX_DCL C SEQERR	DM_RX_DCL D SEQERR	Reserved	Reserved	Reserved	Reserved
59	DM_ERR_ST20 (bit23 -16)							
	DM_RX_DCL A MERR	DM_RX_DCL A_UR ERR	DM_RX_DCL B_T10SC PERR	DM_RX_DCL C_UR ERR	DM_RX_DCL C_T10SC PERR	DM_RX_DCL D_UR ERR	DM_RX_DCL D_T10SC PERR	DM_RX_DCL B_UR ERR
5A	DM_ERR_ST20 (bit15 -08)							
	DM_RX_DCL ZBDLEN PERR	DM_RX_DCL OCRC PERR	DM_RX_DCL GOCRC PERR	DM_RX_DCL LRC PERR	Reserved	Reserved	DM_RX_DCL BADR PERR	DM_RX_DCL DBFWDT PERR
5B	DM_ERR_ST20 (bit07 -00)							
	DM_RX_DCL W0DT PERR	DM_RX_DCL W1DT PERR	DM_RX_DCL W2DT PERR	DM_RX_DCL W3DT PERR	DM_RX_DCL W4DT PERR	DM_RX_DCL W5DT PERR	DM_RX_DCL W6DT PERR	DM_RX_DCL BP PERR
5C	DM_ERR_ST21(bit31 -24)							
	DM_RX_DCL T10CRC PERR	DM_RX_DCL T10GRTAG PERR	DM_RX_DCL T10CRTAG PERR	Reserved	Reserved	Reserved	Reserved	Reserved
5D	DM_ERR_ST21 (bit23 -16)							
	DM_RX_DCL DBV_BNC PERR	DM_RX_DCL DBV_BLC PERR	DM_RX_DCL DBV_LRC PERR	DM_RX_DCL DBV_TLRC PERR	DM_RX_DCL DBV_HD PERR	Reserved	Reserved	Reserved
5E	DM_ERR_ST21 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5F	DM_ERR_ST21 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15 (3/4)

	0	1	2	3	4	5	6	7
60	DM_ERR_ST23 (bit31 -24)							
	DM_TX0_CD CMD SEQERR	DM_TX0_CD TMR SEQERR	DM_TX0_CD CHK SEQERR	DM_TX0_CD RDLEN PERR	DM_TX0_CD HLEN PERR	DM_TX0_CD ZPCMP PERR	DM_TX0_CD ZBCMP PERR	DM_TX0_CD DACMP PERR
61	DM_ERR_ST23 (bit23 -16)							
	DM_TX0_CD ZPDLEN PERR	DM_TX0_CD ZBDLEN PERR	DM_TX0_CD ZRLEN PERR	DM_TX0_CD BP PERR	DM_TX0_CD BAC PERR	DM_TX0_CD DBF UNCRERR	DM_TX0_CD DBF ADRERR	DM_TX0_CD DBF PERR
62	DM_ERR_ST23 (bit15 -08)							
	DM_TX0_CD HTAG PERR	DM_TX0_CD DAC PERR	Reserved	DM_TX0_CD WRQHD PERR	DM_TX0_CD WAC PERR	DM_TX0_CD CHD PERR	DM_TX0_CD TOC PERR	DM_TX0_CD RQDLC PERR
63	DM_ERR_ST23 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
64	DM_ERR_ST24 (bit31 -24)							
	DM_TX0_CD CHK MERR	DM_TX0_CD CHK_UR ERR	DM_TX0_CD T10_SC PERR	DM_TX0_CD OCRC CERR	DM_TX0_CD OCRC PERR	DM_TX0_CD LRC CERR	DM_TX0_CD LRC PERR	Reserved
65	DM_ERR_ST24 (bit23 -16)							
	DM_TX0_CD T10CRC PERR	Reserved	DM_TX0_CD T10RTAG PERR	Reserved	Reserved	Reserved	Reserved	Reserved
66	DM_ERR_ST24 (bit15 -08)							
	DM_TX0_CD T10RTAG0 CERR	DM_TX0_CD T10RTAG1 CERR	DM_TX0_CD T10RTAG2 CERR	DM_TX0_CD T10RTAG3 CERR	DM_TX0_CD WRSEQ CERR	DM_TX0_CD T10ATAG0 CERR	DM_TX0_CD T10ATAG1 CERR	DM_TX0_CD T10CRC CERR
67	DM_ERR_ST24 (bit07 -00)							
	DM_TX0_CD EXFWRSEQ CERR	DM_TX0_CD EXLWRSEQ CERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
68	DM_ERR_ST26 (bit31 -24)							
	DM_TX0_SR SEQERR	DM_TX0_SR WDC PERR	Reserved	DM_TX0_SR TOC PERR	Reserved	Reserved	Reserved	Reserved
69	DM_ERR_ST26 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	DM_ERR_ST26 (bit15 -08)							
	DM_TX0_ST SEQERR	DM_TX0_ST WDC PERR	Reserved	DM_TX0_ST TOC PERR	DM_TX0_ST DT PERR	DM_TX0_ST HLRC ERR	DM_TX0_ST DLRC ERR	Reserved
6B	DM_ERR_ST26 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6C	DM_ERR_ST27 (bit31 -24)							
	DM_TX1_CD CMD SEQERR	DM_TX1_CD TMR SEQERR	DM_TX1_CD CHK SEQERR	DM_TX1_CD RDLEN PERR	DM_TX1_CD HLEN PERR	DM_TX1_CD ZPCMP PERR	DM_TX1_CD ZBCMP PERR	DM_TX1_CD DACMP PERR
6D	DM_ERR_ST27 (bit23 -16)							
	DM_TX1_CD ZPDLEN PERR	DM_TX1_CD ZBDLEN PERR	DM_TX1_CD ZRLEN PERR	DM_TX1_CD BP PERR	DM_TX1_CD BAC PERR	DM_TX1_CD DBF UNCRERR	DM_TX1_CD DBF ADRERR	DM_TX1_CD DBF PERR
6E	DM_ERR_ST27 (bit15 -08)							
	DM_TX1_CD HTAG PERR	DM_TX1_CD DAC PERR	Reserved	DM_TX1_CD WRQHD PERR	DM_TX1_CD WAC PERR	DM_TX1_CD CHD PERR	DM_TX1_CD TOC PERR	DM_TX1_CD RQDLC PERR
6F	DM_ERR_ST27 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/04/05/10/11/12/13/14/15 (4/4)

	0	1	2	3	4	5	6	7
70	DM_ERR_ST28 (bit31 -24)							
	DM_TX1_CD CHK MERR	DM_TX1_CD CHK_UR ERR	DM_TX1_CD T10_SC PERR	DM_TX1_CD OCRC CERR	DM_TX1_CD OCRC PERR	DM_TX1_CD LRC CERR	DM_TX1_CD LRC PERR	Reserved
71	DM_ERR_ST28 (bit23 -16)							
	DM_TX1_CD T10CRC PERR	Reserved	DM_TX1_CD T10RTAG PERR	Reserved	Reserved	Reserved	Reserved	Reserved
72	DM_ERR_ST28 (bit15 -08)							
	DM_TX1_CD T10RTAG0 CERR	DM_TX1_CD T10RTAG1 CERR	DM_TX1_CD T10RTAG2 CERR	DM_TX1_CD T10RTAG3 CERR	DM_TX1_CD WRSEQ CERR	DM_TX1_CD T10ATAG0 CERR	DM_TX1_CD T10ATAG1 CERR	DM_TX1_CD T10CRC CERR
73	DM_ERR_ST28 (bit07 -00)							
	DM_TX1_CD EXFWRSEQ CERR	DM_TX1_CD EXLWRSEQ CERR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
74	DM_ERR_ST30 (bit31 -24)							
	DM_TX0_SR SEQERR	DM_TX0_SR WDC PERR	Reserved	DM_TX0_SR TOC PERR	Reserved	Reserved	Reserved	Reserved
75	DM_ERR_ST30 (bit23 -16)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	DM_ERR_ST30 (bit15 -08)							
	DM_TX0_ST SEQERR	DM_TX0_ST WDC PERR	Reserved	DM_TX0_ST TOC PERR	DM_TX0_ST DT PERR	DM_TX0_ST HLRC ERR	DM_TX0_ST DLRC ERR	Reserved
77	DM_ERR_ST30 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
78	DM_WRN_ST00 (bit31 -24)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DM_TX0 DBF WRN
79	DM_WRN_ST00 (bit23 -16)							
	DM_TX1 DBF WRN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7A	DM_WRN_ST00 (bit15 -08)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7B	DM_WRN_ST00 (bit07 -00)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0(b31 – 24)							
	(RSV)	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRCERR	(RSV)	RXHDBUF WTPT PERR	(RSV)
41	HMA: XARB_RX_PCK_ERR0(b23 – 16)							
	(RSV)	RXNDBUF WTPT PERR	RXHDIX PERR	RXDTIX PERR	RXDTWT ADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RXNDIX PERR
42	HMA: XARB_RX_PCK_ERR0(b15 – 08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	RX PERR	(RSV)	(RSV)	(RSV)	(RSV)
43	HMA: XARB_RX_PCK_ERR0(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44	HMA: XARB_PCI_ECC_RCV(b31 – 24)							
	PCI ECC RCV	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
45	HMA: XARB_PCI_ECC_RCV(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46	HMA: XARB_PCI_ECC_RCV(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47	HMA: XARB_PCI_ECC_RCV(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48	HMA: XARB_TAGXTMR_GPERR(b31 – 24)							
	TAG0TMR GPERR	TAG1TMR GPERR	TAG2TMR GPERR	TAG3TMR GPERR	TAG4TMR GPERR	TAG5TMR GPERR	TAG6TMR GPERR	TAG7TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR(b23 – 16)							
	TAG8TMR GPERR	TAG9TMR GPERR	TAG10TMR GPERR	TAG11TMR GPERR	TAG12TMR GPERR	TAG13TMR GPERR	TAG14TMR GPERR	TAG15TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR(b15 – 08)							
	TAG16TMR GPERR	TAG17TMR GPERR	TAG18TMR GPERR	TAG19TMR GPERR	TAG20TMR GPERR	TAG21TMR GPERR	TAG22TMR GPERR	TAG23TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR(b07 – 00)							
	TAG24TMR GPERR	TAG25TMR GPERR	TAG26TMR GPERR	TAG27TMR GPERR	TAG28TMR GPERR	TAG29TMR GPERR	TAG30TMR GPERR	TAG31TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR(b31 – 24)							
	TAG0TMR SQ EERR	TAG1TMR SQ EERR	TAG2TMR SQ EERR	TAG3TMR SQ EERR	TAG4TMR SQ EERR	TAG5TMR SQ EERR	TAG6TMR SQ EERR	TAG7TMR SQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR(b23 – 16)							
	TAG8TMR SQ EERR	TAG9TMR SQ EERR	TAG10TMR SQ EERR	TAG11TMR SQ EERR	TAG12TMR SQ EERR	TAG13TMR SQ EERR	TAG14TMR SQ EERR	TAG15TMR SQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR(b15 – 08)							
	TAG16TMR SQ EERR	TAG17TMR SQ EERR	TAG18TMR SQ EERR	TAG19TMR SQ EERR	TAG20TMR SQ EERR	TAG21TMR SQ EERR	TAG22TMR SQ EERR	TAG23TMR SQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR(b07 – 00)							
	TAG24TMR SQ EERR	TAG25TMR SQ EERR	TAG26TMR SQ EERR	TAG27TMR SQ EERR	TAG28TMR SQ EERR	TAG29TMR SQ EERR	TAG30TMR SQ EERR	TAG31TMR SQ EERR

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR(b31 – 24)							
	TAG0TMR SQ PERR	TAG1TMR SQ PERR	TAG2TMR SQ PERR	TAG3TMR SQ PERR	TAG4TMR SQ PERR	TAG5TMR SQ PERR	TAG6TMR SQ PERR	TAG7TMR SQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR(b23 – 16)							
	TAG8TMR SQ PERR	TAG9TMR SQ PERR	TAG10TMR SQ PERR	TAG11TMR SQ PERR	TAG12TMR SQ PERR	TAG13TMR SQ PERR	TAG14TMR SQ PERR	TAG15TMR SQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR(b15 – 08)							
	TAG16TMR SQ PERR	TAG17TMR SQ PERR	TAG18TMR SQ PERR	TAG19TMR SQ PERR	TAG20TMR SQ PERR	TAG21TMR SQ PERR	TAG22TMR SQ PERR	TAG23TMR SQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR(b07 – 00)							
	TAG24TMR SQ PERR	TAG25TMR SQ PERR	TAG26TMR SQ PERR	TAG27TMR SQ PERR	TAG28TMR SQ PERR	TAG29TMR SQ PERR	TAG30TMR SQ PERR	TAG31TMR SQ PERR
54	HMA: XARB_TAGXTMR_TOERR(b31 – 24)							
	TAG0TMR TOERR	TAG1TMR TOERR	TAG2TMR TOERR	TAG3TMR TOERR	TAG4TMR TOERR	TAG5TMR TOERR	TAG6TMR TOERR	TAG7TMR TOERR
55	HMA: XARB_TAGXTMR_TOERR(b23 – 16)							
	TAG8TMR TOERR	TAG9TMR TOERR	TAG10TMR TOERR	TAG11TMR TOERR	TAG12TMR TOERR	TAG13TMR TOERR	TAG14TMR TOERR	TAG15TMR TOERR
56	HMA: XARB_TAGXTMR_TOERR(b15 – 08)							
	TAG16TMR TOERR	TAG17TMR TOERR	TAG18TMR TOERR	TAG19TMR TOERR	TAG20TMR TOERR	TAG21TMR TOERR	TAG22TMR TOERR	TAG23TMR TOERR
57	HMA: XARB_TAGXTMR_TOERR(b07 – 00)							
	TAG24TMR TOERR	TAG25TMR TOERR	TAG26TMR TOERR	TAG27TMR TOERR	TAG28TMR TOERR	TAG29TMR TOERR	TAG30TMR TOERR	TAG31TMR TOERR
58	HMA: XARB_RSV(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	HMA: XARB_RSV(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	HMA: XARB_RSV(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	HMA: XARB_RSV(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	HMA: XARB_TX_PCK_ERR0(b31 – 24)							
	TXHD RDPT PERR	TXNH RDPT PERR	TXNH WTPT PERR	TXND RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0(b23 – 16)							
	NHETY FRCERR	PDETY FRCERR	PHETY FRCERR	QETY FRCERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0(b15 – 08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDT RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0(b07 – 00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	(RSV)	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(3) Byte28 = 08/0c/18/1c (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1(b31 – 24)							
	ICNT FRCPERR	TXHDDT AFRCPERR	TXHDDT EFRCPERR	(RSV)	ICNT NPFRCPERR	NPHDBUF FRCPERR	TXDTBUF FRCPERR	TXNDBUF FRCPERR
61	HMA: XARB_TX_PCK_ERR1(b23 – 16)							
	CHCNT FRCERR	NHCNT FRCERR	PHCNT FRCERR	CDCNT FRCERR	NDCNT FRCERR	PDCNT FRCERR	(RSV)	(RSV)
62	HMA: XARB_TX_PCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	HMA: XARB_TX_PCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	HMA: XARB_TXDTBUF_CRT(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65	HMA: XARB_TXDTBUF_CRT(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
66	HMA: XARB_TXDTBUF_CRT(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
67	HMA: XARB_TXDTBUF_CRT(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	HMA: XARB_RX_UCK_ERR0(b31 – 24)							
	RXHDBUF RDPT PERR	RXDTBUF ADRERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDTRDADR PERR	RXHDOX PERR	RXDTOX PERR
69	HMA: XARB_RX_UCK_ERR0(b23 – 16)							
	RXNHOX PERR	RXNDOX PERR	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0(b15 – 08)							
	SWTX DT L GPERR	SWTX ENCERR	SWTX HLRC GERR	(RSV)	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	(RSV)
6B	HMA: XARB_RX_UCK_ERR0(b07 – 00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1(b31 – 24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	(RSV)	(RSV)	(RSV)
6D	HMA: XARB_RX_UCK_ERR1(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E	HMA: XARB_RX_UCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	HMA: XARB_RX_UCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (MAIN Blade CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74	HMA: XARB_TX_UCK_ERR0(b31 – 24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW DT GPERR	SWRX SW VLD GERR	SWRX TOCNT GPERR
75	HMA: XARB_TX_UCK_ERR0(b23 – 16)							
	SWRX TOCNT TO	SWRX TX ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	(RSV)	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
76	HMA: XARB_TX_UCK_ERR0(b15 – 08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	TXDTIX PERR	TXNHCNT PERR	SWRX REQOFFERR	SWRX SW HD PERR	DATCNT PERR
77	HMA: XARB_TX_UCK_ERR0(b07 – 00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
78	HMA: XARB_TX_UCK_ERR1(b31 – 24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	(RSV)	(RSV)	(RSV)
79	HMA: XARB_TX_UCK_ERR1(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7A	HMA: XARB_TX_UCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7B	HMA: XARB_TX_UCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8B (DRR CHK2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	Reserved					
10	JCB ID							
11	LDEV#high (Logical DKC#)							
12	LDEV#low (Logical DKC in LDEV#)							
13								
14	CDEV#							
15	RDEV#							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘B’)			
28	Subcode (See following pages)							
29	Detail information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	PK ID					Message code (x‘0’)		
35	SSID of self storage system (low)							
36	Symptom code (x‘FF8B’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	(Reserved)							
3D	Reserved							
3E								
3F								
40	Detail information (See following pages)							
|								
|								
7F								

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail

(1) Byte28 = 00/01/02/03/10/11/12/13

	0	1	2	3	4	5	6	7
28		Subcode (x‘00’) Subcode (x‘01’) Subcode (x‘02’) Subcode (x‘03’) Subcode (x‘10’) Subcode (x‘11’) Subcode (x‘12’) Subcode (x‘13’)			MAIN Blade CHK2 DRR0 Error MAIN Blade CHK2 DRR1 Error MAIN Blade CHK2 DRR2 Error MAIN Blade CHK2 DRR3 Error MAIN Blade CHK2 DRR0 TIMEOUT MAIN Blade CHK2 DRR1 TIMEOUT MAIN Blade CHK2 DRR2 TIMEOUT MAIN Blade CHK2 DRR3 TIMEOUT			
29	HMA: INT_STATUS(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2A	HMA: INT_STATUS(b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
2B	HMA: INT_STATUS(b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
2C	HMA: INT_STATUS(b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B
2D	HMA: INT_STATUS4(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2E	HMA: INT_STATUS4(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2F	HMA: INT_STATUS4(b15 – 08)							
	DRR3 CHK2	DRR2 CHK2	DRR1 CHK2	DRR0 CHK2	(RSV)	(RSV)	DMAMB1 CHK2	DMAMB0 CHK2
30	HMA: INT_STATUS4(b07 – 00)							
	(RSV)	(RSV)	DMA5 CHK2	DMA4 CHK2	DMA3 CHK2	DMA2 CHK2	DMA1 CHK2	DMA0 CHK2
31	HMA: HMA_STATUS(b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM	(RSV)	(RSV)	IX MODE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail

(2) Byte28 = 08/0c/18/1c

	0	1	2	3	4	5	6	7
28		Subcode (x‘08’) Subcode (x‘0c’) Subcode (x‘18’) Subcode (x‘1c’)			MAIN Blade CHK2 I-path0 Error MAIN Blade CHK2 I-path1 Error MAIN Blade CHK2 I-path0 TIMEOUT MAIN Blade CHK2 I-path1 TIMEOUT			
29	HMA: INT_STATUS(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2A	HMA: INT_STATUS(b23 – 16)							
	(RSV)	(RSV)	(RSV)	INT CHK1B	(RSV)	FDMA4 CHK1B	LRP4STOP CHK1B	LRP4 CHK1B
2B	HMA: INT_STATUS(b15 – 08)							
	(RSV)	FDMA3 CHK1B	LRP3STOP CHK1B	LRP3 CHK1B	(RSV)	FDMA2 CHK1B	LRP2STOP CHK1B	LRP2 CHK1B
2C	HMA: INT_STATUS(b07 – 00)							
	(RSV)	FDMA1 CHK1B	LRP1STOP CHK1B	LRP1 CHK1B	(RSV)	FDMA0 CHK1B	LRP0STOP CHK1B	LRP0 CHK1B
2D	HMA: INT_STATUS4(b15 – 08)							
	DRR3 CHK2	DRR2 CHK2	DRR1 CHK2	DRR0 CHK2	(RSV)	(RSV)	DMAMB1 CHK2	DMAMB0 CHK2
2E	HMA: INT_STATUS4(b07 – 00)							
	(RSV)	(RSV)	DMA5 CHK2	DMA4 CHK2	DMA3 CHK2	DMA2 CHK2	DMA1 CHK2	DMA0 CHK2
2F	HMA: INT_STATUS1(b23 – 16)							
	(RSV)	(RSV)	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
30	DRR_NUMBER							
	DRRNUM (7)	DRRNUM (6)	DRRNUM (5)	DRRNUM (4)	DRRNUM (3)	DRRNUM (2)	DRRNUM (1)	DRRNUM (0)
31	HMA: HMA_STATUS(b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM	(RSV)	(RSV)	IX MODE

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/10/11/12/13 (1/4)

	0	1	2	3	4	5	6	7
40	HMA: HMA_STATUS(b31 – 24)							
	(RSV)	MODULE NUM(2)	MODULE NUM(1)	MODULE NUM(0)	CL NUM	(RSV)	(RSV)	IX MODE
41	HMA: HMA_STATUS(b23 – 16)							
	MP CHK CODE(7)	MP CHK CODE(6)	MP CHK CODE(5)	MP CHK CODE(4)	MP CHK CODE(3)	MP CHK CODE(2)	MP CHK CODE(1)	MP CHK CODE(0)
42	HMA: HMA_STATUS(b15 – 08)							
	LSI REV(7)	LSI REV(6)	LSI REV(5)	LSI REV(4)	LSI REV(3)	LSI REV(2)	LSI REV(1)	LSI REV(0)
43	HMA: HMA_STATUS(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44	HMA: DRR_ERR1_ST00(b31 – 24)							
	PRMREG PERR	(RSV)	(RSV)	(RSV)	SQDRCTL HWERR	SQDRCTL XFRTIMPER	SQDRCTL XFRTO	(RSV)
45	HMA: DRR_ERR1_ST00(b23 – 16)							
	STATCNT PERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46	HMA: DRR_ERR1_ST00(b15 – 08)							
	WACNTM CNTPER	WACNTN CNTPER	(RSV)	(RSV)	RACNTMA CNTPER	RACNTMB CNTPER	RACNTNA CNTPER	RACNTNB CNTPER
47	HMA: DRR_ERR1_ST00(b07 – 00)							
	DRBCNTMA PER	DRBCNTMB PER	RDYCNTMA PER	RDYCNTMB PER	CPSCNTMA PER	CPSCNTMB PER	(RSV)	(RSV)
48	HMA: DRR_ERR1_ST01(b31 – 24)							
	SQRXCTL HWERR	SQRXCTL RXTPNT PER	SQRXCTL RXRPNT PER	SQRXCTL TXTIM PERR	SQRXCTL TIMER PERR	SQRXCTL RXTIM PERR	(RSV)	(RSV)
49	HMA: DRR_ERR1_ST01(b23 – 16)							
	RXB CACNT PER	RXB LENCNT PER	RXB SBDAT PER	RXB ACCCNT PER	RXAL CHKRTAG CNTPER	RXAL GENRTAG CNTPER	RXB TRCNT PER	(RSV)
4A	HMA: DRR_ERR1_ST01(b15 – 08)							
	SQ2 HWERR	SQ2 POSCNT0PER	SQ2 POSCNT1PER	SQ2 TWCNTPER	(RSV)	(RSV)	(RSV)	(RSV)
4B	HMA: DRR_ERR1_ST01(b07 – 00)							
	DB2 DEFCNTPER	DB2 RPTPER	DB2 RPTXPER	DB2 WPTPER	DB2 DTPER	DB2 OVW	(RSV)	(RSV)
4C	HMA: DRR_ERR1_ST02(b31 – 24)							
	SQRX0 HWERR	SQRX0 TXTIM PERR	SQRX0 TIMER PERR	SQRX0 RXTIM PERR	SQRX1 HWERR	SQRX1 TXTIM PERR	SQRX1 TIMER PERR	SQRX1 RXTIM PERR
4D	HMA: DRR_ERR1_ST02(b23 – 16)							
	SQRX2 HWERR	SQRX2 TXTIM PERR	SQRX2 TIMER PERR	SQRX2 RXTIM PERR	SQRX3 HWERR	SQRX3 TXTIM PERR	SQRX3 TIMER PERR	SQRX3 RXTIM PERR
4E	HMA: DRR_ERR1_ST02(b15 – 08)							
	SQRX4 HWERR	SQRX4 TXTIM PERR	SQRX4 TIMER PERR	SQRX4 RXTIM PERR	SQRX5 HWERR	SQRX5 TXTIM PERR	SQRX5 TIMER PERR	SQRX5 RXTIM PERR
4F	HMA: DRR_ERR1_ST02(b07 – 00)							
	SQRX6 HWERR	SQRX6 TXTIM PERR	SQRX6 TIMER PERR	SQRX6 RXTIM PERR	SQRX7 HWERR	SQRX7 TXTIM PERR	SQRX7 TIMER PERR	SQRX7 RXTIM PERR

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/10/11/12/13 (2/4)

	0	1	2	3	4	5	6	7
50	HMA: DRR_ERR1_ST03(b31 – 24)							
	SQ3 HWERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
51	HMA: DRR_ERR1_ST03(b23 – 16)							
	DB3M DTPER	DB3M WPTPER	DB3M RPTPER	DB3M DEFCNTPER	DB3M VCNTPER	DB3M VWCNTPER	(RSV)	(RSV)
52	HMA: DRR_ERR1_ST03(b15 – 08)							
	DB3N DTPER	DB3N WPTPER	DB3N RPTPER	DB3N DEFCNTPER	DB3N VCNTPER	DB3N VWCNTPER	(RSV)	(RSV)
53	HMA: DRR_ERR1_ST03(b07 – 00)							
	SQ4M HWERR	SQ4M TWCNTPER	(RSV)	(RSV)	SQ4N HWERR	SQ4N TWCNTPER	(RSV)	(RSV)
54	HMA: DRR_ERR1_ST04(b31 – 24)							
	SQ5MA HWERR	SQ5MA TWCNTPER	(RSV)	DB5MA WPTPER	DB5MA RPTPER	DB5MA DEFCNTD PER	DB5MA DEFCNTR PER	(RSV)
55	HMA: DRR_ERR1_ST04(b23 – 16)							
	SQ5MB HWERR	SQ5MB TWCNTPER	(RSV)	DB5MB WPTPER	DB5MB RPTPER	DB5MB DEFCNTD PER	DB5MB DEFCNTR PER	(RSV)
56	HMA: DRR_ERR1_ST04(b15 – 08)							
	SQ5NA HWERR	SQ5NA TWCNTPER	(RSV)	DB5NA WPTPER	DB5NA RPTPER	DB5NA DEFCNTD PER	DB5NA DEFCNTR PER	(RSV)
57	HMA: DRR_ERR1_ST04(b07 – 00)							
	SQ5NB HWERR	SQ5NB TWCNTPER	(RSV)	DB5NB WPTPER	DB5NB RPTPER	DB5NB DEFCNTD PER	DB5NB DEFCNTR PER	(RSV)
58	HMA: DRR_ERR1_ST05(b31 – 24)							
	SQ6MA HWERR	DB6MA WPTPER	DB6MA RPTPER	DB6MA RPTXPER	DB6MA DEFCNTPER	DB6MA DTPER	DB6MA ECC UNCOR	DB6MA ECC ADRERR
59	HMA: DRR_ERR1_ST05(b23 – 16)							
	SQ6MB HWERR	DB6MB WPTPER	DB6MB RPTPER	DB6MB RPTXPER	DB6MB DEFCNTPER	DB6MB DTPER	DB6MB ECC UNCOR	DB6MB ECC ADRERR
5A	HMA: DRR_ERR1_ST05(b15 – 08)							
	SQ6NA HWERR	DB6NA WPTPER	DB6NA RPTPER	DB6NA RPTXPER	DB6NA DEFCNTPER	DB6NA DTPER	DB6NA ECC UNCOR	DB6NA ECC ADRERR
5B	HMA: DRR_ERR1_ST05(b07 – 00)							
	SQ6NB HWERR	DB6NB WPTPER	DB6NB RPTPER	DB6NB RPTXPER	DB6NB DEFCNTPER	DB6NB DTPER	DB6NB ECC UNCOR	DB6NB ECC ADRERR
5C	HMA: DRR_ERR1_ST06(b31 – 24)							
	SQTXCTL0_ HWERR	SQTXCTL0 PWCNTPER	SQTXCTL0 TXTIM PERR	SQTXCTL0 TIMER PERR	SQTXCTL0 RXTIM PERR	(RSV)	(RSV)	(RSV)
5D	HMA: DRR_ERR1_ST06(b23 – 16)							
	TXB0 CACNTPER	TXB0 LENCNTPER	TXB0 SBDAT PER	TXB0 ACCCNT PER	SQ7A HWERR	SQ7A POSCNT0 PER	SQ7A POSCNT1 PER	SQ7A TWCNTPER
5E	HMA: DRR_ERR1_ST06(b15 – 08)							
	(RSV)	(RSV)	TXAL0 RDYERR	TXAL0 CHKRTAG CNTPER	TXAL0 GENRTAG CNTPER	TXAL0 DEFCNT PER	TXAL0 RPTPER	TXAL0 WPTPER
5F	HMA: DRR_ERR1_ST06(b07 – 00)							
	TXAL0 DTPER	TXAL0 CRCERR	TXAL0 ATAG0ERR CP	TXAL0 ATAG1ERR CP	TXAL0 RTAG0ERR CP	TXAL0 RTAG1ERR CP	TXAL0 RTAG2ERR CP	TXAL0 RTAG3ERR CP

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/10/11/12/13 (3/4)

	0	1	2	3	4	5	6	7
60	HMA: DRR_ERR1_ST07(b31 – 24)							
	SQTXCTL1_ HWERR	SQTXCTL1 PWCNTPER	SQTXCTL1 TXTIM PERR	SQTXCTL1 TIMER PERR	SQTXCTL1 RXTIM PERR	(RSV)	(RSV)	(RSV)
61	HMA: DRR_ERR1_ST07(b23 – 16)							
	TXB1 CACNTPER	TXB1 LENCNTPER	TXB1 SBDAT PER	TXB1 ACCCNT PER	SQ7B HWERR	SQ7B POSCNT0 PER	SQ7B POSCNT1 PER	SQ7B TWCNTPER
62	HMA: DRR_ERR1_ST07(b15 – 08)							
	(RSV)	(RSV)	TXAL1 RDYERR	TXAL1 CHKRTAG CNTPER	TXAL1 GENRTAG CNTPER	TXAL1 DEFCNT PER	TXAL1 RPTPER	TXAL1 WPTPER
63	HMA: DRR_ERR1_ST07(b07 – 00)							
	TXAL1 DTPER	TXAL1 CRCERR	TXAL1 ATAG0ERR CP	TXAL1 ATAG1ERR CP	TXAL1 RTAG0ERR CP	TXAL1 RTAG1ERR CP	TXAL1 RTAG2ERR CP	TXAL1 RTAG3ERR CP
64	HMA: DRR_ERR1_ST08(b31 – 24)							
	SQRX0 TXTO	SQRX0 TIMEOUT	SQRX0 RXTO	SQRX1 TXTO	SQRX1 TIMEOUT	SQRX1 RXTO	SQRX2 TXTO	SQRX2 TIMEOUT
65	HMA: DRR_ERR1_ST08(b23 – 16)							
	SQRX2 RXTO	SQRX3 TXTO	SQRX3 TIMEOUT	SQRX3 RXTO	SQRX4 TXTO	SQRX4 TIMEOUT	SQRX4 RXTO	SQRX5 TXTO
66	HMA: DRR_ERR1_ST08(b15 – 08)							
	SQRX5 TIMEOUT	SQRX5 RXTO	SQRX6 TXTO	SQRX6 TIMEOUT	SQRX6 RXTO	SQRX7 TXTO	SQRX7 TIMEOUT	SQRX7 RXTO
67	HMA: DRR_ERR1_ST08(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	HMA: DRR_ERR1_ST09(b31 – 24)							
	RXB REQID CMPERR	RXB CMPID CMPERR	RXB TAGID ERR	RXB HDRSTSERR	RXB HLRCERR	RXB DLRCERR	RXB SADAT PER	RXB SATX_ERR
69	HMA: DRR_ERR1_ST09(b23 – 16)							
	RXB SBRX_ERR	RXB DASTSERR	RXB ACCCNT CMPERR	RXB VLDOFF ERR	RXB REQOFF ERR	RXB TYPE_ERR	(RSV)	(RSV)
6A	HMA: DRR_ERR1_ST09(b15 – 08)							
	SQRXCTL TXTO	SQRXCTL TIMEOUT	SQRXCTL RXTO	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6B	HMA: DRR_ERR1_ST09(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6C	HMA: DRR_ERR1_ST10(b31 – 24)							
	TXB0_ REQID CMPERR	TXB0 CMPID CMPERR	TXB0 TAGID ERR	TXB0 HDRSTSERR	TXB0 HLRCERR	TXB0 DLRCERR	TXB0 SADAT PER	TXB0 SATX_ERR
6D	HMA: DRR_ERR1_ST10(b23 – 16)							
	TXB0 SBRX_ERR	TXB0 DASTSERR	TXB0 ACCCNT CMPERR	TXB0 VLDOFF ERR	TXB0 REQOFF ERR	TXB0 TYPE_ERR	(RSV)	(RSV)
6E	HMA: DRR_ERR1_ST10(b15 – 08)							
	SQTXCTL0 TXTO	SQTXCTL0 TIMEOUT	SQTXCTL0 RXTO	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	HMA: DRR_ERR1_ST10(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 00/01/02/03/10/11/12/13 (4/4)

	0	1	2	3	4	5	6	7
70	HMA: DRR_ERR1_ST11(b31 – 24)							
	TXB1_ REQID CMPERR	TXB1 CMPID CMPERR	TXB1 TAGID ERR	TXB1 HDRSTSERR	TXB1 HLRCERR	TXB1 DLRCERR	TXB1 SADAT PER	TXB1 SATX_ERR
71	HMA: DRR_ERR1_ST11(b23 – 16)							
	TXB1 SBRX_ERR	TXB1 DASTSERR	TXB1 ACCCNT CMPERR	TXB1 VLDOFF ERR	TXB1 REQOFF ERR	TXB1 TYPE_ERR	(RSV)	(RSV)
72	HMA: DRR_ERR1_ST11(b15 – 08)							
	SQTXCTL1 TXTO	SQTXCTL1 TIMEOUT	SQTXCTL1 RXTO	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	HMA: DRR_ERR1_ST11(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74	HMA: DRR_WARN_ST00(b31 – 24)							
	DB6MA ECC CRCTERR	DB6MB ECC CRCTERR	DB6NA ECC CRCTERR	DB6NB ECC CRCTERR	(RSV)	(RSV)	(RSV)	(RSV)
75	HMA: DRR_WARN_ST00(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	HMA: DRR_WARN_ST00(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77	HMA: DRR_WARN_ST00(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
78	HMA: DRR_CPRM_02(b31 – 24)							
	CURRENT PRM(31)	CURRENT PRM(30)	CURRENT PRM(29)	CURRENT PRM(28)	CURRENT PRM(27)	CURRENT PRM(26)	CURRENT PRM(25)	CURRENT PRM(24)
79	HMA: DRR_CPRM_02(b23 – 16)							
	CURRENT PRM(23)	CURRENT PRM(22)	CURRENT PRM(21)	CURRENT PRM(20)	CURRENT PRM(19)	CURRENT PRM(18)	CURRENT PRM(17)	CURRENT PRM(16)
7A	HMA: DRR_CPRM_02(b15 – 08)							
	CURRENT PRM(15)	CURRENT PRM(14)	CURRENT PRM(13)	CURRENT PRM(12)	CURRENT PRM(11)	CURRENT PRM(10)	CURRENT PRM(9)	CURRENT PRM(8)
7B	HMA: DRR_CPRM_02(b07 – 00)							
	CURRENT PRM7)	CURRENT PRM(6)	CURRENT PRM(5)	CURRENT PRM(4)	CURRENT PRM(3)	CURRENT PRM(2)	CURRENT PRM(1)	CURRENT PRM(0)
7C	HMA: DRR_SORT1(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	HMA: DRR_SORT1(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	HMA: DRR_SORT1(b15 – 08)							
	SQDRCTL CST(7)	SQDRCTL CST(6)	SQDRCTL CST(5)	SQDRCTL CST(4)	SQDRCTL CST(3)	SQDRCTL CST(2)	SQDRCTL CST(1)	SQDRCTL CST(0)
7F	HMA: DRR_SORT1(b07 – 00)							
	SQRXCTL CST(7)	SQRXCTL CST(6)	SQRXCTL CST(5)	SQRXCTL CST(4)	SQRXCTL CST(3)	SQRXCTL CST(2)	SQRXCTL CST(1)	SQRXCTL CST(0)

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (1/4)

	0	1	2	3	4	5	6	7
40	HMA: XARB_RX_PCK_ERR0(b31 – 24)							
	(RSV)	RXSEQ0 QENCERR	RXSEQ0 QPERR	PCI ECC DETECT	RXBLK ECRCERR	(RSV)	RXHDBUF WTPT PERR	(RSV)
41	HMA: XARB_RX_PCK_ERR0(b23 – 16)							
	(RSV)	RXNDBUF WTPT PERR	RXHDIX PERR	RXDTIX PERR	RXDTWT ADR PERR	RXSEQ0 TCNT PERR	RXNHIX PERR	RXNDIX PERR
42	HMA: XARB_RX_PCK_ERR0(b15 – 08)							
	P2C SEQ DECERR	P2C SEQ ENCERR	P2C SEQ PERR	RX PERR	(RSV)	(RSV)	(RSV)	(RSV)
43	HMA: XARB_RX_PCK_ERR0(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44	HMA: XARB_PCI_ECC_RCV(b31 – 24)							
	PCI ECC RCV	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
45	HMA: XARB_PCI_ECC_RCV(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46	HMA: XARB_PCI_ECC_RCV(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47	HMA: XARB_PCI_ECC_RCV(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48	HMA: XARB_TAGXTMR_GPERR(b31 – 24)							
	TAG0TMR GPERR	TAG1TMR GPERR	TAG2TMR GPERR	TAG3TMR GPERR	TAG4TMR GPERR	TAG5TMR GPERR	TAG6TMR GPERR	TAG7TMR GPERR
49	HMA: XARB_TAGXTMR_GPERR(b23 – 16)							
	TAG8TMR GPERR	TAG9TMR GPERR	TAG10TMR GPERR	TAG11TMR GPERR	TAG12TMR GPERR	TAG13TMR GPERR	TAG14TMR GPERR	TAG15TMR GPERR
4A	HMA: XARB_TAGXTMR_GPERR(b15 – 08)							
	TAG16TMR GPERR	TAG17TMR GPERR	TAG18TMR GPERR	TAG19TMR GPERR	TAG20TMR GPERR	TAG21TMR GPERR	TAG22TMR GPERR	TAG23TMR GPERR
4B	HMA: XARB_TAGXTMR_GPERR(b07 – 00)							
	TAG24TMR GPERR	TAG25TMR GPERR	TAG26TMR GPERR	TAG27TMR GPERR	TAG28TMR GPERR	TAG29TMR GPERR	TAG30TMR GPERR	TAG31TMR GPERR
4C	HMA: XARB_TAGXTMR_SEQ_ENCERR(b31 – 24)							
	TAG0TMR SQ EERR	TAG1TMR SQ EERR	TAG2TMR SQ EERR	TAG3TMR SQ EERR	TAG4TMR SQ EERR	TAG5TMR SQ EERR	TAG6TMR SQ EERR	TAG7TMR SQ EERR
4D	HMA: XARB_TAGXTMR_SEQ_ENCERR(b23 – 16)							
	TAG8TMR SQ EERR	TAG9TMR SQ EERR	TAG10TMR SQ EERR	TAG11TMR SQ EERR	TAG12TMR SQ EERR	TAG13TMR SQ EERR	TAG14TMR SQ EERR	TAG15TMR SQ EERR
4E	HMA: XARB_TAGXTMR_SEQ_ENCERR(b15 – 08)							
	TAG16TMR SQ EERR	TAG17TMR SQ EERR	TAG18TMR SQ EERR	TAG19TMR SQ EERR	TAG20TMR SQ EERR	TAG21TMR SQ EERR	TAG22TMR SQ EERR	TAG23TMR SQ EERR
4F	HMA: XARB_TAGXTMR_SEQ_ENCERR(b07 – 00)							
	TAG24TMR SQ EERR	TAG25TMR SQ EERR	TAG26TMR SQ EERR	TAG27TMR SQ EERR	TAG28TMR SQ EERR	TAG29TMR SQ EERR	TAG30TMR SQ EERR	TAG31TMR SQ EERR

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (2/4)

	0	1	2	3	4	5	6	7
50	HMA: XARB_TAGXTMR_SEQ_PERR(b31 – 24)							
	TAG0TMR SQ PERR	TAG1TMR SQ PERR	TAG2TMR SQ PERR	TAG3TMR SQ PERR	TAG4TMR SQ PERR	TAG5TMR SQ PERR	TAG6TMR SQ PERR	TAG7TMR SQ PERR
51	HMA: XARB_TAGXTMR_SEQ_PERR(b23 – 16)							
	TAG8TMR SQ PERR	TAG9TMR SQ PERR	TAG10TMR SQ PERR	TAG11TMR SQ PERR	TAG12TMR SQ PERR	TAG13TMR SQ PERR	TAG14TMR SQ PERR	TAG15TMR SQ PERR
52	HMA: XARB_TAGXTMR_SEQ_PERR(b15 – 08)							
	TAG16TMR SQ PERR	TAG17TMR SQ PERR	TAG18TMR SQ PERR	TAG19TMR SQ PERR	TAG20TMR SQ PERR	TAG21TMR SQ PERR	TAG22TMR SQ PERR	TAG23TMR SQ PERR
53	HMA: XARB_TAGXTMR_SEQ_PERR(b07 – 00)							
	TAG24TMR SQ PERR	TAG25TMR SQ PERR	TAG26TMR SQ PERR	TAG27TMR SQ PERR	TAG28TMR SQ PERR	TAG29TMR SQ PERR	TAG30TMR SQ PERR	TAG31TMR SQ PERR
54	HMA: XARB_TAGXTMR_TOERR(b31 – 24)							
	TAG0TMR TOERR	TAG1TMR TOERR	TAG2TMR TOERR	TAG3TMR TOERR	TAG4TMR TOERR	TAG5TMR TOERR	TAG6TMR TOERR	TAG7TMR TOERR
55	HMA: XARB_TAGXTMR_TOERR(b23 – 16)							
	TAG8TMR TOERR	TAG9TMR TOERR	TAG10TMR TOERR	TAG11TMR TOERR	TAG12TMR TOERR	TAG13TMR TOERR	TAG14TMR TOERR	TAG15TMR TOERR
56	HMA: XARB_TAGXTMR_TOERR(b15 – 08)							
	TAG16TMR TOERR	TAG17TMR TOERR	TAG18TMR TOERR	TAG19TMR TOERR	TAG20TMR TOERR	TAG21TMR TOERR	TAG22TMR TOERR	TAG23TMR TOERR
57	HMA: XARB_TAGXTMR_TOERR(b07 – 00)							
	TAG24TMR TOERR	TAG25TMR TOERR	TAG26TMR TOERR	TAG27TMR TOERR	TAG28TMR TOERR	TAG29TMR TOERR	TAG30TMR TOERR	TAG31TMR TOERR
58	HMA: XARB_RSV(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	HMA: XARB_RSV(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	HMA: XARB_RSV(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	HMA: XARB_RSV(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	HMA: XARB_TX_PCK_ERR0(b31 – 24)							
	TXHD RDPT PERR	TXNH RDPT PERR	TXNH WTPT PERR	TXND RDPT PERR	BETY ERR	CDETY ERR	CHETY ERR	NDETY ERR
5D	HMA: XARB_TX_PCK_ERR0(b23 – 16)							
	NHETY FRCERR	PDETY FRCERR	PHETY FRCERR	QETY FRCERR	LINKERR	TXSEQ0 QEERR	TXSEQ0 QPERR	P2C SEQ DERR
5E	HMA: XARB_TX_PCK_ERR0(b15 – 08)							
	P2C SEQ EERR	P2C SEQ PERR	TXDT RDADR PERR	P2C CNT PERR	TXHDOX PERR	TXDTOX PERR	TXNHIX PERR	TXNHOX PERR
5F	HMA: XARB_TX_PCK_ERR0(b07 – 00)							
	LINKERR	TXNDBUF WTPT PERR	STOPREQ PERR	TXERR GPERR	TXSEQ0 TCNT PERR	(RSV)	XFBCNT GPERR	XFQCNT PERR

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (3/4)

	0	1	2	3	4	5	6	7
60	HMA: XARB_TX_PCK_ERR1(b31 – 24)							
	ICNT FRCPERR	TXHDDT AFRCPERR	TXHDDT EFRCPERR	(RSV)	ICNT NPFRCPERR	NPHDBUF FRCPERR	TXDTBUF FRCPERR	TXNDBUF FRCPERR
61	HMA: XARB_TX_PCK_ERR1(b23 – 16)							
	CHCNT FRCERR	NHCNT FRCERR	PHCNT FRCERR	CDCNT FRCERR	NDCNT FRCERR	PDCNT FRCERR	(RSV)	(RSV)
62	HMA: XARB_TX_PCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	HMA: XARB_TX_PCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	HMA: XARB_TXDTBUF_CRT(b31 – 24)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65	HMA: XARB_TXDTBUF_CRT(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
66	HMA: XARB_TXDTBUF_CRT(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
67	HMA: XARB_TXDTBUF_CRT(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	HMA: XARB_RX_UCK_ERR0(b31 – 24)							
	RXHDBUF RDPT PERR	RXDTBUF ADRERR	RXDTBUF UNCOR	RXNHBUF RDPT PERR	RXNDBUF RDPT PERR	RXDTRDADR PERR	RXHDOX PERR	RXDTOX PERR
69	HMA: XARB_RX_UCK_ERR0(b23 – 16)							
	RXNHOX PERR	RXNDOX PERR	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR	C2P CNT PERR	SWTX DECERR	SWTX DLRC GERR
6A	HMA: XARB_RX_UCK_ERR0(b15 – 08)							
	SWTX DT L GPERR	SWTX ENCERR	SWTX HLRC GERR	(RSV)	SWTX TOCNT GPERR	SWTX TOCNT TO	SWTX WDCNT GPERR	(RSV)
6B	HMA: XARB_RX_UCK_ERR0(b07 – 00)							
	ARBSEQ QDECERR	ARBSEQ QENCERR	ARBSEQ QPERR	RXNHBUF WTPT PERR	MRG ECC ADRERR	MRG ECC UNCOR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
6C	HMA: XARB_RX_UCK_ERR1(b31 – 24)							
	MRGBUF DTCNT PERR	MRGBUF TMR PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	(RSV)	(RSV)	(RSV)
6D	HMA: XARB_RX_UCK_ERR1(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E	HMA: XARB_RX_UCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	HMA: XARB_RX_UCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(2) Byte28 = 08/0c/18/1c (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74	HMA: XARB_TX_UCK_ERR0(b31 – 24)							
	SWRX DECERR	SWRX DLRCTIM GERR	SWRX DLRC GERR	SWRX ENCERR	SWRX HLRC GERR	SWRX SW DT GPERR	SWRX SW VLD GERR	SWRX TOCNT GPERR
75	HMA: XARB_TX_UCK_ERR0(b23 – 16)							
	SWRX TOCNT TO	SWRX TX ERR GERR	SWRX WDCNT GPERR	TXHDBUF WTPT PERR	(RSV)	C2P SEQ DECERR	C2P SEQ ENCERR	C2P SEQ PERR
76	HMA: XARB_TX_UCK_ERR0(b15 – 08)							
	C2P CNT PERR	TXDTBUF WTADR PERR	TXHDIX PERR	TXDTIX PERR	TXNHCNT PERR	SWRX REQOFFERR	SWRX SW HD PERR	DATCNT PERR
77	HMA: XARB_TX_UCK_ERR0(b07 – 00)							
	DIV ECC ADRERR	DIV ECC CRCTERR	DIV ECC UNCOR	CPLSEQ QDECERR	CPLSEQ QENCERR	CPLSEQ QPERR	MRGBUF WTADR PERR	MRGBUF RDADR PERR
78	HMA: XARB_TX_UCK_ERR1(b31 – 24)							
	CDICNT PERR	CPLSEQ DTCNT PERR	XFCNT GPERR	TKCNT1 PERR	TKCNT2 PERR	(RSV)	(RSV)	(RSV)
79	HMA: XARB_TX_UCK_ERR1(b23 – 16)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7A	HMA: XARB_TX_UCK_ERR1(b15 – 08)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7B	HMA: XARB_TX_UCK_ERR1(b07 – 00)							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8C (SVP Detected Failure : SVP(PC)) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘C’)			
28								
29	Error information (Details will be published separately)							
2A								
2B								
2C								
2D								
2E								
2F								
30	Failure type code (*1)							
31								
32								
33	Error information (Details will be published separately)							
34								
35								
36	Symptom code (x‘FF8C’)							
37								
38	Log and message congtrol (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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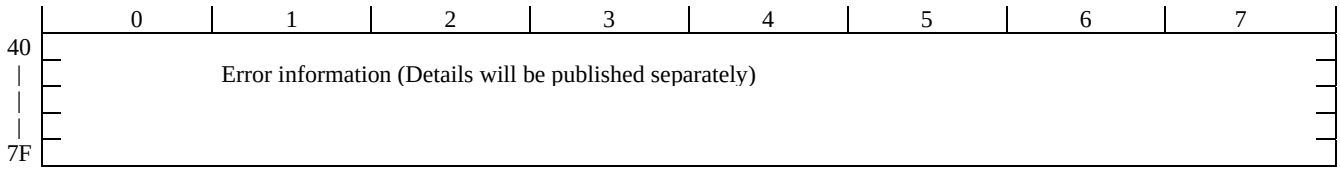
Byte27 = 8C (SVP Detected Failure : SVP(PC)) (2/2)



*1: Failure type code

- x‘0000’ : Logical Inconsist
- x‘0001’ : Windows memory allocate failure
- x‘0002’ : File
- x‘0003’ : LAN failure
- x‘0005’ : Windows failure
- x‘0006’ : CUDG detected failure
- x‘0009’ : BOOT detected failure
- x‘000A’ : SVP forced reboot or maintenance failure
- x‘000B’ : Router failure
- x‘000C’ : Disable SVP reboot
- x‘000D’ : Stop SSB overwrite
- x‘000E’ : Stop SSBS overwrite
- x‘000F’ : Flash failure
- x‘0015’ : Battery failure
- x‘0030’ : Delay of time
- x‘0031’ : Warning of a stack
- x‘0032’ : Single task error
- x‘0033’ : SVP launcher error
- x‘0034’ : SVP reboot
- x‘0035’ : SVP reboot (WSAENOBUF)
- x‘0039’ : IP address setting error
- x‘003A’ : Subnet mask setting error
- x‘003B’ : Virus detection error
- x‘003C’ : Virus detection error
- x‘003D’ : Virus detection error
- x‘003E’ : SVP environment error
- x‘003F’ : Situation observation error
- x‘0040’ : Dummy PS/OFF starting (normal)

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Byte27 = 8C (SVP Detected Failure : SVP(PC)) error information detailed

(1) Logical inconsistency / HEAP / File / LAN / Windows failure /
SVP forced reboot or maintenance failure / Router failure / Disable SVP reboot /
Stop SSB overwrite / Stop SSBS overwrite / Flash memory failure / Battery failure / Delay of time /
Warning of a stack / Single task error / SVP launcher error / SVP reboot /
SVP reboot (WSAENOBUF) / IP address setting error / Subnet mask setting error /
Virus detection error / SVP environment error / Situation observation error /
Dummy PS/OFF starting (normal)

	0	1	2	3	4	5	6	7
28	Failed AP code (*1)							
29								
2A	Reserved							
2F								
30	Error type code (*2)							
31								
32	Error code							
35								

40	Failed Window class (ASCII code: 8characters)
47	
48	Failed function name (ASCII code: 24characters)
5F	
60	Failed line number
61	
62	Error code
65	
66	Reserved
7F	

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*1: Failed AP Code

- x‘0000’ : Dump task
- x‘0001’ : HDD inline
- x‘0002’ : Microprogram change (Online)
- x‘0003’ : Information
- x‘0004’ : LOGOUT
- x‘0005’ : PATH inline
- x‘0006’ : Back Ground
- x‘0007’ : DIAG
- x‘0008’ : Install
- x‘0009’ : Online
- x‘000A’ : Micro-program change (Offline)
- x‘000B’ : Special package change
- x‘000C’ : Common function for communication
- x‘00FF’ : Others

*2: Error type code

- x‘0000’ : Logical inconsistency
- x‘0001’ : Windows memory allocate failure
- x‘0002’ : File
- x‘0003’ : LAN failure
- x‘0005’ : Windows failure
- x‘000A’ : SVP forced reboot or maintenance failure
- x‘000B’ : Router failure
- x‘000C’ : Disable SVP reboot
- x‘000D’ : Stop SSB overwrite
- x‘000E’ : Stop SSBS overwrite
- x‘000F’ : Flash failure
- x‘0015’ : Battery failure
- x‘0030’ : Delay of time
- x‘0031’ : Warning of a stack
- x‘0032’ : Single task error
- x‘0033’ : SVP launcher error
- x‘0034’ : SVP reboot
- x‘0035’ : SVP reboot (WSAENOBUF)
- x‘0039’ : IP address setting error
- x‘003A’ : Subnet mask setting error
- x‘003B’ : Virus detection error
- x‘003C’ : Virus detection error
- x‘003D’ : Virus detection error
- x‘003E’ : SVP environment error
- x‘003F’ : Situation observation error
- x‘0040’ : Dummy PS/OFF starting (normal)

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Byte27 = 8C (SVP Detected Failure : SVP(PC)) error information detailed

(2) CUDG detected error

	0	1	2	3	4	5	6	7
28								
29		‘CUDG ERR’ (x‘43 55 44 47 20 45 52 52’)						
2A								
2B								
2C								
2D								
2E								
2F								
30		Error type code (x‘0006’ : CUDG detection						
31								
32								
33		Error code (x‘00000000’)						
34								
35								

40	Error occurred time (year)
41	Error occurred time (month)
42	Error occurred time (day)
43	Error occurred time (hour)
44	Error occurred time (minute)
45	Error occurred time (second)
46	Report MPID
47	Test object
48	Test type (x‘01’ : CUDG3)
49	Not used
4A	Test contents
4B	Test contents
4C	Error code
4D	Error code
4E	Not used
4F	Not used
50	Cache Module Group No. (slave 1)
51	Cache Module Group No. (slave 1)
52	Cache Module Group No. (slave 1)
53	Cache Module Group No. (slave 1)
54	Cache Module Group No. (slave 2)
55	Cache Module Group No. (slave 2)
56	Cache Module Group No. (slave 2)
57	Cache Module Group No. (slave 2)
58	PCB Location (Main Platter)
59	PCB Location (Main Platter)
5A	PCB Location (Main Platter)
5B	PCB Location (Cache Platter 1)
5C	PCB Location (Cache Platter 1)
5D	PCB Location (Cache Platter 2)
5E	PCB Location (Cache Platter 2)
5F	RUN Option
60	Additional information (32Byte)
|	
7F	

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Byte27 = 8C (SVP Detected Failure : SVP(PC)) error information detailed

(3) BOOT detected error

	0	1	2	3	4	5	6	7
28								
29	‘BOOT ERR’ (x‘42 4F 4F 54 20 45 52 52’)							
2A								
2B								
2C								
2D								
2E								
2F								
30	Error type code (x‘0009’ : BOOT detected error)							
31								
32								
33	Error code (x‘00000000’ X:Processor number)							
34								
35								
40	Error detection point							
|								
4F								
50	Reserved							
51								
52								
53								
54	Error code for loading error							
55								
56								
57								
58	Erro code of initial setting individual function							
59								
5A								
5B								
5C	Error code of initialization function (*1)							
5D								
5E								
5F								
60	Reserved							
|								
7F								

*1: Error code of initialization function.

x‘31000041’ : Forcible start with CE mode switches.

x‘48000041’ : This MP has the micro-programs which type is different from the PCB name. (In the MP-Install procedure, the package may have been set which type is different from one that is specified in the define configuration.)

x‘56000041’ : Sum check error of the load module. (SVP Failure occurred)

others : Loading for the load module impossible. (The load module was incorrect)

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Byte27 = 8E (CHK1)
Byte27 = 8E (CHK1) Byte28-31 Detail

(1) Byte28 = 20

	0	1	2	3	4	5	6	7
28	Subcode (x‘20’)							
29	MP_Number							
	MP_Number							
2A	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2B	IA32_MC9_STATUS B0							
	MCA ErCode 07	MCA ErCode 06	MCA ErCode 05	MCA ErCode 04	MCA ErCode 03	MCA ErCode 02	MCA ErCode 01	MCA ErCode 00
2C	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2D	IA32_MC10_STATUS B0							
	MCA ErCode 07	MCA ErCode 06	MCA ErCode 05	MCA ErCode 04	MCA ErCode 03	MCA ErCode 02	MCA ErCode 01	MCA ErCode 00
2E								
	0	0	0	0	0	0	0	0
2F								
	0	0	0	0	0	0	0	0
30								
	0	0	0	0	0	0	0	0
31								
	0	0	0	0	0	0	0	0

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Byte27 = 8E (CHK1) Byte28-31 Detail

(2) Byte28 = 21

	0	1	2	3	4	5	6	7
28	Subcode (x‘21’)							
29	MP_Number							
	MP_Number							
2A	IA32_MC4_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2B	IA32_MC5_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2C	IA32_MC6_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2D	IA32_MC11_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2E	GFERRST:B3							
	GFER _31	GFER _30	GFER _29	GFER _28	GFER _27	GFER _26	GFER _25	GFER _24
2F	GFERRST:B2							
	GFER _23	GFER _22	GFER _21	GFER _20	GFER _19	GFER _18	GFER _17	GFER _16
30	GFERRST:B1							
	GFER _15	GFER _14	GFER _13	GFER _12	GFER _11	GFER _10	GFER _09	GFER _08
31	GFERRST:B0							
	GFER _07	GFER _06	GFER _05	GFER _04	GFER _03	GFER _02	GFER _01	GFER _00

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Byte27 = 8E (CHK1) Byte28-31 Detail

(3) Byte28 = 22/23/24/25

	0	1	2	3	4	5	6	7
28	Subcode (x‘22’ or x‘23’ or x‘24’ or x‘25’)							
29	MP_Number							
	MP_Number							
2A	NMI_STAT1							
	NMI STAT 17	NMI STAT 16	NMI STAT 15	NMI STAT 14	NMI STAT 13	NMI STAT 12	NMI STAT 11	NMI STAT 10
2B	NMI_STAT0							
	NMI STAT 07	NMI STAT 06	NMI STAT 05	NMI STAT 04	NMI STAT 03	NMI STAT 02	NMI STAT 01	NMI STAT 00
2C	OTHER_ISTAT1							
	OTHER_ ISTAT17	OTHER_ ISTAT16	OTHER_ ISTAT15	OTHER_ ISTAT14	OTHER_ ISTAT13	OTHER_ ISTAT12	OTHER_ ISTAT11	OTHER_ ISTAT10
2D	OTHER_ISTAT0							
	OTHER_ ISTAT07	OTHER_ ISTAT06	OTHER_ ISTAT05	OTHER_ ISTAT04	OTHER_ ISTAT03	OTHER_ ISTAT02	OTHER_ ISTAT01	OTHER_ ISTAT00
2E	GFERRST:B3							
	GFER _31	GFER _30	GFER _29	GFER _28	GFER _27	GFER _26	GFER _25	GFER _31
2F	GFERRST:B2							
	GFER _23	GFER _22	GFER _21	GFER _20	GFER _19	GFER _18	GFER _17	GFER _23
30	GFERRST:B1							
	GFER _15	GFER _14	GFER _13	GFER _12	GFER _11	GFER _10	GFER _09	GFER _15
31	GFERRST:B0							
	GFER _07	GFER _06	GFER _05	GFER _04	GFER _03	GFER _02	GFER _01	GFER _07

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Byte27 = 8E (CHK1) Byte28-31 Detail

(4) Byte28 = 30

	0	1	2	3	4	5	6	7
28	Subcode (x‘30’)							
29	MP_Number							
	MP_Number							
2A	GFERRST:B3							
	GFER_31	GFER_30	GFER_29	GFER_28	GFER_27	GFER_26	GFER_25	GFER_24
2B	GFERRST:B2							
	GFER_23	GFER_22	GFER_21	GFER_20	GFER_19	GFER_18	GFER_17	GFER_16
2C	GFERRST:B1							
	GFER_15	GFER_14	GFER_13	GFER_12	GFER_11	GFER_10	GFER_09	GFER_08
2D	GFERRST:B0							
	GFER_07	GFER_06	GFER_05	GFER_04	GFER_03	GFER_02	GFER_01	GFER_00
2E	GNERRST:B3							
	GNER_31	GNER_30	GNER_29	GNER_28	GNER_27	GNER_26	GNER_25	GNER_24
2F	GNERRST:B2							
	GNER_23	GNER_22	GNER_21	GNER_20	GNER_19	GNER_18	GNER_17	GNER_16
30	GNERRST:B1							
	GNER_15	GNER_14	GNER_13	GNER_12	GNER_11	GNER_10	GNER_09	GNER_08
31	GNERRST:B0							
	GNER_07	GNER_06	GNER_05	GNER_04	GNER_03	GNER_02	GNER_01	GNER_00

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Byte27 = 8E (CHK1) Byte28-31 Detail

(5) Byte28 = 40

	0	1	2	3	4	5	6	7
28	Subcode (x‘40’)							
29	MP_Number							
	MP_Number							
2A	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2B	IA32_MC9_STATUS B0							
	MCA ErCode 07	MCA ErCode 06	MCA ErCode 05	MCA ErCode 04	MCA ErCode 03	MCA ErCode 02	MCA ErCode 01	MCA ErCode 00
2C	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
2D	IA32_MC10_STATUS B0							
	MCA ErCode 07	MCA ErCode 06	MCA ErCode 05	MCA ErCode 04	MCA ErCode 03	MCA ErCode 02	MCA ErCode 01	MCA ErCode 00
2E								
	0	0	0	0	0	0	0	0
2F								
	0	0	0	0	0	0	0	0
30								
	0	0	0	0	0	0	0	0
31								
	0	0	0	0	0	0	0	0

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Byte27 = 8E (CHK1) Byte28-31 Detail

(6) Byte28 = 41/42/43

	0	1	2	3	4	5	6	7
28	Subcode (x‘41’ or x‘42’ or x‘43’)							
29	MP_Number							
	MP_Number							
2A	INT0_ISTAT1							
	I STATE 17	I STATE 16	I STATE 15	I STATE 14	I STATE 13	I STATE 12	I STATE 11	I STATE 10
2B	INT0_ISTAT0							
	I STATE 07	I STATE 06	I STATE 05	I STATE 04	I STATE 03	I STATE 02	I STATE 01	I STATE 00
2C								
	0	0	0	0	0	0	0	0
2D								
	0	0	0	0	0	0	0	0
2E	GNERRST:B3							
	GNER_31	GNER_30	GNER_29	GNER_28	GNER_27	GNER_26	GNER_25	GNER_24
2F	GNERRST:B2							
	GNER_23	GNER_22	GNER_21	GNER_20	GNER_19	GNER_18	GNER_17	GNER_16
30	GNERRST:B1							
	GNER_15	GNER_14	GNER_13	GNER_12	GNER_11	GNER_10	GNER_09	GNER_08
31	GNERRST:B0							
	GNER_07	GNER_06	GNER_05	GNER_04	GNER_03	GNER_02	GNER_01	GNER_00

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Byte27 = 8E (CHK1) Byte28-31 Detail

(7) Byte28 = 44/45

	0	1	2	3	4	5	6	7
28	Subcode (x‘44’ or x‘45’)							
29	MP_Number							
	MP_Number							
2A	INT0_ISTAT1							
	I STATE 17	I STATE 16	I STATE 15	I STATE 14	I STATE 13	I STATE 12	I STATE 11	I STATE 10
2B	INT0_ISTAT0							
	I STATE 07	I STATE 06	I STATE 05	I STATE 04	I STATE 03	I STATE 02	I STATE 01	I STATE 00
2C	IA32 THERM STATUS							
	Therm Thres 1 Log	Therm Thres 1 Status	Out of Spec Status_Log	Out of Spec Status	PROC# or FRCEPR# Log	PROC# or FRCEPR# Event	Thermal _Status Log	Thermal _Status
2D	ESR							
	Illegal Reg Adr	Recved Ilegal Vector	Send Ilegal Vector	Reserved	Receive Acpt Error	Send Acpt Error	Receive Chk SUM Error	Send Chk SUM Error
2E	GNERRST:B3							
	GNER _31	GNER _30	GNER _29	GNER _28	GNER _27	GNER _26	GNER _25	GNER _24
2F	GNERRST:B2							
	GNER _23	GNER _22	GNER _21	GNER _20	GNER _19	GNER _18	GNER _17	GNER _16
30	GNERRST:B1							
	GNER _15	GNER _14	GNER _13	GNER _12	GNER _11	GNER _10	GNER _09	GNER _08
31	GNERRST:B0							
	GNER _07	GNER _06	GNER _05	GNER _04	GNER _03	GNER _02	GNER _01	GNER _00

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Byte27 = 8E (CHK1) Byte28-31 Detail

(8) Byte28 = 47

	0	1	2	3	4	5	6	7
28	Subcode (x‘47’)							
29	MP_Number							
	MP_Number							
2A								
	0	0	0	0	0	0	0	0
2B	P5_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BANDWIDTH CHANGED
2C	P5_PEXLNKSTS:B1							
	BANDWIDTH STATUS	BW MNG STATUS	LINK ACTIVE	SCCON	LNKTRG	Reserved	NLNKWD 5	NLNKWD 4
2D	P5_PEXLNKSTS:B0							
	NLNKWD 3	NLNKWD 2	NLNKWD 1	NLNKWD 0	LNKSPD 3	LNKSPD 2	LNKSPD 1	LNKSPD 0
2E								
	0	0	0	0	0	0	0	0
2F	P6_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BANDWIDTH CHANGED
30	P6_PEXLNKSTS:B1							
	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1	P6_PEXLNK STS:B1
31	P6_PEXLNKSTS:B0							
	NLNKWD 3	NLNKWD 2	NLNKWD 1	NLNKWD 0	LNKSPD 3	LNKSPD 2	LNKSPD 1	LNKSPD 0

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Byte27 = 8E (CHK1) Byte28-31 Detail

(9) Byte28 = 50/51/52

	0	1	2	3	4	5	6	7
28	Subcode (x‘50’ or x‘51’ or x‘52’)							
29	MP_Number							
	MP_Number							
2A	INT0_ISTAT1							
	I STATE 17	I STATE 16	I STATE 15	I STATE 14	I STATE 13	I STATE 12	I STATE 11	I STATE 10
2B	INT0_ISTAT0							
	I STATE 07	I STATE 06	I STATE 05	I STATE 04	I STATE 03	I STATE 02	I STATE 01	I STATE 00
2C	INT0_MSISTAT							
	C0_IRR	C0_MSICNT 6	C0_MSICNT 5	C0_MSICNT 4	C0_MSICNT 3	C0_MSICNT 2	C0_MSICNT 1	C0_MSICNT 0
2D								
	0	0	0	0	0	0	0	0
2E	GNERRST:B3							
	GNER _31	GNER _30	GNER _29	GNER _28	GNER _27	GNER _26	GNER _25	GNER _24
2F	GNERRST:B2							
	GNER _23	GNER _22	GNER _21	GNER _20	GNER _19	GNER _18	GNER _17	GNER _16
30	GNERRST:B1							
	GNER _15	GNER _14	GNER _13	GNER _12	GNER _11	GNER _10	GNER _09	GNER _08
31	GNERRST:B0							
	GNER _07	GNER _06	GNER _05	GNER _04	GNER _03	GNER _02	GNER _01	GNER _00

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Byte27 = 8E (CHK1) Byte28-31 Detail

(10) Byte28 = 60/61/62/63/64/65/66/67/68

	0	1	2	3	4	5	6	7
28	Subcode (x‘60’ or x‘61’ or x‘62’ or x‘63’ or x‘64’ or x‘65’ or x‘66’ or x‘67’ or x‘68’)							
29	INT0_HMA_STATUS B3							
	Not used	Module number			CL Number	Not used	Not used	IX Mode
2A	INT0_HMA_STATUS B1							
	LSI Revision							
2B	LRP_HMA_INFO_TABLE00 B2							
	Not used	Not used	P5 path STATUS	P4 path STATUS	P3 path STATUS	P2 path STATUS	P1 path STATUS	P0 path STATUS
2C	LRP_HMA_INFO_TABLE00 B1							
	CM13 STATUS	CM03 STATUS	CM12 STATUS	CM02 STATUS	CM11 STATUS	CM01 STATUS	CM10 STATUS	CM00 STATUS
2D	LRP_HMA_INFO_TABLE00 B0							
	E1 path STATUS	E0 path STATUS	I1 path STATUS	I0 path STATUS	Not used	Not used	Not used	PON HMA STATUS
2E	INT0_INTSTS0 B3							
	INT CHK1B	LRP4 CHK1B	LRP3-0 CHK1B	SWIF CHK1B	BARB CHK1B	IARB CHK1B	EARB CHK1B	IXARB CHK1B
2F	INT0_INTSTS0 B2							
	PARB CHK1B	XD CHK1B	DXC CHK1B	DXA CHK1B	DRR CHK1B	MPDMA DMAMB CHK1B	DMA CHK1B	RGA CHK1B
30	INT0_INTSTS0 B1							
	FMT CHK1B	BRAM BCOM SH CHK1B	SMC CHK1B	SMBUS CHK1B	CHK4	CHK3	CHK2	WARN
31	INT0_INTSTS0 B0							
	Not used	Not used	MBOX INT	LRP4 INT	LRP3 INT	LRP2 INT	LRP1 INT	LRP0 INT

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Byte27 = 8E (CHK1) Byte28-31 Detail

(11) Byte28 = 80/81

	0	1	2	3	4	5	6	7
28	Subcode (x‘80’ or x‘81’)							
29	MP_Number							
	MP_Number							
2A								
	0	0	0	0	0	0	0	0
2B								
	0	0	0	0	0	0	0	0
2C								
	0	0	0	0	0	0	0	0
2D	Error MCE No.							
2E	IA32 MCi STATUS:B7							
	STATUS _31	STATUS _30	STATUS _29	STATUS _28	STATUS _27	STATUS _26	STATUS _25	STATUS _24
2F	IA32 MCi STATUS:B6							
	STATUS _31	STATUS _30	STATUS _29	STATUS _28	STATUS _27	STATUS _26	STATUS _25	STATUS _24
30	IA32 MCi STATUS:B1							
	STATUS _31	STATUS _30	STATUS _29	STATUS _28	STATUS _27	STATUS _26	STATUS _25	STATUS _24
31	IA32 MCi STATUS:B0							
	STATUS _31	STATUS _30	STATUS _29	STATUS _28	STATUS _27	STATUS _26	STATUS _25	STATUS _24

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Byte27 = 8E (CHK1) Byte40-7F Detail

(1) Byte28 = 20/40 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	'01'							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	GFERRST:B3							
	GFER _31	GFER _30	GFER _29	GFER _28	GFER _27	GFER _26	GFER _25	GFER _24
45	GFERRST:B2							
	GFER _23	GFER _22	GFER _21	GFER _20	GFER _19	GFER _18	GFER _17	GFER _16
46	GFERRST:B1							
	GFER _15	GFER _14	GFER _13	GFER _12	GFER _11	GFER _10	GFER _09	GFER _08
47	GFERRST:B0							
	GFER _07	GFER _06	GFER _05	GFER _04	GFER _03	GFER _02	GFER _01	GFER _00
48	GNERRST:B3							
	GNER _31	GNER _30	GNER _29	GNER _28	GNER _27	GNER _26	GNER _25	GNER _24
49	GNERRST:B2							
	GNER _23	GNER _22	GNER _21	GNER _20	GNER _19	GNER _18	GNER _17	GNER _16
4A	GNERRST:B1							
	GNER _15	GNER _14	GNER _13	GNER _12	GNER _11	GNER _10	GNER _09	GNER _08
4B	GNERRST:B0							
	GNER _07	GNER _06	GNER _05	GNER _04	GNER _03	GNER _02	GNER _01	GNER _00
4C	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4D	IA32_MC9_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
4E	IA32_MC9_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
4F	IA32_MC9_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
50	IA32_MC9_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
51	IA32_MC9_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
52	IA32_MC9_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
53	IA32_MC9_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(1) Byte28 = 20/40 (2/3)

	0	1	2	3	4	5	6	7
54	IA32_MC9_ADDR B7							
	0	0	0	0	0	0	0	0
55	IA32_MC9_ADDR B6							
	0	0	0	0	0	0	0	0
56	IA32_MC9_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
57	IA32_MC9_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
58	IA32_MC9_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
59	IA32_MC9_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
5A	IA32_MC9_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
5B	IA32_MC9_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0
5C	IA32_MC9_MISK B7							
	Info 54	Info 53	Info 52	Info 51	Info 50	Info 49	Info 48	Info 47
5D	IA32_MC9_MISK B6							
	Info 46	Info 45	Info 44	Info 43	Info 42	Info 41	Info 40	Info 39
5E	IA32_MC9_MISK B5							
	Info 38	Info 37	Info 36	Info 35	Info 34	Info 33	Info 32	Info 31
5F	IA32_MC9_MISK B4							
	Info 30	Info 29	Info 28	Info 27	Info 26	Info 25	Info 24	Info 23
60	IA32_MC9_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
61	IA32_MC9_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
62	IA32_MC9_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
63	IA32_MC9_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0
64	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
65	IA32_MC10_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
66	IA32_MC10_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
67	IA32_MC10_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
68	IA32_MC10_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
69	IA32_MC10_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
6A	IA32_MC10_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
6B	IA32_MC10_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(1) Byte28 = 20/40 (3/3)

	0	1	2	3	4	5	6	7
6C	IA32_MC10_ADDR B7							
	0	0	0	0	0	0	0	0
6D	IA32_MC10_ADDR B6							
	0	0	0	0	0	0	0	0
6E	IA32_MC10_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
6F	IA32_MC10_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
70	IA32_MC10_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
71	IA32_MC10_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
72	IA32_MC10_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
73	IA32_MC10_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0
74	IA32_MC10_MISK B7							
	Info 54	Info 53	Info 52	Info 51	Info 50	Info 49	Info 48	Info 47
75	IA32_MC10_MISK B6							
	Info 46	Info 45	Info 44	Info 43	Info 42	Info 41	Info 40	Info 39
76	IA32_MC10_MISK B5							
	Info 38	Info 37	Info 36	Info 35	Info 34	Info 33	Info 32	Info 31
77	IA32_MC10_MISK B4							
	Info 30	Info 29	Info 28	Info 27	Info 26	Info 25	Info 24	Info 23
78	IA32_MC10_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
79	IA32_MC10_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
7A	IA32_MC10_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
7B	IA32_MC10_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 8E (CHK1) Byte40-7F Detail

(2) Byte28 = 21 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘02’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	IA32_MC4_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
45	IA32_MC4_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
46	IA32_MC4_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
47	IA32_MC4_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
48	IA32_MC5_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
49	IA32_MC5_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
4A	IA32_MC5_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
4B	IA32_MC5_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
4C	IA32_MC5_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
4D	IA32_MC5_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
4E	IA32_MC5_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
4F	IA32_MC5_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
50	IA32_MC5_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
51	IA32_MC5_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
52	IA32_MC5_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
53	IA32_MC5_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
54	IA32_MC5_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(2) Byte28 = 21 (2/3)

	0	1	2	3	4	5	6	7
55	IA32_MC5_MISK B4							
	Info 30	Info 29	Info 28	Info 27	Info 26	Info 25	Info 24	Info 23
56	IA32_MC5_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
57	IA32_MC5_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
58	IA32_MC5_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
59	IA32_MC5_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0
5A	IA32_MC6_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
5B	IA32_MC6_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
5C	IA32_MC6_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
5D	IA32_MC6_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
5E	IA32_MC6_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
5F	IA32_MC6_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
60	IA32_MC6_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
61	IA32_MC6_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
62	IA32_MC6_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
63	IA32_MC6_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
64	IA32_MC6_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
65	IA32_MC6_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
66	IA32_MC6_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0
67	IA32_MC6_MISK B7							
	Info 54	Info 53	Info 52	Info 51	Info 50	Info 49	Info 48	Info 47
68	IA32_MC6_MISK B6							
	Info 46	Info 45	Info 44	Info 43	Info 42	Info 41	Info 40	Info 39
69	IA32_MC6_MISK B5							
	Info 38	Info 37	Info 36	Info 35	Info 34	Info 33	Info 32	Info 31
6A	IA32_MC6_MISK B4							
	Info 30	Info 29	Info 28	Info 27	Info 26	Info 25	Info 24	Info 23

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Byte27 = 8E (CHK1) Byte40-7F Detail

(2) Byte28 = 21 (3/3)

	0	1	2	3	4	5	6	7
6B	IA32_MC6_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
6C	IA32_MC6_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
6D	IA32_MC6_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
6E	IA32_MC6_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0
6F	IA32_MC11_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
70	IA32_MC11_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
71	IA32_MC11_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
72	IA32_MC11_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
73	IA32_MC11_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
74	IA32_MC11_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
75	IA32_MC11_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
76	IA32_MC11_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
77	IA32_MC11_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
78	IA32_MC11_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
79	IA32_MC11_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
7A	IA32_MC11_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
7B	IA32_MC11_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0
7C	IA32_MC11_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
7D	IA32_MC11_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
7E	IA32_MC11_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
7F	IA32_MC11_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(3) Byte28 = 22/23/24/25 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘03’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	PLDERR0							
	PLDERR _ 07	PLDERR _ 06	PLDERR _ 05	PLDERR _ 04	PLDERR _ 03	PLDERR _ 02	PLDERR _ 01	PLDERR _ 00
45	PLDERR1							
	PLDERR _ 17	PLDERR _ 16	PLDERR _ 15	PLDERR _ 14	PLDERR _ 13	PLDERR _ 12	PLDERR _ 11	PLDERR _ 10
46								
	0	0	0	0	0	0	0	0
47								
	0	0	0	0	0	0	0	0
48	GNERRST:B3							
	GNER _31	GNER _30	GNER _29	GNER _28	GNER _27	GNER _26	GNER _25	GNER _24
49	GNERRST:B2							
	GNER _23	GNER _22	GNER _21	GNER _20	GNER _19	GNER _18	GNER _17	GNER _16
4A	GNERRST:B1							
	GNER _15	GNER _14	GNER _13	GNER _12	GNER _11	GNER _10	GNER _09	GNER _08
4B	GNERRST:B0							
	GNER _07	GNER _06	GNER _05	GNER _04	GNER _03	GNER _02	GNER _01	GNER _00
4C	IA32_MC4_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4D	IA32_MC4_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
4E	IA32_MC4_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
4F	IA32_MC4_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
50	IA32_MC4_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
51	IA32_MC4_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
52	IA32_MC4_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
53	IA32_MC4_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
54	IA32_MC5_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
55	IA32_MC5_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10

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Byte27 = 8E (CHK1) Byte40-7F Detail

(3) Byte28 = 22/23/24/25 (2/3)

	0	1	2	3	4	5	6	7
56	IA32_MC5_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
57	IA32_MC5_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
58	IA32_MC5_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
59	IA32_MC5_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
5A	IA32_MC5_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
5B	IA32_MC5_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
5C	IA32_MC6_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5D	IA32_MC6_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
5E	IA32_MC6_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
5F	IA32_MC6_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
60	IA32_MC6_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
61	IA32_MC6_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
62	IA32_MC6_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
63	IA32_MC6_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
64	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
65	IA32_MC9_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
66	IA32_MC9_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
67	IA32_MC9_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
68	IA32_MC9_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
69	IA32_MC9_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
6A	IA32_MC9_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8

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Byte27 = 8E (CHK1) Byte40-7F Detail

(3) Byte28 = 22/23/24/25 (3/3)

	0	1	2	3	4	5	6	7
6B	IA32_MC9_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
6C	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
6D	IA32_MC10_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
6E	IA32_MC10_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
6F	IA32_MC10_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
70	IA32_MC10_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
71	IA32_MC10_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
72	IA32_MC10_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
73	IA32_MC10_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
74	IA32_MC11_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
75	IA32_MC11_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
76	IA32_MC11_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
77	IA32_MC11_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
78	IA32_MC11_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
79	IA32_MC11_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
7A	IA32_MC11_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
7B	IA32_MC11_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7C	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7E	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7F	Reserved							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Byte27 = 8E (CHK1) Byte40-7F Detail

(4) Byte28 = 30 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER ‘04’							
41	IA32_MC0_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
42	IA32_MC0_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
43	IA32_MC0_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
44	IA32_MC1_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
45	IA32_MC1_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
46	IA32_MC1_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
47	IA32_MC2_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
48	IA32_MC3_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
49	IA32_MC3_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
4A	IA32_MC3_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
4B	IA32_MC4_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4C	IA32_MC4_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
4D	IA32_MC4_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
4E	IA32_MC5_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4F	IA32_MC5_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
50	IA32_MC5_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
51	IA32_MC6_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
52	IA32_MC6_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
53	IA32_MC6_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
54	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
55	IA32_MC9_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10

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Byte27 = 8E (CHK1) Byte40-7F Detail

(4) Byte28 = 30 (2/3)

	0	1	2	3	4	5	6	7
56	IA32_MC9_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
57	IA32_MC9_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
58	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
59	IA32_MC10_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
5A	IA32_MC10_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
5B	IA32_MC10_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
5C	IA32_MC11_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5D	IA32_MC11_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
5E	IA32_MC11_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
5F	IA32_MC11_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
60	IA32_MC12_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
61	IA32_MC12_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
62	IA32_MC12_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
63	IA32_MC12_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
64	IA32_MC13_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
65	IA32_MC13_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
66	IA32_MC13_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
67	IA32_MC13_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
68	IA32_MC14_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
69	IA32_MC14_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
6A	IA32_MC14_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8

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Byte27 = 8E (CHK1) Byte40-7F Detail

(4) Byte28 = 30 (3/3)

	0	1	2	3	4	5	6	7
6B	IA32_MC14_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
6C	IA32_MC15_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
6D	IA32_MC15_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
6E	IA32_MC15_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
6F	IA32_MC15_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
70	IA32_MC16_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
71	IA32_MC16_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
72	IA32_MC16_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
73	IA32_MC16_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
74	IA32_MC17_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
75	IA32_MC17_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
76	IA32_MC17_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
77	IA32_MC17_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
78	IA32_MC18_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
79	IA32_MC18_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
7A	IA32_MC18_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
7B	IA32_MC18_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7C	IA32_MC19_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
7D	IA32_MC19_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
7E	IA32_MC19_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
7F	IA32_MC19_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(5) Byte28 = 41/43/47/51/52 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘05’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44								
	0	0	0	0	0	0	0	0
45	P0_XPGLBERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIECE	PCIENFE	Reserved
46	P5_XPGLBERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIECE	PCIENFE	Reserved
47	P6_XPGLBERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIECE	PCIENFE	Reserved
48	P0_CORERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	P0_CORERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	P0_CORERRSTS B1							
	Reserved	Reserved	SDVNFERR	RPLYTO	Reserved	Reserved	Reserved	RPLNRLOV
4B	P0_CORERRSTS B0							
	BADDLLP	BADTLP	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVER ERR
4C	P5_CORERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	P5_CORERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	P5_CORERRSTS B1							
	Reserved	Reserved	SDVNFERR	RPLYTO	Reserved	Reserved	Reserved	RPLNRLOV
4F	P5_CORERRSTS B0							
	BADDLLP	BADTLP	Reserved	Reserved	Reserved	Reserved	Reserved	RECEIVER ERR

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Byte27 = 8E (CHK1) Byte40-7F Detail

(5) Byte28 = 41/43/47/51/52 (2/3)

	0	1	2	3	4	5	6	7
50	P6_CORERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	P6_CORERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
52	P6_CORERRSTS B1							
	Reserved	Reserved	SDVNFERR	RPLYTO	Reserved	Reserved	Reserved	Reserved
53	P6_CORERRSTS B0							
	BADDLLP	BADTLP	Reserved	Reserved	Reserved	Reserved	BADDLLP	BADTLP
54	P0_UNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	P0_UNCERRSTS B2							
	Reserved	Reserved	ACSVIOLAT	RCVUR	Reserved	MALTLP	RCVOVF	UNEXPCTCS
56	P0_UNCERRSTS B1							
	CMPABORT	COMPTO	FCPRTCLERR	POISENDTLP	Reserved	Reserved	Reserved	Reserved
57	P0_UNCERRSTS B0							
	Reserved	Reserved	SPRISDOWN	LNKPRTERR	Reserved	Reserved	Reserved	Reserved
58	P5_UNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	P5_UNCERRSTS B2							
	Reserved	Reserved	ACSVIOLAT	RCVUR	Reserved	MALTLP	RCVOVF	UNEXPCTCS
5A	P5_UNCERRSTS B1							
	CMPABORT	COMPTO	FCPRTCLERR	POISENDTLP	Reserved	Reserved	Reserved	Reserved
5B	P5_UNCERRSTS B0							
	Reserved	Reserved	SPRISDOWN	LNKPRTERR	Reserved	Reserved	Reserved	Reserved
5C	P6_UNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	P6_UNCERRSTS B2							
	Reserved	Reserved	ACSVIOLAT	RCVUR	Reserved	MALTLP	RCVOVF	UNEXPCTCS
5E	P6_UNCERRSTS B1							
	CMPABORT	COMPTO	FCPRTCLERR	POISENDTLP	Reserved	Reserved	Reserved	Reserved
5F	P6_UNCERRSTS B0							
	Reserved	Reserved	SPRISDOWN	LNKPRTERR	Reserved	Reserved	Reserved	Reserved
60								
	0	0	0	0	0	0	0	0
61	P0_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LBW CHANGE
62	P5_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LBW CHANGE
63	P6_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LBW CHANGE
64	P0_XPUNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	P0_XPUNCERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
66	P0_XPUNCERRSTS B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OBPOISNDDT	MSIWRERR
67	P0_XPUNCERRSTS B0							
	Reserved	UR	CA	SENTUR	SENTCA	Reserved	FIFOPE	Reserved
68	P5_XPUNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	P5_XPUNCERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6A	P5_XPUNCERRSTS B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OBPOISNDDT	MSIWRERR
6B	P5_XPUNCERRSTS B0							
	Reserved	UR	CA	SENTUR	SENTCA	Reserved	FIFOPE	Reserved

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Byte27 = 8E (CHK1) Byte40-7F Detail

(5) Byte28 = 41/43/47/51/52 (3/3)

	0	1	2	3	4	5	6	7
6C	P6_XPUNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	P6_XPUNCERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6E	P6_XPUNCERRSTS B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OBPOISNDDT	MSIWRERR
6F	P6_XPUNCERRSTS B0							
	Reserved	UR	CA	SENTUR	SENTCA	Reserved	FIFOPE	Reserved
70	IRPP0ERRST B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	IRPP0ERRST B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
72	IRPP0ERRST B1							
	Reserved	PE	OVFLOW	Reserved	Reserved	UNEXPRESP	Reserved	Reserved
73	IRPP0ERRST B0							
	Reserved	Reserved	Reserved	CSRACSERR	WCUNCERR	POISONED	WCCORERR	Reserved
74	IRPP1ERRST B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	IRPP1ERRST B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76	IRPP1ERRST B1							
	Reserved	PE	OVFLOW	Reserved	Reserved	UNEXPRESP	Reserved	Reserved
77	IRPP1ERRST B0							
78								
	0	0	0	0	0	0	0	0
79								
	0	0	0	0	0	0	0	0
7A								
	0	0	0	0	0	0	0	0
7B								
	0	0	0	0	0	0	0	0
7C								
	0	0	0	0	0	0	0	0
7D								
	0	0	0	0	0	0	0	0
7E								
	0	0	0	0	0	0	0	0
7F								
	0	0	0	0	0	0	0	0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(6) Byte28 = 42/50 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘06’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	P5_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
45	P6_XPCORERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
46	P5_XPGLBERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIECE	Reserved	Reserved
47	P6_XPGLBERRSTS							
	Reserved	Reserved	Reserved	Reserved	Reserved	PCIECE	Reserved	Reserved
48	P5_CORERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	P5_CORERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	P5_CORERRSTS B1							
	Reserved	Reserved	SDVNFERR	RPLYTO	Reserved	Reserved	Reserved	Reserved
4B	P5_CORERRSTS B0							
	BADDLLP	BADTLP	Reserved	Reserved	Reserved	Reserved	BADDLLP	BADTLP
4C	P6_CORERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	P6_CORERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4E	P6_CORERRSTS B1							
	Reserved	Reserved	SDVNFERR	RPLYTO	Reserved	Reserved	Reserved	Reserved
4F	P6_CORERRSTS B0							
	BADDLLP	BADTLP	Reserved	Reserved	Reserved	Reserved	BADDLLP	BADTLP
50	P5_UNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	P5_UNCERRSTS B2							
	Reserved	Reserved	ACSVIOLAT	RCVUR	Reserved	MALTLP	Reserved	Reserved
52	P5_UNCERRSTS B1							
	CMPABORT	COMPTO	FCPRTCLERR	POISENDTLP	Reserved	Reserved	CMPABORT	COMPTO
53	P5_UNCERRSTS B0							
	Reserved	Reserved	SPRISDOWN	LNKPRTERR	Reserved	Reserved	Reserved	Reserved
54	P6_UNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	P6_UNCERRSTS B2							
	Reserved	Reserved	ACSVIOLAT	RCVUR	Reserved	MALTLP	Reserved	Reserved
56	P6_UNCERRSTS B1							
	CMPABORT	COMPTO	FCPRTCLERR	POISENDTLP	Reserved	Reserved	CMPABORT	COMPTO
57	P6_UNCERRSTS B0							
	Reserved	Reserved	SPRISDOWN	LNKPRTERR	Reserved	Reserved	Reserved	Reserved

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Byte27 = 8E (CHK1) Byte40-7F Detail

(6) Byte28 = 42/50 (2/3)

	0	1	2	3	4	5	6	7
58	P5_XPUNCERRSTS B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	P5_XPUNCERRSTS B0							
	Reserved	UR	CA	SENTUR	SENTCA	Reserved	Reserved	UR
5A	P6_XPUNCERRSTS B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5B	P6_XPUNCERRSTS B0							
	Reserved	UR	CA	SENTUR	SENTCA	Reserved	Reserved	UR
5C	DMAUNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	DMAUNCERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5E	DMAUNCERRSTS B1							
	Reserved	Reserved	Reserved	Syndrome	Reserved	RDADDECERR	Reserved	Reserved
5F	DMAUNCERRSTS B0							
	RDCMPHDERR	Reserved	Reserved	CFGPE	INTHWPE	POISONEDDT	Reserved	Reserved
60	C0_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	C0_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
62	C0_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
63	C0_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
64	C1_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	C1_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
66	C1_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
67	C1_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
68	C2_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	C2_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
6A	C2_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
6B	C2_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
6C	C3_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6D	C3_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
6E	C3_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
6F	C3_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR

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Byte27 = 8E (CHK1) Byte40-7F Detail

(6) Byte28 = 42/50 (3/3)

	0	1	2	3	4	5	6	7
70	C4_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
71	C4_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
72	C4_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
73	C4_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
74	C5_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
75	C5_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
76	C5_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
77	C5_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
78	C6_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
79	C6_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
7A	C6_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
7B	C6_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
7C	C7_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7D	C7_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
7E	C7_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
7F	C7_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR

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Byte27 = 8E (CHK1) Byte40-7F Detail

(7) Byte28 = 44/45 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘07’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	GFERRST:B3							
	GFER _31	GFER _30	GFER _29	GFER _28	GFER _27	GFER _26	GFER _25	GFER _24
45	GFERRST:B2							
	GFER _23	GFER _22	GFER _21	GFER _20	GFER _19	GFER _18	GFER _17	GFER _16
46	GFERRST:B1							
	GFER _15	GFER _14	GFER _13	GFER _12	GFER _11	GFER _10	GFER _09	GFER _08
47	GFERRST:B0							
	GFER _07	GFER _06	GFER _05	GFER _04	GFER _03	GFER _02	GFER _01	GFER _00
48	DMAUNCERRSTS B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
49	DMAUNCERRSTS B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4A	DMAUNCERRSTS B1							
	Reserved	Reserved	Reserved	Syndrome	Reserved	RDADDECERR	Reserved	Reserved
4B	DMAUNCERRSTS B0							
	RDCMPHDERR	Reserved	Reserved	CFGPE	INTHWPE	POISONEDDT	Reserved	Reserved
4C	C0_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4D	C0_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
4E	C0_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
4F	C0_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
50	C1_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
51	C1_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
52	C1_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
53	C1_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
54	C2_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
55	C2_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
56	C2_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
57	C2_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR

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Byte27 = 8E (CHK1) Byte40-7F Detail

(7) Byte28 = 44/45 (2/3)

	0	1	2	3	4	5	6	7
58	C3_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	C3_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
5A	C3_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
5B	C3_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
5C	C4_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5D	C4_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
5E	C4_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
5F	C4_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
60	C5_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
61	C5_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
62	C5_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
63	C5_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
64	C6_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
65	C6_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
66	C6_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
67	C6_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
68	C7_CHANERR_INT B3							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
69	C7_CHANERR_INT B2							
	Reserved	Reserved	Reserved	Reserved	Reserved	DESCCNTERR	XORQERR	XOWPERR
6A	C7_CHANERR_INT B1							
	UNAFFILERR	Reserved	INTCFGERR	CMPADRERR	DESCLENERR	DESCCTLERR	WRDTERR	RDDTERR
6B	C7_CHANERR_INT B0							
	DTPE	CDTPE	CHANCMDER	CHAINADRER	DESCERR	NDESCERR	DESTADRERR	SRCADRERR
6C	IA32_MC0_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
6D	IA32_MC1_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
6E	IA32_MC2_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
6F	IA32_MC3_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(7) Byte28 = 44/45 (3/3)

	0	1	2	3	4	5	6	7
70	IA32_MC4_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
71	IA32_MC5_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
72	IA32_MC6_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
73	IA32_MC9_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
74	IA32_MC10_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
75	IA32_MC11_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
76	IA32_MC12_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
77	IA32_MC13_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
78	IA32_MC14_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
79	IA32_MC15_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7A	IA32_MC16_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7B	IA32_MC17_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7C	IA32_MC18_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7D	IA32_MC19_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0
7E								
	0	0	0	0	0	0	0	0
7F								
	0	0	0	0	0	0	0	0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(8) Byte28 = 60 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(8) Byte28 = 60 (2/4)

	0	1	2	3	4	5	6	7
50	INT1_INT_ERR_STS0:B3							
	EATR Error STS							
51	INT1_INT_ERR_STS0:B2							
	EATR Error STS							
52	INT1_INT_ERR_STS0:B1							
	EATR Error STS							
53	INT1_INT_ERR_STS0:B0							
	EATR Error STS							
54	INT1_INT_ERR_STS1:B3							
	MPLog1 Error STS							
55	INT1_INT_ERR_STS1:B2							
	MPLog0 Error STS							
56	INT1_INT_ERR_STS1:B1							
	EAC Error STS							
57	INT1_INT_ERR_STS1:B0							
	EAC Error STS							
58	INT1_INT_ERR_STS2:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
59	INT1_INT_ERR_STS2:B2							
	MSI Error STS							
5A	INT1_INT_ERR_STS2:B1							
	DMA ErrorB STS							
5B	INT1_INT_ERR_STS2:B0							
	DMA ErrorA STS							
5C	INT1_INT_ERR_STS3:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5D	INT1_INT_ERR_STS3:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5E	INT1_INT_ERR_STS3:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	MBOX ASEQ Error STS
5F	INT1_INT_ERR_STS3:B0							
	LOCKR3 ASEQ Error STS	LOCKR2 ASEQ Error STS	LOCKR1 ASEQ Error STS	LOCKR0 ASEQ Error STS	Not used	GPTIM2 Parity Error STS	GPTIM1 Parity Error STS	GPTIM0 Parity Error STS

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Byte27 = 8E (CHK1) Byte40-7F Detail

(8) Byte28 = 60 (3/4)

	0	1	2	3	4	5	6	7
60	SWIF_ERR_STATUS_0:B3							
	Error STATUS							
61	SWIF_ERR_STATUS_0:B2							
	Error STATUS							
62	SWIF_ERR_STATUS_0:B1							
	Error STATUS							
63	SWIF_ERR_STATUS_0:B0							
	Error STATUS							
64	SWIF_ERR_STATUS_1:B3							
	Error STATUS							
65	SWIF_ERR_STATUS_1:B2							
	Error STATUS							
66	SWIF_ERR_STATUS_1:B1							
	Error STATUS							
67	SWIF_ERR_STATUS_1:B0							
	Error STATUS							
68	SWIF_ERR_STATUS_2:B3							
	Error STATUS							
69	SWIF_ERR_STATUS_2:B2							
	Error STATUS							
6A	SWIF_ERR_STATUS_2:B1							
	Error STATUS							
6B	SWIF_ERR_STATUS_2:B0							
	Error STATUS							
6C	SWIF_ERR_STATUS_3:B3							
	Error STATUS							
6D	SWIF_ERR_STATUS_3:B2							
	Error STATUS							
6E	SWIF_ERR_STATUS_3:B1							
	Error STATUS							
6F	SWIF_ERR_STATUS_3:B0							
	Error STATUS							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(8) Byte28 = 60 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(9) Byte28 = 61 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(9) Byte28 = 61 (2/4)

	0	1	2	3	4	5	6	7
50	RGARB_CHK_LOG_ALL:B3							
	SWIF DEC Error	SWIF ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
51	RGARB_CHK_LOG_ALL:B2							
	XBF TAG Parity Error	XBF ID Parity Error	XBF LADR Parity Error	XBF LEN Parity Error	XBF BE Parity Error	XBF MPNO Parity Error	TXBF RDT Parity Error	TXBF Error Parity Error
52	RGARB_CHK_LOG_ALL:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
53	RGARB_CHK_LOG_ALL:B0							
	CTL RA Error	DTA RAIF Error	Error05 E TO RAIF	DEC Error	ENC Error	MSI OFF Error	MSI TIMOUT Error	MSI CNT Parity Error
54	XREG_HARX_ERR_ALLLOG:B3							
	DEC Error	ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
55	XREG_HARX_ERR_ALLLOG:B2							
	HED Parity Error	NPCNT Parity Error	PCCNT Parity Error	DLRCTIM Error	VLD OFF Error	REQ OFF Error	Not used	SEQ STS Parity Error
56	XREG_HARX_ERR_ALLLOG:B1							
	TX Error	Not used	MPNO 128OVR Error	LEN0B ACS	BUF OVF	FMT TYPE Error	XBF CNT Parity Error	TXBF CNT Parity Error
57	XREG_HARX_ERR_ALLLOG:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
58	XREG_RAIF_ERR_ALLLOG:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
59	XREG_RAIF_ERR_ALLLOG:B2							
	RGARB ADRBE PCHK	RGARB WDT PCHK	RGARB RDT PCHK	RGARB CMP	SEQ END TIMEOUT	RGARB ARB	RGARB XR RSV	RGARB BEWR VALID
5A	XREG_RAIF_ERR_ALLLOG:B1							
	MPX RSV REG ACS	MPNO PCHK	RA Error PCHK	TXBF OVFLOW	FUNC PCHK	WDT PCHK	WEBE PCHK	ADR PCHK
5B	XREG_RAIF_ERR_ALLLOG:B0							
	SEQ PCHK	SEQ ENC	SEQ DEC	RGARB SEQ	TXBF PCHK	RXBF PCHK	GNT TO	TIMER PCHK
5C	XREG_HATX_ERR_ALLLOG:B3							
	SWIF DEC Error	SWIF ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
5D	XREG_HATX_ERR_ALLLOG:B2							
	XBF TAG Parity Error	XBF ID Parity Error	XBF LADR Parity Error	XBF LEN Parity Error	XBF BE Parity Error	XBF MPNO Parity Error	TXBF RDT Parity Error	TXBF Error Parity Error
5E	XREG_HATX_ERR_ALLLOG:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
5F	XREG_HATX_ERR_ALLLOG:B0							
	CTL RA Error	DTA RAIF Error	Error05 E TO RAIF	DEC Error	ENC Error	MSI OFF Error	MSI TIMOUT Error	MSI CNT Parity Error

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Byte27 = 8E (CHK1) Byte40-7F Detail

(9) Byte28 = 61 (3/4)

	0	1	2	3	4	5	6	7
60	XREG_HARX_ERR_ALLLOG:B3							
	DEC Error	ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
61	XREG_HARX_ERR_ALLLOG:B2							
	HED Parity Error	NPCNT Parity Error	PCCNT Parity Error	DLRCTIM Error	VLD OFF Error	REQ OFF Error	Not used	SEQ STS Parity Error
62	XREG_HARX_ERR_ALLLOG:B1							
	TX Error	Not used	MPNO 128OVR Error	LEN0B ACS	BUF OVF	FMT TYPE Error	XBF CNT Parity Error	TXBF CNT Parity Error
63	XREG_HARX_ERR_ALLLOG:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
64	XREG_RAIF_ERR_ALLLOG:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	XREG_RAIF_ERR_ALLLOG:B2							
	RGARB ADRBE PCHK	RGARB WDT PCHK	RGARB RDT PCHK	RGARB CMP	SEQ END TIMEOUT	RGARB ARB	RGARB XR RSV	RGARB BEWR VALID
66	XREG_RAIF_ERR_ALLLOG:B1							
	MPX RSV REG ACS	MPNO PCHK	RA Error PCHK	TXBF OVFLOW	FUNC PCHK	WDT PCHK	WEBE PCHK	ADR PCHK
67	XREG_RAIF_ERR_ALLLOG:B0							
	SEQ PCHK	SEQ ENC	SEQ DEC	RGARB SEQ	TXBF PCHK	RXBF PCHK	GNT TO	TIMER PCHK
68	XREG_HATX_ERR_ALLLOG:B3							
	SWIF DEC Error	SWIF ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
69	XREG_HATX_ERR_ALLLOG:B2							
	XBF TAG Parity Error	XBF ID Parity Error	XBF LADR Parity Error	XBF LEN Parity Error	XBF BE Parity Error	XBF MPNO Parity Error	TXBF RDT Parity Error	TXBF Error Parity Error
6A	XREG_HATX_ERR_ALLLOG:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
6B	XREG_HATX_ERR_ALLLOG:B0							
	CTL RA Error	DTA RAIF Error	Error05 E TO RAIF	DEC Error	ENC Error	MSI OFF Error	MSI TIMOUT Error	MSI CNT Parity Error
6C	XREG_HARX_ERR_ALLLOG:B3							
	DEC Error	ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
6D	XREG_HARX_ERR_ALLLOG:B2							
	HED Parity Error	NPCNT Parity Error	PCCNT Parity Error	DLRCTIM Error	VLD OFF Error	REQ OFF Error	Not used	SEQ STS Parity Error
6E	XREG_HARX_ERR_ALLLOG:B1							
	TX Error	Not used	MPNO 128OVR Error	LEN0B ACS	BUF OVF	FMT TYPE Error	XBF CNT Parity Error	TXBF CNT Parity Error
6F	XREG_HARX_ERR_ALLLOG:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 8E (CHK1) Byte40-7F Detail

(9) Byte28 = 61 (4/4)

	0	1	2	3	4	5	6	7
70	XREG_RAIF_ERR_ALLLOG:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	XREG_RAIF_ERR_ALLLOG:B2							
	RGARB ADRBE PCHK	RGARB WDT PCHK	RGARB RDT PCHK	RGARB CMP	SEQ END TIMEOUT	RGARB ARB	RGARB XR RSV	RGARB BEWR VALID
72	XREG_RAIF_ERR_ALLLOG:B1							
	MPX RSV REG ACS	MPNO PCHK	RA Error PCHK	TXBF OVFLOW	FUNC PCHK	WDT PCHK	WEBE PCHK	ADR PCHK
73	XREG_RAIF_ERR_ALLLOG:B0							
	SEQ PCHK	SEQ ENC	SEQ DEC	RGARB SEQ	TXBF PCHK	RXBF PCHK	GNT TO	TIMER PCHK
74	XREG_HATX_ERR_ALLLOG:B3							
	SWIF DEC Error	SWIF ENC Error	WDCNT Parity Error	TOCNT TO	TOCNT Parity Error	DT Parity Error	HLRC Error	DLRC Error
75	XREG_HATX_ERR_ALLLOG:B2							
	XBF TAG Parity Error	XBF ID Parity Error	XBF LADR Parity Error	XBF LEN Parity Error	XBF BE Parity Error	XBF MPNO Parity Error	TXBF RDT Parity Error	TXBF Error Parity Error
76	XREG_HATX_ERR_ALLLOG:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
77	XREG_HATX_ERR_ALLLOG:B0							
	CTL RA Error	DTA RAIF Error	Error05 E TO RAIF	DEC Error	ENC Error	MSI OFF Error	MSI TIMOUT Error	MSI CNT Parity Error
78	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
79	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7A	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7B	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7C	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7D	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7E	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error
7F	SMBM_MONI:B1							
	RX Error	XBF CNT Parity Error	TXBF CNT Parity Error	SWIF SEQ Parity Error	SEQ Parity Error	MPX Error	XR Error	DTA RA Error

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Byte27 = 8E (CHK1) Byte40-7F Detail

(10) Byte28 = 62 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(10) Byte28 = 62 (2/4)

	0	1	2	3	4	5	6	7
50	SMC_CHK1_ERRLOG01:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	CRGREGIF RDTH PER Log	CRG REGIF RDTL PER Log
51	SMC_CHK1_ERRLOG01:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ECSEQ WTRDY TOV Log
52	SMC_CHK1_ERRLOG01:B5							
	Not used	ECSEQ TP DECError	ECSEQ TOVTMR Parity Error	ECSEQ PCD WCNT Parity Error	ECSEQ RD CNT Parity Error	ECSEQ PC FCNT CMP Parity Error	ECSEQ SEQ DEC ENC Error	ECSEQ PENC GNTError
53	SMC_CHK1_ERRLOG01:B4							
	Not used	Not used	Not used	Not used	Not used	Not used	ERX HDR WPTR Parity Error	ERX HDR RPTR Parity Error
54	SMC_CHK1_ERRLOG01:B3							
	ERX HDR IMMCNT Parity Error	ERX HDR DLYCNT Parity Error	ERX HDR OverFlow Error	ERX HDR Undrlow Error	ERX DAT DLYCNT Parity Error	ERX DAT IMMCNT Parity Error	ERX DAT OverFlow Error	ERX DAT RPTR Parity Error
55	SMC_CHK1_ERRLOG01:B2							
	ERX DAT Undrlow Error	ERX DAT WPTR Parity Error	ERX PCBSYCNT Parity Error	ERX UR Error	ERX OVER256B Error	ERX DATCNT Parity Error	ERX DAT O Parity Error	ERX HDR MARGE O Parity Error
56	SMC_CHK1_ERRLOG01:B1							
	Not used	ERX E14 REQOFF Error	ERX E13 VLD Error	ERX E12 DLRCTIM Error	ERX E11 PCCNT Parity Error	ERX E10 NPCNT Parity Error	ERX E09 HED Parity Error	ERX E08 DLRC NEQ Log
57	SMC_CHK1_ERRLOG01:B0							
	ERX E07 HLRC NEQ Log	ERX E06 DT Parity Error	ERX E05 TOCNT Parity Error	ERX E04 TOCNT TO Log	ERX E03 WDCNT Parity Error	ERX E02 ENCError	ERX E01 DECError	Not used
58	SMC_CHK1_ERRLOG02:B7							
	Not used	Not used	Not used	E2E AT Micro Error	E2E HDR DIFFCNT Q Parity Error	E2E HDR DIFFCNT Q Parity Error	E2E DAT DIFFCNT Q Parity Error	E2E DAT DIFFCNT Q Parity Error
59	SMC_CHK1_ERRLOG02:B6							
	E2E RAM WTPTR1 Parity Error	E2E DAT WTPTR1 Parity Error	E2E RAM RDPTR Parity Error	E2E DAT RDPTR Parity Error	E2E HDR Undrlow Error	E2E HDR OverFlow Error	E2E DAT Undrlow Error	E2E DAT OverFlow Error
5A	SMC_CHK1_ERRLOG02:B5							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5B	SMC_CHK1_ERRLOG02:B4							
	E2E HDR I1 Parity Error	E2E DAT I1 Parity Error	E2E TX HDR2 Parity Error	E2E TX DAT2 Parity Error	E2E HDR UNCRError	E2E DAT UNCRError	E2E HDR ADRError	E2E DAT ADRError
5C	SMC_CHK1_ERRLOG02:B3							
	Not used	Not used	Not used	Not used	E2ESEQ TMRCNT Parity Error	Not used	E2ESEQ ENCError	E2ESEQ DECError
5D	SMC_CHK1_ERRLOG02:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5E	SMC_CHK1_ERRLOG02:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5F	SMC_CHK1_ERRLOG02:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	E2ESEQ TMROVER Error

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Byte27 = 8E (CHK1) Byte40-7F Detail

(10) Byte28 = 62 (3/4)

	0	1	2	3	4	5	6	7
60	SMC_CHK1_ERRLOG03:B7							
	Not used	Not used	Not used	ENP AT Micro Error	ENP HDR DIFFCNT Q Parity Error	ENP HDR DIFFCNT Q Parity Error	ENP DAT DIFFCNT Q Parity Error	ENP DAT DIFFCNT Q Parity Error
61	SMC_CHK1_ERRLOG03:B6							
	ENP RAM WTPTR1 Parity Error	ENP DAT WTPTR1 Parity Error	ENP RAM RDPTR Parity Error	ENP DAT RDPTR Parity Error	ENP HDR Undrlow Error	ENP HDR OverFlow Error	ENP DAT Undrlow Error	ENP DAT OverFlow Error
62	SMC_CHK1_ERRLOG03:B5							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
63	SMC_CHK1_ERRLOG03:B4							
	ENP HDR I1 Parity Error	ENP DAT I1 Parity Error	ENP TX HDR2 Parity Error	ENP TX DAT2 Parity Error	ENP HDR UNCRError	ENP DAT UNCRError	ENP HDR ADRError	ENP DAT ADRError
64	SMC_CHK1_ERRLOG03:B3							
	Not used	Not used	Not used	Not used	ENPSEQ TMRCNT Parity Error	Not used	ENPSEQ ENCError	ENPSEQ DECError
65	SMC_CHK1_ERRLOG03:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	SMC_CHK1_ERRLOG03:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
67	SMC_CHK1_ERRLOG03:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ENPSEQ TMROVER Error
68	SMC_CHK1_ERRLOG04:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
69	SMC_CHK1_ERRLOG04:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	ENPC RCNT PER Log OR	ENPC GNTError
6A	SMC_CHK1_ERRLOG04:B5							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	SMC_CHK1_ERRLOG04:B4							
	Not used	Not used	Not used	Not used	Not used	Not used	ENPC HDROUT PER Log	ENPC DATOUT PER Log
6C	SMC_CHK1_ERRLOG04:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6D	SMC_CHK1_ERRLOG04:B2							
	Not used	Not used	Not used	Not used	Not used	ENPCSEQ TMRPER Log	ENPCSEQ ENCError	ENPCSEQ DECError
6E	SMC_CHK1_ERRLOG04:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6F	SMC_CHK1_ERRLOG04:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ENPCSEQ SEQTOV Log

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Byte27 = 8E (CHK1) Byte40-7F Detail

(10) Byte28 = 62 (4/4)

	0	1	2	3	4	5	6	7
70	SMC_CHK1_ERRLOG05:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	SMC_CHK1_ERRLOG05:B6							
	ETSQ XNP PCMP Parity Error	ETSEQ ENP PCMP Parity Error	ETSEQ NPTMR Parity Error	ETSEQ PCTMR Parity Error	ETSEQ TX NPPENC GNTError	ETSEQ TX PENC GNTError	ETSEQ SEQ ENCError	ETSEQ SEQ DECError
72	SMC_CHK1_ERRLOG05:B5							
	Not used	Not used	Not used	Not used	Not used	Not used	ETSEQ NPTOV Log	ETSEQ PCTOV Log
73	SMC_CHK1_ERRLOG05:B4							
	Not used	Not used	ETXARB HDR Parity Error	ETXARB DAT Parity Error	Not used	Not used	ETXARB GNTCHK Error	ETXARB SEQ Error
74	SMC_CHK1_ERRLOG05:B3							
	ECTLLog reserve							
75	SMC_CHK1_ERRLOG05:B2							
	ECTL CPL TOV CHK1 Log	Not used	Not used	ECTL HDR OUT Parity Error	ECTL DAT OUT Parity Error	ECTL RXHDR Parity Error	ECTL RXDAT Parity Error	ECTL TP V Parity Error
76	SMC_CHK1_ERRLOG05:B1							
	ECTL MPNUM Parity Error	ECTL MPSEL Parity Error	ECTL TBLDAT Parity Error	ECTL STD WND NUM Parity Error	ECTL TP OUT V Parity Error	ECTL REQ DSTADR Parity Error	ECTL PRDT LMBASE Parity Error	ECTL LMOffset Parity Error
77	SMC_CHK1_ERRLOG05:B0							
	ECTL PREG ADR Parity Error	ECTL EXT WND NUM Parity Error	ECTL LEN OVER256B Error	ECTL NON SMC ADR Error	ECTL HDR MPEN OFF Error	ECTL HLRC Error	ECTL ACC MODECHK Parity Error	ECTL TBL FMT Error
78	SMC_CHK1_ERRLOG06:B7							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ETBL Log TMRPER TBL
79	SMC_CHK1_ERRLOG06:B6							
	Not used	Not used	Not used	Not used	Not used	Not used	ETX ENPC HDR Parity Error	ETX ENPC DAT Parity Error
7A	SMC_CHK1_ERRLOG06:B5							
	Not used	Not used	Not used	ETX NP XNP OCnt0 Parity Error	ETX NP XNP OCnt1 Parity Error	ETX NP XNP DCNT Parity Error	ETX NP XNP WPTR Parity Error	ETX NP XNP RPTR Parity Error
7B	SMC_CHK1_ERRLOG06:B4							
	Not used	Not used	Not used	ETX NP ENP OCnt0 Parity Error	ETX NP ENP OCnt1 Parity Error	ETX NP ENP DCNT Parity Error	ETX NP ENP WPTR Parity Error	ETX NP ENP RPTR Parity Error
7C	SMC_CHK1_ERRLOG06:B3							
	Not used	Not used	ETX NP HDR Parity Error	ETX NP DAT Parity Error	ETX NP XNP HDR Parity Error	ETX NP XNP DAT Parity Error	ETX NP ENP HDR Parity Error	ETX NP ENP DAT Parity Error
7D	SMC_CHK1_ERRLOG06:B2							
	ETX SWIF DECError	ETX SWIF ENCError	ETX SWIF WDCNT Parity Error	ETX SWIF TOCNT TO Log	ETX SWIF TOCNT Parity Error	ETX SWIF DT Parity Error	ETX SWIF HLRCError	ETX SWIF DLRCError
7E	SMC_CHK1_ERRLOG06:B1							
	ETX MVCNT Parity Error	ETX HDR WDFCNT Parity Error	ETX HDR WPTR Parity Error	ETX HDR RDFCNT Parity Error	ETX HDR RPTR Parity Error	ETX DAT WDFCNT Parity Error	ETX DAT WPTR Parity Error	ETX DAT RPTR Parity Error
7F	SMC_CHK1_ERRLOG06:B0							
	Not used	Not used	Not used	Not used	ETX HDR UNCRError	ETX HDR ADRError	ETX DAT UNCRError	ETX DAT ADRError

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Byte27 = 8E (CHK1) Byte40-7F Detail

(11) Byte28 = 63 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(11) Byte28 = 63 (2/4)

	0	1	2	3	4	5	6	7
50	XARB_RX_PCK_ERR0:B3							
	Not used	RXSEQ0 QENC Error	RXSEQ0 Q Parity Error	PCI ECC DETECT	RXBLK ECRC Error	Not used	RXHDBUF WTPT Parity Error	Not used
51	XARB_RX_PCK_ERR0:B2							
	Not used	RXNDBUF WTPT Parity Error	RXHDIX Parity Error	Not used	RXDT WTADR Parity Error	RXSEQ0 TCNT Parity Error	RXNHIX Parity Error	RCRC CMP Parity Error
52	XARB_RX_PCK_ERR0:B1							
	P2C SEQ DEC Error	P2C SEQ ENC Error	P2C SEQ Parity Error	P2C CNT Parity Error	RX Parity Error	RXNDBUF ING Parity Error	RXDTIX DTCMP Parity Error	RXDTIX WADR Parity Error
53	XARB_RX_PCK_ERR0:B0							
	TAGxTMR SEQ Parity Error	TAGxTMR ENC Error	TAGxTMR GP Error	BACNTGP Error	RX PCK CHK4TOP	RX PCK CHK1TOP	RX PCK WRN TOP	Not used
54	XARB_TX_PCK_ERR0:B3							
	TXHD RDPT Parity Error	TXNH RDPT Parity Error	TXNH WTPT Parity Error	TXND RDPT Parity Error	BETY Error	CDETY Error	CHETY Error	NDETY Error
55	XARB_TX_PCK_ERR0:B2							
	NHETY FRC Error	PDETY FRC Error	PHETY FRC Error	QETY FRC Error	LINK Error	TXSEQ0 QE Error	TXSEQ0 Q Parity Error	P2C SEQ D Error
56	XARB_TX_PCK_ERR0:B1							
	P2C SEQ E Error	P2C SEQ Parity Error	TXDT RDADR Parity Error	P2C CNT Parity Error	TXHDOX Parity Error	TXDTOX Parity Error	TXNHIX Parity Error	TXNHOX Parity Error
57	XARB_TX_PCK_ERR0:B0							
	LINK Error	TXNDBUF WTPT Parity Error	STOPREQ Parity Error	TX ErrorGP Error	TXSEQ0 TCNT Parity Error	Not used	XFBCNTGP Error	XFQCNT Parity Error
58	XARB_TX_PCK_ERR1:B3							
	ICNT Parity Error	TXHDDT A Parity Error	TXHDDT E Parity Error	Not used	ICNT NP Parity Error	NPHDBUF Parity Error	TXDTBUF Parity Error	TXNDBUF Parity Error
59	XARB_TX_PCK_ERR1:B2							
	CHCNT Parity Error	NHCNT Parity Error	PHCNT Parity Error	CDCNT Parity Error	NDCNT Parity Error	PDCNT Parity Error	TXDTBUF ADR Error	TXDTBUF UNC Error
5A	XARB_TX_PCK_ERR1:B1							
	FCTMR SEQ Parity Error	FCTMR SEQ ENC Error	FCTMRGP Error	FCTMR TO Error	Not used	Not used	Not used	Not used
5B	XARB_TX_PCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN TOP	Not used
5C	XARB_RX_UCK_ERR0:B3							
	RXHDBUF RDPT Parity Error	RXDTBUF ADR Error	RXDTBUF UNCOR	RXNHBUF RDPT Parity Error	RXNDBUF RDPT Parity Error	RXDT RDADR Parity Error	RXHDOX Parity Error	WCRC CMP Parity Error
5D	XARB_RX_UCK_ERR0:B2							
	RXNHOX Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error	C2P CNT Parity Error	SWTX DEC Error	SWTX DLRC G Error
5E	XARB_RX_UCK_ERR0:B1							
	SWTX DT LGP Error	SWTX ENC Error	SWTX HLRC G Error	Not used	SWTX TOCNTGP Error	SWTX TOCNT TO	SWTX WDCNTGP Error	Not used
5F	XARB_RX_UCK_ERR0:B0							
	ARBSEQ QDEC Error	ARBSEQ QENC Error	ARBSEQ Q Parity Error	RXNHBUF WTPT Parity Error	MRG ECC ADR Error	MRG ECC UNCOR	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error

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Byte27 = 8E (CHK1) Byte40-7F Detail

(11) Byte28 = 63 (3/4)

	0	1	2	3	4	5	6	7
60	XARB_RX_UCK_ERR1:B3							
	MRGBUF DTCNT Parity Error	MRGBUF TMR Parity Error	XFCNTGP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	RXNHBUF OVER	Not used	Not used
61	XARB_RX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
62	XARB_RX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
63	XARB_RX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN TOP	Not used
64	XARB_TX_UCK_ERR0:B3							
	SWRX DEC Error	SWRX DLRCTIM G Error	SWRX DLRC G Error	SWRX ENC Error	SWRX HLRC G Error	SWRX SW DTGP Error	SWRX SW VLD G Error	SWRX TOCNTGP Error
65	XARB_TX_UCK_ERR0:B2							
	SWRX TOCNT TO	SWRX TX Error G Error	SWRX WDCNTGP Error	TXHDBUF WTPT Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error
66	XARB_TX_UCK_ERR0:B1							
	C2P CNT Parity Error	TXDTBUF WTADR Parity Error	TXHDIX Parity Error	Not used	TXNHCNT Parity Error	SWRX REQOFF Error	SWRX SW HD Parity Error	DATCNT Parity Error
67	XARB_TX_UCK_ERR0:B0							
	DIV ECC ADR Error	DIV ECC CRCT Error	DIV ECC UNCOR	CPLSEQ QDEC Error	CPLSEQ QENC Error	CPLSEQ Q Parity Error	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
68	XARB_TX_UCK_ERR1:B3							
	CDICNT Parity Error	CPLSEQ DTCNT Parity Error	XFCNTGP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	MIC CHK1 Error	TXDTIX DTCMP Parity Error	TXDTIX WACMP Parity Error
69	XARB_TX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	XARB_TX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	XARB_TX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN TOP	Not used
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(11) Byte28 = 63 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(12) Byte28 = 64 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(12) Byte28 = 64 (2/4)

	0	1	2	3	4	5	6	7
50	DXC_REP_ERROR:B3							
	Log-RAM-ST	MICRO Error	DIMM1 Error	DIMM0 Error	HARD Error	Not used	Not used	Not used
51	DXC_REP_ERROR:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
52	DXC_REP_ERROR:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
53	DXC_REP_ERROR:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	DXC_ERROR_1 :B3							
	LENGTH OVER	BE Error	AREA Error	STEP OVER	CMD Error	ACC Error	SMC Error	Not used
55	DXC_ERROR_1 :B2							
	ACC DIMM0 Error	ACC DIMM1 Error	Not used	ACC REFRDY Error	Not used	Not used	Not used	WLST Error
56	DXC_ERROR_1 :B1							
	REQHEAD1 Parity Error	REQHEAD2 Parity Error	WLEN Parity Error	RLEN Parity Error	CMP Error	DQS ACTIVE Error	HLRC Error	DLRC Error
57	DXC_ERROR_1 :B0							
	MEMINIT ADR Parity Error	Not used	MEMINIT ENC Error	CUDG DT Parity Error	MEMINIT CMP Error	CMP DT Parity Error	RDT Parity Error	RADR Parity Error
58	DXC_ERROR_2 :B3							
	Not used	Not used	Not used	Not used	Not used	TRFC DCNT Parity Error	TRP DCNT Parity Error	TZQ DCNT Parity Error
59	DXC_ERROR_2 :B2							
	TRC DCNT Parity Error	TXSDLL DCNT Parity Error	TRAS DCNT Parity Error	TMOD DCNT Parity Error	TCKESR DCNT Parity Error	TRCD DCNT Parity Error	WL DCNT Parity Error	TWR DCNT Parity Error
5A	DXC_ERROR_2 :B1							
	ADR Parity Error	NXADR Parity Error	STR ADR Parity Error	LST ADR Parity Error	CNT Parity Error	LDCNT Parity Error	LDCNT 0 Error	BORROW Error
5B	DXC_ERROR_2 :B0							
	Not used	SEQ1 ENC Error	SEQ2 ENC Error	TIME Parity Error	Not used	Not used	Not used	Not used
5C	DXC_ERROR_3 :B3							
	Error DCRW	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5D	DXC_ERROR_3 :B2							
	Error DCWC		Not used	Not used	Not used	Not used	Not used	Not used
5E	DXC_ERROR_3 :B1							
	COR CYCL Parity Error	COR ADR Parity Error	RDT 16BS Parity Error	REWR CMP Parity Error	RMW ECC Error1 D0	RMW ECC Error0 D0	RMW ECC Error1 D1	RMW ECC Error0 D1
5F	DXC_ERROR_3 :B0							
	ECC UNC Error1 D0	ECC UNC Error0 D0	ECC UNC Error1 D1	ECC UNC Error0 D1	ECC ADR Error1 D0	ECC ADR Error0 D0	ECC ADR Error1 D1	ECC ADR Error0 D1

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Byte27 = 8E (CHK1) Byte40-7F Detail

(12) Byte28 = 64 (3/4)

	0	1	2	3	4	5	6	7
60	DXC_ERROR_4 :B3							
	RT UNCR Error	RT ADR Error	RT AGE PTY Error	RT ADRBUF PTY Error	RT ENC Error	RT FREE TIMER Error	Not used	Not used
61	DXC_ERROR_4 :B2							
	ZQ ENC Error	ZQ RCVPAT CNT Error	ZQ CYCLE CNT Error	Not used	Not used	Not used	Not used	Not used
62	DXC_ERROR_4 :B1							
	AC W UNCR Error	AC R UNCR Error	AC A UNCR Error	AC P UNCR Error	AC D UNCR Error	Not used	Not used	Not used
63	DXC_ERROR_4 :B0							
	AC W ADR Error	AC R ADR Error	AC A ADR Error	AC P ADR Error	AC D ADR Error	Not used	Not used	Not used
64	DXC_ERROR_5 :B3							
	Error INT	Not used	Not used	Not used	Not used	Not used	Not used	Not used
65	DXC_ERROR_5 :B2							
	USR Error1	USR Error0	Not used	Not used	Not used	Not used	Not used	Not used
66	DXC_ERROR_5 :B1							
	USR REFRDY	Not used	Not used	Not used	Not used	Not used	Not used	Not used
67	DXC_ERROR_5 :B0							
	TJCNT PTY Error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	DXC_CORE_DIMMERR_STR:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
69	DXC_CORE_DIMMERR_STR:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	DXC_CORE_DIMMERR_STR:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	DXC_CORE_DIMMERR_STR:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	DIMM Error1	DIMM Error0
6C	DXC_CORE_ERRF:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6D	DXC_CORE_ERRF:B2							
	Not used	Not used	TAPINC Error F	DQS INACTV F	REFI Error F[7]	REFI Error F[6]	REFI Error F[5]	REFI Error F[4]
6E	DXC_CORE_ERRF:B1							
	REFI Error F[3]	REFI Error F[2]	REFI Error F[1]	REFI Error F[0]	RTBLAC TMOVR F	CMD Parity Error F	OUTOFSP F	RNKSEL Parity Error F
6F	DXC_CORE_ERRF:B0							
	CTBL Parity Error F	RTBL Parity Error F	VLDLSTCK Error F	REG RD Parity Error F	REG WD Parity Error F	REG AD Parity Error F	WD Parity Error F	CTLIF Parity Error F

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Byte27 = 8E (CHK1) Byte40-7F Detail

(12) Byte28 = 64 (4/4)

	0	1	2	3	4	5	6	7
70	DXC_CORE_ERR:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
71	DXC_CORE_ERR:B2							
	Not used	Not used	TAPINC Error	DQS INACTV	REFI Error[7]	REFI Error[6]	REFI Error[5]	REFI Error[4]
72	DXC_CORE_ERR:B1							
	REFI Error[3]	REFI Error[2]	REFI Error[1]	REFI Error[0]	RTBLAC TMOVR	CMD Parity Error	OUTOFSP	RNKSEL Parity Error
73	DXC_CORE_ERR:B0							
	CTBL Parity Error	RTBL Parity Error	VLDLSTCK Error	REG RD Parity Error	REG WD Parity Error	REG AD Parity Error	WD Parity Error	CTLIF Parity Error
74	DXC_CORE_WDPERR_STR:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
75	DXC_CORE_WDPERR_STR:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	WD Parity Error L17	WD Parity Error L16
76	DXC_CORE_WDPERR_STR:B1							
	WD Parity Error L15	WD Parity Error L14	WD Parity Error L13	WD Parity Error L12	WD Parity Error L11	WD Parity Error L10	WD Parity Error L09	WD Parity Error L08
77	DXC_CORE_WDPERR_STR:B0							
	WD Parity Error L07	WD Parity Error L06	WD Parity Error L05	WD Parity Error L04	WD Parity Error L03	WD Parity Error L02	WD Parity Error L01	WD Parity Error L00
78	DXC_CORE_RNKSLPERR_STR:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
79	DXC_CORE_RNKSLPERR_STR:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	RNKSEL Parity Error L17	RNKSEL Parity Error L16
7A	DXC_CORE_RNKSLPERR_STR:B1							
	RNKSEL Parity Error L15	RNKSEL Parity Error L14	RNKSEL Parity Error L13	RNKSEL Parity Error L12	RNKSEL Parity Error L11	RNKSEL Parity Error L10	RNKSEL Parity Error L09	RNKSEL Parity Error L08
7B	DXC_CORE_RNKSLPERR_STR:B0							
	RNKSEL Parity Error L07	RNKSEL Parity Error L06	RNKSEL Parity Error L05	RNKSEL Parity Error L04	RNKSEL Parity Error L03	RNKSEL Parity Error L02	RNKSEL Parity Error L01	RNKSEL Parity Error L00
7C	DXC_CORE_DQSINACTV_STR:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7D	DXC_CORE_DQSINACTV_STR:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	DQS INACTV L17	DQS INACTV L16
7E	DXC_CORE_DQSINACTV_STR:B1							
	DQS INACTV L15	DQS INACTV L14	DQS INACTV L13	DQS INACTV L12	DQS INACTV L11	DQS INACTV L10	DQS INACTV L09	DQS INACTV L08
7F	DXC_CORE_DQSINACTV_STR:B0							
	DQS INACTV L07	DQS INACTV L06	DQS INACTV L05	DQS INACTV L04	DQS INACTV L03	DQS INACTV L02	DQS INACTV L01	DQS INACTV L00

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Byte27 = 8E (CHK1) Byte40-7F Detail

(13) Byte28 = 65 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(13) Byte28 = 65 (2/4)

	0	1	2	3	4	5	6	7
50	MPDMA_MD_ERR_ST32:B3							
	DMCTL SEQ Error	Not used	PRERCNT Parity Error	PID Parity Error	PRM W0 7 Parity Error	PRM W8 E Parity Error	STS W0 7 Parity Error	STSADR Parity Error
51	MPDMA_MD_ERR_ST32:B2							
	PFAREQID Parity Error	REQADR Parity Error	Not used	Not used	Not used	Not used	Not used	Not used
52	MPDMA_MD_ERR_ST32:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
53	MPDMA_MD_ERR_ST32:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	MPDMA_MD_ERR_ST36:B3							
	DMPC SEQ Error	PCRIF SEQ Error	SWIF R SEQ Error	TMR0 SEQ Error	TMR1 SEQ Error	TMR2 SEQ Error	TMR3 SEQ Error	PFADR W0 Parity Error
55	MPDMA_MD_ERR_ST36:B2							
	PFADR W1 Parity Error	PBDIFCNT Parity Error	PREWCNT Parity Error	PRMCNT Parity Error	HDRW3 Parity Error	TAG Parity Error	PRMT N HED Parity Error	REQ HED0 Parity Error
56	MPDMA_MD_ERR_ST36:B1							
	REQ HED1 Parity Error	REQ HED2 Parity Error	REQ HED3 Parity Error	PRERCNT Parity Error	PRDT W0 F Parity Error	Not used	Not used	Not used
57	MPDMA_MD_ERR_ST36:B0							
	TOCNT0 Parity Error	TOCNT1 Parity Error	TOCNT2 Parity Error	TOCNT3 Parity Error	Not used	Not used	Not used	Not used
58	MPDMA_MD_ERR_ST37:B3							
	PRMLRC Error	REQID CMP Error	CHEN Error	Not used	Not used	Not used	Not used	Not used
59	MPDMA_MD_ERR_ST37:B2							
	Not used	Not used	Not used	Not used	TIM OVR0	TIM OVR1	TIM OVR2	TIM OVR3
5A	MPDMA_MD_ERR_ST37:B1							
	SW TX ErrorSTS	Not used	Not used	NO HED HIT	Not used	WDCNT Parity Error	TOCNT TO Error	TOCNT Parity Error
5B	MPDMA_MD_ERR_ST37:B0							
	DT Parity Error	HLRC Error	DLRC Error	HED Parity Error	Not used	DLRCTIM Error	VLD Error	REQ Error
5C	MPDMA_MD_ERR_ST38:B3							
	DMSB SEQ Error	SBTIF SEQ Error	STSDIFCNT Parity Error	STSRCNT Parity Error	STSWCNT Parity Error	PC DT Parity Error	PC HED Parity Error	PC DLRC Parity Error
5D	MPDMA_MD_ERR_ST38:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5E	MPDMA_MD_ERR_ST38:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5F	MPDMA_MD_ERR_ST38:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = 8E (CHK1) Byte40-7F Detail

(13) Byte28 = 65 (3/4)

	0	1	2	3	4	5	6	7
60	MPDMA_MD_ERR_ST39:B3							
	ABT Error	TIF SEQ Error	Not used	Not used	Not used	Not used	Not used	Not used
61	MPDMA_MD_ERR_ST39:B2							
	Not used	Not used	Not used	Not used	WDCNT Parity Error	TOCNT TIMOUT Error	TOCNT Parity Error	DT Parity Error
62	MPDMA_MD_ERR_ST39:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
63	MPDMA_MD_ERR_ST39:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	RX ErrorSTS
64	MPDMA_MD_ERR_ST40:B3							
	DECENC Error	OLD IDGNT CM Parity Error	PFADR W01 Parity Error	Not used	Not used	Not used	Not used	Not used
65	MPDMA_MD_ERR_ST40:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	MPDMA_MD_ERR_ST40:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
67	MPDMA_MD_ERR_ST40:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	Reserved							
	Reserved							
69	Reserved							
	Reserved							
6A	Reserved							
	Reserved							
6B	Reserved							
	Reserved							
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(13) Byte28 = 65 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(14) Byte28 = 66 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(14) Byte28 = 66 (2/4)

	0	1	2	3	4	5	6	7
50	DMA_DM_ERR_ST32:B3							
	DMCTL SEQ Error	Not used	PRERCNT Parity Error	PID Parity Error	PRM W0 7 Parity Error	PRM W8 E Parity Error	STS W0 7 Parity Error	STSADR Parity Error
51	DMA_DM_ERR_ST32:B2							
	PFAREQID Parity Error	REQADR Parity Error	Not used	Not used	Not used	Not used	Not used	Not used
52	DMA_DM_ERR_ST32:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
53	DMA_DM_ERR_ST32:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	DMA_DM_ERR_ST33:B3							
	Not used	Not used	Not used	Not used	PRMLRC Error	REQID CMP Error	CHEN Error	MPN CMP Error
55	DMA_DM_ERR_ST33:B2							
	CPLD STS NOT SC	CPL STS NOT SC	Not used	CPL TIM OVR	Not used	Not used	Not used	Not used
56	DMA_DM_ERR_ST33:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
57	DMA_DM_ERR_ST33:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
58	DMA_DM_ERR_ST34:B3							
	IRREGU INF0							
59	DMA_DM_ERR_ST34:B2							
	IRREGU INF0							
5A	DMA_DM_ERR_ST34:B1							
	IRREGU INF0							
5B	DMA_DM_ERR_ST34:B0							
	IRREGU INF0							
5C	DMA_DM_ERR_ST35:B3							
	IRREGU INF1							
5D	DMA_DM_ERR_ST35:B2							
	IRREGU INF1							
5E	DMA_DM_ERR_ST35:B1							
	IRREGU INF1							
5F	DMA_DM_ERR_ST35:B0							
	IRREGU INF1							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(14) Byte28 = 66 (3/4)

	0	1	2	3	4	5	6	7
60	DMA_DM_ERR_ST36:B3							
	DMPC SEQ Error	PCRIF SEQ Error	SWIF R SEQ Error	TMR0 SEQ Error	TMR1 SEQ Error	TMR2 SEQ Error	TMR3 SEQ Error	PFADR W0 Parity Error
61	DMA_DM_ERR_ST36:B2							
	PFADR W1 Parity Error	PBDIFCNT Parity Error	PREWCNT Parity Error	PRMCNT Parity Error	HDRW3 Parity Error	TAG Parity Error	PRMT N HED Parity Error	REQ HED0 Parity Error
62	DMA_DM_ERR_ST36:B1							
	REQ HED1 Parity Error	REQ HED2 Parity Error	REQ HED3 Parity Error	PRERCNT Parity Error	PRDT W0 F Parity Error	Not used	Not used	Not used
63	DMA_DM_ERR_ST36:B0							
	TOCNT0 Parity Error	TOCNT1 Parity Error	TOCNT2 Parity Error	TOCNT3 Parity Error	Not used	Not used	Not used	Not used
64	DMA_DM_ERR_ST37:B3							
	PRMLRC Error	REQID CMP Error	CHEN Error	Not used	Not used	Not used	Not used	Not used
65	DMA_DM_ERR_ST37:B2							
	Not used	Not used	Not used	Not used	TIM OVR0	TIM OVR1	TIM OVR2	TIM OVR3
66	DMA_DM_ERR_ST37:B1							
	SW TX ErrorSTS	Not used	Not used	NO HED HIT	Not used	WDCNT Parity Error	TOCNT TO Error	TOCNT Parity Error
67	DMA_DM_ERR_ST37:B0							
	DT Parity Error	HLRC Error	DLRC Error	HED Parity Error	Not used	DLRCTIM Error	VLD Error	REQ Error
68	DMA_DM_ERR_ST38:B3							
	DMSB SEQ Error	SBTIF SEQ Error	STSDIFCNT Parity Error	STSRCNT Parity Error	STSWCNT Parity Error	PC DT Parity Error	PC HED Parity Error	PC DLRC Parity Error
69	DMA_DM_ERR_ST38:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	DMA_DM_ERR_ST38:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	DMA_DM_ERR_ST38:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6C	DMA_DM_ERR_ST39:B3							
	ABT Error	TIF SEQ Error	Not used	Not used	Not used	Not used	Not used	Not used
6D	DMA_DM_ERR_ST39:B2							
	Not used	Not used	Not used	Not used	WDCNT Parity Error	TOCNT TIMOUT Error	TOCNT Parity Error	DT Parity Error
6E	DMA_DM_ERR_ST39:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6F	DMA_DM_ERR_ST39:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	RX ErrorSTS

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Byte27 = 8E (CHK1) Byte40-7F Detail

(14) Byte28 = 66 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(15) Byte28 = 67 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(15) Byte28 = 67 (2/4)

	0	1	2	3	4	5	6	7
50	DRR_DM_ERR_ST32:B3							
	DMCTL SEQ Error	Not used	PRERCNT Parity Error	PID Parity Error	PRM W0 7 Parity Error	PRM W8 E Parity Error	STS W0 7 Parity Error	STSADR Parity Error
51	DRR_DM_ERR_ST32:B2							
	PFAREQID Parity Error	REQADR Parity Error	Not used	Not used	Not used	Not used	Not used	Not used
52	DRR_DM_ERR_ST32:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
53	DRR_DM_ERR_ST32:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	DRR_DM_ERR_ST33:B3							
	Not used	Not used	Not used	Not used	PRMLRC Error	REQID CMP Error	CHEN Error	MPN CMP Error
55	DRR_DM_ERR_ST33:B2							
	CPLD STS NOT SC	CPL STS NOT SC	Not used	CPL TIM OVR	Not used	Not used	Not used	Not used
56	DRR_DM_ERR_ST33:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
57	DRR_DM_ERR_ST33:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
58	DRR_DM_ERR_ST34:B3							
	IRREGU INF0							
59	DRR_DM_ERR_ST34:B2							
	IRREGU INF0							
5A	DRR_DM_ERR_ST34:B1							
	IRREGU INF0							
5B	DRR_DM_ERR_ST34:B0							
	IRREGU INF0							
5C	DRR_DM_ERR_ST35:B3							
	IRREGU INF1							
5D	DRR_DM_ERR_ST35:B2							
	IRREGU INF1							
5E	DRR_DM_ERR_ST35:B1							
	IRREGU INF1							
5F	DRR_DM_ERR_ST35:B0							
	IRREGU INF1							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(15) Byte28 = 67 (3/4)

	0	1	2	3	4	5	6	7
60	DRR_DM_ERR_ST36:B3							
	DMPC SEQ Error	PCRIF SEQ Error	SWIF R SEQ Error	TMR0 SEQ Error	TMR1 SEQ Error	TMR2 SEQ Error	TMR3 SEQ Error	PFADR W0 Parity Error
61	DRR_DM_ERR_ST36:B2							
	PFADR W1 Parity Error	PBDIFCNT Parity Error	PREWCNT Parity Error	PRMCNT Parity Error	HDRW3 Parity Error	TAG Parity Error	PRMT N HED Parity Error	REQ HED0 Parity Error
62	DRR_DM_ERR_ST36:B1							
	REQ HED1 Parity Error	REQ HED2 Parity Error	REQ HED3 Parity Error	PRERCNT Parity Error	PRDT W0 F Parity Error	Not used	Not used	Not used
63	DRR_DM_ERR_ST36:B0							
	TOCNT0 Parity Error	TOCNT1 Parity Error	TOCNT2 Parity Error	TOCNT3 Parity Error	Not used	Not used	Not used	Not used
64	DRR_DM_ERR_ST37:B3							
	PRMLRC Error	REQID CMP Error	CHEN Error	Not used	Not used	Not used	Not used	Not used
65	DRR_DM_ERR_ST37:B2							
	Not used	Not used	Not used	Not used	TIM OVR0	TIM OVR1	TIM OVR2	TIM OVR3
66	DRR_DM_ERR_ST37:B1							
	SW TX ErrorSTS	Not used	Not used	NO HED HIT	Not used	WDCNT Parity Error	TOCNT TO Error	TOCNT Parity Error
67	DRR_DM_ERR_ST37:B0							
	DT Parity Error	HLRC Error	DLRC Error	HED Parity Error	Not used	DLRCTIM Error	VLD Error	REQ Error
68	DRR_DM_ERR_ST38:B3							
	DMSB SEQ Error	SBTIF SEQ Error	STSDIFCNT Parity Error	STSRCNT Parity Error	STSWCNT Parity Error	PC DT Parity Error	PC HED Parity Error	PC DLRC Parity Error
69	DRR_DM_ERR_ST38:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	DRR_DM_ERR_ST38:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	DRR_DM_ERR_ST38:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6C	DRR_DM_ERR_ST39:B3							
	ABT Error	TIF SEQ Error	Not used	Not used	Not used	Not used	Not used	Not used
6D	DRR_DM_ERR_ST39:B2							
	Not used	Not used	Not used	Not used	WDCNT Parity Error	TOCNT TIMOUT Error	TOCNT Parity Error	DT Parity Error
6E	DRR_DM_ERR_ST39:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6F	DRR_DM_ERR_ST39:B0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	RX ErrorSTS

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Byte27 = 8E (CHK1) Byte40-7F Detail

(15) Byte28 = 67 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(16) Byte28 = 68 (1/4)

	0	1	2	3	4	5	6	7
40	INT0_INT_STATUS0:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	INT0_INT_STATUS0:B2							
	Not used	Not used	Not used	INT INT CHK1B	Not used	INT FDMA4 CHK1B	INT LRP4STOP CHK1B	INT LRP4 CHK1B
42	INT0_INT_STATUS0:B1							
	Not used	INT FDMA3 CHK1B	INT LRP3STOP CHK1B	INT LRP3 CHK1B	Not used	INT FDMA2 CHK1B	INT LRP2STOP CHK1B	INT LRP2 CHK1B
43	INT0_INT_STATUS0:B0							
	Not used	INT FDMA1 CHK1B	INT LRP1STOP CHK1B	INT LRP1 CHK1B	Not used	INT FDMA0 CHK1B	INT LRP0STOP CHK1B	INT LRP0 CHK1B
44	INT0_INT_STATUS1:B3							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	INT SWIF CHK1B
45	INT0_INT_STATUS1:B2							
	Not used	Not used	INT BARBREG CHK1B	INT BARB CHK1B	INT IARB1REG CHK1B	INT IARB1 CHK1B	INT IARB0REG CHK1B	INT IARB0 CHK1B
46	INT0_INT_STATUS1:B1							
	INT EARB1REG CHK1B	INT EARB1 CHK1B	INT EARB0REG CHK1B	INT EARB0 CHK1B	INT IXARB1REG CHK1B	INT IXARB1 CHK1B	INT IXARB0REG CHK1B	INT IXARB0 CHK1B
47	INT0_INT_STATUS1:B0							
	INT PARB3REG CHK1B	INT PARB3 CHK1B	INT PARB2REG CHK1B	INT PARB2 CHK1B	INT PARB1REG CHK1B	INT PARB1 CHK1B	INT PARB0REG CHK1B	INT PARB0 CHK1B
48	INT0_INT_STATUS2:B3							
	Not used	Not used	Not used	INT XD CHK1B	Not used	Not used	Not used	Not used
49	INT0_INT_STATUS2:B2							
	INT DXC3 CHK1B	INT DXC2 CHK1B	INT DXC1 CHK1B	INT DXC0 CHK1B	INT DXA3 CHK1B	INT DXA2 CHK1B	INT DXA1 CHK1B	INT DXA0 CHK1B
4A	INT0_INT_STATUS2:B1							
	INT DRR3 CHK1B	INT DRR2 CHK1B	INT DRR1 CHK1B	INT DRR0 CHK1B	INT MPDMA1 CHK1B	INT MPDMA0 CHK1B	INT DMAMB1 CHK1B	INT DMAMB0 CHK1B
4B	INT0_INT_STATUS2:B0							
	Not used	Not used	INT DMA5 CHK1B	INT DMA4 CHK1B	INT DMA3 CHK1B	INT DMA2 CHK1B	INT DMA1 CHK1B	INT DMA0 CHK1B
4C	INT0_INT_STATUS3:B3							
	Not used	Not used	Not used	Not used	INT RGARB CHK1B	INT REG2 CHK1B	INT REG1 CHK1B	INT REG0 CHK1B
4D	INT0_INT_STATUS3:B2							
	Not used	Not used	Not used	INT FMT CHK1B	Not used	INT SHC CHK1B	INT BRAM CHK1B	INT BCOM CHK1B
4E	INT0_INT_STATUS3:B1							
	Not used	Not used	Not used	INT SMC CHK1B	Not used	Not used	Not used	INT SMBUSM8 CHK1B
4F	INT0_INT_STATUS3:B0							
	INT SMBUSM7 CHK1B	INT SMBUSM6 CHK1B	INT SMBUSM5 CHK1B	INT SMBUSM4 CHK1B	INT SMBUSM3 CHK1B	INT SMBUSM2 CHK1B	INT SMBUSM1 CHK1B	INT SMBUSM0 CHK1B

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Byte27 = 8E (CHK1) Byte40-7F Detail

(16) Byte28 = 68 (2/4)

	0	1	2	3	4	5	6	7
50	XARB_RX_PCK_ERR0:B3							
	Not used	RXSEQ0 QENC Error	RXSEQ0 Q Parity Error	PCI ECC DETECT	RXBLK ECRC Error	Not used	RXHDBUF WTPT Parity Error	Not used
51	XARB_RX_PCK_ERR0:B2							
	Not used	RXNDBUF WTPT Parity Error	RXHDIX Parity Error	Not used	RXDT WTADR Parity Error	RXSEQ0 TCNT Parity Error	RXNHIX Parity Error	RCRC CMP Parity Error
52	XARB_RX_PCK_ERR0:B1							
	P2C SEQ DEC Error	P2C SEQ ENC Error	P2C SEQ Parity Error	P2C CNT Parity Error	RX Parity Error	RXNDBUF ING Parity Error	RXDTIX DTCMP Parity Error	RXDTIX WADR Parity Error
53	XARB_RX_PCK_ERR0:B0							
	TAGxTMR SEQ Parity Error	TAGxTMR ENC Error	TAGxTMR GP Error	BACNTGP Error	RX PCK CHK4TOP	RX PCK CHK1TOP	RX PCK WRN TOP	Not used
54	XARB_TX_PCK_ERR0:B3							
	TXHD RDPT Parity Error	TXNH RDPT Parity Error	TXNH WTPT Parity Error	TXND RDPT Parity Error	BETY Error	CDETY Error	CHETY Error	NDETY Error
55	XARB_TX_PCK_ERR0:B2							
	NHETY FRC Error	PDETY FRC Error	PHETY FRC Error	QETY FRC Error	LINK Error	TXSEQ0 QE Error	TXSEQ0 Q Parity Error	P2C SEQ D Error
56	XARB_TX_PCK_ERR0:B1							
	P2C SEQ E Error	P2C SEQ Parity Error	TXDT RDADR Parity Error	P2C CNT Parity Error	TXHDOX Parity Error	TXDTOX Parity Error	TXNHIX Parity Error	TXNHOX Parity Error
57	XARB_TX_PCK_ERR0:B0							
	LINK Error	TXNDBUF WTPT Parity Error	STOPREQ Parity Error	TX ErrorGP Error	TXSEQ0 TCNT Parity Error	Not used	XFBCNTGP Error	XFQCNT Parity Error
58	XARB_TX_PCK_ERR1:B3							
	ICNT Parity Error	TXHDDT A Parity Error	TXHDDT E Parity Error	Not used	ICNT NP Parity Error	NPHDBUF Parity Error	TXDTBUF Parity Error	TXNDBUF Parity Error
59	XARB_TX_PCK_ERR1:B2							
	CHCNT Parity Error	NHCNT Parity Error	PHCNT Parity Error	CDCNT Parity Error	NDCNT Parity Error	PDCNT Parity Error	TXDTBUF ADR Error	TXDTBUF UNC Error
5A	XARB_TX_PCK_ERR1:B1							
	FCTMR SEQ Parity Error	FCTMR SEQ ENC Error	FCTMRGP Error	FCTMR TO Error	Not used	Not used	Not used	Not used
5B	XARB_TX_PCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX PCK CHK4TOP	TX PCK CHK1TOP	TX PCK WRN TOP	Not used
5C	XARB_RX_UCK_ERR0:B3							
	RXHDBUF RDPT Parity Error	RXDTBUF ADR Error	RXDTBUF UNCOR	RXNHBUF RDPT Parity Error	RXNDBUF RDPT Parity Error	RXDT RDADR Parity Error	RXHDOX Parity Error	WCRC CMP Parity Error
5D	XARB_RX_UCK_ERR0:B2							
	RXNHOX Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error	C2P CNT Parity Error	SWTX DEC Error	SWTX DLRC G Error
5E	XARB_RX_UCK_ERR0:B1							
	SWTX DT LGP Error	SWTX ENC Error	SWTX HLRC G Error	Not used	SWTX TOCNTGP Error	SWTX TOCNT TO	SWTX WDCNTGP Error	Not used
5F	XARB_RX_UCK_ERR0:B0							
	ARBSEQ QDEC Error	ARBSEQ QENC Error	ARBSEQ Q Parity Error	RXNHBUF WTPT Parity Error	MRG ECC ADR Error	MRG ECC UNCOR	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error

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Byte27 = 8E (CHK1) Byte40-7F Detail

(16) Byte28 = 68 (3/4)

	0	1	2	3	4	5	6	7
60	XARB_RX_UCK_ERR1:B3							
	MRGBUF DTCNT Parity Error	MRGBUF TMR Parity Error	XFCNTGP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	RXNHBUF OVER	Not used	Not used
61	XARB_RX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
62	XARB_RX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
63	XARB_RX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	RX UCK CHK4TOP	RX UCK CHK1TOP	RX UCK WRN TOP	Not used
64	XARB_TX_UCK_ERR0:B3							
	SWRX DEC Error	SWRX DLRCTIM G Error	SWRX DLRC G Error	SWRX ENC Error	SWRX HLRC G Error	SWRX SW DTGP Error	SWRX SW VLD G Error	SWRX TOCNTGP Error
65	XARB_TX_UCK_ERR0:B2							
	SWRX TOCNT TO	SWRX TX Error G Error	SWRX WDCNTGP Error	TXHDBUF WTPT Parity Error	Not used	C2P SEQ DEC Error	C2P SEQ ENC Error	C2P SEQ Parity Error
66	XARB_TX_UCK_ERR0:B1							
	C2P CNT Parity Error	TXDTBUF WTADR Parity Error	TXHDIX Parity Error	Not used	TXNHCNT Parity Error	SWRX REQOFF Error	SWRX SW HD Parity Error	DATCNT Parity Error
67	XARB_TX_UCK_ERR0:B0							
	DIV ECC ADR Error	DIV ECC CRCT Error	DIV ECC UNCOR	CPLSEQ QDEC Error	CPLSEQ QENC Error	CPLSEQ Q Parity Error	MRGBUF WTADR Parity Error	MRGBUF RDADR Parity Error
68	XARB_TX_UCK_ERR1:B3							
	CDICNT Parity Error	CPLSEQ DTCNT Parity Error	XFCNTGP Error	TKCNT1 Parity Error	TKCNT2 Parity Error	MIC CHK1 Error	TXDTIX DTCMP Parity Error	TXDTIX WACMP Parity Error
69	XARB_TX_UCK_ERR1:B2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	XARB_TX_UCK_ERR1:B1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6B	XARB_TX_UCK_ERR1:B0							
	Not used	Not used	Not used	Not used	TX UCK CHK4TOP	TX UCK CHK1TOP	TX UCK WRN TOP	Not used
6C	Reserved							
	Reserved							
6D	Reserved							
	Reserved							
6E	Reserved							
	Reserved							
6F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(16) Byte28 = 68 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	Reserved							
71	Reserved							
	Reserved							
72	Reserved							
	Reserved							
73	Reserved							
	Reserved							
74	Reserved							
	Reserved							
75	Reserved							
	Reserved							
76	Reserved							
	Reserved							
77	Reserved							
	Reserved							
78	Reserved							
	Reserved							
79	Reserved							
	Reserved							
7A	Reserved							
	Reserved							
7B	Reserved							
	Reserved							
7C	Reserved							
	Reserved							
7D	Reserved							
	Reserved							
7E	Reserved							
	Reserved							
7F	Reserved							
	Reserved							

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Byte27 = 8E (CHK1) Byte40-7F Detail

(17) Byte28 = 80/81 (1/3)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT FORMAT NUMBER							
	‘08’							
41								
	0	0	0	0	0	0	0	0
42	I_STATE0							
	I_STATE 07	I_STATE 06	I_STATE 05	I_STATE 04	I_STATE 03	I_STATE 02	I_STATE 01	I_STATE 00
43	I_STATE1							
	I_STATE 17	I_STATE 16	I_STATE 15	I_STATE 14	I_STATE 13	I_STATE 12	I_STATE 11	I_STATE 10
44	GFERRST:B3							
	GFER _31	GFER _30	GFER _29	GFER _28	GFER _27	GFER _26	GFER _31	GFER _30
45	GFERRST:B2							
	GFER _23	GFER _22	GFER _21	GFER _20	GFER _19	GFER _18	GFER _23	GFER _22
46	GFERRST:B1							
	GFER _15	GFER _14	GFER _13	GFER _12	GFER _11	GFER _10	GFER _15	GFER _14
47	GFERRST:B0							
	GFER _07	GFER _06	GFER _05	GFER _04	GFER _03	GFER _02	GFER _07	GFER _06
48	GNERRST:B3							
	GNER _31	GNER _30	GNER _29	GNER _28	GNER _27	GNER _26	GNER _25	GNER _24
49	GNERRST:B2							
	GNER _23	GNER _22	GNER _21	GNER _20	GNER _19	GNER _18	GNER _17	GNER _16
4A	GNERRST:B1							
	GNER _15	GNER _14	GNER _13	GNER _12	GNER _11	GNER _10	GNER _09	GNER _08
4B	GNERRST:B0							
	GNER _07	GNER _06	GNER _05	GNER _04	GNER _03	GNER _02	GNER _01	GNER _00
4C	IA32_MC0_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4D	IA32_MC1_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4E	IA32_MC2_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
4F	IA32_MC3_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
50	IA32_MC4_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
51	IA32_MC5_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
52	IA32_MC6_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
53	IA32_MC9_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag

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Byte27 = 8E (CHK1) Byte40-7F Detail

(17) Byte28 = 80/81 (2/3)

	0	1	2	3	4	5	6	7
54	IA32_MC10_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
55	IA32_MC11_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
56	IA32_MC12_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
57	IA32_MC13_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
58	IA32_MC14_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
59	IA32_MC15_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5A	IA32_MC16_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5B	IA32_MC17_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5C	IA32_MC18_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5D	IA32_MC19_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
5E								
	0	0	0	0	0	0	0	0
5F								
	0	0	0	0	0	0	0	0
60	IA32_MCi_STATUS B7							
	VAL	OVER	UC	Error enabled	MISCV	ADDRV	PCC	Signaling Flag
61	IA32_MCi_STATUS B6							
	AR	Th_Err_Sts 1	Th_Err_Sts 0	Corr_Err_Cnt 14	Corr_Err_Cnt 13	Corr_Err_Cnt 12	Corr_Err_Cnt 11	Corr_Err_Cnt 10
62	IA32_MCi_STATUS B5							
	Corr_Err_Cnt 9	Corr_Err_Cnt 8	Corr_Err_Cnt 7	Corr_Err_Cnt 6	Corr_Err_Cnt 5	Corr_Err_Cnt 4	Corr_Err_Cnt 3	Corr_Err_Cnt 2
63	IA32_MCi_STATUS B4							
	Corr_Err_Cnt 1	Corr_Err_Cnt 0	Other_Info 5	Other_Info 4	Other_Info 3	Other_Info 2	Other_Info 1	Other_Info 0
64	IA32_MCi_STATUS B3							
	MSCOD 15	MSCOD 14	MSCOD 13	MSCOD 12	MSCOD 11	MSCOD 10	MSCOD 9	MSCOD 8
65	IA32_MCi_STATUS B2							
	MSCOD 7	MSCOD 6	MSCOD 5	MSCOD 4	MSCOD 3	MSCOD 2	MSCOD 1	MSCOD 0
66	IA32_MCi_STATUS B1							
	MCACOD 15	MCACOD 14	MCACOD 13	MCACOD 12	MCACOD 11	MCACOD 10	MCACOD 9	MCACOD 8
67	IA32_MCi_STATUS B0							
	MCACOD 7	MCACOD 6	MCACOD 5	MCACOD 4	MCACOD 3	MCACOD 2	MCACOD 1	MCACOD 0

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Byte27 = 8E (CHK1) Byte40-7F Detail

(17) Byte28 = 80/81 (3/3)

	0	1	2	3	4	5	6	7
68	IA32_MCi_ADDR B7							
	0	0	0	0	0	0	0	0
69	IA32_MCi_ADDR B6							
	0	0	0	0	0	0	0	0
6A	IA32_MCi_ADDR B5							
	0	0	MCEADR 45	MCEADR 44	MCEADR 43	MCEADR 42	MCEADR 41	MCEADR 40
6B	IA32_MCi_ADDR B4							
	MCEADR 39	MCEADR 38	MCEADR 37	MCEADR 36	MCEADR 35	MCEADR 34	MCEADR 33	MCEADR 32
6C	IA32_MCi_ADDR B3							
	MCEADR 31	MCEADR 30	MCEADR 29	MCEADR 28	MCEADR 27	MCEADR 26	MCEADR 25	MCEADR 24
6D	IA32_MCi_ADDR B2							
	MCEADR 23	MCEADR 22	MCEADR 21	MCEADR 20	MCEADR 19	MCEADR 18	MCEADR 17	MCEADR 16
6E	IA32_MCi_ADDR B1							
	MCEADR 15	MCEADR 14	MCEADR 13	MCEADR 12	MCEADR 11	MCEADR 10	MCEADR 9	MCEADR 8
6F	IA32_MCi_ADDR B0							
	MCEADR 7	MCEADR 6	MCEADR 5	MCEADR 4	MCEADR 3	MCEADR 2	MCEADR 1	MCEADR 0
70	IA32_MCi_MISK B7							
	Info 54	Info 53	Info 52	Info 51	Info 50	Info 49	Info 48	Info 47
71	IA32_MCi_MISK B6							
	Info 46	Info 45	Info 44	Info 43	Info 42	Info 41	Info 40	Info 39
72	IA32_MCi_MISK B5							
	Info 38	Info 37	Info 36	Info 35	Info 34	Info 33	Info 32	Info 31
73	IA32_MCi_MISK B4							
	Info 30	Info 29	Info 28	Info 27	Info 26	Info 25	Info 24	Info 23
74	IA32_MCi_MISK B3							
	Info 22	Info 21	Info 20	Info 19	Info 18	Info 17	Info 16	Info 15
75	IA32_MCi_MISK B2							
	Info 14	Info 13	Info 12	Info 11	Info 10	Info 9	Info 8	Info 7
76	IA32_MCi_MISK 1							
	Info 6	Info 5	Info 4	Info 3	Info 2	Info 1	Info 0	ADRMD 2
77	IA32_MCi_MISK B0							
	ADRMD 1	ADRMD 0	Rec_Err_LSB 5	Rec_Err_LSB 4	Rec_Err_LSB 3	Rec_Err_LSB 2	Rec_Err_LSB 1	Rec_Err_LSB 0
78								
	0	0	0	0	0	0	0	0
79								
	0	0	0	0	0	0	0	0
7A								
	0	0	0	0	0	0	0	0
7B								
	0	0	0	0	0	0	0	0
7C								
	0	0	0	0	0	0	0	0
7D								
	0	0	0	0	0	0	0	0
7E								
	0	0	0	0	0	0	0	0
7F								
	0	0	0	0	0	0	0	0

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Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (WCHK1)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID (*1)							
08	Processor ID (*1)							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Not used							
|								
31								
32	Module ID							
33	Routine ID							
34	Package number				Message code (x‘0’)			
35	SSID (low) of self storage system							
36	Symptom code (x‘FF8E’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’) (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								
40	Not used							
|								
7F								

*1: Failed processor number for WCHK1

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Byte27 = 8E & Byte34:bit4-7=5 (CHK1B Reset) (1/3)
Byte27 = 81 & Byte34:bit4-7=3 (CHK3 Reset) (1/3)
Byte27 = 84 & Byte34:bit4-7=5 (CHK4 Reset) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘E’ or x‘1’ or x‘4’)			
28	Related failure internal SSB log number							
29								
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Old PSW (interrupted address)							
2D								
2E								
2F								
30	Internal SSB log number (reset)							
31								
32	Related reset detailed log number							
33								
34	Package number				Message code (x‘5’ or x‘3’)			
35	SSID (low) of self storage system							
36	Symptom code (x‘FF8E’)							
37								

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Byte27 = 8E & Byte34:bit4-7=5 (CHK1B Reset) (2/3)
Byte27 = 81 & Byte34:bit4-7=3 (CHK3 Reset) (2/3)
Byte27 = 84 & Byte34:bit4-7=5 (CHK4 Reset) (2/3)

	0	1	2	3	4	5	6	7
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 8E & Byte34:bit4-7=5 (CHK1B Reset) (3/3)
Byte27 = 81 & Byte34:bit4-7=3 (CHK3 Reset) (3/3)
Byte27 = 84 & Byte34:bit4-7=5 (CHK4 Reset) (3/3)

	0	1	2	3	4	5	6	7
40		Not used (x‘00’)						
41		Not used (x‘00’)						
42		Initialize interface information (rstkindc)						
43		Initialize interface information (inidcodec)						
44		Reset type code (rstkindc)						
45		Reset type code (rstkindoldc)						
46		1st reset type code (firstkindc)						
47		Reset SSB type code (ssbkindc)						
48		Interrupt task code (inttaskc)						
49		Self CHK1A difference code (genchklac)						
4A		Multi reset type code (rstmultics)						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number (from LCT)						
55								
56		Current LPN number						
57								
58		Initiation cause code (from LCT)						
59								
5A		Command interface (from LCT)						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (from LCT)						
5F								
60								
61		wchklmpbitmap (from LCT)						
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved (x‘00’)						
6F								
70		DCN (wldcn11)						
|								
73								
74		DCN (wldcn21)						
|								
77								
78		DKC task head address						
|								
7B								
7C		SLV-DCN (slvdcnr)						
|								
7F								

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Byte27 = 8E & Byte34:bit4-7=6 (DKC Internal Reset) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Old PSW (interruputed address)							
2D								
2E								
2F								
30	Internal SSB log number (reset)							
31								
32	Related reset detailed log number							
33								
34	Package number				Message code (x‘6’)			
35	SSID (low) of self storage system							
36	Symptom code (x‘FF8E’)							
37	(This information is not fixed until DKC reports SSB to HOST.)							

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Byte27 = 8E & Byte34:bit4-7=6 (DKC Internal Reset) (2/3)

	0	1	2	3	4	5	6	7
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 8E & Byte34:bit4-7=6 (DKC Internal Reset) (3/3)

	0	1	2	3	4	5	6	7
40		Not used (x‘00’)						
41		Not used (x‘00’)						
42		Initialize interface information (rstkindc)						
43		Initialize interface information (inidcodec)						
44		Reset type code (rstkindc)						
45		Reset type code (rstkindoldc)						
46		1st reset type code (firstkindc)						
47		Reset SSB type code (ssbkindc)						
48		Interrupt task code (inttaskc)						
49		Self CHK1A difference code (genchklac)						
4A		Multi reset type code (rstmultics)						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number (from LCT)						
55								
56		Current LPN number						
57								
58		Initiation cause code (from LCT)						
59								
5A		Command interface (from LCT)						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (from LCT)						
5F								
60								
61		wchklmpbitmap (from LCT)						
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved (x‘00’)						
6F								
70		DCN (wldcn11)						
|								
73								
74		DCN (wldcn21)						
|								
77								
78		DKC task head address						
|								
7B								
7C		SLV-DCN (slvdcnr)						
|								
7F								

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Byte27 = 8E & Byte34:bit4-7=8 (Force Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format(x‘8’)				Message (x‘E’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Old PSW (interrupted address)							
2D								
2E								
2F								
30	Internal SSB log number (reset)							
31								
32	Related reset detailed log							
33								
34	Package number				Message code (x‘8’)			
35	SSID (low) of self storage system							
36	Symptom code (x‘FF8E’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 8E & Byte34:bit4-7=8 (Force Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used (x‘00’)							
41	Not used (x‘00’)							
42	Initialize interface information (rstkindc)							
43	Initialize interface information (inidcodec)							
44	Reset type code (rstkindc)							
45	Reset type code (rstkindoldc)							
46	1st reset type code (firstkindc)							
47	Reset SSB type code (ssbkindc)							
48	Interrupt task code (inttaskc)							
49	Self CHK1A difference code (genchklac)							
4A	Multi reset type code (rstmultics)							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted operation code							
51								
52								
53								
54	Current LDEV number (from LCT)							
55								
56	Current LPN							
57								
58	Initiation cause code (from LCT)							
59								
5A	Command interface (from LCT)							
5B	DSB (from LCT)							
5C	sys status							
5D	REQ ID (from LCT)							
5E	JCB ID (from LCT)							
5F								
60	wchklmpbitmap (from LCT)							
61								
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved (x‘00’)							
6F								
70	DCN (wldcn11)							
|								
73								
74	DCN (wldcn21)							
|								
77								
78	DKC task head address							
|								
7B								
7C	SLV-DCN (slvdcnr)							
|								
7F								

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Byte27 = 8E & Byte34:bit4-7=9 (Logical Inconsistency Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (x‘00’)							
29								
2A								
2B								
2C	Old PSW (interrupted address)							
2D								
2E								
2F								
30	Internal SSB log number (reset)							
31								
32	Related reset detailed log							
33								
34	Package number				Message code (x‘9’)			
35	SSID (low) of self storage system							
36	Symptom code (x‘FF8E’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte27 = 8E & Byte34:bit4-7=9 (Logical Inconsistency Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used (x‘00’)							
41	Not used (x‘00’)							
42	Initialize interface information (rstkindc)							
43	Initialize interface information (inidcodec)							
44	Reset type code (rstkindc)							
45	Reset type code (rstkindoldc)							
46	1st reset type code (firstkindc)							
47	Reset SSB type code (ssbkindc)							
48	Interrupt task code (inttaskc)							
49	Self CHK1A difference code (genchklac)							
4A	Multi reset type code (rstmultics)							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted operation code							
51								
52								
53								
54	Current LDEV number (from LCT)							
55								
56	Current LPN							
57								
58	Initiation cause code (from LCT)							
59								
5A	Command interface (from LCT)							
5B	DSB (from LCT)							
5C	sys status							
5D	REQ ID (from LCT)							
5E	JCB ID (from LCT)							
5F								
60	wchklmpbitmap (from LCT)							
61								
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved (x‘00’)							
6F								
70	DCN (wldcn11)							
73								
74	DCN (wldcn21)							
77								
78	DKC task head address							
7B								
7C	SLV-DCN (slvdcnr)							
7F								

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Byte27 = 8F (Logical Inconsistency) (1/2)

	0	1	2	3	4	5	6	7
00 – 05	Time stamp							
06	Format Message							
07	Processor ID							
08 – 09	System error code							
0A – 0B	JCB#							
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12 – 13	LDEV# LOW (LDEV# IN LOGICAL DKC)							
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16 – 17	Internal SSB log number							
18 – 19	Related failure log number							
1A – 1B	Related SIM log number							
1C – 1D	Related SSB log number							
1E	Reserved							
1F	SCB							
20 – 26	Reserved							
27	Format (x‘8’)				Message (x‘F’)			
28	Module ID							
29	Routine ID							
2A – 33	Error information							
34	Package number				Message code (x‘00’)			
35	SSID (low) of self storage system							
36 – 37	Symptom code (x‘FF8E’)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A – 3B	Configuration information							
3C – 3F	Reserved							

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Byte27 = 8F (Logical Inconsistency) (2/2)

	0	1	2	3	4	5	6	7
40								
41		Error information						
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

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Byte27 = 9F (Trace data/Log data) (1/2)

	0	1	2	3	4	5	6	7
00 – 05	Time stamp							
06	Format Message							
07	Processor ID							
08 – 09	System error code							
0A – 0B	JCB#							
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12 – 13	LDEV# LOW (LDEV# IN LOGICAL DKC)							
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16 – 17	Internal SSB log number							
18 – 19	Related failure log number							
1A – 1B	Related SIM log number							
1C – 1D	Related SSB log number							
1E	Reserved							
1F	SCB							
20 – 26	Reserved							
27	Format (x‘9’)				Message (x‘F’)			
28	Module ID (*1)							
29	Routine ID (*1)							
2A – 33	Error information							
34	Package number				Message code (x‘00’)			
35	SSID (low) of self storage system							
36 – 37	Symptom code (x‘FF9F’)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A – 3B	Configuration information							
3C – 3F	Reserved							

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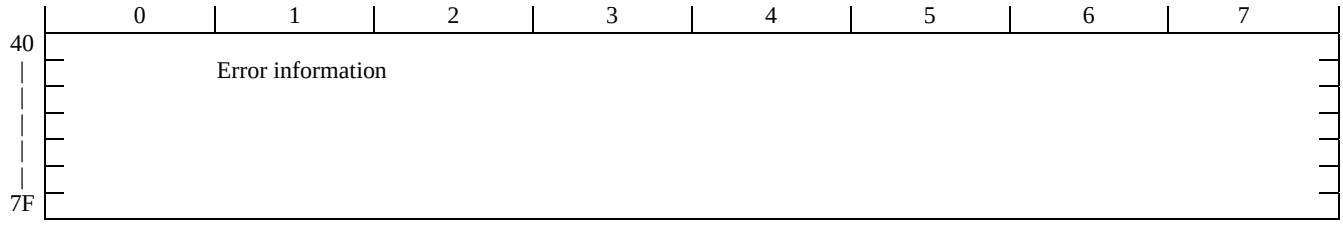
Byte27 = 9F (Trace data/Log data) (2/2)



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*1: In case of Mode 449 ON at the primary storage system of UR, if the secondary storage system is powered off or the path between primary and secondary storage system is blocked, error code x‘DB00’ might be displayed on primary storage system.
These error codes, which are generated when the communication between primary and secondary storage system fails, doesn’t indicate any failures.
Please ignore them.

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Byte27 = EC (Environment Monitor Detected Failure : Controller Environment Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘E’)				Message (x‘C’)			
28	Error detection code (*1)							
29	Error component code (*2)							
2A	Error reason code (*3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	Package number (invalid)				Message code (invalid)			
35	SSID (low) of self storage system (invalid)							
36	Symptom code (x‘FFEC’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information (invalid)							
3B								
3C	Reserved							
|								
3F								

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Byte27 = EC (Environment Monitor Detected Failure : Controller Environment Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code (*1)							
41	Error Component Code (*2)							
42	Error Reason Code (*3)							
43	Not used							
7F								

*1: Error Detection Code

Code	Detection
10	MPB1
20	MPB2
30	MAIN1
40	MAIN2
00	Others

*2: Error Component Code

Code	Component
10	MN1
11	MN2
12	SH1
13	SH2
A3	Others

*3: Error Reason Code (1/2)

Code	Reason
10	External temperature alarm.
11	External high temperature warning.
12	External low temperature warning.
13	Temperature abnormality warning.
14	Temperature abnormality.
20	Injustice DC voltage control.
40	DKCPS1 warning.
41	DKCPS2 warning.
70	DKCFAN warning. (DKCFAN10/12/20/22)
71	DKCFAN warning. (DKCFAN11/13/21/23)
85	SVP RAS Switch#1 remains.
A2	External temperature disagreement.
A5	PSOFFREQ I/F disagreement.
A6	PSOFFOK I/F disagreement.
A7	SYSON output disagreement.
A8	DKCPS1 warning disagreement.
A9	DKCPS2 warning disagreement.

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*3: Error Reason Code (2/2)

Code	Reason
AA	PS Status disagreement.
AF	MN error.
B1	MN communication error.
C0	Injustice CEMODE.
C1	Injustice CEDT.
D0	Battery warning.
D1	Battery charge EMPTY.
D2	CFM warning.
D3	Warning for forcible volatile mode.
D4	CM Backup mounting warning.

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Byte27 = EE (Environment Monitor Detected DB Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	Reserved
0F	SEMI-SYNC	RCU SIM	PORT#VLD	Reserved				
10	JCB ID							
11	LDEV# HIGH (LOGICAL DKC#)							
12	LDEV# LOW (LDEV# IN LOGICAL DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘E’)				Message (x‘E’)			
28	Error Detection code (*1)							
29	Error Component code (*2)							
2A	Error Reason code (*3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	Package number (invalid)				Message code (invalid)			
35	SSID (low) of self storage system (invalid)							
36	Symptom code (x‘FFEE’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information (invalid)							
3B								
3C	Reserved							
|								
3F								

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Byte27 = EE (Environment Monitor Detected DB Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code (*1)							
41	Error Component Code (*2)							
42	Error Reason code (*3)							
43	Not used							
7F								

*1: Error Detection Code

Code	Detection	
80	ENCxx-1	xx: 0/4/8/12/16/20/24/28/32/36/40/44
82	ENCxx-2	
90	ENCxx-1	xx: 1/5/9/13/17/21/25/29/33/37/41/45
92	ENCxx-2	
A0	ENCxx-1	xx: 3/6/10/14/18/22/26/30/34/38/42/46
A2	ENCxx-2	
B0	ENCxx-1	xx: 4/7/11/15/19/23/27/31/35/39/43/47
B2	ENCxx-2	

*2: Error Component Code

Code	Detection	Code	Detection	Code	Detection
00	DB-0	16	DB-16	32	DB-32
01	DB-1	17	DB-17	33	DB-33
02	DB-2	18	DB-18	34	DB-34
03	DB-3	19	DB-19	35	DB-35
04	DB-4	20	DB-20	36	DB-36
05	DB-5	21	DB-21	37	DB-37
06	DB-6	22	DB-22	38	DB-38
07	DB-7	23	DB-23	39	DB-39
08	DB-8	24	DB-24	40	DB-40
09	DB-9	25	DB-25	41	DB-41
10	DB-10	26	DB-26	42	DB-42
11	DB-11	27	DB-27	43	DB-43
12	DB-12	28	DB-28	44	DB-44
13	DB-13	29	DB-29	45	DB-45
14	DB-14	30	DB-30	46	DB-46
15	DB-15	31	DB-31	47	DB-47

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*3: Error Reason Code

Code	Reason
50	DBPS error. (DBPSxx-1)
51	DBPS error. (DBPSxx-2)
60	DBPS AC input error. (DBPSxx-1)
61	DBPS AC input error. (DBPSxx-1)
70	I2C#0 error.
71	I2C#1 error.
72	I2C#2 error.
80	Expander error.
90	I2C#0 access error.
91	I2C#1 access error.
92	I2C#2 access error.
A0	CPLD access retry error.
A1	I2C access retry error.
B0	SXP error, I2C stop, or ENC Micro-program exchange failure. (ENCxx-1)
B1	SXP error, I2C stop, or ENC Micro-program exchange failure. (ENCxx-2)
BA	SXP write error. (ENCxx-1)
BB	SXP write error. (ENCxx-2)
C0	FAN_ADCFAIL is detected. (ENCxx-1)
C1	FAN_ADCFAIL is detected. (ENCxx-2)
F0	ENC data disagreement.

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Byte27 = F1 (Micro-program Detected Cache Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	Separate	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x'F')				Message (x'1')			
28	Queue transition in progress (Side A)	Queue transition in progress (Side B)	Free SGCB queue operation in progress	Free SLCB queue operation in progress	Free GRPT queue operation in progress	'000'		
29	Not used							(*1)
	VDEV number (high)							(*1)
2A	Queue type							(*1)
	VDEV number (low)	Slot number (high)						(*1)
2B	Queue number (high)							(*1)
	Slot number (middle)							(*1)
2C	Queue number (low)							(*1)
	Slow number (low)							(*1)
2D	SSID of mate storage system (x'0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x'00')							
30	Not used							
31	Module ID							
32	Routine ID							
33	Package number				Error code (invalid)			
34	SSID of self storage system							
35								
36	Symptom code (x'FFF1')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								

*1: When byte 28, bit2-4 = 000, upper value is valid.
When byte 28, bit2-4 ≠ 000, lower value is valid.

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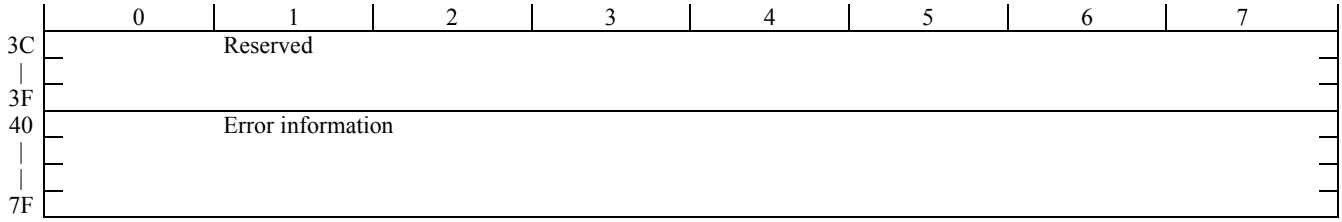
Byte27 = F1 (Micro-program Detected Cache Failure) (2/2)



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Byte27 = F2 (CACHE ERR)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	Reserved					
10	JCB ID							
11	LDEV#high (Logical DKC#)							
12	LDEV#low (LDEV# in DKC)							
13								
14	CDEV#							
15	RDEV#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Host Information							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘F’)				Message (x‘2’)			
28	Subcode (See following pages)							
29	Hardwre information (See following pages)							
2A								
2B								
2C								
2D	SSID for Other storage system (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Hardwre information (See following pages)							
31	Module ID							
32	Routine ID							
33	PKID				Message code (x‘0’)			
34	SSID of self storage system							
35								
36	Symptom code (x‘FFF2’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Reserved							
3E								
3F								
40	Hardwre information (See following pages)							
|								
|								
7F								

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Byte27 = F2 (CACHE ERR) Byte28-2C, 30 Detail

	0	1	2	3	4	5	6	7
28	Subcode							
	x‘1’=C04/C05/C14/C15 (CACHE error) (CHK2) x‘2’=D00/D10/D20/D30/D01/D11/D21/D31 (CHK3)				Not used‘0’	Not used‘0’	Not used‘0’	HMA register LOG error
29	Transfer information							
	Transfer PK Type x‘1’= MAIN Blade x‘5’= MP-PK				Act mode (Not used‘0’)			
2A	Transfer Master PK board number							
	MAIN Blade: x‘00’ ~ x‘01’ MP-PK: x‘00’ ~ x‘01’							
2B	Using path code0 (CHK2)							
	Not used‘0’	Access CACHE Cluster Number#1	Access CACHE Cluster Number#2	Not used ‘0’	Not used ‘0’			
2C	Not used’0’							
30	Transfer Master Path							
	x‘0’=Not used ‘0’ x‘1’=SMC, MPDMA, XD x‘3’=DMA0, x‘4’=DMA1, x‘5’=DMA2, x‘6’=DMA3, x‘7’=DMA4, x‘8’=DMA5, x‘9’=DRR0, x‘A’=DRR1, x‘B’=DRR2, x‘C’=DRR3,				Not used ‘0’			

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Byte27 = F2 (CACHE ERR) Byte40-47 Detail (1/3)

(1) Byte30 = x‘10’ : MPDMA(W1) error status

	0	1	2	3	4	5	6	7
40	Status byte0							
	Not used‘0’	Not used‘0’	E04_TOCNT_TO	Not used‘0’	E06_DT	E07_HLRC_NEQ	E08_DLRC_NEQ	E09_HED
41	Status byte1							
	E10_NPCNT	E11_PCCNT	E12_DLRCTIM	E13_VLD	E14_REQ	Not used‘0’	Not used‘0’	TX_ERRSTS
42	Status byte2							
	Not used‘0’	Not used‘0’	E04_TOCNT_TO	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’	RX_ERRSTS
43	Status byte3							
	TM0_OVER	TM1_OVER	TM2_OVER	TM3_OVER	TM4_OVER	TM5_OVER	TM6_OVER	TM7_OVER
44	Status byte4							
	ACC_CMD_ERR	ACC_CODE_ERR	LENGTH_OVER	LENGTH_ERR	OUT_OF_DIMM_AREA	RANK_STEP_OVER	ACC_CMG0_ERR	ACC_CMG1_ERR
45	Status byte5							
	CMG0_ACC_IN_ERR	CMG1_ACC_IN_ERR	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’
46	Status byte6							
	CMG0_ECC_ERR	CMG0_ECC_ADR_ERR	CMG0_PTY_ERR	CMG1_ECC_ERR	CMG1_ECC_ADR_ERR	CMG1_PTY_ERR	CMG0_1st_ERR_SET	CMG1_1st_ERR_SET
47	Status byte7							
	ERR_CPLD_NOT_SC	ERR_CPL_NOT_SC	ERR_HEAD	ERR_NOT_CPL_CPLD	Not used‘0’	Not used‘0’	ERR_EP	AC_CM_ERR

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Byte27 = F2 (CACHE ERR) Byte40-47 Detail (2/3)

(2) Byte30 = x‘30’ , x‘40’ , x‘50’ , x‘60’ , x‘70’ , x‘80’ : DMA(W2) error status

	0	1	2	3	4	5	6	7
40	Status byte0							
	ACC_CMD_ ERR	ACC_CODE_ ERR	LENGTH_ OVER	LENGTH_ ERR	OUT_OF_ DIMM_AREA	RANK_STEP_ OVER	ACC_CMG0_ ERR	ACC_CMG1_ ERR
41	Status byte1							
	CMG0_ACC_ IN_ERR	CMG1_ACC_ IN_ERR	Not used’0’	Not used’0’	Not used’0’	Not used’0’	CMG0_DQS_ ERR	CMG1_DQS_ ERR
42	Status byte2							
	CMG0_ECC_ ERR	CMG0_ECC_ ADR_ERR	CMG0_PTY_ ERR	CMG1_ECC_ ERR	CMG1_ECC_ ADR_ERR	CMG1_PTY_ ERR	CMG0_1st_ ERR_SET	CMG1_1st_ ERR_SET
43	Status byte3							
	ERR_CPLD_ NOT_SC	ERR_CPL_ NOT_SC	ERR_HEAD	ERR_NOT_ CPL_CPLD	Not used’0’	CPL_T_ OVER	ERR_EP	AC_CM_ ERR

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Byte27 = F2 (CACHE ERR) Byte40-47 Detail (3/3)
(3) Byte30 = x‘90’, x‘A0’, x‘B0’, x‘C0’: DRR(W2) error status

	0	1	2	3	4	5	6	7
40	Status byte0							
	ACC_CMD_ ERR	ACC_CODE_ ERR	LENGTH_ OVER	LENGTH_ ERR	OUT_OF_ DIMM_ AREA	RANK_STEP_ OVER	ACC_CMG0_ ERR	ACC_CMG1_ ERR
41	Status byte1							
	CMG0_ACC_ IN_ERR	CMG1_ACC_ IN_ERR	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’	Not used‘0’
42	Status byte2							
	CMG0_ECC_ ERR	CMG0_ECC_ ADR_ERR	CMG0_PTY_ ERR	CMG1_ECC_ ERR	CMG1_ECC_ ADR_ERR	CMG1_PTY_ ERR	CMG0_1st_ ERR_SET	CMG1_1st_ ERR_SET
43	Status byte3							
	ERR_CPLD_ NOT_SC	ERR_CPL_ NOT_SC	ERR_HEAD	ERR_NOT_ CPL_CPLD	Not used‘0’	Not used‘0’	Not used‘0’	AC_CM_ ERR

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Byte27 = F2 (CACHE ERR) Byte50-5F Detail

	0	1	2	3	4	5	6	7
50	CM00,CM10 representative error							
	Loging RAM status	Micro Error	CM00 error	CM10 error	Hardware error	Not used	Not used	Not used
51	CM01,CM11 representative error							
	Loging RAM status	Micro error	CM01 error	CM11 error	Hardware error	Not used	Not used	Not used
52	CM02,CM12 representative error							
	Loging RAM status	Micro Error	CM02 error	CM12 error	Hardware error	Not used	Not used	Not used
53	CM03,CM13 representative error							
	Loging RAM status	Micro error	CM03 error	CM13 error	Hardware error	Not used	Not used	Not used
54	CM00,CM10 DQS ECC error							
	CM00 DQS error	Not used	CM10 DQS error	Not used	CM00 RMW Error1	CM00 RMW Error2	CM10 RMW Error1	CM10 RMW Error2
55	CM00,CM10 ECC error							
	CM00 UNC Error1	CM00 UNC Error2	CM10 UNC Error1	CM10 UNC Error2	CM00 ADR Error1	CM00 ADR Error2	CM10 ADR Error1	CM10 ADR Error2
56	CM01,CM11 DQS ECC error							
	CM01 DQS error	Not used	CM11 DQS error	Not used	CM01 RMW Error1	CM01 RMW Error2	CM11 RMW Error1	CM11 RMW Error2
57	CM01,CM11 ECC error							
	CM01 UNC Error1	CM01 UNC Error2	CM11 UNC Error1	CM11 UNC Error2	CM01 ADR Error1	CM01 ADR Error2	CM11 ADR Error1	CM11 ADR Error2
58	CM02,CM12 DQS ECC error							
	CM02 DQS error	Not used	CM12 DQS error	Not used	CM02 RMW Error1	CM02 RMW Error2	CM12 RMW Error1	CM12 RMW Error2
59	CM02,CM12 ECC error							
	CM02 UNC Error1	CM02 UNC Error2	CM12 UNC Error1	CM12 UNC Error2	CM02 ADR Error1	CM02 ADR Error2	CM12 ADR Error1	CM12 ADR Error2
5A	CM03,CM13 DQS ECC error							
	CM03 DQS error	Not used	CM13 DQS error	Not used	CM03 RMW Error1	CM03 RMW Error2	CM13 RMW Error1	CM13 RMW Error2
5B	CM03,CM13 ECC error							
	CM03 UNC Error1	CM03 UNC Error2	CM13 UNC Error1	CM13 UNC Error2	CM03 ADR Error1	CM03 ADR Error2	CM13 ADR Error1	CM13 ADR Error2
5C	CM00,CM10 Parity error							
	CM10 parity error	CM00 parity error	Not used	Not used	Not used	Not used	Not used	Not used
5D	CM01,CM11 Parity error							
	CM11 parity error	CM01 parity error	Not used	Not used	Not used	Not used	Not used	Not used
5E	CM02,CM12 Parity error							
	CM12 parity error	CM02 parity error	Not used	Not used	Not used	Not used	Not used	Not used
5F	CM03,CM13 Parity error							
	CM13 parity error	CM03 parity error	Not used	Not used	Not used	Not used	Not used	Not used

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Byte27 = F2 (CACHE ERR) Byte60-7F Detail
(1) If Byte50:(b2= ‘1’ or b3=‘1’) then CM00 or CM01 error
(2) If Byte51:(b2= ‘1’ or b3=‘1’) then CM10 or CM11 error
(3) If Byte52:(b2= ‘1’ or b3=‘1’) then CM20 or CM21 error
(4) If Byte53:(b2= ‘1’ or b3=‘1’) then CM30 or CM31 error

	0	1	2	3	4	5	6	7
60	CMxx ECC error address monitor 1st (byte3)							
	CMG	RANK	Row Address(15)	Row Address(14)	Row Address(13)	Row Address(12)	Row Address(11)	Row Address(10)
61	CMxx ECC error address monitor 1st (byte2)							
	Row Address(9)	Row Address(8)	Row Address(7)	Row Address(6)	Row Address(5)	Row Address(4)	Row Address(3)	Row Address(2)
62	CMxx ECC error address monitor 1st (byte1)							
	Row Address(1)	Row Address(0)	Bank Address(2)	Bank Address(1)	Bank Address(0)	Column Address(10)	Column Address(9)	Column Address(8)
63	CMxx ECC error address monitor 1st (byte0)							
	Column Address(7)	Column Address(6)	Column Address(5)	Column Address(4)	Column Address(3)	Column Address(2)	Column Address(1)	Column Address(0)
64	CMxx ECC error address monitor 2nd (byte3)							
	CMG	RANK	Row Address(15)	Row Address(14)	Row Address(13)	Row Address(12)	Row Address(11)	Row Address(10)
65	CMxx ECC error address monitor 2nd (byte2)							
	Row Address(9)	Row Address(8)	Row Address(7)	Row Address(6)	Row Address(5)	Row Address(4)	Row Address(3)	Row Address(2)
66	CMxx ECC error address monitor 2nd (byte1)							
	Row Address(1)	Row Address(0)	Bank Address(2)	Bank Address(1)	Bank Address(0)	Column Address(10)	Column Address(9)	Column Address(8)
67	CMxx ECC error address monitor 2nd (byte0)							
	Column Address(7)	Column Address(6)	Column Address(5)	Column Address(4)	Column Address(3)	Column Address(2)	Column Address(1)	Column Address(0)
68	CMxx ECC error address monitor 3rd (byte3)							
	CMG	RANK	Row Address(15)	Row Address(14)	Row Address(13)	Row Address(12)	Row Address(11)	Row Address(10)
69	CMxx ECC error address monitor 3rd (byte2)							
	Row Address(9)	Row Address(8)	Row Address(7)	Row Address(6)	Row Address(5)	Row Address(4)	Row Address(3)	Row Address(2)
6A	CMxx ECC error address monitor 3rd (byte1)							
	Row Address(1)	Row Address(0)	Bank Address(2)	Bank Address(1)	Bank Address(0)	Column Address(10)	Column Address(9)	Column Address(8)
6B	CMxx ECC error address monitor 3rd (byte0)							
	Column Address(7)	Column Address(6)	Column Address(5)	Column Address(4)	Column Address(3)	Column Address(2)	Column Address(1)	Column Address(0)
6C	CMxx ECC error address monitor 4th (byte3)							
	CMG	RANK	Row Address(15)	Row Address(14)	Row Address(13)	Row Address(12)	Row Address(11)	Row Address(10)
6D	CMxx ECC error address monitor 4th (byte2)							
	Row Address(9)	Row Address(8)	Row Address(7)	Row Address(6)	Row Address(5)	Row Address(4)	Row Address(3)	Row Address(2)
6E	CMxx ECC error address monitor 4th (byte1)							
	Row Address(1)	Row Address(0)	Bank Address(2)	Bank Address(1)	Bank Address(0)	Column Address(10)	Column Address(9)	Column Address(8)
6F	CMxx ECC error address monitor 4th (byte0)							
	Column Address(7)	Column Address(6)	Column Address(5)	Column Address(4)	Column Address(3)	Column Address(2)	Column Address(1)	Column Address(0)
70	CMxx ECC error address loging result							
	Not used	Not used	Not used	Not used	Loging result 1st	Loging result 2nd	Loging result 3rd	Loging result 4th

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Byte27 = F5 (Remote Copy Paths Removed / Restored) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Intetnal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘F’)				Message (x‘5’)			
28	Reason code (*1)							
29	RCU device address							
2A	RCU Manufacture code/Factory code							
2B								
2C	RCU Sequence No.							
2D								
2E								
2F	MCU Manufacture code/Factory code							
30								
31	MCU Sequence No.							
32								
33								
34	SSID of self storage system							
35								
36	Symptom code (x‘38’)							
37	Symptom code (x‘87’)							
38	Log and message control							
39	Duplex pair failure	Program action code						
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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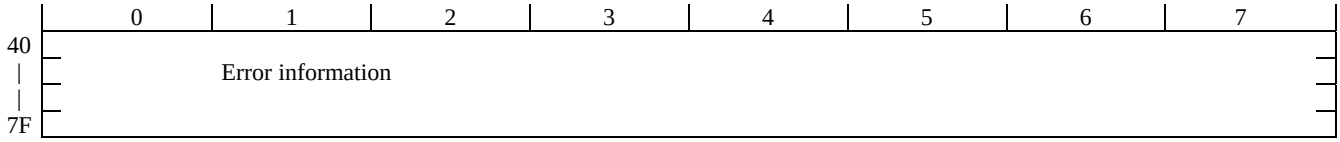
Byte27 = F5 (Remote Copy Paths Removed / Restored) (2/2)



*1: Reason code
x‘01’ : One or more remote copy paths removed unexpectedly
x‘02’ : One or more remote copy paths restored
x‘03’ : All remote copy paths removed unexpectedly

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Byte27 = FA (NVS Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Intetnal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x‘F’)				Message (x‘A’)			
28	Reason code (x‘02’: NVS failure)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	SSID of mate storage system (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Not used (x‘00’)							
31	Module ID							
32	Routine ID							
33	Packeage number				Error code (invalid)			
34	SSID of self storage system							
35								
36	Symptom code (x‘FFFA’)							
37								

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Byte27 = FA (NVS Terminated) (2/2)

	0	1	2	3	4	5	6	7
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								
40	Key code (for reconnection)							
41	Format/Message (for reconnection)							
42	Module ID (for reconnection)							
43	Routine ID (for reconnection)							
44	Reserved							
|								
|								
7F								

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Byte27 = FB (TrueCopy for Pair suspend) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Intetnal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x'F')				Message (x'B')			
28	R-VOL Suspend	R-VOL failure	Reason code (*1)					
29	RCU device address							
2A	RCU Manufacture code/Factory code							
2B								
2C								
2D	RCU Sequence No.							
2E								
2F	MCU Manufacture code/Factory code							
30								
31								
32	MCU Sequence No.							
33								

*1: Reason code
x'04'-x'2F': Reserved
x'30': Pair suspended. MCU device write error.
x'31': Pair suspended. RCU storage systemerror/or MCU storage system error.
x'32': Pair suspended. RCU device communication error.
x'33': Pair suspended (Critical device status). All write command is rejected until the pair is re-established.
x'34': Pair suspended. RCU device is not ready (intervention required).

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Byte27 = FB (TrueCopy for Pair suspend) (2/2)

	0	1	2	3	4	5	6	7
34 35	SSID of self storage system							
36	Symptom code (x‘FE’)							
37	Symptom code (same byte #28)							
38	Log and message control							
39	Duplex pair failure	Program action code						
3A 3B	Configuration information							
3C | 3F	Reserved							
40 | | 7F	Error information							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	Processor ID							
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP REPORT	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	Reserved					
10	JCB ID							
11	LDEV#high (Logical DKC#)							
12	LDEV#low (LDEV# in DKC)							
13								
14	CDEV#							
15	RDEV#							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26								
27	Format (x'F')				Message (x'F')			
28	Subcode (See following pages)							
29	Hardwre information (See following pages)							
|								
|								
31								
32	Module ID							
33	Routine ID							
34	PKID				Message code (x'0')			
35	SSID of self storage system							
36	Symptom code (x'FF8B')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used							
3D	Reserved							
3E								
3F								
40	Hardwre information (See following pages)							
|								
|								
7F								

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(1) Byte28 = 02 : Cache Memory correctable error (1/2)

	0	1	2	3	4	5	6	7
28	Subcode : x‘02’ : Cache Memory correctable error							
29	MPID (Reported SSB)							
2A	Not used	Module number			Cluster number	Not used		
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Warning CM00, CM10 status							
	CM00 Warning1	CM00 Warning2	CM10 Warning1	CM10 Warning2	Not used (x‘00’)			
41	Not used (x‘00’)							
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Warning CM01, CM11 status							
	CM01 Warning1	CM01 Warning2	CM11 Warning1	CM11 Warning2	Not used (x‘00’)			
45	Not used (x‘00’)							
46	Not used (x‘00’)							
47	Not used (x‘00’)							
48	Warning CM02, CM12 status							
	CM02 Warning1	CM02 Warning2	CM12 Warning1	CM12 Warning2	Not used (x‘00’)			
49	Not used (x‘00’)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Warning CM03, CM13 status							
	CM03 Warning1	CM03 Warning2	CM13 Warning1	CM13 Warning2	Not used (x‘00’)			
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(1) Byte28 = 02 : Cache Memory correctable error (2/2)

	0	1	2	3	4	5	6	7
50	CMxx correctable error address monitor 1st (byte3)							
	CMG	RANK	Row Address(15)	Row Address(14)	Row Address(13)	Row Address(12)	Row Address(11)	Row Address(10)
51	CMxx correctable error address monitor 1st (byte2)							
	Row Address(9)	Row Address(8)	Row Address(7)	Row Address(6)	Row Address(5)	Row Address(4)	Row Address(3)	Row Address(2)
52	CMxx correctable error address monitor 1st (byte1)							
	Row Address(1)	Row Address(0)	Bank Address(2)	Bank Address(1)	Bank Address(0)	Column Address(10)	Column Address(9)	Column Address(8)
53	CMxx correctable error address monitor 1st (byte0)							
	Column Address(7)	Column Address(6)	Column Address(5)	Column Address(4)	Column Address(3)	Column Address(2)	Column Address(1)	Column Address(0)
54	CMxx correctable error address monitor 2nd (byte3)							
55	CMxx correctable error address monitor 2nd (byte2)							
56	CMxx correctable error address monitor 2nd (byte1)							
57	CMxx correctable error address monitor 2nd (byte0)							
58	CMxx correctable error address monitor 3rd (byte3)							
59	CMxx correctable error address monitor 3rd (byte2)							
5A	CMxx correctable error address monitor 3rd (byte1)							
5B	CMxx correctable error address monitor 3rd (byte0)							
5C	CMxx correctable error address monitor 4th (byte3)							
5D	CMxx correctable error address monitor 4th (byte2)							
5E	CMxx correctable error address monitor 4th (byte1)							
5F	CMxx correctable error address monitor 4th (byte0)							
60	CMxx correctable error LOC. Information0							
61	CMxx correctable error LOC. Information1							
62	CMxx correctable error LOC. Information2							
63	CMxx correctable error LOC. Information3							
64	CMxx correctable error LOC. Information4							
65	CMxx correctable error LOC. Information5							
66	CMxx correctable error LOC. Information6							
67	CMxx correctable error LOC. Information7							
68	CMxx correctable error address loging result (byte3)							
	Not used	Not used	Not used	Not used	Loging result 1st	Loging result 2nd	Loging result 3rd	Loging result 4th
69	CMxx correctable error address loging result (byte2)							
	Not used	Not used	Not used	Not used	RMW result 1st	RMW result 2nd	RMW result 3rd	RMW result 4th
6A	CMxx correctable error address loging result (byte1)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Bigin or Last
6B	CMxx correctable error address loging result (byte0)							
	Not used	Not used	Not used	Not used	Loging EN result 1st	Loging EN result 2nd	Loging EN result 3rd	Loging EN result 4th

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(2) Byte28 = 84 : HMA correctable error (1/2)

	0	1	2	3	4	5	6	7
28	Subcode : x‘84’ : HMA correctable error							
29	MPID (Reported SSB)							
2A	MDID/CLID							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	HMA::LRP warning							
	Not used	Not used	Not used	INT LRP4 WNG	INT LRP3 WNG	INT LRP2 WNG	INT LRP1 WNG	INT LRP0 WNG
41	HMA::FDMA warning							
	Not used	Not used	Not used	INT FDMA4 WNG	INT FDMA3 WNG	INT FDMA2 WNG	INT FDMA1 WNG	INT FDMA0 WNG
42	HMA::DRR/MPDMA/DMAMB warning							
	INT DRR3 WNG	INT DRR2 WNG	INT DRR1 WNG	INT DRR0 WNG	INT MPDMA1 WNG	INT MPDMA0 WNG	INT DMAMB1 WNG	INT DMAMB0 WNG
43	HMA::DMA warning							
	Not used	Not used	INT DMA5 WNG	INT DMA4 WNG	INT DMA3 WNG	INT DMA2 WNG	INT DMA1 WNG	INT DMA0 WNG
44	HMA::BARB/IARB warning							
	Not used	Not used	Not used	Not used	Not used	INT BARB WNG	INT IARB1 WNG	INT IARB0 WNG
45	HMA::EARB/IXARB/PARB warning							
	INT EARB1 WNG	INT EARB0 WNG	INT IXARB1 WNG	INT IXARB0 WNG	INT PARB3 WNG	INT PARB2 WNG	INT PARB1 WNG	INT PARB0 WNG
46	HMA::BARBREG/IARBREG warning							
	INT EARBREG1 WNG	INT EARBREG0 WNG	INT IXARBREG1 WNG	INT IXARBREG0 WNG	INT PARBREG3 WNG	INT PARBREG2 WNG	INT PARBREG1 WNG	INT PARBREG0 WNG
47	HMA::EARBREG/IXARBREG/PARBREGwarning							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	TX SIZE CHK WNG
48	HMA::DC/TXFAULT/PCIE/XD/BRAM/BCOM/SMCwarning							
	DC UPDOWN WNG	TX FAULT	PCI CORE WNG	Not used	INT XD WNG	INT BRAM WNG	INT BCOM WNG	INT SMC WNG
49	HMA::REG2/DXA warning							
	Not used	Not used	Not used	INT REG2 WNG	INT DXA3 WNG	INT DXA2 WNG	INT DXA1 WNG	INT DXA0 WNG

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(2) Byte28 = 84 : HMA correctable error (2/2)

4A	HMA::DXC warning							
	INT DXC3 MICRO	INT DXC2 MICRO	INT DXC1 MICRO	INT DXC0 MICRO	INT DXC3 WNG	INT DXC2 WNG	INT DXC1 WNG	INT DXC0 WNG
4B	HMA::DXC DIMM warning							
	INT DXC3 WNG DIMM1	INT DXC2 WNG DIMM1	INT DXC1 WNG DIMM1	INT DXC0 WNG DIMM1	INT DXC3 WNG DIMM0	INT DXC2 WNG DIMM0	INT DXC1 WNG DIMM0	INT DXC0 WNG DIMM0
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							
60 | 7F	Not used (x‘00’)							

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(3) Byte28 = 40 : Abnormal DC Voltage control warning (1/1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘40’ : Abnormal DC Voltage control warning							
29	MPID (Reported SSB)							
2A	Register access result BYTE (00:No error, 01:Error detected)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Threshold counter for the warning (MAIN Blade#1)				Threshold counter for the warning (MAIN Blade#0)			
41	Threshold counter for the warning (MP PK#1)				Threshold counter for the warning (MP PK#0)			
42	Not used (x‘00’)				Not used (x‘00’)			
43	Not used (x‘00’)				Not used (x‘00’)			
44	Not used (x‘00’)				Not used (x‘00’)			
45	Not used (x‘00’)				Not used (x‘00’)			
46	Not used (x‘00’)				Not used (x‘00’)			
47	Not used (x‘00’)				Not used (x‘00’)			
48	Not used (x‘00’)				Not used (x‘00’)			
49	Not used (x‘00’)				Not used (x‘00’)			
4A	Not used (x‘00’)				Not used (x‘00’)			
4B	Not used (x‘00’)				Not used (x‘00’)			
4C	Not used (x‘00’)				Not used (x‘00’)			
4D	Not used (x‘00’)				Not used (x‘00’)			
4E	Not used (x‘00’)				Not used (x‘00’)			
4F	Not used (x‘00’)				Not used (x‘00’)			
50	Voltage control register information (MAIN Blade#1))				Voltage control register information (MAIN Blade#0)			
	DC_CTL_EN		DC_UP (+5%)	DC_DWN (-5%)	DC_CTL_EN		DC_UP (+5%)	DC_DWN (-5%)
51	Voltage control register information (MP PK#1)				Voltage control register information (MP PK#0)			
	DC_CTL_EN		DC_UP (+5%)	DC_DWN (-5%)	DC_CTL_EN		DC_UP (+5%)	DC_DWN (-5%)
52	Not used (x‘00’)				Not used (x‘00’)			
53	Not used (x‘00’)				Not used (x‘00’)			
54	Not used (x‘00’)				Not used (x‘00’)			
55	Not used (x‘00’)				Not used (x‘00’)			
56	Not used (x‘00’)				Not used (x‘00’)			
57	Not used (x‘00’)				Not used (x‘00’)			
58	Not used (x‘00’)				Not used (x‘00’)			
59	Not used (x‘00’)				Not used (x‘00’)			
5A	Not used (x‘00’)				Not used (x‘00’)			
5B	Not used (x‘00’)				Not used (x‘00’)			
5C	Not used (x‘00’)				Not used (x‘00’)			
5D	Not used (x‘00’)				Not used (x‘00’)			
5E	Not used (x‘00’)				Not used (x‘00’)			
5F	Not used (x‘00’)				Not used (x‘00’)			
60 | 7F	Not used (x‘00’)				Not used (x‘00’)			

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(4) Byte28 = 41 : Abnormal CEMODE warning (1/1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘41’ : Abnormal CEMODE warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	PK status							
	PSOFFOK	THAWAR	LIDET2	LIDET1	CEMODE	CEDT2	CEDT1	CEDT0
41	UPDOWN							
	Reserved	Reserved	Down (Moni)	Up (Moni)	Reserved	Reserved	Down (set)	Up (set)
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Not used (x‘00’)							
45	Not used (x‘00’)							
46	Not used (x‘00’)							
47	Not used (x‘00’)							
48	Not used (x‘00’)							
49	Not used (x‘00’)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							
60 | 7F	Not used (x‘00’)							

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(5) Byte28 = 42 : Abnormal CEDT warning (1/1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘42’ : Abnormal CEDT warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	PK status							
	PSOFFOK	THAWAR	LIDET2	LIDET1	CEMODE	CEDT2	CEDT1	CEDT0
41	Not used (x‘00’)							
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Not used (x‘00’)							
45	Not used (x‘00’)							
46	Not used (x‘00’)							
47	Not used (x‘00’)							
48	Not used (x‘00’)							
49	Not used (x‘00’)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							
60 | 7F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(6) Byte28 = C0 : SFP (Tachyon) warning (1/2)

	0	1	2	3	4	5	6	7
28	Subcode : x‘C0’ : SFP (Tachyon) warning							
29	MPID (Reported SSB)							
2A	Tx_Fault detection CL number							
2B	Tx_Fault detection port number							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Not used (x‘00’)							
41	Not used (x‘00’)							
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Device address “A0”, Data address “6”							
45	Device address “A0”, Data address “10”							
46	Device address “A0”, Data address “40”							
47	Device address “A0”, Data address “41”							
48	Device address “A0”, Data address “42”							
49	Device address “A0”, Data address “43”							
4A	Device address “A0”, Data address “44”							
4B	Device address “A0”, Data address “45”							
4C	Device address “A0”, Data address “46”							
4D	Device address “A0”, Data address “47”							
4E	Device address “A0”, Data address “48”							
4F	Device address “A0”, Data address “49”							
50	Device address “A0”, Data address “50”							
51	Device address “A0”, Data address “51”							
52	Device address “A0”, Data address “52”							
53	Device address “A0”, Data address “53”							
54	Device address “A0”, Data address “54”							
55	Device address “A0”, Data address “55”							
56	Device address “A0”, Data address “60”							
57	Device address “A0”, Data address “61”							
58	Device address “A0”, Data address “68”							
59	Device address “A0”, Data address “69”							
5A	Device address “A0”, Data address “70”							
5B	Device address “A0”, Data address “71”							
5C	Device address “A0”, Data address “72”							
5D	Device address “A0”, Data address “73”							

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(6) Byte28 = C0 : SFP (Tachyon) warning (2/2)

	0	1	2	3	4	5	6	7
5F	Device address “A0”, Data address “75”							
60	Device address “A0”, Data address “76”							
61	Device address “A0”, Data address “77”							
62	Device address “A0”, Data address “78”							
63	Device address “A0”, Data address “79”							
64	Device address “A0”, Data address “80”							
65	Device address “A0”, Data address “81”							
66	Device address “A0”, Data address “82”							
67	Device address “A0”, Data address “83”							
68	Device address “A0”, Data address “96”							
69	Device address “A0”, Data address “97”							
6A	Device address “A2”, Data address “112”							
6B	Device address “A2”, Data address “113”							
6C	Device address “A2”, Data address “114”							
6D	Device address “A2”, Data address “115”							
6E	Device address “A2”, Data address “116”							
6F	Device address “A2”, Data address “117”							
70	Device address “A2”, Data address “118”							
71	Device address “A2”, Data address “119”							
72	Device address “A2”, Data address “128”							
73	Device address “A2”, Data address “129”							
74	Not used (x‘00’)							
75	Not used (x‘00’)							
76	Not used (x‘00’)							
77	Not used (x‘00’)							
78	Not used (x‘00’)							
79	Not used (x‘00’)							
7A	Not used (x‘00’)							
7B	Not used (x‘00’)							
7C	Not used (x‘00’)							
7D	Not used (x‘00’)							
7E	Not used (x‘00’)							
7F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(7) Byte28 = 45 : Battery warning (1/3)

	0	1	2	3	4	5	6	7
28	Subcode : x‘45’ : Battery warning							
29	MPID (Reported SSB)							
2A	MDCLID (Reported SSB)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Parts status0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
41	Parts status1							
	Not used	Not used	Not used	Not used	Not used	Not used	CM Backup Warning	Battery Warning
42	Parts status2							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	FAN Control Warning
43	Parts status3							
	BRG _P Warning	BRG _S Warning	SH Micon Warning	CFM1 Warning	CFM0 Warning	Battery Controller Warning	Battery Warning	Battery Charge
44	Battery status0							
	ENV Alarm	Not used	Not used	Not used	Volatile PIN	Not used	Not used	Not used
45	Battery status1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	Battery status2							
	Battery Full	Not used	Not used	Not used	Not used	Not used	Not used	Battery Half
47	Battery status3							
	Not used	Not used	Not used	Not used	Not used	Not used	Battery Empty	Not used
48	Parts firm exchange status0							
	SPROM Erase Fail	SPROM Erase Completion	Not used	Not used	CFM1 Erase Fail	CFM0 Erase Fail	CFM1 Erase Completion	CFM0 Erase Completion
49	Parts firm exchange status1							
	Not used	Not used	Not used	Not used	BATC_FIRM Exchange Fail	CFM1_FIRM Exchange Fail	CFM0_FIRM Exchange Fail	SH_FIRM Exchange Fail
4A	Parts firm exchange status2							
	BATC_FIRM Exchange Done	CFM1_FIRM Exchange Done	CFM0_FIRM Exchange Done	SH_FIRM Exchange Done	BATC_FIRM Exchange Busy	CFM1_FIRM Exchange Busy	CFM0_FIRM Exchange Busy	SH_FIRM Exchange Busy
4B	Parts firm exchange status3							
	Not used	Not used	Not used	Not used	Not used	Battery Exchange Fail	Battery Exchange Done	Battery Exchange Ready

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(7) Byte28 = 45 : Battery warning (2/3)

	0	1	2	3	4	5	6	7
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Battery controller LOG00							
51	Battery controller LOG01							
52	Battery controller LOG02							
53	Battery controller LOG03							
54	Battery controller LOG04							
55	Battery controller LOG05							
56	Battery controller LOG06							
57	Battery controller LOG07							
58	Battery controller LOG08							
59	Battery controller LOG09							
5A	Battery controller LOG10							
5B	Battery controller LOG11							
5C	Battery controller LOG12							
5D	Battery controller LOG13							
5E	Battery controller LOG14							
5F	Battery controller LOG15							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(7) Byte28 = 45 : Battery warning (3/3)

	0	1	2	3	4	5	6	7
60	Battery controller LOG16							
61	Battery controller LOG17							
62	Battery controller LOG18							
63	Battery controller LOG19							
64	Battery controller LOG20							
65	Battery controller LOG21							
66	Battery controller LOG22							
67	Battery controller LOG23							
68	Battery controller LOG24							
69	Battery controller LOG25							
6A	Battery controller LOG26							
6B	Battery controller LOG27							
6C	Battery controller LOG28							
6D	Battery controller LOG29							
6E	Battery controller LOG30							
6F	Battery controller LOG31							
70	Battery controller LOG32							
71	Battery controller LOG33							
72	Battery controller LOG34							
73	Battery controller LOG35							
74	Battery controller LOG36							
75	Battery controller LOG37							
76	Battery controller LOG38							
77	Battery controller LOG39							
78	Battery controller LOG40							
79	Battery controller LOG41							
7A	Battery controller LOG42							
7B	Battery controller LOG43							
7C	Battery controller LOG44							
7D	Battery controller LOG45							
7E	Battery controller LOG46							
7F	Battery controller LOG47							

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(8) Byte28 = 46 : CFM warning (1/3)

	0	1	2	3	4	5	6	7
28	Subcode : x‘46’ : CFM warning							
29	MPID (Reported SSB)							
2A	MDCLID (Reported SSB)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Store / Restore status0							
	DIAG Restore Done	DIAG Store Done	Not used	Not used	CFM Inline Done	CFM CUDG5 Done	CFM CUDG4 Done	CFM CUDG3 Done
41	Store / Restore status1							
	Not used	Not used	Not used	Internal DIAG Running	Not used	Not used	Not used	Invalid Command Error
42	Store / Restore status2							
	Not used	Not used	Config Done	Config Fail	Restore Done	Restore Busy	Restore Fail	Restore Success
43	Store / Restore status3							
	Restore Volatile	Not used	Not used	Not used	Store Done	Store Busy	Store Fail	Store Success
44	PARTS status0							
	Not used	Not used	Not used	Not used	Not used	Not used	CM Backup Warning	Battery Warning
45	PARTS status1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	FAN Control Warning
46	PARTS status2							
	BRG _P Warning	BRG _S Warning	SH Micon Warning	Not used	CFM0 Warning	Battery Controller Warning	Battery Warning	Battery Charge
47	SH bus error status(GPIO)							
	Not used	Not used	Not used	Not used	SH Bus Warning	SH Bus(micro) Warning	PK LED Test	PK Thermistor Alarm
48	Parts Firm exchange status0							
	SPROM Erase Fail	SPROM Erase Completion	Not used	Not used	Not used	CFM0 Erase Fail	Not used	CFM0 Erase Completion
49	Parts Firm exchange status1							
	Not used	Not used	Not used	Not used	BATC_FIRM Exchange Fail	Not used	CFM0_FIRM Exchange Fail	SH_FIRM Exchange Fail
4A	Parts Firm exchange status2							
	BATC_FIRM Exchange Done	CFM1_FIRM Exchange Done	CFM0_FIRM Exchange Done	SH_FIRM Exchange Done	BATC_FIRM Exchange Busy	Not used	CFM0_FIRM Exchange Busy	SH_FIRM Exchange Busy
4B	Parts Firm exchange status3							
	Not used	Not used	Not used	Not used	Not used	Battery Exchange Fail	Battery Exchange Done	Battery Exchange Ready

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(8) Byte28 = 46 : CFM warning (2/3)

	0	1	2	3	4	5	6	7
4C	CFM CONFIG0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	CFM CONFIG1							
	Not used	Not used	Not used	Not used	CFM0 Capa 128GB	CFM0 Capa 64GB	Not used	Not used
4E	Store error LOG							
	Restore Error_log MG7	Restore Error_log MG6	Restore Error_log MG5	Restore Error_log MG4	Restore Error_log MG3	Restore Error_log MG2	Restore Error_log MG1	Restore Error_log MG0
4F	Restore error LOG							
	Store Error_log MG7	Store Error_log MG6	Store Error_log MG5	Store Error_log MG4	Store Error_log MG3	Store Error_log MG2	Store Error_log MG1	Store Error_log MG0
50	SH_micro Firm revision0							
51	SH_micro Firm revision1							
52	SH_micro Firm revision2							
53	SH_micro Firm revision3							
54	Bridge_Chip error status (PCI express) 0							
55	Bridge_Chip error status (PCI express) 1							
56	Bridge_Chip error status (PCI express) 2							
57	Bridge_Chip error status (PCI express) 3							
58	Bridge_Chip error status (SATA_P0) 0							
59	Bridge_Chip error status (SATA_P0) 1							
5A	Bridge_Chip error status (SATA_P0) 2							
5B	Bridge_Chip error status (SATA_P0) 3							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(8) Byte28 = 46 : CFM warning (3/3)

	0	1	2	3	4	5	6	7
60	CFM0 SATA error status0							
61	CFM0 SATA error status1							
62	CFM0 RFIS error status0							
63	CFM0 RFIS error status1							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	CFM model number0							
69	CFM model number1							
6A	CFM model number2							
6B	CFM model number3							
6C	CFM model number4							
6D	CFM model number5							
6E	CFM model number6							
6F	CFM model number7							
70	CFM SMART0							
71	CFM SMART1							
72	CFM SMART2							
73	CFM SMART3							
74	CFM SMART4							
75	CFM SMART5							
76	CFM SMART6							
77	CFM SMART7							
78	CFM SMART8							
79	CFM SMART9							
7A	CFM SMART10							
7B	CFM SMART11							
7C	CFM SMART12							
7D	CFM SMART13							
7E	CFM SMART14							
7F	CFM SMART15							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(9) Byte28 = 48 : MPPK Abnormal temperature warning (1/1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘48’ : MPPK Abnormal temperature warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	IA32 Thermistor status0 :B7							
	Reserved							
41	IA32 Thermistor status1 :B6							
	Reserved							
42	IA32 Thermistor status2 :B5							
	Reserved							
43	IA32 Thermistor status3 :B4							
	Reserved							
44	IA32 Thermistor status4 :B3							
	Reading Valid	Resolution in Degrees Celsius				Reserved	Reserved	Reserved
45	IA32 Thermistor status5 :B2							
	Reserved	Digital Readout						
46	IA32 Thermistor status6 :B1							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Thmal Thres #2 Log	Thmal Thres #2 Status
47	IA32 Thermistor status7 :B0							
	Thmal Thres #1 Log	Thmal Thres #1 Status	Out of Spec Status Log	Out of Spec Status	PRCHOT# or FRCEPR# Log	PRCHOT# or FRCEPR# Eve	Thrmal Status Log	Thrmal Status
48	LM84(0) Local temperature							
	Local Temp(0)							
49	LM84(1) Local temperature							
	Local Temp(1)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							
60 | 7F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(10) Byte28 = 49 : PK Abnormal temperature warning (1/2)

	0	1	2	3	4	5	6	7
28	Subcode : x‘49’ : PK Abnormal temperature warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	MAIN Blade Abnormal temperature register (Module0, MAIN Blade#0)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	PK Temperature Warning
41	MAIN Blade Abnormal temperature register (Module0, MAIN Blade#1)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	PK Temperature Warning
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Not used (x‘00’)							
45	Not used (x‘00’)							
46	Not used (x‘00’)							
47	Not used (x‘00’)							
48	Not used (x‘00’)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(10) Byte28 = 49 : PK Abnormal temperature warning (2/2)

	0	1	2	3	4	5	6	7
60	Not used (x‘00’)							
61	Not used (x‘00’)							
62	Not used (x‘00’)							
63	Not used (x‘00’)							
64	Not used (x‘00’)							
65	Not used (x‘00’)							
66	Not used (x‘00’)							
67	Not used (x‘00’)							
68	Not used (x‘00’)							
6A	Not used (x‘00’)							
6B	Not used (x‘00’)							
6C	Not used (x‘00’)							
6D	Not used (x‘00’)							
6E	Not used (x‘00’)							
6F	Not used (x‘00’)							
70	Not used (x‘00’)							
71	Not used (x‘00’)							
72	Not used (x‘00’)							
73	Not used (x‘00’)							
74	Not used (x‘00’)							
75	Not used (x‘00’)							
76	Not used (x‘00’)							
77	Not used (x‘00’)							
78	MP Abnormal temperature register (Module0, MPPK#0)							
	PSOFFOK	THAWAR	LIDET2	LIDET1	CEMODE	CEDT2	CEDT1	CEDT0
79	MP Abnormal temperature register (Module0, MPPK#1)							
	PSOFFOK	THAWAR	LIDET2	LIDET1	CEMODE	CEDT2	CEDT1	CEDT0
7A	Not used (x‘00’)							
7B	Not used (x‘00’)							
7C	Not used (x‘00’)							
7D	Not used (x‘00’)							
7E	Not used (x‘00’)							
7F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(11) Byte28 = 43 : Forced volatile reboot warning (1/1)

	0	1	2	3	4	5	6	7
28	Subcode : x‘43’ : Forced volatile reboot warning							
29	MPID (Reported SSB)							
2A	MDCLID (Reported SSB)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Volatile PIN (Main1)							
	ENV Alarm	Not used	Not used	Not used	Volatile PIN	Not used	Not used	Not used
41	Volatile PIN (Main2)							
	ENV Alarm	Not used	Not used	Not used	Volatile PIN	Not used	Not used	Not used
42	Not used (x‘00’)							
43	Not used (x‘00’)							
44	Not used (x‘00’)							
45	Not used (x‘00’)							
46	Not used (x‘00’)							
47	Not used (x‘00’)							
48	Not used (x‘00’)							
49	Not used (x‘00’)							
4A	Not used (x‘00’)							
4B	Not used (x‘00’)							
4C	Not used (x‘00’)							
4D	Not used (x‘00’)							
4E	Not used (x‘00’)							
4F	Not used (x‘00’)							
50	Not used (x‘00’)							
51	Not used (x‘00’)							
52	Not used (x‘00’)							
53	Not used (x‘00’)							
54	Not used (x‘00’)							
55	Not used (x‘00’)							
56	Not used (x‘00’)							
57	Not used (x‘00’)							
58	Not used (x‘00’)							
59	Not used (x‘00’)							
5A	Not used (x‘00’)							
5B	Not used (x‘00’)							
5C	Not used (x‘00’)							
5D	Not used (x‘00’)							
5E	Not used (x‘00’)							
5F	Not used (x‘00’)							
60 | 7F	Not used (x‘00’)							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(12) Byte28 = 47 : CFM Config warning (1/3)

	0	1	2	3	4	5	6	7
28	Subcode : x‘47’ : CFM warning							
29	MPID (Reported SSB)							
2A	MDCLID (Reported SSB)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Store / Restore status0							
	DIAG ReStore Done	DIAG store Done	Not used	Not used	CFM Inline Done	CFM CUDG5 Done	CFM CUDG4 Done	CFM CUDG3 Done
41	Store / Restore status1							
	Not used	Not used	Not used	Internal DIAG Running	Not used	Not used	Not used	Invalid Command Error
42	Store / Restore status2							
	Not used	Not used	Config Done	Config Fail	Restore Done	Restore Busy	Restore Fail	Restore Success
43	Store / Restore status3							
	Restore Volatile	Not used	Not used	Not used	Store Done	Store Busy	Store Fail	Store Success
44	PARTS status0							
	Not used	Not used	Not used	Not used	Not used	Not used	CM Backup Warning	Battery Warning
45	PARTS status1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	FAN Control Warning
46	PARTS status2							
	BRG _P Warning	BRG _S Warning	SH Micon Warning	Not used	CFM0 Warning	Battery Controller Warning	Battery Warning	Battery Charge
47	SH bus error status (GPIO)							
	Not used	Not used	Not used	Not used	SH Bus Warning	SH Bus (micro) Warning	PK LED Test	PK Thermistor Alarm
48	Parts Firm exchange status0							
	SPROM Erase Fail	SPROM Erase Completion	Not used	Not used	Not used	CFM0 Erase Fail	Not used	CFM0 Erase Completion
49	Parts Firm exchange status1							
	Not used	Not used	Not used	Not used	BATC_FIRM Exchange Fail	Not used	CFM0_FIRM Exchange Fail	SH_FIRM Exchange Fail
4A	Parts Firm exchange status2							
	BATC_FIRM Exchange Done	CFM1_FIRM Exchange Done	CFM0_FIRM Exchange Done	SH_FIRM Exchange Done	BATC_FIRM Exchange Busy	Not used	CFM0_FIRM Exchange Busy	SH_FIRM Exchange Busy
4B	Parts Firm exchange status3							
	Not used	Not used	Not used	Not used	Not used	Battery Exchange Fail	Battery Exchange Done	Battery Exchange Ready

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(12) Byte28 = 47 : CFM Config warning (2/3)

	0	1	2	3	4	5	6	7
4C	CFM CONFIG0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	CFM CONFIG1							
	Not used	Not used	Not used	Not used	CFM0 Capa 128GB	CFM0 Capa 64GB	Not used	Not used
4E	Store error LOG							
	Restore Error_log MG7	Restore Error_log MG6	Restore Error_log MG5	Restore Error_log MG4	Restore Error_log MG3	Restore Error_log MG2	Restore Error_log MG1	Restore Error_log MG0
4F	Restore error LOG							
	Store Error_log MG7	Store Error_log MG6	Store Error_log MG5	Store Error_log MG4	Store Error_log MG3	Store Error_log MG2	Store Error_log MG1	Store Error_log MG0
50	SH_micro Firm revision0							
51	SH_micro Firm revision1							
52	SH_micro Firm revision2							
53	SH_micro Firm revision3							
54	Bridge_Chip error status (PCI express) 0							
55	Bridge_Chip error status (PCI express) 1							
56	Bridge_Chip error status (PCI express) 2							
57	Bridge_Chip error status (PCI express) 3							
58	Bridge_Chip error status (SATA_P0) 0							
59	Bridge_Chip error status (SATA_P0) 1							
5A	Bridge_Chip error status (SATA_P0) 2							
5B	Bridge_Chip error status (SATA_P0) 3							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(12) Byte28 = 47 : CFM Config warning (3/3)

	0	1	2	3	4	5	6	7
60	CFM0 SATA error status0							
61	CFM0 SATA error status1							
62	CFM0 RFIS error status0							
63	CFM0 RFIS error status1							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	CFM model number0							
69	CFM model number1							
6A	CFM model number2							
6B	CFM model number3							
6C	CFM model number4							
6D	CFM model number5							
6E	CFM model number6							
6F	CFM model number7							
70	CFM SMART0							
71	CFM SMART1							
72	CFM SMART2							
73	CFM SMART3							
74	CFM SMART4							
75	CFM SMART5							
76	CFM SMART6							
77	CFM SMART7							
78	CFM SMART8							
79	CFM SMART9							
7A	CFM SMART10							
7B	CFM SMART11							
7C	CFM SMART12							
7D	CFM SMART13							
7E	CFM SMART14							
7F	CFM SMART15							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(13) Byte28 = 4A : MAIN Blade FAN warning (1/3)

	0	1	2	3	4	5	6	7
28	Subcode : x‘4A’ : CFM warning							
29	MPID (Reported SSB)							
2A	MDCLID (Reported SSB)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

	0	1	2	3	4	5	6	7
40	Store / Restore status0							
	DIAG Restore Done	DIAG Store Done	Not used	Not used	CFM Inline Done	CFM CUDG5 Done	CFM CUDG4 Done	CFM CUDG3 Done
41	Store / Restore status1							
	Not used	Not used	Not used	Internal DIAG Running	Not used	Not used	Not used	Invalid Command Error
42	Store / Restore status2							
	Not used	Not used	Config Done	Config Fail	Restore Done	Restore Busy	Restore Fail	Restore Success
43	Store / Restore status3							
	Restore Volatile	Not used	Not used	Not used	Store Done	Store Busy	Store Fail	Store Success
44	PARTS status0							
	Not used	Not used	Not used	Not used	Not used	Not used	CM Backup Warning	Battery Warning
45	PARTS status1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	FAN Control Warning
46	PARTS status2							
	BRG _P Warning	BRG _S Warning	SH Micon Warning	Not used	CFM0 Warning	Battery Controller Warning	Battery Warning	Battery Charge
47	SH bus error status (GPIO)							
	Not used	Not used	Not used	Not used	SH Bus Warning	SH Bus (micro) Warning	PK LED Test	PK Thermistor Alarm
48	Parts Firm exchange status0							
	SPROM Erase Fail	SPROM Erase Completion	Not used	Not used	Not used	CFM0 Erase Fail	Not used	CFM0 Erase Completion
49	Parts Firm exchange status1							
	Not used	Not used	Not used	Not used	BATC_FIRM Exchange Fail	Not used	CFM0_FIRM Exchange Fail	SH_FIRM Exchange Fail
4A	Parts Firm exchange status2							
	BATC_FIRM Exchange Done	CFM1_FIRM Exchange Done	CFM0_FIRM Exchange Done	SH_FIRM Exchange Done	BATC_FIRM Exchange Busy	Not used	CFM0_FIRM Exchange Busy	SH_FIRM Exchange Busy
4B	Parts Firm exchange status3							
	Not used	Not used	Not used	Not used	Not used	Battery Exchange Fail	Battery Exchange Done	Battery Exchange Ready

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(13) Byte28 = 4A : MAIN Blade FAN warning (2/3)

	0	1	2	3	4	5	6	7
4C	CFM CONFIG0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	CFM CONFIG1							
	Not used	Not used	Not used	Not used	CFM0 Capa 128GB	CFM0 Capa 64GB	Not used	Not used
4E	Store error LOG							
	Restore Error_log MG7	Restore Error_log MG6	Restore Error_log MG5	Restore Error_log MG4	Restore Error_log MG3	Restore Error_log MG2	Restore Error_log MG1	Restore Error_log MG0
4F	Restore error LOG							
	Store Error_log MG7	Store Error_log MG6	Store Error_log MG5	Store Error_log MG4	Store Error_log MG3	Store Error_log MG2	Store Error_log MG1	Store Error_log MG0
50	SH_micro Firm revision0							
51	SH_micro Firm revision1							
52	SH_micro Firm revision2							
53	SH_micro Firm revision3							
54	Bridge_Chip error status (PCI express) 0							
55	Bridge_Chip error status (PCI express) 1							
56	Bridge_Chip error status (PCI express) 2							
57	Bridge_Chip error status (PCI express) 3							
58	Bridge_Chip error status (SATA_P0) 0							
59	Bridge_Chip error status (SATA_P0) 1							
5A	Bridge_Chip error status (SATA_P0) 2							
5B	Bridge_Chip error status (SATA_P0) 3							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (DXBF / Cache Memory / PCI Express Correctable / Abnormal MODE / SFP / Batteriy / CFM / FAN / Abnormal Temperature / Forced volatile Warning : Error handing support) Hardware detail information

(13) Byte28 = 4A : MAIN Blade FAN warning (3/3)

	0	1	2	3	4	5	6	7
60	CFM0 SATA error status0							
61	CFM0 SATA error status1							
62	CFM0 RFIS error status0							
63	CFM0 RFIS error status1							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	CFM model number0							
69	CFM model number1							
6A	CFM model number2							
6B	CFM model number3							
6C	CFM model number4							
6D	CFM model number5							
6E	CFM model number6							
6F	CFM model number7							
70	CFM SMART0							
71	CFM SMART1							
72	CFM SMART2							
73	CFM SMART3							
74	CFM SMART4							
75	CFM SMART5							
76	CFM SMART6							
77	CFM SMART7							
78	CFM SMART8							
79	CFM SMART9							
7A	CFM SMART10							
7B	CFM SMART11							
7C	CFM SMART12							
7D	CFM SMART13							
7E	CFM SMART14							
7F	CFM SMART15							

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Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 81/82/84 (FPC Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PK TYPE		MP#					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HST REP	HST REP	EXPLS
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26					Format (x'1')			
27	Reserved							
28	Internal Failure Part							
29								
2A	SCSI command (See SSBLOG05-5220)							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	CDEV#							
2F	Reserved							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Exception Class				Reserved			
37	RDEV#							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								
40	The fixed value (x'00')							
41								
42								
43								

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Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 81/82/84 (FPC Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40		Time of occurrence						
41								
42								
43								
44		Type Cord (x‘81’ or x‘82’ or x‘84’)						
45		Reserved						
46								
47								
48		SAS Port#						
49		EXP#						
4A		CDEV#						
4B		RDEV#						
4C		CMDB#						
4D								
4E		JCB ID						
4F								
50		Command start time						
51								
52								
53								
54		Command Type						
55								
56		Target Type						
57		Reserved						
58		SCSI command						
59		SCSI command LBA						
5A								
5B								
5C								
5D								
5E		SCSI command Length						
5F								
60		Error Code						
61								
62								
63								
64		Error Code (EVENT)						
65								
66								
67								
68		Error Code (COMPLITION)						
69								
6A								
6B								
6C		Reserved						
⋮								
7F								

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*1: SCSI command code

Code	Command Name	Code	Command Name
00	TEST UNIT READY	28	READ (EXTEND)
03	REQUEST SENSE	2A	WRITE (EXTEND)
04	FORMAT UNIT	2E	WRITE AND VERIFY
07	REASSIGN BLOCKS	3B	WRITE BUFFER
0A	VERIFY	88	READ
12	INQUIRY	8A	WRITE
15	MODE SELECT	8E	WRITE AND VERIFY
1A	MODE SENSE	9E	READ CAPACITY
1B	START/STOP UNIT	FF	COMMAND is non-decision
1C	RECEIVE DIAGNOSTIC RESULT		
1D	SEND DIAGNOSTIC		

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Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 83 (Drive Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PK TYPE		MP#					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARAT	HST REP	HST REP	EXPLS
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26					Format (x'1')			
27	Reserved							
28	Reserved							
29								
2A	SCSI command							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	CDEV#							
2F	Reserved							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Exception Class				Reserved			
37	RDEV#							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte36: bit0-3 = D & Byte26: bit4-7 = 1 & Byte44 = 83 (Drive Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Time of occurrence							
41								
42								
43								
44	Type Cord (x‘83’)							
45	Reserved							
46								
47								
48	SAS Port#							
49	EXP#							
4A	CDEV#							
4B	RDEV#							
4C	CMDB#							
4D								
4E	JCB ID							
4F								
50	Command start time							
51								
52								
53								
54	Command Type							
55								
56	Target Type							
57	SCSI Status							
58	Sense Data (8byte)							
|								
5F								
60	SCSI RSP acquisition result							
61	Sense Key							
62	Additional Sense Code							
63	Additional Sense Code Qualifier							
64	Non-transfer number of bytes							
65								
66								
67								
68	Obstacle LBA of Sense Data							
69								
6A								
6B								
6C								
6D								
6E								
6F								
70	CDB							
|								
7F								

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Byte36: bit0-3 = E & Byte26: bit4-7 = 1 (Drive Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PK type		MP#					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SRAID	RCOPY	SEPARAT	HST REP	HST REP	EXPLS
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26					Format (x'1')			
27	Reserved							
28	Reserved							
29								
2A	SCSI command							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	CDEV#							
2F	Reserved							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Exception Class				Reserved			
37	RDEV#							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Reserved							
|								
3F								

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Byte36: bit0-3 = E & Byte26: bit4-7 = 1 (Drive Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Time of occurrence							
41								
42								
43								
44	Type Cord (x‘83’)							
45	Reserved							
46								
47								
48	SAS Port#							
49	EXP#							
4A	CDEV#							
4B	RDEV#							
4C	CMDB#							
4D								
4E	JCB ID							
4F								
50	Command start time							
51								
52								
53								
54	Command Type							
55								
56	Target Type							
57	SCSI Status							
58	Sense Data (8byte)							
|								
5F								
60	SCSI RSP acquisition result							
61	Sense Key							
62	Additional Sense Code							
63	Additional Sense Code Qualifier							
64	Non-transfer number of bytes							
65								
66								
67								
68	Obstacle LBA of Sense Data							
69								
6A								
6B								
6C								
6D								
6E								
6F								
70	CDB							
|								
7F								

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Byte26: b4-7 = F & Byte3C = F1 (DKC SIM) (1/3)

	0	1	2	3	4	5	6	7
00 | 05	Time stamp							
06	Format Message							
07	PK type	Processor ID						
08 | 09	System error code							
0A | 0B	JCB#							
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12 | 13	LDEV# low (LDEV# in Logical DKC)							
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16 | 17	Internal SSB log number							
18 | 19	Related failure log number							
1A | 1B	Related SIM log number							
1C | 1D	Related SSB log number							
1E	Reserved							
1F	SCB (x‘ ’)							
20 | 26	Reserved							
27	SIM sense record ID (x‘E0’)							
28	Range subject to the error (*1)				Range affected by repair (*2)			
29	Range affected by repair (*3)		Failure SPs (*4)	SPs in SSID (*5)	Failure SSIDs (*6)	Affected SSIDs (*7)	Status (*8)	0
2A	Resent SIM (*9)	‘0000000’						
2B | 2C	Hardware level (*10)							
2D	Isolation code (*11)							
2E	SSB ID (*12)	SIM sequence number						SVP ID (*13)
2F | 33	DKC serial number (x‘0CE5’ + DKC sequence number)							
34 | 35	SSID of self storage system							
36 | 37	Reference code (See “Reference code” table)							
38	Log and message control (*14)							
39	Program action code (x‘10’)							
3A	Dual frame	EDCC Mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR
3B	32 byte SSB (0)	0	0	0	0	Extended path	Storage path number	
3C	Message code (x‘F1’)							
3D | 3E	SSID of mate storage system							
3F	Not used							

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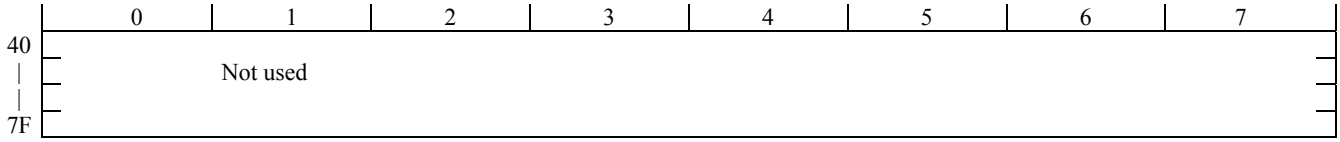
Byte26: b4-7 = F & Byte3C = F1 (DKC SIM) (2/3)



*1: Range subject to the error
x‘0’: Not used
x‘1’: Error range not known
x‘2’: SP error
x‘3’: CHL-I error
x‘4’: Not affect performance
x‘5 ~ F’: Not used

*2: Range affected by repair
x‘0’: Not used
x‘1’: Repair range not known
x‘2’: Repair does not affect performance
x‘3’: SP disabled during repair
x‘4’: SSID disabled during repair
x‘5 ~ F’: Not used

*3: Failure level
00: SERVICE ALERT
01: MODERATE ALERT
10: SERIOUS ALERT
11: ACUTE ALERT

*4: Failure SPs
0: 1SP
1: 2SP

*5: SPs in SSID
0: 2SP
1: 4SP

*6: Failure SSIDs
0: 1SSID
1: 2SSID

*7: Affected SSIDs
0: 1SSID
1: 2SSID

*8: Status
0: Reduction
1: Stop

*9: Resent SIM
0: Unresent SIM
1: Resent SIM

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Byte26: b4-7 = F & Byte3C = F1 (DKC SIM) (3/3)

*10: Hardware level

Bit 0 : Serial channel hardware level

① When Bit 0 is 0

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per Cluster
00 : 4
01 : 8
10 : Not used
11 : Not used
Bit 6 : NVS
0 : Without NVS
1 : With NVS
Bit 7 : Not used
Bit 8-10 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1,024MB
101 : 1,280MB
110 : 1,536MB
111 : Over 1,537MB
Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When Bit 0 is 1

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-7 : ChLs per Cluster
0000 : Parallel =4, serial =0
0001 : Parallel =8, serial =0
0010 : Parallel =4, serial =2
0100 : Parallel =4, serial =4
0110 : Parallel =0, serial =2
1000 : Parallel =0, serial =4
1010 : Parallel =0, serial =8
1100 : Parallel =0, serial =6
Bit 8 : Dual frame
0 : Dual frame
1 : Single frame
Bit 9-11 : Cache size
000 : Non Cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1,024MB
101 : 1,280MB
110 : 1,536MB
111 : Over 1,537MB
Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

*11: Isolation code

Byte 2D ≠ x‘00’ : Byte 36 and 37 are a symptom code.
Byte 2D = x‘00’ : Byte 36 and 37 are a symptom code. This byte is byte 2 of the isolation code.

*12: SSB ID

0: SVP
1: SP

*13: SVP ID

0: SVP1
1: SVP2

*14: Log and message control

Bit 0-2 : Not used
Bit 3 : Log mode(0)
Bit 4-5 : Logging action
00: Don’t log
01: Unconditionl log
10: Log only once
11: Log only if persistent
Bit 6-7 : Operator message
00: No message
01: Unconditional message
10: Send only once
11: Send only if persistent

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Byte26: b4-7 = F & Byte3C = F2 (CACHE SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK TYPE		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Reserved							
|								
26					Format (x‘F’)			
27	SIM sence code ID (x‘E0’)							
28	Range subject to the error (*1)				Range affected by repair (*2)			
29	Failure level (*3)		Failure SPs (*4)	SPs in SSID (*5)	Failure SSIDs (*6)	Affected SSIDs (*7)	Status (*8)	0
2A	Resent SIM (*9)	‘0000000’						
2B	Hardware level (*10)							
2C								
2D	Isolation code (*11)							
2E	SSB ID (*12)	SIM sequence number						SVP ID (*13)
2F	DKC serial number (x‘0CE5’ + DKC sequence number)							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Reference code (See “Reference code” table)							
37								
38	Log and message control (*14)							
39	Program action code (x‘10’)							
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR
3B	32 byte SSB (0)	0	0	0	0	Extended path	Storage path number	
3C	Message code (x‘F2’)							
3D	SSID of mate storage system							
3E								
3F	Not used							

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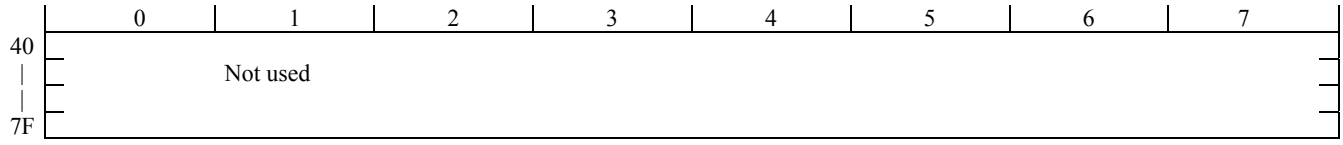
Byte26: b4-7 = F & Byte3C = F2 (CACHE SIM) (2/3)



*1: Range subject to the error
x‘0’: Not used
x‘1’: Error range not known
x‘2’: SP error
x‘3’: CHL-I error
x‘4’: Not affect performance
x‘5 ~ F’: Not used

*2: Range affected by repair
x‘0’: Not used
x‘1’: Repair range not known
x‘2’: Repair does not affect performance
x‘3’: SP disabled during repair
x‘4’: SSID disabled during repair
x‘5 ~ F’: Not used

*3: Failure level
00: SERVICE ALERT
01: MODERATE ALERT
10: SERIOUS ALERT
11: ACUTE ALERT

*4: Failure SPs
0: 1SP
1: 2SP

*5: SPs in SSID
0: 2SP
1: 4SP

*6: Failure SSIDs
0: 1SSID
1: 2SSID

*7: Affected SSIDs
0: 1SSID
1: 2SSID

*8: Status
0: Reduction
1: Stop

*9: Resent SIM
0: Unresent SIM
1: Resent SIM

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Byte26: b4-7 = F & Byte3C = F2 (CACHE SIM) (3/3)

*10: Hardware level
Bit 0 : Serial channel hardware level
① When Bit 0 is 0
Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per Cluster
00 : 4
01 : 8
10 : Not used
11 : Not used
Bit 6 : NVS
0 : Without NVS
1 : With NVS
Bit 7 : Not used
Bit 8-10 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1,024MB
101 : 1,280MB
110 : 1,536MB
111 : Over 1,537MB
Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When Bit 0 is 1
Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-7 : ChLs per Cluster
0000 : Parallel =4, serial =0
0001 : Parallel =8, serial =0
0010 : Parallel =4, serial =2
0100 : Parallel =4, serial =4
0110 : Parallel =0, serial =2
1000 : Parallel =0, serial =4
1010 : Parallel =0, serial =8
1100 : Parallel =0, serial =6
Bit 8 : Dual frame
0 : Dual frame
1 : Single frame
Bit 9-11 : Cache size
000 : Non Cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1,024MB
101 : 1,280MB
110 : 1,536MB
111 : Over 1,537MB
Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

*11: Isolation code
Byte 2D ≠ x‘00’ : Byte 36 and 37 are a symptom code.
Byte 2D = x‘00’ : Byte 36 and 37 are a symptom code. This byte is byte 2 of the isolation code.

*12: SSB ID
0: SVP
1: SP

*13: SVP ID
0: SVP1
1: SVP2

*14: Log and message control
Bit 0-2 : Not used
Bit 3 : Log mode(0)
Bit 4-5 : Logging action
00: Don’t log
01: Unconditionl log
10: Log only once
11: Log only if persistent
Bit 6-7 : Operator message
00: No message
01: Unconditional message
10: Send only once
11: Send only if persistent

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Byte26: b4-7 = F & Byte3C = FE (Device SIM) (1/2)

	0	1	2	3	4	5	6	7
00 | 05	Time stamp							
06	Format Message							
07	PK type	Processor ID						
08 | 09	System error code							
0A | 0B	JCB#							
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARAT	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12 | 13	LDEV# low (LDEV# in Logical DKC)							
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16 | 17	Internal SSB log number							
18 | 19	Related failure log number							
1A | 1B	Related SIM log number							
1C | 1D	Related SSB log number							
1E	Reserved							
1F	SCB							
20 | 26	Reserved							
27	SSB ID (*1)	SIM sequence number						SVP ID (*2)
28	Device exception (x‘1’)				Service message (x‘1’: Action, x‘C’: No Action)			
29	Failure level (*3)	‘000000’						
2A	Resent SIM (*4)	‘0000000’						
2B	Exception Class FRU List Code (x‘80’)							
2C	Hardware and Microcode Corequsite Indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (x‘05’)							
2F | 33	Drive serial number (x‘0CE5’ + DKC sequence number)							
34 | 35	SSID of self storage system							
36 | 37	Reference code (See “Reference code” table)							
38	Log and message control (*5)							
39	Program action code (x‘10’)							
3A	Dual frame	EDCC Mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR
3B	32 byte SSB (0)	0	0	0	0	Extended path	Storage path number	
3C	Message code (x‘FE’)							
3D | 3E	SSID of mate storage system							
3F	Not used							

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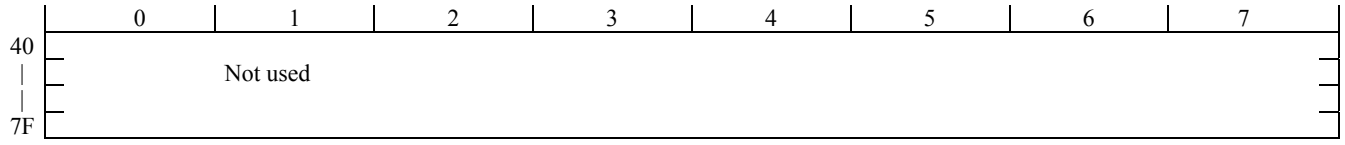
Byte26: b4-7 = F & Byte3C = FE (Device SIM) (2/2)



*1: SSB ID
0: SVP
1: SP

*2: SVP ID
0: SVP1
1: SVP2

*3: Failure level
00: SERVICE ALERT
01: MODERATE ALERT
10: SERIOUS ALERT
11: ACUTE ALERT

*4: Resent SIM
0: Unresent SIM
1: Resent SIM

*5: Log and message control
Bit 0-2 : Not used
Bit 3 : Log mode(0)
Bit 4-5 : Logging action
00: Don’t log
01: Unconditional log
10: Log only once
11: Log only if persistent
Bit 6-7 : Operator message
00: No message
01: Unconditional message
10: Send only once
11: Send only if persistent

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Byte26: b4-7 = F & Byte3C = FF (MEDIA SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PK type		Processor ID					
08	System error code							
09								
0A	JCB#							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARAT	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	PK information VLD	0
0F	SEMI-SYNC	RCU SIM	PORT#VLD	0	RCU#			
10	JCB ID							
11	LDEV# high (Logical DKC#)							
12	LDEV# low (LDEV# in Logical DKC)							
13								
14	CDEV# / PORT#							
15	RDEV# / PORT#							
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB (x‘ ’)							
20	Reserved							
|								
26					Format (x‘F’)			
27	SSB ID (*1)	SIM sequence number						SVP ID (*2)
28	Device exception (x‘1’)				Service message (x‘1’)			
29	Failure level (*3)	Media Maintenance Procedure Number (Correctable: x‘07’, Uncorrectable: x‘05’)						
2A	Resent SIM (*4)	‘0000000’						
2B	Exception Class FRU List Code (x‘80’)							
2C	Hardware and Microcode Corequsite Indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (Correctable : x‘87’, Uncorrectable : x‘85’)							
2F	Drive serial number (x‘0CE5’ + DKC sequence number)							
30								
31								
32								
33								
34	SSID of self storage system							
35								
36	Reference code (See “Reference code” table)							
37								
38	Log and message control (*5)							
39	Program action code (x‘10’)							
3A	Dual frame	EDCC Mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR
3B	32 byte SSB (0)	0	0	0	0	Extended path	Storage path number	
3C	Message code (x‘FF’)							
3D	SSID of mate storage system							
3E								
3F	Not used							

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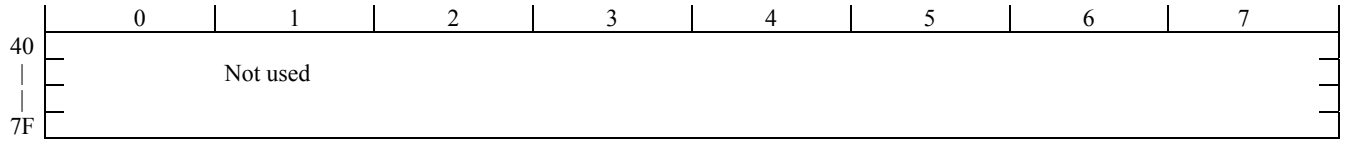
Byte26: b4-7 = F & Byte3C = FF (MEDIA SIM) (2/2)



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