Masterfile Documentation

T2000 Maintenance Manual 10/10

DOCUMENTATION REVISION LEVEL									
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D*T20001019010

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(13) Byte28=55 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x' 55' : LANC LM correctable error 0 (address=400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (DKA CHK1B) Byte28-31 Detail

(14) Byte28 = 56 : LANC LM correctable error 1

	0	1	2	3	4	5	6	7
28	Subcode : x'56' : LANC LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(15) Byte28=57 : i960 XR read address error

	0	1	2	3	4	5	6	7
28	Subcode : x' 57' : i960 XR read address error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(16) Byte28=58 : i960 XR write address error

	0	1	2	3	4	5	6	7
28	Subcode : x' 58' : i960 XR write address error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(17) Byte28=59 : LANC XR access error

	0	1	2	3	4	5	6	7
28	Subcode : x' 59' : LANC XR access error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E & Byte34 = X0 & Byte28 = 6X/7X (CHK1A/WCHK1 (SRAM P/K)) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'6X'/x'7X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number (Note 1)				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I) (Note 2)							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

(Note 1) Failed processor number for WCHK1

(Note 2) This information is not fixed until DKC reports SSB to HOST.

Byte27=8E & Byte34=X0 & Byte28=6X/7X (CHK1A/WCHK1 (SRAM P/K)) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address (1) when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected						(RSV)	(RSV)
44	RCHK::ERBYT							
	(RSV)	(RSV)	(RSV)	(RSV)	L-bus BE0-3 signal			
45	RCHK::ERORD							
	Data (0) before correction when LM access erroroccurred							
46	RCHK::ERORD							
	Data (1) before correction when LM access error occurred							
47	RCHK::ERORD							
	Data (2) before correction when LM access error occurred							
48	RCHK::ERORD							
	Data (3) before correction when LM access error occurred							
49	RCHK::ERORC							
	Check bit before correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8E & Byte34=X0 & Byte28=6X/7X (CHK1A/WCHK1 (SRAM P/K)) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	LANC→LM access CORREC		LANC→LM access CORREC ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::SCANER							
	Scan→LM access UNCOR ERR detect		Not used	Scan→LM Out of LM area	Scan→XR Invalid RD XR ADR	Scan→XR Invalid WR XR ADR	Not used	Not used
	Bank0	Bank1						
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	MIC::SRMERRSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1A detected at SRAM	CHK1B detected at SRAM	LAN access error detected
58	MIC::SRMERRSTS							
	Sequencer state error detected	Sequencer parity error detected	Out of mounting area in accessing	Write protected area in accessing	Parity error detected (00-07)	Parity error detected (10-17)	Parity error detected (20-27)	Parity error detected (30-37)
59	MIC::SRMERRADR							
	Error address in accessing to SRAM							
5A	MIC::SRMERRADR							
	Error address in accessing to SRAM							
5B	MIC::SRMERRADR							
	Error address in accessing to SRAM							
5C	MIC::SRMERRADR							
	Error address in accessing to SRAM						Write/Read flg	Command/ data flg
5D	RCHK::C1WSTS							
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	CHK1A detected in processing CHK1A	micro force WCHK1 detected
5E	MIC::MPCERRSTS							
	Not used	Not used	WCHK1 detected at MPCHK	CHK1A detected at MPCHK	parity error at timer	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
5F	MIC::LAST 1 IP							
	Last 1 IP address (0)							

Byte27=8E & Byte34=X0 & Byte28=6X/7X (CHK1A/WCHK1 (SRAM P/K)) (4/5)

	0	1	2	3	4	5	6	7
60	MIC::LAST 1 IP							
	Last 1 IP address (1)							
61	MIC::LAST 1 IP							
	Last 1 IP address (2)							
62	MIC::LAST 1 IP							
	Last 1 IP address (3)							
63	MIC::LAST 2 IP							
	Last 2 IP address (0)							
64	MIC::LAST 2 IP							
	Last 2 IP address (1)							
65	MIC::LAST 2 IP							
	Last 2 IP address (2)							
66	MIC::LAST 2 IP							
	Last 2 IP address (3)							
67	MIC::LAST 3 IP							
	Last 3 IP address (0)							
68	MIC::LAST 3 IP							
	Last 3 IP address (1)							
69	MIC::LAST 3 IP							
	Last 3 IP address (2)							
6A	MIC::LAST 3 IP							
	Last 3 IP address (3)							
6B	MIC::LAST 4 IP							
	Last 4 IP address (0)							
6C	MIC::LAST 4 IP							
	Last 4 IP address (1)							
6D	MIC::LAST 4 IP							
	Last 4 IP address (2)							
6E	MIC::LAST 4 IP							
	Last 4 IP address (3)							
6F	MIC::LAST 1 ADR							
	Last 1 access address (0)							

Byte27=8E & Byte34=X0 & Byte28=6X/7X (CHK1A/WCHK1 (SRAM P/K)) (5/5)

	0	1	2	3	4	5	6	7
70	MIC::LAST 1 ADR							
	Last 1 access address (1)							
71	MIC::LAST 1 ADR							
	Last 1 access address (2)							
72	MIC::LAST 1 ADR							
	Last 1 access address (3)							
73	MIC::LAST 2 ADR							
	Last 2 access address (0)							
74	MIC::LAST 2 ADR							
	Last 2 access address (1)							
75	MIC::LAST 2 ADR							
	Last 2 access address (2)							
76	MIC::LAST 2 ADR							
	Last 2 access address (3)							
77	RCHK::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	L bus W/R signal
78	RCHK::CHK1ASTS							
	i960→ Uncorrectable error detected in accessing to LM		i960→Write protected area	i960→Out of mounting area	Not used	Not used	LANC→ Write protected area	LANC→Out of mounting area
79	RCHK::CECTH							
	Limit number of LM correctable error							
7A	MIC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
7B	MIC::CHK1BSTS							
	XR0 CHK1B	XR1 CHK1B	XR2 CHK1B	XR3 CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK CHK1B
7C	MIC::MIC CHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7D	MIC::MIC CHK1STS							
	LAN hold time-out	Wait time-out	XR decode error (29A)	XR decode error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
7E	MIC ::ERR STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7F	MIC ::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(1) Byte28 = 60 : MP check error

	0	1	2	3	4	5	6	7
28	Subcode : x'60' : MP check error							
29	MIC::MPCERRSTS							
	(Not used)	(Not used)	WCHK1 detected at MPCHK	CHK1A detected at MPCHK	parity error at timer	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
2A	MIC::AREG							
	← Consistent data A register →							
2B	MIC::AREG							
	← Consistent data A register →							
2C	MIC::AREG							
	← Consistent data A register →							
2D	MIC::AREG							
	← Consistent data A register →							
2E	MIC::BREG							
	← Consistent data B register →							
2F	MIC::BREG							
	← Consistent data B register →							
30	MIC::BREG							
	← Consistent data B register →							
31	MIC::BREG							
	← Consistent data B register →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(2) Byte28 = 61 : Uncorrectable error when MP reads/writes LM data

	0	1	2	3	4	5	6	7
28	Subcode : x'61' : Uncorrectable error when MP reads/writes LM data							
29	RCHK::ERADR							
	← Address from L bus →							
2A	RCHK::ERADR							
	← Address from L bus →							
2B	RCHK::ERADR							
	← Address from L bus →							
2C	RCHK::ERADR							
	← Address from L bus →						(Not used)	(Not used)
2D	RCHK::ERORD							
	← Data before correction →							
2E	RCHK::ERORD							
	← Data before correction →							
2F	RCHK::ERORD							
	← Data before correction →							
30	RCHK::ERORD							
	← Data before correction →							
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(3) Byte28 = 62 : Write protection violated when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'62' : Write protection violated when MP accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMWRADRU							
	(Not used)	High limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	High limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
2F	RCHK::LMWRADRL							
	(Not used)	Low limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Low limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(4) Byte28 = 63 : Out of mounting area accessed when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'63' : Out of mounting area accessed when MP accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMADRLMT							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	High limit address of LM mounting area (higher order)
2E	RCHK::LMADRLMT							
	High limit address of LM mounting area (lower order)				(Not used)	(Not used)	(Not used)	(Not used)
2F	RCHK::ERSTS0							
	CMP ERR	(Not used)	READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan error	(Not used)	(Not used)
30	RCHK::SCANER							
	Scanning→Uncorrectable error detected in accessing to LM		(Not used)	Scanning→ Out of mounting area in accessing to LM	Scanning→ Invalid address in reading from XR	Scanning→ Invalid address in writing to XR	(Not used)	(Not used)
	Bank 0	Bank 1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(5) Byte28 = 64 : Write protection violated when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'64' : Write protection violated when LANC accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMWRADRU							
	(Not used)	High limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	High limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
2F	RCHK::LMWRADRL							
	(Not used)	Low limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Low limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(6) Byte28 = 65 : Out of mounting area accessed when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'65' : Out of mounting area accessed when LANC accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMADRLMT							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	High limit address of LM mounting area (higher order)
2E	RCHK::LMADRLMT							
	High limit address of LM mounting area (lower order)				(Not used)	(Not used)	(Not used)	(Not used)
2F	RCHK::ERSTS0							
	Inconsistency in i960 writing operation	(Not used)	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR access error	(Not used)	(Not used)
30	RCHK::SCANER							
	Scanning→Uncorrectable error detected in accessing to LM		(Not used)	Scanning→ Out of mounting area in accessing to LM	Scanning→ Invalid address in reading from XR	Scanning→ Invalid address in writing to XR	(Not used)	(Not used)
	Bank 0	Bank 1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(7) Byte28 = 66 : LM sequence error

	0	1	2	3	4	5	6	7
28	Subcode : x'66' : LM sequence error							
29	MIC::C1WSTS							
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	CHK1A detected in processing CHK1A	micro force WCHK1 detected
2A	MIC::LAST1IP							
	← last IP address →							
2B	MIC::LAST1IP							
	← last IP address →							
2C	MIC::LAST1IP							
	← last IP address →							
2D	MIC::LAST1IP							
	← last IP address →							
2E	MIC::LAST1ADR							
	← last access address →							
2F	MIC::LAST1ADR							
	← last access address →							
30	MIC::LAST1ADR							
	← last access address →							
31	MIC::LAST1ADR							
	← last access address →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(8) Byte28 = 67 : LM sequence parity error

	0	1	2	3	4	5	6	7
28	Subcode : x'67' : LM sequence parity error							
29	MIC::C1WSTS							
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	CHK1A detected in processing CHK1A	micro force WCHK1 detected
2A	MIC::LAST1IP							
	← last IP address →							
2B	MIC::LAST1IP							
	← last IP address →							
2C	MIC::LAST1IP							
	← last IP address →							
2D	MIC::LAST1IP							
	← last IP address →							
2E	MIC::LAST1ADR							
	← last access address →							
2F	MIC::LAST1ADR							
	← last access address →							
30	MIC::LAST1ADR							
	← last access address →							
31	MIC::LAST1ADR							
	← last access address →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(9) Byte28 = 68 : SRAM CHK1A

	0	1	2	3	4	5	6	7
28	Subcode : x'68' : SRAM CHK1A							
29	MIC::C1WSTS						MIC::SRMMODE	
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	size of SRAM mounting area	
2A	MIC::SRMERRSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHK1A detected at SRAM	CHK1B detected at SRAM	LAN access error detected
2B	MIC::SRMERRSTS							
	sequencer state error detected	sequencer parity error detected	Out of mounting area in accessing to SRAM	Write protected area in accessing to SRAM	parity error detected in reading from SRAM (00-07)	parity error detected in reading from SRAM (10-17)	parity error detected in reading from SRAM (20-27)	parity error detected in reading from SRAM (30-37)
2C	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2D	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2E	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2F	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→						Write/Read flg in accessing to SRAM	command/ data flg in accessing to SRAM
30	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
31	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK CHK1B

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(10) Byte28 = 69 : DRAM CHK1A

	0	1	2	3	4	5	6	7
28	Subcode : x'69' : DRAM CHK1A							
29	MIC::C1WSTS						MIC::SRMMODE	
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	size of SRAM mounting area	
2A	RCHK::ERADR							
	← Address from L bus →							
2B	RCHK::ERADR							
	← Address from L bus →							
2C	RCHK::ERADR							
	← Address from L bus →							
2D	RCHK::ERADR							
	← Address from L bus →						(Not used)	(Not used)
2E	RCHK::ERSYD							
	← Syndrom when LM access error detected →							
2F	RCHK::ERWR							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	L bus W/R signal
30	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
31	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(11) Byte28 = 71 : Uncorrectable error when MP reads/writes LM data

	0	1	2	3	4	5	6	7
28	Subcode : x'71' : Uncorrectable error when MP reads/writes LM data							
29	RCHK::ERADR							
	← Address from L bus →							
2A	RCHK::ERADR							
	← Address from L bus →							
2B	RCHK::ERADR							
	← Address from L bus →							
2C	RCHK::ERADR							
	← Address from L bus →						(Not used)	(Not used)
2D	RCHK::ERORD							
	← Data before correction →							
2E	RCHK::ERORD							
	← Data before correction →							
2F	RCHK::ERORD							
	← Data before correction →							
30	RCHK::ERORD							
	← Data before correction →							
31	RCHK::ERORC							
	← Check bit before correction →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(12) Byte28 = 72 : Write protection violated when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'72' : Write protection violated when MP accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMWRADRU							
	(Not used)	High limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	High limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
2F	RCHK::LMWRADRL							
	(Not used)	Low limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Low limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(13) Byte28 = 73 : Out of mounting area accessed when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'73' : Out of mounting area accessed when MP accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMADRLMT							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	High limit address of LM mounting area (higher order)
2E	RCHK::LMADRLMT							
	High limit address of LM mounting area (lower order)				(Not used)	(Not used)	(Not used)	(Not used)
2F	RCHK::ERSTS0							
	Inconsistency in i960 writing operation	(Not used)	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR access error	(Not used)	(Not used)
30	RCHK::SCANER							
	Scanning→Uncorrectable error detected in accessing to LM		(Not used)	Scanning→ Out of mounting area in accessing to LM	Scanning→ Invalid address in reading from XR	Scanning→ Invalid address in writing to XR	(Not used)	(Not used)
	Bank 0	Bank 1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(14) Byte28 = 74 : Write protection violated when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'74' : Write protection violated when LANC accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMWRADRU							
	(Not used)	High limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	High limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
2F	RCHK::LMWRADRL							
	(Not used)	Low limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Low limit address of writable LM mounting area (lower order)						(Not used)	(Not used)
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(15) Byte28 = 75 : Out of mounting area accessed when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x'75' : Out of mounting area accessed when LANC accesses to LM							
29	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2D	RCHK::LMADRLMT							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)
2E	RCHK::LMADRLMT							
	High limit address of LM mounting area (higher order)				(Not used)	(Not used)	(Not used)	(Not used)
2F	RCHK::ERSTS0							
	Inconsistency in i960 writing operation	(Not used)	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR access error	(Not used)	(Not used)
30	RCHK::SCANER							
	Scanning→Uncorrectable error detected in accessing to LM		(Not used)	Scanning→ Out of mounting area in accessing to LM	Scanning→ Invalid address in reading from XR	Scanning→ Invalid address in writing to XR	(Not used)	(Not used)
	Bank 0	Bank 1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error detected in accessing to LM		i960→Write protected area in accessing to LM	i960→Out of mounting area in accessing to LM	(Not used)	(Not used)	LANC→ Write protected area in accessing to LM	LANC→ Out of mounting area in accessing to LM
	Bank 0	Bank 1						

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(16) Byte28 = 76 : LM sequence error

	0	1	2	3	4	5	6	7
28	Subcode : x'76' : LM sequence error							
29	MIC::C1WSTS							
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	CHK1A detected in processing CHK1A	micro force WCHK1 detected
2A	MIC::LAST1IP							
	← last IP address →							
2B	MIC::LAST1IP							
	← last IP address →							
2C	MIC::LAST1IP							
	← last IP address →							
2D	MIC::LAST1IP							
	← last IP address →							
2E	MIC::LAST1ADR							
	← last access address →							
2F	MIC::LAST1ADR							
	← last access address →							
30	MIC::LAST1ADR							
	← last access address →							
31	MIC::LAST1ADR							
	← last access address →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(8) Byte28 = 77 : LM sequencer parity error

	0	1	2	3	4	5	6	7
28	Subcode : x'77' : LM sequencer parity error							
29	MIC::C1WSTS							
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	CHK1A detected in processing CHK1A	micro force WCHK1 detected
2A	MIC::LAST1IP							
	← last IP address →							
2B	MIC::LAST1IP							
	← last IP address →							
2C	MIC::LAST1IP							
	← last IP address →							
2D	MIC::LAST1IP							
	← last IP address →							
2E	MIC::LAST1ADR							
	← last access address →							
2F	MIC::LAST1ADR							
	← last access address →							
30	MIC::LAST1ADR							
	← last access address →							
31	MIC::LAST1ADR							
	← last access address →							

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(18) Byte28 = 78 : SRAM CHK1A

	0	1	2	3	4	5	6	7
28	Subcode : x'78' : SRAM CHK1A							
29	MIC::C1WSTS						MIC::SRMMODE	
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	size of SRAM mounting area	
2A	MIC::SRMERRSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHK1A detected at SRAM	CHK1B detected at SRAM	LAN access error detected
2B	MIC::SRMERRSTS							
	sequencer state error detected	sequencer parity error detected	Out of mounting area in accessing to SRAM	Write protected area in accessing to SRAM	parity error detected in reading from SRAM (00-07)	parity error detected in reading from SRAM (10-17)	parity error detected in reading from SRAM (20-27)	parity error detected in reading from SRAM (30-37)
2C	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2D	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2E	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→							
2F	MIC::SRMERRADR							
	←---------- Error address in accessing to SRAM ----------→						Write/Read flg in accessing to SRAM	command/ data flg in accessing to SRAM
30	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
31	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK CHK1B

Byte27 = 8E (CHK1A/WCHK1 (SRAM P/K)) Byte28-31 Detail

(19) Byte28 = 79 : DRAM CHK1A

	0	1	2	3	4	5	6	7
28	Subcode : x'79' : DRAM CHK1A							
29	MIC::C1WSTS						MIC::SRMMODE	
	other CHK1A detected	other WCHK1 detected	CHK1A detected at MPCHK	CHK1A detected at SRAM	CHK1A detected at RCHK	WCHK1 detected at MPCHK	size of SRAM mounting area	
2A	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2B	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2C	RCHK::ERADR							
	←---------- Address from L bus ----------→							
2D	RCHK::ERADR							
	←---------- Address from L bus ----------→						(Not used)	(Not used)
2E	RCHK::ERSYD							
	←---------- Syndrom when LM access error detected ----------→							
2F	RCHK::ERWR							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	L bus W/R signal
30	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
31	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17

Byte27 = 8E & Byte34 = X0 & Byte28 = 8X (CHA CHK1B (SRAM P/K)) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'8X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8E & Byte34=X0 & Byte28=8X (CHA CHK1B (SRAM P/K)) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address (1) when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected							
44	RCHK::ERBYT				MIC::CHK1BBE			
	L-bus BE0-3 signal				L-bus BE0-3 signal when error detected			
45	MIC::CHK1BADRS							
	Error address when error detected							
46	MIC::CHK1BADRS							
	Error address when error detected							
47	MIC::CHK1BADRS							
	Error address when error detected							
48	MIC::CHK1BADRS							
	Error address when error detected						Write/Read flg	command/ data flg
49	RCHK::ERORC							
	Check bit befor correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8E & Byte34=X0 & Byte28=8X (CHA CHK1B (SRAM P/K)) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		LANC→LM access UNCORR ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	L bus W/R signal
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	MIC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/PBA CHK1B error	SMP/DRR CHK1B error	MIC CHK1B error
58	MIC::CHK1BSTS							
	XR0:EADP CHK1B error	XR1:BSA0 CHK1B error	XR2:BSA1 CHK1B error	XR3 CHK1B ERR (0)	XR4 CHK1B ERR (0)	XR5 CHK1B ERR (0)	Not used	RCHK1 CHK1B error
59	MIC::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity ER	Hard timer parity ER	Wait timer parity ER	Hold timer parity ER
5A	MIC::MICCHK1STS							
	LAN hold timer parity ER	Wait time-out	XR decoder ERR (29A)	XR decoder ERR (3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
5B	MIC::TIMER							
	Timer#0 parity error	Timer#1 arity error	Timer#2 arity error	Timer#3 arity error	Timer#4 arity error	Timer#5 arity error	Timer#6 arity error	Not used
5C	MIC::ABTERR				MIC::MPCERRSTS			
	Not used	Transfer start time-out	LIVEINS delay timer PE	Transfer start timer PE	parity error at timer	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
5D	MIC::XRDBSPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR bus ADR P-ERR (24-27)	XR bus ADR P-ERR (30-37)
5E	MIC::LBUSPER				MIC::MICPERRSTS			
	Local DT bus P-ERR (00-07)	Local DT bus P-ERR (10-17)	Local DT bus P-ERR (20-27)	Local DT bus P-ERR (30-37)	Not used	Not used	XR bus ADR parity ER (24-27)	XR bus ADR parity ER (30-37)
5F	MIC::XBUSPER							
	Not used	Not used	Not used	Not used	XR bus DT parity ER (00-07)	XR bus DT parity ER (10-17)	XR bus DT parity ER (20-27)	XR bus DT parity ER (30-37)

Byte27=8E & Byte34=X0 & Byte28=8X (CHA CHK1B (SRAM P/K)) (4/5)

	0	1	2	3	4	5	6	7
60	MIC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3
61	MIC::RSTSTS							
	Not used	Not used	Micro CHK1B pending	Micro CHK1A pending	Micro MCNRST2 pending	Micro MCNRST1 pending	Micro MPRST pending	Micro MNTRST pending
62	MIC::RSTSTS							
	Not used	Not used	Scan mode set pending	CHK1A pending	WCHK1 pending	SELRST pending	SYSRST pending	P/S on reset pending
63	MIC::ARBCTL							
	LIVEINS count PE CHK test	XFR start timer PE CHK test	Sequencer reset	(RSV)	LIVEINS input SIG mask	CHK3 reset	DIAG mode	Arbier initiate
64	SMP::CHK1B							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
65	SMP::SMPERROR							
	Not used	Not used	Not used	Not used	Not used	Master CHK3 error	Slave CHK3 error	CHK1 error
66	SMP ::WAD							
	i960 address (0) for M bus access							
67	SMP ::WAD							
	i960 address (0) for M bus access							
68	SMP ::WAD							
	i960 address (0) for M bus access							
69	SMP ::WAD							
	i960 address (0) for M bus access							
6A	SMP ::WAT							
	Write data (0) for M bus access							
6B	SMP ::WAT							
	Write data (1) for M bus access							
6C	SMP ::WAT							
	Write data (2) for M bus access							
6D	SMP ::WAT							
	Write data (3) for M bus access							
6E	SMP ::WR/BE							
	Not used	Not used	Not used	Write/read	i960 byte enable for M bus access			
6F	SMP ::TXSEQ							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Master sequencer state

Byte27=8E & Byte34=X0 & Byte28=8X (CHA CHK1B (SRAM P/K)) (5/5)

	0	1	2	3	4	5	6	7
70	RCHK::TXSEQ							
	Master sequencer state(0)							
71	RCHK:: TXSEQ							
	Master sequencer state(1)							
72	RCHK::XFC							
	Data trasfer enable	Data transfer execute	(RSV)	(RSV)	CBP mode	CBF PTR increment inhibited	CACHE I/O REG access	SSD/ DKC200
73	RCHK::XFC							
	Data path 0	Data path 1	Data path 2	Data path 3	(RSV)	F-bus WID 0:8byte/ 1:4byte	F-bus BSA0 connect	F-bus BSA1 connect
74	RCHK::PCMD2							
	'1'	Bus mode			Transfer mode			
		Bus width 0:8,1:4b	FBUS0 enable	FBUS1 enable	0:Write 1:Read	2:Cache to cache 3:Double write		
75	RCHK::XFS0							
	CHA data transfer end	BSA0 retry request	BSA1 retry request	PACKET FLOW CNT REG STAT	CHK2	EADP CHK2	CHA CHK2	BSA0 CHK2
76	RCHK::XFS0							
	BSA1 CHK2	Truncation	Halt I/O	Search result DASD=CPU	Search result DASD>CPU	Search result DASD<CPU	MP REQ BSA0,1 retry	MP REQ BSA0,1 abort
77	RCHK::XFS1							
	1:PARAL 0:SERIAL	XFR mode0 (CHL BUS width)	XFR mode1 (Data XFR speed)	MP retry occurred	MP abort occurred	CHA abort occurred	Pseud ERR occurred (CHK1B)	Pseud ER occurred (CHK2)
78	RCHK::CHK1ASTS							
	NEXT SEG ADR REG status	BSA0 last packet XFR end	BSA1 last packet XFR end	BSA0 CHK1B	BSA1 CHK1B	Next SEG address wait	Packet flow CNT	MCN RST occurred
79	RCHK::XFS1							
	XR address 2 parity ER	XR address 3 parity ER	DBUS parity error 0	DBUS parity error 1	BBUS parity error 0	BBUS parity error 1	XR ADR decode error 2	XR ADR decode error 3
7A	RCHK::MPCHK1B							
	Clock error	Micro access error	Not used	Not used	Not used	Not used	Not used	Not used
7B	EADP::CCK10							
	XRAPER3	BEPER	DBUSPER3	BBUSPER3	XRADDECER	(RSV)	(RSV)	(RSV)
7C	RCHK::LMWRADRL							
	Address parity error	WR data bus(H) parity ER	WR data bus(L) parity ER	RD data bus(H) parity ER	RD data bus(L) parity ER	(RSV)	(RSV)	(RSV)
7D	EADP::CCK11							
	LCM BUSY	LCP STOP	LCP ADRCMP match	LCP TRACER stop	LCM detected ADPLCM ERR	LCM detected WCHK1	LCM path disable	Parallel chanel
7E	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7F	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(1) Byte28 = 81 : RCHA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'81' : RCHA CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	CHA::MPCHK1B							
	XR address 2 parity error	XR address 3 parity error	DBUS write data parity error 0	DBUS write data parity error 1	BBUS read data parity error 0	BBUS read data parity error 1	XR address 2 decode error	XR address 3 decode error
2C	CHA::MPCHK1B							
	CHK clock failure	Micro access error	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(2) Byte28 = 82 : SMP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'82' : SMP CHK1B: XR bus parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	MIC::CHK1B							
	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	Address byte 3 parity error	Data byte 0 parity error	Data byte 1 parity error	Data byte 2 parity error	Data byte 3 parity error
2C	MIC::TIMER							
	Timer #0 parity error	Timer #1 parity error	Timer #2 parity error	Timer #3 parity error	Timer #4 parity error	Timer #5 parity error	Timer #6 parity error	(Not used)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(1) Byte28 = 83 : ADP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'83' : ADP CHK1B: XR bus parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	EADP::CCK10							
	XRAPER3	BEPER	DBUSPER3	BBUSPER3	XRADDECER	(RSV)	(RSV)	(RSV)
2C	EADP::CCK11							
	i960 I/F address parity error	i960 I/F WT DT(H) parity error	i960 I/F WT DT(L) parity error	i960 I/F RD DT(H) parity error	i960 I/F RD DT(L) parity error	(RSV)	(RSV)	(RSV)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(4) Byte28 = 84 : BSA0 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'84' : BSA0 CHK1B: MP access error/bus mode parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	MP address parity error	MP WR data (H) parity error	MP WR data (L) parity error	MP RD data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2C	BSA1::CK1BST0							
	MP address parity error	MP WR data (H) parity error	MP WR data (L) parity error	MP RD data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(5) Byte28 = 85 : BSA1 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'85' : BSA1 CHK1B: MP access error/bus mode parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	MP address parity error	MP WR data (H) parity error	MP WR data (L) parity error	MP RD data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2C	BSA1::CK1BST0							
	MP address parity error	MP WR data (H) parity error	MP WR data (L) parity error	MP RD data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(6) Byte28 = 86 : MIC CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'86' : MIC CHK1B: internal counter timer error/LAN hold time-out/XR wait time-out/XR bus access error/L bus data parity error/arbiter data parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MIC:: MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2D	MIC::TIMER							
	Timer #0 parity error	Timer #1 parity error	Timer #2 parity error	Timer #3 parity error	Timer #4 parity error	Timer #5 parity error	Timer #6 parity error	(Not used)
2E	MIC::ABTERR							
	SQST08	SQST09	SQST10	(Not used)	(Not used)	Transfer start time-out error	LIVE INS delay timer parity error	Transfer start time-out timer parity error
2F	MIC::XADRSPER							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	XR address parity error (24-27)	XR address parity error (30-37)
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(7) Byte28 = 87 : RCHK CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'87' : RCHKCHK1B: MP LM data error/XR register R/W address error/LANC access error/refresh address error/L bus parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	RCHK::CHK1BSTS							
	i960→Correctable error is over the specified value in accessing to LM		i960→ Invalid address in reading from XR	i960→ Invalid address in writing to XR	(Not used)	(Not used)	(Not used)	(Not used)
	Bank 0	Bank 1						
2C	RCHK::CHK1BSTS							
	LANC→Correctable error is over the specified value in accessing to LM		LANC→Uncorrectable error detected in accessing to LM		LANC→XR invalid address	(Not used)	(Not used)	(Not used)
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	RCHK::CHK1BSTS							
	Refresh address register parity error	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)
2E	RCHK::ERORD							
	←---------- Data before correction ----------→							
2F	RCHK::ERORD							
	←---------- Data before correction ----------→							
30	RCHK::ERORD							
	←---------- Data before correction ----------→							
31	RCHK::ERORD							
	←---------- Data before correction ----------→							

Byte27 = 8E (CHA CHK1B (SRAM P/K)) Byte28-31 Detail

(8) Byte28 = 88 : PBA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'88' : PBA CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/PBA CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 CHK1B (0)	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	Not used							
2C	Not used							
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E & Byte34 = X0 & Byte28 = 9X (DKA CHK1B (SRAM P/K)) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'9X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8E & Byte34=X0 & Byte28=9X (DKA CHK1B (SRAM P/K)) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address (1) when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected							
44	RCHK::ERBYT				MIC::CHK1BBE			
	L-bus BE0-3 signal				L-bus BE0-3 signal when error detected			
45	MIC::CHK1BADRS							
	Error address when error detected							
46	MIC::CHK1BADRS							
	Error address when error detected							
47	MIC::CHK1BADRS							
	Error address when error detected							
48	MIC::CHK1BADRS							
	Error address when error detected						Write/Read flg	command/ data flg
49	RCHK::ERORC							
	Check bit befor correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8E & Byte34=X0 & Byte28=9X (DKA CHK1B (SRAM P/K)) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI time-out	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		LANC→LM access UNCORR ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	L bus W/R signal
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	MIC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B error	SMP/DRR CHK1B error	MIC CHK1B error
58	MIC::CHK1BSTS							
	XR0:EADP CHK1B error	XR1:BSA0 CHK1B error	XR2:BSA1 CHK1B error	XR3 CHK1B ERR (0)	XR4 CHK1B ERR (0)	XR5 CHK1B ERR (0)	Not used	RCHK1 CHK1B error
59	MIC::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity ER	Hard timer parity ER	Wait timer parity ER	Hold timer parity ER
5A	MIC::MICCHK1STS							
	LAN hold timer parity ER	Wait time-out	XR decoder ERR (29A)	XR decoder ERR (3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
5B	MIC::TIMER							
	Timer#0 parity error	Timer#1 arity error	Timer#2 arity error	Timer#3 arity error	Timer#4 arity error	Timer#5 arity error	Timer#6 arity error	Not used
5C	MIC::ABTERR				MIC::MPCERRSTS			
	Not used	Transfer start timeout	LIVEINS delay timer PE	Transfer start timer PE	parity error at timer	A/B REG inconsistent check error	A/R REG write time-out	A/B REG access sequence error
5D	MIC::XRDBSPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR bus ADR P-ERR (24-27)	XR bus ADR P-ERR (30-37)
5E	MIC::LBUSPER				MIC::MICPERRSTS			
	Local DT bus P-ERR (00-07)	Local DT bus P-ERR (10-17)	Local DT bus P-ERR (20-27)	Local DT bus P-ERR (30-37)	Not used	Not used	XR bus ADR parity ER (24-27)	XR bus ADR parity ER (30-37)
5F	MIC::XBUSPER							
	Not used	Not used	Not used	Not used	XR bus DT parity ER (00-07)	XR bus DT parity ER (10-17)	XR bus DT parity ER (20-27)	XR bus DT parity ER (30-37)

Byte27=8E & Byte34=X0 & Byte28=9X (DKA CHK1B (SRAM P/K)) (4/5)

	0	1	2	3	4	5	6	7
60	RCHK::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3
61	RCHK::RSTSTS							
	Not used	Not used	Micro CHK1B pending	Micro CHK1A pending	Micro MCNRST2 pending	Micro MCNRST1 pending	Micro MPRST pending	Micro MNTRST pending
62	RCHK::RSTSTS							
	Not used	Not used	Scan mode set pending	CHK1A pending	WCHK1 pending	SELRST pending	SYSRST pending	P/S on reset pending
63	RCHK::ARBCTL							
	LIVEINS count PE CHK test	XFR start timer PE CHK test	Sequencer reset	(RSV)	LIVEINS input SIG mask	CHK3 reset	DIAG mode	Arbier initiate
64	RCHK::CHK1B							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
65	RCHK::SMPERROR							
	Not used	Not used	Not used	Not used	Not used	Master CHK3 error	Slave CHK3 error	CHK1 error
66	SMP ::WAD							
	i960 address (0) for M bus access							
67	SMP ::WAD							
	i960 address (1) for M bus access							
68	SMP ::WAD							
	i960 address (2) for M bus access							
69	SMP ::WAD							
	i960 address (3) for M bus access							
6A	DRR ::STATUS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	CHK1B	Force transfer end	Pseud error
6B	DRR ::ESTA0							
	Unused register WR error	RD only register WR error	Side A A REG WR error	Side B B REG WR error	Address parity error	Byte access error	Input data parity ER	Output data parity ER
6C	DRR ::ESTA0							
	Addres decode error	Clock phase error	(RSV)	(RSV)	(RSV)	(RSV)	BSA0 CHK1	BSA1 CHK1
6D	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
6E	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
6F	DRR ::MODE4							
	Micro I/F ADR PRTY reversed	Micro I/F inout DT reversed	Micro I/F output DT reversed	S-BUS G-ID PRTY reversed	BSA I/F mode PRTY reversed	BSA I/F CMD ID P reversed	BSA I/F IN DT P reversed	BSA I/F OUT DT P reversed

Byte27=8E & Byte34=X0 & Byte28=9X (DKA CHK1B (SRAM P/K)) (5/5)

	0	1	2	3	4	5	6	7
70	SCA0::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 parity ER	Write data 1 parity ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
71	SCA0::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
72	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
73	BSA1::CK1BSTS0							
	MP addres parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
74	SCA1::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
75	SCA1::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
76	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
77	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
78	SCA2::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
79	SCA2::CHKB							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
7A	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7B	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7C	SCA3::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
7D	SCA3::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
7E	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7F	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(1) Byte28 = 91 : DRR CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'91' : DRR CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2C	DDR::STATUS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	CHK1B	Transfer forcibly terminated	Pseudo-failure occurred
2D	DRR::ESTA0							
	Unused register write error	Read-dedicated register write error	A register write error in execution of side-A	B register write error in execution of side-B	Address parity error	Byte access error	Input data parity error	Output data parity error
2E	DRR::CK1BSTS0							
	Address decode error	Clock phase error	(RSV)	(RSV)	(RSV)	(RSV)	BSA0 CHK1 error	BSA1 CHK1 error
2F	BSA0::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
30	BSA1::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
31	DRR::MODE4							
	Micro I/F address parity reversed	Micro I/F input data parity reversed	Micro I/F output data parity reversed	S-BUS grant ID parity reversed	BSA I/F mode signal parity reversed	BSA I/F command ID parity reversed	BSA I/F input data parity reversed	BSA I/F output data parity reversed

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(2) Byte28 = 92 : SMP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'92' : SMP CHK1B: XR bus parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	SMP::CHK1B							
	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	Address byte 3 parity error	Data byte 0 parity error	Data byte 1 parity error	Data byte 2 parity error	Data byte 3 parity error
2C	MIC::TIMER							
	Timer #0 parity error	Timer #1 parity error	Timer #2 parity error	Timer #3 parity error	Timer #4 parity error	Timer #5 parity error	Timer #6 parity error	(Not used)
2D	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC::XRADRPER							
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(3) Byte28 = 93 : SCA0 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'93' : SCA0 CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	SCA0::CHK1B							
	XR address (H) parity error	XR address (L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error (H)	Address decode error (L)
2C	SCA0::CHK1B							
	8-phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10-phase clock error	(Not used)	(Not used)	(Not used)
2D	BSA0::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2E	BSA1::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2F	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hardtimer parity error	Wait timer parity error	Hold timer parity error
30	MIC::CHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC::MBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(4) Byte28 = 94 : SCA1 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'94' : SCA1 CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	SCA1::CHK1B							
	XR address (H) parity error	XR address (L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error (H)	Address decode error (L)
2C	SCA1::CHK1B							
	8-phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10-phase clock error	(Not used)	(Not used)	(Not used)
2D	BSA1::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2E	BSA1::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2F	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC::MBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(5) Byte28 = 95 : SCA2 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'95' : SCA2 CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	SCA2::CHK1B							
	XR address (H) parity error	XR address (L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error (H)	Address decode error (L)
2C	SCA2::CHK1B							
	8-phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10-phase clock error	(Not used)	(Not used)	(Not used)
2D	BSA2::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2E	BSA2::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2F	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC::MBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(6) Byte28 = 96 : SCA3 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'96' : SCA3 CHK1B: XR bus access error/internal clock error/micro access error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	SCA3::CHK1B							
	XR address (H) parity error	XR address (L) parity error	Write data 0 parity error	Write data 1 parity error	Read data 0 parity error	Read data 1 parity error	Address decode error (H)	Address decode error (L)
2C	SCA3::CHK1B							
	8-phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10-phase clock error	(Not used)	(Not used)	(Not used)
2D	BSA3::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2E	BSA3::CK1BSTS0							
	MP address parity error	MP write data H-side parity error	MP write data L-side parity error	MP read data parity error	Higher bus mode parity error	(Not used)	(Not used)	(Not used)
2F	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC::MBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(7) Byte28 = 97 : MIC CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'97' : MIC CHK1B: internal counter timer error/LAN hold time-out/XR wait time-out/XR bus access error/L bus data parity error/arbiter data parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	(Not used)	RCHK1 CHK1B
2B	MIC::MICCHK1STS							
	(Not used)	(Not used)	(Not used)	(Not used)	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	MIC::MICCHK1STS							
	LAN hold time-out	Wait time-out	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2D	MIC::TIMER							
	Timer #0 parity error	Timer #1 parity error	Timer #2 parity error	Timer #3 parity error	Timer #4 parity error	Timer #5 parity error	Timer #6 parity error	(Not used)
2E	MIC::ABTERR							
	SQST08	SQST09	SQST10	(Not used)	(Not used)	Transfer start time-out error	LIVE INS delay timer parity error	Transfer start time-out timer parity error
2F	MIC::XADRSPER							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	XR address parity error (24-27)	XR address parity error (30-37)
30	MIC::XBUSDTPER							
	(Not used)	(Not used)	(Not used)	(Not used)	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSDTPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E (DKA CHK1B (SRAM P/K)) Byte28-31 Detail

(8) Byte28 = 98 : RCHK CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x'98' : RCHKCHK1B: MP LM data error/XR register R/W address error/LANC access error/refresh address error/L bus parity error							
29	MIC::CHK1BSTS							
	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	(Not used)	RCHK1 CHK1B
2B	RCHK::CHK1BSTS							
	i960→Correctable error is over the specified value in accessing to LM		i960→ Invalid address in reading from XR	i960→ Invalid address in writing to XR	(Not used)	(Not used)	(Not used)	(Not used)
	Bank 0	Bank 1						
2C	RCHK::CHK1BSTS							
	LANC→Correctable error is over the specified value in accessing to LM		LANC→Uncorrectable error detected in accessing to LM		LANC→XR invalid address	(Not used)	(Not used)	(Not used)
	Bank 0	Bank 1	Bank 0	Bank 1				
2D	RCHK::CHK1BSTS							
	Refresh address register parity error	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)	(Not used)
2E	RCHK::ERORD							
	←---------- Data before correction ----------→							
2F	RCHK::ERORD							
	←---------- Data before correction ----------→							
30	RCHK::ERORD							
	←---------- Data before correction ----------→							
31	RCHK::ERORD							
	←---------- Data before correction ----------→							

Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (Microprogram detected WCHK1) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'F0')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID (See following pages)							
33	Routine ID (See following pages)							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	Free area							
7F								

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(1) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	Failure section information							
2B								
2C	Bus mode information							
2D	Shared memory data informatin							
2E								
2F								
30	CHK3 status information							
31	Master error information							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 32' : Error procedure aid
Routine ID : x' 51' : CHK3 in initializing
x' 52' : CHK3 in scanning
x' 53' : Unknown CHK3
x' 54' : CHK3 threshold exceeded
x' 55' : CHK3 in main recovery process
x' 56' : CHK3 in slave proces
x' 57' : Other function failed in CHK3 process
x' 58' : Reconstruction failed in CHK3 process
x' 59' : Making SSB failed in CHK3 interruption process
x' 5A' : Making CHK3 SIM failed
x' 5B' : Making SSB failed in CHK3 error process
x' 5C' : System down in CHK3 process
x' 5D' : MP down because reset CHK3 impossibly

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(2) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	Not used							
2B	Not used							
2C	Not used							
2D	Not used							
2E	Not used							
2F	Not used							
30	Not used							
31	Not used							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 32' : Error procedure aid
Routine ID : x' 81' : Unknown CHA CHK3
x' 82' : Unknown DKA CHK3
x' F1' : CHK1A threshold exdeeded
x' F4' : CHK1B threshold exceeded
x' F7' :None MP
x' F8' :No logical error information when pseudo-WCHK1 detected
x' FB' : CHK1A detected (execte REBOOT)

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(3) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	Return value of arbiter process							
2B								
2C								
2D								
2E								
2F	Not used							
30	Not used							
31	Not used							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 32' : Error procedure aid
Routine ID : x' C1' : Arbiter process failed in cluster failure

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(4) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	Access test bit map (initial value)							
2B								
2C								
2D								
2E	Access test bit map for succeeded section							
2F								
30								
31								
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 32' : Error procedure aid
Routine ID : x' C2' : No last path in cluster failure

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(5) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	Interruption information							
2B								
2C								
2D								
2E	CHK1B status information							
2F								
30								
31	Master error information							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 32' : Error procedure aid
Routine ID : x' F5' : CHK1B in CHK3
x' F6' : No error CHK3
x' F9' : Reser CHK3 impossibly

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(6) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x' F0' : Micro WCHK1							
29	Not used							
2A	INITYPER (x' 49 4E 49 54 59 45 52')							
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x' 80' : CHA/DKA kernael
Routine ID : x' 00' : Invalid reset cause

Byte27=8 E (Micro WCHK1) Byte28-31 Detail

(7) Byte28=F0 : Micro WCHK1 (Note 1)

	0	1	2	3	4	5	6	7
28	Subcode : x'F0' : Micro WCHK1							
29	Not used							
2A	WCHK1 type code							
2B	Reserved							
2C	Initialize interface information							
2D								
2E	Reset type code							
2F								
30	1st reset type code							
31	Reset SSB type code							
32	Module ID (Note 2)							
33	Routine ID (Note 2)							

(Note 1) This format is soecfied by byte 32 and 33.

(Note 2) Module ID : x'16' : Reset
Routine ID : x'27' : CHK1B in initializing
Routine ID : x'28' : Force Reset in initializing
Routine ID : x'29' : Initernal Reset in initializing
Routine ID : x'2f' : CHK3 in initializing
Routine ID : x'32' : Logical Inconsistency Reset in initializing
Routine ID : x'33' : Live Ins in initializing
Routine ID : x'34' : Power Failure Reset in initializing
Routine ID : x'37' : Fault Reset in initializing
Routine ID : x'60' : Internal Reset Loop in Resetting
Routine ID : x'61' : Logical Inconsistency Reset Loop in Resetting
Routine ID : x'62' : CHK1B Loop in Resetting
Routine ID : x'63' : CHK3 Loop in Resetting
Routine ID : x'64' : CHK1B unrecoverable
Routine ID : x'65' : Fault Reset Loop in Resetting
Routine ID : x'66' : CHK2A Reset
Routine ID : x'8e' : Force WCHK1 (by another MP)

Byte27 = 8E & Byte34 = X0 & Byte28 = F1 (Microprogram CHK1A) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'F0')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID (See following pages)							
33	Routine ID (See following pages)							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	Free area							
7F								

Byte27=8E (Microprogram CHK1A) Byte28-31 Detail

(1) Byte32·33 = x'165X' : Microprogram simulated CHK1A for error recovery by REBOOT.

	0	1	2	3	4	5	6	7
28	Subcode : x'F1' : Microprogram CHK1A							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 wrote operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E & Byte34 : bit4-7=1 (Selective Reset) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure Log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x' 8')				Message (x' E')			
28	LPN							
29	DCN status							
	Force device busy	Channel connect request	Command chain execute	Path reserve	Stack status	Sense pending	Long Busy (Command process)	Processor connect
2A	DCN status							
	Single path mode	Gurant path mode	MCB queuing	(RSV)	Load balance control	(RSV)	(RSV)	(RSV)
2B	DCN flag							
	RST NTF/ RST ALG SSB PND	Pin Data pending	(RSV)	(RSV)	ODE pending	RSQ pending	SCI/SCE pending	PCH pending
2C	LCT initiation cause							
	0:Ready 1:Not ready	0:Disable 1:Enable	0:No SNS 1:64SNS pending	0:Mount 1:Not mount	0:No RST ALG LPN 1:Exist	0:No SYS RST LPN 1:Exist	0:No stack 1:Exist	0:No wait SNS 1:Exist
2D	LCT initiation cause							
	0:No wait-RI 1:Exist	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	0:Others 1:DEV BSY JOB

Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (2/3)

	0	1	2	3	4	5	6	7
2E	Command interface flag							
	Pending exist	SCE(RSP)	(RSV)	(RSV)	ODE pending	RSQ pending	SCI pending	PCH pending
2F	Command code							
30	Internal SSB log number							
31								
32	Related reset detailed log number							
33								
34	Processor number				Message code (x'1')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A diference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x'00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (from LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=1 (Selective Reset) (3/3)

	0	1	2	3	4	5	6	7
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
71								
72								
73								
74		DCN						
75								
76								
77								
78		Reserved						
79								
7A								
7B								
7C								
7D								
7E								
7F								

Byte27 = 8E & Byte34 : bit4-7 = 3 (wait SENSE Timeout) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	Current LPN							
29	LDEV number							
2A	24-byte format	Basic SSB			32-byte format	Basic SSB		
2B								
2C						Exception code		
2D		F/M						
2E		System error code				System error code		
2F								
30	Reset internal SSB number							
31								
32	Detail log number for RESET							
33								
34	Processor number				Message code (x'3')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=3 (Wait SENSE Timeout) (2/2)

	0	1	2	3	4	5	6	7
40								
41		Not used						
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55		LPN						
56		Not used						
5F								
60								
61		Timeout SSB						
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Byte27 = 8E & Byte34 : bit4-7 = 5 (CHK1B Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	Processor number				Message code (x'3')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=5 (CHK1B Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x' 00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (form LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved							
6F								
70	DCN							
71								
72								
73								
74	DCN							
75								
76								
77								
78								
	Reserved							
7F								

Byte27 = 8E & Byte34 : bit4-7 = 6 (DKC Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	Not used							
29								
2A								
2B								
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	Processor number				Message code (x'6')			
35	SSID (Low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=6 (DKC Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x' 00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (form LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved							
6F								
70	DCN							
71								
72								
73								
74	DCN							
75								
76								
77								
78								
	Reserved							
7F								

Byte27 = 8E & Byte34 : bit4-7 = 7 (LCP Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x'8')				Message (x'E')			
28	LPN							
29	Not used							
2A	Internal Sel ective Reset cause							
2B								
2C	For Hotline	Old PSW			For INT SEL RST	LCP error code		
2D								
2E						x'00'		
2F						x'00'		
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	Processor number				Message code (x'7')			
35	SSID (Low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=7 (LCP Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x' 00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (form LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved							
6F								
70	DCN							
71								
72								
73								
74	DCN							
75								
76								
77								
78								
⋮	Reserved							
7F								

Byte27 = 8E & Byte34 : bit4-7 = 8 (Force Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'8')				Message (x'E')			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Reset detail log number							
33								
34	Processor number				Message code (x'8')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=8 (Foece Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Reset type code for making SSB						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55		Current LPN (x' 00' for DKA)						
56		LCP error code						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		wchklmpbitmap						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		sys status						
61		Reserved						
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
71								
72								
73								
74		DCN						
75								
76								
77								
78								
		Reserved						
7F								

Byte27 = 8E & Byte34 : bit4-7 = 9 (Logical Inconsistency Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
1								
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'8')				Message (x'E')			
28	Not used							
29								
2A								
2B								
2C								
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	Processor number				Message code (x'9')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=9 (Logical Inconsistency Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x' 00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (form LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved							
6F								
70	DCN							
71								
72								
73								
74	DCN							
75								
76								
77								
78								
⊢	Reserved							
⊢								
7F								

Byte27 = 8E & Byte34 : bit4-7 = A (Power Failure Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
1								
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'8')				Message (x'E')			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	Processor number				Message code (x'A')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34 : bit4-7=A (Power Failure Reset) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Reset type code for making SSB							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted opration code							
51								
52								
53								
54	Current LDEV number							
55	Current LPN (x' 00' for DKA)							
56	LCP error code							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	wchklmpbitmap							
5D	REQ ID (from LCT)							
5E	JCB ID (form LCT)							
5F								
60	sys status							
61	Reserved							
62								
63								
64	jcb id							
65								
66	req id							
67	Job type code							
68	job status							
69	Executing processor number							
6A	Initiation cause code							
6B	Initiation detail code							
6C	Command code							
6D	Channel sequence							
6E	Reserved							
6F								
70	DCN							
71								
72								
73								
74	DCN							
75								
76								
77								
78								
⊢	Reserved							
⊢								
7F								

Byte27 = 8F (Logical Inconsistency) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'8')				Message (x'F')			
28	Module ID							
29	Routine ID							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	Processor number				Not used (x'00')			
35	SSID(low) of self subsystem							
36	Symptom code (x'FF8F' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 F (Logical Inconsistency) (2/2)

	0	1	2	3	4	5	6	7
40	Error information							
41								
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Byte27 = 9F (Trace data/Log data) (1/2)

All of F/M = 9F SSB informations are no problem on DKC performance.

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code (Note 1)							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'9')				Message (x'F')			
28	Module ID							
29	Routine ID							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	Processor number				Not used (x'00')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF9F')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

Byte27=9 F (Trace data/Log data) (2/2)

	0	1	2	3	4	5	6	7
40		Error information						
7F								

Note 1

The pare of system error code x'AE5A' (Drive not Ready) and x'A772' are reported even when one of the following processes has completed successfully. These indicate the PDEV spin down executed correctly and do not mean the error condition. Please ignore them.

- PDEV replace
- DKU Inline execution at Installation or at PDEV expansion.

Note 2

System error code x'AE5B' (Unit Attention) is reported even after one of the following processes has completed successfully. It indicates the PDEV was reset correctly and does not mean the error condition. Please ignore it.

- DKA replace
- DKA expansion
- PDEV expansion
- DKA micro-program exchange
- PDEV micro-program exchange

Byte27=E C (Envirnment Monitor Detected DKC Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x' E')				Message (x' C')			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B	Reserved area							
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	Processor number (don't care)				Message code (don't care)			
35	SSID(low) of self subsystem (don't care)							
36	Symptom code (x' FFEC')							
37								
38	Log and message control (x' 00')							
39	Program action code (x' 00')							
3A	Configuration information							
3B								
3C	Not usde							
3D	Cylinder address							
3E								
3F	Head address							

Byte27 = EC (Environment Monitor Detected DKC Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error detection code (Note 1)							
41	Error detection code (Note 2)							
42	Error detection code (Note 3)							
43	Not used							
7F								

(Note 1) Error detection code

Code	Detection
10	PWRCTL-1 PCB
20	PWRCTL-2 PCB
11	DKUMN-R1F
21	DKUMN-R1R
12	DKUMN-L1F
22	DKUMN-L1R
13	DKUMN-R2F
23	DKUMN-R2R
14	DKUMN-L2F
24	DKUMN-L2R
30	SSVP

(Note 2) Error component code

Code	Component	Code	Component	Code	Component	Code	Component
10	Logic 1	40	HDU-L10	54	HDU-R24	70	DKUMN-R1F
11	Cache 1	41	HDU-L11	55	HDU-R25	71	DKUMN-R1R
20	Logic 2	42	HDU-L12	56	HDU-R26	72	DKUMN-L1F
21	Cache 2	43	HDU-L13	57	HDU-R27	73	DKUMN-L1R
30	HDU-R10	44	HDU-L14	60	HDU-L20	74	DKUMN-R2F
31	HDU-R11	45	HDU-L15	61	HDU-L21	75	DKUMN-R2R
32	HDU-R12	46	HDU-L16	62	HDU-L22	76	DKUMN-L2F
33	HDU-R13	47	HDU-L17	63	HDU-L23	77	DKUMN-L2R
34	HDU-R14	50	HDU-R20	64	HDU-L24	80	PWRCTL-1
35	HDU-R15	51	HDU-R21	65	HDU-L25	81	PWRCTL-2
36	HDU-R16	52	HDU-R22	66	HDU-L26	90	AC BOX-R10
37	HDU-R17	53	HDU-R23	67	HDU-L27	91	AC BOX-R11

(Note 3) Error reason code

Code	Reason
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow 80%.
40	5V PS 0 box abnormality has been detected.
41	5V PS 1 box abnormality has been detected.
42	5V PS 2 box abnormality has been detected.
43	3.3V PS 0 box abnormality has been detected.
44	3.3V PS 1 box abnormality has been detected.
45	Multi PS 0 box abnormality has been detected.
46	Multi PS 1 box abnormality has been detected.
47	HDD P/L Multi PS 1 box abnormality has been detected.
48	HDD P/L Multi PS 0 box abnormality has been detected.
50	Battery power for shared memory has dropped below 3.8V.
51	Battery power for cache memory has dropped below 3.8V.
52	Battery 0 power for cache memory has dropped below 3.8V.
53	Battery 1 power for cache memory has dropped below 3.8V.
54	Battery 2 power for cache memory has dropped below 3.8V.
60	AC power off/interruption of the breaker box occurred.
70	Low rotation speed of the fan 0 has been detected.
71	Low rotation speed of the fan 1 has been detected.
72	Low rotation speed of the fan 2 has been detected.
73	Low rotation speed of the fan 3 has been detected.
74	Low rotation speed of the fan 4 has been detected.
75	Low rotation speed of the fan 5 has been detected.
76	Low rotation speed of the PS fan 0 has been detected.
77	Low rotation speed of the PS fan 1 has been detected.
78	Low rotation speed of the PS fan 2 has been detected.
79	Low rotation speed of the PS fan 3 has been detected.
80	JP for voltage control remains.
81	JP for LOGIC 1 remains.
82	JP for LOGIC 2 remains.
83	JP for CACHE 1 remains.
84	JP for CACHE 2 remains.
85	JP for HDU-XX0 ~ HDU-XX3 remains.
86	JP for HDU-XX4 ~ HDU-XX7 remains.
90	Environment monitor register access error
91	Basic clock error of the environment monitor PCB occured.
92	Parity error of the environment monitor occured.
A0	An environment monitor disagreement error occured.
A1	An environment monitor disagreement error of power occurred.

Byte27 = EE (Envirnment Monitor Detected DKU Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'E')				Message (x'E')			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	Processor number (don't care)				Message code (don't care)			
35	SSID (low) of self subsystem (don't care)							
36	Symptom code (x'FFEE')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde							
3D	Cylinder address							
3E								
3F	Head address							

Byte27 = EE (Environment Monitor Detected DKU Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error detection code (Note 1)							
41	Error detection code (Note 2)							
42	Error detection code (Note 3)							
43	Not used							
7F								

(Note 1) Error detection code

Code	Detection
10	PWRCTL-1 PCB
20	PWRCTL-2 PCB
11	DKUMN-R1F
21	DKUMN-R1R
12	DKUMN-L1F
22	DKUMN-L1R
13	DKUMN-R2F
23	DKUMN-R2R
14	DKUMN-L2F
24	DKUMN-L2R
30	SSVP

(Note 2) Error component code

Code	Component	Code	Component	Code	Component	Code	Component
10	Logic 1	40	HDU-L10	54	HDU-R24	70	DKUMN-R1F
11	Cache 1	41	HDU-L11	55	HDU-R25	71	DKUMN-R1R
20	Logic 2	42	HDU-L12	56	HDU-R26	72	DKUMN-L1F
21	Cache 2	43	HDU-L13	57	HDU-R27	73	DKUMN-L1R
30	HDU-R10	44	HDU-L14	60	HDU-L20	74	DKUMN-R2F
31	HDU-R11	45	HDU-L15	61	HDU-L21	75	DKUMN-R2R
32	HDU-R12	46	HDU-L16	62	HDU-L22	76	DKUMN-L2F
33	HDU-R13	47	HDU-L17	63	HDU-L23	77	DKUMN-L2R
34	HDU-R14	50	HDU-R20	64	HDU-L24	80	PWRCTL-1
35	HDU-R15	51	HDU-R21	65	HDU-L25	81	PWRCTL-2
36	HDU-R16	52	HDU-R22	66	HDU-L26	90	AC BOX-R10
37	HDU-R17	53	HDU-R23	67	HDU-L27	91	AC BOX-R11

(Note 3) Error reason code

Code	Reason
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow 80%.
40	5V PS 0 box abnormality has been detected.
41	5V PS 1 box abnormality has been detected.
42	5V PS 2 box abnormality has been detected.
43	3.3V PS 0 box abnormality has been detected.
44	3.3V PS 1 box abnormality has been detected.
45	Multi PS 0 box abnormality has been detected.
46	Multi PS 1 box abnormality has been detected.
47	HDD P/L Multi PS 1 box abnormality has been detected.
48	HDD P/L Multi PS 0 box abnormality has been detected.
50	Battery power for shared memory has dropped below 3.8V.
51	Battery power for cache memory has dropped below 3.8V.
52	Battery 0 power for cache memory has dropped below 3.8V.
53	Battery 1 power for cache memory has dropped below 3.8V.
54	Battery 2 power for cache memory has dropped below 3.8V.
60	AC power off/interruption of the breaker box occurred.
70	Low rotation speed of the fan 0 has been detected.
71	Low rotation speed of the fan 1 has been detected.
72	Low rotation speed of the fan 2 has been detected.
73	Low rotation speed of the fan 3 has been detected.
74	Low rotation speed of the fan 4 has been detected.
75	Low rotation speed of the fan 5 has been detected.
76	Low rotation speed of the PS fan 0 has been detected.
77	Low rotation speed of the PS fan 1 has been detected.
78	Low rotation speed of the PS fan 2 has been detected.
79	Low rotation speed of the PS fan 3 has been detected.
80	JP for voltage control remains.
81	JP for LOGIC 1 remains.
82	JP for LOGIC 2 remains.
83	JP for CACHE 1 remains.
84	JP for CACHE 2 remains.
85	JP for HDU-XX0 ~ HDU-XX3 remains.
86	JP for HDU-XX4 ~ HDU-XX7 remains.
90	Environment monitor register access error
91	Basic clock error of the environment monitor PCB occured.
92	Parity error of the environment monitor occured.
A0	An environment monitor disagreement error occured.
A1	An environment monitor disagreement error of power occurred

Byte27 = F0 (Operation Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'F')				Message (x'E')			
28	Not used (x'00')							
29	Not used (x'00')							
2A	Not used (x'00')							
2B	Hardware level (Note 1)							
2C								
2D	SSID of mate subsystem (x'0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x'00')							
30	Not used (x'00')							
31	Module ID							
32	Routine ID							
33	Processor number				Message code (x'0')			
34	SSID of self subsystem							
35								
36	Symptom code (x'FFF0')							
37								
38	Log and message control (x'00')							
39	Program action code (x'1D')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

Byte27=F 0 (Openation Terminated) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
7F								

(Note 1) Hardware level

Bit0 : Hardware level flag

For bit0=0

Bit 1	: Not used
Bit 2 ~ 3	: SP number
Bit 4 ~ 5	: CHLs per Cluster
	00 : 4
	01 : 8
	10 : Not used
	11 : Not used
Bit 6	: NVS
	0 : Without NVS
	1 : With NVS
Bit 7	: Not used
Bit 8 ~ 10	: Cache size
	000 : Non cache
	001 : 256MB
	010 : 512MB
	011 : 768MB
	100 : 1024MP
	101 : 1280MP
	110 : 1536MP
	111 : Over 1536MB
Bit11 ~ 13	: Cluster hardware level
Bit14 ~ 15	: Cache/NVS hardware level

For bit0=1

Bit 1	: Not used
Bit 2 ~ 3	: SP number
Bit 4 ~ 5	: CHLs per Cluster
	0000 : Parallel=4, Serial=0
	0001 : Parallel=8, Serial=0
	0010 : Parallel=4, Serial=2
	0100 : Parallel=4, Serial=4
	0110 : Parallel=0, Serial=2
	1000 : Parallel=0, Serial=4
	1010 : Parallel=0, Serial=8
	1100 : Parallel=0, Serial=8
Bit 8	: DUAL FRAME
	0 : DUAL FRAME
	1 : MODULAR POWER
Bit 9 ~ 11	: Cache size
	000 : Non cache
	001 : 256MB
	010 : 512MB
	011 : 768MB
	100 : 1024MB
	101 : 1280MB
	110 : 1536MB
	111 : Over 1536MB
Bit12 ~ 13	: Cluster hardware level
Bit14 ~ 15	: Cache/NVS hardware level

Byte27 = F1 (Micro-program Detected Cache Failure) (1/2)

	0	1	2	3	4	5	6	7	
00	Time stamp								
05									
06	Log type								
07									
08	Failure classification								
09									
0A	System error code								
0B									
0C	JCB ID								
0D									
0E	REQ ID								
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID				
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log	
11	VDEV number								
12									
13	CDEV number				RDEV number				
14	LDEV type								
15	PDEV type								
16	SSB log number								
17									
18	Related failure log number								
19									
1A	Related SIM log number								
1B									
1C	Related SSB log number								
1D									
1E	(Reserved)								
1F	SCB								
20	Basic SSB								
21									
22									
23	Count								
24	Device address								
25	Cylinder addres (low)								
26	Cylinder address (high)				Head address				
27	Format (x'F')				Message (x'1')				
28	Queue transition in progress (Side A)	Queue transition in progress (Side B)	Free SGCB queue operation in progress	Free SLCB queue operation in progress	Free GRPT queue operation in progress	Not used			
29	Not used								*
	VDEV number								*
2A	Queue type								*
	VDEV number		Slot number						*
2B	Queue number								*
	Slot number								*
2C	Queue number								*
	Slot number								*
2D	SSID of mate subsystem (x'0000' for EDCC)								
2E									
2F	Maker code & Manufacture code (x'00')								
30	Not used (x'00')								

* : When byte 28, bit2-4 = 000, upper value is valid.
: When byte 28, bit2-4 ≠ 000, lower value is valid.

Byte27 = F1 (Micro-program Detected Cache Failure) (2/2)

	0	1	2	3	4	5	6	7
31	Module ID							
32	Routine ID							
33	Processor number				Message code (x'0')			
34	SSID of self subsystem							
35								
36	Symptom code (x'FFF1')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	Error information							
⋮								
7F								

Byte27 = F2 (Cache Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low)							
26	Cylinder address (high)				Head address			
27	Format (x'F')				Message (x'2')			
28	Subcode (See following pages)							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D	SSID of mate subsystem (x'0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x'00')							
30	Hardware information (See following pages)							
31	Module ID							
32	Routine ID							
33	Processor number				Not used (x'0)			
34	SSID of self subsystem							
35								
36	Symptom code (x'FFF2')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not usde (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

Byte27=F 2 (Cache Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Hardware information (See following pages) (Note 1)							
7F								

(Note 1)

(1) When Module ID (byte31) is x' 58' or x' 59'
see the type specified by subcode.
(2) When Module ID (byte31) is not x' 58' / x' 59' and Processor ID (byte 33, bit0-3) is x' 8' -x' F' , see the type spcified by subcode.
(3) When Module ID (byte31) is not x' 58' / x' 59' and Processor ID (byte 33, bit0-3) is x' 0' -x' 7' , see the type 9 information.

Byte27 = F2 (Cache Faiure) Hardware information

(1) Byte28 = 01/81 : Error in cache board

	0	1	2	3	4	5	6	7
28	Subcode : x'01' : Error in cache board (Not ECCUNCORR, PLRCERR), without undefine register x'81' : Error in cache board (Not ECCUNCORR, PLRCERR), with undefine register							
29		BOARD ERR						
	WRENABLE signal abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	ADR0 signal parity error	ADR1 signal parity errorl	SYND signal parity errorl
2A		BOARD ERR						
	ECC compare error	Uncorrec-table memory error at read	ECC error at writing	Not used	LRC0 error at writing	LRC1 error at writing	LRC2 error at writing	LRC3 error at writing
2B		CR ERR						
	Clock abnormal	ADRCTC detected abnormal clock	ECCCTL1 detected abnormal clock	ECCCTL2 detected abnormal clock	Not used	Address counter abnormal	Data transfer counter abnormal	Refresh counter abnormal
2C		CR ERR						
	Refresh operation abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	Not used	Not used	Not used

30	Cache slot number with an inboard error (Slot number : See SSBLOG05-4620)

40 ‖ 7F	Hardware common information (See "type 1") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x, see type 1.
(2) When Module ID (byte31) is not x'58'/x'59' and Preocessor ID (btye33,bit0-3) is x'8'-x'F', see type 1.
(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

Byte27 = F2 (Cache Failure) Hardware information

(2) Byte28 = 02/82 : Error in cache board

	0	1	2	3	4	5	6	7
28	Subcode : x'02' : Error in cache board (ECCUNCORR), without undefined register x'82' : Error in cache board (ECCUNCORR), with undefined register							
29	Accessed module group number							
2A	BOARD ERR							
	ECC compare error	Uncorre-ctable memory error at read	ECC error at writing	Not used	LRC0 error at writing	LRC1 error at writing	LRC2 error at writin	LRC3 error at writin
2B	MEM ERROR							
	Module group number			Module side number	bits0 to 11 valid	Byte number with a memory erro		
2C	MEM ERROR							
	Byte number with a memory error			Bits 12 to 17 valid	Byte number with a memory error (Second byte)			

30	Cache slot number with an inboard error (Slot number : See SSBLOG05-4620)

40 7F	Hardware common information (See "type 1") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 1.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 1.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

Byte27 = F2 (Cache Failure) Hardware information

(3) Byte28 = 03/83 : Error in cache board

	0	1	2	3	4	5	6	7
28	Subcode : x'03' : Error in cache board (PLRCERR)' without undefined register x'83' : Error in cache board (PLRCERR)' without undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	CACHE slave 1 BODERR							
	ECC compare error	Uncorrec-table memory error at read	ECC error at writing	Not used	LRC0 error at writing	LRC1 error at writing	LRC2 error at writing	LRC3 error at writing
2C	CACHE slaeve 2 BODERR (x' 00' for 1 slave mode)							
	ECC compare error	Uncorrec-table memory error at read	ECC error at writing	Not used	LRC0 error at writing	LRC1 error at writing	LRC2 error at writing	LRC3 error at writing

30	Cache slot number with an inboard error (Slog number : See SSBLOG05-4620)

40 ‖ 7F	Hardware common information (See "type 1") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 1.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 1.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

Byte27 = F 2 (Cache Faiure) Hardware information

(4) Byte28 = 04/84 : Error in CPC board

	0	1	2	3	4	5	6	7
28	Subcode : x'04' : Error in CPC board without undefined register x'84' : Error in CPC board with undefined register							
29	LBUS ERR							
	Address parity error	Transfer count ≥4	(RSV)	(RSV)	Data parity error	(RSV)	(RSV)	(RSV)
2A	CPCLS1 ERR							
	RW1 sequencer counter parity error	RW2 sequencer counter parity error	OUT sequencer counter parity error	LOCAL sequencer counter parity error	Transfer counter parity error	DTSYNC counter parity error	Local bus DTSYNC counter parity error	(RSV)
2B	CPCLS1 ERR							
	RW1 sequencer sequencer parity error	RW2 sequencer sequencer parity error	RW1 sequencer abnormal flag	LOCAL sequencer sequencer parity error	OUT sequencer sequencer parity error	(RSV)	(RSV)	(RSV)
2C	CPCLS ERR							
	OBF data data parity error	OUT data data parity error	Cache port data buffer empty	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

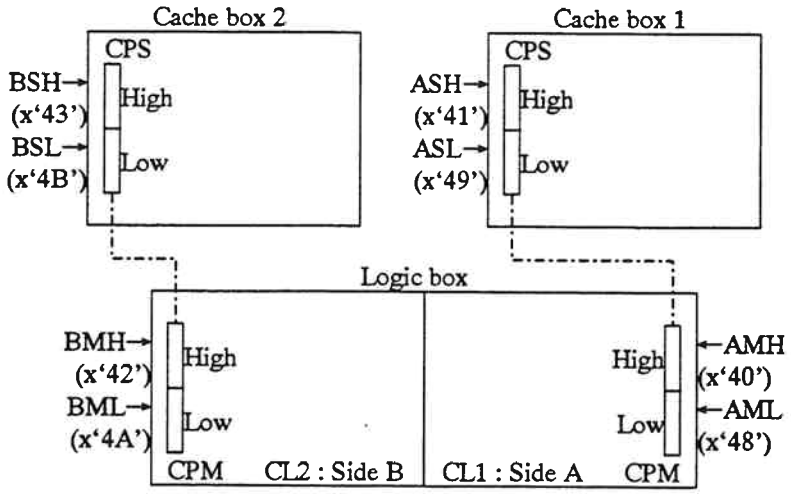
30	CPC slot number with an inboard error (Note 2)

40 ‖ 7F	Hardware common information (See "type 2") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x, see type 2.
(2) When Module ID (byte31) is not x'58'/x'59' and Preocessor ID (byte33,bit0-3) is x'8'-x'F', see type 2.
(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) CPC slot number



Byte27 = F2 (Cache Failure) Hardware information

(5) Byte28 = 08/88 : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'08' : Bus error (2 bus, 2 slaves, CPC used), without undefined register x'88' : Bus error (2 bus, 2 slaves, CPC used), with undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Cache (slave 1) address error	Cache (slave 1) protocol/ nonprotocol error		Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))				
2C	Cache (slave 1) address error	Cache (slave 1) protocol/ nonprotocol error		Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')				

30	CPC(AMH) detected bus error	CPC(AML) detected bus error	CPC(ASH) detected bus error	CPC(ASL) detected bus error	CPC(BMH) detected bus error	CPC(BML) detected bus error	CPC(BSH) detected bus error	CPC(BSL) detected bus error

40 | | 7F	Hardware common information (See "type 3") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59' ,see type 3.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 3.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(6) Byte28 = 09/89 : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'09' : Bus error (2 bus, 2 slaves, CPC unused), without undefined register x'89' : Bus error (2 bus, 2 slaves, CPC unused), without undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization :x'00')							

30	Cache (Slave 1) bus H address error	Cache (Slave 1) bus H protocol/ nonprotocol error	Cache (Slave 1) bus L address error	Cache (Slave 1) bus L protocol/ nonprotocol error	Cache (Slave 2) bus H address error	Cache (Slave 2) bus H protocol/ nonprotocol error	Cache (Slave 2) bus L address error	Cache (Slave 2) bus L protocol/ nonprotocol error

40 ‖ 7F	Hardware common information (See "type 4") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 4.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 4.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

Byte27 = F2 (Cache Failure) Hardware information

(7) Byte28 = 0A/8A : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'0A' : Bus error (2 bus, 1 slave, CPU used)' without undefined register x'8A' : Bus error (2 bus, 1 slave, CPC used)' with undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Cache bus H address error 1	Cache bus H addres error 2	Cache bus H protocol/ nonprotocol error	Cache bus L address error 1	Cache bus L addres error 2	Cache bus L protocol/ nonprotocol error	Cache inboard error 1	Cache inboard error 2
30	CPC(AMH/ BMH) detected address error	CPC(AMH/ BMH) detected protocol/ nonprotocol error	CPC(AML/ BML) detected address error	CPC(AML/ BML) detected protocol/ nonprotocol error	CPC(ASH/ BSH) detected address error	CPC(ASH/ BSH) detected protocol/ nonprotocol error	CPC(ASL/ BSL) detected address error	CPC(ASL/ BSL) detected protocol/ nonprotocol error
40 ‖ 7F	Hardware common information (See "type 5") (Note 1)							

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 5.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 5.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(8) Byte28 = 0B/8B : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'0B' : Bus error (2 bus, 1 slave, CPU unused)' without undefined register x'8B' : Bus error (2 bus, 1 slave, CPC unused)' with undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2))							
2C	Cache bus H address error 1 (A/CSYNC error)	Cache bus H address error 1 (Parity error)	Cache bus H address error 1 (Program error)	Cache bus H address error 1 (Compare error)	Cache bus L address error 2	Cache bus L protocol error (Not ESSEQERR)	Cache bus L protocol error (ESSEQ-ERR)	Cache bus L nonprotocol error
30	Cache bus H address error 1 (A/CSYNC error)	Cache bus H address error 1 (Parity error)	Cache bus H address error 1 (Program error)	Cache bus H address error 1 (Compare error)	Cache bus L address error 2	Cache bus L protocol error (Not ESSEQERR)	Cache bus L protocol error (ESSEQ-ERR)	Cache bus L nonprotocol error
40 ‖ 7F	Hardware common information (See "type 5") (Note 1)							

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 5.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 5.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

Byte27 = F2 (Cache Failure) Hardware information

(9) Byte28=0C/8C : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'0C' : Bus error (Bus H/L, 2 slaves, CPC used), without undefined register x'8C' : Bus error (Bus H/L, 2 slaves, CPC used), with undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Cache (slave 1) address error	Cache (slave 1) protocol/ nonprotocol error	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))					
2C	Cache (slave 1) address error	Cache (slave 1) protocol/ nonprotocol error	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')					

30	CPC(AMH/ BMH) detected address error	CPC(AMH/ BMH) detected protocol/ nonprotocol error	CPC(AML/ BML) detected address error	CPC(AML/ BML) detected protocol/ nonprotocol error	CPC(ASH/ BSH) detected address error	CPC(ASH/ BSH) detected protocol/ nonprotocol error	CPC(ASL/ BSL) detected address error	CPC(ASL/ BSL) detected protocol/ nonprotocol error

40 ‖ 7F	Hardware common information (See "type 6") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 6.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 6.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(10) Byte28 = 0D/8D : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'0D' : Bus error (Bus H/L, 2 slave, CPC unused), without undefined register x'8D' : Bus error (Bus H/L, 2 slave, CPC unused), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00')							

30	Cache (Slave 1) bus H/L address error	Cache (Slave 1) bus H/L protocol/ nonprotocol error	Cache (S1) Bus H/L protocol/ nonprotocol error	Cache (Slave 1) inboard error	Cache (Slave 2) Bus H/L address error 1	Cache (Slave 2) Bus H/L address error 2	Cache (S2) Bus H/L protocol/ nonprotocol error	Cache (Slave 2) inboard error

40 ‖ 7F	Hardware common information (See "type 6") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 6.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 6.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

Byte27 = F2 (Cache Failure) Hardware information

(11) Byte28 = 0E/8E : Bus error (Cache access)

	0	1	2	3	4	5	6	7
28	Subcode : x'0E' : Bus error (Bus H/L, 1 slave, CPC Used), without undefined register x'8E' : Bus error (Bus H/L, 1 slave, CPC Used), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2))							
2C	Cache Bus H/L addres error 1 (A/CSYNC error)	Cache Bus H/L address error 1 (Parity error)	Cache Bus H/L address error 1 (Program error)	Cache Bus H/L address error 1 (Compare error)	Cache Bus H/L address error 2	Cache Bus H/L protocol/ error (Not ESSEQERR)	Cache Bus H/L protocol/ error (ESSEQ-ERR)	Cache Bus H/L nonprotocol error
30	CPC (AMH/L, BMH/L detected address error 1	CPC (AMH/L, BMH/L detected address error 2	CPC (AMH/L, BMH/L detected FBUSERR	CPC (AMH/L, BMH/L detected JBUSERR	CPC (AMH/L, BMH/L detected address error 1	CPC (AMH/L, BMH/L detected address error 2	CPC (AMH/L, BMH/L detected FBUSERR	CPC (AMH/L, BMH/L detected JBUSERR
40 ‖ 7F	Hardware common information (See "type 1") (Note 1)							

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 1.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 1.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

Byte27 = F2 (Cache Failure) Hardware information

(12) Byte28 = 0E/8E : Bus error (CPC access)

	0	1	2	3	4	5	6	7
28	Subcode : x'0E' :Bus error (Bus H/L, 1 slave, CPC Used), without undefined register x'8E' :Bus error (Bus H/L, 1 slave, CPC Used), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Accessed CPC slot number (See SSBLOG05-3440)							
2C	LBUS ERR							
	Address parity error	Transfer count ≥4	(RSV)	(RSV)	Data parity error	(RSV)	(RSV)	(RSV)

30	CPC (AMH/L, BMH/L detected address error 1	CPC (AMH/L, BMH/L detected address error 2	CPC (AMH/L, BMH/L detected FBUSERR	CPC (AMH/L, BMH/L detected JBUSERR	CPC (AMH/L, BMH/L detected address error 1	CPC (AMH/L, BMH/L detected address error 2	CPC (AMH/L, BMH/L detected FBUSERR	CPC (AMH/L, BMH/L detected JBUSERR

40 | | 7F	Hardware common information (See "type 6") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 6.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 6.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

Byte27 = F 2 (Cache Failure) Hardware information

(13) Byte28 = 0F/8F : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'0F' :Bus error (Bus H/L, 1 slave, CPC unused), without undefined register x'8F' :Bus error (Bus H/L, 1 slave, CPC unused), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2))							
2C	Cache Bus H/L AC SEQ ERR	Cache Bus H/L AC TIM OUT	Cache Bus H/L address error 1 (Program error)	Cache Bus H/L address error 1 (Compare error)	Cache Bus H/L address error 1 (LRC unmatch)	Cache Bus H/L address error 1 (Compare error)	Cache Bus H/L address compare error	Cache Bus H/L command compare error

30	DTSEQERR (REG:20C/ 21C:b00) detected	DTSTOP (REG:20C/ 21C:b01) detected	ACACT (REG:20C/ 21C:b02) detected	CNTUN-MATCH (REG:20C/ 21C:b03) detected	ENOFF (REG:20C/ 21C:b04) detected	ESSEQERR (REG:20C/ 21C:b05) detected	DATAPE (REG:20C/ 21C:b08) detected	OVERRUN (REG:20C/ 21C:b09) detected

40 ‖ 7F	Hardware common information (See "type 6") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 6.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 6.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

Byte27 = F2 (Cache Failure) Hardware information

(14) Byte28 = 10/90 : Time-out

	0	1	2	3	4	5	6	7
28	Subcode : x'10' : Timeout (no error cause, 2 bus), without undefined register x'90' : Timeout (no error cause, 2 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(15) Byte28 = 11/91 : CHKERR report

	0	1	2	3	4	5	6	7
28	Subcode : x'11' : CHKERR report (no error cause, 2 bus), without undefined register x'91' : CHKERR report (no error cause, 2 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(16) Byte28 = 12/92 : BSA detected error

	0	1	2	3	4	5	6	7
28	Subcode : x'12' : BSA detected error (no error cause, 2 bus), without undefined register x'92' : BSA detected error (no error cause, 2 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 1 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00'							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40	Hardware common information (See "type 7") (Note 1)
7F	

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(17) Byte28 = 13/93 :Error status report

	0	1	2	3	4	5	6	7
28	Subcode : x'13' : Error status report (no error cause, 2 bus), without undefined register x'93' : Error status report (no error cause, 2 bus), with undefined register							
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST2 ~ 5							
	Tow-bus access error in one-bus mode	Blocked MG/ Cache access	Inboard error or clock/ refresh abnormal	Register/ Memory access before INIT	Cache memory access in self refresh	Vaiolate setting access mode	Vaiolate DIAG/SP mode	Master send data parity error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(18) Byte28 = 14/94 : Bus error

	0	1	2	3	4	5	6	7
28	Subcode : x'14' : Timeout (no error cause, 1 bus), without undefined register x'94' : Timeout (no error cause, 1 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 3) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(19) Byte28 = 15/95 : CHKERR report

	0	1	2	3	4	5	6	7
28	Subcode : x'15' : CHKERR report (no error cause, 1 bus), without undefined register x'95' : CHKERR report (no error cause, 1 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(20) Byte28 = 16/96 : BSA detected error

	0	1	2	3	4	5	6	7
28	Subcode : x'16' : BSA detected error (no error cause, 1 bus), without undefined register x'96' : BSA detected error (no error cause, 1 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST1							
	EXERR1 HI data parity error	EXERR1 LO data parity error	EXERR2 HI data parity error	EXERR2 LO data parity error	Mate BSA error	Slave ID error	LRC check field parity error	LRC check field LRC error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : SSBLOG05-3440.

Byte27 = F2 (Cache Failure) Hardware information

(21) Byte28 = 17/97 : Error status report

	0	1	2	3	4	5	6	7
28	Subcode : x'17' : Error status report (no error cause, 1 bus), without undefined register x'97' : Error status report (no error cause, 1 bus), with undefined register						—	
29	Operation mode							
	Bus ues mode 0 : Sequential 1 : Transaction 2 : Transaction to Sequential 3 : Sequential to Transaction		Access 0 : Memory/ Initialize 1 : Cache/ CPC register	Bus mode 0 : Two - bus mode 1 : Not used 2 : Bus-L mode 3 : Bus - H mode (0 for Initialization)		Transfer mode 0 : Normal write 1 : Normal read 3: Cache to cache 4 : Dual write 7 : Initialize 2,5,6 : Not used		
2A	Response staus							
	F bus H response timeout	CACHE/CP C bus error (F bus H)	H-side BSA bus error	CACHE/CP C abnormal (F bus H)	F bus L response timeout	CACHE/CP C bus error (F bus L)	L-side BSA bus error	CACHE/CP C bus error (F bus L)
2B	Slave 1 number (Cache access : Slot number of Cache (Slave 1) (Note 2) Cache initialization : Slot number of Cache (Note 2) CPC access : Slot number of CPC (Note 3))							
2C	Slave 2 number (Cache access : Slot number of Cache (Slave 2) (Note 2) Cache initialization : x'00' CPC access : x'00')							

30	BSA0/1::CK2AST2 ~ 5							
	Tow-bus access error in one-bus mode	Blocked MG/ Cache accesss	Inboard error or clock/ refresh abnormal	Register/ memory access before initialization	Cache memory access in self refresh	Vaiolate access mode	Vaiolate DIAG/SP mode	Master recieved data parity error

40 ‖ 7F	Hardware common information (See "type 7") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x'59', see type 7.

(2) When Module ID (byte31) is not x'58' and Processor ID (byte33,bit0-3) is x'8'-x'F', see type 7.

(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

(Note 2) Cache slot number : See SSBLOG05-4620.

(Note 3) CPC slot number : See SSBLOG05-3440.

Byte27 = F2 (Cache Faiure) Hardware information

(22) Byte28 = 70/F0 : Inboard error at initialization

	0	1	2	3	4	5	6	7
28	Subcode : x'70' : Inboard error at initialization, without undefine register x'F0' : Inboard error at initialization, with undefine register						—	
29	BOARD ERR							
	WRENABLE signal abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	ADR0 signal parity error	ADR1 signal parity errorl	signal parity errorl
2A	BOARD ERR							
	ECC compare error	Uncorrectabl ememory error at read	ECC error at writing	Not used	LRCO error at writing	LRC1 error at writing	LRC2 error at writing	LRC3 error at writing
2B	CR ERR							
	Clock abnormal	ADRCTC detected abnormal clock	ECCCTL1 detected abnormal clock	ECCCTL2 detected abnormal clock	Not used	Address counter abnormal	Data transfer counter abnormal	Refresh counter abnormal
2C	CR ERR							
	Refresh operation abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	Not used	Not used	Not used

30	Cache slot number with an inboard error (See SSBLOG05-4620)

40 ‖ 7F	Hardware common information (See "type 8") (Note 1)

(Note 1)

(1) When Module ID (byte31) is x'58' or x, see type 8.
(2) When Module ID (byte31) is not x'58'/x'59' and Preocessor ID (byte33,bit0-3) is x'8'-x'F', see type 8.
(3) When Module ID (byte31) is not x'58'/x'59' and Processor ID (byte33,bit0-3) is x'0'-x'3', see type 9.

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 1 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number						—	
42	slave 1 number							
43	MPID:Error detected MP							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus eror	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Cache undefined registet flag 1 (Slave 1) (b00-03:Bus H, b04-07:Bus L)							
	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X
46	Cache undefined registet flag 1 (Slave 2)							
	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X
47	Cache undefined registet flag 3 (Inboard) (b00-03:Bus H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CACHE ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 Baoard unmatch	Slave 2 register access	Slave 2 Address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
4C	CACHE BUSERRH							
	Data sequence error	Data stop	DT phase FAFYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CACHE ADRERR1L							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 transfer count ER
4F	CACHE ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Access timeout (others)

Byte27=F 2 (Cache Failure)Byte 40-7F Common information : Type 1 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access unmatch	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
51	CACHE ADRERR2L							
	Slave 1 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Not used
52	CACHE BUSERRL							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
53	CACHE BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not usesd	Not used	Not used	Not used	FENT SIG off (others)
54	CACHE BOARDERR							
	Write enable abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	ADR0 signal parity ER	ADR 1 signal parity ER	SYND signal parity ER
55	CACHE BOARDERR							
	ECC compare error	ECC UNCORREC ERR (read)	ECC error (Write)	Not used	LRC0 error (write)	LRC1 error (write)	LRC2 error (write)	LRC error (write)
56	CACHE CRERR							
	Clock abnormal	ADRCTL Clock abnormal	ECCCTL1 Clock abnormal	ECCCTL2 Clock abnormal	Not used	Address counter abnormal	Data XFR counter abnormal	Refresh counter abnormal
57	CACHE CRERR							
	Refresh action abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	Not used	Not used	Not used
58	CACHE MEMERROR0							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
59	CACHE MEMERROR0							
	Byte number 1 with error (low order)		Byte13-17 valid	Byte number 2 with error (high order)				
5A	CACHE MEMERROR1							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (low order)		
5B	CACHE MEMERROR1							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				
5C	CACHE MEMERROR2							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
5D	CACHE MEMERROR2							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				
5E	CACHE MEMERROR3							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
5F	CACHE MEMERROR3							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				

Byte27 = F2 (Cache Failure) Byte 40-7F Common information : Type 1 (3/4)

	0	1	2	3	4	5	6	7
60	Cache access address							
61	Cache access address							
62	Cache access address							
63	Cache access address							
64	Cache access address (for two slave access)							
65	Cache access address (for two slave access)							
66	Cache access address (for two slave access)							
67	Cache access address (for two slave access)							
68	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
69	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HL input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HI input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
6B	BSA H CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
6C	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
6D	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
6E	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
6F	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 1 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
71	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
72	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
73	BSA H CK2AST5							
	Board error (others)	Clock/refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
74	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
75	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
77	BSA H CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
78	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
79	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7A	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7B	BSA H CK2AST3							
	Board error (others)	Clock/refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
7C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
7D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7E	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 2 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected MP							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus eror	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Cache undefined registet flag 1 (Slave 1) (b00-03:Bus H, b04-07:Bus L)							
	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X
46	Cache undefined registet flag 1 (Slave 2)							
	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X	REG 00X	REG 01X	REG 02X	REG 20X, 21X, 22X, 38X
47	Cache undefined registet flag 3 (Inboard) (b00-03:Bus H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CPC AMH/BMH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
49	CPC AMH/BMH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
4A	CPC AMH/BMH LBUSERR							
	Address parity error	Transfer count †4	(RSV)	(RSV)	Received data parity ER	(RSV)	(RSV)	(RSV)
4B	CPC AMH/BMH CPCLSIERR1							
	RW1 SEQ counter parity ER	RW2 SEQ counter parity ER	OUT SEQ counter parity ER	Local SEQ counter parity ER	XFR CNT counter parity ER	F bus DT SYNC CNT parity ER	L bus DT SYNC CNT parity ER	(RSV)
4C	CPC AMH/BMH CPCLSIERR1							
	RW1 SEQ sequencer parity ER	RW2 SEQ sequencer parity ER	RW1 SEQ flag abnormal	Local SEQ sequencer parity ER	OUT SEQ sequencer parity ER	(RSV)	(RSV)	(RSV)
4D	CPC AMH/BMH CPCLSIERR2							
	OBF data data parity ER	OUT data data parity ER	Cache port data overrun	Cache port CLK abnormal	(RSV)	(RSV)	(RSV)	(RSV)
4E	CPC AML/BML FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
4F	CPC AML/BML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 2 (2/4)

	0	1	2	3	4	5	6	7
50	CPC AMH/BMH LBUSERR							
	Address parity error	Transfer count †4	(RSV)	(RSV)	Received data parity ER	(RSV)	(RSV)	(RSV)
51	CPC AMH/BML CPCLSIERR1							
	RW1 SEQ counter parity ER	RW2 SEQ counter parity ER	OUT SEQ counter parity ER	Local SEQ counter parity ER	XFR CNT counter parity ER	F bus DT SYNC CNT parity ER	L bus DT SYNC CNT parity ER	(RSV)
52	CPC AMH/BML CPCLSIERR1							
	RW1 SEQ sequencer parity ER	RW2 SEQ sequencer ER	RW1 SEQ flag abnormal	Local SEQ sequencer parity ER	OUT SEQ sequencer parity ER	(RSV)	(RSV)	(RSV)
53	CPC AMH/BML CPCLSIERR2							
	OBF data data parity ER	OUT data data parity ER	Cache port data overrun	Cache port CLK abnormal	(RSV)	(RSV)	(RSV)	(RSV)
54	CPC ASH/BSH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
55	CPC ASH/BSH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
56	CPC ASH/BSH LBUSERR							
	Address parity error	Transfer count †4	(RSV)	(RSV)	Received data parity ER	(RSV)	(RSV)	(RSV)
57	CPC ASH/BSH CPCLSIERR1							
	RW1 SEQ counter parity ER	RW2 SEQ counter parity ER	OUT SEQ counter parity ER	Local SEQ counter parity ER	XFR CNT counter parity ER	F bus DT SYNC CNT parity ER	L bus DT SYNC CNT parity ER	(RSV)
58	CPC ASH/BSH CPCLSIERR1							
	RW1 SEQ sequencer parity ER	RW2 SEQ sequencer parity ER	RW1 SEQ flag abnormal	Local SEQ sequencer parity ER	OUT SEQ sequencer parity ER	(RSV)	(RSV)	(RSV)
59	CPC ASH/BSH CPCLSIERR2							
	OBF data data parity ER	OUT data data parity ER	Cache port data overrun	Cache port CLK abnormal	(RSV)	(RSV)	(RSV)	(RSV)
5A	CPC ASL/BSL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
5B	CPC ASL/BSL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
5C	CPC ASH/BSL LBUSERR							
	Address parity error	Transfer count †4	(RSV)	(RSV)	Received data parity ER	(RSV)	(RSV)	(RSV)
5D	CPC ASL/BSL CPCLSIERR1							
	RW1 SEQ sequencer parity ER	RW2 SEQ counter parity ER	OUT SEQ counter parity ER	Local SEQ counter parity ER	XFR CNT counter parity ER	F bus DT SYNC CNT parity ER	L bus DT SYNC CNT parity ER	(RSV)
5E	CPC ASL/BSL CPCLSIERR1							
	RW1 SEQ sequencer parity ER	RW2 SEQ sequencer parity ER	RW1 SEQ flag abnormal	Local SEQ sequencer parity ER	OUT SEQ sequencer parity ER	(RSV)	(RSV)	(RSV)
5F	CPC ASL/BSL CPCLSIERR2							
	OBF data data parity ER	OUT data data parity ER	Cache port data overrun	Cache port CLK abnormal	(RSV)	(RSV)	(RSV)	(RSV)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 2 (3/4)

	0	1	2	3	4	5	6	7
60	CPC undefined register flag 1 (AMH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
61	CPC undefined register flag 1 (AML)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
62	CPC undefined register flag 1 (ASH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
63	CPC undefined register flag 1 (ASL)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
64	CPC undefined register flag 1 (BMH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
65	CPC undefined register flag 1 (BML)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
66	CPC undefined register flag 1 (BSH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
67	CPC undefined register flag 1 (BSL)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
68	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
69	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
6A	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
6B	BSA H CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
6C	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
6D	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
6E	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
6F	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 2 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 1 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
71	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
72	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
73	BSA H CK2AST5							
	Board error (others)	Clock/refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
74	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
75	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
77	BSA H CK2AST1							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
78	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
79	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7A	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7B	BSA H CK2AST3							
	Board error (others)	Clock/refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
7C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
7D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7E	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 3 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected MP							
44	CPC undefined register flag 2 (A side) (b00-03:bus H, b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 23X, 24X	REG 20X	REG 21X	REG 22X	REG 23X, 24X
45	CPC undefined register flag 2 (B side) (b00-03:bus H, b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 23X, 24X	REG 20X	REG 21X	REG 22X	REG 23X, 24X
46	Cache undefined registet flag 3 (Slave 1) (b00-03:bus H, b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined registet flag 3 (Slave 2) (b00-03:Bus H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CACHE ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 Board # match	Slave 2 register access	Slave 2 Address COMP. ERR	Slave 2 command COMP ERR	Not used	Not used	Slave 2 timeout (others)
4C	CACHE S1 BUSERRH							
	Data sequence error	Data stop	DT phase FAFYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE S1 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CACHE S1 ADRERR1L							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode erroe	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 transfer count ER
4F	CACHE S1 ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Access timeout (others)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 3 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE S1 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
51	CACHE S1 ADRERR2L							
	Slave 1 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
52	CACHE S1 BUSERRL							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
53	CACHE S1 BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not usesd	Not used	Not used	Not used	FENT SIG off (others)
54	CACHE S2 ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
55	CACHE S2 ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
56	CACHE S2 ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 count errot
57	CACHE S2 ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
58	CACHE S2 BUSERRH							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
59	CACHE S2 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
5A	CACHE S2 ADRERR1L							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 commnad parity ER	Slave 1 bus mode error	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 transfer count ERR
5B	CACHE S2 ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Not used
5C	CACHE S2 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 commnad parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
5D	CACHE S2 ADRERR2L							
	Slave 1 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Not used
5E	CACHE S2 BUSERRL							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Trasnfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
5F	CACHE S2 BUSERRL (REG 21C:B10-17)							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)

Byte27=F 2 (Cache Faiure) Byte 40-7F Common information : Type 3 (3/4)

	0	1	2	3	4	5	6	7
60	CPC AMH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
61	CPC AMH ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
62	CPC AMH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
63	CPC AMH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
64	CPC AML ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ER	Slave 1 LRC unmatch
65	CPC AML ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
66	CPC AML FUBSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
67	CPC AML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
68	CPC ASH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transter count ERR	Slave 1 LRC unmatch
69	CPC ASH ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6A	CPC ASH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6B	CPC ASH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6C	CPC ASL ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
6D	CPC ASL ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6E	CPC ASL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6F	CPC ASL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 3 (4/4)

	0	1	2	3	4	5	6	7
70	CPC BMH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
71	CPC BMH ACERR							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
72	CPC BMH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
73	CPC BMH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
74	CPC BML ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
75	CPC BML ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
76	CPC BML FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
77	CPC BML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
78	CPC BSH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
79	CPC BSH ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
7A	CPC BSH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
7B	CPC BSH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
7C	CPC BSL ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
7D	CPC BSL ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
7E	CPC BSL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
7F	CPC BSL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)

Byte27=F 2 (Cache Failure)Byte 40-7F Common information : Type 4 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected MP							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus eror	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Not used							
	0	0	0	0	0	0	0	0
46	Cache undefined register flag 3 (Slave 1) (b00-03:bus H, b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined registet flag 3 (Slave 2) (b00-03:Bus H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CACHE ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE S1 ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE S1 ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE S1 ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 Board # match	Slave 2 register access	Slave 2 Address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
4C	CACHE S1 BUSERRH							
	Data sequence error	Data stop	DT phase FAFYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE S1 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CACHE S1 ADRERR1L							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode erroe	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 transfer count ER
4F	CACHE S1 ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Access timeout (others)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 4 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE S1 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
51	CACHE S1 ADRERR2L							
	Slave 1 LRC unmatch	Slave 1-2 board # match	Slave 2 register address	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Not used
52	CACHE S1 BUSERR1							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
53	CACHE S1 BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
54	CACHE S2 ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
55	CACHE S2 ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
56	CACHE S2 ADRERR2H							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
57	CACHE S2 ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
58	CACHE S2 BUSERRH							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
59	CACHE S2 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
5A	CACHE S2 ADRERR1L							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
5B	CACHE S2 ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
5C	CACHE S2 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
5D	CACHE S2 ADRERR2L							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Not used
5E	CACHE S2 ADRERR2L							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
5F	CACHE S2 BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 4 (3/4)

	0	1	2	3	4	5	6	7
60	BSA H MONITOR1							
	Side A WR from upper	Side A RD from upper	Side A WR from F bus	A-DBF F bus transfer	B-DBF F bus transfer	Not used	Not used	Not used
61	BSA H MONITOR1							
	Side A command ID code			Side B command ID code			Abort process complete	Not used
62	BSA H MONITOR2							
	A side PLRC ADD bit	Side A bus mode			Side A transfer mode			
63								
	B side PLRC ADD bit	Side B bus mode			Side B transfer mode			
64	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
65	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
67	BSA H CK2AST1							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
68	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
69	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
6A	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blobkade module	Access to blockade cache
6B	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refersh	Setting access unmatch	DIAG mode-access unmatch	SP mode-access unmatch	Master XFR data parity ER
6C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
6D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Master XFR data parity ER
6E	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
6F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmtach	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 4 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H MONITOR1							
	Side A WR from upper	Side A RD from upper	Side A WR from F bus	A-DBF F bus transfer	B-DBF F bus transfer	Not used	Not used	Not used
71	BSA H MONITOR1							
	Side A command ID code			Side B command ID code			Abort process complete	Not used
72	BSA H MONITOR2							
	A side PLRC ADD bit	Side A bus mode			Side A transfer mode			
73								
	B side PLRC ADD bit	Side B bus mode			Side B transfer mode			
74	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
75	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
77	BSA H CK2AST1							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
78	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
79	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7A	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blobkade module	Access to blockade cache
7B	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refersh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
7C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
7D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Master XFR data parity ER
7E	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmtach	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 5 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected MP							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus eror	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Not used							
	0	0	0	0	0	0	0	0
46	Cache undefined register flag 3 (Slave 1) (b00-03:bus H, b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined registet flag 3 (Slave 2) (b00-03:Bus H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CACHE ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE S1 ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE S1 ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE S1 ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 Board # match	Slave 2 register access	Slave 2 Address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
4C	CACHE S1 BUSERRH							
	Data sequence error	Data stop	DT phase FAFYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE S1 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CACHE S1 ADRERR1L							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode erroe	Slave 1 transfer mode ERR	Slave 1 invalid bit	Slave 1 transfer count ER
4F	CACHE S1 ADRERR1L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Access timeout (others)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 5 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE S1 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
51	CACHE S1 ADRERR2L							
	Slave 1 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
52	CACHE S1 BUSERRL							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
53	CACHE S1 BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
54	CACHE S1 ADRERR1H							
	Write enable abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	ADR0 signal parity ER	ADR1 signal parity ER	SYND signal parity ER
55	CACHE S1 ADRERR1H							
	ECC compare error	ECC UNCORREC ERR (read)	ECC error (write)	Not used	LRC0 error (write)	LRC1 error (write)	LRC2 error (write)	LRC3 error (write)
56	CACHE S1 ADRERR2H							
	Clock abnormal	ADRCTL Clock abnormal	ECCTL1 Clock abnormal	ECCTL2 Clock abnormal	Not used	Address counter abnormal	Data XFR counter abnormal	Refresh counter abnormal
57	CACHE S1 ADRERR2H							
	Refresh action abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	Not used	Not used	Not used
58	CPC undefined register flag 1 (AMH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
59	CPC undefined register flag 1 (AML)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5A	CPC undefined register flag 1 (ASH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5B	CPC undefined register flag 1 (ASL)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5C	CPC undefined register flag 1 (BMH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5D	CPC undefined register flag 1 (BML)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5E	CPC undefined register flag 1 (BSH)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			
5F	CPC undefined register flag 1 (BSL)							
	REG 20X	REG 21X	REG 22X	REG 23X 24X	REG 20X	REG 21X	REG 22X	REG 23X 24X
	Access from bus H				Access from bus L			

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 5 (3/4)

	0	1	2	3	4	5	6	7
60	CPC AMH/BMH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
61	CPC AMH/BMH ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
62	CPC AMH/BMH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
63	CPC AMH/BMH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
64	CPC AMH/BMH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
65	CPC AML/BML ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
66	CPC AML/BML FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
67	CPC AML/BML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
68	CPC ASH/BSH ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
69	CPC ASH/BSH ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6A	CPC ASH/BSH FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6B	CPC ASH/BSH JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6C	CPC ASL/BSL ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
6D	CPC ASL/BSL ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6E	CPC ASL/BSL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)
6F	CPC ASL/BSL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Received data parity ER	Data overrun	End response parity ER	(RSV)

Byte27=F 2 (Cache Failure) Byte 40-7F Common information : Type 5 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
71	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	BSA H CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 HO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 HO input DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
73	BSA H CK2AST1							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
74	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
75	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cahce port			Warning detected (cache)
76	BSA H CH2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
77	BSA L CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refersh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
78	BSA L CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
79	BSA L CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	BSA L CK2AST1							
	EXERR1 HI input DT parity ER	EXERR1 LO input DT parity ER	EXERR2 HI input DT parity ER	EXERR2 LO input DT parity ER	Mate BSA error	Slave ID erroe	LRC section data parity ER	LRC section LRC error
7B	BSA L CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
7C	BSA L CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
7D	BSA L CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7E	BSA L CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA L CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC before INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data pairty ER

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 6 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected Mp							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Not used							
	0	0	0	0	0	0	0	0
46	Cache undefined register flag 3 (Slave 1) (b00-03:bus h,b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined register flag 3 (slave 2) (b00-03:Bus, H, b04-07:Bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48	CACHE ADRERR1H/L							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE S1 ADRERR1H/L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE S1 ADRERR2H/L							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE S1 ADRERR2H/L							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Notused
4C	CACHE S1 BUSERRH/L							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE S1 BUSERRH/L							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CHCHE S1 BOADERR							
	Write enable abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CSA1 signal abnormal	ADR0 signal abnormal	ADR0 signal abnormal	SYND signal abnormal
4F	CACHE S1 BOARDERR							
	ECC compare error	ECC UNCORREC ERR (read)	ECC error (write)	Not used	LRC0 error (write)	LRC1 error (write)	LRC2 error (write)	LRC3 error (write)

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 6 (2/4)

	0	1	2	3	4	5	6	7
50	CHCHE S1 CRERR							
	Clock abnormal	ADRCTL Clock abnormal	ECCCTL1 Clock abnormal	ECCCTL2 Clock abnormal	Not used	Address counter abnormal	Data XFR 1 counter abnorma	Refresh counter abnorma
51	CACHE S1 CRERR							
	Refresh action abnormal	RAS0 signal abnormal	RAS1 signal abnorma	CAS0 signal abnorma	CAS1 signal abnorma	Not used	Not used	Not used
52	CACHE MEMERROR0							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
53	CACHE MEMERROR0							
	Byte number 1 with error (low order)		Bit13-17 valid		Byte number 2 with error (high order)			
54	CACHE S2 ADRERR1H/L							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
55	CACHE S2 ADRERR1H/L							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
56	CACHE S2 ADRERR2H/L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 transfer mode ERR	Slave 2 invalid bit	Slave 2 transfer count ERR
57	CACHE S2 ADRERR2H/L							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 addres COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Not used
58	CACHE S2 BUSERRH/L							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
59	CACHE S2 BUSERRH/L							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
5A	CACHE S2 BDRERR							
	Write enable abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CSA1 signal abnormal	ADR0 signal abnormal	ADR0 signal abnormal	SYND signal abnormal
5B	CACHE S2 BDRERR1L							
	ECC compare error	ECC UNCORREC ERR (read)	ECC error (write)	Not used	LRC0 error (write)	LRC1 error (write)	LRC2 error (write)	LRC3 error (write)
5C	CACHE S2CRERR							
	Clock abnormal	ADRCTL Clock abnormal	ECCCTL1 Clock abnormal	ECCCTL2 Clock abnormal	Not used	Address counter abnormal	Data XFR 1 counter abnorma	Refresh counter abnorma
5D	CACHE S2CRERR							
	Refresh action abnormal	RAS0 signal abnormal	RAS1 signal abnorma	CAS0 signal abnorma	CAS1 signal abnorma	Not used	Not used	Not used
5E	CPC undefined register flag 2 (Side A)							
	CPC AMH	CPC AML	CPC ASH	CPC ASL	CPC AMH	CPC AML	CPC ASH	CPC ASL
	Access from bus H				Access form bus L			
5F	CPC undefined register flag 2 (Side B)							
	CPC BMH	CPC BML	CPC BSH	CPC BSL	CPC BMH	CPC BML	CPC BSH	CPC BSL
	Access from bus H				Access form bus L			

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 6 (3/4)

	0	1	2	3	4	5	6	7
60	CPC AMH/AML ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
61	CPC AMH/AML ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
62	CPC AMH/AML FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
63	CPC ASH/AML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
64	CPC ASH/ASL ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
65	CPC ASH/ASL ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
66	CPC ASH/ASL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
67	CPC ASH/ASL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
68	CPC BMH/BML ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
69	CPC BMH/BML ACER2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6A	CPC BMH/BML FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
6B	CPC BMH/BML JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
6C	CPC BSH/BSL ACERR1							
	Slave 1 access PROTCL ER	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 zero error	Slave 1 transfer count ERR	Slave 1 LRC unmatch
6D	CPC BSH/BSL ACERR2							
	Slave 2 access PROTCL ER	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 zero error	Slave 2 transfer count ERR	Slave 2 LRC unmatch
6E	CPC BSH/BSL FBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)
6F	CPC BSH/BSL JBUSERR							
	Data XFR protocol error	Data XFR count unmatch	(RSV)	(RSV)	Recieved data parity ER	Data overrun	End response parity ER	(RSV)

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 6 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H/L MONITOR1							
	Side A WR from upper	Side A RD from uppe	Side A WR from F bus	A -DBF F bus transfer	B -DBF F bus transfer	Not used	Not used	Not used
71	BSA H/L MONITOR1							
	Side A command ID code			Side B command ID code			Abort process complete	Not used
72	BSA H/L MONITOR2							
	A side PLRC ADD bit	Side A bus mode			Side A transfer mode			
73	BSA H/L MONITOR2							
	B side PLRC ADD bit	Side B bus mode			Side B transfer mode			
74	BSA H/L CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
75	BSA H/L CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	BSA H/L CK2AST1							
	EXERR1 HI imput DT parity ER	EXERR1 HO imput DT parity ER	EXERR2 HI imput DT parity ER	EXERR2 HO imput DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
77	BSA H/L CK2AST1							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
78	BSA H/L CK2AST2							
	01 : Slave 1 RESP 10 : Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
79	BSA H/L CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warning information bits for cache port			Warning detected (cache)
7A	BSA H/L CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7B	BSA H/L CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Settingaccess unmatch	DIAG mode -access unmatch	SP mode - access unmatch	Master XFR data parity ER
7C	BSA H/L CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit		Error information bits for cache port		
7D	BSA H/L CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warnig information bits for cache port			Warning detected (cache)
7E	BSA H/L CK2AST5							
		Warning information bits for cache port			Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA H/LCK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27 = F2 (Cache Failure) Byte40-7F Common information : Type 7 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 1 number							
43	MPID:Error detected Mp							
44	Response status							
	F bus H response timeout	CACHE/CPC bus error (F bus H)	H-side BSA bus error	CACHE/CPC abnormal (F bus H)	F bus L response timeout	CACHE/CPC bus error (F bus L)	L-side BSA bus error	CACHE/CPC abnormal (F bus L)
45	Not used							
	0	0	0	0	0	0	0	0
46	Cache undefined register flag 3 (Slave 1)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined register flag 3 (Slave 2)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
48								
	Cache access address							
49								
	Cache access address							
4A								
	Cache access address							
4B								
	Cache access address							
4C								
	Cache access address (for two slave access)							
4D								
	Cache access address (for two slave access)							
4E								
	Cache access address (for two slave access)							
4F								
	Cache access address (for two slave access)							

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 7 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE S1 MEMREADY							
	Memory ready	INHSELF2 valid	Not used	Not used	Not used	Not used	Not used	Not used
51	CACHE S1 CMCMODE							
	DIAG mode	SP mode	Not used	Not used	Not used	Not used	Not used	Not used
52	CACHE S1 MEMCONF							
	Cache size (high)		x' 0003' : 128MB x' 000F' : 256MB x' 003F' : 384MB	x' 00FF' : 512MB x' 03FF' : 640MB x' 0FFF' : 768MB		x' 3FFF' : 896MB x' FFFF' : 1024MB		
53	CACHE S1 MEMCONF							
	Cache size (low)							
54	CACHE S1 MEMENBL							
	1	1	1	1	1	1	1	1
55	CACHE S1 MEMENBL							
	Module group 7 valid	Module group 6 valid	Module group 5 valid	Module group 4 valid	Module group 3 valid	Module group 2valid	Module group 1valid	Module group 0valid
56	CACHE S1 BOARDENBL							
	Board enable	Not used	Not used	Not used	Not used	Not used	Not used	Not used
57	Not used							
58	CACHE S2 MEMREADY							
	Memory ready	INHSELF2 valid	Not used	Not used	Not used	Not used	Not used	Not used
59	SACHE S2 CMCMODE							
	DIAG mode	SP mode	Not used	Not used	Not used	Not used	Not used	Not used
5A	CACHE S2 MEMCONF							
	Cache size (high)		x' 0003' : 128MB x' 000F' : 256MB x' 003F' : 384MB	x' 00FF' : 512MB x' 03FF' : 640MB x' 0FFF' : 768MB		x' 3FFF' : 896MB x' FFFF' : 1024MB		
5B	CACHE S2 MEMCONF							
	Cache size (high)							
5C	CACHE S MEMENBL							
	1	1	1	1	1	1	1	1
5D	CACHE S2 MEMENBL							
	Module group 7 valid	Module group 6 valid	Module group 5 valid	Module group 4 valid	Module group 3 valid	Module group 2valid	Module group 1valid	Module group 0valid
5E	CACHE S2 BOARDENBL							
	Board enable	Not used	Not used	Not used	Not used	Not used	Not used	Not used
5F	Not used							

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 7 (3/4)

	0	1	2	3	4	5	6	7
60	BSA H MONITOR1							
	Side A WR from upper	Side A RD from uppe	Side A WR from F bus	A -DBF F bus transfer	B -DBF F bus transfer	Not used	Not used	Not used
61	BSA H MONITOR1							
	Side A command ID code			Side B command ID code			Abort process complete	Not used
62	BSA H MONITOR2							
	A side PLRC ADD bit	Side A bus mode			Side A transfer mode			
63								
	B side PLRC ADD bit	Side B bus mode			Side B transfer mode			
64	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
65	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
66	BSA H CK2AST1							
	EXERR1 HI imput DT parity ER	EXERR1 HO imput DT parity ER	EXERR2 HI imput DT parity ER	EXERR2 HO imput DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
67	BSA H CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
68	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit		Error information bits for cache port		
69	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warnig information bits for cache port			Warning detected (cache)
6A	BSA H CK2AST3							
		Warning information bits for cache port			Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
6B	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
6C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit		Error information bits for cache port		
6D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warnig information bits for cache port			Warning detected (cache)
6E	BSA H CK2AST5							
		Warning information bits for cache port			Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
6F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 7 (4/4)

	0	1	2	3	4	5	6	7
70	BSA H MONITOR1							
	Side A WR from upper	Side A RD from uppe	Side A WR from F bus	A -DBF F bus transfer	B -DBF F bus transfer	Not used	Not used -	Not used
71	BSA H MONITOR1							
	Side A command ID code			Side B command ID code			Abort process complete	Not used
72	BSA H MONITOR2							
	A side PLRC ADD bit	Side A bus mode			Side A transfer mode			
73								
	B side PLRC ADD bit	Side B bus mode			Side B transfer mode			
74	BSA H CK2AST0							
	CHKERR0 signal input	CHKERR1 signal input	CHKERR2 signal input	CHKERR0,1 majority decision	CHKERR0,2 majority decision	CHKERR1,2 majority decision	Not used	Not used
75	BSA H CK2AST0							
	Last cycle error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
76	BSA H CK2AST1							
	EXERR1 HI imput DT parity ER	EXERR1 HO imput DT parity ER	EXERR2 HI imput DT parity ER	EXERR2 HO imput DT parity ER	Mate BSA error	Slave ID error	LRC section data parity ER	LRC section LRC error
77	BSA H CK2AST2							
	FDB1 data parity ER	FDB2 data parity ER	FDB3 data parity ER	FDB4 data parity ER	FDB5 data parity ER	FDB6 data parity ER	FDB7 data parity ER	FDB8 data parity ER
78	BSA H CK2AST2							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
79	BSA H CK2AST2							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warnig information bits for cache port			Warning detected (cache)
7A	BSA H CK2AST3							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7B	BSA H CK2AST3							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER
7C	BSA H CK2AST4							
	01:Slave 1 RESP 10:Slave 2 RESP		Error typical bit	Warning typical bit	Error information bits for cache port			
7D	BSA H CK2AST4							
	Mate bus error (cache)	Error information bits for cache port		Not used	Warnig information bits for cache port			Warning detected (cache)
7E	BSA H CK2AST5							
	Warning information bits for cache port				Not used	2 bus ACC in 1 bus mode	Access to blockade module	Access to blockade cache
7F	BSA H CK2AST5							
	Board error (others)	Clock/ refresh abnormal	Cache ACC befor INIT	Cache ACC in self refresh	Setting-access unmatch	DIAG mode access unmatch	SP mode access unmatch	Master XFR data parity ER

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 8 (1/4)

	0	1	2	3	4	5	6	7
40	Operation mode							
	Bus using mode		Access sectin	Bus mode		Trasfer mode		
41	slave 1 number							
42	slave 2 number							
43	MPID:Error detected Mp							
44	Not used							
	0	0	0	0	0	0	0	0
45	Not used							
	0	0	0	0	0	0	0	0
46	Cache undefined register flag 3 (Slave 1) (b00-03:bus H,b04-07:bus L)							
	REG 20X	REG 21X	REG 22X	REG 38X	REG 20X	REG 21X	REG 22X	REG 38X
47	Cache undefined registe flag 2(slave 1)							
	REG 00	REG 01X	REG 02X	REG 03X	REG 04X	REG 05X	REG 06X	REG 08X
48	CACHE ADRERR1H							
	Slave 1 sequence error	Slave 1 timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 Transfer mode ERR	Slave 1 invalid bit	Slave 1 count error
49	CACHE S1 ADRERR1H							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Slave 1 timeout (others)
4A	CACHE S1 ADRERR2H							
	Slave 2 sequence error	Slave 2 timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 Transfer mode ERR	Slave 2 invalid bit	Slave 2 count error
4B	CACHE S1 ADRERR2H							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Notused
4C	CACHE S1 BUSERRH							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
4D	CACHE S1 BUSERRH							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
4E	CHCHE S1 BOADERR							
	Slave 1 access SEQ ERR	Slave 1 access timeout	Slave 1 address parity ER	Slave 1 command parity ER	Slave 1 bus mode error	Slave 1 XFR mode error	Slave 1 invalid bit	Slave 1 transfer count ERR
4F	CACHE S1 BOARDERR							
	Slave 1 LRC unmatch	Not used	Not used	Slave 1 address COMP ERR	Slave 1 command COMP ERR	Not used	Not used	Access timeout (others)

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 8 (2/4)

	0	1	2	3	4	5	6	7
50	CACHE S1 ADRERR2L							
	Slave 2 access SEQ ERR	Slave 2 access timeout	Slave 2 address parity ER	Slave 2 command parity ER	Slave 2 bus mode error	Slave 2 XFR mode error	Slave 2 invalid bit	Slave 2 transfer count ERR
51	CACHE S1 ADRERR2L							
	Slave 2 LRC unmatch	Slave 1-2 board # match	Slave 2 register access	Slave 2 address COMP ERR	Slave 2 command COMP ERR	Not used	Not used	Notused
52	CACHE S1 BUSERRL							
	Data sequence error	Data stop	DT phase FASYNC/ FCSYNC	Transfer count unmatch	FENT signal off	ES sequence error	Not used	Not used
53	CACHE S1 BUSERRL							
	Write data parity ER	Write data overrun	Not used	Not used	Not used	Not used	Not used	FENT SIG off (others)
54	CACHE S1 BOARDERR							
	Write enable abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CSA1 signal abnormal	ADR0 signal parity ER	ADR1 signal parity ERl	SYND signal parity ER
55	CACHE S1 BOARDERR							
	ECC compare error	ECC UNCORREC ERR (read)	ECC error (write)	Not used	LRC0 error (write)	LRC1 error (write)	LRC2 error (write)	LRC3 error (write)
56	CACHE S1 CRERR							
	Clock abnormal	ADRCTL Clock abnormal	ECCCTL1 Clock abnormal	ECCCTL2 Clock abnormal	Not used	Address counter abnormal	Data XFR counter abnorma	Refresh counter abnorma
57	CACHE S1 CRERR							
	Refresh action abnormal	RAS0 signal abnormal	RAS1 signal abnormal	CAS0 signal abnormal	CAS1 signal abnormal	Not used	Not used	Not used
58	CACHE MEMERROR0							
	@Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
59	CACHE MEMERROR0							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				
5A	CACHE MEMERROR1							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
5B	CACHE MEMERROR1							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				
5C	CACHE MEMERROR2							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
5D	CACHE MEMERROR2							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				
5E	CACHE MEMERROR3							
	Module group number			Module side number	Bit05-11 valid	Byte number 1 with error (high order)		
5F	CACHE MEMERROR3							
	Byte number 1 with error (low order)		Bit13-17 valid	Byte number 2 with error (high order)				

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 8 (3/4)

	0	1	2	3	4	5	6	7
60	CACHE S1 MEMREADY							
	Memory ready	INHSELF2 invalid	Not used	Not used	Not used	Not used	Not used	Not used
61	CACHE S1 CMCMODE							
	DIAG mode	SP mode	Not used	Not used	Not used	Not used	Not used	Not used
62	CACHE S1 MEMCONF							
	Cache size (high)		x' 0003' : 128MB x' 000F' : 256MB x' 003F' : 384MB	x' 00FF' : 512MB x' 03FF' : 640MB x' 0FFF' : 768MB		x' 3FFF' : 896MB x' FFFF' : 1024MB		
63	CACHE S1 MEMCONF							
	Cache size (low)							
64	CACHE S1 MEMENBL							
	1	1	1	1	1	1	1	1
65	CACHE S1 MEMENBL							
	Module group 7 valid	Module group 6 valid	Module group 5 valid	Module group 4 valid	Module group 3 valid	Module group 2valid	Module group 1valid	Module group 0valid
66	CACHE S1 TESTCTL							
	Test start	Write enable	Not used	Not used	Not used	Not used	Not used	Not used
67	CACHE S1 TESTCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	CACHE S1 TESTADRH							
	Memory address for disconnection							
69	CACHE S1 TESTADRH							
	Memory address for disconnection							
6A	CACHE S1 TESTADRL							
	Memory address for disconnection							
6B	CACHE S1 TESTADRL							
	Memory address for disconnection							
6C	CACHE S1 TESTCNTH							
	Byte count for disconnection							
6D	CACHE S1 TESTCNTH							
	Byte count for disconnection							
6E	CACHE S1 TESTCNTL							
	Byte count for disconnection							
6F	CACHE S1 TESTTCNTL							
	Byte count for disconnection							

Byte27=F 2 (Cache Failure) Byte40-7F Common information : Type 8 (4/4)

	0	1	2	3	4	5	6	7
70	CACHE S1 FRCDIAG							
	ECC WRITE	ECC LWR	FRC BUSY	INH BUSY	FRC BACK UP	Not used	Not used	Not used
71	CACHE S1 BOARDENBL							
	Board enable	Not used	Not used	Not used	Not used	Not used	Not used	Not used
72	CACHE S1 FRCERRH							
	Slave 1 FCSYNC reject	Slave 1 ADR PRTY reverse	Slave 1 CMD PRTY reverse	Slave 2 FCSYNC reject	Slave 2 ADR PRTY reverse	Slave 2 CMD PRTY reverse	FLSTCYCL reject	FRESYNC reject
73	CACHE S1 FRCERRH							
	WR data parity reverse	Not used	Not used	Not used	Not used	Byte position for parity reversion		
74	CACHE S1 FRCERRL							
	Slave 1 FCSYNC reject	Slave 1 ADR PRTY reverse	Slave 1 CMD PRTY reverse	Slave 2 FCSYNC reject	Slave 2 ADR PRTY reverse	Slave 2 CMD PRTY reverse	FLSTCYCL reject	FRESYNC reject
75	CACHE S1 FRCERRL							
	WR data parity reverse	Not used	Not used					
76	CACHE S1 FRCERRB							
	WR ENBL signal reverse	RAS0 dignal reject	RAS1 dignal reject	CAS0 dignal reject	CAS1dignal reject	ADR0 parity reverse	ADR1 parity reverse	SYND data bit reverse
77	CACHE S1 FRCERRB							
	Not used	Not used	Not used	Not used	LSIH/L output reverse	Byte position for parity reversion		
78	CACHE S1 INHECCW1							
	1	1	1	1	1	1	1	1
79	CACHE S1 INHECCW1							
	Module group inhibit warning for memory 1 bit error							
	Module group 7	Module group 6	Module group 5	Module group 4	Module group 3	Module group 2	Module group 1	Module group 0
7A	CACHE S1 INHECCW2							
	1	1	1	1	1	1	1	1
7B	CACHE S1 INHECCW2							
	Module group inhibit warning for memouy 2 bit error							
	Module group 7	Module group 6	Module group 5	Module group 4	Module group 3	Module group 2	Module group 1	Module group 0
7C	CACHE S1 INHREWR1							
	1	1	1	1	1	1	1	1
7D	CACHE S1 INHREWR1							
	Module group inhibit retry memouy 1 bit error							
	Module group 7	Module group 6	Module group 5	Module group 4	Module group 3	Module group 2	Module group 1	Module group 0
7E	CACHE S1 INHREWR2							
	1	1	1	1	1	1	1	1
7F	CACHE S1 INHREWR2							
	Module group inhibit retryemouy 2bit error							
	Module group 7	Module group 6	Module group 5	Module group 4	Module group 3	Module group 2	Module group 1	Module group 0

Byte27 = F2 (Cache Failure) Byte40-7F Common information : Type 9

	0	1	2	3	4	5	6	7
40	Causal Key code							
41	Causal Format/Message							
42	Causal Module ID							
43	Causal Routine ID							
44	Cause of error process (Note 1)							
45	Processor number							
46	LCP number							
47	Cause of error process (Note 2)							
48	Monitoring time for end of transfer							
49								
4A								
4B								
4C	Time of error detection							
4D								
4E								
4F								
50	XFC0 register							
51								
52	XFS0 register							
53								
54	CS1 register							
55								
56	Not used							
57								
58	Command code							
59	Not used							
5A								
5B								
5C	MCI							
5D								
5E								
5F								
60	VDEV and slot number							
61								
62								
63								
64	Slot status							
65								
66								
67								
68	SN							
69								
6A	Block type (Note 3)							
6B	Side type (Note 4)							
6C	Record number							
6D	Key length							
6E	Data length							
6F								
70	Orientation (Note 5)							
71	Subblock number for head of transfer							
72	Offset in subblock							
73								
74	Not used							
7F								

Byte27=F2 (Cache Failure) Byte40-7F Common information : Type 9

(Note 1) Cause of error process

x'00' : CHK2 occured
x'01' : Time over occured in CHA (200ms)
x'02' : Time over occured in ADP (50ms)

(Note 2) Data transfer direction

x'01' : From CHL to cache
x'02' : From cache to CHL
x'03' : From CHL to CBUF
x'04' : From CBUF to CHL
x'05' : From CBUF to cache
x'06' : From cache to CBUF
x'07' : From cache to cache

(Note 3) Block type

x'00' : Data block
x'01' : HA/RO block
x'02' : Bit map block

(Note 4) Side type

x'00' : Cache write side
x'01' : NVS write side
x'02' : Cache read side
x'03' : NVS read side

(Note 5) Orientation

x'00' : Not established
x'01' : Index marker
x'02' : Home address
x'03' : Head of count field
x'04/84' : Count field
x'05/85' : Key field
x'06' : Data field
x'07' : Head of home address
x'08' : Head of index marker

Byte27= F 6 (CFW Access not Authorized) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x' F')				Message (x' 6')			
28	Reason code (x' 01' : CFW ID unmatch)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x' 0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x' 00')							
30	Not used							
31	Module ID							
32	Routine ID							
33	Processor number				Not used			
34	SSID of self subsystem							
35								
36	Symptom code (x' FFF6')							
37								
38	Log and message control (x' 00')							
39	Program action code (x' 00')							
3A	Configuration information							
3B								
3C	Not usde (x' 00')							
3D	Cylinder address							
3E								
3F	Head address							

Byte27= F 6 (CFW Access not Authorized) (2/2)

	0	1	2	3	4	5	6	7
43		Not used						
7F								

Byte27= F A (NVS Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x' F')				Message (x' A')			
28	Reason code (x' 02' : NVS failure)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x' 0000' for EDCC)							
2E								
2F	Mader code & Manufacture code (x' 00')							
30	Not used							
31	Module ID							
32	Routine ID							
33	Processor number				Error code (x' F')			
34	SSID of self subsystem							
35								
36	Symptom code (x' FFFA')							
37								
38	Log and message control (x' 00')							
39	Program action code (x' 00')							
3A	Configuration information							
3B								
3C	Not usde (x' 00')							
3D	Cylinder address							
3E								
3F	Head address							

Byte27=F A (NVS Terminated) (2/2)

	0	1	2	3	4	5	6	7
40	Key cede (for reconnection)							
41	Format/Message (for reconnection)							
42	Module ID (for reconnection)							
43	Routine ID(for reconnection)							
44	Not used							
7F								

Byte27 = FB (HRC/HODM Pair suspend) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'F')				Message (x'B')			
28	R-Vol Suspended	R-Vol failed	Reason code(Note)					
29	RCU device address							
2A	RCU Manufacture code/Factory code							
2B								
2C								
2D	RCU Sequence No.							
2E								
2F	MCU Manufacture code/Factory code							
30								
31								
32	MCU Sequence No.							
33								
34	SSID of self subsystem							
35								
36	Sympton code (x'FE')							
37	Sympton code (same byte #28)							
38	Not used (x'00')							
39	Not used (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Not used (x'00')							
3E	Reference code(x'FFFB')							
3F								

Byte27=FB (HRC/HODM Pair suspend) (2/2)

	0	1	2	3	4	5	6	7
40	Error information							
7F								

(Note) Reason code

X'14'-X'2F'	: Reserved
X'30'	: Pair suspended. MCU device write error.
X'31'	: Pair suspended. RCU subsystem error/or MCU subsystem error.
X'32'	: Pair suspended. RCU device communication error.
X'33'	: Pair suspended (Critical device status). All write command is rejected until pair re-established.
X'34'	: Pair suspended. RCU device is not ready (intervention required).

Byte27= F F (Cache/Shared Memory/M bus/F bus/J bus warning) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x' F')				Message (x' F')			
28	Subcode (See following pages)							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D	SSID of mate subsystem (x' 0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x' 00')							
30	Hardware information (See following pages)							
31	Module ID							
32	Routine ID							
33	Processor number				Message code (x' 0')			
34	SSID of self subsystem							
35								
36	Symptom code (x' FFFF')							
37								
38	Log and message control (x' 00')							
39	Program action code (x' 00')							
3A	Configuration information							
3B								
3C	Not used (x' 00')							
3D	Sylinder address							
3E								
3F	Head address							
40	Hardware information (See following pages)							
7F								

Byte27=FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(1) Byte28=02 : Cache 1 bit error

	0	1	2	3	4	5	6	7
28	Subcode : x'02' : Cache 1 bit error							
29	Slot number of cache board							
2A	MEMERROR 0/1/2/3							
	Module group number			Module side unmber	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
2B	MEMERROR 0/1/2/3							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error • 2nd byte number with 2 bits error				
2C	WARNING							
	Memory 1 bit error	Memory 2 bit error	Not used	Not used	Not used	Not used	Not used	Not used
30	Module number (CMXX : See LOCATION02-50/60)							
40 | 7F	Common information (See "Type 1")							

(2) Byte28 = 03 : Cache 2 bits error

	0	1	2	3	4	5	6	7
28	Subcode : x'03' : Cache 2 bits error							
29	Slot number of cache board							
2A	MEMERROR 0/1/2/3							
	Module group number			Module side unmber	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
2B	MEMERROR 0/1/2/3							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error • 2nd byte number with 2 bits error				
2C	WARNING							
	Memory 1 bit error	Memory 2 bit error	Not used	Not used	Not used	Not used	Not used	Not used
30	Module group number (four CMXX : See LOCATION02-50/60)							
40 | 7F	Common information (See "Type 1")							

Byte27=FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(1) Byte28=04 : Shared memory 1 symbol error

	0	1	2	3	4	5	6	7
28	Subcode : x'04' : Shared memory 1 symbol error							
29	Slot number of shared memory (Side A : x'00' ,Side B : x'01')							
2A	SMC MBUS ERROR STATUS							
	Correctable error	Uncorre-ctable error	Read data check	Write data check	DBL access unmatch	Trnsfer count error	Bus mode error	Transfer mode error
2B	SMC FBUS ERROR STATUS							
	Correctable error	Uncorre-ctable error	Read data check	Write data check	DBL access unmatch	Trnsfer count error	Bus mode error	Transfer mode error
2C	SMC MEMORY READY							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Memory ready
2D	SMC MBUS ERROR LOCATION							
	Smodule with correctable error							
	module 00	module 01	module 02	module 03	module 04	module 05	module 06	module 07
2E	SMC MBUS ERROR LOCATION							
	Smodule with correctable error							
	module 08	module 09	module 10	module 11	module 12	module 13	module 14	module 15
2F	SMC FBUS ERROR LOCATION							
	Smodule with correctable error							
	module 00	module 01	module 02	module 03	module 04	module 05	module 06	module 07
30	SMC FBUS ERROR LOCATION							
	Smodule with correctable error							
	module 08	module 09	module 10	module 11	module 12	module 13	module 14	module 15

40 | 7F	Common information (See "Type 2")

(4) Byte28 = 10 :Three SMC MBUS BUSOPEN lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'10' : Three SMC MBUS BUSOPEN lines inconsistent							
29	Slot number of shared memory (Side A : x'00' ,Side B: x'01')							
2A	SMC MBUS ERROR STATUS							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data check	Command check	Address check
2B	SMC FBUS ERROR STATUS							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data check	Command check	Address check
2C	Not used							

30	Not used

40 | 7F	Common information (See "Type 3")

Byte27 = FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(5) Byte28 = 11/12: Three SMP lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'11' : Three SMP MBUSOPEN lines inconsistent x'12' : Three SMP MCHKERR lines inconsistent							
29	MPID							
2A	SMP MBOPEN R							
	Not used	Not used	Not used	Not used	MBOPEN 0	MBOPEN 1	MBOPEN 2	Warning
2B	SMP MCHKERR R							
	Not used	Not used	Not used	Not used	MCHK error 0	MCHK error 1	MCHK error 2	Warning
2C	SMP FLCHKERR R							
	Not used	Not used	Not used	Not used	FLCHK error 0	FLCHK error 1	FLCHK error 2	Warning

30	Not used

40 ‖ 7F	Common information (See "Type 6")

(6) Byte28 = 14: Three SMC FBUSL BUSOPEN lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'14' : Three SMC FBUSL BUSOPEN lines inconsistent							
29	Slot number of shared memory (Side A:x'00' , Side B : x'01')							
2A	SMC MBUS ERRORSTATUS							
	BUS open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data check	command check	Address check
2B	SMC FBUS ERRORSTATUS							
	BUS open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data check	command check	Address check
2C	Not used							

30	Not used

40 ‖ 7F	Common information (See "Type 4")

Byte27 = FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(7) Byte28 = 16 :Three SMP lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'16' : Three SMP FLCKERR lines inconsistent							
29	MPID							
2A	SMP MBOPEN R							
	Not used	Not used	Not used	Not used	MBOPEN 0	MBOPEN 1	MBOPEN 2	Warning
2B	SMP MCHKERR R							
	Not used	Not used	Not used	Not used	MCHK error 0	MCHK error 1	MCHK error 2	Warning
2C	SMP FLCHKERR R							
	Not used	Not used	Not used	Not used	FLCHK error 0	FLCHK error1	FLCHK error2	Warning
30	Not used							
40 – 7F	Common information (See "Type 6")							

(8) Byte28 = 18/19/1A :Three BSA FBUSH lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'18' : Three BSA FBUSH BUSOPEN lines inconsistent x'19' : Three BSA FBUSH LIVEINS lines inconsistent x'1A' : Three BSA FBUSH CHKERR lines inconsistent							
29	MPID							
2A	BSA H CK2DST1							
	FBUS open 0	FBUS open 1	FBUS open 2	FBUS open 0 & 1	FBUS open 1 & 2	FBUS open 0 & 2	Not used	Not used
2B	BSA H CK2DST2							
	LIVE INS 0	LIVE INS 1	LIVE INS 2	LIVE INS 0 & 1	LIVE INS 0 &2	LIVE INS 1 &2	Not used	Not used
2C	BSA H CK2AST0							
	CHKERR0	CHKERR1	CHKERR2	CHKERR0 & CHKERR1	CHKERR0 & CHKERR2	CHKERR1 & CHKERR2	Not used	Not used
30	Not used							
40 – 7F	Common information (See "Type 5")							

Byte27 = FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(9) Byte28 = 1C/1D/1E : Three BSA FBUSL lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'1C' : Three BSA FBUSL BUSOPEN lines inconsistent x'1D' : Three BSA FBUSL LIVEINS lines inconsistent x'1E' : Three BSA FBUSL CHKERR lines inconsistent							
29	MPID							
2A	BSA L CK2DST1							
	FBUS OPEN 0	FBUS OPEN 1	FBUS OPEN 2	FBUS OPEN 0 & 1	FBUS OPEN 1 &2	FBUS OPEN 0 &2	Not used	Not used
2B	BSA L CK2DST2							
	LIVE INS 0	LIVE INS 1	LIVE INS 2	LIVE INS 0 & 1	LIVE INS 0 & 2	LIVE INS 1 &2	Not used	Not used
2C	BSA L CK2AST0							
	CHKERR0	CHKERR1	CHKERR2	CHKERR0 & CHKERR1	CHKERR0 & CHKERR2	CHKERR1 & CHKERR2	Not used	Not used
30	Not used							
40 | 7F	Common information (See "Type 4")							

(10) Byte28 = 20/21 :Three CPC (H-side) CHKERR lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'20' : Three CPC (AMH/BMH) JBUSH CHKERR lines inconsistent x'21' : Three CPC (ASH/BSH) JBUSH CHKERR lines inconsistent							
29	CPC LSI number							
2A	CPC AMH/BMH WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2B	CPC ASH/BSH WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2C	CPC AML/BML WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
30	CPC ASL/BSL WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
40 | 7F	Common information (See "Type 5")							

Byte27 = FF (Cache/Shared Memory/M bus/F bus/J bus warning) Detail

(11) Byte28 = 24/25 : Three CPC (L-side) CHKERR lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x'24' : Three CPC (AML/BML) JBUSL CHKERR lines inconsistent x'25' : Three CPC (ASL/BSL) JBUSL CHKERR lines inconsistent							
29	CPC LSI number							
2A	CPC AMH/BMH WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2B	CPC ASH/BSH WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2C	CPC AML/BML WARNING							
	F bus FCHKERR0 -2 unmatch	J bus JCHKERR0-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
30	CPC ASL/BSL WARNING							
	F bus FCHKER-2 unmatch	J bus JCHKER-2 unmatch	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
40 | 7F	Common information (See "Type 4")							

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/F bus/J bus warnig) type1 (1/4)

	0	1	2	3	4	5	6	7
40	MEMERROR0							
	Module group number			Module side number	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
41	MEMERROR0							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error •2nd byte number with 2 bits error				
42	MEMERROR1							
	Module group number			Module side number	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
43	MEMERROR1							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error •2nd byte number with 2 bits error				
44	MEMERROR2							
	Module group number			Module side number	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
45	MEMERROR2							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error •2nd byte number with 2 bits error				
46	MEMERROR3							
	Module group number			Module side number	Bit 05-11 valid	Byte # with memory error •Byte # with 1 bit error •Byte # with 2 bits error		
47	MEMERROR3							
	Byte # with memory error		Bit 13-17 valid	Byte # with memory error •2nd byte number with 2 bits error				
48	Not used							
49	Not used							
4A	Not used							
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) type1 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for cache memory 1 bit error							
	Module #0				Module #1			
51	Threshold counter for cache memory 1 bit error							
	Module #2				Module #3			
52	Threshold counter for cache memory 1 bit error							
	Module #4				Module #5			
53	Threshold counter for cache memory 1 bit error							
	Module #6				Module #7			
54	Threshold counter for cache memory 1 bit error							
	Module #8				Module #9			
55	Threshold counter for cache memory 1 bit error							
	Module #10				Module #11			
56	Threshold counter for cache memory 1 bit error							
	Module #12				Module #13			
57	Threshold counter for cache memory 1 bit error							
	Module #14				Module #15			
58	Threshold counter for cache memory 1 bit error							
	Module #16				Module #17			
59	Threshold counter for cache memory 1 bit error							
	Module #18				Module #19			
5A	Threshold counter for cache memory 1 bit error							
	Module #20				Module #21			
5B	Threshold counter for cache memory 1 bit error							
	Module #22				Module #23			
5C	Threshold counter for cache memory 1 bit error							
	Module #24				Module #25			
5D	Threshold counter for cache memory 1 bit error							
	Module #26				Module #27			
5E	Threshold counter for cache memory 1 bit error							
	Module #28				Module #29			
5F	Threshold counter for cache memory 1 bit error							
	Module #30				Module #30			

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) type1 (3/4)

	0	1	2	3	4	5	6	7
60	Threshold counter for cache memory 1 bit error							
	Module #32				Module #33			
61	Threshold counter for cache memory 1 bit error							
	Module #34				Module #35			
62	Threshold counter for cache memory 1 bit error							
	Module #36				Module #37			
63	Threshold counter for cache memory 1 bit error							
	Module #38				Module #39			
64	Threshold counter for cache memory 1 bit error							
	Module #40				Module #41			
65	Threshold counter for cache memory 1 bit error							
	Module #42				Module #43			
66	Threshold counter for cache memory 1 bit error							
	Module #44				Module #45			
67	Threshold counter for cache memory 1 bit error							
	Module #46				Module #47			
68	Threshold counter for cache memory 1 bit error							
	Module #48				Module #49			
69	Threshold counter for cache memory 1 bit error							
	Module #50				Module #51			
6A	Threshold counter for cache memory 1 bit error							
	Module #52				Module #53			
6B	Threshold counter for cache memory 1 bit error							
	Module #54				Module #55			
6C	Threshold counter for cache memory 1 bit error							
	Module #56				Module #57			
6D	Threshold counter for cache memory 1 bit error							
	Module #58				Module #59			
6E	Threshold counter for cache memory 1 bit error							
	Module #60				Module #61			
6F	Threshold counter for cache memory 1 bit error							
	Module #62				Module #63			

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) type1 (4/4)

	0	1	2	3	4	5	6	7
70	Threshold counter for cache memory 2 bit error							
	Module group #0							
71	Threshold counter for cache memory 2 bit error							
	Module group #1							
72	Threshold counter for cache memory 2 bit error							
	Module group #2							
73	Threshold counter for cache memory 2 bit error							
	Module group #3							
74	Threshold counter for cache memory 2 bit error							
	Module group #4							
75	Threshold counter for cache memory 2 bit error							
	Module group #5							
76	Threshold counter for cache memory 2 bit error							
	Module group #6							
77	Threshold counter for cache memory 2 bit error							
	Module group #7							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 2 (1/4)

	0	1	2	3	4	5	6	7
40	SMC SMC CONTROL							
	Retry inhibit module 00	Retry inhibit module 01	Retry inhibit module 02	Retry inhibit module 03	Retry inhibit module 04	Retry inhibit module 05	Retry inhibit module 06	Retry inhibit module 07
41	SMC SMC CONTROL							
	Retry inhibit module 08	Retry inhibit module 09	Retry inhibit module 10	Retry inhibit module 11	Retry inhibit module 12	Retry inhibit module 13	Retry inhibit module 14	Retry inhibit module 15
42	SMC SMC CONTROL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Board error mask
43	SMC SMC CONTROL (REG 0G:B30-37)							
	Not used	Not used	Not used	Refresh mode	Access mode	10X : Data read 110 : ECC read /write 111 : ECC test write		Reverse write inhibit
44	SMC BOARD ERROR STARUS							
45	SMC BOARD ERROR STATUS							
46	SMC BOARD ERROR STATUS							
	RAS output error	CAS output error	WE output error	OE(DIR)output error		Address output error	Data output error	ECC out put error
47	SMC BOARD ERROR STATUS							
	Clock error	Refresh error	Timer error	M bus counter error	M bus timer error	Main sequencer error	M bus sequencer error	F bus sequencer error
48	SMC MBUS ERROR STATUS							
49	SMC MBUS ERROR STATUS							
				Board error	All lock busy	Memory not ready	Back up busy	Double lock error
4A	SMC MBUS ERROR STATUS							
	Correctable error	Uncorrec-table error	Read data check	Write data check	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
4B	SMC MBUS ERROR STATUS							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data chek	Command check	Address check
4C	SMC MBUS ERROR LOCATION							
	Smodule with correctable error							
	module 00	module 01	module 02	module 03	module 04	module 05	module 06	module 07
4D	SMC MBUS ERROR LOCATION							
	Smodule with correctable error							
	module 08	module 09	module 10	module 11	module 12	module 13	module 14	module 15
4E	SMC MBUS ERROR LOCATION							
	Not used	Not used	Not used	Not used	Not used	Memoty element with error		
						Element0	Element1	Element2
						Data memory		
4F	SMC MBUS ERROR LOCATION							
	Memory element with correctable error							
	Element 3	Element 4	Element 5	Element 6	Element7	Element 0	Element 1	Element 2
	Data memory					ECC memory		

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 2 (2/4)

	0	1	2	3	4	5	6	7
50	SMC FBUS ERROR STATUS							
51	SMC FBUS ERROR STATUS							
				Board error	All lock busy	Memory not ready	Back up busy	Double lock error
52	SMC FBUS ERROR STATUS							
	Correctable error	Uncorrec-table error	Read data check	Write data check	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
53	SMC FBUS ERROR STATUS							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	Wait ESYNC error	Data chek	Command check	Address check
54	SMC FBUS ERROR LOCATION							
	Smodule with correctable error							
	module 00	module 01	module 02	module 03	module 04	module 05	module 06	module 07
55	SMC FBUS ERROR LOCATION							
	Smodule with correctable error							
	module 08	module 09	module 10	module 11	module 12	module 13	module 14	module 15
56	SMC FBUS ERROR LOCATION							
	Not used	Not used	Not used	Not used	Not used	Memoty element with error		
						Element0	Element1	Element2
						Data memory		
57	SMC FBUS ERROR LOCATION							
	Memory element with correctable error							
	Element 3	Element 4	Element 5	Element 6	Element7	Element 0	Element 1	Element 2
		Data memory				ECC memory		
58	Threshold counter							
	Module #00							
59	Threshold counter							
	Module #01							
5A	Threshold counter							
	Module #02							
5B	Threshold counter							
	Module #03							
5C	Threshold counter							
	Module #04							
5D	Threshold counter							
	Module #05							
5E	Threshold counter							
	Module #06							
5F	Threshold counter							
	Module #07							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 2 (3/4)

	0	1	2	3	4	5	6	7
60	Threshold counter							
	Module #08							
61	Threshold counter							
	Module #09							
62	Threshold counter							
	Module #10							
63	Threshold counter							
	Module #11							
64	Threshold counter							
	Module #12							
65	Threshold counter							
	Module #13							
66	Threshold counter							
	Module #14							
67	Threshold counter							
	Module #15							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 2 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 3 (1/4)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	Not used							
43	Not used							
44	Not used							
45	Not used							
46	Not used							
47	Not used							
48	Not used							
49	Not used							
4A	Not used							
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 3 (2/4)

	0	1	2	3	4	5	6	7
50	Not used							
51	Not used							
52	Not used							
53	Not used							
54	Not used							
55	Not used							
56	Not used							
57	Not used							
58	Not used							
59	Not used							
5A	Not used							
5B	Not used							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 3 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	Not used							
62	Not used							
63	Not used							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 3 (4/4)

	0	1	2	3	4	5	6	7
70	MBUSOPEN threshold counter for SMC side A							
71	MBUSOPEN threshold counter for SMC side B							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 4 (1/4)

	0	1	2	3	4	5	6	7
40	BSA L CHKERR threshold counter for MPID00							
41	BSA L CHKERR threshold counter for MPID01							
42	BSA L CHKERR threshold counter for MPID02							
43	BSA L CHKERR threshold counter for MPID03							
44	BSA L CHKERR threshold counter for MPID04							
45	BSA L CHKERR threshold counter for MPID05							
46	BSA L CHKERR threshold counter for MPID06							
47	BSA L CHKERR threshold counter for MPID07							
48	BSA L CHKERR threshold counter for MPID08							
49	BSA L CHKERR threshold counter for MPID09							
4A	BSA L CHKERR threshold counter for MPID0A							
4B	BSA L CHKERR threshold counter for MPID0B							
4C	BSA L CHKERR threshold counter for MPID0C							
4D	BSA L CHKERR threshold counter for MPID0D							
4E	BSA L CHKERR threshold counter for MPID0E							
4F	BSA L CHKERR threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 4 (2/4)

	0	1	2	3	4	5	6	7
50	BSA L BUSOPEN threshold counter for MPID00							
51	BSA L BUSOPEN threshold counter for MPID01							
52	BSA L BUSOPEN threshold counter for MPID02							
53	BSA L BUSOPEN threshold counter for MPID03							
54	BSA L BUSOPEN threshold counter for MPID04							
55	BSA L BUSOPEN threshold counter for MPID05							
56	BSA L BUSOPEN threshold counter for MPID06							
57	BSA L BUSOPEN threshold counter for MPID07							
58	BSA L BUSOPEN threshold counter for MPID08							
59	BSA L BUSOPEN threshold counter for MPID09							
5A	BSA L BUSOPEN threshold counter for MPID0A							
5B	BSA L BUSOPEN threshold counter for MPID0B							
5C	BSA L BUSOPEN threshold counter for MPID0C							
5D	BSA L BUSOPEN threshold counter for MPID0D							
5E	BSA L BUSOPEN threshold counter for MPID0E							
5F	BSA L BUSOPEN threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 4 (3/4)

	0	1	2	3	4	5	6	7
60	BSA L LIVEINS threshold counter for MPID00							
61	BSA L LIVEINS threshold counter for MPID01							
62	BSA L LIVEINS threshold counter for MPID02							
63	BSA L LIVEINS threshold counter for MPID03							
64	BSA L LIVEINS threshold counter for MPID04							
65	BSA L LIVEINS threshold counter for MPID05							
66	BSA L LIVEINS threshold counter for MPID06							
67	BSA L LIVEINS threshold counter for MPID07							
68	BSA L LIVEINS threshold counter for MPID08							
69	BSA L LIVEINS threshold counter for MPID09							
6A	BSA L LIVEINS threshold counter for MPID0A							
6B	BSA L LIVEINS threshold counter for MPID0B							
6C	BSA L LIVEINS threshold counter for MPID0C							
6D	BSA L LIVEINS threshold counter for MPID0D							
6E	BSA L LIVEINS threshold counter for MPID0E							
6F	BSA L LIVEINS threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 4 (4/4)

	0	1	2	3	4	5	6	7
70	FBUSOPEN threshold counter for SMC side A							
71	FBUSOPEN threshold counter for SMC side B							
72	Not used							
73	Not used							
74	CHKERR threshold counter for CPC AML							
75	CHKERR threshold counter for CPC ASL							
76	CHKERR threshold counter for CPC BML							
77	CHKERR threshold counter for CPC BSL							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 5 (1/4)

	0	1	2	3	4	5	6	7
40	BSA H CHKERR threshold counter for MPID00							
41	BSA H CHKERR threshold counter for MPID01							
42	BSA H CHKERR threshold counter for MPID02							
43	BSA H CHKERR threshold counter for MPID03							
44	BSA H CHKERR threshold counter for MPID04							
45	BSA H CHKERR threshold counter for MPID05							
46	BSA H CHKERR threshold counter for MPID06							
47	BSA H CHKERR threshold counter for MPID07							
48	BSA H CHKERR threshold counter for MPID08							
49	BSA H CHKERR threshold counter for MPID09							
4A	BSA H CHKERR threshold counter for MPID0A							
4B	BSA H CHKERR threshold counter for MPID0B							
4C	BSA H CHKERR threshold counter for MPID0C							
4D	BSA H CHKERR threshold counter for MPID0D							
4E	BSA H CHKERR threshold counter for MPID0E							
4F	BSA H CHKERR threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 5 (2/4)

	0	1	2	3	4	5	6	7
50	BSA H BUSOPEN threshold counter for MPID00							
51	BSA H BUSOPEN threshold counter for MPID01							
52	BSA H BUSOPEN threshold counter for MPID02							
53	BSA H BUSOPEN threshold counter for MPID03							
54	BSA H BUSOPEN threshold counter for MPID04							
55	BSA H BUSOPEN threshold counter for MPID05							
56	BSA H BUSOPEN threshold counter for MPID06							
57	BSA H BUSOPEN threshold counter for MPID07							
58	BSA H BUSOPEN threshold counter for MPID08.							
59	BSA H BUSOPEN threshold counter for MPID09							
5A	BSA H BUSOPEN threshold counter for MPID0A							
5B	BSA H BUSOPEN threshold counter for MPID0B							
5C	BSA H BUSOPEN threshold counter for MPID0C							
5D	BSA H BUSOPEN threshold counter for MPID0D							
5E	BSA H BUSOPEN threshold counter for MPID0E							
5F	BSA H BUSOPEN threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 5 (3/4)

	0	1	2	3	4	5	6	7
60	BSA H LIVEINS threshold counter for MPID00							
61	BSA H LIVEINS threshold counter for MPID01							
62	BSA H LIVEINS threshold counter for MPID02							
63	BSA H LIVEINS threshold counter for MPID03							
64	BSA H LIVEINS threshold counter for MPID04							
65	BSA H LIVEINS threshold counter for MPID05							
66	BSA H LIVEINS threshold counter for MPID06							
67	BSA H LIVEINS threshold counter for MPID07							
68	BSA H LIVEINS threshold counter for MPID08							
69	BSA H LIVEINS threshold counter for MPID09							
6A	BSA H LIVEINS threshold counter for MPID0A							
6B	BSA H LIVEINS threshold counter for MPID0B							
6C	BSA H LIVEINS threshold counter for MPID0C							
6D	BSA H LIVEINS threshold counter for MPID0D							
6E	BSA H LIVEINS threshold counter for MPID0E							
6F	BSA H LIVEINS threshold counter for MPID0F							

Byte27= F F (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 5 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	CHKERR threshold counter for CPC AMH							
75	CHKERR threshold counter for CPC ASH							
76	CHKERR threshold counter for CPC BML							
77	CHKERR threshold counter for CPC BSL							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 6 (1/4)

	0	1	2	3	4	5	6	7
40	SMP MBUSOPEN threshold counter for MPID 00							
41	SMP MBUSOPEN threshold counter for MPID 01							
42	SMP MBUSOPEN threshold counter for MPID 02							
43	SMP MBUSOPEN threshold counter for MPID 03							
44	SMP MBUSOPEN threshold counter for MPID 04							
45	SMP MBUSOPEN threshold counter for MPID 05							
46	SMP MBUSOPEN threshold counter for MPID 06							
47	SMP MBUSOPEN threshold counter for MPID 07							
48	SMP MBUSOPEN threshold counter for MPID 08							
49	SMP MBUSOPEN threshold counter for MPID 09							
4A	SMP MBUSOPEN threshold counter for MPID 0A							
4B	SMP MBUSOPEN threshold counter for MPID 0B							
4C	SMP MBUSOPEN threshold counter for MPID 0C							
4D	SMP MBUSOPEN threshold counter for MPID 0D							
4E	SMP MBUSOPEN threshold counter for MPID 0E							
4F	SMP MBUSOPEN threshold counter for MPID 0F							

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 6 (2/4)

	0	1	2	3	4	5	6	7
50	SMP MCHKERR threshold counter for MPID 00							
51	SMP MCHKERR threshold counter for MPID 01							
52	SMP MCHKERR threshold counter for MPID 02							
53	SMP MCHKERR threshold counter for MPID 03							
54	SMP MCHKERR threshold counter for MPID 04							
55	SMP MCHKERR threshold counter for MPID 05							
56	SMP MCHKERR threshold counter for MPID 06							
57	SMP MCHKERR threshold counter for MPID 07							
58	SMP MCHKERR threshold counter for MPID 08							
59	SMP MCHKERR threshold counter for MPID 09							
5A	SMP MCHKERR threshold counter for MPID 0A							
5B	SMP MCHKERR threshold counter for MPID 0B							
5C	SMP MCHKERR threshold counter for MPID 0C							
5D	SMP MCHKERR threshold counter for MPID 0D							
5E	SMP MCHKERR threshold counter for MPID 0E							
5F	SMP MCHKERR threshold counter for MPID 0F							

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 6 (3/4)

	0	1	2	3	4	5	6	7
60	SMP FLCHKERR threshold counter for MPID 00							
61	SMP FLCHKERR threshold counter for MPID 01							
62	SMP FLCHKERR threshold counter for MPID 02							
63	SMP FLCHKERR threshold counter for MPID 03							
64	SMP FLCHKERR threshold counter for MPID 04							
65	SMP FLCHKERR threshold counter for MPID 05							
66	SMP FLCHKERR threshold counter for MPID 06							
67	SMP FLCHKERR threshold counter for MPID 07							
68	SMP FLCHKERR threshold counter for MPID 08							
69	SMP FLCHKERR threshold counter for MPID 09							
6A	SMP FLCHKERR threshold counter for MPID 0A							
6B	SMP FLCHKERR threshold counter for MPID 0B							
6C	SMP FLCHKERR threshold counter for MPID 0C							
6D	SMP FLCHKERR threshold counter for MPID 0D							
6E	SMP FLCHKERR threshold counter for MPID 0E							
6F	SMP FLCHKERR threshold counter for MPID 0F							

Byte27 = FF (Cache/shared Mrmory/M bus/F bus/J bus warnig) Common : Type 6 (4/4)

	0	1	2	3	4	5	6	7
70	MBUSOPEN threshold counter for SMC Side A							
71	MBUSOPEN threshold counter for SMC Side B							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

Byte0F : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x'6')				Format (x'3')			
27	Operation byte of LR/LRE command parameter							
28	Auxiliary byte of LR/LRE command parameter							
29	Byte 2 for LR/LRE command							
2A	Reserved							
2B								
2C	Search parameter of LR command(CCHHR)							
2D	or							
2E	Record ID of re-execution command(R)							
2F								
30	Sector number to re-execute the LR command							
31	TLF for LR/LRE command							
32								
33	Operation byte = 0x3F :LRE External operation byte others :Reserved							
34	SSID (Low) of self subsystem							
35								
36	Exception code (x'08C1')							
37								
38	Log and message control (x'05')							
39	Program action code (x'10')							
3A	Configuration information							
3B								
3C	Not usde (x'01')							
3D	Cylinder address							
3E								
3F	Head address							

Byte0F : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (2/2)

	0	1	2	3	4	5	6	7
40								
41		Not used						
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
⋮								
7F								

Byte0F : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception: Incomplete Domain) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x'6')				Format (x'4')			
27	Operation byte of LR/LRE command parameter							
28	Extension operation byte of LR/LRE command parameter							
29	Head address of extent (DX command parameter)							
2A								
2B								
2C								
2D								
2E	Path group ID (byte 1 to 7 of the ID by the last Set Path Group ID command)							
2F								
30								
31								
32								
33								
34	SSID (Low) of self subsystem							
35								
36	Exception code (x'0212')							
37								
38	Log and message control (x'05')							
39	Program action code (x'10')							
3A	Configuration information							
3B								
3C	Not usde (x'01')							
3D	Cylinder address							
3E								
3F	Head address							

Byte0F : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception : Incomplete Domain) (2/2)

	0	1	2	3	4	5	6	7
40								
41		Not used						
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55	Module ID (detected error)							
56	Routine ID (detected error)							
57	Not used							
⋮								
7F								

Byte0F : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cache DKC)							
23	Count							
24	Device address							
25	Device type (x'24' :DKU87I-3)							
26	Content				Format (x'1')			
27	Sector number (Note 1)							
28	Cylinder address (Note 1)							
29								
2A	Head address (Note 1)							
2B								
2C	Record number (Note 1)							
2D	Error displacement (Note 1)							
2E								
2F	Drive serial number (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception class (x'4')				Message (Note 2)			
37	Correction flag (Note 3)							
38	Log and message control (x'08')							
39	Program action code (x'91')							
3A	Configuration information							
3B								
3C	Not usde (x'01')							
3D	Cylinder address							
3E								
3F	Head address							

Byte0F : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (2/3)

	0	1	2	3	4	5	6	7
40	Causal Key code							
41	Causal Format/Message							
42	Causal Module ID							
43	Causal Routine ID							
44	VDEV number, slot number							
45								
46								
47								
48	Slot status							
49								
4A								
4B								
4C	staging bit map/Dirty bit map							
4D								
4E								
4F								
50	Current subblock number							
51	EXIT falg (Note 4)							
52	Slot failure information (Note 5)							
53	Obtained information flat (Note 6)							
54	Head subblock number for HIT/MISS decision + Remain subblock count							
55	(when byte36 is x'40/41/42/43') / PACC in CBUF (when byte36 is x'45')							
56	Not used (when byte36 is x'40/41/42/43') /							
57	PAHF in CBUF (when byte36 is x'45')							
58	Not used (when byte36 is x'40/41/42/43') /							
59	Current CC in JCB (when byte36 is x'45')							
5A	Not used (when byte36 is x'40/41/42/43') /							
5B	Current HH in JCB (when byte36 is x'45')							
5C								
	Reserved							
7F								

(Note 1) Not determined for occurrence in HA or RO

(Note 2) Contents of message

x'0' : Data check in HA field
x'1' : Data check in C field
x'2' : Data check in K field
x'3' : Data check in D field
x'4' : Missing SYNC byte in HA field
x'5' : Missing SYNC byte in C field (PA error)
x'6' : Missing SYNC byte in K field
x'7' : Missing SYNC byte in D field
x'8' : Not used
x'9' : Missing AM during retry
x'A'to x'F' : Not used

(Note 3) Contents of correctionflag

Bits 0 and 1 : ECC correction bit
10 : Correctable (Recoverd)
11 : Uncorrectable
Bit 2 : offset activ
Bits 3 to 7 : Not used

Byte0F : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (3/3)

(Note 4) EXIT flag

x'08' : CHL I/F CHK2 timeover
x'0D' : EOF
x'0E' : DSB=0E requested
x'0F' : Logical error
x'1E' : Make sense only
x'1F' : Logical error (make sense only)
x'30' : Selective reset requested
x'40' : 'Staging' requested
x'41' : 'Waiting free segment' requested
x'42' : 'Timeover of waiting for staging' requested
x'43' : 'Staging for PA unmatch' requested
x'45' : 'Destaging' requested
x'46' : 'High priority destaging' requested
x'47' : 'Pseud-through process' requested
x'4B' : 'DSB=4E retry' requested (data transfer)
x'4E' : 'DSB=4E retry' requested (DSB=4E retry)
x'4F' :STG requested (Read or STG in progress)

(Note 5) Slot failure

x'80' : Sector write error
x'40' : Sector read error
x'20' : ECC/LRC error
x'10' : Incomplete data
x'08' : No decision

(Note 6) Obtained information flag

bit0-1 : Block type
- 00 : Data block
- 01 : HA/RO block
- 10 : Bit map block

bit2-3 : Side
- 00 : Cache write side
- 01 : NVS write side
- 10 : Cache read side

bit4 : Segment
- 0 :No segment
- 1 :Segment exist

bit5-7 : Reserved

Byte36 = 6F (Subsystem Information) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cace DKC)							
23	Command overrun threshold exceeded							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Unused(0)	Format (x'1')			
27	Data overrun hreshold exceeded							
28	Seek count							
29								
2A	Drive serial number (x'0C') +							
2B	(x'69') +							
2C	(DKU sequence number)							
2D								
2E								
2F	DKC serial number (x'0C') +							
30	(x'69') +							
31	(x'00') +							
32	(DKC sequence number : high) +							
33	(DKC sequence number : low)							
34	SSID of self subsystem							
35								
36	Exception code Y : 0 : Statistics/RRBL command, 2 : Channel data overrun							
37	(x'6FXY') X : For serial CHL : LCP#, For parallel CHL : CHL#							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Read/search byte count							
3D								
3E								
3F								
40	Not used							
7F								

Byte36 : Bit0-3 = D & Byte27 : bit0-2 = 7 (SPC Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used	Format (x'1')			
27	Type code (b'111')			Not used	Reserved			
28	SPC interuption status register (See SSBLOG05-4334 ~ 4337)							
29	SPC comand step register (See SSBLOG05-4338 ~ 4340)							
2A	SCSI command code (See SSBLOG05-4348)							
2B	Threshold type (See SSBLOG05-4341)							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number* (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x'Dxyz') x : DKA number							
37	y : CDEV number z : RDEV number							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte36 : Bit0-3 = D & Byte27 : bit0-2 = 7 (SPC Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Status byte							
41	Message							
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	SPC status register							
4D	SPC nexus status register							
4E	SPC data block register							
4F								
50	SPC data byte register							
51								
52								
53	SPC SCSI control signal status register							
54	SCA SFC							
55								
56	SCA SFS0							
57								
58	SCA XFS1							
59								
5A	SCA INT							
5B								
5C	SCA SCHK1							
5D								
5E	SCA SCHK20							
5F								
60	SCA SCHK21							
61								
62	SCA SCHK22							
63								
64	SCA SCHK23							
65								
66	SCA SCHK24							
67								
68	SCA SCHK25							
69								
6A	SCA SCACHK2							
6B								
6C	SCA BSACHK2							
6D								
6E	SCA XFS2							
6F								
70	SCA XFS3							
71								
72	Not used							
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

Interruption status codes

1. Interruption related to SCSI reset

Interruption code	Cause of interruption	Conditions for interruption
01h	RESET-CONDITION DETECTED	Reset status has been detected on the SCSI bus.

2. Interruption related to transfer

Interruption code	Cause of interruption	Conditions for interruption
24h	SCSI parity error	A parity error has been detected in the input/output data of the SCSI interface in the current phase.
22h	MPU parity error	A parity error has been detected in the output data of the MPU interface during program transfer (data phase).
21h	DMA parity error	A parity error has been detected in the input/output data of the DMA interface during DMA transfer (data phase).
26h	SCSI parity error & MPU parity error	A parity error has been detected in the input/output data of the MPU and SCSI interfaces during program transfer (data phase).
25h	SCSI parity error & DMA parity	A parity error has been detected in the input/output data of the DMA and SCSI interfaces during DMA transfer (data phase).
29h	Offset error	More REQ/ACK signals have been received in synchronous transfer than the offset value that is set
2Ah	Short transfer period error	SPC could not be tracked during synchronous transfer because the cycle of the received REQ/ACK signal was short.
2Bh	Offset error & Short transfer period error	An offset error and short transfer period error have been detected during synchronous transfer.
2Ch	REQ/ACK timeout	The time that is set for REQ/ACK TIMEOUT has been exceeded.
31h	Disconnected in transfer progress	Bus free status has been detected during phase execution (transfer operation).
32h	Phase error in transfer progress	A phase error has occurred during phase execution (transfer operation).

3. Interruption related to phase transition

Interruption code	Cause of interruption	Conditions for interruption
54h	Initial phase error*	Inconsistency occurred when the phase of the received C. COMMAND received the first REQ signal.
55h	Initial phase error & MSG received†	An initial phase error occurred and one message was received for the target MSG-IN request.
56h	Initial phase error & STATUS received†	An initial phase error occurred and one STATUS was received for the target STATUS receive request.
42h	Command stop (ATN condition detected)††	During execution of the data phase that failed in phase transition due to the generation of the ATN condition of the initiator, the transfer is stopped at the transfer block boundary and this interruption is reported. (At this time, the data register is empty.)
43h	Command stop (ATN condition detected & MSG received)†	One message was received after responding to the MSG-OUT request of the initiator that failed in phase transition due to the generation of the ATN condition of the initiator. During execution of the data phase, one message is received after responding at the transfer block boundary. (At this time, the data register is empty.)

* If a phase error has occurred and the DATAIN phase has been requested, the operation is as follows:

1) When the target with a nexus is in the asynchronous transfer mode

   One-byte data is received.

2) When the target with a nexus is in the synchronous transfer mode

   The number of bytes for the received REQ signal are received (ACK signal is not asserted).

† Occurs only when the AUTO receive mode is set.

†† Occurs only when the AUTO receive mode is not set.

4. Interruption related to report

Interruption code	Cause of interruption	Conditions for interruption
60h	Command complete	Received command has ended normally.
64h	Command Reject	1) A command has been received during automatic operation of this SPC (AUTO selection/reselection response). 2) Another command has been received during execution of a command. 3) The message length is 33 or more bytes when the SEND MSG command for EXTEND-MSG has been received.
65h	Command Invalid	1) A command of the target has been received during operation as an initiator. 2) A command of the initiator has been received during operation as a target. 3) A sequential command is present in the user program memory. 4) The received command code is not defined. 5) A command that requires the setting of the data block register/data byte register (MC byte counter) has been received, but the register value is "0". 6) Transfer is impossible because the CDB length of group 6/7 is set to "0". 7) The CDB of group 3/4 or a transfer command has been received.
66h	REG parity error detected	A parity error has been detected in the register set by the host MPU.
67h	COMMAND PAUSE	1) The COMMAND PAUSE command was received and processing ended.
68h	Self-diagnostic result "GOOD"	Self-diagnostics are performed, and the result is "normal."
69h	Self-diagnostic result "NO GOOD"	Self-diagnostics are performed, and the result is "abnormal."
70h	Disconnected	Bus free status has been detected while making a nexus as an initiator.
71h	REQ Asserted	Next phase execution is requested from the target. This interruption occurs only when no command is received in the nexus.
61h	Command complete (ATN condition detected)	The command ends normally and the ATN condition generated by the initiator is detected only when an ATN signal is asserted when an ACK signal is asserted for the last phase of the executed command.
62h	Command complete (ATN condition detected & MSG received)	A command has ended normally and one message has been received after responding to the ATN condition generated by the initiator. An ATN signal is detected only when an ATN signal is asserted when an ACK signal is asserted for the last phase of the executed command.

5. Interruption related to selection/reselection

Interruption code	Cause of interruption	Conditions for interruption
82h	Sel/Reselection timeout	The time that is set for selection/reselection timeout has been exceeded.
90h	Reselected	The target has been reset as the initiator.
80h	Selected	The initiator has been selected as the target.
81h	Selected with ATN	The initiator has been selected as the target, and the ATN condition generated by the initiator has been detected.

5. Interruption related to response operation for auto selection/reselection

Interruption code	Cause of interruption	Conditions for interruption
B0h	AUTO mode phase error	The reselection phase changed to a phase other than the MSG-IN phase.
B1h	MSG received	After the reselection phase, one message was received.
A0h	AUTO mode phase error	No ATN signal was asserted in the selection phase. This interruption occurs only when the MSG-OUT phase is set after the selection phase.
A1h	MSG received	After the selection phase, a message other than Identify-MSG was received.
A2h	Illegal Identify MSG received	Identify-MSG was received after the selection phase, but bits 5, 4, and 3 are set to ē1í.
A3h	MSG received with Identify MSG	After the selection phase, Identify-MSG was received, followed by another message.
A4h	unknown CDB received	After the selection phase, an attempt to receive one command was made, but only one byte was received because the CD8 length of group 6 or 7 was unobtainable. This interruption occurs only when the MSG or CMD phase is set after the selection phase.
A5h	unknown CDB received with Identify MSG	After the selection phase, an attempt was made to receive a command following Identify-MSG, but only one byte was received because the CD8 length of group 6 or 7 was unobtainable.
A6h	CMD received **	After the selection phase, one command was received. This interruption occurs only when the MSG or CMD phase is set after the selection phase.
A7h	CMD received with Identify MSG	After the selection phase, Identify-MSG was received, followed by a command.
A8h	CMD received & MSG received	After the selection phase, one command was received. Then one message was received for the attention status. This interruption occurs only when the MSG or CMD phase is set after the selection phase.
A9h	CMD received with Identify MSG received	After the selection phase, Identify-MSG was received, followed by a command. Then one message was received for the attention status.

Command step

No.	Command name	Function	STEP	Description
1	RESELECTION & 1-MSG	1) Performs reselection. 2) Changes to the MSG-IN phase. 3) Issues a message.	X'00'	Command received BUS FREE phase awaited
			X'01'	BUS FREE phase detected During arbitration
			X'02'	Bus use right acquired During reselection
			X'03'	Nexus established Transition to the MSG-IN phase MSG-IN phase running
			X'04'	All MSG bytes being issued Command complete
2	RESELECTION & N-Byte-MSG	1) Performs reselection. 2) Changes to the MSG-IN phase. 3) Issues a message.	X'00'	Command received BUS FREE phase awaited
			X'01'	BUS FREE phase detected During arbitration
			X'02'	Bus use right acquired During reselection
			X'03'	Nexus established Transition to the MSG-IN phase MSG-IN phase running
			X'04'	All MSG bytes being issued Command complete
3	RESELECTION & TERMINATE	1) Performs reselection. 2) Performs the Terminate sequence.	X'00'	Command received BUS FREE phase awaited
			X'01'	BUS FREE phase detected During arbitration
			X'02'	Bus use right acquired During reselection
			X'03'	Nexus established Transition to the STATUS phase STATUS phase running
			X'04'	STATUS issuance complete Transition to the MSG-IN phase MSG-IN phase running
			X'05'	Message issuance complete Disconnect Command complete
4	RESELECTION & LINK TERMINATE	1) Performs reselection. 2) Performs the LINK-Terminate sequence.	X'00'	Command received BUS FREE phase awaited
			X'01'	BUS FREE phase detected During arbitration
			X'02'	Bus use right acquired During reselection
			X'01'	Nexus established Transition to the STATUS phase STATUS phase running
			X'03'	STATUS issuance complete Transition to the MSG-IN phase MSG-IN phase running
			X'04'	All MSG bytes being issued Command complete

No.	Command name	Function	STEP	Description
5	TERMINATE	1) Changes to the STATUS phase. 2) Issues one-byte status. 3) Changes to the MSG-IN phase. 4) Issues a one-byte message. 5) Disconnect	X'00'	Command received
			X'01'	During transition to the STATUS phase STATUS phase running
			X'02'	STATUS issuance complete Transition to the MSG-IN phase MSG-IN phase running
			X'03'	Message issuance complete Disconnect Command complete
6	LINK TERMINATE	1) Changes to the STATUS phase. 2) Issues one-byte status. 3) Changes to the MSG-IN phase. 4) Issues a one-byte message.	X'00'	Command received BUS FREE phase awaited
			X'01'	Transition to the STATUS phase STATUS phase running
			X'02'	STATUS issuance complete Transition to the MSG-IN phase MSG-IN phase running
			X'03'	Message issuance complete Command complete
7	DISCONNECT SEQUENCE	1) Changes to the MSG-IN phase. 2) Issues a two-byte message. 3) Disconnect	X'00'	Command received BUS FREE phase awaited
			X'01'	Transition to the MSG-IN phase MSG-IN phase running
			X'02'	Two-byte message issuance complete Disconnect Command complete
8	SEND N-Byte-MSG	1) Changes to the MSG-IN phase 2) Issues N-byte messages (two or more messages)	X'00'	Command received
			X'03'	Transition to the MSG-IN phase MSG-IN phase running
			X'04'	All MSG bytes being issued Command complete
9	RECEIVE N-Byte-CMD	1) Changes to the CMD phase. 2) Receives an N-byte CDB (undefined CDB).	X'00'	Command received
			X'04'	Transition to the CMD phase CMD phase running
			X'05'	All CDB bytes received completely Command complete
10	RECEIVE N-Byte-MSG	1) Transition to the MSG-OUT phase 2) Receives an N-byte CDB (33 bytes or more messages).	X'00'	Command received
			X'02'	Transition to the MSG-OUT phase MSG-OUT phase running
			X'03'	All message bytes received completely Command complete
11	RESELECTION	Performs reselection.	X'00'	Command received BUS FREE phase awaited
			X'01'	BUS FREE phase detected During arbitration
			X'02'	Bus use right acquired During reselection
			X'03'	Nexus established Command complete
12	SET REQ	Asserts REQ.	X'00'	Command received
			X'01'	C. Command Complete
13	RESET REQ	Negates REQ.	X'00'	Command received
			X'01'	C. Command Complete

No.	Command name	Function	STEP	Description
14	Disconnect	Releases a BSY signal.	X'00'	Command received
			X'01'	C. Command Complete
15	SEND DATA from MPU	1) Changes to the DATA-IN. phase. 2) Issues data in the program transfer mode	X'00'	Command received
			X'01'	Transition to the DATA-IN phase DATA-IN phase running
			X'02'	All data bytes received completely Command complete
16	SEND DATA from DMA	1) Changes to the DATA-IN. phase. 2) Issues data in the program transfer mode	X'00'	Command received
			X'01'	Transition to the DATA-IN phase DATA-IN phase running
			X'02'	All data bytes received completely Command complete
17	RECEIVE DATA from MPU	1) Changes to the DATA-OUT phase. 2) Receives data in the program transfer mode.	X'00'	Command received
			X'01'	Transition to the DATA-OUT phase. DATA-OUT phase running
			X'02'	All data bytes received completely Command complete
18	RECEIVE DATA from DMA	1) Changes to the DATA-OUT phase. 2) Receives data in the program transfer mode.	X'00'	Command received
			X'01'	Transition to the DATA-OUT phase. DATA-OUT phase running
			X'02'	All data bytes received completely Command complete
19	SEND 1-MSG	1) Changes to the MSG-IN phase 2) Issues a message.	X'00'	Command received
			X'01'	Transition to the MSG-IN phase MSG-IN phase running
			X'02'	All message bytes issued completely Command complete
20	RECEIVE MSG	1) Changes to the MSG-OUT phase. 2) Issues a message.	X'00'	Command received
			X'01'	Transition to the MSG-OUT phase MSG-OUT phase running
			X'02'	All message bytes received completely Command complete
21	SEND STATUS	1) Changes to the STATUS phase. 2) Issues one-byte status.	X'00'	Command received
			X'01'	Transition to the STATUS phase STATUS phase running
			X'02'	STATUS issuance complete Command complete
22	RECEIVE CMD	1) Changes to the CMD phase. 2) Receives CDB.	X'00'	Command received
			X'01'	Transition to the CMD phase CMD phase running
			X'02'	All CDB bytes received completely Command complete

Threshold type

Code	Threshold (failure) type	Code	Threshold (failure) type
00	CHA CHK1A	30	Cache 1 bit correctable error
01	CHA CHK1B	31	Cache uncorrectable error
02	CHA CHK3	32	Cache 2 bits correctable error
03	CHA CHK2	33	CPC check error
04	CHA ADP temporary error	40	SCSI port failure
05	LCM hardware error	41	Drive mechanism recovered error
06	BSA F bus open	42	Drive mechanism unrecovered error
07	BSA LIVEINS	43	Drive media recovered error
08	BSA check error	44	Drive media unrecovered error
09	SMP M bus open	45	Drive R/W recovered error
0A	SMP M bus check error	46	Drive R/W unrecovered error
0B	SMP H/L check error	47	Drive interface recovered error
10	DKA CHK1A	48	Drive interface unrecovered error
11	DKA CHK1B	49	Controller recovered error
12	DKA CHK3	4A	Controller unrecovered error
13	DKA SCA temporary error	4B	SCSI interface recovered error
14	DKA DRR temporary error	4C	SCSI interface unrecovered error
16	BSA F bus open	4D	Drive I/O read error
17	BSA LIVEINS	4E	Drive I/O write error
18	BSA check error	60	SVP interface error
19	SMP M bus open	FF	Invalid threshold type
1A	SMP M bus check error		
1B	SMP H/L check error		
20	Shared memory correctable error		
21	Shared memory uncorrectable error		
22	SMC M bus open		
23	SMC H/L bus open		

Byte36 : Bit0-3 = D & Byte27 : bit0-2 = 0 (Drive Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used	Format (x'1')			
27	Type code (b'000')			Not used	Sense key (Note 1)			
28	Additional sense code (Note 2)							
29	Additional sense code qualifier (Note 2)							
2A	SCSI Command (Note 3)							
2B	Threshold type (Note 4)							
2C	Module ID (≠ x'50/52')							
2D	Routine ID							
2E	Not used							
2F	Drive serial number* (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x'Dxyz') x : DKA number							
37	y : CDEV number z : RDEV number							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte36 : Bit0-3 = D & Byte27 : bit0-2 = 0 (Drive Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
40	Status byte							
41	Message							
42	CDB							
4B								
4C	SPC status register							
4D	SPC nexus status register							
4E	SPC data block register							
4F								
50	SPC data byte register							
51								
52								
53	SPC SCSI control signal status register							
54	SCSI extended sense data							
73								
74	Not used							
7F								

(Note 1) Sense key

x'0' : No sense
x'1' : Recoverd error
x'2' : Not ready
x'3' : Medium error
x'4' : Hardware error
x'5' : Illigal request
x'6' : Unit attention
x'7' : Data protect
x'8' : Blank check (Not used)
x'9' : Vender unique (Not used)
x'A' : Copy aborted (Not used)
x'B' : Aborted command
x'C' : Equal (Not used)
x'D' : Volume overflow (Not used)
x'E' : Miscompare
x'F' : (Reserved)

(Note 2) See SSBLOG05-350~SSBLOG05-4390

(Note 3) SCSI command

x'00' : Test unit ready
x'03' : Request sense
x'04' : Format unit
x'07' : Reassign blocks
x'12' : Inquiry
x'15' : Mode serect
x'1A' : Mode sense
x'1B': Start/stop unit
x'1C' : Recieve diagnostic result
x'1D' : Send diagnostic
x'28' : Read (extend)
x'2A' : Write (extend)
x'2E' : Write and verify
x'3B' : Write buffer

(Note 4) See SSBLOG05-4400

Byte36 : Bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Detected Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used	Format (x'0')			
27	Type code (b'000')			Not used	Sense key (Note 1)			
28	Additional sense code (Note 2)							
29	Additional sense code qualifier (Note 2)							
2A	SCSI Command (Note 3)							
2B	Threshold type (Note 4)							
2C	Module ID (≠ x'5X/6X')							
2D	Routine ID							
2E	Not used							
2F	Drive serial number* (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x'Exyz') x : DKA number							
37	y : CDEV number z : RDEV number							
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

3yte36 : Bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Status byte							
41	Message							
42	CDB							
⋮								
4B								
4C	SPC status register							
4D	SPC nexus status register							
4E	SPC data block register							
4F								
50	SPC data byte register							
51								
52								
53	SPC SCSI control signal status register							
54	SCSI extended sense data							
⋮								
73								
74	Not used							
⋮								
7F								

(Note 1) Sense key

x'0' : No sense
x'1' : Recoverd error
x'2' : Not ready
x'3' : Medium error
x'4' : Hardware error
x'5' : Illigal request
x'6' : Unit attention
x'7' : Data protect
x'8' : Blank check (Not used)
x'9' : Vender unique (Not used)
x'A' : Copy aborted (Not used)
x'B' : Aborted command
x'C' : Equal (Not used)
x'D' : Volume overflow (Not used)
x'E' : Miscompare
x'F' : (Reserved)

(Note 3) SCSI command

x'00' : Test unit ready
x'03' : Request sense
x'04' : Format unit
x'07' : Reassign blocks
x'12' : Inquiry
x'15' : Mode serect
x'1A' : Mode sense
x'1B' : Start/stop unit
x'1C' : Recieve diagnostic result
x'1D' : Send diagnostic
x'28' : Read (extend)
x'2A' : Write (extend)
x'2E' : Write and verify
x'3B' : Write buffer

Reference code of MP detected SIM for HRC/HODM (2/2)

Error		REF CODE 22	23	13	SIM 28	Level of error	Host report	Remarks
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	32	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	33	XX	FE	Service	No	XX: LDEV number
	MCU detected an Acute or Serious Level SIM for RCU.	DF	40	XX	FE	Serious	Yes	XX: LDEV number
	MCU detected a Moderate Level SIM for RCU.	DF	48	XX	FE	Moderate	Yes	XX: LDEV number

*1:Contents of byte37 when a temperature abnormality occured

Byte37	Error
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.

*2:Contents of byte37 when a voltage alarm was given

Byte37	Error
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.

*3:Contents of byte37 when a voltage warning was given

Byte37	Error
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow80%.

3yte36 : Bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Detected Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Status byte							
41	Message							
42	CDB							
4B								
4C	SPC status register							
4D	SPC nexus status register							
4E	SPC data block register							
4F								
50	SPC data byte register							
51								
52								
53	SPC SCSI control signal status register							
54	SCSI extended sense data							
73								
74	Not used							
7F								

(Note 1) Sense key

x'0' : No sense
x'1' : Recoverd error
x'2' : Not ready
x'3' : Medium error
x'4' : Hardware error
x'5' : Illigal request
x'6' : Unit attention
x'7' : Data protect
x'8' : Blank check (Not used)
x'9' : Vender unique (Not used)
x'A' : Copy aborted (Not used)
x'B' : Aborted command
x'C' : Equal (Not used)
x'D' : Volume overflow (Not used)
x'E' : Miscompare
x'F' : (Reserved)

(Note 3) SCSI command

x'00' : Test unit ready
x'03' : Request sense
x'04' : Format unit
x'07' : Reassign blocks
x'12' : Inquiry
x'15' : Mode serect
x'1A' : Mode sense
x'1B' : Start/stop unit
x'1C' : Recieve diagnostic result
x'1D' : Send diagnostic
x'28' : Read (extend)
x'2A' : Write (extend)
x'2E' : Write and verify
x'3B' : Write buffer

Byte36 : bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Error)

(Note 2) Additionel sense code + AdAdditional sense code qualifier (1/3)

Sense key	Code *	Meanning
0	00 00	No additionsl sense information
4	01 00	No index/sector signal
1/4	02 00	No seek complete
1/4	03 00	Write fault
1/4	03 80	Write at inhibit condition
2	04 00	Drive not ready
2	04 01	Drive is in process of becoming ready
2	04 02	Drive not ready,initializing command required
2	04 04	Drive not ready,format in progress
2	04 80	Drive not ready
2	05 00	Drive not selected (Not used)
1/4	06 00	Not track zero found
4	08 00	Logical unit communication failure
4	08 01	Logical unit communication timeout
4	08 02	Logical unit communication parity error
1/4	09 00	Track following error
1/4	09 80	Track positioning error during ATN off to MESDI CMD execute
1	0C 01	Write error recoverd with auto reallocation (Not used)
3	0C 02	Write error-auto reallocation failed (Not used)
3	10 00	ID CRC error (Not used)
3	11 00	Unrecovered read error
3	11 01	Read retries exhausted
3	11 02	Error too long to correct
3	11 04	Unrecovered read error-auto reallocation failed (Not used)
3	11 82	Error too long to Multi- symbol soft correction
3	12 00	No address mark found in ID field (Not used)
1/3	13 00	No address mark found in Data field
1/3	13 80	Sprit data AM not found
1	13 E1	Data AM not found: Recovered with VFO Hi-gain offset (1)
1	13 E2	Data AM not found: Recovered with VFO Hi-gain offset (2)
1	13 E3	Data AM not found: Recovered with VFO Hi-gain offset (3)
1	13 E4	Data AM not found: Recovered with VFO Hi-gain offset (4)
1	13 E5	Data AM not found: Recovered with VFO Hi-gain offset (5)
1	13 E6	Data AM not found: Recovered with VFO Hi-gain offset (6)
1/3	14 01	No record found
1/3	14 80	Flag error
1/3	14 81	Drive fault with ATN off
1/3	14 82	Mismatch sector ID
1/3	14 83	Drive error with no factor
3	14 84	ID check code error at ID on-the-fly
3	14 91	Uncorrectable data error using previous sector ID
3	14 93	Data AM not found using previous sector ID
1	14 98	ECC correctable error using previous dector ID
3	14 A0	Reassign fault because of reserve sector NO REC
3	14 A1	Previous sector error with previous sector ID retry
3	14 B1	Error too many to recover using previous sector ID
1/3	14 C0	ID on-the-fly correction error
1/3	14 E1	No record found with VFO hi-gain offset (1)
1/3	14 E2	No record found with VFO hi-gain offset (2)
1/3	14 E3	No record found with VFO hi-gain offset (3)
1/3	14 E4	No record found with VFO hi-gain offset (4)
1/3	14 E5	No record found with VFO hi-gain offset (5)
1/3	14 E6	No record found with VFO hi-gain offset (6)
3	15 00	Seek positioning error (Not used)
1/3	15 01	Mechanical positioning error (Not used)
1/3	15 02	Positioning error detected by read of medium
1/3	16 00	Data synchronization mark error (Not used)
1	17 00	Recovered data with no error correction applied
1	17 01	Recovered data with retries
1	17 02	Recovered data with positive head offset
1	17 03	Recovered data with negative head offset
1	17 05	Recovered data using previous sector ID

*: The higher-order byte of the code indicate an additional sense code (byte 28), and the lower-order byte an additional sense code qualifier (byte 29).

Reference code of MP detected SIM for HRC/HODM (2/2)

Error		REF CODE 22	REF CODE 23	REF CODE 13	SIM 28	Level of error	Host report	Remarks
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	32	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	33	XX	FE	Service	No	XX: LDEV number
	MCU detected an Acute or Serious Level SIM for RCU.	DF	40	XX	FE	Serious	Yes	XX: LDEV number
	MCU detected a Moderate Level SIM for RCU.	DF	48	XX	FE	Moderate	Yes	XX: LDEV number

*1:Contents of byte37 when a temperature abnormality occured

Byte37	Error
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.

*2:Contents of byte37 when a voltage alarm was given

Byte37	Error
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.

*3:Contents of byte37 when a voltage warning was given

Byte37	Error
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow80%.

Reference code of MP detected SIM for HRC Semisynchronous

Error		REF CODE 22	23	13	SIM 28	Level of error	Host report	Remarks
Pair volume status error	HRC for this volume was suspended (Due to an unrecoverable failure on the remote copy connections.)	DE	00	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	DE	01	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Due to an unrecoverable failure on the R-VOL)	DE	02	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Caused by cache or DFW to the R-VOL was prohibited)	DE	05	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Due to an internal error condition detected by the RCU)	DE	06	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Caused by Delete pair operation was issued to the R-VOL)	DE	07	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC started the initial copy or out of sync for this volume.	DE	08	XX	FE	Service	Yes (*28)	XX: LDEV number
	HRC completed the initial copy for this volume.	DE	09	XX	FE	Service	Yes (*28)	XX: LDEV number
	MCU changed volume pair status. (Operation from an SVP/remote console or a host processor)	DE	0C	XX	FE	Service	No	XX: LDEV number
	Status of the M-VOL was not consistent with the R-VOL.	DE	0D	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was deleted. (Operation from an SVP/remote console or a host processor)	DE	0E	XX	FE	Service	Yes (*28)	XX: LDEV number
	Status of the R-VOL is changed.	DE	2Y	XX	FE	Service	Yes (*28)	XX: LDEV number Y: (note *26)
	RCU changed status of R-VOL to suspend. (Operation from an SVP/remote console or a host processor.)	DE	30	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from suspend to simplex. (Operation from an SVP/remote console or a host processor.)	DE	31	XX	FE	Service	No	XX: LDEV number
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	DE	32	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	DE	33	XX	FE	Service	No	XX: LDEV number

*1:Contents of byte37 when a temperature abnormality occured

Byte37	Error
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.

*2:Contents of byte37 when a voltage alarm was given

Byte37	Error
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.

*3:Contents of byte37 when a voltage warning was given

Byte37	Error
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow80%.

Byte36 : bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Error)

(Note 2) Additionel sense code + AdAdditional sense code qualifier (2/3)

Sense key	Code *	Meanning
1	17 06	Recovered data without ECC-data auto reallocated (Not used)
1	17 85	Recovered data with physical SCT pulse read
1	17 86	Auto rea. exhausted without ECC correction (Not used)
1	17 D6	Drive overrun occurred
1	17 E1	Recovered data with VFO hi-gain offset (1)
1	17 E2	Recovered data with VFO hi-gain offset (2)
1	17 E3	Recovered data with VFO hi-gain offset (3)
1	18 00	Recovered data with error correction applied
1	18 01	Recovered data with ECC and retries applied
1	18 02	Recovered data with ECC and/or retries data auto reallocated
1	18 80	Recovered data without retries or multi-symbol soft correction
1	18 81	Recovered data with retries and/or multi-symbol soft correction
1/3	19 02	Defect list error in primary list
1/3	19 03	Defect list error in grown list
5	1A 00	Parameter list length error (Not used)
1/3	1C 01	Primary defect list not found
1/3	1C 02	Grown defect list not found
E	1D 00	Miscompare during verify operation
5	20 00	Invalid command opration code
5	21 00	Logical blick address out of range
5	21 44	Logical Block Address out of Zone range
5	24 00	Illegal field in CDB
5	24 81	Odd byte data out request in wide transfer
5	25 00	Invalid LUN
5	26 00	Invalid field in parmament list
5	26 01	Prameter not supported
5	26 02	Parameter value invalid
5	26 03	Threshold pamamenters not suppoorted
5	26 80	Microprogram download error
7	27 00	Write protected
-	28 00	Not ready to ready transition (Not used)
6	29 00	Power on reset or bus device reset occured
6	2A 00	Paramenter changed (Not used)
6	2A 01	Mode parameters changed (Not used)
6	2A 02	Log parameters changed (Not used)
6	2F 00	Command cleared by another initiator (Not used)
3/4	31 00	Medium not present
3	31 01	Format command failed
1/4	32 00	No defect space allocation available
1/3	32 01	Defect list update failure
1	37 00	Rounded parameter
1	3D 00	Invalid bits in identify message
2	3E 00	Logical unit has not self-configured yet
4	3E 03	Can't found program with program loader
4	3E 04	Check SUM error with program loader
4	3E 05	Can't found end mark with program loader
6	3F 00	Target oprating conditions have changed (Not used)
6	3F 01	Microcode has been changed
6	3F 01	Microcode has been changed
6	3F 03	Inquiry data has changed

*: The higher-order byte of the code indicate an additional sense code(byte 28),and the lower-order byte an additional sense code qualifier(byte 29).

Byte36 : bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Error)

(Note 2) Additionel sense code + AdAdditional sense code qualifier (2/3)

Sense key	Code *	Meanning
1	17 06	Recovered data without ECC-data auto reallocated (Not used)
1	17 85	Recovered data with physical SCT pulse read
1	17 86	Auto rea. exhausted without ECC correction (Not used)
1	17 D6	Drive overrun occurred
1	17 E1	Recovered data with VFO hi-gain offset (1)
1	17 E2	Recovered data with VFO hi-gain offset (2)
1	17 E3	Recovered data with VFO hi-gain offset (3)
1	18 00	Recovered data with error correction applied
1	18 01	Recovered data with ECC and retries applied
1	18 02	Recovered data with ECC and/or retries data auto reallocated
1	18 80	Recovered data without retries or multi-symbol soft correction
1	18 81	Recovered data with retries and/or multi-symbol soft correction
1/3	19 02	Defect list error in primary list
1/3	19 03	Defect list error in grown list
5	1A 00	Parameter list length error (Not used)
1/3	1C 01	Primary defect list not found
1/3	1C 02	Grown defect list not found
E	1D 00	Miscompare during verify operation
5	20 00	Invalid command opration code
5	21 00	Logical blick address out of range
5	21 44	Logical Block Address out of Zone range
5	24 00	Illegal field in CDB
5	24 81	Odd byte data out request in wide transfer
5	25 00	Invalid LUN
5	26 00	Invalid field in parmament list
5	26 01	Prameter not supported
5	26 02	Parameter value invalid
5	26 03	Threshold pamamenters not suppoorted
5	26 80	Microprogram download error
7	27 00	Write protected
-	28 00	Not ready to ready transition (Not used)
6	29 00	Power on reset or bus device reset occured
6	2A 00	Paramenter changed (Not used)
6	2A 01	Mode parameters changed (Not used)
6	2A 02	Log parameters changed (Not used)
6	2F 00	Command cleared by another initiator (Not used)
3/4	31 00	Medium not present
3	31 01	Format command failed
1/4	32 00	No defect space allocation available
1/3	32 01	Defect list update failure
1	37 00	Rounded parameter
1	3D 00	Invalid bits in identify message
2	3E 00	Logical unit has not self-configured yet
4	3E 03	Can't found program with program loader
4	3E 04	Check SUM error with program loader
4	3E 05	Can't found end mark with program loader
6	3F 00	Target oprating conditions have changed (Not used)
6	3F 01	Microcode has been changed
6	3F 01	Microcode has been changed
6	3F 03	Inquiry data has changed

*: The higher-order byte of the code indicate an additional sense code(byte 28),and the lower-order byte an additional sense code qualifier(byte 29).

Byte36 : bit0-3 = E & Byte2C : bit0-7 ≠ 5X/6X (Drive Error)

(Note 2) Additionel sense code + AdAdditional sense code qualifier (3/3)

Sense key	Code *	Meanning
4	40 00	RAM failure
4	42 00	Power on or self test failure
4	42 80	Hard register error in send diag self test
B	43 00	Message error
4/B	44 00	Internal target error
4	44 80	Pin occured with forced write after
4	44 90	Management data read error
4	44 91	Multi track R/W error
4	44 97	Master data read error
4	44 98	Can't multi track write remain trackless
4	44 99	Multi track write error
4	44 9E	Master data write error
4	44 9F	Time out in CTL area access
4	44 A0	Internal target error (REA sector not found)
4	44 A1	Reassign data restore fail (Not used)
4	44 A2	Reassign sector ID not found (ID miscompare)
4	44 A3	No defect spare location available at skip rea
4	44 A4	ID string check error
4	44 A5	Reassign data save error
4	44 A6	Reassign write error
4	44 B0	HDC FIFO error (Check code error etc.)
4	44 B1	SCSI FIFO error (Check code error etc.)
4	44 C0	HDC DMAC error
4	44 C1	SCSI DMAC error
4	44 D0	HDC Sequencer setting mismatch
4	44 D1	HDC DMAC next condition full
4	44 D2	Offline ECC correction time out
4	44 D3	HDC time out
4	44 D4	HDC illegal stop
4	44 D5	STRD register error
4	44 D6	EERD register error
4	44 D7	ESDIERR register error
4	44 D8	ECSTR register error
4	44 D9	SST register error
4	44 DF	Error factor analysis error
4	44 F0	Spare head select error
4	44 F1	Invalid logical cylinder count
4	44 FF	Multi track R/W parameter error
B	45 00	Select/reselect failed
B	47 00	SCSI parity error
B	48 00	Initiator detected error message recieved
B	49 00	Invalid message error
B	4A 00	Command Phase error
B	4B 00	Data phase error
4	4C 00	Logical unit failed self configured
4	4C 80	RAM configuration load error
4	4E 00	Overlapped commands attempted (Not used)
1	5B 00	Log exception (Not used)
6	5B 01	Threshold condition met (Not used)
1	5B 02	Log counter at maximum (Not used)
1	5B 03	Log list codes exhausted (Not used)
4/6	5C 00	RPL status change (Not used)
6	5C 01	Spindles synchronized (Not used)
1/4/6	5C 02	Spindles not synchronized (Not used)
4	81 00	LA check error
1	AE 00	Spare sector less than threshold
3	C2 00	Reassign required error (Code = 11, 13, 14) occurred in ORM
3	C4 00	Reassign required error (Code = 11, 13, 14, 18) occurred in ORM

*: The thgher-order byte of the code indicate an additional sense code (byte 28),and the lower-order byte an additional sense code qualifier (byte 29).

Byte36:bit0-3 = E & Byte2C:bit0-7 ≠ 5X/6X (Drive Error)

(Note 4) Threshold type

Code	Meanning
00	CHA CHK1A failure
01	CHA CHK1B failure
02	CHA CHK3 failure
03	CHA CHK2 failure
04	CHA ADP temporary failure
05	LCM hardware error
06	BSA F bus open
07	BSA LIVEINS
08	BSA check error
09	SMP M bus open
0A	SMP M bus check error
0B	SMP H/L check error
10	DKA CHK1A failure
11	DKA CHK1B failure
12	DKA CHK3 failure
13	DKA SCA temporary failure
14	DKA DRR temporary failure
16	BSA F bus open
17	BSA LIVEINS
18	BSA check error
19	SMP M bus open
1A	SMP M bus check error
1B	SMP H/L check error
20	Shared memory correctable error
21	Shared memory uncorrectable error
22	SMC M bus open
23	SMC H/L bus open
30	Cache one bit correctable error
31	Cache uncorrectable error
32	Cache two bits correctable error
33	CPC check error
40	SCSI port failure
41	Drive recovered error (mechanism)
42	Drive unrecovered error (mechanism)
43	Drive recovered error (media)
44	Drive unrecovered error (media)
45	Drive recovered error (read/write)
46	Drive unrecovered error (read/write)
47	Drive interface recovered error
48	Drive interface unrecovered error
49	Controller recovered error
4A	Controller unrecovered error
4B	SCSI interface recovered error
4C	SCSI interface unrecovered error
4D	Drive I/O read error
4E	Drive I/O write error
60	SVP interface error
FF	Invalid threshold type

Byte36 = E0 & Byte2C = 5X/6X & Byte20 : b3 = 1 (LDEV blokckade/Pin VOL detected/Write inhibited) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used	Format (x'1')			
27	Type code (b'000')			Not used	Not used			
28	Ready	Enable	SSB pending	Not used				
29	Not used							
2A	M.M. RSV	PIN VOL	Write INH	Not used				
2B	Not used							
2C	Module ID (Note 1)							
2D	Routine ID (Note 1)							
2E	Not used							
2F	Drive serial number (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x'E000')							
37								
38	Log and message control (x'08')							
39	Program action code (x'92')							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Byte36 = E0 & Byte 2C = 5X/6X & Byte20 : b3 = 1 (LDEV blokckade/Pin VOL detected/Write inhibited) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
7F								

(Note 1) Module ID·Routine ID

x'5011/501C/5202' ; LDEV blockade
x'501A/501B' ; Pin VOL detected
x'6605/6697/6705/6784/6805/6853/6909/6953' ; Write inhibited

Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : b1 = 1 (Intervention requested : LDEV not ready) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x'06' : Cace DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used	Format (x'2')			
27	Type code (b'000')			Not used	Not used			
28	Ready	Enable	SSB PEND	0	0	0	0	0
29	x'00'							
2A	M.M RSV	PIN VOL	0	0	0	0	0	0
2B	Host type	DKC type	0	0		DKU type		
2C	Module ID¥Routine ID							
2D	(x'501C/5202' : LDEV not ready)							
2E	Command code							
2F	Drive serial number (x'0C') +							
30	(x'69') +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x'E210')							
37								
38	Log and message control (x'01')							
39	Program action code (x'02')							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : b1 = 1 (Intervention requested : LDEV not ready) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
7F								

Byte26 : b4-7 = F & Byte3C = F1 (DKC SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x'06' : Cache DKC)*							
23	Count (x'00')*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x'F')			
27	SIM sense record ID (x'E0')							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure SPs (Note 5)	SPs in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	'0000000'						
2B	Hardware level (Note 11)							
2C								
2D	Isoration code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number (x'0C') +							
30	(x'69') +							
31	(x'00') +							
	(DKC sequence number : high) +							
32	(DKC sequence number : low)*							
33								

* : This information is not fixed until DKC reports SIM to HOST.

Byte26 : b4-7 = F & Byte3C = F1 (DKC SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See "Reference code " table)								
37									
38	Log and message control (Note 15')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'F1')								
3D	Affected SSID*								
3E									
3F	Not used								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) Range subject to the error

x'0' : Not used
x'1' : Error range not known
x'2' : SP error
x'3' : CHL-I error
x'4' : Not affect performance
x'5~F' : Not used

(Note 3) Range affecte by repair

x'0' : Not used
x'1' : Repair range not known
x'2' : Repair dose not affect performance
x'3' : SP disabled during repair
x'4' : SSID disabled during repair
x'5~F' : Not used

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Failure SPs

0 : 1SP
1 : 2SP

(Note 6) SPs in SSID

0 : 2SP
1 : 4SP

(Note 7) Failure SSIDs

0 : 1SSID
1 : 2SSID

(Note 8) Affected SSIDs

0 : 1SSID
1 : 2SSID

(Note 9) Status

0 : Reduction
1 : Stop

(Note 10) Resent SIM

0 :Unresent SIM
1 : Resent SIM

Byte26 : b4-7 = F & Byte3C = F1 (DKC SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
00 : 4
01 : 8
10 : Not used
10 : Not used
11 : Not used
Bit 6 :NVS
0 : Without NVS
1 : With NVS

Bit 8-10 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MP
100 : 1024MB
101 : 1280MB
110 : 1536MB
111 : Over 1536MB
Bit 11-13 : Cluster hardware level ('000')
Bit 14-15 : Cache/NVS hardware level ('000')

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
0000 : Parallel=4, serial=0
0001 : Parallel=8, serial=0
0010 : Parallel=4, serial=2
0100 : Parallel=4, serial=4
0110 : Parallel=0, serial=2
1000 : Parallel=0, serial=4
1010 : Parallel=0, serial=8
1100 : Parallel=0, serial=6

Bit 8 : Dual frame
0 : Dual frame
1 : Single frame
Bir 9-11 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1024MB
101 : 1280MB
110 : 1536MB
111 : Over 1536MB
Bit 12-13 : Cluster hardware level ('00')
Bit 14-15 : Cache/NVS hardware level ('00')

(Note 12) Isolation code

Byte 2D ≠ x' 00' : Byte 36 and 37 are a sympton code.
Byte 2D = x' 00' : Byte 36 and 37 are a sympton code.
This byte is byte 2 of the isorarion code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don't log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

Byte26 : b4-7 = F & Byte3C = F2 (CACHE SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x'06' : Cache DKC)*							
23	Count (x'00')*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x'F')			
27	SIM sense record ID (x'E0')							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure Sps (Note 5)	Sps in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	'0000000'						
2B	Hardware level (Note 11)							
2C								
2D	Isoration code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number (x'0C') +							
30	(x'69') +							
31	(x'00') +							
	(DKC sequence number : high) +							
32	(DKC sequence number : low)*							
33								

* : This information is not fixed until DKC reports SIM to HOST.

Byte26 : b4-7 = F & Byte3C = F2 (CACHE SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See "Reference code" table)								
37									
38	Log and message control (Note 15')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'F1')								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) Range subject to the error

x'0' : Not used
x'1' : Error range not known
x'2' : SP error
x'3' : CHL-I error
x'4' : Not affect performance
x'5~F' : Not used

(Note 3) Range affecte by repair

x'0' : Not used
x'1' : Repair range not known
x'2' : Repair dose not affect performance
x'3' : SP disabled during repair
x'4' : SSID disabled during repair
x'5~F' : Not used

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Failure SPs

0 : 1SP
1 : 2SP

(Note 6) SPs in SSID

0 : 2SP
1 : 4SP

(Note 7) Failure SSIDs

0 : 1SSID
1 : 2SSID

(Note 8) Affected SSIDs

0 : 1SSID
1 : 2SSID

(Note 9) Status

0 : Reduction
1 : Stop

(Note 10) Resent SIM

0 :Unresent SIM
1 : Resent SIM

Byte26 : b4-7 = F & Byte3C = F2 (CACHE SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
00 : 4
01 : 8
10 : Not used
10 : Not used
11 : Not used
Bit 6 :NVS
0 : Without NVS
1 : With NVS

Bit 8-10 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MP
100 : 1024MB
101 : 1280MB
110 : 1536MB
111 : Over 1536MB
Bit 11-13 : Cluster hardware level ('000')
Bit 14-15 : Cache/NVS hardware level ('000')

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
0000 : Parallel = 4, serial = 0
0001 : Parallel = 8, serial = 0
0010 : Parallel = 4, serial = 2
0100 : Parallel = 4, serial = 4
0110 : Parallel = 0, serial = 2
1000 : Parallel = 0, serial = 4
1010 : Parallel = 0, serial = 8
1100 : Parallel = 0, serial = 6

Bit 8 : Dual frame
0 : Dual frame
1 : Single frame
Bir 9-11 : Cache size
000 : Non cache
001 : 256MB
010 : 512MB
011 : 768MB
100 : 1024MB
101 : 1280MB
110 : 1536MB
111 : Over 1536MB
Bit 12-13 : Cluster hardware level ('00')
Bit 14-15 : Cache/NVS hardware level ('00')

(Note 12) Isolation code

Byte 2D ≠ x'00' : Byte 36 and 37 are a sympton code.
Byte 2D = x'00' : Byte 36 and 37 are a sympton code.
This byte is byte 2 of the isorarion code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don't log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

Byte26 : b4-7 = F & Byte3C = FE (Device SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x'06' : Cache DKC)*							
23	Count (x'00')*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x'F')			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x'1')				Service message (x'1' : Action, x'C' : No action)			
29	Failure level (Note 4)		'000000'					
2A	Resent SIM (Note 5)	'0000000'						
2B	Exception class FRU list code (x'80')							
2C	Harware and microcode corequisite indicator (x'01')							
2D	Device address (See reference code)							
2E	Action flag (x'05')							
2F	Drive serial number* (x'0C') + (x'69') + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

Byte26 : b4-7 = F & Byte3C = FE (Device SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See "Reference code" table)								
37									
38	Log and message control (Note 6')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'FE')								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reported SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2)SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don't log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

Byte26 : b4-7 = F & Byte3C = FF (Media SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x'06' : Cache DKC)*							
23	Count (x'00')*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x'F')			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x'1')				Service message (x'1')			
29	Failure level (Note 4)	Media maintenance procedure number (Correctable : x'07', Uncorrectable : x'05')						
2A	Resend SIM (Note 5)	'0000000'						
2B	Exception class FRU list code (x'80')							
2C	Harware and microcode corequisite indicator (x'01')							
2D	Device address (See reference code)							
2E	Action flag (Correctable : x'87' . Uncorrectable : x'85')							
2F	Drive serial number* (x'0C') + (x'69') + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

Byte26 : b4-7 = F & Byte3C = FF (Media SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See "Reference code" table)								
37									
38	Log and message control (Note 6')*								
39	Program action code (x'10')*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Seial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x'FF')								
3D	Cylinder addres*								
3E									
3F	Head address*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don't log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

Reference code of MP detected SIM (1/3)

Error		REF CODE 36	37	2D	SIM 3C	Error level	Host report	Remarks
LCP/MCP Failure	CHA hardware error	21	3Z	XY	F1	Moderate	Yes	X:Processor number *18 Y,Z:LCP number 1,2 *3
	ADP permanent error	21	70	X0	F1	Moderate	Yes	X:Processor number *18
	ADP temporary error	21	71	XY	F1	Service	No	X:Processor number *18 Y:LCP number 1 *20
	ADP blockade	21	72	XY	F1	Moderate	Yes	X:Processor number *18 Y:LCP number 1 *20
Processor Failure	CHK1A threshold over	30	70	X0	F1	Service	No	X:Processor number *18
	CHK1B threshold over	30	71	X0	F1	Service	No	X:Processor number *18
	CHK3 threshold over	30	72	X0	F1	Service	No	X:Processor number *18
	Processor blockade	30	73	X0	F1	Moderate	Yes	X:Processor number *18
	FM threshold over	30	74	X0	F1	Service	No	X:Processor number *18
	FM error	30	75	X0	F1	Moderate	Yes	X:Processor number *18
	LDEV blockade (Effect of processor blockade)	30	90	X0	F1	Serious	Yes	X:Processor number
	P/S OFF impossible	38	8F	00	F1	Moderate	No	
	P/S OFF impossible (Device reserved)	38	9F	00	F1	Moderate	No	
	Undefined package is mounted	39	90	X0	F1	Moderate	No	X:Processor number *18
	V-R or serial number is inconsistent	39	91	X0	F1	Moderate	No	X:Processor number *18
	RAID5 booster is inconsistent	39	92	X0	F1	Serious	No	X:Processor number *18
	Replace failed	39	93	X0	F1	Moderate	No	X:Processor number
	Micro-program version up	39	94	X0	F1	Service	No	X:Processor number *18
	Micro-program version up impossible	39	95	XY	F1	Service	No	X:Processor number *18 Y:reason code *24
	Package type changed	39	96	XY	F1	Service	No	X:Processor number *18 Y:Change type number *25
M bus Failure	Warning of M bus open (SMC detected)	FF	D0	X0	F1	Moderate	No	X:0=Side A *19 1=Side B
	Warning of M bus open (SMP detected)	FF	D1	X0	F1	Moderate	No	X:Processor number *18
	Warning of CHK error (SMP detected)	FF	D2	X0	F1	Moderate	No	X:Processor number *18
	Abiter error	FF	E9	X0	F1	Service	No	X:Processor number *18
	Bus blockade	FF	EA	00	F1	Serious	Yes	
	CHK3 threshold over	FF	EB	00	F1	Service	No	
	Sequential mode only (Bus mode is unchanged)	FF	ED	00	F1	Service	No	

A three-byte reference code (RC) is provided for a SIM (Service Informaition Message) to identify an error and error section. The following shows 32 SIM bytes and reference code.

Byte	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
SIM SSB	00	90	10	00	00	00	8F	E0	44	10	00	04	00	80	04	0C	69	00	00	00	00	02	30	00	05	10	42	0C	F1	00	02	00

Indecates SIM

RS=3000-XXXX-80XX

SIM type
F1 : DKC SIM
F2 : CACHE SIM
FE : DEVICE SIM
FF : MEDIA SIM

Reference code of MP detected SIM (2/3)

Error		REF CODE 36	37	2D	SIM 3C	Error level	Host report	Remarks
F bus Failure (High/Low)	Warning of bus open (F-bus/L) (SMC detected)	FF	F6	X0	F1	Moderate	No	X:0=Side A *19 1=Side B
	Warning of CHK error (F-bus/L) (SMP detected)	FF	F7	X0	F1	Moderate	No	X:Processor number *18
	Abiter error	FF	F9	XY	F1	Service	No	X:Processor number *18 Y:0=Low 1=High
	Bus blockade	FF	FA	0X	F1	Serious	Yes	X:0=Low 1=High
	F bus (low) threshold over	FF	FB	00	F1	Service	No	
	Warning of F bus open (BSA detected)	FF	FC	YX	F1	Moderate	No	X:0=Low 1=High Y:Processor number *18
	Warning of LIVE INS (BSA detected)	FF	FD	YX	F1	Moderate	No	X:0=Low 1=High Y:Processor number *18
	Warning of CHK error (BSA detected)	FF	FE	YX	F1	Moderate	No	X:0=Low 1=High Y:Processor number *18
CHA CHK2 (Processor)	RCHA temporary error	3F	84	X0	F1	Service	No	X:Processor number *18
	RCHA blockade	3F	85	X0	F1	Serious	Yes	X:Processor number *18
CHS CHK2 (Processor)	SCP path temporary error	3F	86	XY	F1	Service	No	X:Processor number *18 Y:SCP number
	SCP path blockade	3F	87	XY	F1	Moderate	Yes	X:Processor number *18 Y:SCP number
DKA CHK2 (Processor)	PIN slot	CF	04	XX	F1	Moderate	No	XX:LDEV#
	DRR temporary error	CF	80	X0	F1	Service	No	X:Processor number *18
	SCA temporary error	CF	81	XY	F1	Service	No	X:Processor number *18 Y:Port # *21
	DRR blockade	CF	82	X0	F1	Moderate	Yes	X:Processor number *18
	SCA blockade (0~3)	CF	83	XY	F1	Moderate	Yes	X:Processor number *18 Y:Port # *21
	SCSI port blocking (Effect of PATH INLINE failed)	CF	84	XY	F1	moderate	No	X:Processor number *18 Y:Port # *21
	LDEV blockadE (Effect of SCA blockade)	CF	90	XY	F1	Serious	Yes	X:Processor number Y:Port #
Cache Failure	PIN slot	FF	04	XX	F2	Modetate	No	XX:LDEV#
	Area is volatiled	FF	CD	0X	F2	Service	No	X:0=Side A *19 1=Side B
	Package is volatiled	FF	CE	0X	F2	Service	No	X:Package number *19 Side A:Even, Side B:odd
	Module group is volatiled	FF	CF	YX	F2	Service	No	X:Package number *19 Side A:Even, Side B:odd Y:Module group number
	Correctable error 1 bit	FF	F0	YX	F2	Service	No	X:Package number *19 Side A:Even, Side B:odd Y:Module group number
	Correctable error 2 bits	FF	F8					
	Cache temporary error	FF	F1	YX	F2	Service	Yes	X:Package number *19 Side A:Even, Side B:odd Y:Module group number
	Module group blockade	FF	F2	YX	F2	Moderate	Yes	X:Package number *19 Side A:Even, Side B:odd Y:Module group number
	Package blockade	FF	F3	0X	F2	Moderate	Yes	X:Package number *19 Side A:Even, Side B:odd
	A/B side blockade	FF	F4	0X	F2	Serious	Yes	X:0=Side A 1=Side B *19
	Both side failure	FF	F5	0X	F2	Moderate	No	X:Package number *19 Side A:Even, Side B:odd
	Warning of CHK error (CPC detected)	FF	FF	0X	F2	Moderate	No	X:CPC number *23
Shared Memory Failure	Configuration check	FF	D3	XX	F1	Service	No	XX:Error code *27
	One side is volatiled	FF	DF	0X	F1	Service	No	X:0=Side A 1=Side B *19
	Correctable error	FF	E0	YX	F1	Service	No	X:0=Side A 1=Side B *19 Y:Module number
	Uncorrectable error	FF	E1	0X	F1	Service	Yes	X:0=Side A 1=Side B *19
	A/B side blockade	FF	E2	0X	F1	Serious	Yes	X:0=Side A 1=Side B *19

* : Warning end : (1) LDEV blockade status is detected, and copy process for the LDEV is skipped.
(2) Some failure is detected, and copy process is complete.

** : When the drive is 3380 emulation mode, the SIM is not reported to host.

Reference code of MP detected SIM (3/3)

Error		REF CODE 36	37	2D	SIM 3C	Error level	Host report	Remarks
Shared Memory Failure	Real memory size inconsistent	FF	E3	XY	F1	Serious	No	X:Number of module (side A) Y:Number of module (side B)
	Replace failed	FF	E4	0X	F1	Serious	No	X:0=Side A 1=Side B
	Both side invalid	FF	E5	00	F1	Acute	No	
	Configuration compare error	FF	E6	00	F1	Acute	No	
	Shared memory is volatiled	FF	E7	00	F1	Serious	No	
	Configuration number	FF	E8	00	F1	Acute	No	
	CHK3 threshold over	FF	EC	0X	F1	Service	No	X:0=Side A 1=Side B
	Area temporary blocking	FF	EE	0X	F1	Service	Yes	X:0=Side A 1=Side B
Drive Failure (Normal R/W)	SCSI temporaryerror	DF	7Y	XX	FE	Service	No	XX:CDEV# + RDEV# Y:Drive path number 0:Boundary0, 1:Boundary1
	Drive temporary error	EF	1A	XX	FE	Service	No	XX:CDEV# + RDEV#
	Drive media error	43	40	XX	FF	Service	No	XX:CDEV# + RDEV#
	SCSI blockade	DF	8Y	XX	FE	Moderate	Yes **	XX:CDEV# + RDEV# Y:Drive path number 0:Boundary0, 1:Boundary1
	LDEV blockade (Effect of SCSI blockade)	DF	9Y	XX	FE	Serious	Yes **	XX:Drive number (CDEV#:4b+RDEV#:4b) Y:Drive path 0:Boundary0, 1:Boundary1
	Drive blockade (Drive)	EF	10	XX	FE	Serious	Yes **	XX:CDEV# + RDEV#
	Drive blockade (Effect of Dynamic sparing normal end)	EF	11	XX	FE	Service	Yes **	XX:Drive number (CDEV#:4b+RDEV#:4b)
	LDEV blockade (Effect of drive blockade)	EF	90	XX	FE	Serious	Yes **	XX:Drive number (CDEV#:4b+RDEV#:4b)
	Drive blockade (Media)	43	CO	XX	FF	Serious	Yes **	XX:CDEV# + RDEV#
	Correction copy start	45	10	XX	FE	Service	Yes **	XX:CDEV# + RDEV#
	Correction copy normal end	45	20	XX	FE	Service	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Correction copyabnormal end	45	21	XX	FE	Serious	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Correction copy discontinued	45	22	XX	FE	Service	No	XX:CDEV# + RDEV# (Input side for copy)
	Corrction copy warning end (with blockade LDEV or some error)*	45	24	XX	FE	Service	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Dynamic sparing start (DRV copy)	46	10	XX	FE	Service	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Dynamic sparing normal end (DRV copy)	46	20	XX	FE	Service	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Dynamic sparing abnormal end (DRV copy)	46	21	XX	FE	Moderate	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	Dynamic sparing discotinued	46	22	XX	FE	Service	No	XX:CDEV# + RDEV# (Input side for copy)
	Dynamic sparing warning end (with blockade LDEV or some error)* (DRV copy)	46	24	XX	FE	Service	Yes **	XX:CDEV# + RDEV# (Input side for copy)
	PIN slot	EF	04	XX	FE	Moderate	No	XX:LDEV number
	LDEV read only status	EF	30	XX	FE	Serious	Yes **	XX:LDEV number
Drive Failure (ORM)	SCSI temporary error	50	0Y	XX	FE	Service	No	XX:CDEV# + RDEV# Y:Drive path number 0:Boundary0, 1:Boundary1
	Drive temporary error	50	10	XX	FE	Service	No	XX:CDEV# + RDEV#
	Drive media error	50	20	XX	FF	Service	No	XX:CDEV# + RDEV#
SVP I/F Failure	SVP ETHERNET error	14	00	X0	F1	Moderate	Yes	X:Processor number *18
Power Failure	HDU power off	AC	50	XY	F1	Service	No	X:DKU number *22 Y:HDU number *22
	HDU power recovered	AC	51	XY	F1	Service	No	X:DKU number *22 Y:HDU number *22

** : When the drive is 3380 emulation mode, the SIM is not reported to host.

Reference code of SVP detected SIM

Error		REF CODE 36	37	2D	SIM 3C	Error level	Host report	Remarks
Environment Abnormal (Note 1)	Temperature abnormal	BF	1X	XX *13	F1	Moderate	Yes	*1
	Voltage alarm	BF	2X	XX *13	F1	Moderate	Yes	*2
	Voltage warning	BF	3X	XX *13	F1	Moderate	Yes	*3
	P/S warning	BF	4X	XX *13	F1	Moderate	Yes	*4
	Battery warning	BF	5X	XX *13	F1	Moderate	Yes	*5
	AC warning	BF	6X	XX *13	F1	Moderate	Yes	*6
	Fan abnormality : CL1 logic	BF	7X	10	F1	Moderate	Yes	*7
	Fan abnormality : CL1 cache	BF	7X	11	F1	Moderate	Yes	*8
	Fan abnormality : CL2 logic	BF	7X	20	F1	Moderate	Yes	*7
	Fan abnormality : CL2 cache	BF	7X	21	F1	Moderate	Yes	*8
	Fan abnormality : HDU	BF	7X	3X~ 6X	F1	Moderate	Yes	*9
	JP remains	BF	8X	XX *13	F1	Moderate	Yes	*10
	Environment monitor error	BF	9X	XX *13	F1	Moderate	No	*11
	Environment monitor disagreement	BF	AX	XX *13	F1	Moderate	No	*12
SVP error	Logical inconsistency	70	XX	00	F1	Moderate	No	*14
	HEAP error	71	XX	00	F1	Moderate	No	*14
	File error	72	XX	00	F1	Moderate	No	*14
	LAN error	73	XX	00	F1	Moderate	No	*14
	S-SVP error	74	XX	XX *15	F1	Moderate	No	*15
	Windows error	75	XX	00	F1	Moderate	No	*14
	CUDG3 detected error	76	01	XX *16	F1	Moderate	No	
	LCDG3 detected error	76	10	XX *16	F1	Moderate	No	
	BOOT detected error	79	00	0X	F1	Moderate	No	X:Processor number
End status of remorte microprogram exchange	Normal end	7A	00	00	F1	Service	No	
	Abnormal end (SVP)	7A	01	00	F1	Service	No	
	Abnormal end (MP)	7A	02	0X	F1	Service	No	X:Processor number
	Version check error	7A	03	XX *17	F1	Service	No	X:Microprogram type
	Sum check error	7A	04	XX *17	F1	Service	No	X:Microprogram type
	LCP patch error	7A	05	0X	F1	Service	No	X:LCP#0
	Warning (Configuration inconsistency)	7A	10	00	F1	Service	No	
	Warning (S-SVP busy)	7A	11	00	F1	Service	No	
	Warning (LCP busy)	7A	12	0X	F1	Service	No	X:LCP#0
Dump received	WCHK1 dump	30	80	X0	F1	Moderate	No	X:Processor number
	ABEND dump	30	81	X0	F1	Moderate	No	X:Processor number

Reference code of MP detected SIM for HRC/HODM (1/2)

Error		REF CODE 22	REF CODE 23	REF CODE 13	SIM 28	Level of error	Host report	Remarks
RCP error	Logical path(s) on the remote copy connections was logically blocked (Due to an error conditions)	21	80	XY	F1	Moderate	Yes	X: Processor # (*19) Y: LCP# 1 (*20)
	The logical path has been recovered from blocked condition on the remote copy conditions.	21	81	XY	-F1	Service	Yes (*28)	X: Processor # (*19) Y: LCP# 1 (*20)
Pair volume status error	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the remote copy connections.)	DF	00	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	DF	01	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the R-VOL)	DF	02	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Caused by cache or DFW to the R-VOL was prohibited)	DF	05	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Due to an internal error condition detected by the RCU)	DF	06	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was suspended (Caused by Delete pair operation was issued to the R-VOL)	DF	07	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC started the initial copy or out of sync for this volume.	DF	08	XX	FE	Service	Yes (*28)	XX: LDEV number
	HRC completed the initial copy for this volume.	DF	09	XX	FE	Service	Yes (*28)	XX: LDEV number
	HODM started the migration copy or out of sync for this volume.	DF	0A	XX	FE	Service	Yes (*28)	XX: LDEV number
	HODM completed the migration copy for this volume.	DF	0B	XX	FE	Service	Yes (*28)	XX: LDEV number
	MCU changed volume pair status. (Operation from an SVP/remote console or a host processor)	DF	0C	XX	FE	Service	No	XX: LDEV number
	Status of the M-VOL was not consistent with the R-VOL.	DF	0D	XX	FE	Serious	Yes (*28)	XX: LDEV number
	HRC for this volume was deleted. (Operation from an SVP/remote console or a host processor)	DF	0E	XX	FE	Service	Yes (*28)	XX: LDEV number
	HODM for this volume was deleted. (Operation from an SVP/remote console)	DF	0F	XX	FE	Service	Yes (*28)	XX:LDEV number
	HODM started the erase operation for the R-VOL.	DF	18	XX	FE	Service	Yes (*28)	XX: LDEV number
	HODM completed the erase operation for the R-VOL.	DF	19	XX	FE	Service	Yes (*28)	XX: LDEV number
	Erase operation for this volume was not completed. (Due to anerror conditions)	DF	1A	XX	FE	Serious	Yes	XX: LDEV number
	Status of the R-VOL is changed.	DF	2Y	XX	FE	Service	Yes (*28)	XX: LDEV number Y: (note *26)
	RCU changed status of R-VOL to suspend. (Operation from an SVP/remote console or a host processor.)	DF	30	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from suspend to simplex. (Operation from an SVP/remote console or a host processor.)	DF	31	XX	FE	Service	No	XX: LDEV number

Reference code of MP detected SIM for HRC/HODM (2/2)

Error		REF CODE 22	23	13	SIM 28	Level of error	Host report	Remarks
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	32	XX	FE	Service	No	XX: LDEV number
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	DF	33	XX	FE	Service	No	XX: LDEV number
	MCU detected an Acute or Serious Level SIM for RCU.	DF	40	XX	FE	Serious	Yes	XX: LDEV number
	MCU detected a Moderate Level SIM for RCU.	DF	48	XX	FE	Moderate	Yes	XX: LDEV number

*1:Contents of byte37 when a temperature abnormality occured

Byte37	Error
10	Abnormal temperature in the unit of over 45°C is detected.
11	Abnormal temperature in the unit of over 60°C is detected.

*2:Contents of byte37 when a voltage alarm was given

Byte37	Error
20	5V voltage has dropped below 80%.
21	3.3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.

*3:Contents of byte37 when a voltage warning was given

Byte37	Error
30	Voltage for shared memory or cache memory or cache memory periphery has dropped bellow80%.

*4:Contents of byte37 when a P/S warning was given

Byte37	Error
40	5V PS 0 box abnormality has been detected.
41	5V PS 1 box abnormality has been detected.
42	5V PS 2 box abnormality has been detected.
43	3.3V PS 0 box abnormality has been detected.
44	3.3V PS 1 box abnormality has been detected.
45	Multi PS 0 box abnormality has been detected.
46	Multi PS 1 box abnormality has been detected.
47	HDD P/L Multi PS 1 box abnormality has been detected.
48	HDD P/L Multi PS 0 box abnormality has been detected.

*5:Contents of byte37 when a battery warning was given

Byte37	Error
50	Battery power for shared memory has dropped below 3.8V.
51	Battery power for cache memory has dropped below 3.8V.
52	Battery 0 power for cache memory has dropped below 3.8V.
53	Battery 1 power for cache memory has dropped below 3.8V.
54	Battery 2 power for cache memory has dropped below 3.8V.

*6:Contents of byte37 when an AC warning was given

Byte37	Error
60	AC power off/interruption of the breaker box occured.

*7:Contents of byte37 when an fan abnormality occurred (Logic)

Byte37	Error	
70	Low rotation speed of the FANX1 has been detected.	(X:Cluster#)
71	Low rotation speed of the FANX1 has been detected.	(X:Cluster#)
72	Low rotation speed of the FANX2 has been detected.	(X:Cluster#)
73	Low rotation speed of the FANX2 has been detected.	(X:Cluster#)
76	Low rotation speed of the FANX1 has been detected.	(X:Cluster#)
77	Low rotation speed of the FANX1 has been detected.	(X:Cluster#)
78	Low rotation speed of the FANX2 has been detected.	(X:Cluster#)
79	Low rotation speed of the FANX2 has been detected.	(X:Cluster#)

*8:Contents of byte 37 when a fan abnormality occurred (Cache)

Byte37	Error	
70	Low rotation speed of the FANCX1-ASSY has been detected.	(X:Cluster#)
71	Low rotation speed of the FANCX2-ASSY has been detected.	(X:Cluster#)
72	Low rotation speed of the FANCX3-ASSY has been detected.	(X:Cluster#)
73	Low rotation speed of the FANCX4-ASSY has been detected.	(X:Cluster#)

*9:Contents of byte 37 when a fan abnormality occurred (HDU)

Byte37	Error	
70	Low rotation speed of the FAN-XXX2-ASSY has been detected.	(FAN-XXX:the part shown in byte 13)
71	Low rotation speed of the FAN-XXX1-ASSY has been detected.	(FAN-XXX:the part shown in byte 13)
72	Low rotation speed of the FAN-XXX0-ASSY has been detected.	(FAN-XXX:the part shown in byte 13)

*10:Contents of byte 37 when JP remains

Byte37	Error
81	JP for LOGIC 1 remains.
82	JP for LOGIC 2 remains.
83	JP for CACHE 1 remains.
84	JP for CACHE 2 remains.
85	JP for HDU-XX0 ~ HDU-XX3 remains.
86	JP for HDU-XX4 ~ HDU-XX7 remains.

*11:Contents of byte37 when an environment monitor error occured

Byte37	Error
90	Environment mpnitor register access error.
91	Basic clock error of the environment monitor PCB occured.
92	Parity error of the environment monitor PCB occured.

*12:Contents of byte37 when an environment disagreement error occured

Byte37	Error
A0	An environment monitor disagreement error occured.
A1	An environment monitor disagreement error of power occurred.

*13:Contents of byte2D when an enviromental abnormality error occured

Byte2D	Error section	Byte2D	Error section	Byte2D	Error section
10	Logic 1	50	HDU-R20	74	DKUMN-R2F
11	Cache 1	51	HDU-R21	75	DKUMN-R2R
20	Logic 2	52	HDU-R22	76	DKUMN-L2F
21	Cache 2	53	HDU-R23	77	DKUMN-L2R
30	HDU-R10	54	HDU-R24	80	PWRCTL-1
31	HDU-R11	55	HDU-R25	81	PWRCTL-2
32	HDU-R12	56	HDU-R26	90	AC BOX-R10
33	HDU-R13	57	HDU-R27	91	AC BOX-R11
34	HDU-R14	60	HDU-L20		
35	HDU-R15	61	HDU-L21		
36	HDU-R16	62	HDU-L22		
37	HDU-R17	63	HDU-L23		
40	HDU-L10	64	HDU-L24		
41	HDU-L11	65	HDU-L25		
42	HDU-L12	66	HDU-L26		
43	HDU-L13	67	HDU-L27		
44	HDU-L14	70	DKUMN-R1F		
45	HDU-L15	71	DKUMN-R1R		
46	HDU-L16	72	DKUMN-L1F		
47	HDU-L17	73	DKUMN-L1R		

*14:Contents of byte37 and 2D when a logical error,a HEEP error,a file error, a LAN error or Windows error occured

Byte37	Byte2D	Error
00	00	Dump task
01	00	DKU inline
02	00	Microprogram change (online)
03	00	Information
04	00	LOGOUT
05	00	PATH inline
06	00	Back Ground
07	00	DIAG
08	00	Install
09	00	Online
0A	00	Microprogram change (offline)
0B	00	Special PCB maintenance
0C	00	Common comunication function
FF	00	Other AP

*15:Contents of byte37 and 2D when S-SVP logical error occured

Byte37:S-SVP error code (hegh byte)
Byte2D:S-SVP error code (low byte)

*16:Contents of byte byte 2D when a CUDG detection error occurred

Byte 2D (bit 0 - bit 3)	MPID
0000	CHP0
0001	CHP1
0010	CHP2
0011	CHP3
0100	CHP4
0101	CHP5
0110	CHP6
0111	CHP7
1000	DKP8
1001	DKP9
1010	DKPA
1011	DKPB
1100	DKPC
1101	DKPD
1110	DKPE
1111	DKPF

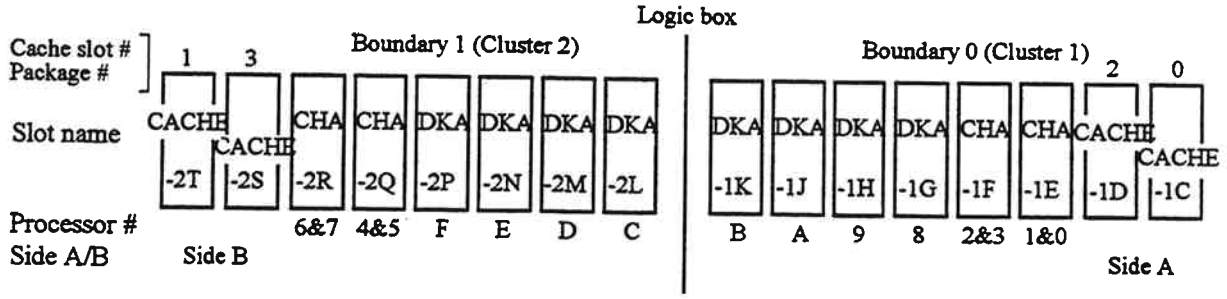
Byte 2D (bit 4 - bit 7)	Section
0001	CHP
0010	DKA
0011	CACHE+Shared Memory
0100	CACHE PORT+Shared Memory
0101	CACHE

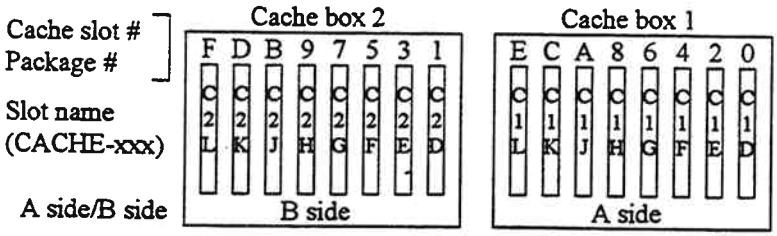
*17:Contents of byte2D when a version check error or sum check error occurred

Byte 2D	Microprogram type
00	RAM BOOT
01	DKC MAIN
02	LCP
03	MCP
04	LCDG
05	DKU
06	SVP
07	S-SVP

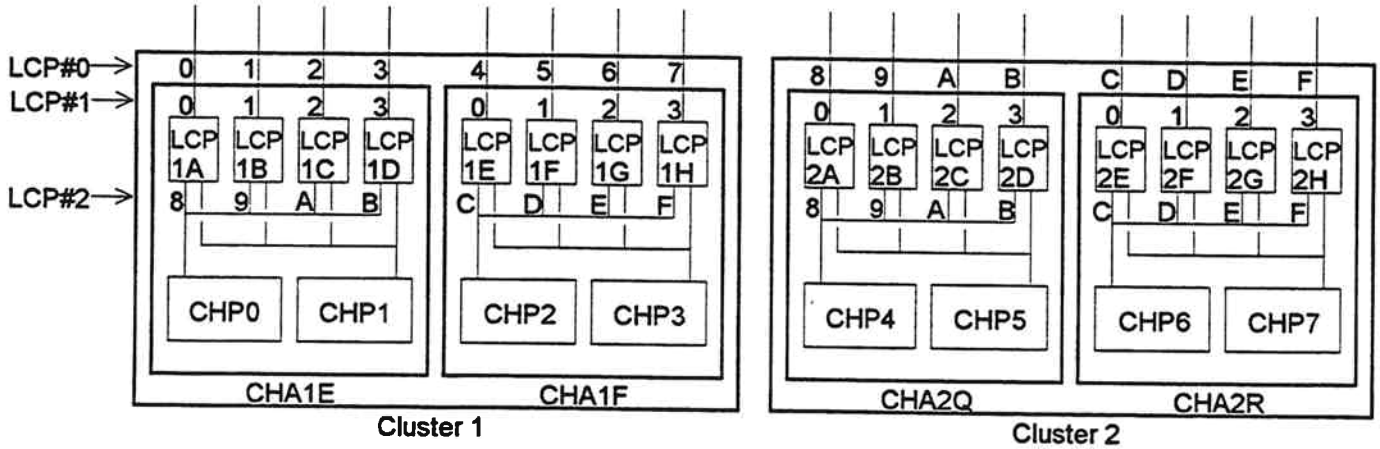
*18 Processor #: x'0' to x'F' indicates the processor number. See the figure below.

*19 Side A/B: Indicates the side of cache/shared memory. See the figure below.

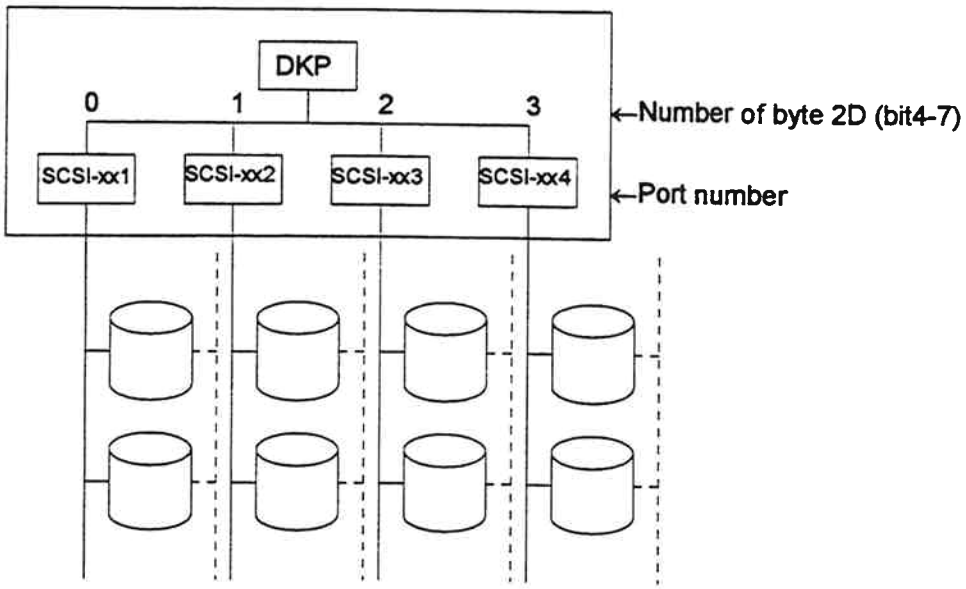




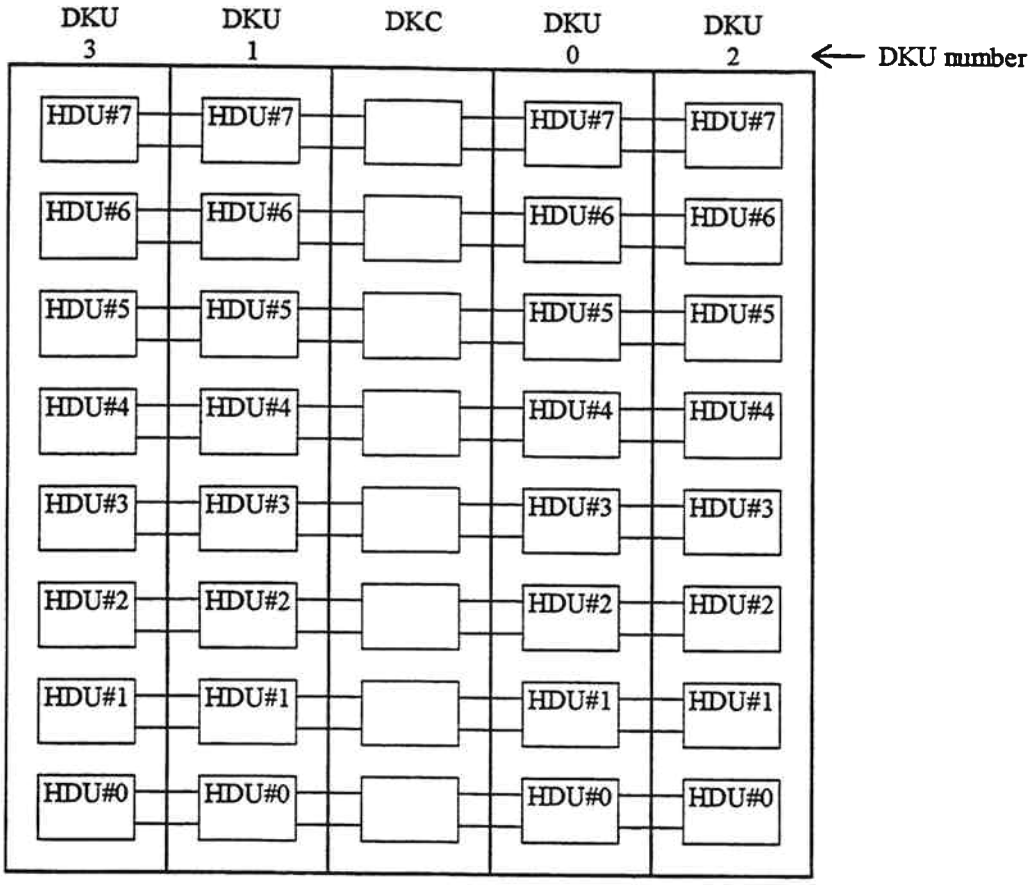
*20 LCP#0: x'0' to x'F' indicates the LCP number. See the figure below.
LCP#1: x'0' to x'3' indicates the LCP number. See the figure below.
LCP#2: x'8' to x'F' indicates the LCP number. See the figure below.



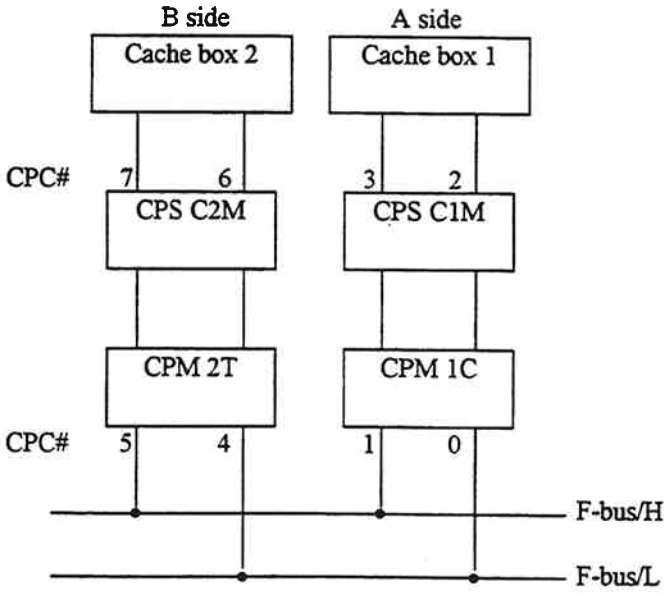
*21 Port #: x'0' to x'3' indicates the SCSI port number 1 to 4. See the figure below.



*22 DKU#: x'0' to x'3' indicates DKU number. See the figure below.
HDU#: x'0' to x'7' indicates HDU number. See the figure below.



*23 CPC#:x'0' to x'7' indicates the CPC number. See the figure below.



*24 reason code
x'0' : Pinned data exist
x'1' : The shutdown of the power supply was occurred
x'2' : Invalid Version/Revision exists

*25 Change type number
x'1' : From SRAM package to DRAM package
x'2' : From DRAM package to SRAM package
x'3' : From unmounted package to DRAM package

*26 Change pair status number
x'0': From simplex to duplex pending
x'1': From simplex to duplex
x'2': From pending duplex to duplex
x'3': From pending duplex to suspend
x'4': From duplex to suspend
x'5': From duplex to simplex
x'6': From pending duplex to simplex
x'7': From suspend to simplex
x'8': From suspend to duplex pending

*27 Error code
x'1' : DKA which controls DK308-90 is previous adapter.

*28 You can suppress reporting the HRC/HODM Service SIM to the HOST by RCU Option operation (PPRC support by HOST and Service SIM of HRC/HODM).

- Service level SIM -

PPRC support by HOST	Service SIM or HRC/HODM	level of error	HRC	HODM
Yes	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Not Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report
No	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report

- Moderate or Serious level SIM -

PPRC support by HOST	level of error	HRC	HODM
Yes	DKC_SIM & DEV_SIM (DF40/DF48)	Host Report	Host Report
	DEV_SIM (except DF40/DF48)	Not Host Report	Host Report
No	DKC_SIM & DEV_SIM (DF40/DF48)	Host Report	Host Report
	DEV_SIM (except DF40/DF48)	Host Report	Host Report