13. GLOSSARY SECTION

ACC (Action Code); Refer to the ACC section.

ADP (ADaPter); Hardware that connects the LCM to the CHA physically and logically. The ADP contains 256 MB of internal buffer.

AP; Short for Application Program.

BSA (BUS Adapter); Hardware that connects the PCBs, FBUS, and MBUS.

CACHE; Intermediate buffer between the channels and drives. CACHE has a maximum of 16 GB (8GB x 2 areas) of capacity. It is available and controlled as two areas of cache (cache A and cache B). It is fully battery-backed (48 hours).

CHA(CHannel Adapter); Provides the channel interface control functions and intercache data transfer functions. It is used to convert the data format between CKD and FBA. The CHA contains an internal processor and 128 bytes of edit buffer memory.

CHA (Prog.); Is a channel command control layer that processors channel commands and controls cache and data transfer operations. It is located in the CHA. CHA Prog is recognized by the logical volume number and logical block number.

CHA PCB (CHannel Adapter PaCkage Board); A PCB used to connect to the host processor. There are two types of CHA PCBs, one for optical channels and the other for metal channels. The CHA PCB for optical channels is provided with the LCM in its optical link control unit.

CM (Cache Memory); Refer to 'CACHE'.

CPM; Short for Cache Port Master. (Cluster for mounting the Cache Box (used for mounting more than 6GB of cache memory) package for connecting Cache Box.)

CPS; Short for Cache Port Slave. (Cluster for mounting the Cache Box (used for mounting more than 6GB of cache memory) package for connecting Cache Box.)

DKA (DisK Adapter); Provides the control functions for data transfer between drives and cache. The DKA contains DRR (Data Recover and Reconstruct) , a party generator circuit. It supports four SCSI buses and offers 64 KB of buffer for each SCSI bus. The DKA also has an internal processor.

DMA0; Controls the data transfer between the ADP and CACHE.

DMA1; Controls data transfer between the buffers in the DKA and CACHE.

DMA2; Controls data transfer between the buffers in the DKA and drives.

DMP (Disk Master Program); Is a RAID control layer and provides cache control, logical-to-physical address translation, and RAID control functions. DMP is located in the DKA. DMP is recognized by the logical volume number and logical blocked number.

DRIVE; Represents a SCSI drive whose internal data format is FBA (fixed length).

DSP (Disk Slave Program); Is a SCSI drive control layer and provides SCSI control, drive data transfer control, and parity control functions. It is located in the DKA . DSP is recognized by the physical volume number and LBA number.

ESC (Error Source Code); Refer to ACC section.

FBUS (Fast I/O BUS); Carries the data that is transferred between the adapter and cache. It is duplexed using two physical buses (H and L sides) each of which provides a data transfer rate of 200 MB per second. The L side bus is also used to access shared memory during interprocessor communication.

FM (Flush Memory); Each microprocessor has FM. FM is non-volatile memory which contains microcodes.

FPC (Failure Parts Code); Refer to the ACC section.

LCM (Link Control Module); Provides link control functions such as conversion of formats between optical and metal channel interfaces. The LCM contains an internal processor (LCP) and 2 KB of buffer memory.

LCP (Link Control Processor); Controls the optical links. LCP is identical to that which is used in the DKC90. LCP is located in the LCM.

LIVE INS; Short for Live Insertion, it is the signal cable for detecting hot-plugging.

LM (Local Memory); Each microprocessor has LM.

Main task; Consists of this subsystem control tasks (CHA Prog., DMP, DSP) and the SC kernel tasks that supervise the DKC control tasks. They switch the control tasks by making use of the SC kernel's task switching facility.

MBUS (Multi CPU BUS); Used to support interprocessor communication between the CHA Prog., DMPs, DSPs, and shared memory.

MFC (Main Failure Code); Refer to the ACC section.

RCHA; Short for RAID Channel Adapter, it is the name of a LSI in the CHA.

SBC (Sub BUS); A data bus in the DKA.

SCA (SCSI Adapter); Controls SCSI packets.

Shared memory; Stores the shared information about the subsystem and the cache control information (director names). This type of information is used for the exclusive control of the subsystem. Like CACHE , shared memory is controlled as two areas of memory and fully non-volatile (sustained for approximately 96 hours). The size of shared memory must be 16 MB for 1 GB of cache.

SM (Shared Memory); Refer to 'Shared memory'.

SPC (SCSI Protocol Controller); A SCSI initiator that controls the SCSI devices.

SVP Communication tasks; Controls the communication with the SVP.

Vx-Works; A basic OS for controlling the RISC processor. Its primary tasks are to control and switch between the main tasks and SVP communication tasks.