Byte27=8A (Disk Adapter CHK2) Byte28-31

(35) Byte28=B4:SCA#2 error & BSA#1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'B4':SCA#2 error & BSA#1 error							
29		SCA#0::SCHK2						
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A		SCA#0::BCHK2						
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B		SCA#0::CXM						
	(Not used)	Bus mode			Transfer mode 0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable				
2C		SCA#0::SCK20						
	AIN data parity error 0	AIN data parity error 1	AIN data parity error 2	AIN data parity error 3	BIN data parity error 0	BIN data parity error 1	BIN data parity error 2	BIN data parity error 3
2D		parity::SCK20						
	SCB write data parity error 0	SCB write data parity error 1	SCB write data parity error 2	SCB write data parity error 3	BSA write data parity error 0	BSA write data parity error 1	BSA write data parity error 2	BSA write data parity error 3
2E		BSA::BSASSB #02 (CHK2A information)						
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F		BSA::BSASSB #09 (CHK2B & CHK2C information)						
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30		BSA::BSASSB #10 (CHK2C information)						
	Request error	Control parity error	Transfer over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31		BSA::BSASSB #11 (CHK2D information)						
	LIVE INS	F bus open	Arbitration sequencer parity error	LI counter parity error	Arbitration timeout	Arbitration timer parity error	Request protocol error	(RSV)

Byte27=8A (Disk Adapter CHK2) Byte28-31

(36) Byte28=B8:SCA#2 error & BSA#0 error

	0	1	2	3	4	5	6	7
28	Subcode: x'B8':SCA#2 error & BSA#0 error							
29	SCA#0::SCHK2							
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A	SCA#0::BCHK2							
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B	SCA#0::CXM							
	(Not used)	Bus mode			Transfer mode 0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable				
2C	SCA#0::SCK20							
	AIN data parity error 0	AIN data parity error 1	AIN data parity error 2	AIN data parity error 3	BIN data parity error 0	BIN data parity error 1	BIN data parity error 2	BIN data parity error 3
2D	SCA#0::SCK20							
	SCB write data parity error 0	SCB write data parity error 1	SCB write data parity error 2	SCB write data parity error 3	BSA write data parity error 0	BSA write data parity error 1	BSA write data parity error 2	BSA write data parity error 3
2E	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F	BSA::BSASSB #09 (CHK2B & CHK2C information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	Arbitration sequencer parity error	LI counter parity error	Arbitration timeout	Arbitration timer parity error	Request protocol error	(RSV)

Byte27=8A (Disk Adapter CHK2) Byte28-31

(37) Byte28=BC:SCA#2 error & BSA#1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'BC':SCA#2 error & BSA#0 error & BSA#1 error							
29	SCA#0::SCHK2							
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A	SCA#0::BCHK2							
	BSA0 CHK2A/B	BSA0 CHK2C (control error)	BSA0 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B	SCA#0::BCHK2							
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2C	SCA#0::CXM							
	(Not used)	Bus mode			Transfer mode			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable	0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
2D	SCA#0::SCK21							
	BUS GRT ID PER ST	CMD ID PER 0 ST	CMD ID PER 1 ST	DCNT 0 parity error	DCNT 1 parity error	SPC write data parity error 0	SPC write data parity error 1	PKT DCNT parity error
2E	BSA::BSASSB #12 (CHK2 information)							
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
2F	BSA::BSASSB #13 (CHK2 information)							
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	Arbitration error	Arbitration timeout
30	BSA::BSASSB #12 (CHK2 information)							
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
31	BSA::BSASSB #13 (CHK2 information)							
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	Arbitration error	Arbitration timeout

Byte27=8A (Disk Adapter CHK2) Byte28-31

(38) Byte28=C4:SCA#3 error & BSA#1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'C4':SCA#3 error & BSA#1 error							
29		SCA#0::SCHK2						
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A		SCA#0::BCHK2						
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B		SCA#0::CXM						
	(Not used)	Bus mode			Transfer mode 0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
		Bus width 0: 8 1: 4B	BSA0 enable	BSA1 enable				
2C		SCA#0::SCK20						
	AIN data parity error 0	AIN data parity error 1	AIN data parity error 2	AIN data parity error 3	BIN data parity error 0	BIN data parity error 1	BIN data parity error 2	BIN data parity error 3
2D		parity::SCK20						
	SCB write data parity error 0	SCB write data parity error 1	SCB write data parity error 2	SCB write data parity error 3	BSA write data parity error 0	BSA write data parity error 1	BSA write data parity error 2	BSA write data parity error 3
2E		BSA::BSASSB #02 (CHK2A information)						
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F		BSA::BSASSB #09 (CHK2B & CHK2C information)						
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30		BSA::BSASSB #10 (CHK2C information)						
	Request error	Control parity error	Transfer over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31		BSA::BSASSB #11 (CHK2D information)						
	LIVE INS	F bus open	Arbitration sequencer parity error	LI counter parity error	Arbitration timeout	Arbitration timer parity error	Request protocol error	(RSV)

Byte27=8A (Disk Adapter CHK2) Byte28-31

(39) Byte28=C8:SCA#3 error & BSA#0 error

	0	1	2	3	4	5	6	7
28	Subcode: x'C8':SCA#3 error & BSA#0 error							
29	SCA#0::SCHK2							
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A	SCA#0::BCHK2							
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B	SCA#0::CXM							
	(Not used)	Bus mode			Transfer mode			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable	0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
2C	SCA#0::SCK20							
	AIN data parity error 0	AIN data parity error 1	AIN data parity error 2	AIN data parity error 3	BIN data parity error 0	BIN data parity error 1	BIN data parity error 2	BIN data parity error 3
2D	parity::SCK20							
	SCB write data parity error 0	SCB write data parity error 1	SCB write data parity error 2	SCB write data parity error 3	BSA write data parity error 0	BSA write data parity error 1	BSA write data parity error 2	BSA write data parity error 3
2E	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F	BSA::BSASSB #09 (CHK2B & CHK2C information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	Arbitration sequencer parity error	LI counter parity error	Arbitration timeout	Arbitration timer parity error	Request protocol error	(RSV)

Byte27=8A (Disk Adapter CHK2) Byte28-31

(40) Byte28=CC:SCA#3 error & BSA#0 error & BSA#1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'CC':SCA#3 error & BSA#0 error & BSA#1 error							
29	SCA#0::SCHK2							
	BSA data bus parity error	SPC data bus parity error	SCA data bus parity error	LA/LRC error	SCA hardware error	SBUS I/F error	MICRO access error	Not used
2A	SCA#0::BCHK2							
	BSA0 CHK2A/B	BSA0 CHK2C (control error)	BSA0 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2B	SCA#0::BCHK2							
	BSA1 CHK2A/B	BSA1 CHK2C (control error)	BSA1 CHK2D (arbiter error)	Not used	Not used	Not used	Not used	Not used
2C	SCA#0::CXM							
	(Not used)	Bus mode			Transfer mode 0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable				
2D	SCA#0::SCK21							
	BUS GRT ID PER ST	CMD ID PER 0 ST	CMD ID PER 1 ST	DCNT 0 parity error	DCNT 1 parity error	SPC write data parity error 0	SPC write data parity error 1	PKT DCNT parity error
2E	BSA::BSASSB #12 (CHK2 information)							
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
2F	BSA::BSASSB #13 (CHK2 information)							
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	Arbitration error	Arbitration timeout
30	BSA::BSASSB #12 (CHK2 information)							
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
31	BSA::BSASSB #13 (CHK2 information)							
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	Arbitration error	Arbitration timeout

Byte27=8A (Disk Adapter CHK2) Byte28-31

(41) Byte28=FX:SCA#n CHK2 without hardware cause

	0	1	2	3	4	5	6	7
28	Subcode: x'FX':SCA#n CHK2 without hardware error (n:SCA#:0,1,2,3)							
29		SCA#n::SCAINT						
	SCA data transfer end	SPC interruption	SCA CHK2	BSA0 CHK2	BSA1 CHK2	Not used	Not used	Not used
2A		SCA#n::XFC						
		DMA transfer force end bits						Not used
	Transfer mode 1 SPC→ CACHE	Transfer mode 2 CACHE→ SPC	Transfer mode 3 SCB→ CACHE	Transfer mode 4 CACHE→ SCB	Transfer mode 5 SPC→ SCB	Transfer mode 6 SCB→SCP	Transfer mode 7 CACHE→ CACHE	
2B		SCA#n::XFC						
		DMA transfer start bits						Not used
	Transfer mode 1 SPC→ CACHE	Transfer mode 2 CACHE→ SPC	Transfer mode 3 SCB→ CACHE	Transfer mode 4 CACHE→ SCB	Transfer mode 5 SPC→ SCB	Transfer mode 6 SCB→SCP	Transfer mode 7 CACHE→ CACHE	
2C		SCA#n::XFS0						
		DMA transfer executing bits						Not used
	Transfer mode 1 SPC→ CACHE	Transfer mode 2 CACHE→ SPC	Transfer mode 3 SCB→ CACHE	Transfer mode 4 CACHE→ SCB	Transfer mode 5 SPC→ SCB	Transfer mode 6 SCB→SCP	Transfer mode 7 CACHE→ CACHE	
2D		SCA#n::XFS1						
		DMA transfer normal end bits						Not used
	Transfer mode 1 SPC→ CACHE	Transfer mode 2 CACHE→ SPC	Transfer mode 3 SCB→ CACHE	Transfer mode 4 CACHE→ SCB	Transfer mode 5 SPC→ SCB	Transfer mode 6 SCB→SCP	Transfer mode 7 CACHE→ CACHE	
2E		SCA#n::XFS1						
		DMA transfer abnormal end bits						Not used
	Transfer mode 1 SPC→ CACHE	Transfer mode 2 CACHE→ SPC	Transfer mode 3 SCB→ CACHE	Transfer mode 4 CACHE→ SCB	Transfer mode 5 SPC→ SCB	Transfer mode 6 SCB→SCP	Transfer mode 7 CACHE→ CACHE	
2F	Cache package number (master)				Cache package number (Slave)			
30	Cache module group number (master)				Cache module group number (Slave)			
31		SCA#n::CXM						
	(Not used)	Bus mode			Transfer mode 0000 : Normal write 0001 : Normal read 001x : Cache to Cache 01xx : Double write/read 1000 : Broadcast write			
		Bus width 0: 8B 1: 4B	BSA0 enable	BSA1 enable				

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Byte27 = 8B (DRR CHK2) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x'8')				Message (x'B')			
28	Hardware information (See following pages)							
29								
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number				Message code (don't care)			
35	SSID (low) of self subsystem							
36	Symptom Code (x'FF8B' : LDEV type = DKU87I/x'EF8B' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27-8B (DRR CHK2) (2/5)

	0	1	2	3	4	5	6	7
40	Cache access P/K#							
	Slave 1 number				Slave 2 number			
41	MIC::RCVINT							
	SYSRST interruption	SELRST interruption	CHK1A interruption	CHK1B interruption	SMP interruption	LAN/SIO interruption	CHA/DRR interruption	ADP/SCA0 interruption
42	MIC::RCVINT							
	Not used	CHK3 interruption	Not used	SCA1 interruption	SCA2 interruption	SCA3 interruption	SCA4 interruption	SCA5 interruption
43	MIC::RCVINT							
	Timer 0 interruption	Timer 1 interruption	Timer 2 interruption	Timer 3 interruption	Timer 4 interruption	Timer 5 interruption	Timer 6 interruption	SYNC stop interruption
44	Reserved							
45	Reserved							
46	Reserved							
47	Reserved							
48	Reserved							
49	Reserved							
4A	DRR::STATS							
	Transfer end A	0	CMD A wait/execute	CMD A data transfer	Transfer end B	0	CMB B wait/execute	CMD B data transfer
4B	DRR::STATS							
	CHK2 typical bit	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Force transfer end	Pseudo failure
4C	DRR::ESTA0							
	Undefine register write error	Read only register write error	A REG write error (side A)	B REG write error (side B)	Address parity error	Byte access error	Input data parity error	Output data parity error
4D	DRR::ESTA0							
	Address decode error	Clock phase error	0	0	0	0	BSA0 CHK1	BSA1 CHK1
4E	DRR::ESTA1							
	Sequencer error							
	DRR→ BUFF	BUFF→ DRR	Data XFR in BUFF	BUFF control	Both side command	Multi PK transfer	Read in BSA	Write in BSA
4F	DRR::ESTA1							
	0	Transfer command set error	Total DT counter parity error	Packet DT counter parity error	RD packet counter parity error	WR packet counter parity error	BUFF WR ADR CNT parity error	BUFF RD ADR CNT parity error

Byte27-8B (DRR CHK2) (3/5)

	0	1	2	3	4	5	6	7
50	DRR::ESTA2							
	RD/WT PTR & SYNCO CNT PERR	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID, BUS G-ID parity error	Offset address parity error
51	DRR::ESTA2							
	Offset address overflow	LRC DT counter parity error	CMD parameter error (side A)	CMD parameter error (side B)	BSA0 CHK2C	BSA0 CHK2D	BSA1 CHK2C	BSA1 CHK2D
52	DRR::ESTA3							
	Data BUFF (TRI) parity error	Data BUFF (DMO) parity error	Data BUFF (DNO) parity error	Data BUFF (DMI) parity error	Data BUFF (DNI) parity error	ECC GEN MULTI 0 parity error	ECC GEN MULTI 1 parity error	ECC GEN ADDER 0 parity error
53	DRR::ESTA3							
	ECC GEN ADDER 1 parity error	ECC GEN ADDER 2 parity error	ECC GEN ADDER 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC CHK MULTI parity error	ECC CHK ADDER parity error
54	DRR::ESTA4							
	0	BSA input data parity error	BSA output data parity error	OFSET ADR ADDER parity error	Statistic counter parity error	BSA0 CHK2A	BSA1 CHK2	0
55	DRR::ESTA4							
	0	0	0	0	0	0	0	0
56	DRR::MODE2							
	CUDG mode	System clock mask	Pseudo failure setting	BSA Micro access	Subblock LRC CHK mask	DRB access mode	DRB ACC RD/WT select	Subblock data # variable
57	DRR::MODE2							
	DRB RD/WR ADR change	0	OUT SEL force change	Output selector change	Selector change signal in circuit			
58	DRR::MODE5							
	DRR parity inverse 0	DRR parity inverse 1	DRR parity inverse 2	DRR parity inverse 3	Sequencer forcible error	0/MD5PINV 05	0	0/CHK2A inhibit
59	DRR::MODE5							
	0/CHK2C inhibit	0/MD5EMS K11	0/MD5EMS K12	0/CHK2RST ON	0/CHK1B inhibit	0/DATAPER inhibit	0/DERR INH	0/SERR inhibit
5A	DRR::CSABM0							
	Arbiter sequencer bit 00	Arbiter sequencer bit 01	Arbiter sequencer bit 02	Arbiter sequencer bit 03	Arbiter sequencer bit 04	Arbiter sequencer bit 05	Arbiter sequencer bit 06	Arbiter sequencer bit 07
5B	DRR::CSABM0							
	Arbiter sequencer bit 10	Arbiter sequencer bit 11	Arbiter sequencer bit 12	Arbiter sequencer bit 13	Arbiter sequencer bit 14	Arbiter sequencer bit 15	Arbiter sequencer bit 16	0
5C	DRR::CMD0A							
	(RSV)	(RSV)	Packet LRC exist	Cache access exclusive	Special operation	(RSV)	(RSV)	(RSV)
5D	DRR::CMD0A							
	(RSV)	Bus mode	000 : Normal 010 : Reduction (H) 011 : Reduction (L)		(RSV)	(RSV)	(RSV)	(RSV)
5E	DRR::CMD0B							
	(RSV)	(RSV)	Packet LRC exist	Cache access exclusive	Special operation	(RSV)	(RSV)	(RSV)
5F	DRR::CMD0B							
	(RSV)	Bus mode	000 : Normal 010 : Reduction (H) 011 : Reduction (L)		(RSV)	(RSV)	(RSV)	(RSV)

Byte27=8B (DRR CHK2) (4/5)

	0	1	2	3	4	5	6	7
60	DRR::TRMDA							
	Syndrome verify	(RSV)	(RSV)	Double write	Transfer command			
61	DRR::TRMDA							
	Verify factor for 2 parity							
62	DRR::TRMDB							
	Syndrome verify	(RSV)	(RSV)	Double write	Transfer command			
63	DRR::TRMDB							
	Verify factor for 2 parity							
64	DRR::ADR0A							
	Cache package number of side A							
65	DRR::ADR0A							
	Cache package number of side A (Double access)							
66	DRR::ADR0B							
	Cache package number of side B							
67	DRR::ADR0B							
	Cache package number of side B (Double access)							
68	BSA#0::STATUS1							
	EXEC XFR in cache : CACHE RD	EXEC XFR in cache : CACHE WT	Arbiter master enable	Requester master enable	F bus (H) enable	F bus (L) enable	Transaction mode	F bus open set
69	BSA#0::ERR1							
	CHK1B typical bit	CHK2A typical bit	CHK2B typical bit	CHK2C typical bit	CHK2D typical bit	Not used	Not used	Not used
6A	BSA#0::MONITOR1							
	WR data transfer (Side A)	RD data transfer (Side A)	F bus DT transfer (Side A)	DBF-F bus transfer (Side A)	DBF-F bus transfer (Side B)	Not used	Not used	Not used
6B	BSA#0::MONITOR1							
	Command ID code (side A)			Command ID code (side B)			ABORT complete	Not used
6C	BSA#0::MONITOR2							
	PLRC ADD bit (side A)	F bus transfer bus mode (side A)			F bus transfer mode			
6D	BSA#0::MONITOR2							
	PLRC ADD bit (side B)	F bus transfer bus mode (side B)			F bus transfer mode			
6E	BSA#0::COPY							
	Slave busy signal	Cache RD transfer end	Cache WT transfer end	F bus ABT master in self section	F bus arbiter master	Not used	Not used	Not used
6F	BSA#0::CK2CST0							
	ADR/CMD parity error (side A)	ADR/CMD parity error (side B)	Invalid data (side A)	Invalid data (side B)	F bus access timeout	Not used	WCHK1 assert	F bus timer parity error

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Byte27=8B (DRR CHK2) (5/5)

	0	1	2	3	4	5	6	7
70	BSA#0::CK2CST0							
	Not used	Request sequencer parity error	Request counter parity error	MY GRANT parity error	Arbitration count over	DBF ADR/CMD parity error	CHA invalid read	Upper bus mode parity error
71	BSA#0::CK2CST1							
	WRS SEQ CNT/PTR parity error	Not used	WR1 sequencer parity error	WR1 SEQ CNT/PTR parity error	Not used	WR2 SEQ sequencer parity error	WR2 SEQ CNT/PTR parity error	Not used
72	BSA#0::CK2CST1							
	WR3 sequencer parity errro	WR3 SEQ CNT/PTR parity error	DBF ADR CNT PTYER (side A)	DBF ADR CNT PTYER (side B)	Transfer count over	Not used	CMD REG A/ST1 REG unmatch	CMD REG B/ST1 REG unmatch
73	BSA#0::CK2BST0							
	HDB1 data parity error	HDB3 data parity error	HDB2 data parity error	HDB4 data parity error	LRC GEN data parity error	Not used	Not used	Not used
74	BSA#0::STATUS1							
	EXEC XFR in cache : CACHE RD	EXEC XFR in cache : CACHE WT	Arbiter master enable	Requester master enable	F bus (H) enable	F bus (L) enable	Transaction mode	F bus open set
75	BSA#0::ERR1							
	CHK1B typical bit	CHK2A typical bit	CHK2B typical bit	CHK2C typical bit	CHK2D typical bit	Not used	Not used	Not used
76	BSA#0::MONOTOR1							
	WR data transfer (Side A)	RD data transfer (Side A)	F bus DT transfer (Side A)	DBF-F bus transfer (Side A)	DBF-F bus transfer (Side B)	Not used	Not used	Not used
77	BSA#0::MONITOR1							
	Command ID code (side A)			Command ID code (side B)			ABORT complete	Not used
78	BSA#0::MONITOR2							
	PLRC ADD bit (side A)	F bus transfer bus mode (side A)			F bus transfer mode			
79	BSA#1::MONITOR2							
	PLRC ADD bit (side B)	F bus transfer bus mode (side B)			F bus transfer mode			
7A	BSA#1::COPY							
	Slave busy signal	Cache RD transfer end	Cache WT transfer end	F bus ABT master in self section	F bus arbiter master	Not used	Not used	Not used
7B	BSA#1::CK2CST0							
	ADR/CMD parity error (side A)	ADR/CMD parity error (side B)	Invalid data (side A)	Invalid data (side B)	F bus access timeout	Not used	WCHK1 assert	F bus timer parity error
7C	BSA#1::CK2CST0							
	Not used	Request sequencer parity error	Request counter parity error	MY GRANT parity error	Arbit count over	DBF ADR/CMD parity error	CHA invalid read	Upper bus mode parity error
7D	BSA#1::CK2CST1							
	WRS SEQ CNT/PTR parity error	Not used	WR1 sequencer parity error	WR1 SEQ CNT/PTR parity error	Not used	WR2 SEQ sequencer parity error	WR2 SEQ CNT/PTR parity error	Not used
7E	BSA#1::CK2CST1							
	WR3 sequencer parity error	WR3 SEQ CNT/PTR parity error	DBF ADR CNT PTYER (side A)	DBF ADR CNT PTYER (side B)	Transfer count over	Not used	CMD REG A/ST1 REG unmatch	CMD REG B/ST1 REG unmatch
7F	BSA#0::CK2BST0							
	HDB1 data parity error	HDB3 data parity error	HDB2 data parity error	HDB4 data parity error	LRC GEN data parity error	Not used	Not used	Not used

Byte27=8B (DRR CHK2) Byte28-31 Detail

(1) Byte28=10:DRR data error

	0	1	2	3	4	5	6	7
28	Subcode: x'10':DRR data error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA3						
	Data BUF (TRI) parity error	Data BUF (DMO) parity error	Data BUF (DNO) parity error	Data BUF (DMI) parity error	Data BUF (DNI) parity error	ECC GEN multipl 0 parity error	ECC GEN multipl 1 parity error	ECC GEN adder 0 parity error
2C		DRR::EST3						
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	write data parity error	LRC error	LRC CHK multipl parity error	LRC CHK adder parity error
2D		DRR::ESTA4						
	(RSV)	BSA in data parity error	BSA out data parity error	Offset address parity error	Statistic counter parity error	SA0 CHK2A error	BSA1 CHK2A error	(RSV)
2E		DDR::CMD0A						
		Slave 1 transfer command (REG A)						
2F		DRR::TMRDA						
	Verify ON	(RSV)	(RSV)	Double write	Command (Note1)			
30		DDR::CMD0B						
		Slave 1 transfer command (REG B)						
31		DRR::TMRDB						
	Verify ON	(RSV)	(RSV)	Double write	Command (Note1)			

(Note1) 0010 : Dm RD XFR (without intermediate result)
0011 : Dm RD XFR (with intermediate result)
0100 : Dn RD XFR (without intermediate result)
0101 : Dn RD XFR (with intermediate result)
0110 : Dm & Dn RD XFR (without intermediate result)
0111 : Dm & Dn RD XFR (with intermediate result)
1000 : RD XFR (with old Dm)
1001 : RD XFR (with old Dn)
1010 : Syndrome (without intermediate result)
1011 : Syndrome (with intermediate result)
1100 : WR XFR Dm
1101 : WR XFR Dn
1110 : Copy between caches

Byte27=8B (DRR CHK2) Byte28-31 Detail

(2) Byte28=11:DRR control error

	0	1	2	3	4	5	6	7
28	Subcode: x'11':DRR control error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA1						
	Sequencer error (DRR-BUF)	Sequencer error (BUF-DRR)	Sequencer error (INT XFR)	Sequencer error (buffer)	Sequencer error (command)	Sequencer error (XFR)	Sequencer error (BSA RD)	Sequencer error (BSA WR)
2C		DRR::ESTA1						
	(RSV)	Transfer command error	Total data counter parity error	Packet data counter parity error	Read packet counter parity error	Write packet counter parity error	BUF write address counter parity error	BUF read address counter parity error
2D		DRR::ESTA2						
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2E		DDR::ESTA2						
	Offset address overflow	LRC data counter parity error	Side-A command parameter error	Side-B command parameter error	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2F		DDR::CMD0A						
		Slave 1 transfer command (READ A)						
30		DRR::TMRDA						
	Verify ON	(RSV)	(RSV)	Double write	Command (Note1)			
31		DRR::TMRDB						
	Verify ON	(RSV)	(RSV)	Double write	Command (Note1)			

(Note1) 0010 : Dm RD XFR (without intermediate result)
0011 : Dm RD XFR (with intermediate result)
0100 : Dn RD XFR (without intermediate result)
0101 : Dn RD XFR (with intermediate result)
0110 : Dm & Dn RD XFR (without intermediate result)
0111 : Dm & Dn RD XFR (with intermediate result)
1000 : RD XFR (with old Dm)
1001 : RD XFR (with old Dn)
1010 : Syndrome (without intermediate result)
1011 : Syndrome (with intermediate result)
1100 : WR XFR Dm
1101 : WR XFR Dn
1110 : Copy between caches

Byte27=8B (DRR CHK2) Byte28-31 Detail

(3) Byte28=12:DRR data error & control error

	0	1	2	3	4	5	6	7
28	Subcode: x'12':DRR data error & control error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer error terminate	Pseudo-failure occurred
2B		DRR::ESTA1						
	Sequencer error (DRR-BUF)	Sequencer error (BUF-DRR)	Sequencer error (INT XFR)	Sequencer error (buffer)	Sequencer error (command)	Sequencer error (XFR)	Sequencer error (BSA RD)	Sequencer error (BSA WR)
2C		DRR::ESTA1						
	(RSV)	Transfer setting error	Total data counter parity error	Packet data counter parity error	Read packet counter parity error	Write packet counter parity error	BUF write address counter parity error	BUF read address counter parity error
2D		DRR::ESTA2						
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2E		DRR::ESTA2						
	Offset address overflow	LRC data counter parity error	Side-A command parameter error	Side-B command parameter error	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2F		DRR::ESTA3						
	Data BUF (TRI) parity error	Data BUF (DMO) parity error	Data BUF (DNO) parity error	Data BUF (DMI) parity error	Data BUF (DNI) parity error	ECC GEN multipl 0 parity error	ECC GEN multipl 1 parity error	ECC GEN adder 0 parity error
30		DRR::ESTA3						
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC CHK multipl parity error	LRC CHK adder parity error
31		DRR::ESTA4						
	(RSV)	BSA in data parity error	BSA out data parity error	Offset address adder parity error	Statistic counter parity error	SA0 CHK2A error	BSA1 CHK2A error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(4) Byte28=13:DRR error without cause

	0	1	2	3	4	5	6	7
28	Subcode: x'13':DRR error without cause							
29	DRR::STATS							
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A	DRR::STATS							
	CHK2 typical	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer error terminate	Pseudo-failure occurred
2B	DRR::MODE2							
	CUDG mode switching	System clock mask	Pseudo-failure setting	BSA micro access request	Sub-block LRC check masking	DRB access mode	Write register selection	Number of data changeable
2C	DRR::ESTA1							
	(RSV)	Transfer setting error	Total data counter parity error	Packet data counter parity error	Read packet counter parity error	Write packet counter parity error	BUF write address counter parity error	BUF read address counter parity error
2D	DRR::ESTA2							
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2E	DRR::ESTA2							
	Offset address overflow	LRC data counter parity error	Side-A command parameter error	Side-B command parameter error	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2F	DRR::ESTA3							
	Data BUF (TRI) parity error	Data BUF (DMO) parity error	Data BUF (DNO) parity error	Data BUF (DMI) parity error	Data BUF (DNI) parity error	ECC GEN multipl 0 parity error	ECC GEN multipl 1 parity error	ECC GEN adder 0 parity error
30	DRR::ESTA3							
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC CHK multipl parity error	LRC CHK adder parity error
31	DRR::ESTA4							
	(RSV)	BSA in data parity error	BSA out data parity error	Offset address adder parity error	Statistic counter parity error	SA0 CHK2A error	BSA1 CHK2A error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(5) Byte28=20:BSA0 error

	0	1	2	3	4	5	6	7
28	Subcode: x'20':BSA0 error							
29	BSA::BSASSB #00 (CHK2A information)							
	CHK error	Last cycle error	Slave1 parity error	Slave 2 parity error	Slave ID error	F bus RD data error	F bus RD P-LRC error	FDB parity error
2A	BSA::BSASSB #01 (CHK2A information)							
	Slave1 error	Slave1 warning	Slave2 error	Slave2 warning	(RSV)	(RSV)	(RSV)	(RSV)
2B	BSA::BSASSB #03 (CHK2B information)							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	HDB 1/2 data parity error	HDB 3/4 data parity error	(RSV)
2C	BSA::BSASSB #04 (CHK2C information)							
	Side-A parity error	Side-B parity error	Side-A invalid error	Side-B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity error
2D	BSA::BSASSB #05 (CHK2C information)							
	(RSV)	Request sequencer parity error	Request counter/ pointer parity error	MYGRANT parity error	ABT count over	DBF access parity error	CHA invalid read	Bus mode error
2E	BSA::BSASSB #06 (CHK2C information)							
	WRS counter/ pointer parity error	WR1 sequence error	WR1 counter/ pointer parity error	WR2 sequence error	WR2 counter/ pointer parity error	WR3 sequence error	WR3 counter/ pointer parity error	DBF address count (A) parity error
2F	BSA::BSASSB #07 (CHK2C information)							
	DBF address count (B) parity error	Transfer count over	CMD/ST A inconsistent	CMD/ST B inconsistent	RD1 sequence error	RD1 counter/ pointer parity error	RD2 sequence error	RD2 counter/ pointer parity error
30	BSA::BSASSB #08 (CHK2C information)							
	HDB parity error	LRC GEN parity error	access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(6) Byte28=21:BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'21':BSA1 error							
29	BSA::BSASSB #00 (CHK2A information)							
	CHK error	Last cycle error	Slave1 parity error	Slave2 parity error	Slave ID error	F bus RD data error	F bus RD P-LRC error	FDB parity error
2A	BSA::BSASSB #01 (CHK2A information)							
	Slave1 error	Slave1 warning	Slave2 error	Slave2 warning	(RSV)	(RSV)	(RSV)	(RSV)
2B	BSA::BSASSB #03 (CHK2B information)							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	HDB 1/2 data parity error	HDB 3/4 data parity error	(RSV)
2C	BSA::BSASSB #04 (CHK2C information)							
	Side-A parity error	Side-B parity error	Side-A invalid error	Side-B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity error
2D	BSA::BSASSB #05 (CHK2C information)							
	(RSV)	Request sequencer parity error	Request counter/ pointer parity error	MYGRANT parity error	ABT count over	DBF access parity error	CHA invalid read	Bus mode error
2E	BSA::BSASSB #06 (CHK2C information)							
	WRS counter/ pointer parity error	WR1 sequence error	WR1 counter/ pointer parity error	WR2 sequence error	WR2 counter/ pointer parity error	WR3 sequence error	WR3 counter/ pointer parity error	DBF address count (A) parity error
2F	BSA::BSASSB #07 (CHK2C information)							
	DBF address count (B) parity error	Transfer count over	CMD/ST A inconsistent	CMD/ST B inconsistent	RD1 sequence error	RD1 counter/ pointer parity error	RD2 sequence error	RD2 counter/ pointer parity error
30	BSA::BSASSB #08 (CHK2C information)							
	HDB parity error	LRC GEN parity error	access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

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Byte27=8B (DRR CHK2) Byte28-31 Detail

(7) Byte28=22:BSA0 & BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'22': BSA0 & BSA1 error							
29	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2A	BSA::BSASSB #09 (CHK2B & CHK2D information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
2B	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
2C	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)
2D	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2E	BSA::BSASSB #09 (CHK2B & CHK2D information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
2F	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
30	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)
31	DRR::STATS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred

Byte27=8B (DRR CHK2) Byte28-31 Detail

(8) Byte28=34:DRR data error & BSA0 error

	0	1	2	3	4	5	6	7
28	Subcode: x'34': DRR data error & BSA0 error							
29	DRR::STATS							
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A	DRR::STATS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B	DRR::ESTA3							
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC check multiple parity error	LRC check adder parity error
2C	DRR::ESTA4							
	(RSV)	BSA input data parity error	BSA output data parity error	Offset address adder parity error	Statistic counter parity error	BSA0 CHK2A error	BSA1 CHK2A error	(RSV)
2D	BSA0::ERR							
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F	BSA::BSASSB #09 (CHK2B & CHK2D information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(9) Byte28=35:DRR control error & BSA0 error

	0	1	2	3	4	5	6	7
28	Subcode: x'35': DRR control error & BSA0 error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA2						
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2C		DRR::ESTA2						
	Offset address overflow	LRC data counter parity error	Side-A command parameter error	Side-B command parameter error	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2D		BSA0::ERR						
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E		BSA::BSASSB #02 (CHK2A information)						
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F		BSA::BSASSB #09 (CHK2B & CHK2D information)						
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30		BSA::BSASSB #10 (CHK2C information)						
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31		BSA::BSASSB #11 (CHK2D information)						
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(10) Byte28=38:DRR data error & BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'38': DRR data error & BSA1 error							
29	DRR::STATS							
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A	DRR::STATS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B	DRR::ESTA3							
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC check multiple parity error	LRC check adder parity error
2C	DRR::ESTA4							
	(RSV)	BSA input data parity error	BSA output data parity error	Offset address adder parity error	Statistic counter parity error	BSA0 CHK2A error	BSA1 CHK2A error	(RSV)
2D	BSA0::ERR							
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E	BSA::BSASSB #02 (CHK2A information)							
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave 1 error	Slave 2 error
2F	BSA::BSASSB #09 (CHK2B & CHK2D information)							
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30	BSA::BSASSB #10 (CHK2C information)							
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31	BSA::BSASSB #11 (CHK2D information)							
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(11) Byte28=39:DRR control error & BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'39': DRR control error & BSA1 error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA2						
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2C		DRR::ESTA2						
	Offset address overflow	LRC data counter parity error	Side-A command parameter error	Side-B command parameter error	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2D		BSA0::ERR						
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E		BSA::BSASSB #02 (CHK2A information)						
	CHK error	Last cycle error	Error phase parity error	Slave ID error	F bus read data error	FDB parity error	Slave1 error	Slave2 error
2F		BSA::BSASSB #09 (CHK2B & CHK2D information)						
	HDB parity error	LRC GEN parity error	Access parity error	Invalid command	F bus timeout	WCHK1 assert	F bus timer parity error	Request sequence error
30		BSA::BSASSB #10 (CHK2C information)						
	Request error	Control parity error	Transfer count over	DBF address counter parity error	WRS/WR1 parity error	WR2/WR3 parity error	RD1/RD2 parity error	RD3/RD4 parity error
31		BSA::BSASSB #11 (CHK2D information)						
	LIVE INS	F bus open	ABT sequencer parity error	LI counter parity error	ABT timeout	ABT timer parity error	Request protocol error	(RSV)

Byte27=8B (DRR CHK2) Byte28-31 Detail

(12) Byte28=3C:DRR data error & BSA0 error & BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'3C': DRR data error & BSA0 error & BSA1 error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA3						
	ECC GEN adder 1 parity error	ECC GEN adder 2 parity error	ECC GEN adder 3 parity error	Syndrome (ECC) error	Write data parity error	LRC error	LRC check multiple parity error	LRC check adder parity error
2C		DRR::ESTA4						
	(RSV)	BSA input data parity error	BSA output data parity error	Offset address adder	Statistic counter parity error	BSA0 CHK2A error	BSA1 CHK2A error	(RSV)
2D		BSA0::ERR						
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E		BSA::BSASSB #12 (CHK2 information)						
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
2F		BSA::BSASSB #13 (CHK2 information)						
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	ABT error	ABT timeout
30		BSA::BSASSB #12 (CHK2 information)						
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
31		BSA::BSASSB #13 (CHK2 information)						
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	ABT error	ABT timeout

Byte27=8B (DRR CHK2) Byte28-31 Detail

(13) Byte28=3D:DRR control error & BSA0 error & BSA1 error

	0	1	2	3	4	5	6	7
28	Subcode: x'3D': DRR control error & BSA0 error & BSA1 error							
29		DRR::STATS						
	XFR END A	(RSV)	CMD A execute	CMD A data transfer	XFR END B	(RSV)	CMD B execute	CMD B data transfer
2A		DRR::STATS						
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2B		DRR::ESTA2						
	RD/WT PTR & SYNC CNT parity error	SYNC IN pointer parity error	DIF counter parity error	SBL counter parity error	PL counter parity error	MODE output parity error	CMD ID & BUS G ID parity error	Offset address parity eror
2C		DRR::ESTA2						
	Offset address overflow	LRC data counter parity error	Side-A command parameter	Side-B command parameter	BSA0 CHK2C error	BSA0 CHK2D error	BSA1 CHK2C error	BSA1 CHK2D error
2D		BSA0::ERR						
	Typical CHK1B error	Typical CHK2A error	Typical CHK2B error	Typical CHK2C error	Typical CHK2D error			
2E		BSA::BSASSB #12 (CHK2 information)						
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
2F		BSA::BSASSB #13 (CHK2 information)						
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	ABT error	ABT timeout
30		BSA::BSASSB #12 (CHK2 information)						
	CHK error	FDB parity error	F bus bus error	Slave error	CHK2B	Invalid command/ sequence	F bus timeout	WCHK1 assert
31		BSA::BSASSB #13 (CHK2 information)						
	BSA data parity error	BSA counter parity error	Request error	Sequencer parity error	LIVE INS	F bus open	ABT error	ABT timeout

Byte27=8B (DRR CHK2) Byte28-31 Detail

(14) Byte28=F4:CHK2 without hardware cause

	0	1	2	3	4	5	6	7
28	Subcode: x'F4': CHK2 without hardware cause							
29	DRR::STATS							
	Transfer end A	(RSV)	CMD A wait/execute	CMD A data transfer	Transfer end B	(RSV)	CMD B wait/execute	CMD B data transfer
2A	DRR::STATS							
	CHK2 typical bit	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Force transfer end	Pseudo-failure
2B	Cache module group number (Master)				Cache module group number (Slave)			
2C	DRR::TMRDA							
	Verify on	(RSV)	(RSV)	Double write	Command (Note 1)			
2D	DRR::TMRDB							
	Verify on	(RSV)	(RSV)	Double write	Command (Note 1)			
2E	DRR::ADR0A							
	Transfer address							
2F	DRR::ADR0A							
	Transfer address							
30	DRR::ADR0B							
	Transfer address							
31	DRR::ADR0B							
	Transfer address							

(Note1) 0010 : Dm RD XFR (without intermediate result)
0011 : Dm RD XFR (with intermediate result)
0100 : Dn RD XFR (without intermediate result)
0101 : Dn RD XFR (with intermediate result)
0110 : Dm & Dn RD XFR (without intermediate result)
0111 : Dm & Dn RD XFR (with intermediate result)
1000 : RD XFR (with old Dm)
1001 : RD XFR (with old Dn)
1010 : Syndrome (without intermediate result)
1011 : Syndrome (with intermediate result)
1100 : WR XFR Dm
1101 : WR XFR Dn
1110 : Copy between caches

Blank Sheet

Blank Sheet

Blank Sheet

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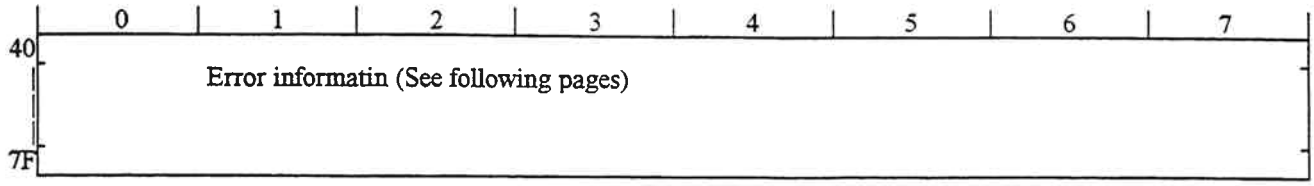
Byte27–8 C (SVP Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
08	Log type							
0A	Failure classification							
0C	System error code							
0E	JCB ID							
0F	REQ ID							
10	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
18	Related failure log number							
1A	Related SIM log number							
1C	Related SSB log number							
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x' 8')				Message (x' C')			
28	Error information (See following pages)							
30	Error type code (Note 1)							
32	Error information (See following pages)							
36	Sympton code (x' FF8C')							
38	Log and message control (x' 00')							
39	Program action code (x' 00')							
3A	Configuration information							
3C	Not used (x' 00')							
3D	Cylinder address							
3F	Head address							

REV.3	May.1995	Jun.1995	Oct.1995	Mar.1996		

Byte27 = 8C (SVP Failure) (2/2)

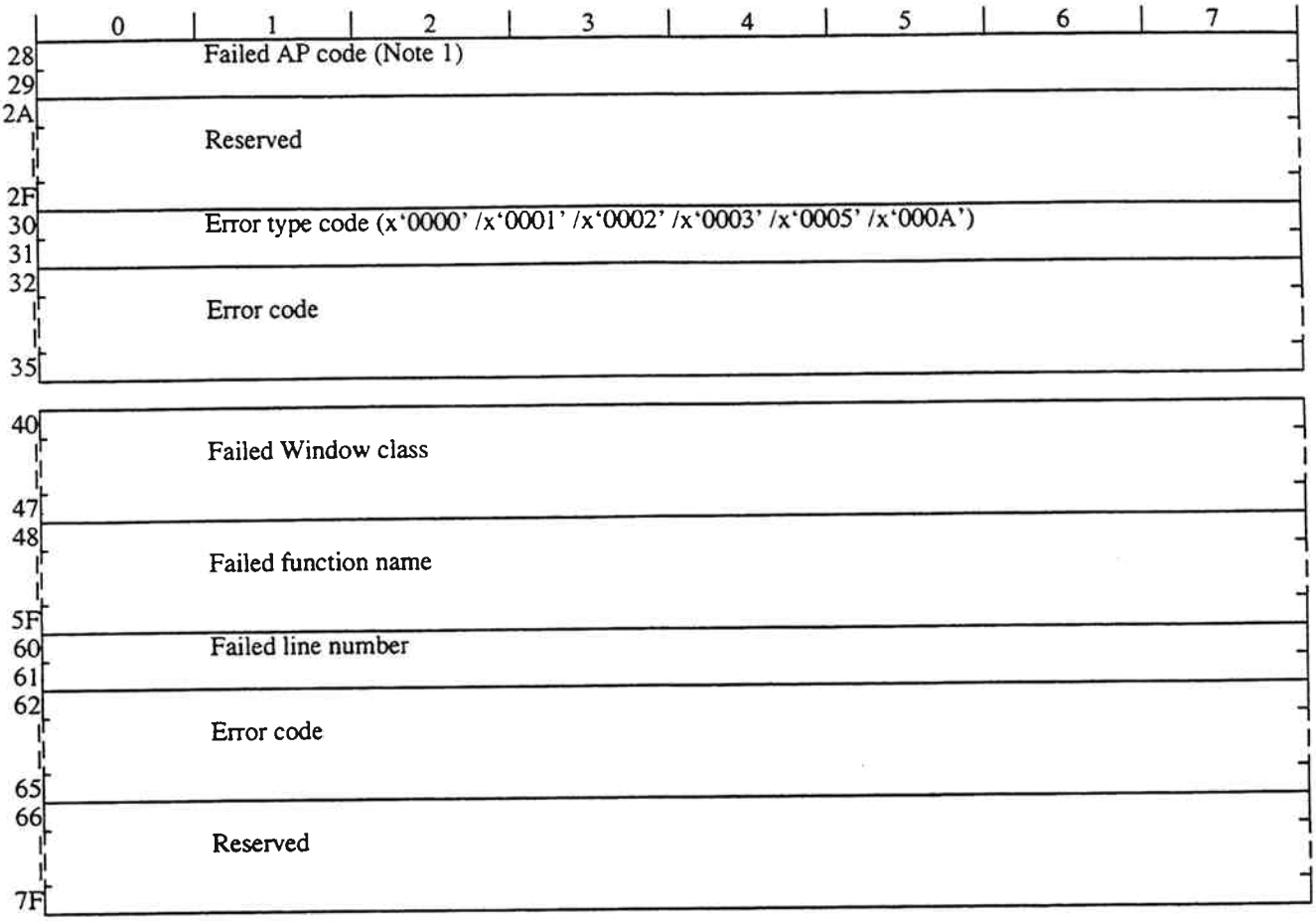


(Note 1) Error type code

x'0000' : Logical inconsistency
x'0001' : HEAP related error
x'0002' : File related error
x'0003' : LAN failure
x'0004' : SSVP failure
x'0005' : Windows failure
x'0006' : CUDG detected error
x'0009' : BOOT detected error
x'000A' : SVP message

Byte27-8 C (SVP Failure) Byte28-35,40-7F detail

(1) Logical inconsistency / HEEP/File/LAN/Windows failure/SVP message

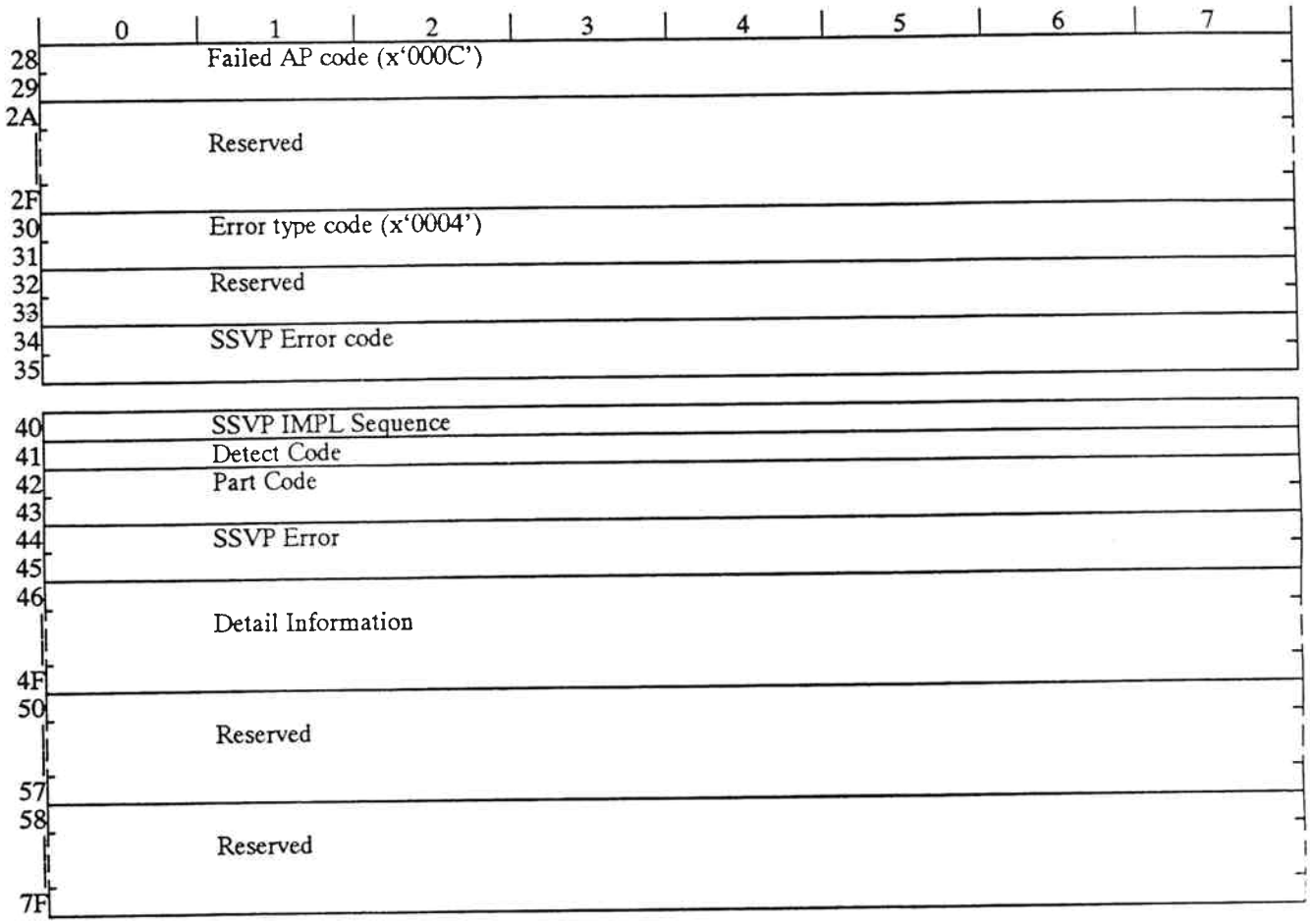


(Note 1) Failed AP code

x'0000' : Dump task
x'0001' : DKU inline
x'0002' : Microprogram change (online)
x'0003' : Information
x'0004' : LOGOUT
x'0005' : PATH inline
x'0006' : Back ground
x'0007' : DIAG
x'0008' : Install
x'0009' : On-line
x'000A' : Micro-program change (off-line)
x'000B' : Special package change
x'000C' : Common function for communication
x'00FF' : Others

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(2) SSVP failure



REV.1	Jul.1995	Oct.1995				

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(3) CUDG detected error

	0	1	2	3	4	5	6	7
28	'CUDG ERR' (x'43 55 44 47 20 45 52 52')							
29								
2A								
2B								
2C								
2D								
2E								
2F								
30	Error type code (x'0006')							
31								
32	Error code (x'00000000')							
33								
34								
35								
40	Error occured time (year)							
41	Error occured time (month)							
42	Error occured time (day)							
43	Error occured time (hour)							
44	Error occured time (minute)							
45	Error occured time (second)							
46	Report MPID							
47	Test object							
48	Test type (x'01' : CUDG3, x'10' : LCDG3)							
49	Failed LCP number							
4A	Test contents							
4B	Test contents							
4C	Error code							
4D	Error code							
4E	Not used							
4F	Not used							
50	Cache module group number (slave 1)							
51	Cache module group number (slave 1)							
52	Cache module group number (slave 1)							
53	Cache module group number (slave 1)							
54	Cache module group number (slave 2)							
55	Cache module group number (slave 2)							
56	Cache module group number (slave 2)							
57	Cache module group number (slave 2)							
58	PCB location (main platter)							
59	PCB location (main platter)							
5A	PCB location (main platter)							
5B	PCB location (cache platter 1)							
5C	PCB location (cache platter 1)							
5D	PCB location (cache platter 2)							
5E	PCB location (cache platter 2)							
5F	Run option							
60	Additional information (Note 1)							
7F								

Byte27 = 8C (SVP Failure) Byte28-35, 40-7F detail

(Note 1) Additional information (for LCDG3 only)

	0	1	2	3	4	5	6	7
60	Reserved							
61								
62								
63								
64	Record type (x'0F' : LCP IMPL diagnostic)							
65	Reserved							
66	MP ID (of CHP : x'10'~x'17')							
67	LCP ID (LCP#A : x'80'~LCP#H : x'01')							
68	Error code (Note 2)							
69	Process type (Note 3)							
6A	Error status 1 (Note 4)							
6B								
6C	Error status 2 (Note 5)							
6D								
6E								
6F								
70								
71								
72								
73								
74	Reserved							
|								
7F								

(Note 2) Error code

Code	Meaning	Function	Remarks
0A	LCDG3' load error	LCDG3'	Make status in loading process
10	Memory clear and test error	LCDG3'	Set LCP address into error status 1
18	LCDG3' MP detected error	LCDG3	Detail information in error status 1 and 2
1A	LCDG3 load error	LCDG3	Make status in loading process
1F	LCDG3' error before LCP loading	Main loading	LCDG 3 information in status
20	SCAN detected error	All	MP detected error
2A	LCP main load error	Main loading	Make status in loading process
30	LCPdetected error	LCDG3'	Detail information in error status 1 and 2
|		LCDG3	
FF			

(Note 3) Process type

Code	Process	Remarks
01	LCDG3'	Set loading error status when a loading error occured.
02	LCDG3	Set loading error status when a loading error occured.
03	Loading	

Byte27=8C (SVP Failure) Byte 28-35,40-7F detail

(Note 4) Error status 1

Code	Meaning
0101	LCDG3' activation faild.
010F	LCP terminated after LCDG3' activation.
0118	No notification after LCDG3' communication.
011F	LCP CHK1 occured after LCDG3' activation.
0120	No REQM after LCDG3' completion.
0122	No notification after LCDG3' set CALM.
0123	No notification after LCDG3' set DGIN.
0125	LCP# ≠ Board#
0301	CRC check start error after loading.
030F	LCP terminated after CRC check completion.
0318	No notification for communicatin after CRC check completion.
031F	CHK1 occured in CRC check.
0320	No REQM after CRC check completion.
0322	No notification after CRC check and CALM completion.
0323	No notification after CRC check and DGIN completion.
0325	LCP# ≠ Board#
032F	No CRC check status ID.
0340	CRC check error in LCDG3 loading/Main loaking.
0380	No start address for CRC check routine.
0385	An error occured in configuration/version information transfer for Main loading.
0401	LCDG3 activation for internal diagnosis failed.
040F	LCP terminated after LCDG3' activation.
0418	No notification after communication for internal diagnosis.
041F	LCP CHK1 occured after internal diagnosis activation.
0420	No REQM after internal diagnosis completion.
0422	No notification after internal diagnosis and CALM.
0423	No notification after internal diagnosis and DGIN.
0425	LCP# ≠ Board#
042F	No status ID for internal diagnosis effect.
043F	No parameter ID for internal diagnosis activation.
044F	No activation address ID for internal diagnosis.
04F0	Controller in configutation is inconsistent with real machine.
04F1	Controller in configutation is inconsistent with real machine.
0501	LCDG3 activation for communication diagnosis failed.
050F	LCP terminated after LCDG3' activation.
0518	No notification after communication for communication diagnosis.
051F	LCP CHK1 occured after communication diagnosis activation.
0520	No REQM after communication diagnosis completion.
0522	No notification after communication diagnosis and CALM.
0523	No notification after communication diagnosis and DGIN.
0525	LCP# ≠ Board#
052F	No effect status ID for communication diagnosis.
053F	No activation parameter ID for communication diagnosis.
054F	No activation address ID for communication diagnosis.
1000-FFFF	An error address of memory clear test (when error code = x'10')
1000-FFFF	LCDG3 error code for internal/communication diagnosis (when error code ≥ x'30')
XXXX	MP error code for LCDG3 communication diagnosis (when error code = x'18')

(Note 5) Error status 2

(1) When process type = x'01' and error code ≥ x'30' and error status 1 ≥ x'1000', LCP error code for LCDG3'.
(2) When process type = x'02' and error code ≥ x'30' and error status 1 ≥ x'1000'), LCP error code for LCDG3.
(3) When process type = x'02' and error code = x'18',
  Byte 6C-6D : Error register address
  Byte 6E-6F : Active register value.
  Byte 70-71 : Expected register value
  Byte 72-73 : Return sequence
(4) When other case, this value is invalid.

Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(4) BOOT detected error

	0	1	2	3	4	5	6	7
28	'BOOT ERR' (x'42 4F 4F 54 20 45 52 52')							
29								
2A								
2B								
2C								
2D								
2E								
2F								
30	Error type code (x'0009')							
31								
32	Error code (x'0000X000' X:Processor number)							
33								
34								
35								
40	Error detection point							
...								
4F								
50	Reserved							
51								
52								
53								
54	Error code for loading error							
55								
56								
57								
58	Error code of internal interface							
59								
5A								
5B								
5C	Error code of initialization function (Note 1)							
5D								
5E								
5F								
60	Reserved							
...								
7F								

(Note 1) Error code of initialization function.

x'31000041' : Forcible start with jumper pin.

x'40000041' : Load module ID in FM is incorrect.
(FM writing was failed or load module is incorrect)

x'42000041' : Sum check error of FM.
(Failure occured at FM writing or input/output error of FM occurred)

Others : Loading for the load module impossible.
(The load module was incorrect)

Byte27 = 8 D (Power Failure) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'D')			
28	Hardware information (See following pages)							
29								
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Error analisis flag (x'00FF' : executed x'FF00' : don't execute)							
33								
34	Processor number (CHA:x'00'~x'07', DKA:x'08'~x'0F')							
35	SSID of self subsystem (low order)							
36	Sympton code (x'FF8D' : LDEV type = DKU87I/x'EF8D' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 D (Power Failure) Hardware information (CHA) (1/5)

	0	1	2	3	4	5	6	7
28	Subcode : x'01' : CHA detected cluster 1 down. x'02' : CHA detected cluster 2 down. x'0F' : CHA detected cluster 1 or 2 down.*							
29		MIC ::RCVINT						
	SYS RST interruption	SEL RST interruption	CHK1A interruption	CHK1B interruption	SMP interruption	LAN/SIO interruption	CHA/DRR interruption	ADP/SCA0 interruption
2A		MIC ::RCVINT						
	Not used	CHK3 interruption	Not used	SCA1 interruption	SCA2 interruption	SCA3 interruption	SCA4 interruption	SCA5 interruption
2B		MIC :: PSOFFOK						
	Not used	Not used	Not used	Not used	Not used	power off request	Reset LAN INT register	Allow power off
2C		MIC ::CHK3STS						
	Not used	Not used	Not used	Not used	Not used	Not used	MIC ABT CHK3	SMP LSI CHK3
2D		SMP ::MSTERR						
	Requester error (M bus)	Shared MEM reduction error	Bus mode setting error	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	1st read data bus code error	2nd read data bus code error
2E		SMP ::MSTERR						
	Read data compare error	1st error phase bus code error	2nd error phase bus code error	Error phase warning	Error phase any error	F bus check error	M bus check error	Master timeout error
2F		SMP ::MSTERR						
	Master timer parity error	F bus arbitration error	Address byte 3 parity error	SMP data parity error	Last data check error	F bus open	M bus open	Not used
30		RCHA::XFS0						
	CHA transfer end	BSA0 request retry	BSA1 request retry	PKT flow count REG status	CHK2	EADP CHK2	CHA CHK2	BSA0 CHK2
31		RCHA::XFS0						
	BSA1 CHK2	Truncation	Halt I/O	Search result DASD=CPU	Search result DASD>CPU	Search result DASD>CPU	MP request BSA0,1 retry	MP or CHA abort BSA0,1

* If cluster # is necessary, refer to the SSB reported from other MPs.

Byte27=8 D (Power Failure) Hardware information (CHA) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERSTS0							
	i960 WR compare error	Not used	MIC READYI timeout	CHK1A	CHK1B	Scan LM,XR access error	Not used	Not used
41	RCHK::CHK1ASTS							
	i960→LM access uncorrectable error		i960→LM write protect	i960→LM out of area	Not used	Not used	LANC→LM write protect	LANC→LM out of area
	Bank0	Bank1						
42	RCHK::CHK1BSTS							
	Refresh address parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
43	MIC::CHK3STS+MIC::MICCHK1STS							
	MIC arbiter CHK3	SMP CHK3	Not used	Not used	MPU reset counter parity ER	Hardware timer parity ER	Wait timer parity ER	Hold timer parity ER
44	MIC::MICHK1STS							
	LAN hold timeout	Wait timeout	XR decoder ERR(29A)	XR decoder ERR(3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
45	MIC::ARBERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	MIC::ARBERR							
	SQST00	SQST01	SQST02	SQST03	SQST04	SQST05	SQST06	SQST07
	Sequencer status							
47	MIC::ARBERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start timeout	LIVEINS delay timer PER	XFR start T.O timer parity ER
	Sequencer status							
48	SMP::CHK1BERROR							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
49	SMP::SLVERR							
	Address bus code error	Command bus code error	Data bus code error	Write bus parity error	Transfer count ERR (command)	Bus mode error (command)	Transfer mode ERR (command)	0
4A	SMP::SLVERR							
	0	0 --	0	Slave timeout error	Slave timer parity ER	Sequencer condition error	0	0
4B	SMP::SLVERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4C	SMP::SLVERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	SMP::SYNCENB							
	(RSV)	(RSV)	MASYNC enable	FASYNC enable	MCSYNC enable	FCSYNC enable	MDSYNC enable	FDSYNC enable
4E	SMCA::MBUSERR							
				Board error	All lock busy	Memory not ready	Backup busy	Double lock error
4F	SMCA::MBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error

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Byte27=8 D (Power Failure) Hardware information (CHA) (3/5)

	0	1	2	3	4	5	6	7
50	SMCA::MBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
51	SMCA:FBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
52	SMCA:FBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
53	SMCA:FBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check errror	Command check error	Address check error
54	SMCA::BORD ERR							
	RAS output error	CAS output error	WE output error	OE(DIR) output error	0	Address output error	Data output error	ECC output error
55	SMCA::BORD ERR							
	Clock error	Refresh error	Timer error	M bus counter error	M bus timer error	Main sequencer error	M bus sequencer error	F bus sequencer error
56	SMCA::MBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
57	SMCB::MBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
58	SMCB::MBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
59	SMCB::FBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
5A	SMCB::FBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Trasfer count error	Bus mode error	Transfer mode error
5B	SMCB::FBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
5C	SMCB::BORD ERR							
	RAS output error	CAS output error	WE output error	OE(DIR) output error	0	Address output error	Data output error	ECC output error
5D	SMCB::BORD ERR							
	Clock error	Refresh error	Timer error	M bus counter error	M bus timer error	Main sequencer error	M bus sequencer error	F bus sequencer error
5E	RCHA::XFC0							
	Data transfer enable	Data transfer execute	(RSV)	(RSV)	CBP mode	Inhibit increment CBF PTR	Cache I/O register access	0:DKA200 1:SSD
5F	RCHA::XFC0							
	Data path 0	Data path 1	Data path 2	Data path 3	(RSV)	F bus width		
						0:8byte 1:4byte	BSA0 enable	BSA1 enable

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Byte27=8 D (Power Failure) Hardware information (CHA) (4/5)

	0	1	2	3	4	5	6	7
60	RCHA::XFS0							
	CHA transfer end	BSA0 retry requested	BSA1 retry requested	Packet flow count REG status	CHK2	EADP CHK2	CHA CHK2	BSA0 CHK2
61	RCHA::XFS0							
	BSA1 CHK2	Truncation	Halt I/O	Search result DASD=CPU	Search result DASD>CPU	Search result DASD<CPU	MP request BSA0,1 retry	MP/CHA abort BSA0,1
62	RCHA::CHK2ST0							
	M/E sequencer parity ER	M/E loop pointer parity ER	CHL XFR sequencer parity ER	CHR/CBIR pointer parity ER	CHR SEQ pointer parity ER	CHR/CHL pointer parity ER	CBIR sequencer parity ER	CBIR0/1 pointer parity ER
63	RCHA::CHK2ST0							
	CBR pointer parity ER	CBX sequencer parity ER	CBX SEQ CBOR PTR parity ER	CBOR pointer parity ER	CBOR/CHR/ SHR PTR parity ER	Packet sequencer parity ER	Search sequencer parity ER	SCH0/1 pointer parity ER
64	RCHA::CHK2ST1							
	Pending counter parity ER	Subblock OFSET CNT parity ER	CKD data LEN COUNT paroty ER	XFR LEN counter parity ER	Block LEN counter parity ER	SEG LEN counter parity ER	FBA data LEN COUNT parity ER	Packet LEN COUNT parity ER
65	RCHA::CHK2ST1							
	CHL/CHR pointer parity ER	CBF XFR W/R PTR parity ER	BSA PAKT recieve stop	CBIR0 FLRC COMP ERR	CBX FLRC COMP ERR	CHC parity ERR	BSA data REG COUNT parity ER	CBXSQ CBR PTR parity ER
66	RCHA::CHK2ST2							
	Pending counter hardware	CBIRDY/AL WCBI CNT parity ER	CBI ready counter overflow	CHR IN-data parity ER	CHR OUT-data parity ER	CBIR0 IN-data parity ER	Micro PKT COUNT parity ER	XFREND0 counter parity ER
67	RCHA::CHK2ST2							
	CBF IN-data parity ER	CBOR IN-data parity ER	LA compare error	SHRA LRC compare error	SHRB LRC compare error	SHRA IN-data parity ER	SHRA OUT-data parity ER	SHRB IN-data parity ER
68	RCHA::CHK2ST3							
	SHRB OUT-data parit ER	SHR compare error 0	SHR compare error 1	MRKOUT/PRT OUT/PRTOUT PP-ERR	CBIR0 SEL PTR parity ER	CBIR1 SEL PTR parity ER	Micro PKT COUNT parity ER	XFREND0 counter parity ER
69	RCHA::CHK2ST3							
	XFREND1 counter parity ER	WR BSA0/1 pointer parity ER	RD BSA0/1 pointer parity ER	CSA0 counter parity ER	CSA1 counter parity ER	CBP R/W pointer parity ER	PFC counter overflow	Reduction CBIR PTR parity ER
6A	RCHA::CHK2ST4							
	Next SEG ADR remain at XFREND	CHR data remain at XFREND	CBIR0 DT remain at XFREND	CBIR1 DT remain at XFREND	CBR data remain at XFREND	CBOR data remain at XFREND	(RSV)	(RSV)
6B	RCHA::CHK2ST4							
	Micro access ER (CKDDL ER)	Micro access ER (FBADL ER)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6C	RCHA::ADPCK2							
	CHL transfer check	CHL overrun	CHACHK2 (CHA)	CHACHK2 (EADP)	CHACK2 (BSA)	CHACHK2 (MP)	CHL side CHC=0	BSA side FBADL=0
6D	RCHA::BSACK2							
	BSA0 PKT retry enable	BSA0 XFR continue CHK2	BSA0 XFR DISCON CHK2	BSA0 NONSYNC CHK2	BSA1 PKT retry enable	BSA1 XFR continue CHK2	BSA1 XFR DISCON CHK2	BSA1 NONSYNC CHK2
6E	BSA0::BSASSB #00							
	CHK error	Last cycle error	Slave 1 parity error	Slave 2 parity error	Slave ID error	FBS read data error	FBS read P-LRC error	FDB parity error
6F	BSA0::BSASSB #01							
	Slave 1 error	Slave 1 warning	Slave 2 error	Slave 2 warning	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27=8 D (Power Failure) Hardware information (CHA) (5/5)

	0	1	2	3	4	5	6	7
70	BSA0::BSASSB #03							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	(RSV)	(RSV)	(RSV)
71	BSA0::BSASSB #04							
	Side A access parity ER	Side B access parity ER	Side A invalid error	Side B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity ER
72	BSA0::BSASSB #05							
	(RSV)	Request sequencer parity ER	Request COUNT/PTR parity ER	MYGRANT parity error	ABT count over	DBF access parity ER	CHA invalid read	Bus mode error
73	BSA0::BSASSB #06							
	WRS COUNT/PTR parity ER	WR1 sequence error	WR1 COUNT/PTR parity ER	WR2 sequence error	WR2 COUNT/PTR parity ER	WR3 sequence error	WR3 COUNT/PTR parity ER	DBF ADR COUNT(A) parity ER
74	BSA0::BSASSB #07							
	DBF ADR COUNT(B) parity ERR	Transfer count over	Command/ status A unmatch	Command/ status B unmatch	RD1 sequence error	RD1 COUNT/PTR parity ER	RD2 sequence error	RD2 COUNT/PTR parity ER
75	BSA0::BSASSB #08							
	RD3 sequence error	RD3 COUNT/PTR parity ER	RD4 sequence error	RD4 COUNT/PTR parity ER	DKA sequence error	DKA COUNT/PTR parity ER	(RSV)	(RSV)
76	BSA0::BSASSB #11							
	LIVE INS	F bus open	ABT sequencer parity ER	LI counter parity ER	ABT tomeout	ABT timer parity ER	Request protocol error	(RSV)
77	BSA1::BSASSB #00							
	CHK error	Last cycle error	Slave 1 parity error	Slave 2 parity error	Slave ID error	FBS read data error	FBS read P-LRC error	FDB parity error
78	BSA1::BSASSB #01							
	Slave 1 error	Slave 1 warning	Slave 2 error	Slave 2 warning	(RSV)	(RSV)	(RSV)	(RSV)
79	BSA1::BSASSB #03							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	(RSV)	(RSV)	(RSV)
7A	BSA1::BSASSB #04							
	Side A access parity ER	Side B access parity ER	Side A invalid error	Side B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity ER
7B	BSA1::BSASSB #05							
	(RSV)	Request sequencer parity ER	Request COUNT/PTR parity ER	MYGRANT parity error	ABT count over	DBF access parity ER	CHA invalid read	Bus mode error
7C	BSA1::BSASSB #06							
	WRS COUNT/PTR parity ER	WR1 sequence error	WR1 COUNT/PTR parity ER	WR2 sequence error	WR2 COUNT/PTR parity ER	WR3 sequence error	WR3 COUNT/PTR parity ER	DBF ADR COUNT(A) parity ER
7D	BSA1::BSASSB #07							
	DBF ADR COUNT(B) parity ER	Transfer count over	Command/ status A unmatch	Command/ status B unmatch	RD1 sequence error	RD1 COUNT/PTR parity ER	RD2 sequence error	RD2 COUNT/PTR parity ER
7E	BSA1::BSASSB #08							
	RD3 sequence error	RD3 COUNT/PTR parity ER	RD4 sequence error	RD4 COUNT/PTR parity ER	DKA sequence error	DKA COUNT/PTR parity ER	(RSV)	(RSV)
7F	BSA1::BSASSB #11							
	LIVE INS	F bus open	ABT sequencer parity ER	LI counter parity ER	ABT tomeout	ABT timer parity ER	Request protocol error	(RSV)

Byte27=8 D (Power Failure) Hardware information (DKA) (1/5)

	0	1	2	3	4	5	6	7
28	Subcode : x'11' : DKA detected cluster 1 down. x'12' : DKA detected cluster 2 down. x'1F' : DKA detected cluster 1 or 2 down.*							
29	MIC ::RCVINT							
	SYS RST interruption	SEL RST interruption	CHK1A interruption	CHK1B interruption	SMP interruption	LAN/SIO interruption	CHA/DRR interruption	ADP/SCA0 interruption
2A	MIC ::RCVINT							
	Not used	CHK3 interruption	Not used	SCA1 interruption	SCA2 interruption	SCA3 interruption	SCA4 interruption	SCA5 interruption
2B	MIC :: PSOFFOK							
	Not used	Not used	Not used	Not used	Not used	power off request	Reset LAN INT register	Allow power off
2C	MIC ::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC ABT CHK3	SMP LSI CHK3
2D	SMP ::MSTERR							
	Requester error (M bus)	Shared MEM reduction error	Bus mode setting error	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	1st read data bus code error	2nd read data bus code error
2E	SMP ::MSTERR							
	Read data compare error	1st error phase bus code error	2nd error phase bus code error	Error phase warning	Error phase any error	F bus check error	M bus check error	Master timeout error
2F	SMP ::MSTERR							
	Master timer parity error	F bus arbitration error	Address byte 3 parity error	SMP data parity error	Last data check error	F bus open	M bus open	Not used
30	BSA0::MONITOR0							
	Not used	Not used	Not used	Not used	Not used	Not used	Option information bit0	Option information bit1
31	BASA1::MONITOR0							
	Not used	Not used	Not used	Not used	Not used	Not used	Option information bit0	Option information bit1

* If cluster # is necessary, refer to the SSB reported from other MPs.

Byte27=8 D (Power Failure) Hardware information (DKA) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERSTS0							
	i960 WR compare error	Not used	MIC READYI timeout	CHK1A	CHK1B	Scan LM,XR access error	Not used	Not used
41	RCHK::CHK1ASTS							
	i960→LM access uncorrectable error		i960→LM write protect	i960→LM out of area	Not used	Not used	LANC→LM write protect	LANC→LM out of area
	Bank0	Bank1						
42	RCHK::CHK1BSTS							
	Refresh address parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
43	MIC::CHK3STS+MIC::MICCHK1STS							
	MIC arbiter CHK3	SMP CHK3	Not used	Not used	MPU reset counter parity ER	Hardware timer parity ER	Wait timer parity ER	Hold timer parity ER
44	MIC::MICHK1STS							
	LAN hold timeout	Wait timeout	XR decoder ERR(29A)	XR decoder ERR(3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
45	MIC::ARBERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	MIC::ARBERR							
	SQST00	SQST01	SQST02	SQST03	SQST04	SQST05	SQST06	SQST07
	Sequencer status							
47	MIC::ARBERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start timeout	LIVEINS delay timer PER	XFR start T.O timer parity ER
	Sequencer status							
48	SMP::CHK1BERROR							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
49	SMP::SLVERR							
	Address bus code error	Command bus code error	Data bus code error	Write bus parity error	Transfer count ERR (command)	Bus mode error (command)	Transfer mode ERR (command)	0
4A	SMP::SLVERR							
	0	0	0	Slave timeout error	Slave timer parity ER	Sequencer condition error	0	0
4B	SMP::SLVERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4C	SMP::SLVERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D	SMP::SYNCENB							
	(RSV)	(RSV)	MASYNC enable	FASYNC enable	MCSYNC enable	FCSYNC enable	MDSYNC enable	FDSYNC enable
4E	SMCA::MBUSERR							
				Board error	All lock busy	Memory not ready	Backup busy	Double lock error
4F	SMCA::MBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error

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Byte27=8 D (Power Failure) Hardware information (DKA) (3/5)

	0	1	2	3	4	5	6	7
50	SMCA::MBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
51	SMCA:FBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
52	SMCA:FBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
53	SMCA:FBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check errror	Command check error	Address check error
54	SMCA::BORD ERR							
	RAS output error	CAS output error	WE output error	OE(DIR) output error	0	Address output error	Data output error	ECC output error
55	SMCA::BORD ERR							
	Clock error	Refresh error	Timer error	M bus counter error	M bus timer error	Main sequencer error	M bus sequencer error	F bus sequencer error
56	SMCA::MBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
57	SMCB::MBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Transfer count error	Bus mode error	Transfer mode error
58	SMCB::MBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
59	SMCB::FBUSERR							
	0	0	0	Board error	All lock busy	Memory not ready	Backup busy	Double lock error
5A	SMCB::FBUSERR							
	Correctable error	Uncorrec-table error	Read data check error	Write data check error	Double access unmatch	Trasfer count error	Bus mode error	Transfer mode error
5B	SMCB::FBUSERR							
	Bus open unmatch	Last cycle error	No DSYNC	No CSYNC	ESYNC wait error	Data check error	Command check error	Address check error
5C	SMCB::BORD ERR							
	RAS output error	CAS output error	WE output error	OE(DIR) output error	0	Address output error	Data output error	ECC output error
5D	SMCB::BORD ERR							
	Clock error	Refresh error	Timer error	M bus counter error	M bus timer error	Main sequencer error	M bus sequencer error	F bus sequencer error
5E	SCA0::INT							
	SCA data trasfer end	SPC interruption	SCA failure	BSA0 failure	BSA1 failure	Not used	Not used	Not used
5F	SCA0::BCK2							
	BSA0 CHK2A/2B error	BSA0 control error	BSA0 arbiter error	Not used	Not used	Not used	Not used	Not used

Byte27=8 D (Power Failure) Hardware information (DKA) (4/5)

	0	1	2	3	4	5	6	7
60	SCA0::BCK2							
	BSA1 CHK2A/2B error	BSA1 control error	BSA1 arbiter error	Not used	Not used	Not used	Not used	Not used
61	SCA1::INT							
	SCA data transfer end	SPC interruption	SCA failure	BSA0 failure	BSA1 failure	Not used	Not used	Not used
62	SCA1::BCK2							
	BSA0 CHK2A/2B error	BSA0 control error	BSA0 arbiter error	Not used	Not used	Not used	Not used	Not used
63								
	BSA1 CHK2A/2B error	BSA1 control error	BSA1 arbiter error	Not used	Not used	Not used	Not used	Not used
64	SCA2::INT							
	SCA data transfer end	SPC interruption	SCA failure	BSA0 failure	BSA1 failure	Not used	Not used	Not used
65	SCA2::BCK2							
	BSA0 CHK2A/2B error	BSA0 control error	BSA0 arbiter error	Not used	Not used	Not used	Not used	Not used
66	SCA2::BCK2							
	BSA1 CHK2A/2B error	BSA1 control error	BSA1 arbiter error	Not used	Not used	Not used	Not used	Not used
67	SCA3::INT							
	SCA data transfer end	SPC interruption	SCA failure	BSA0 failure	BSA1 failure	Not used	Not used	Not used
68	SCA3::BCK2							
	BSA0 CHK2A/2B error	BSA0 control error	BSA0 arbiter error			Not used	Not used	Not used
69	SCA3::BCK2							
	BSA1 CHK2A/2B error	BSA1 control error	BSA1 arbiter error	Not used	Not used	Not used	Not used	Not used
6A	DRR::STATS							
	Transfer end A	0	Wait or executing command A	Comand A transfer in progess	Transfer end B	0	Wait or executing command B	Command B transfer in progess
6B	DRR::STATS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	0/CHK1B	Force transfer end	Pseudo failure
6C	DRR::ESTA0							
	Undefined register write ERR	Read only register write ERR	Side A register write ERR	Side B register write ERR	Address parity error	Byte access error	Input data parity ER	Output data parity ER
6D	DRR::RMODE7							
	0	0	0	0	ALARM	MESSAGE	CUDG3A FALL	CUDG3B FALL
6E	BSA0::BSASSB #00							
	CHK error	Last cycle error	Slave 1 parity error	Slave 2 parity error	Slave ID error	FBS read data error	FBS read P-LRC error	FDB parity error
6F	BSA0::BSASSB #01							
	Slave 1 error	Slave 1 warning	Slave 2 error	Slave 2 warning	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27=8 D (Power Failure) Hardware information (DKA) (5/5)

	0	1	2	3	4	5	6	7
70	BSA0::BSASSB #03							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	(RSV)	(RSV)	(RSV)
71	BSA0::BSASSB #04							
	Side A access parity ER	Side B access parity ER	Side A invalid error	Side B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity ER
72	BSA0::BSASSB #05							
	(RSV)	Request sequencer parity ER	Request COUNT/PTR parity ER	MYGRANT parity error	ABT count over	DBF access parity ER	CHA invalid read	Bus mode error
73	BSA0::BSASSB #06							
	WRS COUNT/PTR parity ER	WR1 sequence error	WR1 COUNT/PTR parity ER	WR2 sequence error	WR2 COUNT/PTR parity ER	WR3 sequence error	WR3 COUNT/PTR parity ER	DBF ADR COUNT(A) parity ER
74	BSA0::BSASSB #07							
	DBF ADR COUNT(B) parity ERR	Transfer count over	Command/ status A unmatch	Command/ status B unmatch	RD1 sequence error	RD1 COUNT/PTR parity ER	RD2 sequence error	RD2 COUNT/PTR parity ER
75	BSA0::BSASSB #08							
	RD3 sequence error	RD3 COUNT/PTR parity ER	RD4 sequence error	RD4 COUNT/PTR parity ER	DKA sequence error	DKA COUNT/PTR parity ER	(RSV)	(RSV)
76	BSA0::BSASSB #11							
	LIVE INS	F bus open	ABT sequencer parity ER	LI counter parity ER	ABT tomeout	ABT timer parity ER	Request protocol error	(RSV)
77	BSA1::BSASSB #00							
	CHK error	Last cycle error	Slave 1 parity error	Slave 2 parity error	Slave ID error	FBS read data error	FBS read P-LRC error	FDB parity error
78	BSA1::BSASSB #01							
	Slave 1 error	Slave 1 warning	Slave 2 error	Slave 2 warning	(RSV)	(RSV)	(RSV)	(RSV)
79	BSA1::BSASSB #03							
	HDB 1 parity error	HDB 3 parity error	HDB 2 parity error	HDB 4 parity error	LRC GEN parity error	(RSV)	(RSV)	(RSV)
7A	BSA1::BSASSB #04							
	Side A access parity ER	Side B access parity ER	Side A invalid error	Side B invalid error	F bus timeout	(RSV)	WCHK1 assert	F bus timer parity ER
7B	BSA1::BSASSB #05							
	(RSV)	Request sequencer parity ER	Request COUNT/PTR parity ER	MYGRANT parity error	ABT count over	DBF access parity ER	CHA invalid read	Bus mode error
7C	BSA1::BSASSB #06							
	WRS COUNT/PTR parity ER	WR1 sequence error	WR1 COUNT/PTR parity ER	WR2 sequence error	WR2 COUNT/PTR parity ER	WR3 sequence error	WR3 COUNT/PTR parity ER	DBF ADR COUNT(A) parity ER
7D	BSA1::BSASSB #07							
	DBF ADR COUNT(B) parity ER	Transfer count over	Command/ status A unmatch	Command/ status B unmatch	RD1 sequence error	RD1 COUNT/PTR parity ER	RD2 sequence error	RD2 COUNT/PTR parity ER
7E	BSA1::BSASSB #08							
	RD3 sequence error	RD3 COUNT/PTR parity ER	RD4 sequence error	RD4 COUNT/PTR parity ER	DKA sequence error	DKA COUNT/PTR parity ER	(RSV)	(RSV)
7F	BSA1::BSASSB #11							
	LIVE INS	F bus open	ABT sequencer parity ER	LI counter parity ER	ABT tomeout	ABT timer parity ER	Request protocol error	(RSV)

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Byte27=8 D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x'80' : DKA detected DKU/HDU Power Failure							
29	Failure detected PDEV							
	SPC Pass# (0 ~ 3)				SCSI id# (0 ~ x'F')			
2A	PDEV Power Status (SPC Pass#0, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2B	PDEV Power Status (SPC Pass#0, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
2C	PDEV Power Status (SPC Pass#1, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2D	PDEV Powr Status (SPC Pass#1, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
2E	PDEV Power Status (SPC Pass#2,basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2F	PDEV Power Status (SPC Pass#2, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
30	PDEV Power Status (SPC Pass#3, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
31	PDEV Power Status (SPC Pass#3, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')

(*) BYTE32 ~ 7F : Not Used

Byte27=8 D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x'90' : DKA detected DKU/HDU Power Failure							
29	Failure HDU (SPC Pass) before restore detected							
	0				Pass#3 Status	Pass#2 Status	Pass#1 Status	Pass#0 Status
2A	PDEV Power Status (SPC Pass#0, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2B	PDEV Power Status (SPC Pass#0, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
2C	PDEV Power Status (SPC Pass#1, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2D	PDEV Powr Status (SPC Pass#1, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
2E	PDEV Power Status (SPC Pass#2,basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
2F	PDEV Power Status (SPC Pass#2, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')
30	PDEV Power Status (SPC Pass#3, basic DKU box)							
	PDEV (id# x'F')	PDEV (id# x'E')	PDEV (id# x'D')	PDEV (id# x'C')	PDEV (id# x'B')	PDEV (id# x'A')	PDEV (id# x'9')	PDEV (id# x'8')
31	PDEV Power Status (SPC Pass#3, extent DKU box)							
	PDEV (id# x'7')	PDEV (id# x'6')	PDEV (id# x'5')	PDEV (id# x'4')	PDEV (id# x'3')	PDEV (id# x'2')	PDEV (id# x'1')	PDEV (id# x'0')

(*) BYTE32 ~ 7F : Not Used

Byte27 = 8E & Byte34 = X0 & Byte28 = 0X/1X (CHK1A/WCHK1) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'0X'/x'1X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number (Note 1)				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I) (Note 2)							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

(Note 1) Failed processor number for WCHK1

(Note 2) This information is not fixed until DKC reports SSB to HOST.

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Byte27=8 E & Byte34=X0 & Byte28=0X/1X (CHK1A/WCHK1) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address (1) when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected						(RSV)	(RSV)
44	RCHK::ERBYT							
	(RSV)	(RSV)	(RSV)	(RSV)	L-bus BE0-3 signal			
45	RCHK::ERORD							
	Data (0) before correction when LM access erroroccurred							
46	RCHK::ERORD							
	Data (1) before correction when LM access error occurred							
47	RCHK::ERORD							
	Data (2) before correction when LM access error occurred							
48	RCHK::ERORD							
	Data (3) before correction when LM access error occurred							
49	RCHK::ERORC							
	Check bit before correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8 E & Byte34=X0 & Byte28=0X/1X (CHK1A/WCHK1) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	LANC→LM access CORREC		LANC→LM access CORREC ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::SCANER							
	Scan→LM access UNCOR ERR detect		Not used	Scan→LM Out of LM area	Scan→XR Invalid RD XR ADR	Scan→XR Invalid WR XR ADR	Not used	Not used
	Bank0	Bank1						
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	RCHK::RCMADR							
	i960-M address (0)							
58	RCHK::RCMADR							
	i960-M address (1)							
59	RCHK::RCMADR							
	i960-M address (2)							
5A	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
5B	RCHK::RCMDATA							
	i960-M data (0)							
5C	RCHK::RCMDATA							
	i960-M data (1)							
5D	RCHK::RCMDATA							
	i960-M data (2)							
5E	RCHK::RCMDATA							
	i960-M data (3)							
5F	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M RD/WR INFO	i960-M burst last INFO	i960-M address strobe

Byte27=8 E & Byte34=X0 & Byte28=0X/1X (CHK1A/WCHK1) (4/5)

	0	1	2	3	4	5	6	7
60	RCHK::RCCHADR							
	i960-CH address (0)							
61	RCHK::RCCHADR							
	i960-CH address (1)							
62	RCHK::RCCHADR							
	i960-CH address (2)							
63	RCHK::RCCHADR							
	i960-CH address (3)						Not used	Not used
64	RCHK::RCCHDATA							
	i960-CH data (0)							
65	RCHK::RCCHDATA							
	i960-CH data (1)							
66	RCHK::RCCHDATA							
	i960-CH data (2)							
67	RCHK::RCCHDATA							
	i960-CH data (3)							
68	RCHK::CMCNTL							
	Not used	Not used	Not used	Not used	Not used	i960-CH write/read	i960-CH burst last	i960-CH address strobe
69	MIC::LAST 1 IP							
	Last 1 IP address (0)							
6A	MIC::LAST 1 IP							
	Last 1 IP address (1)							
6B	MIC::LAST 1 IP							
	Last 1 IP address (2)							
6C	MIC::LAST 1 IP							
	Last 1 IP address (3)							
6D	MIC::LAST 2 IP							
	Last 2 IP address (0)							
6E	MIC::LAST 2 IP							
	Last 2 IP address (1)							
6F	MIC::LAST 2 IP							
	Last 2 IP address (2)							

Byte27=8 E & Byte34=X0 & Byte28=0X/1X (CHK1A/WCHK1) (5/5)

	0	1	2	3	4	5	6	7
70	MIC::LAST 2 IP							
	Last 2 IP address (3)							
71	RCHK::RCLOGCNT							
	i960-M byte enable information				Not used	i960-M/CH write/read	i960-M/CH burst last	i960-M/CH address strobe
72	RCHK::RCSTATUS							
	Not used	RISC compare eror	Byte enable error	WR/RD compare error	Burst last COMP ERR	Address strobe COMP ERR	Data compare error	Address compare error
73	RCHK::RCREGION							
	Region table 00 bus width (00:8b, 01:16b, 10:32bit)		Region table 01 bus width (00:8b, 01:16b, 10:32bit)		Region table 02 bus width (00:8b, 01:16b, 10:32bit)		Region table 03 bus width (00:8b, 01:16b, 10:32bit)	
74	RCHK::RCREGION							
	Region table 04 bus width (00:8b, 01:16b, 10:32bit)		Region table 05 bus width (00:8b, 01:16b, 10:32bit)		Region table 06 bus width (00:8b, 01:16b, 10:32bit)		Region table 07 bus width (00:8b, 01:16b, 10:32bit)	
75	RCHK::RCREGION							
	Region table 08 bus width (00:8b, 01:16b, 10:32bit)		Region table 09 bus width (00:8b, 01:16b, 10:32bit)		Region table 10 bus width (00:8b, 01:16b, 10:32bit)		Region table 11 bus width (00:8b, 01:16b, 10:32bit)	
76	RCHK::RCREGION							
	Region table 12 bus width (00:8b, 01:16b, 10:32bit)		Region table 13 bus width (00:8b, 01:16b, 10:32bit)		Region table 14 bus width (00:8b, 01:16b, 10:32bit)		Region table 15 bus width (00:8b, 01:16b, 10:32bit)	
77	RCHK::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	L bus W/R signal
78	RCHK::CHK1ASTS							
	i960→LM access uncorrectable ERR		i960→LM Write protect	i960→LM Out of LM area	Not used	Not used	LANC→LM Write protect	LANC→LM Out of LM area
	Bank0	Bank1						
79	RCHK::CECTH							
	Threshold for LM correctable error							
7A	RCHK::LMWRADRU							
	Not used	Upper limit address for LM writing (high)						
7B	RCHK::LMWRADRU							
	Upper limit address for LM writing (low)						Not used	Not used
7C	RCHK::LMWRADRL							
	Not used	Lower limit address for LM writing (high)						
7D	RCHK::LMWRADRL							
	Lower limit address for LM writing (low)						Not used	Not used
7E	MIC ::ERR_STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7F	MIC ::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(1) Byte28=01 : Address inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 01' : Address inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCMADR							
	i960-M address (0)							
2B	RCHK::RCMADR							
	i960-M address (1)							
2C	RCHK::RCMADR							
	i960-M address (2)							
2D	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
2E	RCHK::RCCHADR							
	i960-CH address (0)							
2F	RCHK::RCCHADR							
	i960-CH address (1)							
30	RCHK::RCCHADR							
	i960-CH address (2)							
31	RCHK::RCCHADR							
	i960-CH address (3)						Not used	Not used

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(2) Byte28=02 : Data inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 02' : Data inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCMADR							
	i960-M address (0)							
2B	RCHK::RCMADR							
	i960-M address (1)							
2C	RCHK::RCMADR							
	i960-M address (2)							
2D	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
2E	RCHK::RCCHADR							
	i960-M DATA (0)							
2F	RCHK::RCMDATA							
	i960-M DATA (1)							
30	RCHK::RCMDATA							
	i960-M DATA (2)							
31	RCHK::RCMDATA							
	i960-M DATA (3)							

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(3) Byte28=03 : ADS signal inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 03' : ADS signal inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCCHCNTL							
	Not used	Not used	Not used	Not used	Not used	i960-CH read/write information	i960-CH burst last information	i960-CH address strobe information
2B	RCHK::RCLOGCNT							
	i960-M byte enable information				Not used	i960-M/CH read/write information	i960-M/CH burst last information	i960-M/CH address strobe information
2C	RCHK::RCMADR							
	i960-M address (0)							
2D	RCHK::RCMADR							
	i960-M address (1)							
2E	RCHK::RCMADR							
	i960-M address (2)							
2F	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
30	RCHK::RCSTATUS							
	Not used	RISC compare error	Burst enable error	WR/RD compare error	Burst last compare error	Address strobe compare error	Data strobe compare error	Address compare error
31	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR	Not used	Not used
	Bank0	Bank1						

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Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(4) Byte28=04 : BLAST signal inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 04' : BLAST signal inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCCHCNTL							
	Not used	Not used	Not used	Not used	Not used	i960-CH read/write information	i960-CH burst last information	i960-CH address strobe information
2B	RCHK::RCLOGCNT							
	i960-M byte enable information				Not used	i960-M/CH read/write information	i960-M/CH burst last information	i960-M/CH address strobe information
2C	RCHK::RCMADR							
	i960-M address (0)							
2D	RCHK::RCMADR							
	i960-M address (1)							
2E	RCHK::RCMADR							
	i960-M address (2)							
2F	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
30	RCHK::RCSTATUS							
	Not used	RISC compare error	Burst enable error	WR/RD compare error	Burst last compare error	Address strobe compare error	Data strobe compare error	Address compare error
31	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR	Not used	Not used
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(5) Byte28=05 : WE signal inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 05' : WE signal inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCCHCNTL							
	Not used	Not used	Not used	Not used	Not used	i960-CH read/write information	i960-CH burst last information	i960-CH address strobe information
2B	RCHK::RCLOGCNT							
	i960-M byte enable information				Not used	i960-M/CH read/write information	i960-M/CH burst last information	i960-M/CH address strobe information
2C	RCHK::RCMADR							
	i960-M address (0)							
2D	RCHK::RCMADR							
	i960-M address (1)							
2E	RCHK::RCMADR							
	i960-M address (2)							
2F	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
30	RCHK::RCSTATUS							
	Not used	RISC compare error	Burst enable error	WR/RD compare error	Burst last compare error	Address strobe compare error	Data strobe compare error	Address compare error
31	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(6) Byte28=06 : BE signal inconsistent in MP comparison

	0	1	2	3	4	5	6	7
28	Subcode : x' 06' : BE signal inconsistent in MP comparison							
29	RCHK::RCMCNTL							
	i960-M byte enable information				Not used	i960-M read/write information	i960-M burst last information	i960-M address strobe information
2A	RCHK::RCCHCNTL							
	Not used	Not used	Not used	Not used	Not used	i960-CH read/write information	i960-CH burst last information	i960-CH address strobe information
2B	RCHK::RCLOGCNT							
	i960-M byte enable information				Not used	i960-M/CH read/write information	i960-M/CH burst last information	i960-M/CH address strobe information
2C	RCHK::RCMADR							
	i960-M address (0)							
2D	RCHK::RCMADR							
	i960-M address (1)							
2E	RCHK::RCMADR							
	i960-M address (2)							
2F	RCHK::RCMADR							
	i960-M address (3)						Not used	Not used
30	RCHK::RCSTATUS							
	Not used	RISC compare error	Burst enable error	WR/RD compare error	Burst last compare error	Address strobe compare error	Data compare error	Address compare error
31	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR	Not used	Not used
	Bank0	Bank1						

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Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(7) Byte28=07 : Uncorrectable error when MP reads/writes LM data

	0	1	2	3	4	5	6	7
28	Subcode : x' 07' : Uncorrectable error when MP reads/writes LM data							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK:: ERORD							
	Data (0) before correction							
2E	RCHK:: ERORD							
	Data (1) before correction							
2F	RCHK:: ERORD							
	Data (2) before correction							
30	RCHK:: ERORD							
	Data (3) before correction							
31	RCHK::CHK1ASTS:8000 0128 (b30-b37)							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(8) Byte28=08 : Write protection violated when MP reads/writes LM data

	0	1	2	3	4	5	6	7
28	Subcode : x' 08' : Write protection violated when MP acess to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMWRADRU							
	Not used	Upper limit address of writable LM mounting area (high)						
2E	RCHK::LMWRADRU							
	Upper limit address of writable LM mounting area (low)						Not used	Not used
2F	RCHK::LMWRADRL							
	Not used	Lower limit address of writable LM mounting area (high)						
30	RCHK::LMWRADRL							
	Lower limit address of writable LM mounting area (low)						Not used	Not used
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(9) Byte28=09 : Out of mounting area accessed when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 09' : Out of mounting area accessed when MP accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	CMP ERR	Not used	READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(10) Byte28=0A : Write protection violated when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 0A' : Write protection violated when LANC accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMWRADRU							
	Not used	Upper limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	Upper limit address of writable LM mounting area (lower order)						Not used	Not used
2F	RCHK::LMWRADRL							
	Not used	Lower limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Lower limit address of writable LM mounting area (lower order)						Not used	Not used
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(11) Byte28=0B : Out of mounting area accessed when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 0B' : Out of mounting area accessed when LANC accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 write operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		i960 WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(12) Byte28=0C : MIC ready timeout

	0	1	2	3	4	5	6	7
28	Subcode : x' 0C' : x' 0C' : MIC ready timeout							
29	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2A	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2B	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2C	RCHK:: IFTMRCTL							
	Control information for READY timeout timer							
2D	Not used							
	0	0	0	0	0	0	0	0
2E	RCHK::TOSTS							
	MIC READYI timeout	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 write operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of area LM	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		i960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(13) Byte28=10 : Uncorrectable error when MP reads/writes LM data

	0	1	2	3	4	5	6	7
28	Subcode : x' 10' : Uncorrectable error when MP reads/writes LM data							
29	RCHK::ERADR							
	Address(0) for L bus							
2A	RCHK::ERADR							
	Address(1)for L bus							
2B	RCHK::ERADR							
	Address(2)for L bus							
2C	RCHK::ERADR							
	Address(3)for L bus						Not used	Not used
2D	RCHK::ERORD							
	Data(0) before correction							
2E	RCHK::ERORD							
	Data(1) before correction							
2F	RCHK::ERORD							
	Data(2) before correction							
30	RCHK::ERORD							
	Data(3) before correction							
31	RCHK::ERORC							
	Check bit before correction							

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(14) Byte28=11 : Write protection violated when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 11' : Write protection violated when MP accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMWRADRU							
	Not used	Upper limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	Upper limit address of writable LM mounting area (lower order)						Not used	Not used
2F	RCHK::LMWRADRL							
	Not used	Lower limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Lower limit address of writable LM mounting area (lower order)						Not used	Not used
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(15) Byte28=12 : Out of mounting area accessed when MP accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 12' : Out of mounting area accessed when MP accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 wrote operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(16) Byte28=13 : Write protection violated when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 13' : Write protection violated when LANC accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMWRADRU							
	Not used	Upper limit address of writable LM mounting area (higher order)						
2E	RCHK::LMWRADRU							
	Upper limit address of writable LM mounting area (lower order)						Not used	Not used
2F	RCHK::LMWRADRL							
	Not used	Lower limit address of writable LM mounting area (higher order)						
30	RCHK::LMWRADRL							
	Lower limit address of writable LM mounting area (lower order)						Not used	Not used
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		I960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(17) Byte28=14 : Out of mounting area accessed when LANC accesses to LM

	0	1	2	3	4	5	6	7
28	Subcode : x' 14' : Out of mounting area accessed when LANC accesses to LM							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Upper limit address of LM
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 write operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		i960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27=8 E (CHK1A/WCHK1) Byte28-31 Detail

(18) Byte28=15 : MIC ready timeout

	0	1	2	3	4	5	6	7
28	Subcode : x' 15' : MIC ready timeout							
29	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2A	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2B	RCHK::IFTMRCTL							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2C	RCHK:: IFTMRCTL							
	Control information for READY timeout timer							
2D	Not used							
	0	0	0	0	0	0	0	0
2E	RCHK::TOSTS							
	MIC READYI timeout	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Inconsist in i960 write operation	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	Not used	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of area LM	Scan→ Invalid read XR address	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	i960→Uncorrectable error in LM		i960→WR protected LM area	i960→Out of mount LM area	Not used	Not used	LANC→WR protected LM area	LANC→Out of mount LM area
	Bank0	Bank1						

Byte27 = 8E & Byte34 = X0 & Byte28 = 2X/3X (CHA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'2X'/x'3X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34=X0 & Byte28=2X/3X (CHA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address () when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected							
44	RCHK::ERBYT							
	(RSV)	(RSV)	(RSV)	(RSV)	L-bus BE0-3 signal			
45	RCHK::ERORD							
	Data (0) befor correction when LM access error occurred							
46	RCHK::ERORD							
	Data (1) befor correction when LM access error occurred							
47	RCHK::ERORD							
	Data (2) befor correction when LM access error occurred							
48	RCHK::ERORD							
	Data (3) befor correction when LM access error occurred							
49	RCHK::ERORC							
	Check bit befor correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8 E & Byte34=X0 & Byte28=2X/3X (CHA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		LANC→LM access UNCORR ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::SCANER							
	Scan→LM access UNCOR ERR detect		Not used	Scan→LM Out of LM area	Scan→XR Invalid RD XR ADR	Scan→XR Invalid WR XR ADR	Not used	Not used
	Bank0	Bank1						
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	RCHK::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B error	SMP/DRR CHK1B error	MIC CHK1B error
58	RCHK::CHK1BSTS							
	XR0:EADP CHK1B error	XR1:BSA0 CHK1B error	XR2:BSA1 CHK1B error	XR3 CHK1B ERR (0)	XR4 CHK1B ERR (0)	XR5 CHK1B ERR (0)	Not used	RCHK1 CHK1B error
59	RCHK::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity ER	Hard timer parity ER	Wait timer parity ER	Hold timer parity ER
5A	RCHK::MICCHK1STS							
	LAN hold timer parity ER	Wait timeout	XR decoder ERR (29A)	XR decoder ERR (3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
5B	RCHK::TIMERR							
	Timer#0 parity error	Timer#1 arity error	Timer#2 arity error	Timer#3 arity error	Timer#4 arity error	Timer#5 arity error	Timer#6 arity error	Not used
5C	RCHK::ABTERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start tomeout	LIVEINS delay timer PE	Transfer start timer PE
5D	RCHK::XRDBSPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR bus ADR P-ERR (24-27)	XR bus ADR P-ERR (30-37)
5E	RCHK::LBUSPER							
	Not used	Not used	Not used	Not used	Local DT bus P-ERR (00-07)	Local DT bus P-ERR (10-17)	Local DT bus P-ERR (20-27)	Local DT bus P-ERR (30-37)
5F	RCHK::XBUSPER							
	Not used	Not used	Not used	Not used	XR bus DT parity ER (00-07)	XR bus DT parity ER (10-17)	XR bus DT parity ER (20-27)	XR bus DT parity ER (30-37)

Byte27=8 E & Byte34=X0 & Byte28=2X/3X (CHA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	RCHK::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3
61	RCHK::RSTSTS							
	Not used	Not used	Micro CHK1B pending	Micro CHK1A pending	Micro MCNRST2 pending	Micro MCNRST1 pending	Micro MPRST pending	Micro MNTRST pending
62	RCHK::RSTSTS							
	Not used	Not used	Scan mode set pending	CHK1A pending	WCHK1 pending	SELRST pending	SYSRST pending	P/S on reset pending
63	RCHK::ARBCTL							
	LIVEINS count PE CHK test	XFR start timer PE CHK test	Sequencer reset	(RSV)	LIVEINS input SIG mask	CHK3 reset	DIAG mode	Arbier initiate
64	RCHK::CHK1B							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
65	RCHK::SMPERROR							
	Not used	Not used	Not used	Not used	Not used	Master CHK3 error	Slave CHK3 error	CHK1 error
66	SMP ::WAD							
	i960 address (0) for M bus access							
67	SMP ::WAD							
	i960 address (0) for M bus access							
68	SMP ::WAD							
	i960 address (0) for M bus access							
69	SMP ::WAD							
	i960 address (0) for M bus access							
6A	SMP ::WAD							
	Write data (0) for M bus access							
6B	SMP ::WAD							
	Write data (1) for M bus access							
6C	SMP ::WAD							
	Write data (2) for M bus access							
6D	SMP ::WAD							
	Write data (3) for M bus access							
6E	SMP ::WR/BE							
	Not used	Not used	Not used	Write/read	i960 byte enable for M bus access			
6F	SMP ::TXSEQ							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Master sequencer state

Byte27=8 E & Byte34=X0 & Byte28=2X/3X (CHA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	RCHK::TXSEQ							
	Master sequencer state(0)							
71	RCHK:: TXSEQ							
	Master sequencer state(1)							
72	RCHK::XFC							
	Data trasfer enable	Data transfer execute	(RSV)	(RSV)	CBP mode	CBF PTR increment inhibited	CACHE I/O REG access	SSD/ DKC200
73	RCHK::XFC							
	Data path 0	Data path 1	Data path 2	Data path 3	(RSV)	F-bus WID 0:8byte/ 1:4byte	F-bus BSA0 connect	F-bus BSA1 connect
74	RCHK::PCMD2							
	'1'	Bus mode			Transfer mode			
		Bus width 0:8,1:4b	FBUS0 enable	FBUS1 enable	0:Write 2:Cache to cache 1:Read 3:Double write			
75	RCHK::XFS0							
	CHA data transfer end	BSA0 retry request	BSA1 retry request	PACKET FLOW CNT REG STAT	CHK2	EADP CHK2	CHA CHK2	BSA0 CHK2
76	RCHK::XFS0							
	BSA1 CHK2	Truncation	Halt I/O	Search result DASD=CPU	Search result DASD>CPU	Search result DASD<CPU	MP REQ BSA0,1 retry	MP REQ BSA0,1 abort
77	RCHK::XFS1							
	1:PARAL 0:SERIAL	XFR mode0 (CHL BUS width)	XFR mode1 (Data XFR speed)	MP retry occurred	MP abort occurred	CHA abort occurred	Pseud ERR occurred (CHK1B)	Pseud ER occurred (CHK2)
78	RCHK::CHK1ASTS							
	NEXT SEG ADR REG status	BSA0 last packet XFR end	BSA1 last packet XFR end	BSA0 CHK1B	BSA1 CHK1B	Next SEG address wait	Packet flow CNT	MCN RST occurred
79	RCHK::XFS1							
	XR address 2 parity ER	XR address 3 parity ER	DBUS parity error 0	DBUS parity error 1	BBUS parity error 0	BBUS parity error 1	XR ADR decode error 2	XR ADR decode error 3
7A	RCHK::MPCHK1B							
	Clock error	Micro access error	Not used	Not used	Not used	Not used	Not used	Not used
7B	EADP::CCK10							
	XRAPER3	BEPER	DBUSPER3	BBUSPER3	XRADDECER	(RSV)	(RSV)	(RSV)
7C	RCHK::LMWRADRL							
	Address parity error	WR data bus(H) parity ER	WR data bus(L) parity ER	RD data bus(H) parity ER	RD data bus(L) parity ER	(RSV)	(RSV)	(RSV)
7D	EADP::CCK11							
	LCM BUSY	LCP STOP	LCP ADRCMP match	LCP TRACER stop	LCM detected ADPLCM ERR	LCM detected WCHK1	LCM path disable	Parallel chanel
7E	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7F	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(1) Byte28=21 : RCHA CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 21' : RCHA CHK1B : XR bus access ERR/internal clock ERR/ micro access ERR							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (EADP) CHK1B	XR2 (EADP) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	CHA ::MPCHK1B							
	XR address2 parity error	XR address3 parity error	DBUS write data parity error 0	DBUS write data parity error 1	BBUS read data parity error 0	BBUS read data parity error 1	XR address2 decode eror	XR address3 decode eror
2C	CHA ::MPCHK1B							
	CHA clock failure	Micro access error	Not used	Not used	Not used	Not used	Not used	Not used
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(2) Byte28=22 : SMP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 22' : SMP CHK1B : XRE bus parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	MIC :: CHK1B							
	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	Address byte 3 parity error	Data byte 0 parity error	Data byte 1 parity error	Data byte 2 parity error	Data byte 3 parity error
2C	MIC ::TIMER							
	CHA clock failure	Micro access error	Not used	Not used	Not used	Not used	Not used	Not used
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(3) Byte28=23 : ADP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 23' : ADP CHK1B (XR bus parity error)							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	EADP::CCK10							
	XRAPER3	BEPER	DBUSPER3	BBUSPER3	XRADDECER	(RSV)	(RSV)	(RSV)
2C	EADP::CCK11							
	i960 I/F address parity error	i960 I/F write data(H) parity error	i960 I/F write data(L) parity error	i960 I/F read data(H) parity error	i960 I/F read data(L) parity error	(RSV)	(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(4) Byte28=24 : BSA0 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 24' : BSA0 CHK1B : MP access error/bus mode parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2C	BSA1::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(5) Byte28=25 : BSA1 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 25' : BSA1 CHK1B : MP access error/bus mode parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2C	BSA1::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local data parity error (00-07)	Local data parity error (10-17)	Local data parity error (20-27)	Local data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(6) Byte28=26 : MIC CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 26' : MIC CHK1B : internal counter timer error/LAN hold timeout/ XR wait timeout/XR bus access error/ L bus data parity error/arbiter data parity							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2C	BSA1::CK1BST0							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2D	MIC ::TIMER							
	Timer#0 parity error	Timer#1 parity error	Timer#2 parity error	Timer#3 parity error	Timer#4 parity error	Timer#5 parity error	Timer#6 parity error	Not used
2E	MIC ::ABTERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start timeout parity error	LIVEINS delay timer parity error	Transfer start timer parity error
2F	MIC ::XRADRPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR address parity error (24-27)	XR address parity error (30-37)
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(7) Byte28=27 : RCHK CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 27' : RCHK CHK1B : MP LM data error/XR register R/W address error/ LANC access error/refresh address error/L bus parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (EADP) CHK1B	XR1 (BSA0) CHK1B	XR2 (BSA1) CHK1B	XR3 CHK1B (0)	XR4 CHK1B (0)	XR5 CHK1B (0)	Not used	RCHK1 CHK1B
2B	RCHK::CHK1BSTS							
	i960→LM correctable error overflow		i960→XR Invalid read XR address	i960→XR Invalid write XR address	Not used	Not used	Not used	Not used
	Bank0	Bank1						
2C	RCHK::CHK1BSTS							
	LANC→LM correctable error overflow		LANC→LM uncorrectable error detected		LANC→XR invalid address	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
2D	RCHK::CHK1BSTS							
	Refresh address register parity error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2F	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local data parity error (00-07)	Local data parity error (10-17)	Local data parity error (20-27)	Local data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(8) Byte28=31 : i960 LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x' 31' : i960 LM correctable error 0 (address=400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (CHA CHK1B) Byte28-31 Detail

(9) Byte28 = 32 : i960 LM correctable error 1

	0	1	2	3	4	5	6	7
28	Subcode : x'32' : i960 LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) before correction							
2E	RCHK::ERORD							
	Data (1) before correction							
2F	RCHK::ERORD							
	Data (2) before correction							
30	RCHK::ERORD							
	Data (3) before correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (CHA CHK1B) Byte28-31 Detail

(10) Byte28 = 33 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x'33' : LANC LM correctable error 0 (address = 400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) before correction							
2E	RCHK::ERORD							
	Data (1) before correction							
2F	RCHK::ERORD							
	Data (2) before correction							
30	RCHK::ERORD							
	Data (3) before correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (CHA CHK1B) Byte28-31 Detail

(11) Byte28 = 34 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x'34' : LANC LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) before correction							
2E	RCHK::ERORD							
	Data (1) before correction							
2F	RCHK::ERORD							
	Data (2) before correction							
30	RCHK::ERORD							
	Data (3) before correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(12) Byte28=35 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x' 35' : LANC LM correctable error 0 (address=400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (CHA CHK1B) Byte28-31 Detail

(13) Byte28 = 36 : LANC LM correctable error 1

	0	1	2	3	4	5	6	7
28	Subcode : x'36' : LANC LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(14) Byte28=37 : i960 XR read address error

	0	1	2	3	4	5	6	7
28	Subcode : x' 37' : i960 XR read address error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(15) Byte28=38 : i960 XR write address error

	0	1	2	3	4	5	6	7
28	Subcode : x' 38' : i960 XR write address error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (CHA CHK1B) Byte28-31 Detail

(16) Byte28=39 : LANC XR access error

	0	1	2	3	4	5	6	7
28	Subcode : x' 39' : LANC XR access error							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27 = 8E & Byte34 = X0 & Byte28 = 4X/5X (DKA CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
01								
02								
03								
04								
05								
06	Log type							
07								
08	Failure classification							
09								
0A	System error code							
0B								
0C	JCB ID							
0D								
0E	REQ ID							
0F	24CMPAT	ECKD32	HOST RSP	SVP RSP	Processor ID			
10	VDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	Force log
11	VDEV number							
12								
13	CDEV number				RDEV number			
14	LDEV type							
15	PDEV type							
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x'8')				Message (x'E')			
28	Subcode (x'4X'/x'5X')							
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Module ID							
33	Routine ID							
34	Processor number				Message code (x'0')			
35	SSID (low) of self subsystem							
36	Sympton code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

Byte27=8 E & Byte34=X0 & Byte28=4X/5X (DKA CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	RCHK::ERADR							
	L-bus address (0) when error detected							
41	RCHK::ERADR							
	L-bus address () when error detected							
42	RCHK::ERADR							
	L-bus address (2) when error detected							
43	RCHK::ERADR							
	L-bus address (3) when error detected						(RSV)	(RSV)
44	RCHK::ERBYT							
	(RSV)	(RSV)	(RSV)	(RSV)	L-bus BE0-3 signal			
45	RCHK::ERORD							
	Data (0) befor correction when LM access error occurred							
46	RCHK::ERORD							
	Data (1) befor correction when LM access error occurred							
47	RCHK::ERORD							
	Data (2) befor correction when LM access error occurred							
48	RCHK::ERORD							
	Data (3) befor correction when LM access error occurred							
49	RCHK::ERORC							
	Check bit befor correction when LM access error occurred							
4A	RCHK::ERCRD							
	Data (0) after correction when LM access error occurred							
4B	RCHK::ERCRD							
	Data (1) after correction when LM access error occurred							
4C	RCHK::ERCRD							
	Data (2) after correction when LM access error occurred							
4D	RCHK::ERCRD							
	Data (3) after correction when LM access error occurred							
4E	RCHK::ERCRC							
	Check bit after correction when LM access error occurred							
4F	RCHK::ERSYD							
	Syndrom when LM access error occurred							

Byte27=8 E & Byte34=X0 & Byte28=4X/5X (DKA CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	RCHK::ERSTS0							
	i960 WR action unmatch	Not used	MIC READYI timeout	CHK1A cause detected	CHK1B cause detected	Scan LM/XR ACC ERR	Not used	Not used
51	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		i960→XR RD invalid ADR	i960→XR WR invalid ADR	Not used	Not used	Not used	Not used
	Bank0	Bank1						
52	RCHK::CHK1BSTS							
	i960→LM access CORREC ERR over		LANC→LM access UNCORR ERR detect		LANC→XR Invalid access	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
53	RCHK::CHK1BSTS							
	Refresh ADR REG parity ER	Not used	Not used	Not used	Not used	Not used	Not used	Not used
54	RCHK::SCANER							
	Scan→LM access UNCOR ERR detect		Not used	Scan→LM Out of LM area	Scan→XR Invalid RD XR ADR	Scan→XR Invalid WR XR ADR	Not used	Not used
	Bank0	Bank1						
55	RCHK::CECNT							
	CECNT00	CECNT01	CECNT02	CECNT03	CECNT04	CECNT05	CECNT06	CECNT07
56	RCHK::CECNT							
	CECNT10	CECNT11	CECNT12	CECNT13	CECNT14	CECNT15	CECNT16	CECNT17
57	MIC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B error	SMP/DRR CHK1B error	MIC CHK1B error
58	MIC::CHK1BSTS							
	XR0:EADP CHK1B error	XR1:BSA0 CHK1B error	XR2:BSA1 CHK1B error	XR3 CHK1B ERR (0)	XR4 CHK1B ERR (0)	XR5 CHK1B ERR (0)	Not used	RCHK1 CHK1B error
59	MIC::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity ER	Hard timer parity ER	Wait timer parity ER	Hold timer parity ER
5A	MIC::MICCHK1STS							
	LAN hold timer parity ER	Wait timeout	XR decoder ERR (29A)	XR decoder ERR (3B)	Arbiter data parity ER	XR address parity ER	Local bus data parity ER	Data parity error
5B	MIC::TIMERR							
	Timer#0 parity error	Timer#1 arity error	Timer#2 parity error	Timer#3 parity error	Timer#4 parity error	Timer#5 parity error	Timer#6 parity error	Not used
5C	MIC::ABTERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start tomeout	LIVEINS delay timer PE	Transfer start timer PE
5D	MIC::XRDBSPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR bus ADR P-ERR (24-27)	XR bus ADR P-ERR (30-37)
5E	MIC::LBUSPER							
	Not used	Not used	Not used	Not used	Local DT bus P-ERR (00-07)	Local DT bus P-ERR (10-17)	Local DT bus P-ERR (20-27)	Local DT bus P-ERR (30-37)
5F	MIC::XBUSPER							
	Not used	Not used	Not used	Not used	XR bus DT parity ER (00-07)	XR bus DT parity ER (10-17)	XR bus DT parity ER (20-27)	XR bus DT parity ER (30-37)

Byte27=8 E & Byte34=X0 & Byte28=4X/5X (DKA CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	RCHK::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	MIC arbiter CHK3	SMP CHK3
61	RCHK::RSTSTS							
	Not used	Not used	Micro CHK1B pending	Micro CHK1A pending	Micro MCNRST2 pending	Micro MCNRST1 pending	Micro MPRST pending	Micro MNTRST pending
62	RCHK::RSTSTS							
	Not used	Not used	Scan mode set pending	CHK1A pending	WCHK1 pending	SELRST pending	SYSRST pending	P/S on reset pending
63	RCHK::ARBCTL							
	LIVEINS count PE CHK test	XFR start timer PE CHK test	Sequencer reset	(RSV)	LIVEINS input SIG mask	CHK3 reset	DIAG mode	Arbier initiate
64	RCHK::CHK1B							
	Address byte 0 parity ER	Address byte 1 parity ER	Address byte 2 parity ER	Address byte 3 parity ER	Data byte 0 parity ER	Data byte 1 parity ER	Data byte 2 parity ER	Data byte 3 parity ER
65	RCHK::SMPERROR							
	Not used	Not used	Not used	Not used	Not used	Master CHK3 error	Slave CHK3 error	CHK1 error
66	SMP ::WAD							
	i960 address (0) for M bus access							
67	SMP ::WAD							
	i960 address (1) for M bus access							
68	SMP ::WAD							
	i960 address (2) for M bus access							
69	SMP ::WAD							
	i960 address (3) for M bus access							
6A	DRR ::STATUS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	CHK1B	Force transfer end	Pseud error
6B	DRR ::ESTA0							
	Unused register WR error	RD only register WR error	Side A A REG WR error	Side B B REG WR error	Address parity error	Byte access error	Input data parity ER	Output data parity ER
6C	DRR ::ESTA0							
	Addres decode error	Clock phase error	(RSV)	(RSV)	(RSV)	(RSV)	BSA0 CHK1	BSA1 CHK1
6D	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
6E	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
6F	DRR ::MODE4							
	Micro I/F ADR PRTY reversed	Micro I/F inout DT reversed	Micro I/F output DT reversed	S-BUS G-ID PRTY reversed	BSA I/F mode PRTY reversed	BSA I/F CMD ID P reversed	BSA I/F IN DT P reversed	BSA I/F OUT DT P reversed

Byte27=8 E & Byte34=X0 & Byte28=4X/5X (DKA CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	SCA0::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 parity ER	Write data 1 parity ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
71	SCA0::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
72	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
73	BSA1::CK1BSTS0							
	MP addres parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
74	SCA1::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
75	SCA1::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
76	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
77	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
78	SCA2::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
79	SCA2::CHKB							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
7A	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7B	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7C	SCA3::CHK1B							
	XR ADR (H) parity ER	XR ADR (L) parity ER	Write data 0 pariy ER	Write data 1 pariy ER	Read data 0 parity ER	Read data 1 parity ER	Address decode ERR(H)	Address decode ERR(L)
7D	SCA3::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
7E	BSA0::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
7F	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(1) Byte28=41 : DRR CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 41' : DRR CHK1B : XR bus access error/internal clock error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2C	DRR ::STATUS							
	CHK2 typical error	DRR data transfer CHK2	DRR control CHK2	BSA0 CHK2 (A/C/D)	BSA1 CHK2 (A/C/D)	CHK1B	Transfer forcibly terminate	Pseudo-failure occurred
2D	DRR ::ESTA0							
	Unused register write error	Read-dedicated register write error	A register write error side-A	B register write error side-B	Addres parity error	Byte access error	Input data parity error	Output data parity error
2E	DRR ::ESTA0							
	Address decode error	Clock phase error	(RSV)	(RSV)	(RSV)	(RSV)	BSA0 CHK1 error	BSA1 CHK1 error
2F	BSA0::CK1BSTS0							
	MP address parity error	MP wrote data(H) parity error	MP wrote data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
30	BSA1::CK1BSTS0							
	MP address parity error	MP wrote data(H) parity error	MP wrote data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
31	DRR ::MODE4							
	Address parity reversed	Input DT parity reversed	Output DT parity reversed	Grant/ID parity reversed	Mode SIG parity reversed	CMD ID parity reversed	Input DT parity reversed	Output DT parity reversed

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(2) Byte28=42 : SMP CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 42' : SMP CHK1B (XR bus parity error)							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	SMP :: CHK1B							
	Address byte 0 parity error	Address byte 1 parity error	Address byte 2 parity error	Address byte 3 parity error	Data byte 0 parity error	Data byte 1 parity error	Data byte 2 parity error	Data byte 3 parity error
2C	MIC ::TIMER							
	Timer#0 parity error	Timer#1 parity error	Timer#2 parity error	Timer#3 parity error	Timer#4 parity error	Timer#5 parity error	Timer#6 parity error	Not used
2D	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
2F	MIC ::XRADRPER							
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

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Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(3) Byte28=43 : SCA0 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 43' : SCA0 CHK1B : XR bus access error/internal clock error/micro access error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	SCA0::CHK1B							
	XR address(H) parity error	XR address(L) parity error	Write data0 parity error	Write data1 parity error	Read data0 parity error	Read data1 parity error	Address dacode error(H)	Address decode error(L)
2C	SCA0::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10-pahse Clock error	Not used	Not used	Not used
2D	BSA0::CK1BSTS0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Upper bus mode parity error	Not used	Not used	Not used
2E	BSA1::CK1BSTS0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Upper bus mode parity error	Not used	Not used	Not rsed
2F	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(4) Byte28=44 : SCA1 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 44' : SCA1 CHK1B : XR bus access error/internal clock error/micro access error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	SCA1:: CHK1B							
	XR address(H) parity error	XR address(L) parity error	Write data0 parity error	Write data1 parity error	Read data0 parity error	Read data1 parity error	Address dacode error(H)	Address decode error(L)
2C	SCA1::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
2D	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
2E	BSA1::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed
2F	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(5) Byte28=45 : SCA2 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 45' : SCA2 CHK1B : XR bus access error/internal clock error/micro access error							
29		MIC ::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A		MIC ::CHK1BSTS						
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B		SCA2::CHK1B						
	XR address(H) parity error	XR address(L) parity error	Write data0 parity error	Write data1 parity error	Read data0 parity error	Read data1 parity error	Address dacode error(H)	Address decode error(L)
2C		SCA2::CHK1B						
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
2D		BSA2::CK1BSTS0						
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
2E		BSA2::CK1BSTS0						
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed
2F		MIC ::MICCHK1STS						
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30		MIC ::MICCHK1STS						
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity parity error
31		MIC ::LBUSPER + RCHK::CHK1BSTS						
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(6) Byte28=46 : SCA3 CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 46' : SCA3 CHK1B : XR bus access error/internal clock error/micro access error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	SCA3::CHK1B							
	XR address(H) parity error	XR address(L) parity error	Write data0 parity error	Write data1 parity error	Read data0 parity error	Read data1 parity error	Address dacode error(H)	Address decode error(L)
2C	SCA3::CHK1B							
	8 phase clock error	Invalid address access	BSA0 CHK1	BSA1 CHK1	10 phase Clock error	Not used	Not used	Not used
2D	BSA3::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not used
2E	BSA3::CK1BSTS0							
	MP address parity ER	MP write data(H) parity ER	MP write data(L) parity ER	MP read data parity ER	Upper bus mode parity ER	Not used	Not used	Not rsed
2F	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
30	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decoder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(7) Byte28=47 : MIC CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 47' : MIC CHK1B : internal counter timer error/LAN hold timeout/XR wait timeout/XR bus access error/L bus data parity error/arbiter data parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	BSA0::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2C	BSA1::CK1BST0							
	MP address parity error	MP write data(H) parity error	MP write data(L) parity error	MP read data parity error	Higher bus mode parity error	Not used	Not used	Not used
2D	MIC ::TIMER							
	Timer#0 parity error	Timer#1 parity error	Timer#2 parity error	Timer#3 parity error	Timer#4 parity error	Timer#5 parity error	Timer#6 parity error	Not used
2E	MIC ::ABTERR							
	SQST08	SQST09	SQST10	Not used	Not used	Transfer start timeout parity error	LIVEINS delay timer parity error	Transfer start timer parity error
2F	MIC ::XRADRPER							
	Not used	Not used	Not used	Not used	Not used	Not used	XR address parity error (24-27)	XR address parity error (30-37)
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(8) Byte28=48 : RCHK CHK1B

	0	1	2	3	4	5	6	7
28	Subcode : x' 48' : RCHK CHK1B : MP LM data error/XR register R/W address error/LANC access error/refresh address error/L bus parity error							
29	MIC ::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA/DRR CHK1B	SMP CHK1B	MIC CHK1B
2A	MIC ::CHK1BSTS							
	XR0 (SCA#0) CHK1B	XR1 (SCA#1) CHK1B	XR2 (SCA#2) CHK1B	XR3 (SCA#3) CHK1B	XR4 CHK1B	XR5 CHK1B	Not used	RCHK1 CHK1B
2B	RCHK::CHK1BSTS							
	i960→LM correctable error overflow		i960→ Invalid read XR address	i960→ Invalid write XR address	Not used	Not used	Not used	Not used
	Bank0	Bank1						
2C	RCHK::CHK1BSTS							
	LANC→LM correctable error overflow		LANC→LM uncorrectable error		LANC→XR invalid address	Not used	Not used	Not used
	Bank0	Bank1	Bank0	Bank1				
2D	RCHK::CHK1BSTS							
	Refresh address register parity error	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MIC ::MICCHK1STS							
	Not used	Not used	Not used	Not used	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2F	MIC ::MICCHK1STS							
	LAN hold timeout	Wait timeout	XR decoder error (29A)	XR decorder error (3B)	Arbiter data parity error	XR address parity error	Local bus data parity error	Data parity error
30	MIC ::XBUSDTPER							
	Not used	Not used	Not used	Not used	XR bus data parity error (00-07)	XR bus data parity error (10-17)	XR bus data parity error (20-27)	XR bus data parity error (30-37)
31	MIC ::LBUSPER + RCHK::CHK1BSTS							
	Local bus data parity error (00-07)	Local bus data parity error (10-17)	Local bus data parity error (20-27)	Local bus data parity error (30-37)				

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(9) Byte28=51 : i960 LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x' 51' : i960 LM correctable error 0 (address=400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (DKA CHK1B) Byte28-31 Detail

(10) Byte28 = 52 : i960 LM correctable error 1

	0	1	2	3	4	5	6	7
28	Subcode : x'52' : i960 LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27=8 E (DKA CHK1B) Byte28-31 Detail

(11) Byte28=53 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x' 53' : LANC LM correctable error 0 (address=400-3FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							

Byte27 = 8E (DKA CHK1B) Byte28-31 Detail

(12) Byte28 = 54 : LANC LM correctable error 0

	0	1	2	3	4	5	6	7
28	Subcode : x'54' : LANC LM correctable error 1 (address = 40000-7FFFF)							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK::ERADR							
	Address (1) from L bus							
2B	RCHK::ERADR							
	Address (2) from L bus							
2C	RCHK::ERADR							
	Address (3) from L bus						(RSV)	(RSV)
2D	RCHK::ERORD							
	Data (0) befor correction							
2E	RCHK::ERORD							
	Data (1) befor correction							
2F	RCHK::ERORD							
	Data (2) befor correction							
30	RCHK::ERORD							
	Data (3) befor correction							
31	RCHK::ERORC							
	Check bit bifore correction							