SSBLOG SECTION

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Contents

19.1 Introduction SSBLOG01-10
19.2 Classification of Internal SSB SSBLOG02-10
19.3 Common information description SSBLOG03-10
19.4 Host SSB information and internal SSB format-depended information description SSBLOG04-10
19.4.1 24-byte type SSB SSBLOG04-10
19.4.2 32-byte type SSB SSBLOG04-40
19.4.3 SCSI host report format SSB SSBLOG04-60
19.5 Format-depended information description SSBLOG05-10
• Byte27 = 0X (X ≠ 8/A:System/program Check) SSBLOG05-20
• Byte27 = 08 (Reset Notification) SSBLOG05-50
• Byte27 = 0A (Bus out parity check/Overrun on LCP interface (Byte3A:b4 = 1)) SSBLOG05-70
• Byte27 = 10 (Intervention required) SSBLOG05-80
• Byte27 = 1X (Drive report error) SSBLOG05-100
• Byte27 = 3F (Reset Allegiance) SSBLOG05-120
• Byte27 = 4X (Data check) SSBLOG05-140
• Byte27 = 6X (Statistics) SSBLOG05-170
• Byte27 = 74 & Byte40:Bit7 = 0 (FPC Detected Failure:DSP) SSBLOG05-180
• Byte27 = 74 & Byte40:Bit7 = 1 (FPC Detected Failure:FBP) SSBLOG05-200
• Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memory Failure) SSBLOG05-220
• Byte27 = 81 (Shared Memory Failure) Byte28-31 Detail SSBLOG05-240
• Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)(Byte29=x'01'lx'02') SSBLOG05-250
• Byte27 = 81 Byte40-7F(X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') SSBLOG05-290
• Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') SSBLOG05-330
• Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') SSBLOG05-370
• Byte27 = 81 & Byte34:b4-7 = 3 (CHK3 Reset) SSBLOG05-410
• Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) SSBLOG05-430
• Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Receive Error) SSBLOG05-450
• Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) SSBLOG05-470
• Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) SSBLOG05-490
• Byte27 = 88 & Byte34:b4-7 = A & Byte28 ≠ 01/02/0C/0E (LCP Failure:Others) SSBLOG05-510
• Byte27 = 89 & Byte0D Bit2 = 0 (ESCON CHA CHK2) SSBLOG05-530
• Byte27 = 89 & Byte0D Bit2 ≠ 0 (FIBRE CHA CHK2) SSBLOG05-540
• Byte27 = 89 (CHA CHK2) Byte28-31 Detail SSBLOG05-550
• Byte27 = 89 (CHA CHK2) Byte40-7F Detail SSBLOG05-610
• Byte27 = 8A (FCA CHK2) SSBLOG05-910
• Byte27 = 8A (FCA CHK2) Byte28-31 Detail SSBLOG05-920
• Byte27 = 8A (FCA CHK2) Byte40-7F Detail SSBLOG05-930
• Byte27 = 8B (DRR CHK2) SSBLOG05-1290
• Byte27 = 8B (DRR CHK2) Byte28-31 Detail SSBLOG05-1300
• Byte27 = 8B (DRR CHK2) Byte40-7F Detail SSBLOG05-1420
• Byte27 = 8C (SVP Failure) SSBLOG05-1540
• Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail SSBLOG05-1560
• Byte27 = 8D (Power Failure) SSBLOG05-1630
• Byte27 = 8D (DKU/HDU Power Failure) Hard information SSBLOG05-1650
• Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) SSBLOG05-1670
• Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) SSBLOG05-1740
• Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) SSBLOG05-1800
• Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) SSBLOG05-1860
• Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71 (CHK1B) SSBLOG05-1950
• Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) SSBLOG05-2040

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- Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) SSBLOG05-2100
- Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74 (CHK1B) SSBLOG05-2160
- Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75 (CHK1B) SSBLOG05-2260
- Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B) SSBLOG05-2350
- Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67 (CHK1B) SSBLOG05-2420
- Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) SSBLOG05-2481
- Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) SSBLOG05-2490
- Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (Microprogram detected WCHK1) SSBLOG05-2575
- Byte27 = 8E & Byte34 = X0 & Byte28 = F1 (Microprogram CHK1A) SSBLOG05-2580
- Byte27 = 8E (Microprogram CHK1A) Byte28-31 Detail SSBLOG05-2590
- Byte27 = 8E & Byte34:bit4-7 = 1 (Selective Reset) SSBLOG05-2600
- Byte27 = 8E & Byte34:bit4-7 = 3 (Wait SENSE Timeout) SSBLOG05-2630
- Byte27 = 8E & Byte34:bit4-7 = 5 (CHK1B Reset) SSBLOG05-2650
- Byte27 = 8E & Byte34:bit4-7 = 6 (DKC Internal Reset) SSBLOG05-2670
- Byte27 = 8E & Byte34:bit4-7 = 7 (LCP Internal Reset) SSBLOG05-2690
- Byte27 = 8E & Byte34:bit4-7 = 8 (Force Reset) SSBLOG05-2710
- Byte27 = 8E & Byte34:bit4-7 = 9 (Logical Inconsistency Reset) SSBLOG05-2730
- Byte27 = 8F (Logical Inconsistency) SSBLOG05-2750
- Byte27 = 9F (Trace data/Log data) SSBLOG05-2770
- Byte27 = EC (Environment Monitor Detected DKC Failure) SSBLOG05-2790
- Byte27 = EE (Environment Monitor Detected DKU Failure) SSBLOG05-2811
- Byte27 = F0 (Operation terminated) SSBLOG05-2820
- Byte27 = F1 (Micro-program Detected Cache Failure) SSBLOG05-2840
- Byte27 = F2 (CACHE CHK2) SSBLOG05-2860
- Byte27 = F2 (CACHE CHK2) Byte28-31 Detail SSBLOG05-2870
- Byte27 = F2 (CACHE CHK2) Byte40-7F Detail SSBLOG05-2880
- Byte27 = F6 (CFW Access not Authorized) SSBLOG05-3060
- Byte27 = FA (NVS Terminated) SSBLOG05-3080
- Byte27 = FB (HRC/HODM Pair suspend) SSBLOG05-3100
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning : Error handling support) SSBLOG05-3120
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning : Error handling support) Hardware detail information SSBLOG05-3130
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type1 ..... SSBLOG05-3240
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type2 ..... SSBLOG05-3280
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type3 ..... SSBLOG05-3320
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type4 ..... SSBLOG05-3360
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type5 ..... SSBLOG05-3400
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type6 ..... SSBLOG05-3440
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type7 ..... SSBLOG05-3480
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type8 ..... SSBLOG05-3520
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type9 ..... SSBLOG05-3560
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type10 ..... SSBLOG05-3600
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type11 ..... SSBLOG05-3631

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- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type12 ..... SSBLOG05-3635
- Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error/Warning) Byte 40-7F Common detail information : Type13 ..... SSBLOG05-3639
- Byte0D : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) SSBLOG05-3640
- Byte0D : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception: Incomplete Domain)..... SSBLOG05-3660
- Byte0D : Bit1 = 1 & Byte36-37=4XXX (Data exception) SSBLOG05-3680
- Byte36 = 6F (Subsystem Information) SSBLOG05-3710
- Byte36:Bit0-3=D & Byte26:Bit4-7=1 & Byte27:Bit0-2=7 & Byte40:Bit7=0 (FPC Detected Failure:DSP)..... SSBLOG05-3720
- Byte36:Bit0-3=D & Byte26:Bit4-7=1 & Byte27:Bit0-2=7 & Byte40:Bit7=1 (FPC Detected Failure:FBP)..... SSBLOG05-3740
- Byte36:Bit0-3= D & Byte26:Bit4-7=1 & Byte27:Bit0-2=0 (Drive Detected Failure:DSP)..... SSBLOG05-3770
- Byte36:Bit0-3 = E & Byte2C:bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP) SSBLOG05-3790
- Byte36 = E0 & Byte2C = 5X/6X & Byte20:b3 =1 (LDEV blockade/Pin VOL detected/Write inhibited) SSBLOG05-3910
- Byte36-37 = E210 & Byte2C = 5X/6X & Byte20:b1 = 1 (Intervention requested:LDEV not ready) SSBLOG05-3930
- Byte26:b4-7 = F & Byte3C = F1 (DKC SIM) SSBLOG05-3950
- Byte26:b4-7 = F & Byte3C = F2 (CACHE SIM) SSBLOG05-3980
- Byte26:b4-7 = F & Byte3C = FE (Device SIM) SSBLOG05-4010
- Byte26:b4-7 = F & Byte3C = FF (Media SIM) SSBLOG05-4030
- SIM Reference Codes Detected by the Processor SSBLOG05-4050
- SIM Reference Codes Detected by the Processor for HRC/HODM SSBLOG05-4120
- SIM Reference Codes Detected by the Processor for HRC/HORC (Asynchronous) SSBLOG05-4140
- SIM Reference Codes Detected by the Processor for HMRCF/HOMRCF/HIHSM/HXRC/HRCA SSBLOG05-4160
- SIM Reference Codes Detected by the Processor for DCR SSBLOG05-4160

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1 Introduction

The internal SSB (SSB Log) information is presented as either 24-byte compatibility SSB format or ECKD 32-byte SSB format. The 24-byte SSB is used for DKC and the 32-byte SSB is used for DKU.

The internal SSB is divided into the following sections:

- Internal SSB common information
  This information is used for SSB management, and same for all formats.

- External SSB information presented to host.
  This is 32 bytes sense information presented to host as SSB.

- Format-dependent information
  This is auxiliary information for error analysis.

See Fig.1-1 and Fig.1-2.

Note : The byte offset in SSB logs is described in hexadecimal number.
This section is corresponding to SSB log on SVP.
If you want to know about SSB which was reported to host, you should see SSB section.

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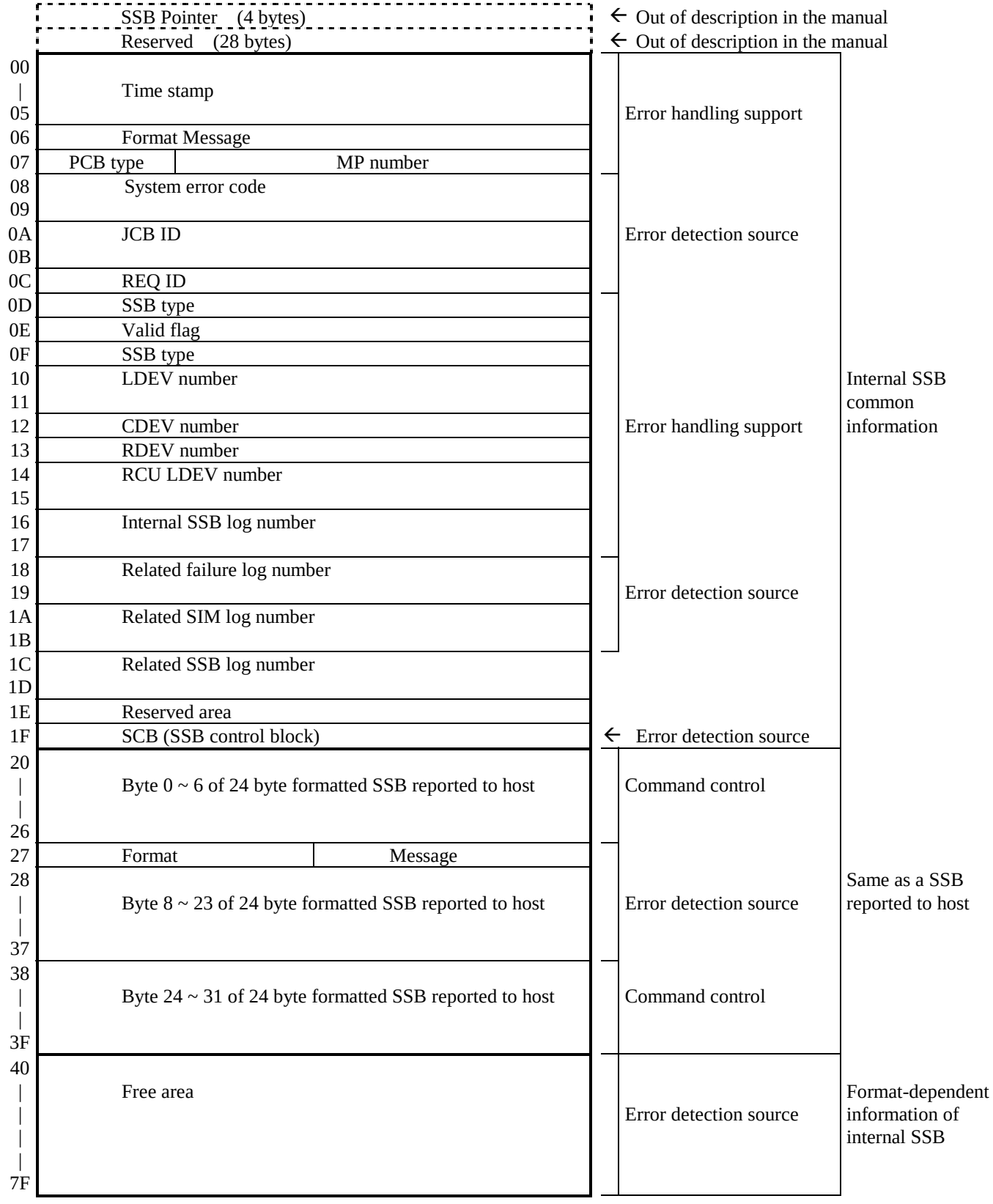

Fig.1-1 Outline of 24-byte Format Internal SSB

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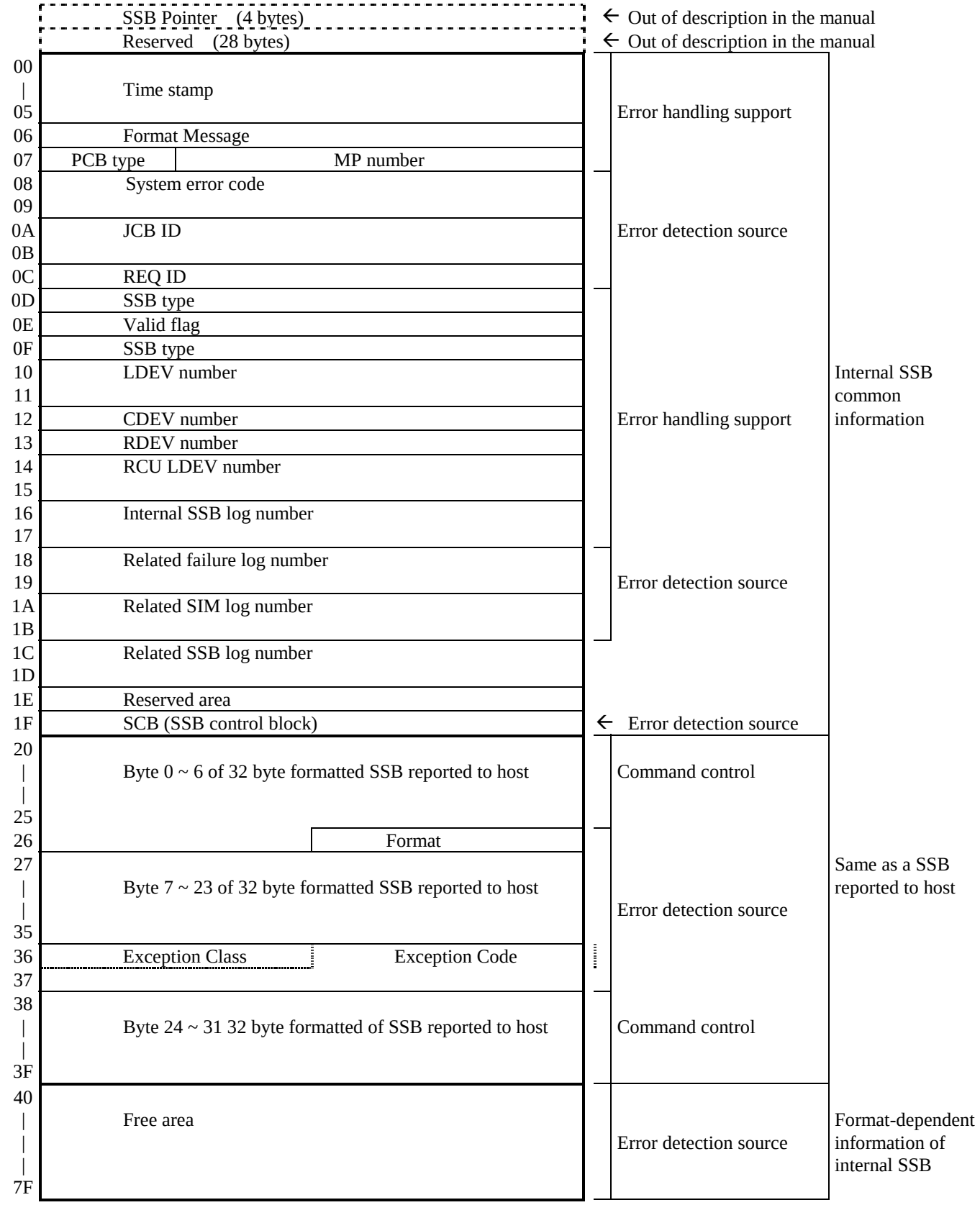

Fig.1-2 Outline of 32-byte Format Internal SSB

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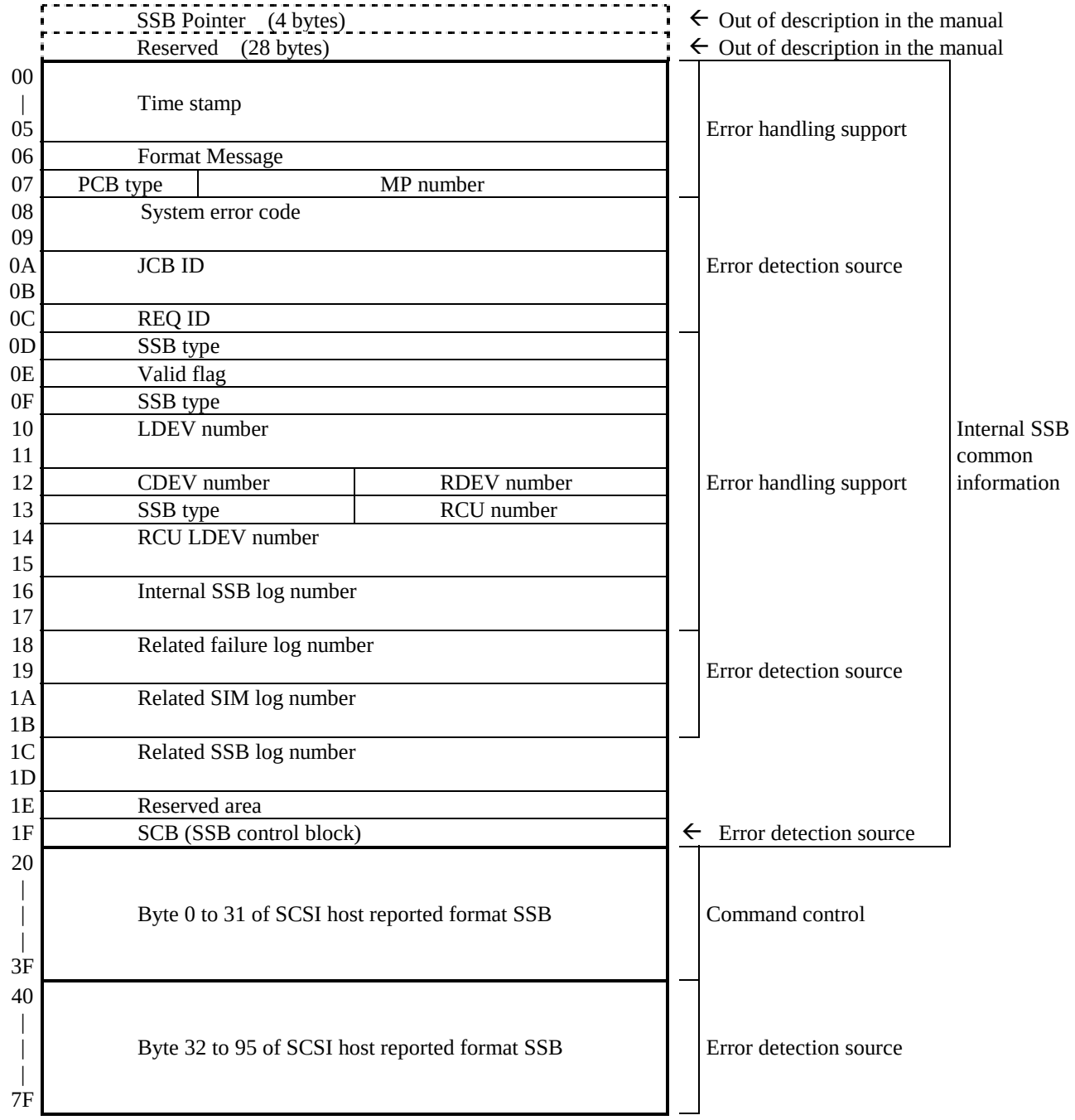

Fig.1-3 Overview of SCSI Host Report Format Internal SSB

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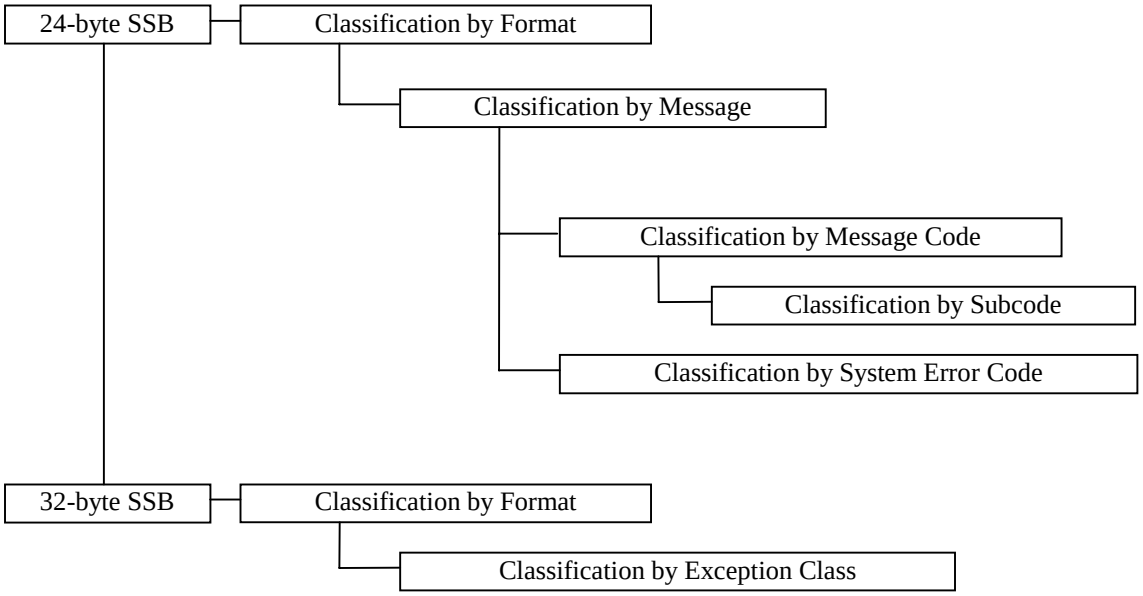
2 Classification of Internal SSB

The internal SSB is classified as the following figure, and Fig.2-1 for detail.



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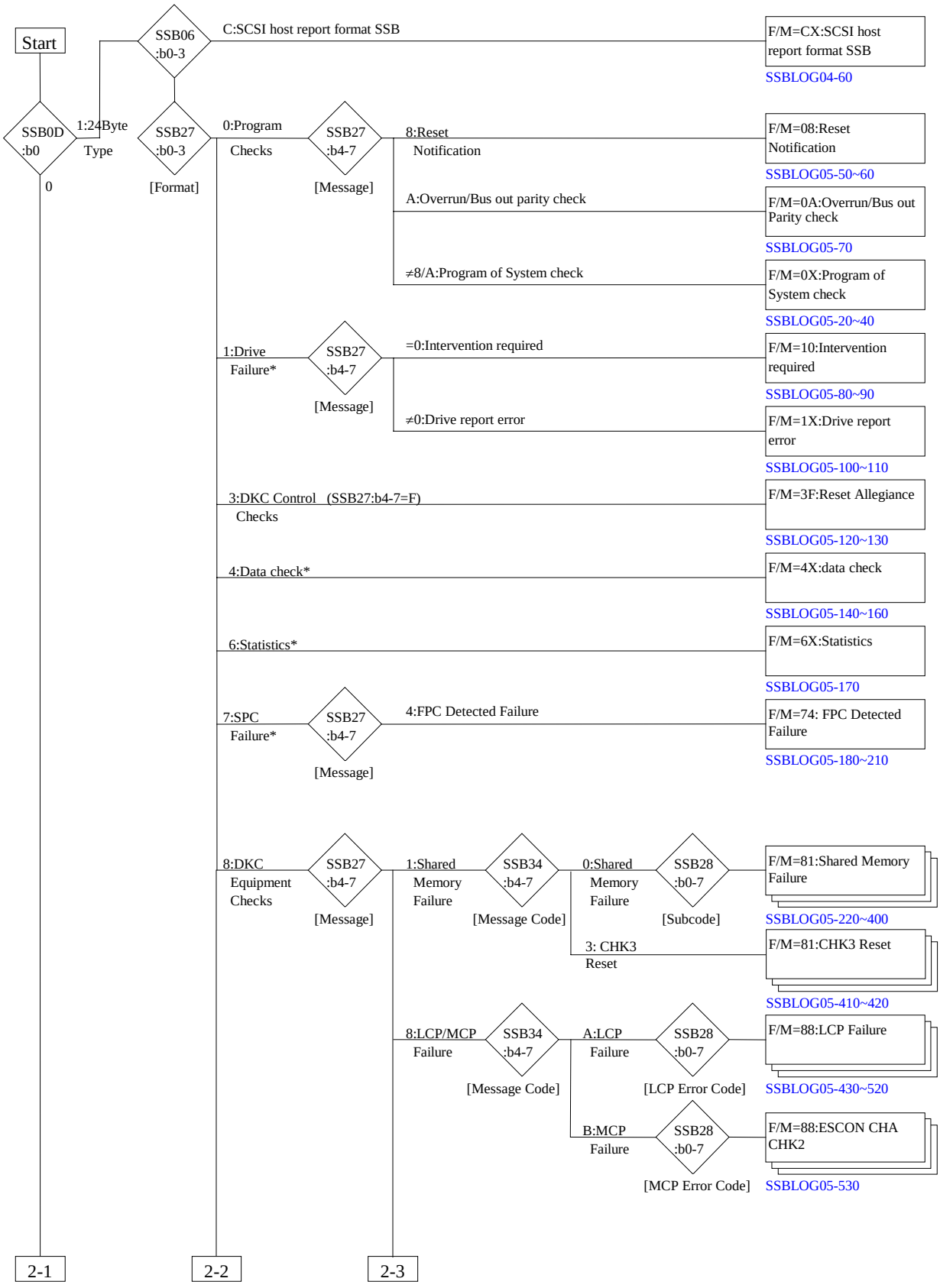

* : For DKU86I (IBM 3380 emulation mode) only.

Fig.2-1 Search method for SSB tables (1/5)

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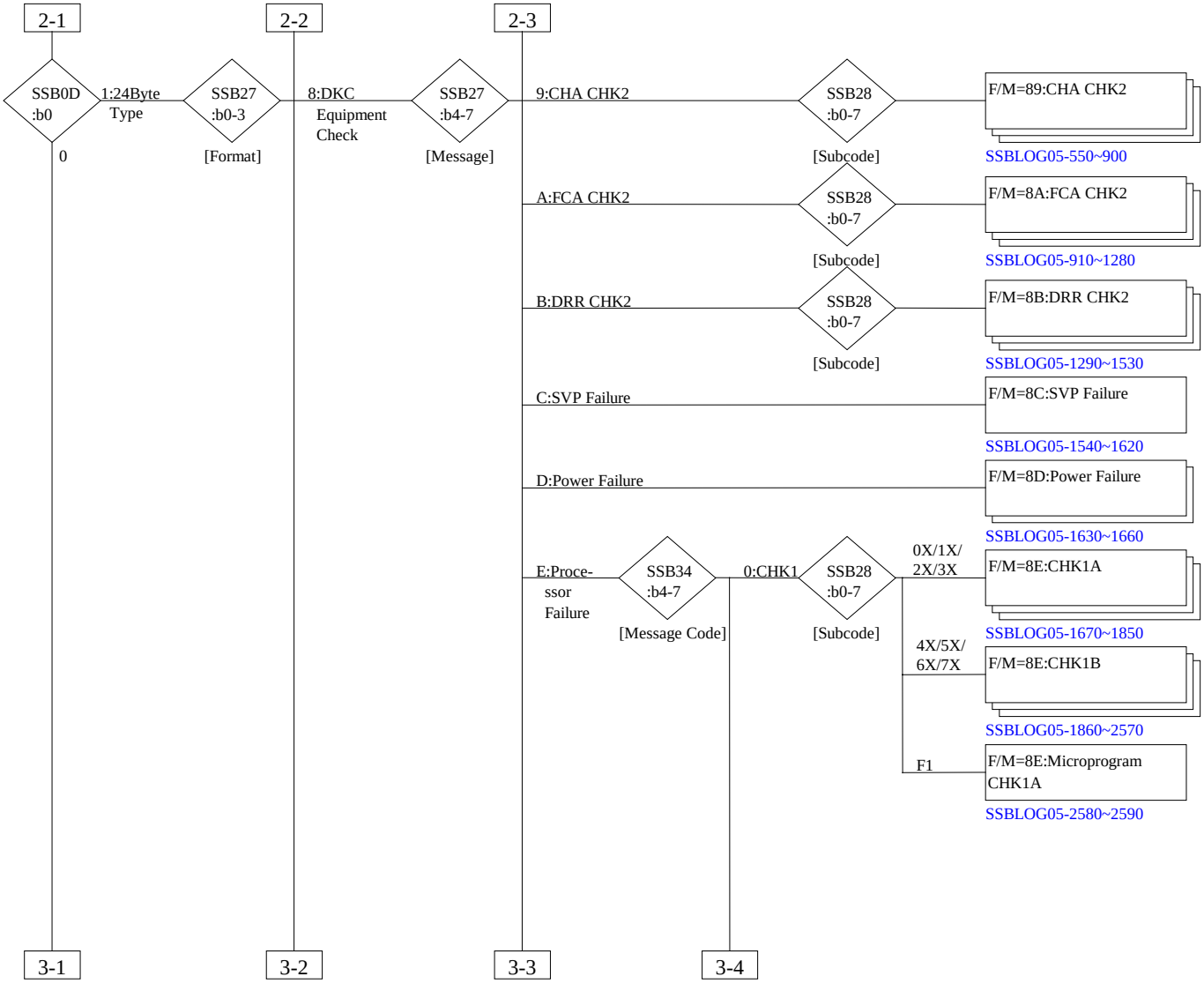

Fig.2-1 Search method for SSB tables (2/5)

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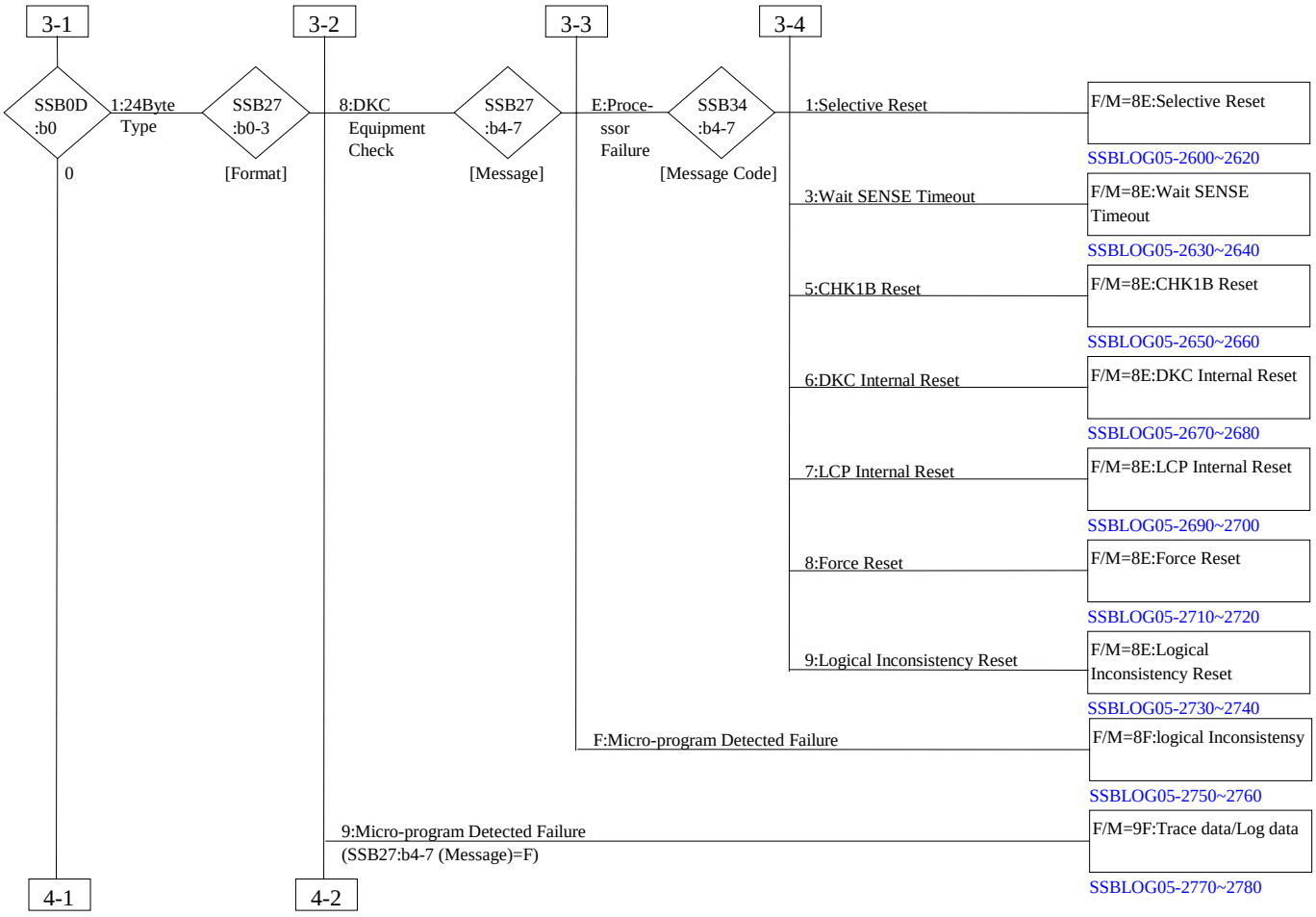

Fig.2-1 Search method for SSB tables (3/5)

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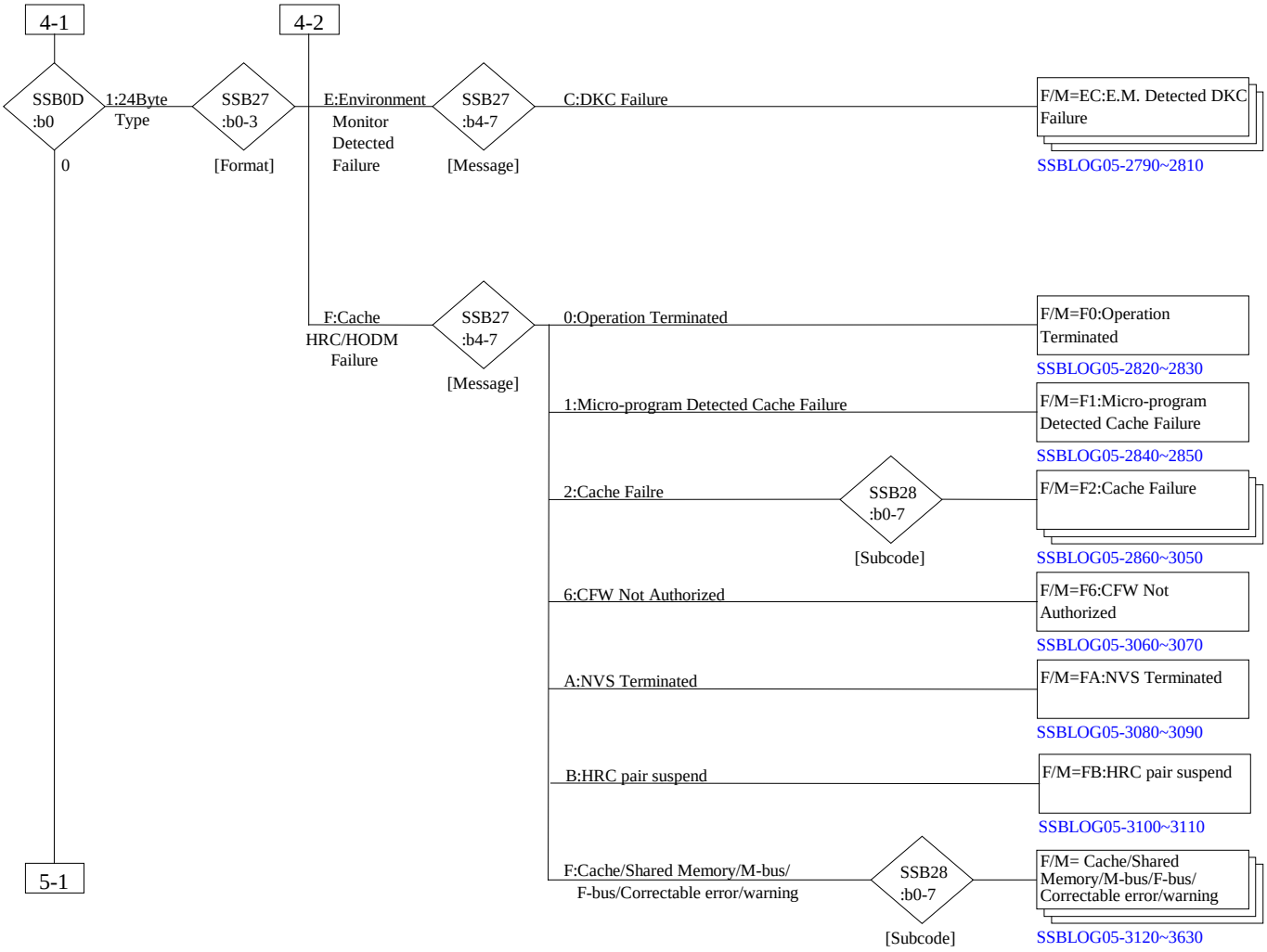

Fig.2-1 Search method for SSB tables (4/5)

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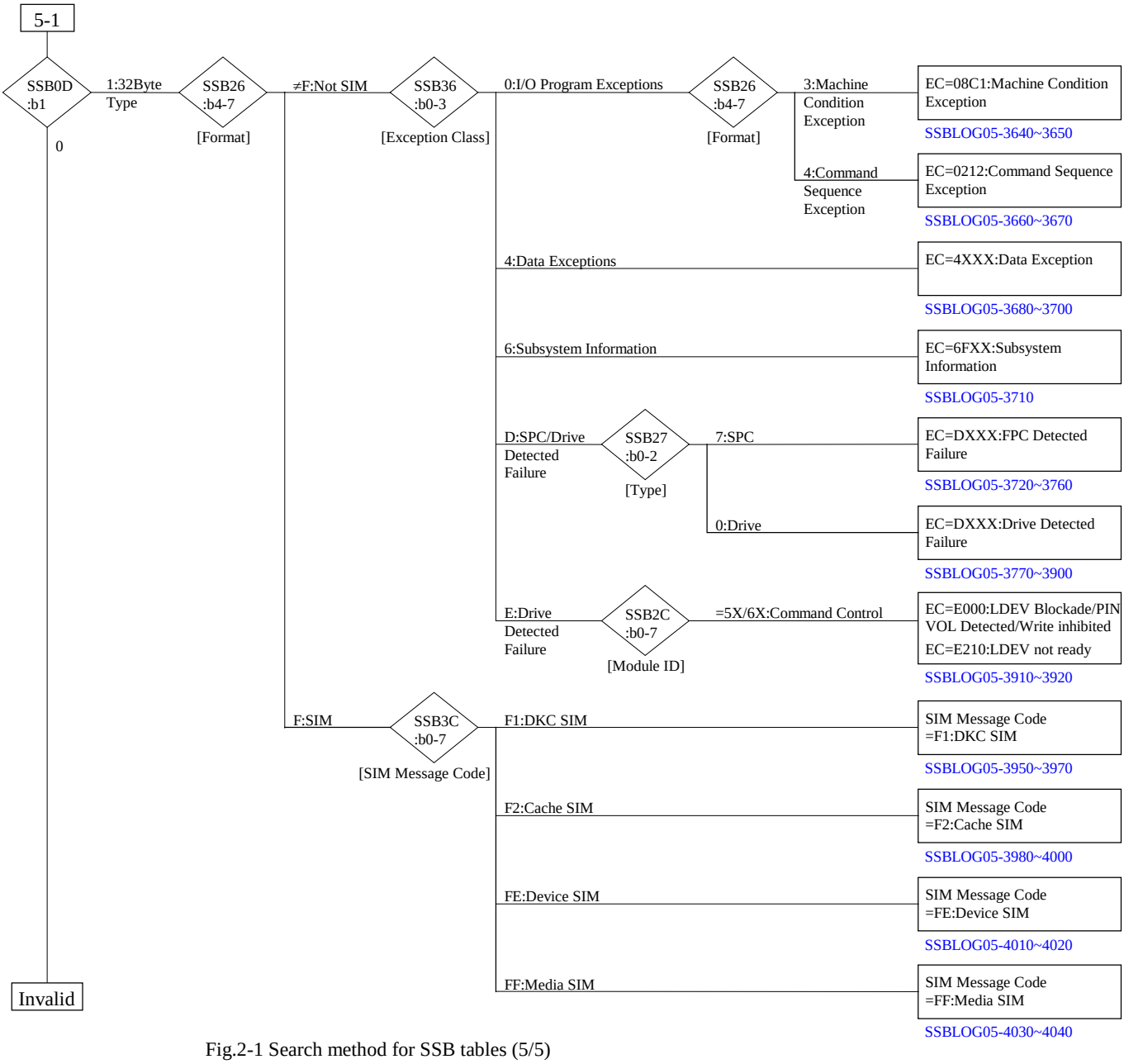

Fig.2-1 Search method for SSB tables (5/5)

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3 Common information description

	0	1	2	3	4	5	6	7
00	Time Stamp							
01								
02								
03								
04								
05								
06	Format Message							
07	PCB Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host RSP	SVP RSP	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Rerserved							
1F	SCB (SSB Control Block)							
20	Host SSB Information							
|								
3F								
40	Internal SSB Format-Dependent Information							
7F								

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Common Information (1/2)

Byte	Bit	Meaning	Setting	Remarks
00 - 05		Time stamp The time error occurred	Error handling support	
06		Format Message	Error handling support	
07		Information of the processor detected this error	Error handling support	
	0 - 1	PCB type x‘1’ : CHA x‘2’ : DKA x‘3’ : CHS		
	2 - 7	Processor number (Internal ID) x‘00’ - x‘07’ : CHA0 - CHA7 x‘08’ - x‘0F’ : DKA0 - DKA7		
08 - 09		System error code	Error detection source	
	0 - 7	Module ID See “Module ID” table.		
	8 - 15	Routine ID		
0A - 0B		JCB ID	Error detection source	
0C		REQ ID	Error detection source	
0D		Valid flag	Error handling support	
	0	24Byte type flag 0:Invalid 1:24Byte type SSB		
	1	32Byte type flag 0:Invalid 1:32Byte type SSB		
	2	Flag for SCSI host processor detected the error 0:SSB detected by CHA and DKA 1:SSB detected by CHS		
	3	Remote copy flag 0:Invalid 1:Remote copy valid		
	4	Separately stored log flag 0:General log 1:Separately stored log		
	5	Host report flag 0:Pending 1:Reported		
	6	SVP report flag 0:Pending 1:Reported		
	7	Forcible log flag 0:Normal 1:Forcibly ejected log		

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Common Information (2/2)

Byte	Bit	Meaning		
0E		Valid flag	Error handling support	
	0	LDEV number valid or invalid 0:Invalid 1:Valid		
	1	PDEV number valid or invalid 0:Invalid 1:Valid		
	2	SSB number valid or invalid 0:Invalid 1:Valid		
	3	Related failure log number valid or invalid 0:Invalid 1:Valid		
	4	Related SIM log number valid or invalid 0:Invalid 1:Valid		
	5	Related SSB log number valid or invalid 0:Invalid 1:Valid		
	6 - 7	Reserved		
0F		Valid flag	Error handling support	
	0	SIM reception flag 0:First log / Log after the host reported 1:Log after SIM was received		
	1 - 7	Reserved		
10 - 11		LDEV number	Error handling support	
12		PDEV number	Error handling support	
	0 - 3	CDEV number		
	4 - 7	RDEV number		
13		HRC information	Error handling support	
	0	Reserved		
	1	RCU SIM flag 0:Invalid 1:RCU SIM valid		
	2 - 3	Reserved		
	4 - 7	RCU number		
14 - 15		RCU LDEV number		
16 - 17		Internal SSB log number		
18 - 19		Related Failure log number		
1A - 1B		Related SIM log number		
1C - 1D		Related SSB log number		
1E		Reserved area		
1F		SSB control block Use when assemble BASIC SSB of Host SSB. See "SSB Key Code" table.		

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Module ID (1/3)

Module ID	Module Name		Remarks
00	Initializer		
01	Power Off Process		
02	CUDG		
10	Job Management		
11	Synchronous Management		
12	Processor Communication		
13	Cache Control		
14	Resource Management		
15	Configuration Control		
16	Reset		
17	SVP Management		
18	Configuration Control(RAID)		
19	Configuration Control(Drive Recovery)		
30	Standard Function		
31	SVP Function		
32	Error Procedure Aid		
34	Error Procedure Aid		
35	Error Procedure Aid		
40	CHA Kernel	CHA Monitor	
41		CHA Initiator	
42		CHA Terminator	
43		CHA Common Function	
50	Command Control	Command Chain Initiate(Command Main)	
51		Command Chain Terminate(Command Main)	
52		Command Execution Status Analyze	
53		Command Execution Channel Interface Control	
54		Channel Server Common Process 1	
55		Channel Server Common Process 2	
56		Channel Server Common Process 3	
57		Channel Server Common Process 4	
58		Channel Server Transfer Process 1	
59		Channel Server Transfer Process 2	
5A		Read/Write Common Process	
5B		Subsystem Command Common Process	
5C		Channel Server Asynchronous Control 1	
5D		Channel Server Asynchronous Control 2	
5E		Channel Server Command Queuing Control	
5F		Channel Server Job FRR	
60		Read Command Process 1	
61		Read Command Process 2	
62		Read Command Process 3	
63		Read Command Process 4	
64		Read Command Process 5	
65		Read Command Process 6	
66		Write Command Process 1	
67		Write Command Process 2	
68		Write Command Process 3	
69		Write Command Process 4	
6A		Write Command Process 5	
6B		Write Command Process 6	
6D		Control Command Process 1	
6E		Control Command Process 2	
6F		Search Command Process	

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Module ID (2/3)

Module ID	Module Name		Remarks
70	Command Control	Path Control Command Process	
71		Sense & Miscellaneous Command Process	
72		Diagnostic Command Process	
73		Subsystem Command Process 1	
74		Subsystem Command Process 2	
75		Subsystem Command Process 3	
78		Channel Interface Link Level Frame Control	
79		Channel Interface Device Level Frame Control	
7A		Channel Interface Control Common	
7B		LDEV Format	
7C		Concurrent Copy Process	
7D		Concurrent Copy Process	
7E		Concurrent Copy Process	
7F		Channel Server WDCP/DUMP(M specified)	
80	DKA Kernel	DKA Monitor	
81		DKA Initiator	
82		DKA Terminator	
90	Staging Destaging	Staging	
91		LDEV Destaging	
92		PDEV Destaging	
93	Drive Recovery		
94	Offline Monitor		
95	Physical Device Maintenance		
98	RAID Synchrinous Type		
99	RAID LDEV Destaging		
9A	RAID PDEV Destaging		
9B	RAID Drive Recovery		
9C	RAID external provided		
9D	RAID 0 Destaging		
9E	RAID 0 Error/Merge		
9F	RAID Slot Falure Status Operation		
A0	SCSI Control		
A1	DRR Control		
A2	SVP Command Execution Process		
A3	Test Initiator		
A4	SCSI Control		
A5	Offline Monitor		
A6	Physical Drive Maintenance		
A7	SCSI Control		
A8	DRR Control		
AE	SCSI Control		
C0	HRC/HODM CHL/SVP I/F		
C1	HRC/HODM Remote copy monitor		
C2	HRC/HODM Configuration control		
C3	HRC/HODM Common copy procedure		
C4	HRC Remote copy procedure		
C5	HODM Migration copy procedure		
C6	HRC/HODM channel server procedure		
C7	HRC/HODM Remote I/O manager		
C8	HRC/HODM Remote I/O 1		
C9	HRC/HODM Remote I/O 2		
CA	HRC/HODM path control		
CF	HRC/HODM Service SIM log		

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Module ID (3/3)

Module ID	Module Name		Remarks
D0	Multiplatform Comand Control	Command Main	
D1		Transfer Process/SSB Function	
D2		Read/Write Command	
D3		Read/Write Common Process	
D4		Control/Diagnostic Command	
D8	Multiplatform SCP Control	SCP Control 1	
D9		SCP Control 2	
DA		SCP Control 3	
DC	Multiplatform Kernel	Command Queuing Procedure	
DD		CHS Scan	
DE		CHS Initiator	
DF		CHS Terminator	
E0	RCP initialize / Reset / Sequence control		
E1	RCP idle scan / Starting process		
E2	RCP link level process		
E3	RCP device level process		
E4	RCP error process / Received frame check / physical service		
E5	Communication between RCP and CHP / Path control / Clock timer control / Frame transmission and reception		
E6	RCP sequence process / Device level process		

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SSB Key Code (1/2)

Code	Basic SSB	Meaning	Remarks
00	000000	Dummy SSB	
01	800000	Command reject (A program error or invalid link between BAD and ALT)	
02	400000	Intervention required (An addressed device is offline or not connect)	
03	200000	Bus out check (Channel bus out parity error)	
04	100000	Equipment check (Equipment check in subsystem)	
05	080000	Data check (Uncorrectable:retry failed or retry inhibited)	
06	040000	Overrun (command retry failed when service overrun occurred)	
07	004000	Invalid track format (Track capacity over or track format error)	
08	002000	End of cylinder (A multi track operation outside LOCATE domain)	
09	000800	No record found	
0A	000400	File protected (A seek or multi track operation violates the file mask or extent)	
0B	100200	Equipment check and write inhibited (A write command on the write inhibited path by a DIAG CTL command)	
0C	080040	Data check and correctable (The retry succeeded for data check in PCI fetch mode)	
0D	000020	First log mode error	Not used
0E	800400	Command rejected and file protected (A multi track operation outside primary track)	
0F	800200	Command reject and write inhibited	Not used
10	108000	Equipment check and permanent error) (A retry failed for the equipment check)	
11	088000	Data check and permanent error) (A retry failed for the data check)	
12	009010	SIM (DKC SIM or Cache SIM)	
13	000000	Reserved	
14	000104	Imprecise ending (This error is for a previously completed CCW)	
15	800104	Command reject and imprecise ending	
16	400104	Intervention required and imprecise ending	
17	200104	Bus out check and imprecise ending	
18	100104	Equipment check and imprecise ending	
19	080104	Data check and imprecise ending	
1A	040104	Overrun and imprecise ending	
1B	004104	Invalid track format and imprecise ending	
1C	002104	End of cylinder and imprecise ending	
1D	000904	No record found and imprecise ending	
1E	000504	File protected and imprecise ending	
1F	100304	Equipment check and write inhibited and imprecise ending	

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SSB Key Code (2/2)

Code	Basic SSB	Meaning	Remarks
20	080144	Equipment check and correctable and imprecise ending	
21	000124	First log mode error and imprecise ending	Not used
22	800504	Command reject and file protected and imprecise ending	
23	800304	Command reject and write inhibited and imprecise ending	
24	108104	Equipment check and permanent error and imprecise ending	
25	088104	Data check and permanent error and imprecise ending	
26	009114	SIM and imprecise ending	Not used
27	000000	Reserved	
28	808000	Command reject and permanent error	
29	00C000	Permanent error and invalid track format	
2A	008800	Permanent error and request inhibit write	
2B	088200	Data check and permanent error and write protected	
2C	000000	Reserved	
2D	000000	Reserved	
2E	000000	Reserved	
2F	000000	Reserved	
30	000000	Reserved	
31	000000	Reserved	
32	010000	Incomplete domain (Received commands < LOCATE command parameter)	
33	804000	Command reject and invalid track format (A TLF mismatch in CKD conversion mode)	
34	000000	Reserved	
35	100010	Equipment check and environmental data present (Status change pending)	
36	800010	Command reject and environmental data present	
37	000000	Reserved	
38	000000	Reserved	
39	000000	Reserved	
3A	000000	Reserved	
3B	000000	Reserved	
3C	000000	Reserved	
3D	000000	Reserved	
3E	000000	Reserved	
3F	000000	Reserved	

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4 Host SSB information and internal SSB format-depended information description

4.1 24-byte type SSB

	0	1	2	3	4	5	6	7	
00	Internal SSB common Information								
1F									
20	Command reject	Intervention REQ	Bus out check	Equipment check	Data check	Overrun	Unused	Incomplete domain	Basic SSB
21	Permanent error	Invalid track FMT	End of cylinder	Operator message	No Record found	File protect	Write inhibit	Imprecise ending	
22	Write INH request	Correctable	1st log mode ERR	Environmen-tal DAT	Unused	Imprecise ending	Not used	Not used	
23	Count								
24	Device address								
25	Cylinder address(low)								
26	Cylinder address(high)				Head address				
27	Format (See next page)				Message (See next page)				
28	Host SSB Format-depended Information								
37									
38	Log and message control								
39	Program action code								
3A	Dual frame	EDCC mode (1)	Duplex pair (0)	S-volume ERR (0)	Async operation	Serial channel	Report output	Permanent path ERR	*
3B	24Byte SSB (1)	DEV ADR valid	TRK ADR valid	Not used	3380 TRK COMPT(0)	Not used	Storage path number		
3C	Not used								
3D	Cylinder address								
3E									
3F	Head address								
40	Internal SSB Format-depended Information								
7F									

*:Configuration information

**:Byte 20-27 and byte 38-3F are not certain until DKC reports SSB to Host. So if you want to know the detail, please refer to SSB section.

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Format and Message

(1/2)

Format	Message	Meaning	
0	0	No message	
	1	Invalid command	
	2	Invalid sequence	
	3	Data short	
	4	Invalid data	
	5	Violate file mask	
	6	Channel disconnect retry.	
	7	Invalid retry command	
	8	System reset	
	9	Not used	
	A	Bus of parity check/Overrun	
	B	Invalid link between bad track and alternate track.	
	C	Not used	
	D	Not used	
	E	Invalid command to secondary volume	
	F	Invalid status	
1	0	Intervention required	For DKU86I (IBM 3380 emulation mode) only
	1	Not used	
	2	Drive not ready	
	3	Not used	
	4	Drive report error	
	5~F	Not used	
3	0~E	Not used	
	F	Reset allegiance	
4	0	Data check in HA field	For DKU86I (IBM 3380 emulation mode) only
	1	Data check in C field	
	2	Data check in K field	
	3	Data check in D field	
	4	Not used	
	5	PA error	
	6~F	Not used	
6	0~7	Statistics	
	8~F	Not used	
7	0~3	Not used	
	4	SPC report error	
	5~8	Not used	
	9	SCSI bus parity error	
	A~F	Not used	
8	0	Not used	
	1	Shared memory failure	
	2~7	Not used	
	8	LCP failure or MCP failure	
	9	Host adaptor CHK2	
	A	Disk adaptor CHK2	
	B	DRR failure	
	C	SVP failure	
	D	Power failure	
	E	Processor failure	
	F	Micro-program detected error (Logical Inconsistency)	
9	0~E	Not used	
	F	Micro-program detected error (Trace data/Log data)	
E	0~B	Not used	
	C	Environmental monitor detected DKC failure	
	D	Not used	
	E	Environmental monitor detected DKU failure	
	F	Not used	

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Format and Message

(2/2)

Format	Message	Meaning
F	0	Operation Terminated
	1	Microprogram detected cache failure
	2	Cache failure
	3	Not used
	4	Not used
	5	Not used
	6	CFW not authorized
	7~9	Not used
	A	NVS terminated
	B	HRC/HODM Pair suspend
	C~E	Not used
	F	Cache/Shared memory/M-bus/F-bus/J-bus warning

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4.2 32-byte type SSB

	0	1	2	3	4	5	6	7	
00	Internal SSB common Information								
1F									
20	Command reject	Intervention REQ	Not used	Equipment check	Data check	Not used	Not used	Incomplete domain	Basic SSB
21	Permanent error	Invalid TRK FMT	End of cylinder	Operator message	Not used	File protect	Write inhibit	precise ending	
22	EC=0/1/2/3/F:Environmental data present								
	EC=4/6/D/E :Storage control type (x'06':Cache DKC)								
23	Count / Command overrun threshold is exceeded.								
24	Device address								
25	Device type (x'24':DKU871-3)								
26	SSB2/SSB5 valid	SSB4 valid	SSB29-31 valid	Not used	Format				
27	Host SSB Format-depended Information								
37									
38	Log and message control								
39	Program action code								
3A	Dual frame	EDCC mode (1)	Duplex pair (0)	S-Volume ERR (0)	Async operation	Serial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	Not used	Not used	Not used	3380 TRK COMPT(0)	Not used	Storage path number		
3C	Message code								
3D	Cylinder address								
3E									
3F	Head address								
40	Internal SSB Format-depended Information								
7F									

*:Configuration information

**:Byte 20-26 and byte 38-3F are not certain until DKC reports SSB to Host. So if you want to know the detail, please refer to SSB section.

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Exception Class (Byte36:bit0-3) and Format (Byte26:bit4-7)

Exception Class	Format	Meaning
0	0~2	Not used
	3	Machine condition exception
	4	I/O Program exception (incomplete Domain)
	5~F	Not used
2	0~E	Not used
	F	DKC SIM
3	0~E	Not used
	F	DKC SIM
4	0	Not used
	1	Data exception (PCI,Permanent)*
	2~E	Not used
	F	Dedia SIM
5	0~E	Not used
	F	Device SIM/Media SIM
6	0	Not used
	1	Statistics*
	2~F	Not used
C	0~E	Not used
	F	DKC SIM
D	0	Drive detected failure*
	1	SPC detected failure*
	0~E	Not used
	F	DKC SIM
E	0	Drive detected failure/LDEV blockade/PIN VOL detected/LDEV not ready/Write inhibited*
	1~E	Not used
	F	Device SIM
F	0~E	Not used
	F	DKC SIM/Cache SIM

* : For DKU87I (IBM 3390 emulation mode) only.

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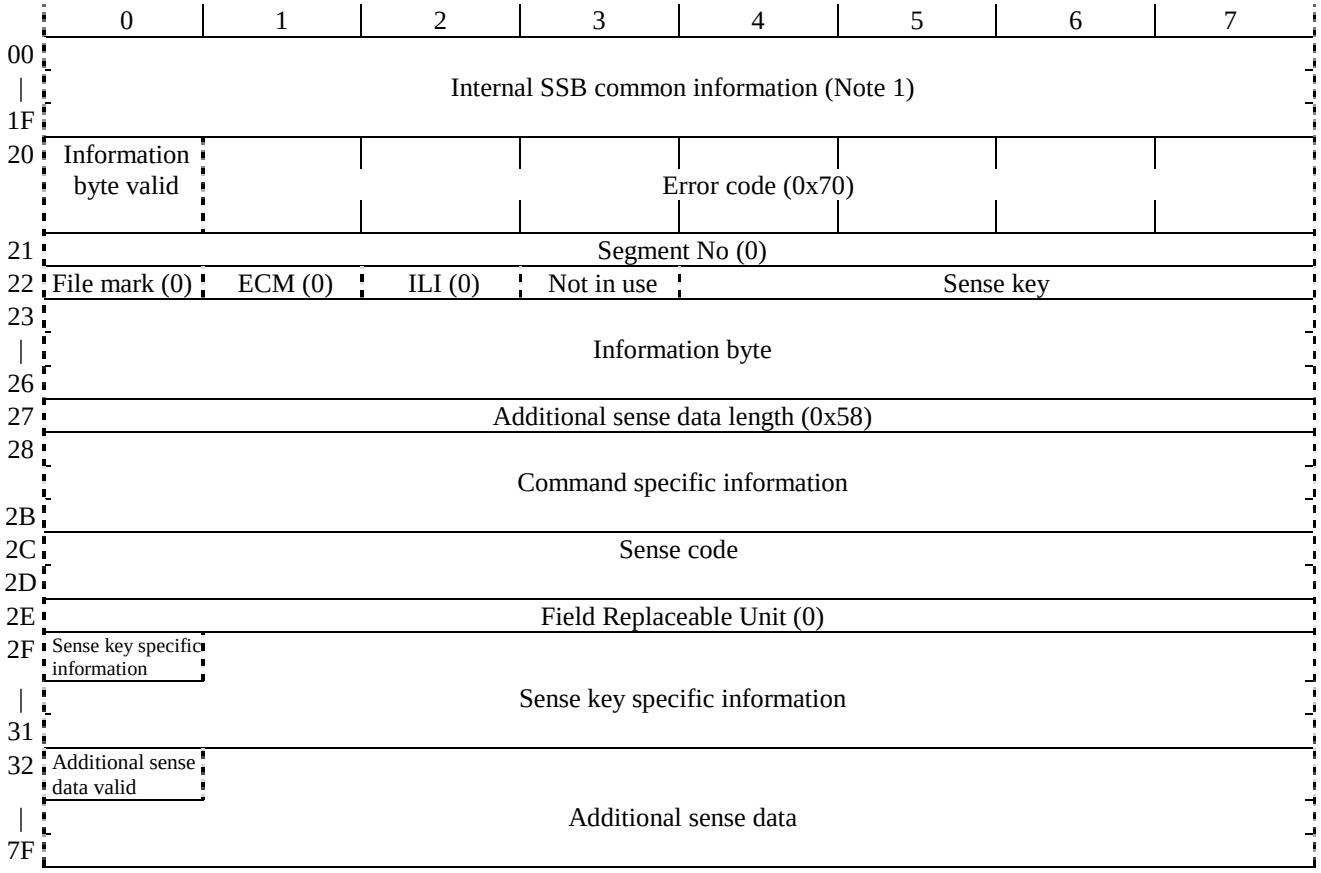
4.3 SCSI host report format SSB



(Note 1) 0xCX (X=sense key) is set to byte 7 (log type low-order byte). SSB on SVP is indicated as F/M=CX.

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Details of SCSI host report format SSB information

Byte	Bit	Description	Setting	Remarks
20	0	Information byte valid/invalid 0:Invalid 1:Valid	CHS command control	
	1 ~ 7	Error code (0x7): Indicates an I/O process error.		
21		Segment No. (0)		
22	0	File mark (0)		
	1	ECM (0)		
	2	ILI (0)		
	3	Not in use		
	4 ~ 7	Sense key: For more details, see “sense keys list”.		
23 ~ 26		Information bytes: LBA related to sense key if information byte is valid.		
27		Additional sense data length (0x58): Indicates sense data length after byte 8 or latter.		
28 ~ 2B		Command specific information		
2C ~ 2D		Sense codes: For more details, see “sense codes list”.		
2E		Field Replaceable Unit (0)		
2F ~ 31	0	Sense key specific information valid/invalid 0:Invalid 1:Valid		
	1 ~ 17	Sense key specific information		
32 ~ 7E	0	Additional sense data valid/invalid 0:Invalid 1:Valid	Error detection source	
	1 ~ END	Additional sense data		

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Sense Keys List

Sense key	Description
0	NO SENSE
1	RECOVERED ERROR
2	NOT READY
3	MEDIUM ERROR
4	HARDWARE ERROR
5	ILLEGAL REQUEST
6	UNIT ATTENTION
7	DATA PROTECT
8	BLANK CHECK (Not in use)
9	VENDOR UNIQUE
A	COPY ABORTED
B	ABORTED COMMAND
C	EQUAL (Not in use)
D	VOLUME OVERFLOW
E	MISCOMPARE
F	(RESERVED)

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Refer to SSB04-180 ~ SSB04-190 about Sense Codes.

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5 Format-depended information description

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Byte27 = 0X (X ≠ 8/A:System/Program Check) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘X’:X ≠ 8/A)			
28	Command code (for F/M ≠ F)/Reason code (for F/M=F) (Note 1)							
29	Detail failure information 1 (Note 2)							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID (Note 4)							
31	Routine ID (Note 4)							
32	PCB number							
33	Detail failure information 2 (Note 3)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘0F0X’)							
37	X=Message code (x‘2F00’ for dummy SENSE)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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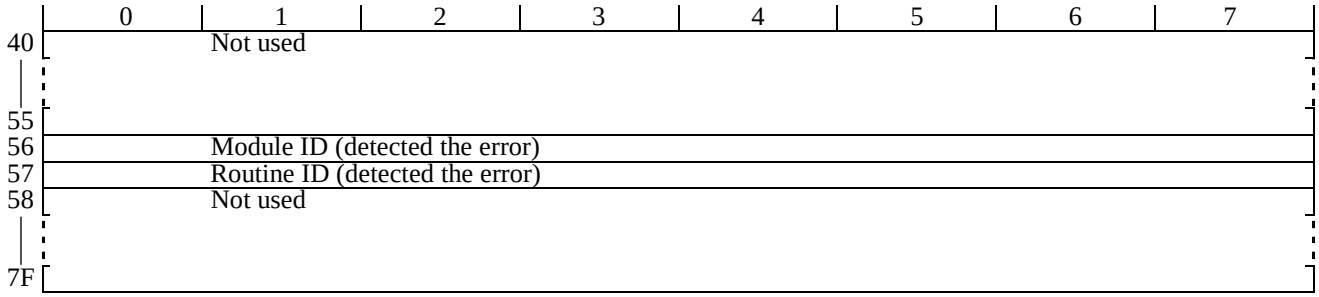
Byte27 = 0X (X ≠ 8/A:System/Program Check) (2/3)



(Note 1)

F/M = 0F:Byte08 Reason code

Code	Reason
00	No message
01	Trying to make cache available and cache status is pending.
02	Not used
03	Trying to make cache force unavailable and cache status is not pending with destage complete.
04	Trying to activate CFW and CFW status is pending.
05	Trying to activate caching (device) and cache status is pending.
06	Trying to destage (track) and NVS is failed.
07	Trying to make NVS unavailable and NVS is initializing.
08	Trying to deactivete caching , DFW or DISCARD (device) , and DFW status is failed.
09	Trying to force deactivate DFW (device) and status is not as follows. • EDFW status is pending or failed. • ENVS is failed and the data exists in NVS, but not in cache.
0A	Trying to make NVS available and DFW status (device) is pending or failed.
0B	Trying to make NVS available and NVS status is pending.
0C	When NVS is failed, trying to stop caching or DFW (device) and the data exists in NVS, but not in cache.
0D	Command requires NVS and NVS is unavailable.
0E	Command requires cache and cache is unavailable.
0F	Not used
10 ~ 28	Not used
29	PFS command (Set Special Interrupt Condition) is issued on an interface on which path group is not established.
2A	Trying to make path group include parallel channel and serial channel.
2B	Message buffer is full.
2C ~ 34	Not used
35	A Set Guaranteed Path subcommand is issued on a fenced path.
36 ~ 3E	Not used
3F	A Make NVS Avail for Subsystem subcommand is issued, but NVS is disable. ('Disable NVS Capability' is set to disable in VPD.)
40	Not used
41	A normal command is issued to a device reserved by maintenance.
42 ~ 7F	Not used
80	A special command is issued on an interface that was disabled by the PFS command with Set Special Intercept Condition order.
81	An attention report on an interface that was disabled by the PFS command with Set Special Intercept Condition order.
82 ~ FF	Not used

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Byte27 = 0X (X ≠ 8/A:System/Program Check) (3/3)

(Note 2) (1) Issued command information when F/M=02

B\b	0	1	2	3	4	5	6	7
29	SCH ID	SCH KEY	Locate, LC EXT	SK, SK CYL	RD IPL	RECAL	SUSP MPR	RD C
2A	DIAG CTL	DIAG CTL (LOC DOM)	DEF EXT	SET FM	SET SUB MODE	SP C	WR CKD	WR R0
2B	SET INTF ID	DIAG CTL (PRE REM)	0	Other command	RD C chainning	All byte match	LC domain	Erase execute
2C	Pseud through	0	0	Allow WR KD	Allow WR D	Allow WR CKD	Allow WR R0	Allow WR HA

(2) Short byte flag when F/M=03
x‘0040 0000’

(3) Mask information when F/M=05

Byte 29: Mask for write control
x‘00’: Allows all write operation except WR HA, WR R0.
x‘40’: Inhibits all write operation.
x‘80’: Allows update write operation.
x‘C0’: Allows all write operation.

Byte 2A: Mask for seek control
x‘00’: Allows all seek commands and RECAL.
x‘08’: Allows SK CYL and SK HD only.
x‘10’: Allows SK HD only.
x‘18’: Inhibits all seek command and multi operation.

Byte 2B: Mask for access
x‘00’: Allows normal access.
x‘02’: Allows device support.
x‘04’: Allows diagnostic access.
x‘06’: Allows device support inhibit data check correction and retry.

Byte 2C: Not used

(4) Record address when other F/M
Byte 29 and 2A : Clinder address
Byte 2B : Head address
Byte 2C : Record number

(Note 3) Bit 4-7 of byte 32: Type of byte 33
x‘08’: Byte 33 is cylinder address (high).
x‘09’: Byte 33 is cylinder address (low).
x‘0A’: Byte 33 is head address (high).
x‘0B’: Byte 33 is head address (low).
x‘0C’: Byte 33 is record number.
Byte 33: One byte of CCHHR.

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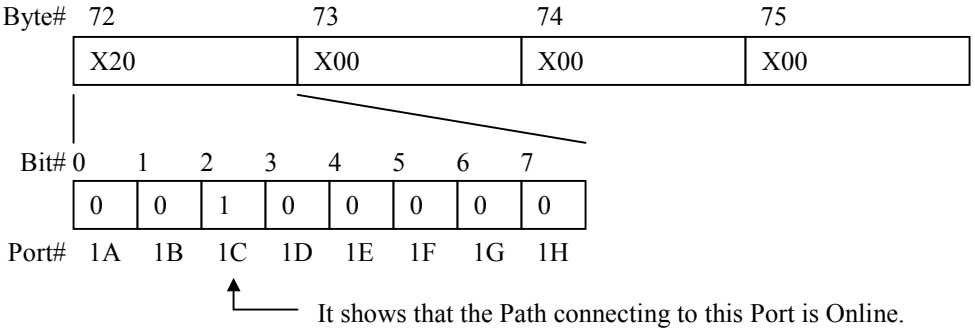
(Note4) The details information of every Module ID & Routine ID

•Module ID & Routine ID=0xC0CA ; The Specified R-VOL of HRC is still Online from the HOST.
(Add Pair operation from the Remote Console was rejected)
Check the SSB.LOG on SVP of the specified RCU. SSB containing EC=C0CA on the specified R-VOL number should be logged.

•Module ID & Routine ID=0xC0A6 ; The M-VOL of HODM is Online from the HOST.
Check the SSB.LOG on SVP of the MCU. SSB containing EC=C0A6 on the specified M-VOL should be logged.

(1) Analyze the SSB.LOG
Both SSB are same format, from SSB byte72(0x48) though byte75(0x4B) show the Bit Map of Port indicating Online from the HOST. Each one bit corresponds to each port. It indicates the LCP Port on which the valid Path Group is established for this device.



(2) Run DSF/ANALYZE-ALLCHPID to trace the Path Group ID of the Online route.
(2.1) In case that DKC Emulation Type is 3990-6/3990-6E or 2105.
Run DSF/ANALYZE with ALLCHPID. The output shows the Path Group ID which is Online to the subsystem.

LOGICAL PATH		SYSTEM ADAPTER ID	FULL ESCON LINK ADDRESS	SP FENCE 0 1 2 3	HOST PATH GROUP ID		
NUMBER	type				CPU SERIAL#	CPU TYPE	CPU TIME STAMP
1	E	00	0101		XXXXXXX	YYYY	ZZZZZZZZ
2-32	N/E	00-01					
33	E	02	0200		XXXXXXX	YYYY	ZZZZZZZZ

"SYSTEM ADAPTER ID" corresponds to the number of the CHL adapter port.
(Ex; Port#1C is "02".)
Trace the Path Group ID indicated the SYSTEM ADAPTER ID corresponding to the value on SSB LOG of EC=C0CA or C0A6.

Note; Reference of Port ID & SAID

CL1								CL2							
CHA-1P		CHA-1Q		CHA-1R		CHA-1S		CHA-2V		CHA-2W		CHA-2X		CHA-2Y	
Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID	Port	SAID
A	00	E	04	J	08	N	0c	A	10	E	14	J	18	N	1c
B	01	F	05	K	09	P	0d	B	11	F	15	K	19	P	1d
C	02	G	06	L	0a	Q	0e	C	12	G	16	L	1a	Q	1e
D	03	H	07	M	0b	R	0f	D	13	H	17	M	1b	R	1f

(2.2) In case that DKC Emulation Type is 3990-3 DSF/ANALYZE-ALLCHPID is not available for 3990-3. Therefore, trace the Path Online Route of the LCP.

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Byte27 = 08 (Reset Notification) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘8’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Hardware level (Note 1)							
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID							
31	Routine ID							
32	PCB number				Not used (x‘0’)			
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘2FFF’)							
37								
38	Log & message control (x‘00’)							
39	Program action code (x‘16’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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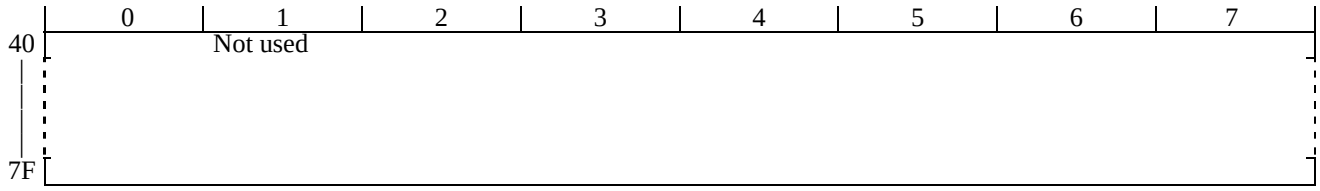
Byte27 = 08 (Reset Notification) (2/2)



(Note 1) Hardware Level

Bit0 : Serial Channel or Parallel Channel

Bit0=0(Parallel channel)

- Bit 1 : Not used
- Bit 2~3 : Strage Path Number
- Bit 4~5 : Channels Per Cluster
  - 00 : 4
  - 01 : 8
  - 10 : Unused
  - 11 : Unused
- Bit 6 : NVS
  - 0 : without NVS
  - 1 : with NVS
- Bit 7 : Unused
- Bit 8~10 : Cache size
  - 000 : none Cache
  - 001 : 256MB
  - 010 : 512MB
  - 011 : 768MB
  - 100 : 1024MB
  - 101 : 1280MB
  - 110 : 1536MB
  - 111 : over 1536MB
- Bit 11~13 : Cluster hardware level
- Bit 14~15 : Cache/NVS hardware level

Bit0=1(Serial Channel)

- Bit 1 : Not used
- Bit 2~3 : Strage Path Number
- Bit 4~7 : Channels Per Cluster
  - 0000 : Parallel=4, Serial=0
  - 0001 : Parallel=8, Serial=0
  - 0010 : Parallel=4, Serial=2
  - 0100 : Parallel=4, Serial=4
  - 0110 : Parallel=0, Serial=2
  - 1000 : Parallel=0, Serial=4
  - 1010 : Parallel=0, Serial=8
  - 1100 : Parallel=0, Serial=6
- Bit 8 : Dual Frame
  - 0 : Dual Frame
  - 1 : Modular Power
- Bit 9~11 : Cache size
  - 000 : none Cache
  - 001 : 256MB
  - 010 : 512MB
  - 011 : 768MB
  - 100 : 1024MB
  - 101 : 1280MB
  - 110 : 1536MB
  - 111 : over 1536MB
- Bit 12~13 : Cluster hardware level
- Bit 14~15 : Cache/NVS hardware level

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Byte27 = 0A (Bus out parity check/Overrun on LCP interface (Byte3A:b4 = 1)) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘0’)				Message (x‘A’)			
28	Command code							
29	Cylinder address							
2A								
2B	Head address							
2C	Record number							
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Module ID							
31	Routine ID							
32	PCB number				BBF OVR	PND OVR	STOP	OVER
33	Not used							
34	SSID of self subsystem							
35								
36	Symptom code (x‘0F0A’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40 -7F	Not used							

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Byte27 = 10 (Intervention required) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘1’)				Message (x‘0’)			
28	Ready	Enable	SSB PEND	Not used (‘00000’)				
29	Not used (x‘00’)							
2A	M.M. RSV	PIN VOL	Not used (‘000000’)					
2B	Host type	DKC type	Not used (‘00’)		DKU type			
2C	Module ID (x‘50’)							
2D	Routine ID (x‘1C’)							
2E	Command code							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	PCB number				Not used (x‘0’)			
33	Not used							
34	SSID of self subsystem							
35								
36	Symptom code (x‘9F10’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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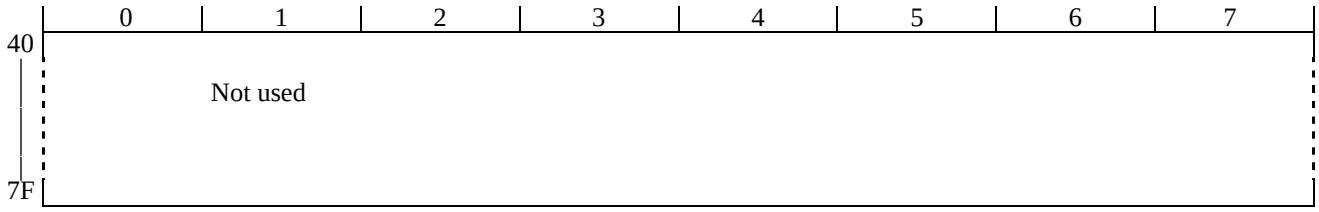
Byte27 = 10 (Intervention required) (2/2)



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Byte27 = 1X (Drive report error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘1’)				Message (x‘2/4’)			
28	Additional sense code (Note 2)							
29	Additional sense code qualifier (Note 2)							
2A	SCSI Command (Note 3)							
2B	Threshold type (Note 4)							
2C	Module ID							
2D	Routine ID							
2E	Not used (x‘0’)				DKA#			
2F	CDEV#				RDEV#			
30	Type code (‘000’)		0		Sense key (Note 1)			
31	Not used (x‘00’)							
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘9F1X’ X:Message)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 1X (Drive report error) (2/2)

	0	1	2	3	4	5	6	7
40		Status byte						
41		Message						
42		CDB						
4B								
4C		SPC status register						
4D		SPC nexus status register						
4E		SPC data block register						
4F								
50		SPC data byte register						
51								
52								
53		SPC SCSI control signal status register						
54		SCSI extended sense data						
73								
74		Not used						
7F								

(Note 1) Sense key
- x‘0’ : No sense
- x‘1’ : Recoverd error
- x‘2’ : Not ready
- x‘3’ : Medium error
- x‘4’ : Hardware error
- x‘5’ : Illigal request
- x‘6’ : Unit attention
- x‘7’ : Data protect
- x‘8’ : Blank check (Not used)
- x‘9’ : Vender unique (Not used)
- x‘A’ : Copy aborted (Not used)
- x‘B’ : Aborted command
- x‘C’ : Equal (Not used)
- x‘D’ : Volume overflow (Not used)
- x‘E’ : Miscompare
- x‘F’ : (Reserved)

(Note 2) See EC = E SSB log.

(Note 3) SCSI command
- x‘00’ : Test unit ready
- x‘03’ : Request sense
- x‘04’ : Format unit
- x‘07’ : Reassign blocks
- x‘12’ : Inquiry
- x‘15’ : Mode serect
- x‘1A’ : Mode sense
- x‘1B’ : Start/stop unit
- x‘1C’ : Recieve diagnostic result
- x‘1D’ : Send diagnostic
- x‘28’ : Read (extend)
- x‘2A’ : Write (extend)
- x‘2E’ : Write and verify
- x‘3B’ : Write buffer

(Note 4) See EC = E SSB log.

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Byte27=3F (Reset Allegiance) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x'3')				Message (x'F')			
28	Not used							
29	Logical path number							
2A	DCN status (Note 1)							
2B								
2C	Command code							
2D	SSID of mate subsystem (x'0000' for EDCC)							
2E								
2F	Maker code & Manufacture code (x'00')							
30	Module ID							
31	Routine ID							
32	PCB number							
33	Not used (x'00')							
34	SSID of self subsystem							
35								
36	Symptom code (x'3F3F')							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27=3F (Reset Allegiance) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
7F								

(Note 1)

	0	1	2	3	4	5	6	7
28	Device busy	ECI	Command chainning	Path reserve	Stack status	Wait SENSE	Long busy	Processor connect
29	Single path mode	Guarant path mode	MCB chainning	0	Block switch	0	0	0

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Byte27 = 4X (Data check) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘4’)				Message (x‘X’)			
28	Cylinder address (Note 1)							
29								
2A	Head address (Note 1)							
2B								
2C	Record number (Note 1)							
2D	Sector number (Note 1)							
2E	Controller ID							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	PCB number				Not used (x‘0’)			
33	Not used							
34	Command code							
35	SSID (low) of self subsystem							
36	Symptom code (x‘4XYY’) (X:Note 2) (YY:Note 3)							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘91’)							
3A	Configuration information							
3B								
3C	Not usde (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 4X (Data check) (2/3)

	0	1	2	3	4	5	6	7
40	Causal Key code							
41	Causal Format/Message							
42	Causal Module ID							
43	Causal Routine ID							
44	LDEV number, slot number							
45								
46								
47								
48	Slot status							
49								
4A								
4B								
4C	staging bit map/Dirty bit map							
4D								
4E								
4F								
50	Current subblock number							
51	EXIT falg (Note 4)							
52	Slot failure information (Note 5)							
53	Obtained information flat (Note 6)							
54	Head subblock number for HIT/MISS decision + Remain subblock count							
55	(when byte36 is x‘40/41/42/43’)/PACC in CBUF (when byte36 is x‘45’)							
56	Not used (when byte36 is x‘40/41/42/43’)/							
57	PAHF in CBUF (when byte36 is x‘45’)							
58	Not used (when byte36 is x‘40/41/42/43’)/							
59	Current CC in JCB (when byte36 is x‘45’)							
5A	Not used (when byte36 is x‘40/41/42/43’)/							
5B	Current HH in JCB (when byte36 is x‘45’)							
5C								
	Reserved							
7F								

(Note 1) Not determined for occurrence in HA or RO

(Note 2) Contents of message

x‘0’ : Data check in HA field
x‘1’ : Data check in C field
x‘2’ : Data check in K field
x‘3’ : Data check in D field
x‘4’ : Missing SYNC byte in HA field
x‘5’ : Missing SYNC byte in C field (PA error)
x‘6’ : Missing SYNC byte in K field
x‘7’ : Missing SYNC byte in D field
x‘8’ : Not used
x‘9’ : Missing AM during retry
x‘A’to x‘F’ : Not used

(Note 3) Contents of correctionflag

Bits 0 and 1 : ECC correction bit
10 : Correctable (Recoverd)
11 : Uncorrectable
Bit 2 : offset activ
Bits 3 to 7 : Not used

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Byte27 = 4X (Data check) (3/3)

(Note 4) EXIT flag
- x‘08’ : CHL I/F CHK2 timeover
- x‘0D’ : EOF
- x‘0E’ : DSB=0E requested
- x‘0F’ : Logical error
- x‘1E’ : Make sense only
- x‘1F’ : Logical error (make sense only)
- x‘30’ : Selective reset requested
- x‘40’ : ‘Staging’ requested
- x‘41’ : ‘Waiting free segment’ requested
- x‘42’ : ‘Timeover of waiting for staging’ requested
- x‘43’ : ‘Staging for PA unmatch’ requested
- x‘45’ : ‘Destaging’ requested
- x‘46’ : ‘High priority destaging’ requested
- x‘47’ : ‘Pseud-through process’ requested
- x‘4B’ : ‘DSB=4E retry’ requested (data transfer)
- x‘4E’ : ‘DSB=4E retry’ requested (DSB = 4E retry)
- x‘4F’ :STG requested (Read or STG in progress)

(Note 5) Slot failure
- x‘80’ : Sector write error
- x‘40’ : Sector read error
- x‘20’ : ECC/LRC error
- x‘10’ : Incomplete data
- x‘08’ : No decision

(Note 6) Obtained information flag
- bit0-1 : Block type
  - 00 : Data block
  - 01 : HA/RO block
  - 10 : Bit map block
- bit2-3 : Side
  - 00 : Cache write side
  - 01 : NVS write side
  - 10 : Cache read side
- bit4 : Segment
  - 0 :No segment
  - 1 :Segment exist
- bit5-7 : Reserved

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Byte27 = 6X (Statistics) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Controller ID							
24	Device address							
25	Command overrun threshold exceeded							
26	Data overrun threshold exceeded							
27	Format (x‘6’)				Message (x‘X’)			
28	Read/search byte count							
29								
2A								
2B								
2C	Seek count							
2D								
2E	Not used (x‘00’)							
2F	Manufacture code (‘000000’)						Factory code (‘00’)	
30	Not used (x‘00’)							
31	DKC serial number							
32								
33								
34	SSID of self SSID							
35								
36	Symptom code (x‘6FXY’ X:0: Statistics/RRBL command, 2: Channel data overrun							
37	Y:CHL# (parallel CHL)/LCP# (serial CHL))							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00000000’)							
3D								
3E								
3F								
40 -7F	Not used							

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Byte27 = 74 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARATE	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’: Cache DKC)							
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘7’)				Message (x‘4’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C24’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘DYZZ’) Y : CDEV number ZZ :RDEV number							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 74 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x‘00’)							
41	Not used							
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	(x‘AB’)							
4D	(x‘CD’)							
4E	CMD BLK number							
4F	Data transfer end flag							
50	I/O status							
51								
52	PDEV status							
53								
54	LOOP status							
55								
56								
57								
58	Frame Manager status							
59								
5A								
5B								
5C	TL status							
5D								
5E								
5F								
60	IO issued status 1							
61								
62	IO issued status 2							
63								
64	Not used							
65								
66								
67								
68	JOB require info							
69								
6A								
6B								
6C	Data transfer status							
6D								
6E								
6F								
70	Not used							
7F								

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Byte27 = 74 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘7’)				Message (x‘4’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Module ID							
2D	Routine ID							
2E	Not used (x‘0’)				DKA number			
2F	CDEV number				RDEV number			
30	Type code (‘111’)			0	Not used (x‘0’)			
31	Not used (x‘00’)							
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	SSID of self subsystem							
35								
36	Symptom code (x‘DF74’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 74 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x‘00’)							
41	Not used							
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	(x‘AB’)							
4D	(x‘CD’)							
4E	CMD BLK number							
4F	Data transfer end flag							
50	I/O status							
51								
52	PDEV status							
53								
54	LOOP status							
55								
56								
57								
58	Frame Manager status							
59								
5A								
5B								
5C	TL status							
5D								
5E								
5F								
60	IO issued status 1							
61								
62	IO issued status 2							
63								
64	Not used							
65								
66								
67								
68	JOB require info							
69								
6A								
6B								
6C	Data transfer status							
6D								
6E								
6F								
70	Not used							
7F								

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Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memory Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘1’)			
28	Subcode			(See following pages)				
29	Hardware information			(See following pages)				
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Not used (x‘00’)							
33	Not used (x‘00’)							
34	PCB number				Message code (x‘0’)			
35	SSID of self subsystem							
36	Symptom code (x‘FF81’ : LDEV type = DKU87I/x‘EF81’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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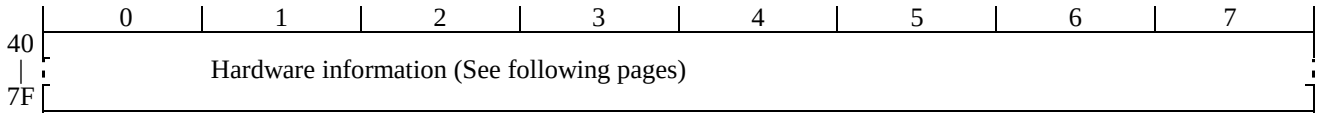
Byte27 = 81 & Byte34:b4-7 = 0 (Shared Memory Failure) (2/2)



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Byte27 = 81 (Shared Memory Failure) Byte28-31 Detail

(1) Byte34, Bit4 to Bit7 = 0: Shared Memory Failure

	0	1	2	3	4	5	6	7
28	Subcode							
	Micro error	MPA error	Shared memory Side A error	Shared memory Side B error	A0 path error	A1 path error	B0 path error	B1 path error
29	Format No.							
	Format No. : x'01': X0A access micro error & MPA internal error x'02': X1A access micro error & MPA internal error x'03': X0A access shared memory error x'04': X1A access shared memory error x'05': X0A access SHSN error x'06': X1A access SHSN error x'07': others error							
2A	MPA:CHK3LOG0:B700 0078(b00-07)							
	Micro SM access address							
2B	MPA:CHK3LOG0:B700 0078(b10-17)							
	Micro SM access address							
2C	MPA:CHK3LOG0:B700 0078(b20-27)							
	Micro SM access address							
2D	MPA:CHK3LOG0:B700 0078(b30-37)							
	Micro SM access address							
2E	MPA: CHK3STS:8200 0108(b00-07)							
	XR send parity error	XR recv parity error	MPID unmatch	Access error	compare error	Resource lock mode/ queue error	XR timeout	XR SEQ error
2F	MPA: CHK3STS:8200 0108(b10-17)							
	A0 collect ANYERR	A1 collect ANYERR	B0 collect ANYERR	B1 collect ANYERR	A0 path error	A1 path error	B0 path error	B1 path error
30	MPA: CHK3STS:8200 0108(b20-27)							
	A0 path timer error	A1 path timer error	B0 path timer error	B1 path timer error	A0 path send parity error	A1 path send parity error	B0 path send parity error	B1 path send parity error
31	MPA: CHK3STS:8200 0108(b30-37)							
	A0 path recv parity error	A1 path recv parity error	B0 path recv parity error	B1 path recv parity error	A0 path no response	A1 path no response	B0 path no response	B1 path no response

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Byte27 = 81 Byte40-7F (X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)
(Byte29=x'01'|x'02') (1/4)

	0	1	2	3	4	5	6	7
40	MPA :HIN :82000050 (b30 - 37)							
	SMDA majority decision result	SMDA input signal status			SMDB majority decision result	SMDB input signal status		
41	MPA :HOUT :82000054 (b30 - 37)							
	SMDA output result	SMDA individual signal output			SMDB output result	SMDB individual signal output		
42	MPA:RXAER:82000210(b20 - 27)							
	Reserved	Reserved	SHSN_A LRC error	SHSN_A LDT byte parity error	PER_RXER0	PER_RXER1	PER_RXER2	PER_RXER3
					SHSN_A EDT byte parity error			
43	MPA:RXAER:82000210(b30 - 37)							
	Reserved	Reserved	Reserved	SHSN_A SDT byte parity error	PER_RXRD 0	PER_RXRD 1	PER_RXRD 2	PER_RXRD 3
						SHSN_A R/W CUDG		
44	MPA:RXBER:82000214(b20 - 27)							
	Reserved	Reserved	SHSN_B LRC error	SHSN_B LDT byte parity error	PER_RXER0	PER_RXER1	PER_RXER2	PER_RXER3
					SHSN_B EDT byte parity error			
45	MPA:RXBER:82000214(b30 - 37)							
	Reserved	Reserved	Reserved	SHSN_B SDT byte parity error	PER_RXRD 0	PER_RXRD 1	PER_RXRD 2	PER_RXRD3
						SHSN_B R/W CUDG		
46	MPA:RXAER1:82000218(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHSN_A MPID unmatch
47	MPA:RXBER1:8200021C(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SHSN_B MPID unmatch
48	MPA:LNEWER : 82000234(b30 - 37)							
	L0LD byte parity error				LNEW byte parity error			
49	MPA:LNEWER1 : 8200023C(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	LNEW lock byte error	LNEW QUE error 1	LNEW QUE error 2	LNEW QUE error all
4A	MPA:LCTLER:82000230(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	LCTL byte parity error			
4B	MPA: LCTLER1: 82000238(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LCTL mode set error	LCTL QUE set error
4C	MPA:SQ0ER:82000260(b30 - 37)							
	XR_IF SEQ#0 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4D	MPA:SQ1ER:82000264(b30 - 37)							
	XR_IF SEQ#1 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4E	MPA:SQ2ER:82000268(b30 -37)							
	XR_IF SEQ#2 SEQ log parity error				Reserved	SEQ divergency error	Reserved	SEQ parity error
4F	MPA:X1AP:82000614(b30 - 37)							
	Reserved	Reserved	X1LOCK exec face #0 XR log	X1WT exec face #0 XR log	X1AP exec face #0 XR address log byte parity bit			

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Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (2/4)

	0	1	2	3	4	5	6	7
50	MPA: X0A 77000600 (b00-07) / X1A 77000610 (b00-07)							
	X0A / X1A = exec face #1 XR address log byte							
51	MPA: X0A 77000600 (b10-17) / X1A 77000610 (b10-17)							
	X0A / X1A = exec face #1 XR address log byte							
52	MPA: X0A 77000600 (b20-27) / X1A 77000610 (b20-27)							
	X0A / X1A = exec face #1 XR address log byte							
53	MPA: X0A 77000600 (b30-37) / X1A 77000610 (b30-37)							
	X0A / X1A = exec face #1 XR address log byte							
54	MPA:ACSER B7000220(b30 -37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Access pattern error	Access mode error	Access hot line error
55	MPA:TIME0ER B7000250(b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	TIM #0 byte parity error			
56	MPA:A0TXER B714j000 (b34 - 37)				MPA:A1TXER B715j000 (b34 - 37)			
	Reserved	Reserved	Send data parity error	Send data LRC error	Reserved	Reserved	Send data parity error	Send data LRC error
57	MPA:B0TXER B716j000 (b34 - 37)				MPA:B1TXER B717j000 (b34 - 37)			
	Reserved	Reserved	Send data parity error	Send data LRC error	Reserved	Reserved	Send data parity error	Send data LRC error
58	MPA:MPASTS B7000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD B7000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP B7000604 (b30 - 37)							
	Reserved	Reserved	X0LOCK exec face#0 XR log	X0WT exec face#0 XR log	X0AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP B700060C (b34 - 37)				MPA:X1WDP B700061C (b34 - 37)			
	X0WDP exec face #0 XR write-data log byte parity bit				X1WDP exec face #0 XR write-data log byte parity bit			
5C	MACS_ADR							
	Micro Access Address							
5D	MACS_ADR							
	Micro Access Address							
5E	MACS_ADR							
	Micro Access Address							
5F	MACS_ADR							
	Micro Access Address							

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Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)
(Byte29=x'01'|x'02') (3/4)

	0	1	2	3	4	5	6	7
60	MACS_DAT							
	Micro Access Data							
61	MACS_DAT							
	Micro Access Data							
62	MACS_DAT							
	Micro Access Data							
63	MACS_DAT							
	Micro Access Data							
64	MPA: X0WD: 77000608 (b00-07) / X1WD: 77000618 (b00-07)							
	X0WD / X1WD = exec face #0 XR write-data log byte							
65	MPA: X0WD: 77000608 (b10-17) / X1WD: 77000618 (b10-17)							
	X0WD / X1WD = exec face #0 XR write-data log byte							
66	MPA: X0WD: 77000608 (b20-27) / X1WD: 77000618 (b20-27)							
	X0WD / X1WD = exec face #0 XR write-data log byte							
67	MPA: X0WD: 77000608 (b30-37) / X1WD: 77000618 (b30-37)							
	X0WD / X1WD = exec face #0 XR write-data log byte							
68	MPA:RXA_EDT:B7000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:B7000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:B7000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:B7000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_path TM0ERR:B714j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_path TM0ERR:B715j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:SHSN ACS ERR:B7000228 (b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	X0 access error	X1 access error
6F	MPA:COMP ERR:B7000224 (b30 - 37)							
	Reserved	Reserved	Reserved	Reserved	Compare error 0	Compare error 1	Compare error 2	Compare error 3

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Byte27 = 81 Byte40-7F(X0A ACCESS MICRO ERROR, X1A ACCESS MICRO ERROR, MPA INTERNAL ERROR)

(Byte29=x'01'|x'02') (4/4)

	0	1	2	3	4	5	6	7
70	MPA:X0ER :B7000208 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MPID register parity error	LCTL register parity error
71	MPA:X0ER :B7000208 (b30 - 37)							
	Input address parity error				Input data parity error			
72	MPA:X1ER :B700020C(b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MPID register parity error	LCTL register parity error
73	MPA:X1ER :B700020C(b30 -37)							
	Input address parity error				Input data parity error			
74	MPA:RXB_EDT:B7000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:B7000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:B7000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:B7000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :B7000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :B7000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :B7000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :B7000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :B7000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :B7000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :B7000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :B7000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

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Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :B780001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :B780001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :B780001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43	SMA ASIDE:PATH0_ERR_DET :B7800104(b14 -17)				SMA ASIDE:PATH1_ERR_DET :B7800114(b14 -17)			
	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved
44	SMA ASIDE: BOARD_ERR_STS : B7800120 (b00 - 07)							
	MCB parity error	MAB parity error	MWB parity error	DIMM select parity error	Path select parity error	RDT latch nothing error	ICB parity error	IAB parity error
45	SMA ASIDE: BOARD _ERR_STS : B7800120 (b10 - 17)							
	IWB parity error	IO path select parity error	PD address output error	Lock address buffer parity error	Lock wait time over	Lock protcol error	Answer PATH ID unmatch error	CACHE slot ID parity error
46	SMA ASIDE: BOARD _ERR_STS : B7800120 (b20 - 27)							
	Clock error	Refresh error	Timer error	Arbiter error	Write sequencer parity error	Read sequencer parity error	Memory sequencer parity error	IO sequencer parity error
47	SMA ASIDE: BOARD _ERR_STS : B7800120 (b30 - 37)							
	ECC generator error	SM data output error	Bus switch error	Valid counter parity error	Scan timeout counter parity error	Scan sequencer error	BCINT output error	SCINT output error
48	SMA ASIDE: BOARD _ERR_DET : B7800124 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Memory Arbiter compare error	Lock Arbiter compare error	I/O Arbiter compareerro r
49	SMA ASIDE: BOARD _ERR_DET : B7800124 (b30 - 37)							
	Reserved	System clock error	Timer clock error	Clock frequency error	Reserved	Memory initialize parity error	Refresh counter parity error	No refresh action detected
4A	SMA ASIDE :DIMM_SIG_ERR_DIMM : B780012C(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when DIMM controll error detected							
4B	SMA ASIDE :UNCOR_ERR_DIMM : B7800130(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
4C	SMA BSIDE :SMA_STS :B7A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS : B7A 0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS : B7A 0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F	SMA BSIDE :PATH0 ERR_DET : B7A 00104 (b14 - 17)				SMA BSIDE :PATH1 ERR_DET : B7A 00114 (b14 - 17)			
	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved	Slave_dual lock access error	Double lock error	Lock access counter over error	Reserved

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Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: BOARD_ERR_STS :B7A00120 (b00 - 07)							
	MCB parity error	MAB parity error	MWB parity error	DIMM select parity error	Path select parity error	RDT latch nothing error	ICB parity error	IAB parity error
51	SMA BSIDE: BOARD_ERR_STS :B7A00120 (b10 - 17)							
	IWB parity error	IO path select parity error	PD address output error	Lock address buffer parity error	Lock wait time over	Lock protcol error	Answer PATH ID unmatch error	CACHE slot ID parity error
52	SMA BSIDE: BOARD_ERR_STS :B7A00120 (b20 - 27)							
	Clock error	Refresh error	Timer error	Arbiter error	Write sequencer parity error	Read sequencer parity error	Memory sequencer parity error	IO sequencer parity error
53	SMA BSIDE: BOARD_ERR_STS :B7A00120 (b30 - 37)							
	ECC generator error	SM data output error	Bus switch error	Valid counter parity error	Scan timeout counter parity error	Scan sequencer error	BCINT output error	SCINT output error
54	SMA BSIDE: BOARD_ERR_DET :B7A00124 (b20 - 27)							
	Reserved	Reserved	Reserved	Reserved	Reserved	Arbiter compare error	Arbiter compare error	Arbiter compareerro r
55	SMA BSIDE: BOARD_ERR_DET :B7A00124 (b30 - 37)							
	Reserved	System clock error	Timer clock error	Clock frequency error	Reserved	Memory Arbiter compare error	Lock Arbiter compare error	I/O Arbiter compareerro r
56	SMA BSIDE :DIMM_SIG_ERR_DIMM :B7A0012C(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when DIMM controll error detected							
57	SMA BSIDE :UNCOR_ERR_DIMM :B7A00130(b30 - 37)							
	DIMM 0	DIMM 1	DIMM 2	DIMM 3	DIMM 4	DIMM 5	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
58	MPA:MPASTS B7000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD B7000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP B7000604 (b30 - 37)/X1AP 82000614 (b30-37)							
	Reserved	Reserved	X0/1LOCK exec face#0 XR log	X0/1WT exec face#0 XR log	X0AP exec face #0/ X1AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP B700060C (b34 - 37) / MPA:X1WDP B700061C (b34 - 37)				MPA:TIMEOUT B7000240 (b34 - 37)			
	X0WDP exec face #0 or X1WDP exec face #0 XR write-data log byte parity bit				Reserved	Reserved	Reserved	time out
5C	MACS_ADR							
	Micro Access Address							
5D	MACS_ADR							
	Micro Access Address							
5E	MACS_ADR							
	Micro Access Address							
5F	MACS_ADR							
	Micro Access Address							

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Byte27 = 81 Byte40-7F (,w0,` ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (3/4)

	0	1	2	3	4	5	6	7
60	MACS_DAT							
	Micro Access Data							
61	MACS_DAT							
	Micro Access Data							
62	MACS_DAT							
	Micro Access Data							
63	MACS_DAT							
	Micro Access Data							
64	MPA:RXA_RDT:B7000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:B7000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:B7000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:B7000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:B7000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:B7000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:B7000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:B7000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:B714j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:B715j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_Path TM0ERR:B716j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:B717j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

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Byte27 = 81 Byte40-7F (X0A ACCESS SM ERROR, X1A ACCESS SM ERROR) (Byte29=x'03'|x'04') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :B7000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :B7000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :B7000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :B7000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:B7000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:B7000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:B7000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:B7000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :B7000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :B7000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :B7000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspattern SM read	Accesspattern SM write	Accesspattern SM read (atomic)	Accesspattern SM write (atomic)
7B	MPA :ACSMODE :B7000650 (b30 -37)							
	Accesspattern resource lock	Accesspattern IO read	Accesspattern IO write	Accesspattern BCAST read	Accesspattern BCAST write	Accesspattern SCAN read	Accesspattern Scan write	Reserved
7C	MPA :ACSPATH :B7000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :B7000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :B7000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :B7000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

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Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :B780001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :B780001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :B780001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43	Reserved							
44	SMA ASIDE: PATH0_ERR_DET :B7800104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1 under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
45	SMA ASIDE: PATH0_ERR_DET :B7800104 (b10 - 17)							
	Recv data LRC error	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
46	SMA ASIDE: PATH0_ERR_DET :B7800104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
47	SMA ASIDE: PATH0_ERR_DET :B7800104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self-path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
48	SMA ASIDE: PATH1_ERR_DET :B7800114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1 under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
49	SMA ASIDE: PATH1_ERR_DET :B7800114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
4A	SMA ASIDE :PATH1_ERR_DET :B7800114 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
4B	SMA ASIDE :PATH1_ERR_DET :B7800114 (b30 - 37))							
	Reserved	Reserved	lock under no lock request	common path self-path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
4C	SMA BSIDE :SMA_STS :B7A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS :B7A0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA alllock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS :B7A0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F	Reserved							

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Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: PATH0_ERR_DET :B7A00104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
51	SMA BSIDE: PATH0_ERR_DET :B7A00104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
52	SMA BSIDE: PATH0_ERR_DET B7A00104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
53	SMA BSIDE: PATH0_ERR_DET :B7A00104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare err	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
54	SMA BSIDE: PATH1_ERR_DET :B7A00114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
55	SMA BSIDE: PATH1_ERR_DET :B7A00114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
56	SMA BSIDE :PATH1_ERR_DET :B7A00114(b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
57	SMA BSIDE :PATH1_ERR_DET :B7A00114(b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare err	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
58	MPA:MPASTS B7000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD B7000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP B7000604 (b30 - 37)/ MPA:X1AP B7000614 (b30 - 37)							
	Reserved	Reserved	X0/1LOCK exec face#0	X0/1WT exec face#0	X0AP exec face #0/ X1AP exec face #0 XR address log byte parity bit			
5B	MPA:X0WDP B700060C (b34 - 37) / MPA:X1WDP B700061C (b34 - 37)				MPA:TIMEOUT B7000240 (b34 - 37)			
	X0WDP exec face #0 /X1WDP exec face #0 XR write-data log byte parity bit				Reserved	Reserved	Reserved	time out
5C	MACS_ADR							
	Micro Access Address							
5D	MACS_ADR							
	Micro Access Address							
5E	MACS_ADR							
	Micro Access Address							
5F	MACS_ADR							
	Micro Access Address							

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Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (3/4)

	0	1	2	3	4	5	6	7
60	MACS_DAT							
	Micro Access Data							
61	MACS_DAT							
	Micro Access Data							
62	MACS_DAT							
	Micro Access Data							
63	MACS_DAT							
	Micro Access Data							
64	MPA:RXA_RDT:B7000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:B7000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:B7000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:B7000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:B7000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:B7000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:B7000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:B7000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:B714j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:B715j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_Path TM0ERR:B716j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:B717j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

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Byte27 = 81 Byte40-7F (X0A ACCESS HSN ERROR, X1A ACCESS HSN ERROR) (Byte29=x'05'|x'06') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :B7000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :B7000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :B7000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :B7000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:B7000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:B7000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:B7000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:B7000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :B7000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :B7000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :B7000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :B7000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :B7000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :B7000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :B7000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :B7000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

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Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (1/4)

	0	1	2	3	4	5	6	7
40	SMA ASIDE:SMA_STS :B780001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
41	SMA ASIDE:SMA_STS :B780001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA all lock status bit	SM ready status bit	SM LSI blockade status bit
42	SMA ASIDE:SMA_STS :B780001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
43	SMA ASIDE: UNCOR_ERR_DIMM:B7800130 (b30 - 37)							
	DIMM00	DIMM01	DIMM02	DIMM03	DIMM04	DIMM05	Reserved	Reserved
	DIMM error status bit when uncorrectable error detected							
44	SMA ASIDE: PATH0_ERR_DET :B7800104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
45	SMA ASIDE: PATH0_ERR_DET :B7800104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
46	SMA ASIDE: PATH0_ERR_DET :B7800104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
47	SMA ASIDE: PATH0_ERR_DET :B7800104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
48	SMA ASIDE: PATH1_ERR_DET :B7800114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1over run error
49	SMA ASIDE: PATH1_ERR_DET :B7800114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
4A	SMA ASIDE :PATH1_ERR_DET :B7800114 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
4B	SMA ASIDE :PATH1_ERR_DET :B7800114 (b30 - 37))							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
4C	SMA BSIDE :SMA_STS :B7A0001C (b10 - 17)							
	Reserved	Reserved	Reserved	Reserved	CACHE PK slot signal bit '01' : A side '10' : B side		SM disconnect status bit	SM power down status bit
4D	SMA BSIDE :SMA_STS :B7A0001C (b20 - 27)							
	disconnect request bit	SM self-refresh status bit	SM voltage status bit	LSI voltage status bit	System timer enable status bit	SMA all lock status bit	SM ready status bit	SM LSI blockade status bit
4E	SMA BSIDE :SMA_STS :B7A0001C (b30 - 37)							
	CACHE PK version bit				SMA LSI version bit			
4F	Reserved							

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Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (2/4)

	0	1	2	3	4	5	6	7
50	SMA BSIDE: PATH0_ERR_DET : B7A00104 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
51	SMA BSIDE: PATH0_ERR_DET : B7A00104 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
52	SMA BSIDE: PATH0_ERR_DET : B7A00104 (b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
53	SMA BSIDE: PATH0_ERR_DET : B7A00104 (b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
54	SMA BSIDE: PATH1_ERR_DET : B7A00114 (b00 - 07)							
	HSN recv command parity error	HSN recv address parity error	HSN recv write data parity error	Reserved	HSN recv sync0 under run error	HSN recv sync1under run error	HSN recv sync0 over run error	HSN recv sync1 over run error
55	SMA BSIDE: PATH1_ERR_DET : B7A00114 (b10 - 17)							
	Recv data LRC	LRC byte check inconsist	Command lock/unlock '0' or '1'	Command read/write bit '0' or '1'	Slave-dual lock access error	Double lock error	Lock access count over error	Reserved
56	SMA BSIDE :PATH1_ERR_DET : B7A00114(b20 - 27)							
	Command bit parity generator error	Address bit parity generator error	Data bit parity generator error	Path command buffer parity error	Path address buffer parity error	Path write data buffer parity error	Path command lock/unlock bit ON	Path command read/write bit ON
57	SMA BSIDE :PATH1_ERR_DET : B7A00114(b30 - 37)							
	Reserved	Reserved	lock under no lock request	common path self path compare error	Reserved	Path sequencer parity error	Request tineout count parity error	Lock timeout count parity error
58	MPA:MPASTS B7000100 (b30 - 37)							
	MPA interrupt status bit	Master CHK3 status bit	Slave CHK3 status bit	Reserved	PROM_IF CHK1B status bit	COM_IF CHK1B status bit	XR_IF CHK1B status bit	MP interrupt status bit
59	MPA:BMD B7000024 (b30 - 37)							
	Reserved	SM copy mode enable	SM disable side A	SM disable side B	A0 path disable	A1 path disable	B0 path disable	B1 path disable
5A	MPA:X0AP B7000604 (b30 - 37)							
	Reserved	Reserved	X0LOCK exec face#0 XR log	X0WT exec face#0 XR log	X0AP exec face #0 XR address log byte parity bit			
5B	MPA:X1AP B7000614 (b34 - 37)							
	Reserved	Reserved	X1LOCK exec face#0 XR log	X1WT exec face#0 XR log	X1AP exec face #0 XR address log byte parity bit			
5C	MACS_ADR							
	Micro Access Address							
5D	MACS_ADR							
	Micro Access Address							
5E	MACS_ADR							
	Micro Access Address							
5F	MACS_ADR							
	Micro Access Address							

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Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (3/4)

	0	1	2	3	4	5	6	7
60	MACS_DAT							
	Micro Access Data							
61	MACS_DAT							
	Micro Access Data							
62	MACS_DAT							
	Micro Access Data							
63	MACS_DAT							
	Micro Access Data							
64	MPA:RXA_RDT:B7000620 (b00 - 07)							
	RXA_RD00	RXA_RD01	RXA_RD02	RXA_RD03	RXA_RD04	RXA_RD05	RXA_RD06	RXA_RD07
	SHSN_A recv-data log read data byte							
65	MPA:RXA_RDT:B7000620 (b10 - 17)							
	RXA_RD10	RXA_RD11	RXA_RD12	RXA_RD13	RXA_RD14	RXA_RD15	RXA_RD16	RXA_RD17
	SHSN_A recv-data log read data byte							
66	MPA:RXA_RDT:B7000620 (b20 - 27)							
	RXA_RD20	RXA_RD21	RXA_RD22	RXA_RD23	RXA_RD24	RXA_RD25	RXA_RD26	RXA_RD27
	SHSN_A recv-data log read data byte							
67	MPA:RXA_RDT:B7000620 (b30 - 37)							
	RXA_RD30	RXA_RD31	RXA_RD32	RXA_RD33	RXA_RD34	RXA_RD35	RXA_RD36	RXA_RD37
	SHSN_A recv-data log read data byte							
68	MPA:RXA_EDT:B7000624 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
69	MPA:RXA_EDT:B7000624 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
6A	MPA:RXA_EDT:B7000624 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
6B	MPA:RXA_EDT:B7000624 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
6C	MPA:A0_Path TM0ERR:B714j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6D	MPA:A1_Path TM0ERR:B715j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6E	MPA:B0_ path TM0ERR:B716j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1
6F	MPA:B1_Path TM0ERR:B717j008 (b30 - 37)							
	Reserved	Time out 7	Time out 6	Time out 5	Time out 4	Time out 3	Time out 2	Time out 1

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Byte27 = 81 Byte40-7F (OTHER ERROR) (Byte29=x'07') (4/4)

	0	1	2	3	4	5	6	7
70	MPA: RXB_RDT :B7000630 (b00 - 07)							
	RXB_RD00	RXB_RD01	RXB_RD02	RXB_RD03	RXB_RD04	RXB_RD05	RXB_RD06	RXB_RD07
	SHSN_B recv-data log read data byte							
71	MPA: RXB_RDT :B7000630 (b10 - 17)							
	RXB_RD10	RXB_RD11	RXB_RD12	RXB_RD13	RXB_RD14	RXB_RD15	RXB_RD16	RXB_RD17
	SHSN_B recv-data log read data byte							
72	MPA: RXB_RDT :B7000630 (b20 - 27)							
	RXB_RD20	RXB_RD21	RXB_RD22	RXB_RD23	RXB_RD24	RXB_RD25	RXB_RD26	RXB_RD27
	SHSN_B recv-data log read data byte							
73	MPA: RXB_RDT :B7000630 (b30 - 37)							
	RXB_RD30	RXB_RD31	RXB_RD32	RXB_RD33	RXB_RD34	RXB_RD35	RXB_RD36	RXB_RD37
	SHSN_B recv-data log read data byte							
74	MPA:RXB_EDT:B7000634 (b00 - 07)							
	MP Status read INT	MP Status read STS flg	MP Status read Valid flg	MP Status read TOV	SCAN INT	SCAN read Data flg	SCAN STS flg	SCAN TOV
75	MPA:RXB_EDT:B7000634 (b10 - 17)							
	All lock busy	Memory not Ready	Back up busy	All lock error	Memory disconnect busy	Illegal address error	DIMM Invalid error	Illegal lock error
76	MPA:RXB_EDT:B7000634 (b20 - 27)							
	Request timeout	PRB timeout	Lock wait timeout	Lock off timeout	PRB parity error	Check code error	Path any error	Path board error
77	MPA:RXB_EDT:B7000634 (b30 - 37)							
	Correctable error	Uncorrectable error	I/O register parity error	Reserved	Reserved	SM PS down error	Memory control signal error	Common board error
78	MPA :ACSMODE :B7000650 (b00 -07)							
	Reserved	Reserved	Reserved	XR access exec face #	Reserved	Reserved	Access path A side	Access path B side
79	MPA :ACSMODE :B7000650 (b10 -17)							
	Access mode 1	Access mode 2	Access mode 3	Access mode 4	Access mode 5	Access mode 6	Access mode 7	Access mode 8
7A	MPA :ACSMODE :B7000650 (b20 -27)							
	Access mode 9	Access mode 10	Reserved	Reserved	Accesspatarn SM read	Access patarn SM write	Access patarn SM read (atomic)	Access patarn SM write (atomic)
7B	MPA :ACSMODE :B7000650 (b30 -37)							
	Access patarn resource lock	Access patarn IO read	Access patarn IO write	Access patarn BCAST read	Access patarn BCAST write	Access patarn SCAN read	Access patarn Scan write	Reserved
7C	MPA :ACSPATH :B7000654 (b00 - 07)							
	1st access read access	1st access write access	1st access lock acquire access	1st access lock termination access	1st access use A0 path	1st access use A1 path	1st access use B0 path	1st access use B1 path
7D	MPA :ACSPATH :B7000654 (b10 - 17)							
	2nd access read access	2nd access write access	2nd access lock acquire access	2nd access lock termination access	2nd access use A0 path	2nd access use A1 path	2nd access use B0 path	2nd access use B1 path
7E	MPA :ACSPATH :B7000654 (b20 - 27)							
	3rd access read access	3rd access write access	3rd access lock acquire access	3rd access lock termination access	3rd access use A0 path	3rd access use A1 path	3rd access use B0 path	3rd access use B1 path
7F	MPA :ACSPATH :B7000654 (b30 - 37)							
	4th access read access	4th access write access	4th access lock acquire access	4th access lock termination access	4th access use A0 path	4th access use A1 path	4th access use B0 path	4th access use B1 path

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Byte27 = 81 & Byte34 : bit4-7 = 3 (CHK3 Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘1’)			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	PCB number				Message code (x‘3’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF81’ : LDEV type = DKU87I/x‘EF81’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 81 & Byte34 : bit4-7 = 3 (CHK3 Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted opration code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN number						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 88 & Byte34:b4-7=A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message”(x‘01’:LCP CHK-2/ADP interface error)							
29	LCP error code							
2A								
2B	XR4B(H)							
	BBF OVERRUN	PND OVERRUN	0	0	0	0	0	0
2C	XR4B(L)							
	LRCA ERR	LRCB ERR	BBFP PER	BBIP PER	BBOP PER	PND CK2	CNT PER	REQ CNT OVERRUN
2D	XR3E(H)							
	RBFA APER	RBFB APER	RBFC APER	RBF WRDER	MBFA APER	MBFB APER	MBFC APER	MBF WRDER
2E	XR3E(L)							
	FRM RCTPE	CMP DPER	XFR CHRPER	XFR SEQPER	M-CNT PER	H-CNT PER	0	0
2F	XR55(H)							
	BUSPE PA	LRCER PA	REQ ER A	ADTDT ER A	0	0	0	0
30	XR55(L)							
	BUSPE PB	LRCER PB	REQ ER B	ADTDT ER B	0	0	0	0
31								
	Control flag	0	0	STOP (XR49:bit15)	CK2 DTX (XR4A:bit0)	CK2 LIN (XR4A:bit1)	IFERA (XR51:bit12)	IFERB (XR51:bit13)

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 01 (LCP Failure:CHK-2/ADP I/F Error) (2/2)

	0	1	2	3	4	5	6	7
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘A’)			
35	SSID (Low) of self subsystem							
36	Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							
40	LCP error message (x‘01’)							
41	Key code (x‘04’)							
42	LCP error code							
43								
44	x‘00’							
45	Command code							
46	x‘00’							
47	x‘00’							
48	XR4B							
49								
4A	XR3E							
4B								
4C	XR55							
4D								
4E	Control flag							
4F	x‘00’							
50	Not used							
7F								

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Receive Error) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message”(x‘02’:Link receive error)							
29	LCP error code							
2A								
2B	XR36(H)							
	L-SIG ERR0	L-SIG ERR1	CONN ERR0	CONN ERR1	CONN ERR2	0	0	0
2C	XR37(H)							
	CONN ERR3	L-SIG ERR	CODE VIOLA	SEQ ERR	CRC ERR	ABORT ERR	PROT ERR0	PROT ERR1
2D	XR37(L)							
	PROT ERR2	PROT ERR3	PROT ERR4	PROT ERR5	PROT ERR6	PROT ERR7	PROT ERR8	PROT ERR9
2E	XR33(H)							
	C-SOF ERR	P-SOF ERR	D-EOF ERR	P-EOF ERR	L-SIG ERR	CODE VIOLA	SEQ ERR	CRC ERR
2F	XR33(L)							
	0	0	0	R-CNT 0	R-CNT 1	R-CNT 2	R-CNT 3	R-CNT 4
30								
	0	0	STOP (XR49:bit15)	ABORT (XR32:bit11)	ER RCV1 (XR4A:bit3)	ER RCV2 (XR4A:bit4)	ER RCV3 (XR4A:bit5)	OTHER (XR51:bit6)
31	XR2A(L)							
	Field Information							

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 02 (LCP Failure:Link Receive Error) (2/2)

	0	1	2	3	4	5	6	7
32		Module ID						
33		Routine ID						
34		PCB number			Message code (x‘A’)			
35		SSID (Low) of self subsystem						
36		Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)						
37								
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used (x‘00’)						
3D		Cylinder address						
3E								
3F		Head address						
40		LCP error message (x‘02’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		XR36						
49								
4A		XR37						
4B								
4C		XR33						
4D								
4E		Control flag						
4F		x‘00’						
50		Not used						
7F								

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message (x‘0C’:Long Write Data)							
29	LCP error code							
2A								
2B	Request count							
2C								
2D	Received data count							
2E								
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘A’)			
35	SSID (low) of self subsystem							
36	Symptom Code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0C (LCP Failure:Long Write Data) (2/2)

	0	1	2	3	4	5	6	7
40	LCP error message (x‘0C’)							
41	Key code (x‘04’)							
42	LCP error code							
43								
44	x‘00’							
45	Command code							
46	x‘00’							
47	x‘00’							
48	Requested count							
49								
4A	Received data count							
4B								
4C	x‘00’							
4D	x‘00’							
4E	x‘00’							
4F	x‘00’							
50	Not used							
⋮								
7F								

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
12	CDEV number					RDEV number		
13	0	RCU SIM	0	0		RCV number		
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)					Head address		
27	Format (x‘8’)					Message (x‘8’)		
28	LCP error message (x‘0E’:Timeout)							
29	LCP error code							
2A								
2B	Reason code (Note 1)							
2C								
2D	XR49 (H)							
	ESYCN	END	RDYOK	RDYRCV	0	CMDFRM	ACPRSP	DATAXF
2E	XR49 (L)							
	XFREND	DEVEND	CNTFLG	EOF	CMPEQ	CMPGT	0	STOP
2F	XR51 (H)							
	CAL PA	CAL PB	RDY	P BSY	CALL	SELTD	CHK1	DCK1
30	XR51 (L)							
	BFBSY	ATTN	0	0	IFERA	IFERB	PA BSY	PB BSY
31	XR48 (H)							
	RUN BSY	RUN TRS	RUN ADP	DAT REQ MOD	XFSTOOP	CDFLG	CMPA	CMPB
32	Module ID							
33	Routine ID							
34	PCB number					Message code (x‘A’)		
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 = 0E (LCP Failure:Timeout) (2/2)

	0	1	2	3	4	5	6	7
38		Log and message control (x‘00’)						
39		Program action code (x‘00’)						
3A		Configuration information						
3B								
3C		Not used (x‘00’)						
3D		Cylinder address						
3E								
3F		Head address						
40		LCP error message (x‘0E’)						
41		Key code (x‘04’)						
42		LCP error code						
43								
44		x‘00’						
45		Command code						
46		x‘00’						
47		x‘00’						
48		Reason code						
49								
4A		XR49(H)						
	ESYCN	END	RDYOK	RDYRCV	0	CMDFRM	ACPRSP	DATAXF
4B		XR49(L)						
	XFREND	DEVEND	CNTFLG	EOF	CMPEQ	CMPGT	0	STOP
4C		XR51(H)						
	CAL PA	CAL PB	RDY	P BSY	CALL	SELTD	CHK1	DCK1
4D		XR51(L)						
	BFBSY	ATTN	0	0	IFERA	IFERB	PA BSY	PB BSY
4E		XR48(H)						
	RUN BSY	RUN TRS	RUN ADP	DAT REQ MOD	XFSTOP	CDFLG	CMPA	CMPB
4F		XR48(L)						
	DATA XF	RD / WR (0) (1)	1st CCW	RD/WR XFR	MEFLG	BBF SWEEP	BBIP INC	BBIP INC
50		Not used						
⋮								
7F								

(Note 1) Reason code

x‘FF01’ : (Read) Timeout in waiting for ACP CMD RSP
x‘FF02’ : (Read) Timeout in waiting for frame header
x‘FF03’ : (Read) Timeout in waiting for data frame
x‘FF04’ : (Read) Timeout in waiting for end of data transfer
x‘FF05’ : (Read) Timeout in waiting for data frame
x‘FF06’ : (Read) Timeout in waiting for end of data transfer
x‘FF07’ : (Read) Timeout in waiting for command frame
x‘FF08’ : (Read) Timeout in waiting for DATA REQ
x‘FF09’ : (Read) Timeout in waiting for status
x‘FFF1’ : (Write) Timeout in waiting for ACP CMD RSP
x‘FFF2’ : (Write) Timeout in waiting for first data
x‘FFF3’ : (Write) Timeout in waiting for frame header
x‘FFF4’ : (Write) Timeout in waiting for frame header
x‘FFF5’ : (Write) Timeout in waiting for frame header
x‘FFF6’ : (Write) Timeout in waiting for command frame
x‘FFF7’ : (Write) Timeout in waiting for frame header
x‘FFF8’ : (Write) Timeout in waiting for end of data transfer
x‘FFF9’ : (Write) Timeout in waiting for status

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 ≠ 01/02/0C/0E (LCP Failure:Others) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘8’)			
28	LCP error message (Note 1)							
29	LCP error code							
2A								
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							
31	Not used (x‘00’)							
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘A’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF88’ : LDEV type = DKU87I/x‘EF88’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 88 & Byte34:b4-7 = A & Byte28 ≠ 01/02/0C/0E (LCP Failure:Others) (2/2)

	0	1	2	3	4	5	6	7
40	LCP error message (Note 1)							
41	Key code (x‘04’)							
42	LCP error code							
43								
44	x‘00’							
45	Command code							
46	x‘00’							
47	x‘00’							
48	x‘00’							
49	x‘00’							
4A	x‘00’							
4B	x‘00’							
4C	x‘00’							
4D	x‘00’							
4E	x‘00’							
4F	x‘00’							
50	Not used							
7F								

(Note 1) LCP error message

x‘00’ : No message
x‘08’ : Transmission error
x‘09’ : Protocol error
x‘0D’ : Retry abort

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Byte27 = 89 & Byte0D Bit2 = 0 (ESCON CHA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	BasicSSB							
21								
22								
23	Count							
24	Device Address							
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘9’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

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Byte27 = 89 & Byte0D Bit2 ≠ 0 (FIBRE CHA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Inf valid	Err Code						
21	Segment Number							
22	Filemark	ECM	ILI	Reserved	Sense Key			
23	Information bytes							
24								
25								
26								
27	Format (x‘8’)				Message (x‘9’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Reserved							
33								
34	Module ID1							
35	Routine ID1							
36	Module ID2							
37	Routine ID2							
38	Master Path Number							
39	SCSI Initiator ID							
3A	SCSI Target ID							
3B	Logical Unit Number							
3C	SCSI Command Code							
3D	Processor Number							
3E	LDEV#							
33								
40	Detail Information (See Following Pages.)							
|								
7F								

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(1) Byte28 = 00

	0	1	2	3	4	5	6	7
28	SubCode (x'00' : ESCON I/F CHA - XFR CHK2)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::PDC							
	(RSV)	(RSV)	(RSV)	ENLPLTB 0:NORMAL 1:LIST XFR	(RSV)	(RSV)	(RSV)	(RSV)
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Tarnsfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(2) Byte28 = 01

	0	1	2	3	4	5	6	7
28	SubCode (x'01' : ESCON I/F CHA - Abnormal Cache Slot Status 1, (Note 1))							
29	Slot Status							
2A								
2B								
2C								
2D	WRITE in Progress	Make GAP	Execute ERASE	Update HA/R0	Update BM	(RSV)		
2E	SubBlock Number for Ready Response to Transfer							
2F	Start SubBlock Number for Incompletet Recode							
30	End SubBlock Number for Incompletet Recode							
31	Reserved							

(Note 1)Expect for cache ECC/LRC error has been detected in read side.
(Note2) (1) Module ID = 55 : After synchronous destage, cache slot with dirty attribute has been detected.
(2) Module ID ≠ 55 : In internal search or orientation process, incomplete subblock has been detected.

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(3) Byte28 = 02

	0	1	2	3	4	5	6	7
28	SubCode (x‘02’ : ESCON I/F CHA - Abnormal Cache Slot Status 2, (Note 1))							
29	Slot Status							
2A								
2B								
2C								
2D	WRITE in Progress	Make GAP	Execute ERASE	Update HA/R0	Update BM	(RSV)		
2E	SubBlock Number for Ready Response to Transfer							
2F	Start SubBlock Number for Processing Recode							
30	End SubBlock Number for Processing Recode							
31	Reserved							

(Note 1) Cache ECC/LRC error has been detected in read side.

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(4) Byte28 = 1F

	0	1	2	3	4	5	6	7
28	SubCode (x'1F' : ESCON I/F CHA - XFR TIME OUT)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::PDC							
	(RSV)	(RSV)	(RSV)	ENLPLTB 0:NORMAL 1:LIST XFR	(RSV)	(RSV)	(RSV)	(RSV)
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Tarnsfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(5) Byte28 = 20

	0	1	2	3	4	5	6	7
28	SubCode (x‘20’ : FICON I/F CHA - XFR CHK2)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::DCTL							
	M128 FLG	RUN	READ FLG	ASYNC FLG	CNP FLG	CD FLG	COF	MSW FLG
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Tarnsfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(6) Byte28 = 3F

	0	1	2	3	4	5	6	7
28	SubCode (x'3F' : FICON I/F CHA – TIME OUT)							
29	CHA::XFS0							
	TRANSFER END	(RSV)	(RSV)	PFC STATUS	CHK2	CHK2A	CHK2B	CHK2C
2A	CHA::XFS0							
	CHK2D	TRUNCA-TION	HALT I/O	SEARCH DASD= CPU	SEARCH DASD> CPU	SEARCH DASD< CPU	(RSV)	ABORT
2B	CHA::XFS1							
	(RSV)	(RSV)	(RSV)	(RSV)	MICRO ABORT	HARD ABORT	Force CHK1	Force CHK2
2C	CHA::XFS1							
	NEXT SEG ADR REG STATUS	(RSV)	(RSV)	(RSV)	(RSV)	NEXT SEG ADR WAIT	PFC ZERO	(RSV)
2D	CHA::DCTL							
	M128 FLG	RUN	READ FLG	ASYNC FLG	CNP FLG	CD FLG	COF	MSW FLG
2E	CHA::XFC0							
	ENBL XFR	EXEC XFR	(RSV)	(RSV)	(RSV)	CBP PNT INC STOP	CACHE I/O MODE	SSD MODE
2F	CHA::XFC0							
	Data Tarnsfer Path: 0:ESCON=>CACHE 2:ESCON=>CBUF 3:CBUF=>ESCON 4:CACHE=>ESCON 6:CACHE=>CBUF 7:CBUF=>ESCON 8:CACHE SEARCH 9:CBUF SEARCH B:CACHE COPY				U-MODE (504B SB FORMAT)	(RSV)	(RSV)	WR FBA MODE
30	CHA::XFC1							
	(RSV)	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(7) Byte28 = 60 ~ 7F

	0	1	2	3	4	5	6	7
28	SubCode (x‘60’ - x ‘7F’ : NAS I/F CHA – DMA CHK2 (Note 1))							
29	NDTM::XFC							
	XFR Mode: ‘00’:XFR Initialize ‘10’:XFR Abort ‘11’:XFR Start		CRC Mode: ‘00’:No CRC ‘10’:CRC Calculate (Cont.) ‘11’:CRC Calculate (New)		(RSV)	(RSV)	INT Mode: 0: Enable 1: Disable	(RSV)
2A	NDTM::XFC							
	Data XFR Path: 0: PCI=>CACHE, 1: PCI=>CACHE(2SLV) 2: DBF=>CACHE, 3: DBF=>CACHE(2SLV) 6: CACHE FORMAT, 7: CACHE FORMAT(2SLV) 8: CACHE=>PCI, 9: CACHE=>DBF C: CtoC COPY D: CinC COPY				PCI Mode: 0: Master 1: Target	PBF Mode: 0: No Fetch 1: Fetch	(RSV)	(RSV)
2B	NDTM::XFC							
	CHSN Data Format: ‘00’: Sub-Block ‘10’: I/O, no SLRC ‘11’: I/O, with LRC		(RSV)	(RSV)	MICRO ABORT	SLRC CHK: 0: Enable 1: Disable	SP Mode: 0: Normal 1: SP ACS	DIAG Mode: 0: Normal 1: DIAG ACS
2C	NDTM::XFC							
	REQID			PBF Chain: Chain Number= 1 ~ 32 (32: When Set as ‘0’)				
2D	XMPA::PnFINTS							
	(RSV)	(RSV)	Other DMA#0 XFR END	Other DMA#1 XFR END	Other DMA#2 XFR END	Other DMA#3 XFR END	Other DMA#4 XFR END	Other DMA#5 XFR END
2E	XMPA::PnFINTS							
	(RSV)	(RSV)	Own DMA#0 XFR END	Own DMA#1 XFR END	Own DMA#2 XFR END	Own DMA#3 XFR END	Own DMA#4 XFR END	Own DMA#5 XFR END
2F	XMPA::PnFINTS							
	(RSV)	(RSV)	Other DMA#0 CHK2AINT	Other DMA#1 CHK2AINT	Other DMA#2 CHK2AINT	Other DMA#3 CHK2AINT	Other DMA#4 CHK2AINT	Other DMA#5 CHK2AINT
30	XMPA::PnFINTS							
	(RSV)	ABORT	Own DMA#0 CHK2AINT	Own DMA#1 CHK2AINT	Own DMA#2 CHK2AINT	Own DMA#3 CHK2AINT	Own DMA#4 CHK2AINT	Own DMA#5 CHK2AINT
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) SubCode Bit 4: DMA# (‘0’:DMA#0/2, ‘1’:DMA#1/3)
SubCode Bit 5: CHSN CHK2 detected
SubCode Bit 6: DMA CHK2 detected
SubCode Bit 7: PCI CHK2 detected

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(8) Byte28 = 80, 81, 82, 83, 84, 85, 86, 87

	0	1	2	3	4	5	6	7
28	SubCode (x‘80’ - x‘87’ : FIBRE I/F CHA – DMA CHK2 (Note 1))							
29	FDTA::PnXFS							
	TRANSFER END	(RSV)	(RSV)	(RSV)	DMA CHK2B	DMA CHK2B	(RSV)	MP STOP0
2A	FDTA::PnXFS							
	MP STOP1	PCI CHK2A	PCI CHK2B0	PCI CHK2B1	PCI CHK2B2	PCI OVER RUN	(RSV)	HSN CHK2
2B	FDTA::PnXFS							
	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C
2C	FDTA::PnXFS							
	(RSV)	(RSV)	(RSV)	COMMON CHK2C	(RSV)	(RSV)	(RSV)	ABORT
2D	FDTA::PnXFC							
	XFR BIT ‘00’:XFR Initialize ‘10’:XFR ABORT ‘11’:XFR START		(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	INT SEL 0:CHP SEL 1:FOP SEL
2E	FDTA::PnXFC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	XFR SEL ‘000’:PCI DEVICE XFR ‘011’:16B - 128B CACHE ACCESS		
2F	FDTA::PnXFC							
	(RSV)	(RSV)	DATA FORMAT ‘00’:528B FORMAT ‘10’:16B-128B FORMAT	(RSV)	16 XFR CNT ‘000’:16B ACCESS ‘011’:64B ACCESS			
30	FDTA::PnXFC							
	(RSV)	(RSV)	XBF CHAIN (Transfer Chain Number :1 - 32)					
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) SubCode Bit 5: CHSN CHK2 detected
SubCode Bit 6: DMA CHK2 detected
SubCode Bit 7: PCI CHK2 detected

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Byte27 = 89 (CHA CHK2) Byte28-31 Detail
(9) Byte28 = 90, 91, 92, 93, 94, 95, 96, 97

	0	1	2	3	4	5	6	7
28	SubCode (x‘90’ - x‘97’ : FIBRE I/F CHA – PMA CHK2 (Note 1))							
29	FDTA::PnXFS							
	TRANSFER END	(RSV)	(RSV)	(RSV)	PMA CHK2B	PMA CHK2B	(RSV)	MP STOP0
2A	FDTA::PnXFS							
	MP STOP1	PCI CHK2A	PCI CHK2B0	PCI CHK2B1	PCI CHK2B2	PCI OVER RUN	(RSV)	HSN CHK2
2B	FDTA::PnXFS							
	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C	(RSV)	P0 CHK2A	P0 CHK2B	P0 CHK2C
2C	FDTA::PnXFS							
	(RSV)	(RSV)	(RSV)	COMMON CHK2C	(RSV)	(RSV)	(RSV)	ABORT
2D	FDTA::PnXFC							
	XFR BIT ‘00’:XFR Initialize ‘01’:XFR ABORT ‘10’:XFR START		(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	INT SEL 0:CHP SEL 1:FOP SEL
2E	FDTA::PnXFC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	XFR SEL ‘010’: DEBUG MODE CACHE ACCESS ‘011’: 16B - 128B CACHE ACCESS		
2F	FDTA::PnXFC							
	(RSV)	(RSV)	DATA FORMAT ‘10’:NO FLRC FORMAT ‘11’:FLRC FORMAT	(RSV)	16 XFR CNT ‘000’:16B ACCESS ‘011’:64B ACCESS			
30	FDTA::PnXFC							
	(RSV)	(RSV)	XBF CHAIN (Transfer Chain Number :1 - 32)					
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) SubCode Bit 5: CHSN CHK2 detected
SubCode Bit 6: PMA CHK2 detected
SubCode Bit 7: PCI CHK2 detected

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40		CHA::CK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNME-NT ERR
41		CHA::CK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)
42		CHA::CK2AST2						
	PLIST XFR SEQ PARITY ERR	XR SET XFR SEQ PARITY ERR	PLIST OUT PARITY ERR	PLIST IN PARITY ERR	CBP CNT PARITY ERR	CBUF CKDDL PARITY ERR	TBP PARITY ERR	XFR MODE ERR
43		CHA::CK2AST2						
	(RSV)	LCM CKDDL PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		CHA::CK2AST1						
	FBADL PARITY ERR	SGOP PARITY ERR	PFC PARITY ERR	WRBF CNT PARITY ERR	RDBF CNT PARITY ERR	PACKET SEQ PARITY ERR	UNMATCH ERR0	UNMATCH ERR1
45		CHA::CK2AST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		CHA::CK2AST1						
	SOP PARITY ERR	BOP PARITY ERR	CKDFBA CNG CKDDL PARITY ERR	CKDFBA CNG SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
47		CHA::CK2AST1						
	SLAVE1 NEXTSEG ADR PARITY ERR	SLAVE1 HSN ADR PARITY ERR	SLAVE2 NEXTSEG ADR PARITY ERR	SLAVE2 HSN ADR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
48		CHA::CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
49		CHA::CHK2ASTS						
	P0 Recive PARITY ERR	P1 Recive PARITY ERR	X0 Recive PARITY ERR	X1 Recive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
4A		CHA::CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
4B		CHA::CHK2ASTS						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		CHA::ADP_CK21						
	SR0 PARITY ERR	CMWAD PARITY ERR	CMWD PARITY ERR	TSEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
4D		CHA::ADP_CK22						
	LCM-A DATA PARITY ERR	LCM-B DATA PARITY ERR	LCM-C DATA PARITY ERR	LCM-D DATA PARITY ERR	LCM-E DATA PARITY ERR	LCM-F DATA PARITY ERR	LCM-G DATA PARITY ERR	LCM-H DATA PARITY ERR
4E		CHA::CHK2DSTS						
	P0 ERR	P1 ERR	CARB	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50	CHA_CHK2CSTS							
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
51	CHA_CHK2CSTS							
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	(RSV)	(RSV)	STATUS0 PKID ERR	STATUS1 PKID ERR
52	CHA_CHK2CSTS							
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
53	CHA_CHK2CSTS							
	X1 Send PARITY ERR	STATUS0 CARB PARITY ERR	STATUS0 CMA PARITY ERR	STATUS1 CARB PARITY ERR	STATUS1 CMA PARITY ERR	(RSV)	(RSV)	(RSV)
54	CHA::ADP_SELP							
	LCM-A SELECT	LCM-B SELECT	LCM-C SELECT	LCM-D SELECT	LCM-E SELECT	LCM-F SELECT	LCM-G SELECT	LCM-H SELECT
55	CHA::ADP_EALT							
	LCP-A CHK1 Detected	LCP-B CHK1 Detected	LCP-C CHK1 Detected	LCP-D CHK1 Detected	LCP-E CHK1 Detected	LCP-F CHK1 Detected	LCP-G CHK1 Detected	LCP-H CHK1 Detected
56	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	CHA::CBP							
	CBUF Data Transfer Start Address							
58	CHA::CKDDL							
	Transfer Data Length(CKD)							
59	CHA::CKDDL							
	Transfer Data Length(CKD)							
5A	CHA::FBADL							
	Transfer Data Length(FBA)							
5B	CHA::FBADL							
	Transfer Data Length(FBA)							
5C	CHA::PDS							
	PLIST MEM FULL	(RSV)	(RSV)	(RSV)	PLHLD NE0	PLHLD EQ0	(RSV)	(RSV)
5D	CHA::PLIN							
	PLIST Setting Parameter Memory Page Pointer (BYTE0)							
5E	CHA::PLOUT							
	Parameter Decoder Processing PLIST Page Pointer (BYTE0)							
5F	CHA::PFC							
	Packet Frow Counter (Packet Number Able to Transfer)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE0)							
61	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE1)							
62	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE2)							
63	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE3)							
64	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE0)							
65	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE1)							
66	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE2)							
67	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE3)							
68	CHA::CSPGR							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
69	CHA::CSPGR							
	Slave 1 REG Access Flag	Slave 1 CARB Access Flag	(RSV)	(RSV)	Slave 2 REG Access Flag	Slave 2 CARB Access Flag	(RSV)	(RSV)
6A	CHA::PCMD1 CACHE Transfer Command (BYTE0)							
6B	CHA::PCMD1 CACHE Transfer Command (BYTE1)							
6C	CHA::PCMD2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6D	CHA::PCMD2 CACHE Transfer Command (BYTE2)							
6E	CHA::LPEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE
6F	CHA::IMPZREF0							
	IMP Setting Value for LSI_UP Side High-Level				IMP Setting Value for LSI_UP Side Low-Level			

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(1) Byte28 = 00/1F and Byte32 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70	CHA::LA0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71	CHA::LA0							
	LA Expected Value (BYTE0)							
72	CHA::LA1							
	LA Expected Value (BYTE1)							
73	CHA::LA1							
	LA Expected Value (BYTE2)							
74	CHA::LA2							
	LA Expected Value (BYTE3)							
75	CHA::LA2							
	LA Expected Value (BYTE4)							
76	CHA::SOP							
	Subblock Offset Pointer							
77	CHA::SOP							
	Subblock Offset Pointer							
78	CHA::BOP							
	Block Offset Pointer							
79	CHA::BOP							
	Block Offset Pointer							
7A	CHA::POP							
	Packet Offset Pointer							
7B	CHA::POP							
	Packet Offset Pointer							
7C	CHA::SGOP							
	Segment Offset Pointer							
7D	CHA::SGOP							
	Segment Offset Pointer							
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail

(2) Byte28 = 00/01/02/1F/20/3F and Byte32 ≠ 58/59 and Byte42 = 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		VDEV and slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		Information of Micro Program						
4D								
4E								
4F								
50		Internal Siearch Parameter (Cylinder number)						
51								
52		Internal Siearch Parameter (Head number)						
53		Internal Siearch Parameter (Reacord number)						
54		Information of Micro Program						
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C		Record number in CBUF						
7D		Key Length in CBUF						
7E		Data Length in CBUF						
7F								

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail

(3) Byte28 = 00/01/02/1F20/3F and Byte32 ≠ 58/59 and Byte42 ≠ 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		Information of Micro Program						
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 20/3F and Byte32 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40		CHA::CK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNME-NT ERR
41		CHA::CK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)
42		CHA::CK2AST2						
	PLIST XFR SEQ PARITY ERR	XR SET XFR SEQ PARITY ERR	PLIST OUT PARITY ERR	PLIST IN PARITY ERR	CBP CNT PARITY ERR	CBUF CKDDL PARITY ERR	TBP PARITY ERR	XFR MODE ERR
43		CHA::CK2AST2						
	(RSV)	LCM CKDDL PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		CHA::CK2AST1						
	FBADL PARITY ERR	SGOP PARITY ERR	PFC PARITY ERR	WRBF CNT PARITY ERR	RDBF CNT PARITY ERR	PACKET SEQ PARITY ERR	UNMATCH ERR0	UNMATCH ERR1
45		CHA::CK2AST1						
	SOP PARITY ERR	BOP PARITY ERR	CKDFBA CNG CKDDL PARITY ERR	CKDFBA CNG SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
46		CHA::CK2AST1						
	SLAVE1 NEXTSEG ADR PARITY ERR	SLAVE1 HSN ADR PARITY ERR	SLAVE2 NEXTSEG ADR PARITY ERR	SLAVE2 HSN ADR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
47		CHA::CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
48		CHA::CHK2ASTS						
	P0 Recive PARITY ERR	P1 Recive PARITY ERR	X0 Recive PARITY ERR	X1 Recive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
49		CHA::CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
4A		CHA_CHK2CSTS						
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
4B		CHA_CHK2CSTS						
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	S1BEP	S2BEP	STATUS0 PKID ERR	STATUS1 PKID ERR
4C		CHA_CHK2CSTS						
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
4D		CHA::DXBFERR0						
	SEQ PARITY ERR	TIMER CHK ERR	RD PATH SEL PARITY ERR	RD ADR PARITY ERR	RD CNT PARITY ERR	RD DATA PARITY ERR	(RSV)	(RSV)
4E		CHA::DXBFERR0						
	BBOP PARITY ERR	(RSV)	WT PATH SEL PARITY ERR	WT ADR PARITY ERR	WT CNT PARITY ERR	(RSV)	DXBF ECC 1BIT ERR	DXBF 2BIT ERR
4F		CHA::CBP						
		CBUF Data Transfer Start Address						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 20/3F and Byte32 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50	CHA::CKDDL Transfer Data Length(CKD)							
51	CHA::CKDDL Transfer Data Length(CKD)							
52	CHA::FBADL Transfer Data Length(FBA)							
53	CHA::FBADL Transfer Data Length(FBA)							
54	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE0)							
55	CHA::MCSA00 Slave 1 CACHE Tranfer Address (BYTE1)							
56	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE2)							
57	CHA::MCSA01 Slave 1 CACHE Tranfer Address (BYTE3)							
58	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE0)							
59	CHA::SCSA00 Slave 2 CACHE Tranfer Address (BYTE1)							
5A	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE2)							
5B	CHA::SCSA01 Slave 2 CACHE Tranfer Address (BYTE3)							
5C	CHA::CSPGR							
	Slave 1 REG Access Flag	Slave 1 CARB Access Flag	(RSV)	(RSV)	Slave 2 REG Access Flag	Slave 2 CARB Access Flag	(RSV)	(RSV)
5D	CHA::POP Packet Offset Pointer							
5E	CHA::PCMD2 CACHE Transfer Command (BYTE2)							
5F	CHA::LA0 LA Expected Value (BYTE0)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 =20/3F and Byte32 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60		CHA::LA1						
		LA Expected Value (BYTE1)						
61		CHA::LA1						
		LA Expected Value (BYTE2)						
62		CHA::LA2						
		LA Expected Value (BYTE3)						
63		CHA::LA2						
		LA Expected Value (BYTE4)						
64		CHA::SOP						
		Subblock Offset Pointer						
65		CHA::SOP						
		Subblock Offset Pointer						
66		CHA::BOP						
		Block Offset Pointer						
67		CHA::BOP						
		Block Offset Pointer						
68		CHA::LPEN						
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
69		CHA::LPEN						
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
6A		CHA::SGOP						
		Segment Offset Pointer						
6B		CHA::SGOP						
		Segment Offset Pointer						
6C		CHA::BBP						
		BBF Pointer						
6D		CHA::BBP						
		BBF Pointer						
6E		CHA::BBP						
		BBF Pointer						
6F		CHA::BBP						
		BBF Pointer						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(4) Byte28 = 20/3F and Byte32 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70		CHA::PFC Packet Flow Counter						
71		CHA::DXOP DXBF OUTPUT Pointer						
72		CHA::DXOP DXBF OUTPUT Pointer						
73		CHA::DXOP DXBF OUTPUT Pointer						
74		CHA::CADR DXBF Current Address						
75		CHA::CADR DXBF Current Address						
76		CHA::CADR DXBF Current Address						
77		CHA::DXIP DXBF INPUT Pointer						
78		CHA::DXIP DXBF INPUT Pointer						
79		CHA::DXIP DXBF INPUT Pointer						
7A		CHA::DCTL DXBF TRF Counter						
7B		CHA::DCTL DXBF TRF Counter						
7C		CHA::RCCNT ASYNC XFR RC Counter						
7D		CHA::RCCNT ASYNC XFR RC Counter						
7E		CHA::DIB DIB Counter						
7F		CHA::DIB DIB Counter						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 80 or 83 or 85 or 87 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x'01'						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		FDTA::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
46		FDTA::PCICHK2A						
	MWB8B PARITY GEN ERR	MWB4B PARITY GEN ERR	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
47		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTA::PCICHK2B0						
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
4A		FDTA::PCICHK2B0						
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
4B		FDTA::PCICHK2B0						
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	DBF 16BI PARITY ERR	DBF 16B0 PARITY ERR	(RSV)
4C		FDTA::PCICHK2B0						
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
4D		FDTA::PCICHK2B1						
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	MRB8B PARITY GEN ERR	MRB4B PARITY GEN ERR	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
4E		FDTA::PCICHK2B1						
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	PWD LRC ERR
4F		FDTA::PCICHK2B1						
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 80 or 83 or 85 or 87 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::PCICHK2B1							
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
51	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
52	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	INV MEMACS ERR	CRC POINTER ERR	DWA CMP ERR	DRA CMP ERR
54	FDTA::PCICHK2B2							
	DBF WT ACSERR	DBF RD ACSERR	DMA DSTT ERR	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
55	FDTA::DMACHK2BST0							
	DMA TJ0 PARITY ERR	DMA TJ1 PARITY ERR	DMA TJ2 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	FDTA::DMACHK2BST0							
	CHAIN CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	FDTA::DMACHK2CST0							
	HSN ADR CNT1 PARITY ERR0	HSN ADR CNT1 PARITY ERR1	HSN ADR CNT1 PARITY ERR2	HSN ADR CNT1 PARITY ERR3	HSN ADR CNT1 PARITY ERR4	(RSV)	(RSV)	(RSV)
58	FDTA::DMACHK2CST0							
	HSN ADR CNT2 PARITY ERR0	HSN ADR CNT2 PARITY ERR1	HSN ADR CNT2 PARITY ERR2	HSN ADR CNT2 PARITY ERR3	HSN ADR CNT2 PARITY ERR4	(RSV)	(RSV)	(RSV)
59	FDTA::DMACHK2CST0							
	SUB BLOCK PARITY ERR	SUB BLOCK CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::DMACHK2CST0							
	XBF CMD PARITY ERR	LA CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	FDTA::DMACHK2CST1							
	HSN RD ADR CNT PARITY ERR	HSN WT ADR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	FDTA::DMACHK2CST1							
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	FDTA::DMACHK2CST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIME OUT
5E	FDTA::DMACHK2CST2							
	SDBF0 PARITY ERR	SDBF1 PARITY ERR	SDBF2 PARITY ERR	SDBF3 PARITY ERR	SDLRC ERR	DBF PARITY ERR	XBF BLOCKCODE ERR	XBF PARITY ERR
5F	FDTA::DMACHK2CST2							
	SLRC GEN PARITY ERR	SLRC CHK PARITY ERR	LA ERR	SLRC ERR	(RSV)	(RSV)	RAID MODE ERR	BLKBD ACSERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 80 or 83 or 85 or 87 (3/4)

	0	1	2	3	4	5	6	7
60	FDTA::DMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	(RSV)	(RSV)	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
61	FDTA::DMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIMER PARITY ERR	(RSV)	(RSV)	DMA SEQ PARITY ERR
62	FDTA::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
63	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
64	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
65	FDTA::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
66	FDTA::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
67	FDTA::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
68	FDTA::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
69	FDTA::H0CHK2CST2							
	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
6A	FDTA::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
6B	FDTA::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
6C	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
6D	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
6E	FDTA::H1CHK2BST2							
0	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
6F	FDTA::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(5) Byte28 = 80 or 83 or 85 or 87 (4/4)

	0	1	2	3	4	5	6	7
70	FDTA::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
71	FDTA::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
72	FDTA::H1CHK2CST2							
	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	FDTA::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
74	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
76	FDTA::PnMSADR							
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
78	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	FDTA::MONI							
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Micro Information							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 DMA#
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 81 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x‘02’						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		XPA::PnXERR0						
	(RSV)	PX RD RSP CNT ERR	XR DMA ACS ERR	XR DMA CNT ERR	PX RD RSP TOV	XR DMA LRC ERR	XR ADR PARITY ERR	XR WR DATA PARITY ERR
46		XPA::PnXERR0						
	(RSV)	(RSV)	PCI Master ADR CNT PARITY ERR	PCI Master ADR PARITY ERR	PCI Master SEQ ERR	PCI Master RD PARITY ERR	PCI Master PERR IN	PCI Master PERR OUT
47		XPA::PnXERR0						
	(RSV)	PCI Target100 ADR CNT ERR	PCI Target66 ADR CNT ERR	PCI Target SEQ ERR	(RSV)	PCI Target RD PARITY ERR	PCI Target PERR IN	PCI Master PERR OUT
48		XPA::PnXERR0						
	XR TRG SEQ ERR	(RSV)	(RSV)	XR Master ADR PARITY ERR	XR Target ADR CNT PARITY ERR	XR DMA RD PARITY ERR	XR TOV	XR RD PARITY ERR
49		XPA::PnDIG0						
		Diag Reg 0						
4A		XPA::PnDIG0						
		Diag Reg 0						
4B		XPA::PnDIG0						
		Diag Reg 0						
4C		XPA::PnDIG0						
		Diag Reg 0						
4D		XPA::PnDIG1						
		Diag Reg 1						
4E		XPA::PnDIG1						
		Diag Reg 1						
4F		XPA::PnDIG1						
		Diag Reg 1						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 81 (2/4)

	0	1	2	3	4	5	6	7
50		XPA::PnDIG1						
		Diag Reg 1						
51		XPA::PnSC						
	DETECTED PARITY ERR	SIGNALED SYSTEM ERR	RECEIVED MASTER ABORT	RECEIVED TARGET ABORT	(RSV)	DEVSEL TIMING 01: Medium		DATA PARITY REPORT
52		XPA::PnSC						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53		XPA::PnSC						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		XPA::PnSC						
	(RSV)	ENABLE PARITY RSP	(RSV)	(RSV)	(RSV)	ENABLE BUS MASERING	ENABLE MEMORY SPACE	ENABLE I/O SPACE
55		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XR Target RD 3 PARITY ERR	XR Target RD 2 PARITY ERR	XR Target RD 1 PARITY ERR	XR Target RD 0 PARITY ERR
56		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XP WR LRC ERR	XP RD LRC ERR	PX WR LRC ERR	PCI DATA IN PARITY ERR
57		XPA::PnXERR1						
	XR Master ADR 3 PARITY ERR	XR Master ADR 2 PARITY ERR	XR Master ADR 1 PARITY ERR	XR Master ADR 0 PARITY ERR	XP DMA DATA OUT 3 PARITY ERR	XP DMA DATA OUT 2 PARITY ERR	XP DMA DATA OUT 1 PARITY ERR	XP DMA DATA OUT 0 PARITY ERR
58		XPA::PnXERR1						
	XR Target ADR 3 PARITY ERR	XR Target ADR 2 PARITY ERR	XR Target ADR 1 PARITY ERR	XR Target ADR 0 PARITY ERR	XR Target WR DATA 3 PARITY ERR	XR Target WR DATA 2 PARITY ERR	XR Target WR DATA 1 PARITY ERR	XR Target WR DATA 0 PARITY ERR
59		XPA::PnDIG2						
		Diag Reg 2						
5A		XPA::PnDIG2						
		Diag Reg 2						
5B		XPA::PnDIG2						
		Diag Reg 2						
5C		XPA::PnDIG2						
		Diag Reg 2						
5D		CXL::CFGSTAT						
		PCI Configuration Reg. STATUS(Hi)						
5E		CXL::CFGSTAT						
		PCI Configuration Reg. STATUS (Lo)						
5F		CXL::CFGCMD						
		PCI Configuration Reg. COMMAND (Hi)						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 81 (3/4)

	0	1	2	3	4	5	6	7
60		CXL::CFGCMD						
		PCI Configuration Reg. COMMAND (Lo)						
61		FDTA::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
62		FDTA::PCICHK2A						
	(RSV)	(RSV)	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
63		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		FDTA::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65		FDTA::PCICHK2B0						
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
66		FDTA::PCICHK2B0						
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
67		FDTA::PCICHK2B0						
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	DBF 16BI PARITY ERR	DBF 16B0 PARITY ERR	(RSV)
68		FDTA::PCICHK2B0						
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
69		FDTA::PCICHK2B1						
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	MRB8B PARITY GEN ERR	MRB4B PARITY GEN ERR	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
6A		FDTA::PCICHK2B1						
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	PWD LRC ERR
6B		FDTA::PCICHK2B1						
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11
6C		FDTA::PCICHK2B1						
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
6D		FDTA::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E		FDTA::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F		FDTA::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	INV MEMACS ERR	CRC POINTER ERR	DWA CMP ERR	DRA CMP ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(6) Byte28 = 81 (4/4)

	0	1	2	3	4	5	6	7
70	FDTA::PCICHK2B2							
	DBF WT ACSERR	DBF RD ACSERR	DMA DSTT ERR	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
71	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	FDTA::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
73	FDTA::HCMD							
	CACHE Transfer Command (BYTE0)							
74	FDTA::HCMD							
	CACHE Transfer Command (BYTE1)							
75	FDTA::HCMD							
	CACHE Transfer Command (BYTE2)							
76	FDTA::PnMSADR							
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
78	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	FDTA::MONI							
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Micro Information							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 DMA#
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 80 or 82 or 84 or 86 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x'03'						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		FDTA::DMACHK2BST0						
	DMA TJ0 PARITY ERR	DMA TJ1 PARITY ERR	DMA TJ2 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		FDTA::DMACHK2BST0						
	CHAIN CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		FDTA::DMACHK2CST0						
	HSN ADR CNT1 PARITY ERR0	HSN ADR CNT1 PARITY ERR1	HSN ADR CNT1 PARITY ERR2	HSN ADR CNT1 PARITY ERR3	HSN ADR CNT1 PARITY ERR4	(RSV)	(RSV)	(RSV)
48		FDTA::DMACHK2CST0						
	HSN ADR CNT2 PARITY ERR0	HSN ADR CNT2 PARITY ERR1	HSN ADR CNT2 PARITY ERR2	HSN ADR CNT2 PARITY ERR3	HSN ADR CNT2 PARITY ERR4	(RSV)	(RSV)	(RSV)
49		FDTA::DMACHK2CST0						
	SUB BLOCK PARITY ERR	SUB BLOCK CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4A		FDTA::DMACHK2CST0						
	XBF CMD PARITY ERR	LA CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		FDTA::DMACHK2CST1						
	HSN RD ADR CNT PARITY ERR	HSN WT ADR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTA::DMACHK2CST1						
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTA::DMACHK2CST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIME OUT
4E		FDTA::DMACHK2CST2						
	SDBF0 PARITY ERR	SDBF1 PARITY ERR	SDBF2 PARITY ERR	SDBF3 PARITY ERR	SDLRC ERR	DBF PARITY ERR	XBF BLOCKCODE ERR	XBF PARITY ERR
4F		FDTA::DMACHK2CST2						
	SLRC GEN PARITY ERR	SLRC CHK PARITY ERR	LA ERR	SLRC ERR	(RSV)	(RSV)	RAID MODE ERR	BLKBD ACSERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 80 or 82 or 84 or 86 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::DMACHK2CST2							
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	(RSV)	(RSV)	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
51	FDTA::DMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	DMA TIMER PARITY ERR	(RSV)	(RSV)	DMA SEQ PARITY ERR
52	FDTA::H0CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
53	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
54	FDTA::H0CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
55	FDTA::H0CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
56	FDTA::H0CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
57	FDTA::H0CHK2CST0							
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
58	FDTA::H0CHK2CST1							
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
59	FDTA::H0CHK2CST2							
	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::H0CHK2CST2							
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
5B	FDTA::H1CHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
5C	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
5D	FDTA::H1CHK2BST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
5E	FDTA::H1CHK2BST2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
5F	FDTA::H1CHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 80 or 82 or 84 or 86 (3/4)

	0	1	2	3	4	5	6	7
60	FDTA::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
61	FDTA::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
62	FDTA::H1CHK2CST2							
	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	FDTA::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
64	FDTA::HADR1UCNT							
	Slave 1 CACHE Tranfer Address (BYTE0)							
65	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE1)							
66	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE2)							
67	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE3)							
68	FDTA::HADR1LCNT							
	Slave 1 CACHE Tranfer Address (BYTE4)							
69	FDTA::HADR2UCNT							
	Slave 2 CACHE Tranfer Address (BYTE0)							
6A	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE1)							
6B	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE2)							
6C	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE3)							
6D	FDTA::HADR2LCNT							
	Slave 2 CACHE Tranfer Address (BYTE4)							
6E	FDTA::HCMD							
	CACHE Tranfer Command (BYTE0)							
6F	FDTA::HCMD							
	CACHE Tranfer Command (BYTE1)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(7) Byte28 = 80 or 82 or 84 or 86 (4/4)

	0	1	2	3	4	5	6	7
70		FDTA::HCMD						
		CACHE Tranfer Command (BYTE2)						
71		FDTA::LA0						
		LA Expected Value (BYTE0)						
72		FDTA::LA1						
		LA Expected Value (BYTE1)						
73		FDTA::LA1						
		LA Expected Value (BYTE2)						
74		FDTA::LA1						
		LA Expected Value (BYTE3)						
75		FDTA::LA1						
		LA Expected Value (BYTE4)						
76		FDTA::PnMSADR						
	(RSV)	(RSV)	(RSV)	XBF Data Transfer Parameter Address (x‘00’ - x‘1F’)				
77		FDTA::CBEN						
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
78		FDTA::CBEN						
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
79		FDTA::PKID						
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A		FDTA::MONI						
	MPID#				LSI REV.			
7B		FDTA::MONI						
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 DMA#
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 90 or 93 or 95 or 97 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x'11'						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		FDTM::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	PMA MRB0 PARITY ERR	PMA MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
46		FDTM::PCICHK2A						
	PMA MRB8B PARITY GEN ERR	PMA MWB4B PARITY GEN ERR	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
47		FDTM::PCICHK2A						
	PRFLRC PARITY ERR	PRFLRC ERR	PRA CMP ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTM::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTM::PCICHK2B0						
	PPACNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	PPBFIN PARITY ERR	PCIPBF PARITY ERR	PBFOUT PARITY ERR
4A		FDTM::PCICHK2B0						
	PWTRFCNT PARITY ERR	PWFLRC PARITY ERR	PRTRFCNT PARITY ERR	PRFLRC PARITY ERR	PRFLRC ERR	(RSV)	(RSV)	(RSV)
4B		FDTM::PCICHK2B0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTM::PCICHK2B0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	PMA MRB8B PARITY GEN ERR	PMA MRB4B PARITY GEN ERR	(RSV)	(RSV)	(RSV)
4E		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F		FDTM::PCICHK2B1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 90 or 93 or 95 or 97 (2/4)

	0	1	2	3	4	5	6	7
50	FDTA::PCICHK2B1							
	(RSV)	(RSV)	PMA MRB0 PARITY ERR	PMA MRB1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
51	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
52	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53	FDTA::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PWA CMP ERR	PRA CMP ERR
54	FDTA::PCICHK2B2							
	PBF WT ACS ERR	PBF RD ACS ERR	PMA DSTT ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
55	FDTA::PMACHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	FDTA::PMACHK2BST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
57	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
58	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
59	FDTA::PMACHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5A	FDTA::PMACHK2CST0							
	HSN CMD LOAD PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B	FDTA::PMACHK2CST1							
	HSN RD ADR CNT PARITY ERR	HSN WT ADRR CNT PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C	FDTA::PMACHK2CST1							
	PWB LRC PARITY ERR0	PWB LRC PARITY ERR1	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	FDTA::PMACHK2CST1							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PMA TIME OUT
5E	FDTA::PMACHK2CST2							
	TX FLRC ERR	TXFLRC PARITY ERR	RX FLRC PARITY ERR	RX FLRC PARITY ERR	PBF0 PARITY ERR	PBF1 PARITY ERR	PBF2 PARITY ERR	PBF3 PARITY ERR
5F	FDTA::PMACHK2CST2							
	(RSV)	(RSV)	(RSV)	(RSV)	PMA ACCMD ERR	XFC MODE ERR	RAID MODE ERR	BLK MODE ACSERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 90 or 93 or 95 or 97 (3/4)

	0	1	2	3	4	5	6	7
60		FDTM::PMACHK2CST2						
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	TX FLRC 0 PADDING ERR	RX FLRC 0 PADDING ERR	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
61		FDTM::PMACHK2CST2						
	HSN PBF IN PARITY ERR	(RSV)	(RSV)	(RSV)	PMA TIMER PARITY ERR	(RSV)	PMA ARB SEQ PARITY ERR	PMA SEQ PARITY ERR
62		FDTM::H0CHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
63		FDTM::H0CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
64		FDTM::H0CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
65		FDTM::H0CHK2BST2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
66		FDTM::H0CHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
67		FDTM::H0CHK2CST0						
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
68		FDTM::H0CHK2CST1						
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
69		FDTM::H0CHK2CST2						
	(RSV)	(RSV)	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
6A		FDTM::H0CHK2CST2						
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
6B		FDTM::H1CHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
6C		FDTM::H1CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
6D		FDTM::H1CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
6E		FDTM::H1CHK2BST2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
6F		FDTM::H1CHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(8) Byte28 = 90 or 93 or 95 or 97 (4/4)

	0	1	2	3	4	5	6	7
70	FDTM::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
71	FDTM::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
72	FDTM::H1CHK2CST2							
	(RSV)	(RSV)	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	P1 PRBPTR 0 CMP ERR	P1 PRBPTR 1 CMP ERR	P1 PRBPTR 0 PARITY ERR	P1 PRBPTR 1 PARITY ERR
73	FDTM::H1CHK2CST2							
	P1 RX TIMER0 PARITY ERR	P1 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 RX PTR PARITY ERR	P1 RX CNT PARITY ERR	(RSV)	P1 RX SEQ PARITY ERR
74	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
76	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
78	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
79	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A	FDTA::MONI							
	MPID#				LSI REV.			
7B	FDTA::MONI							
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 91 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x‘12’						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		XPA::PnXERR0						
	(RSV)	PX RD RSP CNT ERR	XR DMA ACS ERR	XR DMA CNT ERR	PX RD RSP TOV	XR DMA LRC ERR	XR ADR PARITY ERR	XR WR DATA PARITY ERR
46		XPA::PnXERR0						
	(RSV)	(RSV)	PCI Master ADR CNT PARITY ERR	PCI Master ADR PARITY ERR	PCI Master SEQ ERR	PCI Master RD PARITY ERR	PCI Master PERR IN	PCI Master PERR OUT
47		XPA::PnXERR0						
	(RSV)	PCI Target100 ADR CNT ERR	PCI Target66 ADR CNT ERR	PCI Target SEQ ERR	(RSV)	PCI Target RD PARITY ERR	PCI Target PERR IN	PCI Master PERR OUT
48		XPA::PnXERR0						
	XR TRG SEQ ERR	(RSV)	(RSV)	XR Master ADR PARITY ERR	XR Target ADR CNT PARITY ERR	XR DMA RD PARITY ERR	XR TOV	XR RD PARITY ERR
49		XPA::PnDIG0						
		Diag Reg 0						
4A		XPA::PnDIG0						
		Diag Reg 0						
4B		XPA::PnDIG0						
		Diag Reg 0						
4C		XPA::PnDIG0						
		Diag Reg 0						
4D		XPA::PnDIG1						
		Diag Reg 1						
4E		XPA::PnDIG1						
		Diag Reg 1						
4F		XPA::PnDIG1						
		Diag Reg 1						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 91 (2/4)

	0	1	2	3	4	5	6	7
50		XPA::PnDIG1						
		Diag Reg 1						
51		XPA::PnSC						
	DETECTED PARITY ERR	SIGNALED SYSTEM ERR	RECEIVED MASTER ABORT	RECEIVED TARGET ABORT	(RSV)	DEVSEL TIMING 01: Medium		DATA PARITY REPORT
52		XPA::PnSC						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
53		XPA::PnSC						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		XPA::PnSC						
	(RSV)	ENABLE PARITY RSP	(RSV)	(RSV)	(RSV)	ENABLE BUS MASERING	ENABLE MEMORY SPACE	ENABLE I/O SPACE
55		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XR Target RD 3 PARITY ERR	XR Target RD 2 PARITY ERR	XR Target RD 1 PARITY ERR	XR Target RD 0 PARITY ERR
56		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XP WR LRC ERR	XP RD LRC ERR	PX WR LRC ERR	PCI DATA IN PARITY ERR
57		XPA::PnXERR1						
	XR Master ADR 3 PARITY ERR	XR Master ADR 2 PARITY ERR	XR Master ADR 1 PARITY ERR	XR Master ADR 0 PARITY ERR	XP DMA DATA OUT 3 PARITY ERR	XP DMA DATA OUT 2 PARITY ERR	XP DMA DATA OUT 1 PARITY ERR	XP DMA DATA OUT 0 PARITY ERR
58		XPA::PnXERR1						
	XR Target ADR 3 PARITY ERR	XR Target ADR 2 PARITY ERR	XR Target ADR 1 PARITY ERR	XR Target ADR 0 PARITY ERR	XR Target WR DATA 3 PARITY ERR	XR Target WR DATA 2 PARITY ERR	XR Target WR DATA 1 PARITY ERR	XR Target WR DATA 0 PARITY ERR
59		XPA::PnDIG2						
		Diag Reg 2						
5A		XPA::PnDIG2						
		Diag Reg 2						
5B		XPA::PnDIG2						
		Diag Reg 2						
5C		XPA::PnDIG2						
		Diag Reg 2						
5D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5E		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 91 (3/4)

	0	1	2	3	4	5	6	7
60		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61		FDTM::PCICHK2A						
	MWB8B PARITY ERR	MWB4B PARITY ERR	MWB8B PARITY GEN CHK ERR	MWB4B PARITY GEN CHK ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	(RSV)	PCI IN PARITY ERR
62		FDTM::PCICHK2A						
	(RSV)	(RSV)	PCI ADR PARITY ERR	PCI ADR PARITY GEN CHK ERR	(RSV)	(RSV)	(RSV)	PCI IN SERR
63		FDTM::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		FDTM::PCICHK2A						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65		FDTM::PCICHK2B0						
	DBF0 B0 PARITY ERR	DBF0 B1 PARITY ERR	DBF0 B2 PARITY ERR	DBF0 B3 PARITY ERR	DBF0 B4 PARITY ERR	DBF0 B5 PARITY ERR	DBF0 B6 PARITY ERR	DBF0 B7 PARITY ERR
66		FDTM::PCICHK2B0						
	DBF1 B0 PARITY ERR	DBF1 B1 PARITY ERR	DBF1 B2 PARITY ERR	DBF1 B3 PARITY ERR	DBF1 B4 PARITY ERR	DBF1 B5 PARITY ERR	DBF1 B6 PARITY ERR	DBF1 B7 PARITY ERR
67		FDTM::PCICHK2B0						
	DBF IN PARITY ERR 00	DBF IN PARITY ERR 01	DBF IN PARITY ERR 10	DBF IN PARITY ERR 11	(RSV)	(RSV)	(RSV)	(RSV)
68		FDTM::PCICHK2B0						
	XBF B0 PARITY ERR	XBF B1 PARITY ERR	XBF B2 PARITY ERR	XBF B3 PARITY ERR	(RSV)	(RSV)	(RSV)	XBF IN PARITY ERR
69		FDTM::PCICHK2B1						
	PCI SEQ PARITY ERR	WTBDF SEQ PARITY ERR	WTXBF SEQ PARITY ERR	RDBDF SEQ PARITY ERR	(RSV)	(RSV)	XWB WPTR PARITY ERR	XWB SPTR PARITY ERR
6A		FDTM::PCICHK2B1						
	HWB WPTR PARITY ERR	HWB SPTR PARITY ERR	HRB WPTR PARITY ERR	HRB SPTR PARITY ERR	DLRC CMP ERR	DLRC PARITY ERR	(RSV)	WDLRC PARITY ERR
6B		FDTM::PCICHK2B1						
	HWB PARITY ERR 00	HWB PARITY ERR 01	HWB PARITY ERR 10	HWB PARITY ERR 11	HRB PARITY ERR 00	HRB PARITY ERR 01	HRB PARITY ERR 10	HRB PARITY ERR 11
6C		FDTM::PCICHK2B1						
	XWB0 PARITY ERR	XWB1 PARITY ERR	MRB0 PARITY ERR	MRB1 PARITY ERR	DWA XAD PARITY ERR	PCI XAD PARITY ERR	DBFW ADRCNT PARITY ERR	DBFR ADRCNT PARITY ERR
6D		FDTM::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E		FDTM::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F		FDTM::PCICHK2B2						
	(RSV)	(RSV)	(RSV)	PCI OVER RUN ERR	(RSV)	(RSV)	DWA CMP ERR	DRA CMP ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(9) Byte28 = 91 (4/4)

	0	1	2	3	4	5	6	7
70	FDTM::PCICHK2B2							
	(RSV)	(RSV)	(RSV)	XFC MODE ERR	ACC WIDTH ERR	STADR ACC ERR	DBF ACC ERR	XBF ACC ERR
71	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	FDTM::COMMCHK2CST0							
	(RSV)	(RSV)	80ns TIMER CNT PARITY ERR	60ns TIMER CNT PARITY ERR	(RSV)	ARB0 SEQ PARITY ERR	ARB1 SEQ PARITY ERR	ARB CMP ERR
73	FDTM::HCMD							
	CACHE Transfer Command (BYTE0)							
74	FDTM::HCMD							
	CACHE Transfer Command (BYTE1)							
75	FDTM::HCMD							
	CACHE Transfer Command (BYTE2)							
76	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE0)							
77	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE1)							
78	FDTM::HCMD2							
	CACHE Transfer Command 2 (BYTE2)							
79	FDTA::CBEN							
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
7A	FDTA::CBEN							
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
7B	FDTA::PKID							
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7C	FDTA::MONI							
	MPID#				LSI REV.			
7D	FDTA::MONI							
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 92 or 94 or 96 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'13'						
41		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Other	(RSV)	(RSV)	OTHER PCI Master ERR
42		XPA:: PnISTAT						
	(RSV)	(RSV)	(RSV)	(RSV)	FDTM CHK2A Own	PCI SERR IN	PCI CONFIG ERR	XPA ERR
43		XPA::PnISTAT						
	FDTM END DMA Other	FDTM END PMA Other	PCI DEV INT1 Other	PCI DEV INT0 Other	(RSV)	(RSV)	(RSV)	(RSV)
44		XPA::PnISTAT						
	FDTM END DMA Own	FDTM END PMA Own	PCI DEV INT1 Own	PCI DEV INT0 Own	PCI INT	MP INT	XPA XFR END	(RSV)
45		FDTM::PMACHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
46		FDTM::PMACHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
49		FDTM::PMACHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4A		FDTM::PMACHK2CST0						
	HSN CMD LOAD PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4B		FDTM::PMACHK2CST1						
	HSN RD ADR CNT PARTY ERR	HSN WT ADR CNT PARTY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4C		FDTM::PMACHK2CST1						
	PWB LRC PARTY ERR	PWB LRC PARTY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4D		FDTM::PMACHK2CST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PMA TIME OUT
4E		FDTM::PMACHK2CST2						
	TX FLRC ERR	TX FLRC PARITY ERR	RX FLRC PARITY ERR	RX FLRC PARITY ERR	PBF0 PARITY ERR	PBF1 PARITY ERR	PBF2 PARITY ERR	PBF3 PARITY ERR
4F		FDTM::PMACHK2CST2						
	(RSV)	(RSV)	(RSV)	(RSV)	PMA ACCMD ERR	XFC MODE ERR	RAID MODE ERR	BLK MODE ACSERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 92 or 94 or 96 (2/4)

	0	1	2	3	4	5	6	7
50		FDTM::PMACHK2CST2						
	RD DT END-CODE ERR0	RD DT END-CODE ERR1	RD DT END-CODE ERR2	RD DT END-CODE ERR3	TX FLRC 0 PADDING ERR	RX FLRC 0 PADDING ERR	RD DT INV-PLRC ERR0	RD DT INV-PLRC ERR1
51		FDTM::PMACHK2CST2						
	HSN PBF IN PARITY ERR	(RSV)	(RSV)	(RSV)	PMA TIMER PARITY ERR	(RSV)	PMA ARB SEQ PARITY ERR	PMA SEQ PARITY ERR
52		FDTM::H0CHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 DBF PARITY ERR
53		FDTM::H0CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB0 PARITY ERR
54		FDTM::H0CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 PWB1 PARITY ERR
55		FDTM::H0CHK2BST2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 SNB0 PARITY ERR	P0 SNB1 PARITY ERR
56		FDTM::H0CHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P0 TJ1 PARITY ERR	P0 TJ2 PARITY ERR
57		FDTM::H0CHK2CST0						
	P0 TX1 TIMER0 PARITY ERR	(RSV)	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	P0 TX1 CNT PARITY ERR	(RSV)	P0 TX1 SEQ PARITY ERR
58		FDTM::H0CHK2CST1						
	P0 TX2 TIMER0 PARITY ERR	P0 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P0 TX1 PTR PARITY ERR	(RSV)	(RSV)	P0 TX1 SEQ PARITY ERR
59		FDTM::H0CHK2CST2						
	(RSV)	(RSV)	P0 PRBPTR CMP ERR	P0 PRBPTR PARITY ERR	P0 PRBPTR 0 CMP ERR	P0 PRBPTR 1 CMP ERR	P0 PRBPTR 0 PARITY ERR	P0 PRBPTR 1 PARITY ERR
5A		FDTM::H0CHK2CST2						
	P0 RX TIMER0 PARITY ERR	P0 RX TIMER1 PARITY ERR	(RSV)	(RSV)	P0 RX PTR PARITY ERR	P0 RX CNT PARITY ERR	(RSV)	P0 RX SEQ PARITY ERR
5B		FDTM::H1CHK2BST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 DBF PARITY ERR
5C		FDTM::H1CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB0 PARITY ERR
5D		FDTM::H1CHK2BST1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 PWB1 PARITY ERR
5E		FDTM::H1CHK2BST2						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 SNB0 PARITY ERR	P1 SNB1 PARITY ERR
5F		FDTM::H1CHK2CST0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	P1 TJ1 PARITY ERR	P1 TJ2 PARITY ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 92 or 94 or 96 (3/4)

	0	1	2	3	4	5	6	7
60	FDTM::H1CHK2CST0							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
61	FDTM::H1CHK2CST1							
	P1 TX2 TIMER0 PARITY ERR	P1 TX2 TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX1 PTR PARITY ERR	(RSV)	(RSV)	P1 TX1 SEQ PARITY ERR
62	FDTM::H1CHK2CST2							
	(RSV)	(RSV)	P1 PRBPTR CMP ERR	P1 PRBPTR PARITY ERR	P1 PRBPTR 0 CMP ERR	P1 PRBPTR 1 CMP ERR	P1 PRBPTR 0 PARITY ERR	P1 PRBPTR 1 PARITY ERR
63	FDTM::H1CHK2CST2							
	P1 TX TIMER0 PARITY ERR	P1 TX TIMER1 PARITY ERR	(RSV)	(RSV)	P1 TX PTR PARITY ERR	P1 TX CNT PARITY ERR	(RSV)	P1 TX SEQ PARITY ERR
64	FDTM::HADR1UCNT							
	Slave 1 CACHE Transfer Address (BYTE0)							
65	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE1)							
66	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE2)							
67	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE3)							
68	FDTM::HADR1LCNT							
	Slave 1 CACHE Transfer Address (BYTE4)							
69	FDTM::HADR2UCNT							
	Slave 2 CACHE Transfer Address (BYTE0)							
6A	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE1)							
6B	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE2)							
6C	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE3)							
6D	FDTM::HADR2LCNT							
	Slave 2 CACHE Transfer Address (BYTE4)							
6E	FDTM::HCMD							
	CACHE Transfer Command (BYTE0)							
6F	FDTM::HCMD							
	CACHE Transfer Command (BYTE1)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(10) Byte28 = 92 or 94 or 96 (4/4)

	0	1	2	3	4	5	6	7
70		FDTM::HCMD						
		CACHE Transfer Command (BYTE2)						
71		FDTM::HCMD2						
		CACHE Transfer Command 2 (BYTE0)						
72		FDTM::HCMD2						
		CACHE Transfer Command 2 (BYTE1)						
73		FDTM::HCMD2						
		CACHE Transfer Command 2 (BYTE2)						
74		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77		FDTA::CBEN						
	C Path#00 ENABLE	C Path#01 ENABLE	C Path#02 ENABLE	C Path#03 ENABLE	C Path#04 ENABLE	C Path#05 ENABLE	C Path#06 ENABLE	C Path#07 ENABLE
78		FDTA::CBEN						
	C Path#10 ENABLE	C Path#11 ENABLE	C Path#12 ENABLE	C Path#13 ENABLE	C Path#14 ENABLE	C Path#15 ENABLE	C Path#16 ENABLE	C Path#17 ENABLE
79		FDTA::PKID						
	(RSV)	(RSV)	(RSV)	(RSV)	PKID#			
7A		FDTA::MONI						
	MPID#				LSI REV.			
7B		FDTA::MONI						
	(RSV)	(RSV)	(RSV)	(RSV)	LSI REV.-2			
7C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(11) Byte28 = 60 or 62 or 68 or 6a (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'01'						
41		NDTM::XFS						
	TRANSFER END	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	WCHK1 Detected	CHK2 Detected
42		NDTM::XFS						
	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK2E Detected	(RSV)	(RSV)	(RSV)
43		NDTM::XFS						
	REQID			(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		NDTM::CHK2BSTSP0						
	DMA-PCI ARBT ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
45		NDTM::CHK2BSTSP0						
	REQ PCIADR PARITY ERR 0	REQ PCIADR PARITY ERR 1	REQ PCIADR PARITY ERR 2	REQ PCIADR PARITY ERR 3	REQ PCIADR PARITY ERR 4	REQ PCIADR PARITY ERR 5	REQ PCIADR PARITY ERR 6	REQ PCIADR PARITY ERR 7
46		NDTM::CHK2BSTSP0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	REQ LEN PARITYERR
47		NDTM::CHK2BSTSD0						
	PCI-DBF WR DATA PARITY ERR	PCI-DBF RD DATA ECC ERR	PCI-DBF RD DATA ECC ERR(A)	(RSV)	PCI-PBF WR DATA PARITY ERR	PCI-PBF RD DATA ECC ERR	PCI-PBF RD DATA ECC ERR(A)	(RSV)
48		NDTM::CHK2BSTSD0						
	PCI-DBF WR ADR PARITY ERR	PCI-DBF RD ADR PARITY ERR	PCI-PBF WR ADR PARITY ERR	PCI-PBF RD ADR PARITY ERR	DLRC PARITY ERR	DLRC HBUF CMP ERR	DLRC HBUF IN PNT PARITY ERR	DLRC HBUF OUT PNT PARITY ERR
49		NDTM::CHK2BSTSD0						
	DCRC BYTE0 PARITY ERR	DCRC BYTE1 PARITY ERR	DCRC BYTE2 PARITY ERR	DCRC BYTE3 PARITY ERR	LWERR BYTE0 PARITY ERR	LWERR BYTE1 PARITY ERR	(RSV)	(RSV)
4A		NDTM::CHK2BSTSD0						
	PCI XFR CNT PARITY ERR	PCI REQ LEN PARITY ERR	PCI-DBF DATA LEN0 PARITY ERR	PCI-DBF DATA LEN1 PARITY ERR	PCI REQ TIMER0 PARITY ERR	PCI REQ TIMER1 PARITY ERR	PCI REQ TIMER TIMEOUT	EXBF REQ TIMER TIMEOUT
4B		NDTM::CHK2BSTSD1						
	HSN-DBF WR DATA PARITY ERR	HSN-DBF RD DATA ECC ERR	HSN-DBF RD DATA ECC ERR(A)	(RSV)	(RSV)	HSN-PBF RD DATA ECC ERR	HSN-PBF RD DATA ECC ERR(A)	(RSV)
4C		NDTM::CHK2BSTSD1						
	HSN-DBF WR ADR PARITY ERR	HSN-DBF RD ADR PARITY ERR	(RSV)	HSN-PBF RD ADR PARITY ERR	(RSV)	DLRC PBUF CMP ERR	DLRC PBUF IN PNT PARITY ERR	DLRC PBUF OUT PNT PARITY ERR
4D		NDTM::CHK2BSTSD1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4E		NDTM::CHK2BSTSD1						
	HSN XFR CNT PARITY ERR	HSN REQ LEN PARITY ERR	HSN-DBF DATA LEN0 PARITY ERR	HSN-DBF DATA LEN1 PARITY ERR	HSN REQ TIMER0 PARITY ERR	HSN REQ TIMER1 PARITY ERR	HSN REQ TIMER TIMEOUT	HSN-DBF END ERR
4F		NDTM::CHK2BSTSD2						
	HSN WR DATA 0 PARITY ERR	HSN WR DATA 1 PARITY ERR	HSN WR DATA 2 PARITY ERR	HSN WR DATA 3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(11) Byte28 = 60 or 62 or 68 or 6a (2/4)

	0	1	2	3	4	5	6	7
50	NDTM::CHK2BSTSD2							
	HSN MADR0 PARITY ERR	HSN MADR1 PARITY ERR	HSN MADR2 PARITY ERR	HSN MADR3 PARITY ERR	HSN MADR4 PARITY ERR	HSN MADR MASK ERR	(RSV)	(RSV)
51	NDTM::CHK2BSTSD2							
	HSN SADR0 PARITY ERR	HSN SADR1 PARITY ERR	HSN SADR2 PARITY ERR	HSN SADR3 PARITY ERR	HSN SADR4 PARITY ERR	HSN SADR MASK ERR	(RSV)	(RSV)
52	NDTM::CHK2BSTSD2							
	LA CNT0 PARITY ERR	LA CNT1 PARITY ERR	LA CNT2 PARITY ERR	LA CNT3 PARITY ERR	LA CNT4 PARITY ERR	LA CNT5 PARITY ERR	XFC REG PARITY ERR	PBFCTL REG PARITY ERR
53	NDTM::CHK2BSTSD3							
	DMA TARGET DATA RCV OVER RUN	DMA MASTER DATA RCV OVER RUN	DMA TARGET DATA SND OVER RUN	DMA MASTER DATA SND OVER RUN	DBF/PBF PCI TARGET ERR ACS	DBF RD ERR ACS	DBF WR ERR ACS	DMA TARGET DBF/PCI ADR ERR
54	NDTM::CHK2BSTSD3							
	DBF/PBF ADR0 PARITY ERR	DBF/PVF ADR1 PARITY ERR	DBF/PVF ADR2 PARITY ERR	DBF ADR CMP REG PARITY ERR	DBF BYTE ENABLE ERR	(RSV)	(RSV)	(RSV)
55	NDTM::CHK2BSTSD3							
	HSN MADR0 PARITY ERR	HSN MADR1 PARITY ERR	HSN MADR2 PARITY ERR	HSN MADR3 PARITY ERR	HSN MADR4 PARITY ERR	HSN MADR5 PARITY ERR	HSN MADR6 PARITY ERR	HSN MADR7 PARITY ERR
56	NDTM::CHK2BSTSD3							
	DBF-EXBF EXBFADR0 PARITY ERR	DBF-EXBF EXBFADR1 PARITY ERR	DBF-EXBF EXBFADR2 PARITY ERR	PBFCTL PARITY ERR	EXBFCTL PARITY ERR	(RSV)	(RSV)	(RSV)
57	NDTM::CHK2BSTSD4							
	DMA DOUBLE EXEC	XFC ILGAL CMD	DMA CHAIN CNT PARITY ERR	PCI CEND ERR	HSN CEND ERR	DBF DATA CTL ERR	(RSV)	(RSV)
58	NDTM::CHK2BSTSD4							
	PBFADR BYTE0 PARITY ERR	PBFADR BYTE1 PARITY ERR	PBFADR BYTE2 PARITY ERR	PBFADR BYTE3 PARITY ERR	PBFADR BYTE4 PARITY ERR	PBFADR BYTE5 PARITY ERR	PBFADR BYTE6 PARITY ERR	PBFADR BYTE7 PARITY ERR
59	NDTM::CHK2BSTSD4							
	XFC BYTE0 PARITY ERR	XFC BYTE1 PARITY ERR	XFC BYTE2 PARITY ERR	XFC BYTE3 PARITY ERR	IOREG WR CHK	(RSV)	(RSV)	(RSV)
5A	NDTM::CHK2BSTSH0							
	A/C PHASE CNT PARITY ERR	WR DATA CNT1 PARITY ERR	WR DATA CNT2 PARITY ERR	CSTAT0 CNT PARITY ERR	CSTA1 CNT PARITY ERR	(RSV)	RD DATA CNT PARITY ERR	RD DATA ADR PARITY ERR
5B	NDTM::CHK2BSTSH0							
	STATUS1 CNT1 PARITY ERR	STATUS1 CNT2 PARITY ERR	STATUS2 CNT1 PARITY ERR	STATUS2 CNT2 PARITY ERR	(RSV)	FT1,4 CNT PARITY ERR	FT2,5 CNT PARITY ERR	FT3,6 CNT PARITY
5C	NDTM::CHK2BSTSH0							
	FLRC CMP ERR	SLRC CMP ERR	LA CMP ERR	FW MODE ERR	FW CNT ERR	FW CNT PARITY ERR	CHSN PATH ERR	2SLV WR CMA# ERR
5D	NDTM::CHK2BSTSH0							
	CtoC COPY CMA# ERR	CinC COPY CMA# ERR	SLRC CHECKER PARITY ERR	SLRC GENERATER PARITY ERR	HSN ARBT ERR	HSN IT ERR	T00 CNT PARITY ERR	(RSV)
5E	NDTM::CHK2BSTSH1							
	HSN RD DATA PATH0 PARITY ERR	HSN RD DATA PATH1 PARITY ERR	HSN RD DATA PATH2 PARITY ERR	HSN RD DATA PATH3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
5F	NDTM::CHK2BSTSH1							
	HSN WR DATA PATH0 PARITY ERR	HSN WR DATA PATH1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(11) Byte28 = 60 or 62 or 68 or 6a (3/4)

	0	1	2	3	4	5	6	7
60	NDTM::CHK2BSTSH1							
	CSTAT2 PARITY ERR	CSTAT4 PARITY ERR	CSTAT3 PARITY ERR	CSTAT5 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
61	NDTM::CHK2BSTSH1							
	PLRC CHECKER0 PARITY ERR	PLRC CHECKER1 PARITY ERR	PRC GENERATER0 PARITY ERR	PRC GENERATER1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
62	NDTM::CHK2BSTSH2							
	CHSNCTL WR DATA0 PARITY ERR	CHSNCTL WR DATA1 PARITY ERR	CHSNCTL WR DATA2 PARITY ERR	(RSV)	(RSV)	CSTATCTL WR DATA1 PARITY ERR	(RSV)	CSTATCTL WR DATA3 PARITY ERR
63	NDTM::CHK2BSTSH2							
	CTIMER0 WR DATA0 PARITY ERR	CTIMER0 WR DATA1 PARITY ERR	CTIMER0 WR DATA2 PARITY ERR	CTIMER0 WR DATA3 PARITY ERR	CTIMER1 WR DATA0 PARITY ERR	CTIMER1 WR DATA1 PARITY ERR	CTIMER1 WR DATA2 PARITY ERR	CTIMER1 WR DATA3 PARITY ERR
64	NDTM::CHK2BSTSH2							
	CTIMER2 WR DATA0 PARITY ERR	CTIMER2 WR DATA1 PARITY ERR	CTIMER2 WR DATA2 PARITY ERR	CTIMER2 WR DATA3 PARITY ERR	CHSN PRIORITY0 PARITY ERR	(RSV)	(RSV)	(RSV)
65	NDTM::CHK2BSTSH2							
	CHSN EIJ WR DATA0 PARITY ERR	(RSV)	(RSV)	(RSV)	CHSN00CNT WR DATA0 PARITY ERR	(RSV)	(RSV)	(RSV)
66	NDTM::CHNCNT							
	(RSV)	(RSV)	(RSV)	XFR CHAIN#				
67	NDTM::PCIDATAL							
	XFR PCI-DBF DATA CNT (BYTE0)							
68	NDTM::PCIDATAL							
	XFR PCI-DBF DATA CNT (BYTE1)							
69	NDTM::HSNMADRU							
	XFR PCI-DBF HSN Master Address (BYTE0)							
6A	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE1)							
6B	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE2)							
6C	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE3)							
6D	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE4)							
6E	NDTM::HSNSADRU							
	XFR PCI-DBF HSN Slave Address (BYTE0)							
6F	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE1)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(11) Byte28 = 60 or 62 or 68 or 6a (4/4)

	0	1	2	3	4	5	6	7
70		NDTM::HSNSADRL						
		XFR PCI-DBF HSN Slave Address (BYTE2)						
71		NDTM::HSNSADRL						
		XFR PCI-DBF HSN Slave Address (BYTE3)						
72		NDTM::HSNSADRL						
		XFR PCI-DBF HSN Slave Address (BYTE4)						
73		NDTM::LA0						
		Logical Address (BYTE0)						
74		NDTM::LA0						
		Logical Address (BYTE1)						
75		NDTM::LA1						
		Logical Address (BYTE2)						
76		NDTM::LA1						
		Logical Address (BYTE3)						
77		NDTM::LA1						
		Logical Address (BYTE4)						
78		NDTM::LA1						
		Logical Address (BYTE5)						
79		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE0)						
7A		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE1)						
7B		NDTM::CHSNCTL						
	C Path #00 ENABLE	C Path #01 ENABLE	C Path #02 ENABLE	C Path #03 ENABLE	C Path #04 ENABLE	C Path #05 ENABLE	C Path #06 ENABLE	C Path #07 ENABLE
7C		NDTM::CHSNCTL						
	C Path #10 ENABLE	C Path #11 ENABLE	C Path #12 ENABLE	C Path #13 ENABLE	C Path #14 ENABLE	C Path #15 ENABLE	C Path #16 ENABLE	C Path #17 ENABLE
7D		NDTM::CHSNCTL						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PKID		
7E		NDTM::CHSNPHASE						
	ADR/CMD PHASE	WR DATA PHASE	RD DATA PHASE	STATUS1 PHASE	STATUS2 PHASE	(RSV)	(RSV)	(RSV)
7F		NDTM::CHSNPHASE						
	HSN P0 XFR	HSN P1 XFR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(12) Byte28 = 61 or 69 (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'02'						
41		NDTM::XFS						
	TRANSFER END	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	WCHK1 Detected	CHK2 Detected
42		NDTM::XFS						
	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK2E Detected	(RSV)	(RSV)	(RSV)
43		NDTM::XFS						
	REQID			(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		NDTM::CHK2CSTS0						
	P0 RD DATA0 PARITY ERR	P0 RD DATA1 PARITY ERR	P0 RD DATA2 PARITY ERR	P0 RD DATA3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
45		NDTM::CHK2CSTS0						
	(RSV)	(RSV)	P0 SYNC ERR	P0 RD END-CODE ERR	P0 STATUS1 END-CODE ERR	P0 STATUS2 END-CODE ERR	P0 RD PLRC ERR	P0 STSTUS1 PLRC ERR
46		NDTM::CHK2CSTS0						
	P0 STATUS2 PLRC ERR	P0 RD INV-PLRC ERR	P0 STATUS1 INV-PLRC ERR	P0 STATUS2 INV-PLRC ERR	P0 STATUS1 ST0,1 CMP ERR	P0 STATUS2 ST0,1 CMP ERR	P0 STATUS1 PKID ERR	P0 STATUS2 PKID ERR
47		NDTM::CHK2CSTS0						
	P0 ERRINT ERR	P0 ACK ERR	P0 ENTOUT ERR	P0 STENOUT ERR	(RSV)	P0 TIMER1 TIME OUT	P0 TIMER2 TIME OUT	P0 TIMER3 TIME OUT
48		NDTM::CHK2CSTS1						
	P1 RD DATA0 PARITY ERR	P1 RD DATA1 PARITY ERR	P1 RD DATA2 PARITY ERR	P1 RD DATA3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
49		NDTM::CHK2CSTS1						
	(RSV)	(RSV)	P1 SYNC ERR	P1 RD END-CODE ERR	P1 STATUS1 END-CODE ERR	P1 STATUS2 END-CODE ERR	P1 RD PLRC ERR	P1 STSTUS1 PLRC ERR
4A		NDTM::CHK2CSTS1						
	P1 STATUS2 PLRC ERR	P1 RD INV-PLRC ERR	P1 STATUS1 INV-PLRC ERR	P1 STATUS2 INV-PLRC ERR	P1 STATUS1 ST0,1 CMP ERR	P1 STATUS2 ST0,1 CMP ERR	P1 STATUS1 PKID ERR	P1 STATUS2 PKID ERR
4B		NDTM::CHK2CSTS1						
	P1 ERRINT ERR	P1 ACK ERR	P1 ENTOUT ERR	P1 STENOUT ERR	(RSV)	P1 TIMER1 TIME OUT	P1 TIMER2 TIME OUT	P1 TIMER3 TIME OUT
4C		NDTM::CHK2DSTS						
	P0 ERRINT Received	P1 ERRINT Received	(RSV)	(RSV)	(RSV)	(RSV)	HSN STATUS1 ERR ON	HSN STATUS2 ERR ON
4D		NDTM::CHSNSTSPCK						
	P0 STATUS1 B0 PARITY ERR	P0 STATUS1 B1 PARITY ERR	P0 STATUS1 B2 PARITY ERR	P0 STATUS1 B3 PARITY ERR	P0 STATUS1 B4 PARITY ERR	P0 STATUS1 B5 PARITY ERR	P0 STATUS1 B6 PARITY ERR	P0 STATUS1 B7 PARITY ERR
4E		NDTM::CHSNSTSPCK						
	P0 STATUS2 B0 PARITY ERR	P0 STATUS2 B1 PARITY ERR	P0 STATUS2 B2 PARITY ERR	P0 STATUS2 B3 PARITY ERR	P0 STATUS2 B4 PARITY ERR	P0 STATUS2 B5 PARITY ERR	P0 STATUS2 B6 PARITY ERR	P0 STATUS2 B7 PARITY ERR
4F		NDTM::CHSNSTSPCK						
	P1 STATUS1 B0 PARITY ERR	P1 STATUS1 B1 PARITY ERR	P1 STATUS1 B2 PARITY ERR	P1 STATUS1 B3 PARITY ERR	P1 STATUS1 B4 PARITY ERR	P1 STATUS1 B5 PARITY ERR	P1 STATUS1 B6 PARITY ERR	P1 STATUS1 B7 PARITY ERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(12) Byte28 = 61 or 69 (2/4)

	0	1	2	3	4	5	6	7
50	NDTM::CHSNSTSPCK							
	P1 STATUS2 B0 PARITY ERR	P1 STATUS2 B1 PARITY ERR	P1 STATUS2 B2 PARITY ERR	P1 STATUS2 B3 PARITY ERR	P1 STATUS2 B4 PARITY ERR	P1 STATUS2 B5 PARITY ERR	P1 STATUS2 B6 PARITY ERR	P1 STATUS2 B7 PARITY ERR
51	NDTM::CHNCNT							
	(RSV)	(RSV)	(RSV)	XFR CHAIN#				
52	NDTM::PCIDATAL							
	XFR PCI-DBF HSN Slave Address (BYTE0)							
53	NDTM::PCIDATAL							
	XFR PCI-DBF HSN Slave Address (BYTE1)							
54	NDTM::HSNMADRU							
	XFR PCI-DBF HSN Master Address (BYTE0)							
55	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE1)							
56	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE2)							
57	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE3)							
58	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE4)							
59	NDTM::HSNSADRU							
	XFR PCI-DBF HSN Slave Address (BYTE0)							
5A	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE1)							
5B	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE2)							
5C	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE3)							
5D	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE4)							
5E	NDTM::LA0							
	Logical Address (BYTE0)							
5F	NDTM::LA0							
	Logical Address (BYTE1)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(12) Byte28 = 61 or 69 (3/4)

	0	1	2	3	4	5	6	7
60		NDTM::LA1						
		Logical Address (BYTE2)						
61		NDTM::LA1						
		Logical Address (BYTE3)						
62		NDTM::LA1						
		Logical Address (BYTE4)						
63		NDTM::LA1						
		Logical Address (BYTE5)						
64		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE0)						
65		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE1)						
66		NDTM::CHSNCTL						
	C Path #00 ENABLE	C Path #01 ENABLE	C Path #02 ENABLE	C Path #03 ENABLE	C Path #04 ENABLE	C Path #05 ENABLE	C Path #06 ENABLE	C Path #07 ENABLE
67		NDTM::CHSNCTL						
	C Path #10 ENABLE	C Path #11 ENABLE	C Path #12 ENABLE	C Path #13 ENABLE	C Path #14 ENABLE	C Path #15 ENABLE	C Path #16 ENABLE	C Path #17 ENABLE
68		NDTM::CHSNCTL						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PKID		
69		NDTM::CHSNPHASE						
	ADR/CMD PHASE	WR DATA PHASE	RD DATA PHASE	STATUS1 PHASE	STATUS2 PHASE	(RSV)	(RSV)	(RSV)
6A		NDTM::CHSNPHASE						
	HSN P0 XFR	HSN P1 XFR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6B		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(12) Byte28 = 61 or 69 (4/4)

	0	1	2	3	4	5	6	7
70	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
72	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
73	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
77	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
78	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
79	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7A	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7B	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(13) Byte28 = 63 or 6b (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO. x'03'						
41		NDTM::XFS						
	TRANSFER END	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	WCHK1 Detected	CHK2 Detected
42		NDTM::XFS						
	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK2E Detected	(RSV)	(RSV)	(RSV)
43		NDTM::XFS						
	REQID			(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		NDTM::CHK2BSTSD1						
	HSN-DBF WR DATA PARITY ERR	HSN-DBF RD DATA ECC ERR	HSN-DBF RD DATA ECC ERR(A)	(RSV)	(RSV)	HSN-PBF RD DATA ECC ERR	HSN-PBF RD DATA ECC ERR(A)	(RSV)
45		NDTM::CHK2BSTSD1						
	HSN-DBF WR ADR PARITY ERR	HSN-DBF RD ADR PARITY ERR	(RSV)	HSN-PBF RD ADR PARITY ERR	(RSV)	DLRC PBUF CMP ERR	DLRC PBUF IN PNT PARITY ERR	DLRC PBUF OUT PNT PARITY ERR
46		NDTM::CHK2BSTSD1						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47		NDTM::CHK2BSTSD1						
	HSN XFR CNT PARITY ERR	HSN REQ LEN PARITY ERR	HSN-DBF DATA LEN0 PARITY ERR	HSN-DBF DATA LEN1 PARITY ERR	HSN REQ TIMER0 PARITY ERR	HSN REQ TIMER1 PARITY ERR	HSN REQ TIMER TIMEOUT	HSN-DBF END ERR
48		NDTM::CHK2BSTSD2						
	HSN WR DATA 0 PARITY ERR	HSN WR DATA 1 PARITY ERR	HSN WR DATA 2 PARITY ERR	HSN WR DATA 3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
49		NDTM::CHK2BSTSD2						
	HSN MADR0 PARITY ERR	HSN MADR1 PARITY ERR	HSN MADR2 PARITY ERR	HSN MADR3 PARITY ERR	HSN MADR4 PARITY ERR	HSN MADR MASK ERR	(RSV)	(RSV)
4A		NDTM::CHK2BSTSD2						
	HSN SADR0 PARITY ERR	HSN SADR1 PARITY ERR	HSN SADR2 PARITY ERR	HSN SADR3 PARITY ERR	HSN SADR4 PARITY ERR	HSN SADR MASK ERR	(RSV)	(RSV)
4B		NDTM::CHK2BSTSD2						
	LA CNT0 PARITY ERR	LA CNT1 PARITY ERR	LA CNT2 PARITY ERR	LA CNT3 PARITY ERR	LA CNT4 PARITY ERR	LA CNT5 PARITY ERR	XFC REG PARITY ERR	PBFCTL REG PARITY ERR
4C		NDTM::CHK2BSTSH0						
	A/C PHASE CNT PARITY ERR	WR DATA CNT1 PARITY ERR	WR DATA CNT2 PARITY ERR	CSTAT0 CNT PARITY ERR	CSTA1 CNT PARITY ERR	(RSV)	RD DATA CNT PARITY ERR	RD DATA ADR PARITY ERR
4D		NDTM::CHK2BSTSH0						
	STATUS1 CNT1 PARITY ERR	STATUS1 CNT2 PARITY ERR	STATUS2 CNT1 PARITY ERR	STATUS2 CNT2 PARITY ERR	(RSV)	FT1,4 CNT PARITY ERR	FT2,5 CNT PARITY ERR	FT3,6 CNT PARITY
4E		NDTM::CHK2BSTSH0						
	FLRC CMP ERR	SLRC CMP ERR	LA CMP ERR	FW MODE ERR	FW CNT ERR	FW CNT PARITY ERR	CHSN PATH ERR	2SLV WR CMA# ERR
4F		NDTM::CHK2BSTSH0						
	CtoC COPY CMA# ERR	CinC COPY CMA# ERR	SLRC CHECKER PARITY ERR	SLRC GENERATER PARITY ERR	HSN ARBT ERR	HSN IT ERR	TO0 CNT PARITY ERR	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(13) Byte28 = 63 or 6b (2/4)

	0	1	2	3	4	5	6	7
50	NDTM::CHK2BSTSH1							
	HSN RD DATA PATH0 PARITY ERR	HSN RD DATA PATH1 PARITY ERR	HSN RD DATA PATH2 PARITY ERR	HSN RD DATA PATH3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
51	NDTM::CHK2BSTSH1							
	HSN WR DATA PATH0 PARITY ERR	HSN WR DATA PATH1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
52	NDTM::CHK2BSTSH1							
	CSTAT2 PARITY ERR	CSTAT4 PARITY ERR	CSTAT3 PARITY ERR	CSTAT5 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
53	NDTM::CHK2BSTSH1							
	PLRC CHECKER0 PARITY ERR	PLRC CHECKER1 PARITY ERR	PRC GENERATER0 PARITY ERR	PRC GENERATER1 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
54	NDTM::CHK2BSTSH2							
	CHSNCTL WR DATA0 PARITY ERR	CHSNCTL WR DATA1 PARITY ERR	CHSNCTL WR DATA2 PARITY ERR	(RSV)	(RSV)	CSTATCTL WR DATA1 PARITY ERR	(RSV)	CSTATCTL WR DATA3 PARITY ERR
55	NDTM::CHK2BSTSH2							
	CTIMER0 WR DATA0 PARITY ERR	CTIMER0 WR DATA1 PARITY ERR	CTIMER0 WR DATA2 PARITY ERR	CTIMER0 WR DATA3 PARITY ERR	CTIMER1 WR DATA0 PARITY ERR	CTIMER1 WR DATA1 PARITY ERR	CTIMER1 WR DATA2 PARITY ERR	CTIMER1 WR DATA3 PARITY ERR
56	NDTM::CHK2BSTSH2							
	CTIMER2 WR DATA0 PARITY ERR	CTIMER2 WR DATA1 PARITY ERR	CTIMER2 WR DATA2 PARITY ERR	CTIMER2 WR DATA3 PARITY ERR	CHSN PRIORITY0 PARITY ERR	(RSV)	(RSV)	(RSV)
57	NDTM::CHK2BSTSH2							
	CHSN EIJ WR DATA0 PARITY ERR	(RSV)	(RSV)	(RSV)	CHSN00CNT WR DATA0 PARITY ERR	(RSV)	(RSV)	(RSV)
58	NDTM::CHK2CSTS0							
	P0 RD DATA0 PARITY ERR	P0 RD DATA1 PARITY ERR	P0 RD DATA2 PARITY ERR	P0 RD DATA3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
59	NDTM::CHK2CSTS0							
	(RSV)	(RSV)	P0 SYNC ERR	P0 RD END-CODE ERR	P0 STATUS1 END-CODE ERR	P0 STATUS2 END-CODE ERR	P0 RD PLRC ERR	P0 STSTUS1 PLRC ERR
5A	NDTM::CHK2CSTS0							
	P0 STATUS2 PLRC ERR	P0 RD INV-PLRC ERR	P0 STATUS1 INV-PLRC ERR	P0 STATUS2 INV-PLRC ERR	P0 STATUS1 ST0,1 CMP ERR	P0 STATUS2 ST0,1 CMP ERR	P0 STATUS1 PKID ERR	P0 STATUS2 PKID ERR
5B	NDTM::CHK2CSTS0							
	P0 ERRINT ERR	P0 ACK ERR	P0 ENTOUT ERR	P0 STENOUT ERR	(RSV)	P0 TIMER1 TIME OUT	P0 TIMER2 TIME OUT	P0 TIMER3 TIME OUT
5C	NDTM::CHK2CSTS1							
	P1 RD DATA0 PARITY ERR	P1 RD DATA1 PARITY ERR	P1 RD DATA2 PARITY ERR	P1 RD DATA3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
5D	NDTM::CHK2CSTS1							
	(RSV)	(RSV)	P1 SYNC ERR	P1 RD END-CODE ERR	P1 STATUS1 END-CODE ERR	P1 STATUS2 END-CODE ERR	P1 RD PLRC ERR	P1 STSTUS1 PLRC ERR
5E	NDTM::CHK2CSTS1							
	P1 STATUS2 PLRC ERR	P1 RD INV-PLRC ERR	P1 STATUS1 INV-PLRC ERR	P1 STATUS2 INV-PLRC ERR	P1 STATUS1 ST0,1 CMP ERR	P1 STATUS2 ST0,1 CMP ERR	P1 STATUS1 PKID ERR	P1 STATUS2 PKID ERR
5F	NDTM::CHK2CSTS1							
	P1 ERRINT ERR	P1 ACK ERR	P1 ENTOUT ERR	P1 STENOUT ERR	(RSV)	P1 TIMER1 TIME OUT	P1 TIMER2 TIME OUT	P1 TIMER3 TIME OUT

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(13) Byte28 = 63 or 6b (3/4)

	0	1	2	3	4	5	6	7
60	NDTM::CHK2DSTS							
	P0 ERRINT Received	P1 ERRINT Received	(RSV)	(RSV)	(RSV)	(RSV)	HSN STATUS1 ERR ON	HSN STATUS2 ERR ON
61	NDTM::CHSNSTSPCK							
	P0 STATUS1 B0 PARITY ERR	P0 STATUS1 B1 PARITY ERR	P0 STATUS1 B2 PARITY ERR	P0 STATUS1 B3 PARITY ERR	P0 STATUS1 B4 PARITY ERR	P0 STATUS1 B5 PARITY ERR	P0 STATUS1 B6 PARITY ERR	P0 STATUS1 B7 PARITY ERR
62	NDTM::CHSNSTSPCK							
	P0 STATUS2 B0 PARITY ERR	P0 STATUS2 B1 PARITY ERR	P0 STATUS2 B2 PARITY ERR	P0 STATUS2 B3 PARITY ERR	P0 STATUS2 B4 PARITY ERR	P0 STATUS2 B5 PARITY ERR	P0 STATUS2 B6 PARITY ERR	P0 STATUS2 B7 PARITY ERR
63	NDTM::CHSNSTSPCK							
	P1 STATUS1 B0 PARITY ERR	P1 STATUS1 B1 PARITY ERR	P1 STATUS1 B2 PARITY ERR	P1 STATUS1 B3 PARITY ERR	P1 STATUS1 B4 PARITY ERR	P1 STATUS1 B5 PARITY ERR	P1 STATUS1 B6 PARITY ERR	P1 STATUS1 B7 PARITY ERR
64	NDTM::CHSNSTSPCK							
	P1 STATUS2 B0 PARITY ERR	P1 STATUS2 B1 PARITY ERR	P1 STATUS2 B2 PARITY ERR	P1 STATUS2 B3 PARITY ERR	P1 STATUS2 B4 PARITY ERR	P1 STATUS2 B5 PARITY ERR	P1 STATUS2 B6 PARITY ERR	P1 STATUS2 B7 PARITY ERR
65	NDTM::CHNCNT							
	(RSV)	(RSV)	(RSV)	XFR CHAIN#				
66	NDTM::PCIDATAL							
	XFR PCI-DBF DATA CNT (BYTE0)							
67	NDTM::PCIDATAL							
	XFR PCI-DBF DATA CNT (BYTE1)							
68	NDTM::HSNMADRU							
	XFR PCI-DBF HSN Master Address (BYTE0)							
69	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE1)							
6A	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE2)							
6B	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE3)							
6C	NDTM::HSNMADRL							
	XFR PCI-DBF HSN Master Address (BYTE4)							
6D	NDTM::HSNSADRU							
	XFR PCI-DBF HSN Slave Address (BYTE0)							
6E	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE1)							
6F	NDTM::HSNSADRL							
	XFR PCI-DBF HSN Slave Address (BYTE2)							

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(13) Byte28 = 63 or 6b (4/4)

	0	1	2	3	4	5	6	7
70		NDTM::HSNSADRL						
		XFR PCI-DBF HSN Slave Address (BYTE3)						
71		NDTM::HSNSADRL						
		XFR PCI-DBF HSN Slave Address (BYTE4)						
72		NDTM::LA0						
		Logical Address (BYTE0)						
73		NDTM::LA0						
		Logical Address (BYTE1)						
74		NDTM::LA1						
		Logical Address (BYTE2)						
75		NDTM::LA1						
		Logical Address (BYTE3)						
76		NDTM::LA1						
		Logical Address (BYTE4)						
77		NDTM::LA1						
		Logical Address (BYTE5)						
78		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE0)						
79		NDTM::HSNDATAL						
		XFR HSN DATA CNT (BYTE1)						
7A		NDTM::CHSNCTL						
	C Path #00 ENABLE	C Path #01 ENABLE	C Path #02 ENABLE	C Path #03 ENABLE	C Path #04 ENABLE	C Path #05 ENABLE	C Path #06 ENABLE	C Path #07 ENABLE
7B		NDTM::CHSNCTL						
	C Path #10 ENABLE	C Path #11 ENABLE	C Path #12 ENABLE	C Path #13 ENABLE	C Path #14 ENABLE	C Path #15 ENABLE	C Path #16 ENABLE	C Path #17 ENABLE
7C		NDTM::CHSNCTL						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	PKID		
7D		NDTM::CHSNPHASE						
	ADR/CMD PHASE	WR DATA PHASE	RD DATA PHASE	STATUS1 PHASE	STATUS2 PHASE	(RSV)	(RSV)	(RSV)
7E		NDTM::CHSNPHASE						
	HSN P0 XFR	HSN P1 XFR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(14) Byte28 = 64 ~ 67 or 6c ~ 6f (1/4)

	0	1	2	3	4	5	6	7
40		FORMAT NO.						
		x'04'						
41		NDTM::XFS						
	TRANSFER END	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	WCHK1 Detected	CHK2 Detected
42		NDTM::XFS						
	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK2E Detected	(RSV)	(RSV)	(RSV)
43		NDTM::XFS						
	REQID			(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
44		NDTM::CHK2ASTS0						
	PCI ADR PARITY ERR	PCI DATA PARITY ERR	PCI PERR Detected	PCI MASTER ABORT	PCI TARGET ABORT	(RSV)	(RSV)	(RSV)
45		NDTM::CHK2ASTS1						
	MBF0 RD DATA0 PARITY ERR	MBF0 RD DATA1 PARITY ERR	MBF0 RD DATA2 PARITY ERR	MBF0 RD DATA3 PARITY ERR	MBF1 RD DATA0 PARITY ERR	MBF1 RD DATA1 PARITY ERR	MBF1 RD DATA2 PARITY ERR	MBF1 RD DATA3 PARITY ERR
46		NDTM::CHK2ASTS1						
	MBF RD DATA PARITY ERR	(RSV)	MBF OVERFLOW ERR	MBF CALCULATE ERR	(RSV)	(RSV)	MBF WT ADR PARITY ERR	MBF RD ADR PARITY ERR
47		NDTM::CHK2ASTS1						
	(RSV)	(RSV)	(RSV)	MBSE0 BYTE0 PARITY ERR	MBSE0 BYTE1 PARITY ERR	MBSE0 BYTE2 PARITY ERR	MBSE0 BYTE3 PARITY ERR	MBSE0 BYTE4 PARITY ERR
48		NDTM::CHK2ASTS1						
	IOBASE0 BYTE0 PARITY ERR	IOBASE0 BYTE1 PARITY ERR	IOBASE0 BYTE2 PARITY ERR	MBSE0 BYTE0 PARITY ERR	MBSE0 BYTE1 PARITY ERR	MBSE0 BYTE2 PARITY ERR	MBSE0 BYTE3 PARITY ERR	MBSE0 BYTE4 PARITY ERR
49		NDTM::CHK2ASTS2						
	NDTM->PCI DATA BYTE0 PARITY ERR	NDTM->PCI DATA BYTE1 PARITY ERR	NDTM->PCI DATA BYTE2 PARITY ERR	NDTM->PCI DATA BYTE3 PARITY ERR	NDTM->PCI DATA BYTE4 PARITY ERR	NDTM->PCI DATA BYTE5 PARITY ERR	NDTM->PCI DATA BYTE6 PARITY ERR	NDTM->PCI DATA BYTE7 PARITY ERR
4A		NDTM::CHK2ASTS2						
	(RSV)	(RSV)	MBF SEL PARITY ERR	TBF SEL PARITY ERR	(RSV)	(RSV)	(RSV)	PCI SEQ ERR
4B		NDTM::CHK2ASTS2						
	LAY TIMER PARITY ERR	CACHE SIZE PARITY ERR	LAST CNT PARITY ERR	TIMEOUT CNT PARITY ERR	MABT CNT PARITY ERR	DMA CNT PARITY ERR	EXBF CNT PARITY ERR	IOCNT PARITY ERR
4C		NDTM::CHK2ASTS2						
	NADRCAL0 PARITY ERR	NADRCAL1 PARITY ERR	NADRCAL2 PARITY ERR	NADRCAL3 PARITY ERR	NADRCAL4 PARITY ERR	NADRCAL5 PARITY ERR	NADRCAL6 PARITY ERR	NADRCAL7 PARITY ERR
4D		NDTM::PCILOG0						
		PCI Address (BYTE0)						
4E		NDTM::PCILOG0						
		PCI Address (BYTE1)						
4F		NDTM::PCILOG0						
		PCI Address (BYTE2)						

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(14) Byte28 = 64 ~ 67 or 6c ~ 6f (2/4)

	0	1	2	3	4	5	6	7
50		NDTM::PCILOG0						
		PCI Address (BYTE3)						
51		NDTM::PCILOG1						
		PCI Address (BYTE4)						
52		NDTM::PCILOG1						
		PCI Address (BYTE5)						
53		NDTM::PCILOG1						
		PCI Address (BYTE6)						
54		NDTM::PCILOG1						
		PCI Address (BYTE7)						
55		NDTM::PCILOG2						
	LOG HOLD	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56		NDTM::PCILOG2						
	DMA#0 LOGGING	DMA#1 LOGGING	DMA#2 LOGGING	DMA#3 LOGGING	DMA#4 LOGGING	DMA#5 LOGGING	(RSV)	(RSV)
57		NDTM::PCILOG2						
	(RSV)	LOG STS 1: Master 0: Target	LOG STS 1: 64bit 0: 32bit	LOG STS 1: DAC 0: SCA	(RSV)	(RSV)	(RSV)	(RSV)
58		NDTM::PCILOG2						
	PCI Command				(RSV)	(RSV)	(RSV)	(RSV)
59		NDTM_PCICFG01						
	DET PARITY ERR	SIG SYS ERR	MST ABORT	TAG ABORT	(RSV)	DEV SEL0	DEV SEL1	DPTY ERR DET
5A		NDTM_PCICFG01						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	SERR EN
5B		NDTM_PCICFG01						
	(RSV)	PTY ERR RESP	(RSV)	(RSV)	(RSV)	BUS MST	MEM SPACE	IO SPACE
5C		NDTM::CHK2BSTSD0						
	PCI-DBF WR DATA PARITY ERR	PCI-DBF RD DATA ECC ERR	PCI-DBF RD DATA ECC ERR(A)	(RSV)	PCI-PBF WR DATA PARITY ERR	PCI-PBF RD DATA ECC ERR	PCI-PBF RD DATA ECC ERR(A)	(RSV)
5D		NDTM::CHK2BSTSP0						
	DMA-PCI ARBT ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5E		NDTM::CHK2BSTSP0						
	REQ PCIADR PARITY ERR 0	REQ PCIADR PARITY ERR 1	REQ PCIADR PARITY ERR 2	REQ PCIADR PARITY ERR 3	REQ PCIADR PARITY ERR 4	REQ PCIADR PARITY ERR 5	REQ PCIADR PARITY ERR 6	REQ PCIADR PARITY ERR 7
5F		NDTM::CHK2BSTSP0						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	REQ LEN PARITYERR

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(14) Byte28 = 64 ~ 67 or 6c ~ 6f (3/4)

	0	1	2	3	4	5	6	7
60	XPA::PnXERR0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61	XPA::PnXERR0							
	(RSV)	(RSV)	PCI Master ADR CNT PARITY ERR	PCI Master ADR PARITY ERR	PCI Master SEQ ERR	PCI Master RD PARITY ERR	PCI Master PERR IN	PCI Master PERR OUT
62	XPA::PnXERR0							
	(RSV)	PCI Target 100 ADR PARITY ERR	PCI Target 66 ADR PARITY ERR	PCI Target SEQ ERR	(RSV)	PCI Target READ PARITY ERR	PCI Target PERR IN	PCI Target PERR OUT
63	XPA::PnXERR0							
	XR TRG SEQ ERR	(RSV)	(RSV)	XR Master ADR PARITY ERR	XR Target ADR CNT PARITY ERR	XR DMA RD PARITY ERR	XR TOV	XR RD PARITY ERR
64	XPA::PnDIG0							
	Diag Reg 0							
65	XPA::PnDIG0							
	Diag Reg 0							
66	XPA::PnDIG0							
	Diag Reg 0							
67	XPA::PnDIG0							
	Diag Reg 0							
68	XPA::PnDIG1							
	Diag Reg 1							
69	XPA::PnDIG1							
	Diag Reg 1							
6A	XPA::PnDIG1							
	Diag Reg 1							
6B	XPA::PnDIG1							
	Diag Reg 1							
6C	XPA::PnSC							
	DETECTED PARITY ERR	SIGNALED SYSTEM ERR	RECEIVED MASTER ABORT	RECEIVED TARGET ABORT	(RSV)	DEVSEL TIMING 01: Medium		DATA PARITY REPORT
6D	XPA::PnSC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6E	XPA::PnSC							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6F	XPA::PnSC							
	(RSV)	ENABLE PARITY RSP	(RSV)	(RSV)	(RSV)	ENABLE BUS MASTERING	ENABLE MEMORY SPACE	ENABLE I/O SPACE

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Byte27 = 89 (CHA CHK2) Byte40-7F Detail
(14) Byte28 = 64 ~ 67 or 6c ~ 6f (4/4)

	0	1	2	3	4	5	6	7
70		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XR Target RD 3 PARITY ERR	XR Target RD 2 PARITY ERR	XR Target RD 1 PARITY ERR	XR Target RD 0 PARITY ERR
71		XPA::PnXERR1						
	(RSV)	(RSV)	(RSV)	(RSV)	XP WR LRC ERR	XP RD LRC ERR	PX WR LRC ERR	PCI DATA IN PARITY ERR
72		XPA::PnXERR1						
	XR Master ADR 3 PARITY ERR	XR Master ADR 2 PARITY ERR	XR Master ADR 1 PARITY ERR	XR Master ADR 0 PARITY ERR	XP DMA LRC ERR	XP RD LRC ERR	PX WR LRC ERR	PCI DATA IN PARITY ERR
73		XPA::PnXERR1						
	XR Target ADR 3 PARITY ERR	XR Target ADR 2 PARITY ERR	XR Target ADR 1 PARITY ERR	XR Target ADR 0 PARITY ERR	XR Target WR DATA 3 PARITY ERR	XR Target WR DATA 2 PARITY ERR	XR Target WR DATA 1 PARITY ERR	XR Target WR DATA 0 PARITY ERR
74		XPA::PnDIG2						
		Diag Reg 2						
75		XPA::PnDIG2						
		Diag Reg 2						
76		XPA::PnDIG2						
		Diag Reg 2						
77		XPA::PnDIG2						
		Diag Reg 2						
78		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
79		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7A		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7B		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8A (FCA CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTRL no.	DKU Physical Device no.				
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘A’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

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Byte27 = 8A (FCA CHK2) Byte28-31 Detail

	0	1	2	3	4	5	6	7
28	SubCode (Note 1)							
29	MMC::RCVINT							
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
2A	MMC::RCVINT							
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
2B	FCA::INTSTS							
	CHK2E ERR Interrupt	CHK2F ERR Interrupt	CHK2G ERR Interrupt	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
2C	FCA::MODE							
	DRV→ CACHE XFR Start	CACHE→ DRV XFR Start	FSB→ CACHE XFR Start	CACHE→ FDB XFR Start	DRV→FSB XFR Start	FDB→DRV XFR Start	(RSV)	(RSV)
2D	FCA::MODE							
	Data/Parity (1: Data)	LA EX MODE	LA CHK MASK	LBA/LLRC CHK MASK	(RSV)	Subblock Length in Packet (MAX: 4)		
2E	FCA::MODE							
	DMA QUE Number for the PDEV							
2F	FCA::DMASTS							
	DMA END	(RSV)	INT5	INT4	INT3	INT2	INT1	INT0
30	FCA::DMASTS							
	CHK2E Occurred	CHK2F Occurred	CHK2G Occurred	(RSV)	CHK2RST	ABORT	PADDING	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(Note 1) Meaning of SubCode:

x‘10’ = QDTA reported CHK2 when writing to cache,
x‘20’ = FCA CHK2 when writing to cache,
x‘30’ = FCA-QDTA CHK2 when writing to cache,
x‘40’ = PCI CHK2 when writing to cache,
x‘60’ = PCI-FCA CHK2 when writing to cache,
x‘48’ = HDD CHK2 when writing to cache,
x‘F0’ = XFR TOV when writing to cache,
x‘11’ = QDTA reported CHK2 when reading from cache,
x‘21’ = FCA CHK2 when reading from cache,
x‘31’ = FCA-QDTA CHK2 when reading from cache,
x‘41’ = PCI CHK2 when reading from cache,
x‘61’ = PCI-FCA CHK2 when reading from cache,
x‘19’ = CACHE CHK2 when reading from cache,
x‘F1’ = XFR TOV when reading from cache

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (1/4)

	0	1	2	3	4	5	6	7
40	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE0)							
41	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE1)							
42	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE2)							
43	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE3)							
44	DRR::CD0SL1C0 Slave 1 Cache Transfer Address (BYTE4)							
45	DRR::CD0SL1C0 Slave 1 Cache Transfer Command (BYTE0)							
46	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE1)							
47	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE2)							
48	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE0)							
49	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE1)							
4A	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE2)							
4B	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE3)							
4C	DRR::CD0SL2C0 Slave 2 Cache Transfer Address (BYTE4)							
4D	DRR::CD0SL2C0 Slave 2 Cache Transfer Command (BYTE0)							
4E	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE1)							
4F	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE2)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::D0M0DE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
51		DRR::D0M0DE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
52		DRR::D0TXM						
		D0 TX SEQ(Master)						
53		DRR::D0MODE1						
	DTN CUDG MODE	DTN SYSTEM CLK MASK	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		DRR::D0MODE1						
	DTN ABORT	DTN CHSN ABORT	(RSV)	(RSV)	(RSV)	(RSV)	DTN OUT DIAG	DTN CHK2 RST
55		DRR::D0ERR						
	DTN CTL ERR	P0 CTL ERR	P1 CTL ERR	DTN DT ERR	P0 DT ERR	P1 DT ERR	P0 DT CARB/CMA ERR	P0 ST1 CARB/CMA ERR
56		DRR::D0ERR						
	P0 ERR INT	P1 ERR INT	(RSV)	TIME OVER ERR	ST0 VALID	ST1 VALID	P0 USE FLAG	P1 USE FLAG
57		DRR::D0ESTA0						
	TX DT PARITY ERR	TX PD-PNT PARITY ERR	DTN SEQ ERR	DTN WT-PNT PARITY ERR	WT DT-CNT PARITY ERR	INPUT CTL-SIG PARITY ERR	INPUT-PNT PARITY ERR	RD DT CNT PARITY ERR
58		DRR::D0ESTA0						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK ERR	P0 SYNC1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD-PNT PARITY ERR	P0 RX SEQ ERR	P0 TX WT-PNT PARITY ERR
59		DRR::D0ESTA1						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK ERR	P1 SYNC1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD-PNT PARITY ERR	P1 RX SEQ ERR	P1 TX WT-PNT PARITY ERR
5A		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		DRR::D0ESTA2						
	ST0 PLRC ERR	ST0 INV-PLRC ERR	ST0 END-CODE ERR	ST1 PLRC ERR	ST1 INV-PLRC ERR	ST1 END-CODE ERR	TRANS MODE ERR	(RSV)
5C		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
5D		DRR::D0ESTA3						
	OUT DT11 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
5E		DRR::D0ESTA3						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	TX DT4 PARITY ERR	TX DT5 PARITY ERR	TX DT6 PARITY ERR	TX DT7 PARITY ERR
5F		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR
61		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
62		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
63		DRR::D0ESTA6						
	P0 TXX INPUT DT0 PARITY ERR	P0 TXX INPUT DT1 PARITY ERR	P0 TXX OUTPUT DT0 PARITY ERR	P0 TXX OUTPUT DT1 PARITY ERR	P1 TXX INPUT DT0 PARITY ERR	P1 TXX INPUT DT1 PARITY ERR	P1 TXX OUTPUT DT0 PARITY ERR	P1 TXX OUTPUT DT1PARITY ERR
64		DRR::D0ESTA6						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
65		DRR::D0ESTA7						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
66		DRR::D0ESTA7						
	INPUT DT0 PARITY ERR	INPUT DT1 PARITY ERR	INPUT DT2 PARITY ERR	INPUT DT3 PARITY ERR	P0 ERR INT	P1 ERR INT	DT CARB/CMA ERR	ST1 CARB/CMA ERR
67		DRR::D0ESTA8						
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	(RSV)	(RSV)	(RSV)	(RSV)
68		DRR::D0ESTA8						
	ST0 VALID	ST1 VALID	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)
69		DRR::D0ESTA9						
	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA9						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	(RSV)	(RSV)	(RSV)	(RSV)
6B		DRR::D0ESTAB						
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 ST0 PLRC ERR	P0 ST1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 ST0 INV-PLRC ERR	P0 ST1 INV-PLRC ERR
6C		DRR::D0ESTAB						
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 ST0 END-CODE ERR	P0 ST1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
6D		DRR::D0ESTAC						
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 ST0 PLRC ERR	P1 ST1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 ST0 INV-PLRC ERR	P1 ST1 INV-PLRC ERR
6E		DRR::D0ESTAC						
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 ST0 END-CODE ERR	P1 ST1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
6F		FCA::BPMWT21						
		BPM0C Value When Writing to Cache						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(1) Byte28 = 10 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::BPMWT21 BPM0C Value When Writing to Cache							
71	FCA::C2LA14M CC2 LA Value (BYTE1)							
72	FCA::C2LA14M CC2 LA Value (BYTE2)							
73	FCA::C2LA14M CC2 LA Value (BYTE3)							
74	FCA::C2LA14M CC2 LA Value (BYTE4)							
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Micro Information CDEV#							
77	Micro Information RDEV#							
78	Micro Information SCSI Command							
79	Micro Information LBA#(byte0)							
7A	Micro Information LBA#(byte1)							
7B	Micro Information LBA#(byte2)							
7C	Micro Information LBA#(byte3)							
7D	Micro Information							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E	Micro Information Error Devided Result Code							
7F	Micro Information CHK2 Detected Counter (Low)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (1/4)

	0	1	2	3	4	5	6	7
40	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE0)							
41	DRR::CD0SL1A0 Slave 1 Cache Transfer Address (BYTE1)							
42	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE2)							
43	DRR::CD0SL1A1 Slave 1 Cache Transfer Address (BYTE3)							
44	DRR::CD0SL1C0 Slave 1 Cache Transfer Address (BYTE4)							
45	DRR::CD0SL1C0 Slave 1 Cache Transfer Command (BYTE0)							
46	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE1)							
47	DRR::CD0SL1C1 Slave 1 Cache Transfer Command (BYTE2)							
48	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE0)							
49	DRR::CD0SL2A0 Slave 2 Cache Transfer Address (BYTE1)							
4A	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE2)							
4B	DRR::CD0SL2A1 Slave 2 Cache Transfer Address (BYTE3)							
4C	DRR::CD0SL2C0 Slave 2 Cache Transfer Address (BYTE4)							
4D	DRR::CD0SL2C0 Slave 2 Cache Transfer Command (BYTE0)							
4E	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE1)							
4F	DRR::CD0SL2C1 Slave 2 Cache Transfer Command (BYTE2)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (2/4)

	0	1	2	3	4	5	6	7
50		DRR::D0M0DE5						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
51		DRR::D0M0DE5						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
52		DRR::D0TXM						
		D0 TX SEQ(Master)						
53		DRR::D0MODE1						
	DTN CUDG MODE	DTN SYSTEM CLK MASK	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
54		DRR::D0MODE1						
	DTN ABORT	DTN CHSN ABORT	(RSV)	(RSV)	(RSV)	(RSV)	DTN OUT DIAG	DTN CHK2 RST
55		DRR::D0ERR						
	DTN CTL ERR	P0 CTL ERR	P1 CTL ERR	DTN DT ERR	P0 DT ERR	P1 DT ERR	P0 DT CARB/CMA ERR	P0 ST1 CARB/CMA ERR
56		DRR::D0ERR						
	P0 ERR INT	P1 ERR INT	(RSV)	TIME OVER ERR	ST0 VALID	ST1 VALID	P0 USE FLAG	P1 USE FLAG
57		DRR::D0ESTA0						
	TX DT PARITY ERR	TX PD-PNT PARITY ERR	DTN SEQ ERR	DTN WT-PNT PARITY ERR	WT DT-CNT PARITY ERR	INPUT CTL-SIG PARITY ERR	INPUT-PNT PARITY ERR	RD DT CNT PARITY ERR
58		DRR::D0ESTA0						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK ERR	P0 SYNC1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD-PNT PARITY ERR	P0 RX SEQ ERR	P0 TX WT-PNT PARITY ERR
59		DRR::D0ESTA1						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK ERR	P1 SYNC1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD-PNT PARITY ERR	P1 RX SEQ ERR	P1 TX WT-PNT PARITY ERR
5A		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		DRR::D0ESTA2						
	ST0 PLRC ERR	ST0 INV-PLRC ERR	ST0 END-CODE ERR	ST1 PLRC ERR	ST1 INV-PLRC ERR	ST1 END-CODE ERR	TRANS MODE ERR	(RSV)
5C		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
5D		DRR::D0ESTA3						
	OUT DT11 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
5E		DRR::D0ESTA3						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	TX DT4 PARITY ERR	TX DT5 PARITY ERR	TX DT6 PARITY ERR	TX DT7 PARITY ERR
5F		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (3/4)

	0	1	2	3	4	5	6	7
60		DRR::D0ESTA4						
	ST1 DT0 PARITY ERR	ST1 DT1 PARITY ERR	ST1 DT2 PARITY ERR	ST1 DT3 PARITY ERR	ST1 DT4 PARITY ERR	ST1 DT5 PARITY ERR	ST1 DT6 PARITY ERR	ST1 DT7 PARITY ERR
61		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
62		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
63		DRR::D0ESTA6						
	P0 TXX INPUT DT0 PARITY ERR	P0 TXX INPUT DT1 PARITY ERR	P0 TXX OUTPUT DT0 PARITY ERR	P0 TXX OUTPUT DT1 PARITY ERR	P1 TXX INPUT DT0 PARITY ERR	P1 TXX INPUT DT1 PARITY ERR	P1 TXX OUTPUT DT0 PARITY ERR	P1 TXX OUTPUT DT1PARITY ERR
64		DRR::D0ESTA6						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
65		DRR::D0ESTA7						
	TX DT0 PARITY ERR	TX DT1 PARITY ERR	TX DT2 PARITY ERR	TX DT3 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
66		DRR::D0ESTA7						
	INPUT DT0 PARITY ERR	INPUT DT1 PARITY ERR	INPUT DT2 PARITY ERR	INPUT DT3 PARITY ERR	P0 ERR INT	P1 ERR INT	DT CARB/CMA ERR	ST1 CARB/CMA ERR
67		DRR::D0ESTA8						
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	(RSV)	(RSV)	(RSV)	(RSV)
68		DRR::D0ESTA8						
	ST0 VALID	ST1 VALID	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)
69		DRR::D0ESTA9						
	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA9						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	(RSV)	(RSV)	(RSV)	(RSV)
6B		DRR::D0ESTAB						
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 ST0 PLRC ERR	P0 ST1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 ST0 INV-PLRC ERR	P0 ST1 INV-PLRC ERR
6C		DRR::D0ESTAB						
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 ST0 END-CODE ERR	P0 ST1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
6D		DRR::D0ESTAC						
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 ST0 PLRC ERR	P1 ST1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 ST0 INV-PLRC ERR	P1 ST1 INV-PLRC ERR
6E		DRR::D0ESTAC						
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 ST0 END-CODE ERR	P1 ST1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
6F		FCA::BPMRD21						
		BPM0C Value When Reading to Cache						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(2) Byte28 = 11 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::BPMWT21 BPM0C Value When Reading to Cache							
71	FCA::C3LA14M CC3 LA Value (BYTE1)							
72	FCA::C3LA14M CC3 LA Value (BYTE2)							
73	FCA::C3LA14M CC3 LA Value (BYTE3)							
74	FCA::C3LA14M CC3 LA Value (BYTE4)							
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Micro Information CDEV#							
77	Micro Information RDEV#							
78	Micro Information RDEV#							
79	Micro Information SCSI Command							
7A	Micro Information LBA# (BYTE0)							
7B	Micro Information LBA# (BYTE1)							
7C	Micro Information LBA# (BYTE2)							
7D	Micro Information LBA# (BYTE3)							
7E	Micro Information Error Divided Result Code							
7F	Micro Information CHK2 Detected Counter (Low)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20, F0 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E30						
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41		FCA::CHK2E30						
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42		FCA::CHK2E30						
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43		FCA::CHK2E30						
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44		FCA::CHK2E31						
	SPCNT PARITY ERR	SPOINTER PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	TRPRC PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	BPM LRC0 ERR
45		FCA::CHK2E31						
	BPM LRC1 ERR	BPM LRC2 ERR	BPM PARITY ERR0	BPM PARITY ERR1	BPM READ ADR CNT PARITY ERR	BPM WRITE ADR CNT PARITY ERR	SPMS WRITE ADR CNT PARITY ERR	SPMG WRITE ADR CNT PARITY ERR
46		FCA::CHK2E31						
	SPM WRITE PARITY ERR	SPM READ PARITY ERR	SPM LRC ERR	SPMG READ ADR CNT PARITY ERR	SPMS READ ADR CNT PARITY ERR	CW XFR SBC GEN ERR	CW SEGMENT CNT PARITY ERR	CW SLOT CNT PARITY ERR
47		FCA::CHK2E31						
	CR SEGMENT CNT PARITY ERR	CR SLOT CNT PARITY ERR	CR XFR SBC GEN ERR	FDB DCNT PARITY ERR	FDB RCNT PARITY ERR	BPM PARITY ERR (0)	BPM PARITY ERR (1)	BPM PARITY ERR (2)
48		FCA::CHK2E32						
	BPM PARITY ERR (4)	TDSB CNT PARITY ERR	CBUF POINTER0 PARITY ERR	CBUF POINTER1 PARITY ERR	CCNT PARITY ERR	PCI SERR IN DMA	(RSV)	(RSV)
49		FCA::CHK2E32						
	BPM SCNT00 PARITY ERR	BPM SCNT01 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT04 PARITY ERR	BPM SCNT05 PARITY ERR	BPM SCNT06 PARITY ERR	BPM SCNT07 PARITY ERR
4A		FCA::CHK2E32						
	BPM SCNT08 PARITY ERR	BPM SCNT09 PARITY ERR	BPM SCNT10 PARITY ERR	BPM SCNT11 PARITY ERR	BPM SCNT12 PARITY ERR	BPM SCNT13 PARITY ERR	BPM SCNT14 PARITY ERR	BPM SCNT15 PARITY ERR
4B		FCA::CHK2E32						
	BPM SCNT16 PARITY ERR	BPM SCNT17 PARITY ERR	BPM SCNT18 PARITY ERR	BPM SCNT19 PARITY ERR	BPM SCNT20 PARITY ERR	BPM SCNT21 PARITY ERR	BPM SCNT22 PARITY ERR	BPM SCNT23 PARITY ERR
4C		FCA::CHK2E33						
	BPM SCNT24 PARITY ERR	BPM SCNT25 PARITY ERR	BPM SCNT26 PARITY ERR	BPM SCNT27 PARITY ERR	BPM SCNT28 PARITY ERR	BPM SCNT29 PARITY ERR	BPM SCNT30 PARITY ERR	BPM SCNT31 PARITY ERR
4D		FCA::CHK2E40						
	DTN WBF WRITE PNT PARITY ERR	DTN WBF READ PNT PARITY ERR	DTN RBF WRITE PNT PARITY ERR	DTN RBF READ PNT PARITY ERR	QDTA ABORT	QDTA TIME OUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
4E		FCA::CHK2E40						
	FSB RADR PARITY ERR	RPOINT PARITY ERR	FCNT PARITY ERR	FPCNT PARITY ERR	NCNT PARITY ERR	NPCNT PARITY ERR	TCSBC PARITY ERR	ABUF POINT0 PARITY ERR
4F		FCA::CHK2E40						
	ABUF POINT1 PARITY ERR	ACNT PARITY ERR	APCNT PARITY ERR	BBUF POINT0 PARITY ERR	BBUF POINT1 PARITY ERR	BCNT PARITY ERR	BPCNT PARITY ERR	QDTA CHK2

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CHK2E40						
	(RSV)	(RSV)	CR CSA CNT PARITY ERR	CW SLV0 CSA CNT PARITY ERR	CW SLV1 CSA CNT PARITY ERR	FMB WADR CNT PARITY ERR	FMB RADR CNT PARITY ERR	FDB WADR CNT PARITY ERR
51		FCA::CHK2E41						
	CC0 LA CNT PARITY ERR	CC2 LA CNT PARITY ERR	CC2 LBA CNT PARITY ERR	CG2 LA CNT PARITY ERR	CC3 LA CNT PARITY ERR	CC3 LBA CNT PARITY ERR	CC4 LA CNT PARITY ERR	CC4 LBA CNT PARITY ERR
52		FCA::CHK2E41						
	SEQ50 PARITY ERR	SEQ55 PARITY ERR	SEQ75 PARITY ERR	SEQ77 PARITY ERR	FLG ERR0	FLG ERR1	(RSV)	(RSV)
53		FCA::CHK2F30						
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
54		FCA::CHK2F40						
	BBUF OUTPUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
55		FCA::CHK2F40						
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
56		FCA::CHK2F40						
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA ANY ERR
57		FCA::CHK2F40						
	DTN TX BUF0A PARITY ERR	DTN TX BUF1A PARITY ERR	DTN TX BUF2A PARITY ERR	DTN TX BUF3A PARITY ERR	DTN TX BUF4A PARITY ERR	DTN TX BUF5A PARITY ERR	DTN TX BUF6A PARITY ERR	DTN TX BUF7A PARITY ERR
58		FCA::CHK2F41						
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
59		FCA::CHK2G40						
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
5A		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		FCA::TCSBC						
		TCSBC Counter(Cache Total Transfer Subblock Number)						
5C		FCA::TCSBC						
		TCSBC Counter(Cache Total Transfer Subblock Number)						
5D		FCA::BPRD						
		Cache Write Slot Pointer						
5E		FCA::BPRD						
		Cache Write Slot Pointer						
5F		FCA::C2SLRCM						
		CC2 SLRCM Value						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::C2SVSLRC CC2 SVSLRC Value						
61		FCA::C2LA0 CC2 LA Value (BYTE0)						
62		FCA::C2LA14 CC2 LA Value (BYTE1)						
63		FCA::C2LA14 CC2 LA Value (BYTE2)						
64		FCA::C2LA14 CC2 LA Value (BYTE3)						
65		FCA::C2LA14 CC2 LA Value (BYTE4)						
66		FCA::C2LBAM CC2 LBAM Value (BYTE0)						
67		FCA::C2LBA13M CC2 LBAM Value (BYTE1)						
68		FCA::C2LBA13M CC2 LBAM Value (BYTE2)						
69		FCA::C2LBA13M CC2 LBAM Value (BYTE3)						
6A		FCA::CWCSA00 Slave 1 Cache Write Address (BYTE0)						
6B		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE1)						
6C		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE2)						
6D		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE3)						
6E		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE4)						
6F		FCA::CWCSA10 Slave 2 Cache Write Address (BYTE0)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(3) Byte28 = 20 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CWCSA1114 Slave 2 Cache Write Address (BYTE1)						
71		FCA::CWCSA1114 Slave 2 Cache Write Address (BYTE2)						
72		FCA::CWCSA1114 Slave 2 Cache Write Address (BYTE3)						
73		FCA::CWCSA1114 Slave 2 Cache Write Address (BYTE4)						
74		FCA::BMPWT21 BPM0C Value When Writing to Cache						
75		FCA::BMPWT21 BPM0C Value When Writing to Cache						
76		Micro Information CDEV#						
77		Micro Information RDEV#						
78		Micro Information SCSI Command						
79		Micro Information LBA#(byte0)						
7A		Micro Information LBA#(byte1)						
7B		Micro Information LBA#(byte2)						
7C		Micro Information LBA#(byte3)						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E		Micro Information Error Devided Result Code						
7F		Micro Information CHK2 Detected Counter (Low)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21, F1 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E30						
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41		FCA::CHK2E30						
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42		FCA::CHK2E30						
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43		FCA::CHK2E30						
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44		FCA::CHK2E31						
	SPCNT PARITY ERR	SPOINTER PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	TRPRC PARITY ERR	TWRSBC CNT PARITY ERR	TWRSSBC PARITY ERR	BPM LRC0 ERR
45		FCA::CHK2E31						
	BPM LRC1 ERR	BPM LRC2 ERR	BPM PARITY ERR0	BPM PARITY ERR1	BPM READ ADR CNT PARITY ERR	BPM WRITE ADR CNT PARITY ERR	SPMS WRITE ADR CNT PARITY ERR	SPMG WRITE ADR CNT PARITY ERR
46		FCA::CHK2E31						
	SPM WRITE PARITY ERR	SPM READ PARITY ERR	SPM LRC ERR	SPMG READ ADR CNT PARITY ERR	SPMS READ ADR CNT PARITY ERR	CW XFR SBC GEN ERR	CW SEGMENT CNT PARITY ERR	CW SLOT CNT PARITY ERR
47		FCA::CHK2E31						
	CR SEGMENT CNT PARITY ERR	CR SLOT CNT PARITY ERR	CR XFR SBC GEN ERR	FDB DCNT PARITY ERR	FDB RCNT PARITY ERR	BPM PARITY ERR (0)	BPM PARITY ERR (1)	BPM PARITY ERR (2)
48		FCA::CHK2E32						
	BPM PARITY ERR (4)	TDSB CNT PARITY ERR	CBUF POINTER0 PARITY ERR	CBUF POINTER1 PARITY ERR	CCNT PARITY ERR	PCI SERR IN DMA	(RSV)	(RSV)
49		FCA::CHK2E32						
	BPM SCNT00 PARITY ERR	BPM SCNT01 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT02 PARITY ERR	BPM SCNT04 PARITY ERR	BPM SCNT05 PARITY ERR	BPM SCNT06 PARITY ERR	BPM SCNT07 PARITY ERR
4A		FCA::CHK2E32						
	BPM SCNT08 PARITY ERR	BPM SCNT09 PARITY ERR	BPM SCNT10 PARITY ERR	BPM SCNT11 PARITY ERR	BPM SCNT12 PARITY ERR	BPM SCNT13 PARITY ERR	BPM SCNT14 PARITY ERR	BPM SCNT15 PARITY ERR
4B		FCA::CHK2E32						
	BPM SCNT16 PARITY ERR	BPM SCNT17 PARITY ERR	BPM SCNT18 PARITY ERR	BPM SCNT19 PARITY ERR	BPM SCNT20 PARITY ERR	BPM SCNT21 PARITY ERR	BPM SCNT22 PARITY ERR	BPM SCNT23 PARITY ERR
4C		FCA::CHK2E33						
	BPM SCNT24 PARITY ERR	BPM SCNT25 PARITY ERR	BPM SCNT26 PARITY ERR	BPM SCNT27 PARITY ERR	BPM SCNT28 PARITY ERR	BPM SCNT29 PARITY ERR	BPM SCNT30 PARITY ERR	BPM SCNT31 PARITY ERR
4D		FCA::CHK2E40						
	DTN WBF WRITE PNT PARITY ERR	DTN WBF READ PNT PARITY ERR	DTN RBF WRITE PNT PARITY ERR	DTN RBF READ PNT PARITY ERR	QDTA ABORT	QDTA TIME OUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
4E		FCA::CHK2E40						
	FSB RADR PARITY ERR	RPOINT PARITY ERR	FCNT PARITY ERR	FPCNT PARITY ERR	NCNT PARITY ERR	NPCNT PARITY ERR	TCSBC PARITY ERR	ABUF POINT0 PARITY ERR
4F		FCA::CHK2E40						
	ABUF POINT1 PARITY ERR	ACNT PARITY ERR	APCNT PARITY ERR	BBUF POINT0 PARITY ERR	BBUF POINT1 PARITY ERR	BCNT PARITY ERR	BPCNT PARITY ERR	QDTA CHK2

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CHK2E40						
	(RSV)	(RSV)	CR CSA CNT PARITY ERR	CW SLV0 CSA CNT PARITY ERR	CW SLV1 CSA CNT PARITY ERR	FMB WADR CNT PARITY ERR	FMB RADR CNT PARITY ERR	FDB WADR CNT PARITY ERR
51		FCA::CHK2E41						
	CC0 LA CNT PARITY ERR	CC2 LA CNT PARITY ERR	CC2 LBA CNT PARITY ERR	CG2 LA CNT PARITY ERR	CC3 LA CNT PARITY ERR	CC3 LBA CNT PARITY ERR	CC4 LA CNT PARITY ERR	CC4 LBA CNT PARITY ERR
52		FCA::CHK2E41						
	SEQ50 PARITY ERR	SEQ55 PARITY ERR	SEQ75 PARITY ERR	SEQ77 PARITY ERR	FLG ERR0	FLG ERR1	(RSV)	(RSV)
53		FCA::CHK2F30						
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
54		FCA::CHK2F30						
	PCI WBF0 PARITY ERR	PCI WBF1 PARITY ERR	PCI WBF2 PARITY ERR	PCI WBF3 PARITY ERR	PCI WBF4 PARITY ERR	PCI WBF5 PARITY ERR	PCI WBF6 PARITY ERR	PCI WBF7 PARITY ERR
55		FCA::CHK2F40						
	BBUF OUTPUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
56		FCA::CHK2F40						
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
57		FCA::CHK2F40						
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA ANY ERR
58		FCA::CHK2F40						
	DTN TX BUF0A PARITY ERR	DTN TX BUF1A PARITY ERR	DTN TX BUF2A PARITY ERR	DTN TX BUF3A PARITY ERR	DTN TX BUF4A PARITY ERR	DTN TX BUF5A PARITY ERR	DTN TX BUF6A PARITY ERR	DTN TX BUF7A PARITY ERR
59		FCA::CHK2F41						
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
5A		FCA::CHK2G40						
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
5B		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
5D		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
5E		FCA::BPRE						
		Cache Read Slot Pointer						
5F		FCA::BPRE						
		Cache Read Segment Pointer						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61	FCA::SLRC7SV							
	SLRC7SV Value							
62	FCA::C3SLRCM							
	CC3 SLRCM Value							
63	FCA::C3LA0							
	CC3 LA Value (BYTE0)							
64	FCA::C3LA14M							
	CC3 LA Value (BYTE1)							
65	FCA::C3LA14M							
	CC3 LA Value (BYTE2)							
66	FCA::C3LA14M							
	CC3 LA Value (BYTE3)							
67	FCA::C3LA14M							
	CC3 LA Value (BYTE4)							
68	FCA::C3SVLRC							
	CC3 SVLRC Value							
69	FCA::C3PLRCM							
	CC3 PLRCM Value							
6A	FCA::C3PLRCM							
	CC3 PLRCM Value							
6B	FCA::C3LBAM							
	CC3 LBAM Value (BYTE0)							
6C	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE1)							
6D	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE2)							
6E	FCA::C3LBA13M							
	CC3 LBAM Value (BYTE3)							
6F	FCA::CRCSA00							
	Cache Read Address (BYTE0)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(4) Byte28 = 21 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CRCSA0104 Cache Read Address (BYTE1)						
71		FCA::CRCSA0104 Cache Read Address (BYTE2)						
72		FCA::CRCSA0104 Cache Read Address (BYTE3)						
73		FCA::CRCSA0104 Cache Read Address (BYTE4)						
74		FCA::BMPRD21 BPM0C Value When Reading from Cache						
75		FCA::BMPRD21 BPM0C Value When Reading from Cache						
76		Micro Information CDEV#						
77		Micro Information RDEV#						
78		Micro Information SCSI Command						
79		Micro Information LBA#(byte0)						
7A		Micro Information LBA#(byte1)						
7B		Micro Information LBA#(byte2)						
7C		Micro Information LBA#(byte3)						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E		Micro Information Error Devided Result Code						
7F		Micro Information CHK2 Detected Counter (Low)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2E40							
	DTN WBF WR POINTER PARITY ERR	DTN WBF RD POINTER PARITY ERR	DTN RBF WR POINTER PARITY ERR	SEQ20 RD POINTER PARITY ERR	QDTA ABORT	QDTA TIMEOUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
41	FCA::CHK2E41							
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
42	FCA::TCSBC							
	TCSBC Counter(Cache Total Transfer Subblock Number)							
43	FCA::TCSBC							
	TCSBC Counter(Cache Total Transfer Subblock Number)							
44	FCA::BPRD							
	Cache Write Slot Pointer							
45	FCA::BPRD							
	Cache Write Slot Pointer							
46	FCA::C2SLRCM							
	CC2 SLRCM Value							
47	FCA::C2SVSLRC							
	CC2 SVSLRC Value							
48	FCA::C2LA0							
	CC2 LA Value (BYTE0)							
49	FCA::C2LA14M							
	CC2 LA Value (BYTE1)							
4A	FCA::C2LA14M							
	CC2 LA Value (BYTE2)							
4B	FCA::C2LA14M							
	CC2 LA Value (BYTE3)							
4C	FCA::C2LA14M							
	CC2 LA Value (BYTE4)							
4D	FCA::CWCSA00							
	Slave 1 Cache Write Address (BYTE0)							
4E	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE1)							
4F	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE2)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE3)						
51		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE4)						
52		FCA::CWCSA10						
		Slave 2 Cache Write Address (BYTE0)						
53		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE1)						
54		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE2)						
55		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE3)						
56		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE4)						
57		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
58		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
59		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
5A		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
5B		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5C		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		
5D		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		
5E		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5F		FCA::CHSNSTS01						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CHSNSTS01						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
61		FCA::CHSNSTS01						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
62		FCA::CHSNSTS01						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
63		FCA::CHSNSTS10						
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 Reserved	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 Reserved
64		FCA::CHSNSTS10						
	STATUS1 Reserved		STATUS1 PATH ID		STATUS1 Reserved		STATUS1 CACHE P/K#	
65		FCA::CHSNSTS10						
	STATUS1 Reserved		STATUS1 PATH ID		STATUS1 Reserved		STATUS1 CACHE P/K#	
66		FCA::CHSNSTS10						
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 Reserved	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 Reserved
67		FCA::CHSNSTS11						
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
68		FCA::CHSNSTS11						
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB Reserved	STS1 CARB Reserved
69		FCA::CHSNSTS11						
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
6A		FCA::CHSNSTS11						
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
6B		FCA::QDSTS0						
	ANT ERROR	CHK2A/2B	CHK2C	CHK2D	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
6C		FCA::QDSTS0						
	P0 ERRINT	P1 ERRINT	STATUS0 C-ERR	STATUS1 C-ERR	DT0 PLRC ERR	DT1 PLRC ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR
6D		FCA::QDSTS0						
	STATUS0 END-CODE ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	(RSV)	(RSV)	I/O DT0 ERR	I/O DT1 ERR
6E		FCA::QDSTS0						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
6F		FCA::QDSTS1						
	DTN SEQ ERR	DTN INPUT CTL ERR	DTN RD CTL ERR	DTN WT CTL ERR	P0 SYNCI PNT ERR	P1 SYNCI PNT ERR	P0 SYNCI CLOCK ERR	P1 SYNCI CLOCK ERR

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(5) Byte28 = 30 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::QDSTS1							
	P0 SLRC CNT ERR	P0 SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX WT PNT PARITY ERR	P1 SLRC CNT ERR	P1 SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX WT PNT PARITY ERR
71	FCA::QDSTS1							
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
72	FCA::QDSTS1							
	TRANS MODE ERR	ADR/CMD PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	DTN DT0-3 PARITY ERR	DTN DT4-7 PARITY ERR	P0 PLRC ERR	P1 PLRC ERR
73	DRR::D0ESTA0							
	TX DR PARITY ERR	TX RDPT PARITY ERR	DTN SEQ ERR	DTN WTPT PARITY ERR	WT DTCT PARITY ERR	INPUT CLTDT PARITY ERR	IDTPT PARITY ERR	DTN RDDCT PARITY ERR
74	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	SCSI Command							
79	Micro Information							
	LBA#(byte0)							
7A	Micro Information							
	LBA#(byte1)							
7B	Micro Information							
	LBA#(byte2)							
7C	Micro Information							
	LBA#(byte3)							
7D	Micro Information							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2E40							
	DTN WBF WR POINTER PARITY ERR	DTN WBF RD POINTER PARITY ERR	DTN RBF WR POINTER PARITY ERR	SEQ20 RD POINTER PARITY ERR	QDTA ABORT	QDTA TIMEOUT	DTN I/F PARITY ERR	DTN TIME OUT CNT PARITY ERR
41	FCA::CHK2E41							
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
42	FCA::TDSBC							
	TDSBC Counter(Drive Total Transfer Subblock Number)							
43	FCA::TDSBC							
	TDSBC Counter(Drive Total Transfer Subblock Number)							
44	FCA::BPRE							
	Cache Read Slot Pointer							
45	FCA::BPRE							
	Cache Read Segment Pointer							
46	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
47	FCA::SLRC7SV							
	SLRC7SV Value							
48	FCA::C3SLRCM							
	CC3 SLRCM Value							
49	FCA::C3LA0							
	CC3 LA Value (BYTE0)							
4A	FCA::C3LA14M							
	CC3 LA Value (BYTE1)							
4B	FCA::C3LA14M							
	CC3 LA Value (BYTE2)							
4C	FCA::C3LA14M							
	CC3 LA Value (BYTE3)							
4D	FCA::C3LA14M							
	CC3 LA Value (BYTE4)							
4E	FCA::C3SVLRC							
	CC3 SVLRC Value							
4F	FCA::C3PLRCM							
	CC3 PLRCM Value							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::C3PLRCM						
		CC3 PLRCM Value						
51		FCA::CRCSA00						
		Cache Read Address (BYTE0)						
52		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
53		FCA::CRCSA0104						
		Cache Read Address (BYTE2)						
54		FCA::CRCSA0104						
		Cache Read Address (BYTE3)						
55		FCA::CRCSA0104						
		Cache Read Address (BYTE4)						
56		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
57		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
58		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
59		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
5A		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5B		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5C		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved		STATUS0 CACHE P/K#	
5D		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
5E		FCA::CHSNSTS01						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
5F		FCA::CHSNSTS01						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CHSNSTS01						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
61		FCA::CHSNSTS01						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
62		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
65		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
66		DRR::D0ESTA0						
	TX DR PARITY ERR	TX RDPT PARITY ERR	DTN SEQ ERR	DTN WTPT PARITY ERR	WT DTCT PARITY ERR	INPUT CLTDT PARITY ERR	IDTPT PARITY ERR	DTN RDDCT PARITY ERR
67		DRR::D0ESTA0						
	P0 SYNCI0 PNT PARITY ERR	P0 SYNCI1 PNT PARITY ERR	P0 SYNCI0 CLOCK ERR	P0 SYNCI1 CLOCK ERR	P0 TXX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX WT PNT PARITY ERR
68		DRR::D0ESTA1						
	P1 SYNCI0 PNT PARITY ERR	P1 SYNCI1 PNT PARITY ERR	P1 SYNCI0 CLOCK ERR	P1 SYNCI1 CLOCK ERR	P1 TXX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX WT PNT PARITY ERR
69		DRR::D0ESTA1						
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6A		DRR::D0ESTA2						
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	STATUS1 END-CODE ERR	TRANS MODE ERR	(RSV)
6B		DRR::D0ESTA2						
	ADR/CMD PLRC ERR	ADR/CMD INV-PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	OUT DT00 PARITY ERR	OUT DT01 PARITY ERR	OUT DT02 PARITY ERR	OUT DT03 PARITY ERR
6C		DRR::D0ESTA3						
	OUT DT10 PARITY ERR	OUT DT11 PARITY ERR	OUT DT12 PARITY ERR	OUT DT13 PARITY ERR	OUTPUT LOOP DT0 PARITY ERR	OUTPUT LOOP DT1 PARITY ERR	OUTPUT LOOP DT2 PARITY ERR	OUTPUT LOOP DT3 PARITY ERR
6D		DRR::D0ESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
6E		DRR::D0ESTA5						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR
6F		DRR::D0ESTA6						
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(6) Byte28 = 31 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::D0ESTA6						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
71		DRR::D0ESTA7						
	IN DT0 PARITY ERR	IN DT1 PARITY ERR	IN DT2 PARITY ERR	IN DT3 PARITY ERR	P0 ERRINT	P1 ERRINT	P0 DT CARB/CMA ERR	P0 STATUS1 CARB/CMA ERR
72		DRR::D0ESTAB						
	P0 ADR/CMD PLRC ERR	P0 DT PLRC ERR	P0 STATUS0 PLRC ERR	P0 STATUS1 PLRC ERR	P0 ADR/CMD INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 STATUS0 INV-PLRC ERR	P0 STATUS1 INV-PLRC ERR
73		DRR::D0ESTAB						
	P0 ADR/CMD END-CODE ERR	P0 DT END-CODE ERR	P0 STATUS0 END-CODE ERR	P0 STATUS1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
74		DRR::D0ESTAC						
	P1 ADR/CMD PLRC ERR	P1 DT PLRC ERR	P1 STATUS0 PLRC ERR	P1 STATUS1 PLRC ERR	P1 ADR/CMD INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 STATUS0 INV-PLRC ERR	P1 STATUS1 INV-PLRC ERR
75		DRR::D0ESTAC						
	P1 ADR/CMD END-CODE ERR	P1 DT END-CODE ERR	P1 STATUS0 END-CODE ERR	P1 STATUS1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		SCSI Command						
79		Micro Information						
		LBA#(byte0)						
7A		Micro Information						
		LBA#(byte1)						
7B		Micro Information						
		LBA#(byte2)						
7C		Micro Information						
		LBA#(byte3)						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2E30						
	(RSV)	SEQ15 PARITY ERR	SEQ00 PARITY ERR	SEQ20 PARITY ERR	SEQ25 PARITY ERR	SEQ27 PARITY ERR	SEQ28 PARITY ERR	SEQ30 PARITY ERR
41		FCA::CHK2E30						
	SEQ31 PARITY ERR	SEQ33 PARITY ERR	SEQ34 PARITY ERR	SEQ40 PARITY ERR	SEQ45 PARITY ERR	SEQ63 PARITY ERR	SEQ70 PARITY ERR	SEQ72 PARITY ERR
42		FCA::CHK2E30						
	SEQ90 PARITY ERR	SEQ92 PARITY ERR	PCI WBF WRITE PNT ERR	PCI WBF READ PNT ERR	PCI RBF WRITE PNT ERR	PCI RBF READ PNT ERR	(RSV)	PBF0 CNT PARITY ERR
43		FCA::CHK2E30						
	PBF1 CNT PARITY ERR	PBF0 READ ADDRESS PARITY ERR	PBF1 READ ADDRESS PARITY ERR	PBF0 WRITE ADDRESS PARITY ERR	PBF1 WRITE ADDRESS PARITY ERR	FSB CNT PARITY ERR	FSB WRITE ADDRESS PARITY ERR	SCNT PARITY ERR
44		FCA::CHK2F30						
	PCI RBF0 PARITY ERR	PCI RBF1 PARITY ERR	PCI RBF2 PARITY ERR	PCI RBF3 PARITY ERR	PCI RBF4 PARITY ERR	PCI RBF5 PARITY ERR	PCI RBF6 PARITY ERR	PCI RBF7 PARITY ERR
45		FCA::CHK2F30						
	PCI WBF0 PARITY ERR	PCI WBF1 PARITY ERR	PCI WBF2 PARITY ERR	PCI WBF3 PARITY ERR	PCI WBF4 PARITY ERR	PCI WBF5 PARITY ERR	PCI WBF6 PARITY ERR	PCI WBF7 PARITY ERR
46		FCA::TCSBC						
		TCSBC Counter(Cache Total Transfer Subblock Number)						
47		FCA::TCSBC						
		TCSBC Counter(Cache Total Transfer Subblock Number)						
48		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
49		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
4A		FCA::BPRD						
		Cache Write Slot Pointer						
4B		FCA::BPRD						
		Cache Write Segment Pointer						
4C		FCA::BPRE						
		Cache Read Slot Pointer						
4D		FCA::BPRE						
		Cache Read Segment Pointer						
4E		FCA::PBFID						
		PBF0 Side DMA ID						
4F		FCA::PBFID						
		PBF0 Side DMA ID						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::PBFID						
		PBF1 Side DMA ID						
51		FCA::PBFID						
		PBF1 Side DMA ID						
52		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
53		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
54		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
55		FCA::BMPWT21						
		BPM0C Value When Writing to Cache						
56		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
57		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
58		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
59		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
5A		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5B		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5C		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5E		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5F		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (3/4)

	0	1	2	3	4	5	6	7
60	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
61	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
62	FCA::PCICTL							
	PCI BUS RESET	PCI ARB RESET	OPEN MODE	PCI BUS ENABLE	PCI ARB ENABLE	REQ0 ENABLE	REQ1 ENABLE	REQ2 ENABLE
63	FCA::PCICTL							
	SERR OUT ENABLE	SERR RCV ENABLE	PERR RCV ENABLE	(RSV)	(RSV)	(RSV)	(RSV)	PCI DATA EX MODE
64	FCA::SPREQAD							
	PDEV ID							
65	FCA::SPREQAD							
	QUE ID							
66	FCA::DPREQAD							
	PDEV ID							
67	FCA::DPREQAD							
	QUE ID							
68	FCA::TLMWAM							
	TLMWAM Value							
69	FCA::TLMWAM							
	TLMWAM Value							
6A	FCA::TLMRAM							
	TLMRAM Value							
6B	FCA::TLMRAM							
	TLMRAM Value							
6C	FCA::CWCSA00							
	Slave 1 Cache Write Address (BYTE0)							
6D	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE1)							
6E	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE2)							
6F	FCA::CWCSA0104							
	Slave 1 Cache Write Address (BYTE3)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(7) Byte28 = 40, 41, 60, 61 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE4)						
71		FCA::CRCSA00						
		Cache Read Address (BYTE0)						
72		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
73		FCA::CRCSA0104						
		Cache Read Address (BYTE2)						
74		FCA::CRCSA0104						
		Cache Read Address (BYTE3)						
75		FCA::CRCSA0104						
		Cache Read Address (BYTE4)						
76		Micro Information						
		CDEV#						
77		Micro Information						
		RDEV#						
78		Micro Information						
		SCSI Command						
79		Micro Information						
		LBA#(byte0)						
7A		Micro Information						
		LBA#(byte1)						
7B		Micro Information						
		LBA#(byte2)						
7C		Micro Information						
		LBA#(byte3)						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::CHK2G40							
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
41	FCA::CHK2G40							
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
42	FCA::TCSBC							
	TCSBC Counter(Cache Total Transfer Subblock Number)							
43	FCA::TCSBC							
	TCSBC Counter(Cache Total Transfer Subblock Number)							
44	FCA::BPRD							
	Cache Write Slot Pointer							
45	FCA::BPRD							
	Cache Write Segment Pointer							
46	FCA::LA2FEEX							
	LA Value of Start Subblock When LA Err Occurred (BYTE0)							
47	FCA::LA2FEEX							
	LA Value of LA Err Detected Subblock (BYTE0)							
48	FCA::LA2FEEX							
	Expected LA Value When LA Err Occurred (BYTE0)							
49	FCA::C2LA14M							
	CC2 LA Value (BYTE1)							
4A	FCA::C2LA14M							
	CC2 LA Value (BYTE2)							
4B	FCA::C2LA14M							
	CC2 LA Value (BYTE3)							
4C	FCA::C2LA14M							
	CC2 LA Value (BYTE4)							
4D	FCA::LA2FNC							
	Expected LA Value When LA Err Occurred (BYTE1)							
4E	FCA::LA2FNC							
	Expected LA Value When LA Err Occurred (BYTE2)							
4F	FCA::LA2FNC							
	Expected LA Value When LA Err Occurred (BYTE3)							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::LA2FNC Expected LA Value When LA Err Occurred (BYTE4)						
51		FCA::LA2INI LA Value of Start Subblock When LA Err Occurred (BYTE1)						
52		FCA::LA2INI LA Value of Start Subblock When LA Err Occurred (BYTE2)						
53		FCA::LA2INI LA Value of Start Subblock When LA Err Occurred (BYTE3)						
54		FCA::LA2INI LA Value of Start Subblock When LA Err Occurred (BYTE4)						
55		FCA::LA2ERR LA Value of LA Err Detected Subblock (BYTE1)						
56		FCA::LA2ERR LA Value of LA Err Detected Subblock (BYTE2)						
57		FCA::LA2ERR LA Value of LA Err Detected Subblock (BYTE3)						
58		FCA::LA2ERR LA Value of LA Err Detected Subblock (BYTE4)						
59		FCA::C2LBAM CC2 LBAM Value (BYTE0)						
5A		FCA::C2LBA13M CC2 LBAM Value (BYTE1)						
5B		FCA::C2LBA13M CC2 LBAM Value (BYTE2)						
5C		FCA::C2LBA13M CC2 LBAM Value (BYTE3)						
5D		FCA::CWCSA00 Slave 1 Cache Write Address (BYTE0)						
5E		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE1)						
5F		FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE2)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (3/4)

	0	1	2	3	4	5	6	7
60	FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE3)							
61	FCA::CWCSA0104 Slave 1 Cache Write Address (BYTE4)							
62	FCA::BMPWT21 BPM0C Value When Writing to Cache							
63	FCA::BMPWT21 BPM0C Value When Writing to Cache							
64	FCA::BMPWT21 BPM0C Value When Writing to Cache							
65	FCA::BMPWT21 BPM0C Value When Writing to Cache							
66	FCA::SPMSW00 SPMSW00 Value							
67	FCA::SPMSW01 SPMSW01 Value							
68	FCA::SPMSW01 SPMSW01 Value							
69	FCA::SPMSW01 SPMSW01 Value							
6A	FCA::SPMSW01 SPMSW01 Value							
6B	FCA::PBFID PBF0 Side DMA ID							
6C	FCA::PBFID PBF0 Side DMA ID							
6D	FCA::PBFID PBF1 Side DMA ID							
6E	FCA::PBFID PBF1 Side DMA ID							
6F	FCA::SPREQAD PDEV ID							

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(8) Byte28 = 48 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::SPREQAD QUE ID						
71		FCA::DPREQAD PDEV ID						
72		FCA::DPREQAD QUE ID						
73		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
75		Reserved						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76		Micro Information CDEV#						
77		Micro Information RDEV#						
78		Micro Information SCSI Command						
79		Micro Information LBA#(byte0)						
7A		Micro Information LBA#(byte1)						
7B		Micro Information LBA#(byte2)						
7C		Micro Information LBA#(byte3)						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E		Micro Information Error Devided Result Code						
7F		Micro Information CHK2 Detected Counter (Low)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (1/4)

	0	1	2	3	4	5	6	7
40		FCA::CHK2G40						
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC,S LA ERR	CC4 LBA ERR
41		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
42		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
43		FCA::TDSBC						
		TDSBC Counter(Drive Total Transfer Subblock Number)						
44		FCA::BPRE						
		Cache Read Slot Pointer						
45		FCA::BPRE						
		Cache Read Segment Pointer						
46		FCA::LA3FEEX						
		LA Value of Start Subblock When LA Err Occurred (BYTE0)						
47		FCA::LA3FEEX						
		LA Value of LA Err Detected Subblock (BYTE0)						
48		FCA::C3PLRCM						
		CC3 PLRCM Value						
49		FCA::C3PLRCM						
		CC3 PLRCM Value						
4A		FCA::LA3FEEX						
		Expected LA Value When LA Err Occurred (BYTE0)						
4B		FCA::C3LA14M						
		CC3 LA Value (BYTE1)						
4C		FCA::C3LA14M						
		CC3 LA Value (BYTE2)						
4D		FCA::C3LA14M						
		CC3 LA Value (BYTE3)						
4E		FCA::C3LA14M						
		CC3 LA Value (BYTE4)						
4F		FCA::LA3FNC						
		Expected LA Value When LA Err Occurred (BYTE1)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (2/4)

	0	1	2	3	4	5	6	7
50		FCA::LA3FNC Expected LA Value When LA Err Occurred (BYTE2)						
51		FCA::LA3FNC Expected LA Value When LA Err Occurred (BYTE3)						
52		FCA::LA3FNC Expected LA Value When LA Err Occurred (BYTE4)						
53		FCA::LA3INI LA Value of Start Subblock When LA Err Occurred (BYTE1)						
54		FCA::LA3INI LA Value of Start Subblock When LA Err Occurred (BYTE2)						
55		FCA::LA3INI LA Value of Start Subblock When LA Err Occurred (BYTE3)						
56		FCA::LA3INI LA Value of Start Subblock When LA Err Occurred (BYTE4)						
57		FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE1)						
58		FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE2)						
59		FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE3)						
5A		FCA::LA3ERR LA Value of LA Err Detected Subblock (BYTE4)						
5B		FCA::C3LBAM CC3 LBAM Value (BYTE0)						
5C		FCA::C3LBA13M CC3 LBAM Value (BYTE1)						
5D		FCA::C3LBA13M CC3 LBAM Value (BYTE2)						
5E		FCA::C3LBA13M CC3 LBAM Value (BYTE3)						
5F		FCA::CRCSA00 Cache Read Address (BYTE0)						

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (3/4)

	0	1	2	3	4	5	6	7
60		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
61		FCA::CRCSA0104						
		Cache Read Address (BYTE2)						
62		FCA::CRCSA0104						
		Cache Read Address (BYTE3)						
63		FCA::CRCSA0104						
		Cache Read Address (BYTE4)						
64		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
65		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
66		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
67		FCA::BMPRD21						
		BPM0C Value When Reading from Cache						
68		FCA::SPMSR00						
		SPMSR00 Value						
69		FCA::SPMSR01						
		SPMSR01 Value						
6A		FCA::SPMSR01						
		SPMSR01 Value						
6B		FCA::SPMSR01						
		SPMSR01 Value						
6C		FCA::SPMSR01						
		SPMSR01 Value						
6D		FCA::CHSNSTS00						
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
6E		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		
6F		FCA::CHSNSTS00						
	STATUS0 Reserved	STATUS0 PATH ID			STATUS0 Reserved	STATUS0 CACHE P/K#		

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Byte27 = 8A (FCA CHK2) Byte40-7F Detail
(9) Byte28 = 19 (4/4)

	0	1	2	3	4	5	6	7
70	FCA::CHSNSTS00							
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 Reserved	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 Reserved
71	FCA::CHSNSTS01							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
72	FCA::CHSNSTS01							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB Reserved	STS0 CARB Reserved
73	FCA::CHSNSTS01							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
74	FCA::CHSNSTS01							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
75	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
76	Micro Information							
	CDEV#							
77	Micro Information							
	RDEV#							
78	Micro Information							
	SCSI Command							
79	Micro Information							
	LBA#(byte0)							
7A	Micro Information							
	LBA#(byte1)							
7B	Micro Information							
	LBA#(byte2)							
7C	Micro Information							
	LBA#(byte3)							
7D	Micro Information							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	CHK2 FCA#
7E	Micro Information							
	Error Devided Result Code							
7F	Micro Information							
	CHK2 Detected Counter (Low)							

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Byte27 = 8B (DRR CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
05								
06	Format Message							
07	P/K Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	RCV SIM	0	0	0	0	0	0	0
10	LDEV#							
11								
12	CDEV#				RDEV#			
13	SEMI-SYNC	RCU SIM	0	0	RCU#			
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTRL no.	DKU Physical Device no.				
25	Cylinder Address (Low)							
26	Cylinder Address (High)				Head Address			
27	Format (x‘8’)				Message (x‘B’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
31								
32	Module ID							
33	Routine ID							
34	P/K ID				Message Code (x‘0’)			
35	SSID for Self Subsystem							
36	Symptom Code (x'FF89':LDEV Type=DKU87I / x’EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
7F								

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(1) Byte28 = 10

	0	1	2	3	4	5	6	7
28	SubCode (x'10' : DRR CHK2B - DRR DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(2) Byte28 = 11

	0	1	2	3	4	5	6	7
28	SubCode (x'11' : DRR CHK2B - CHSN0 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA5							
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
2C	DRR::DRESTA6							
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P0 RX DT2 PARITY ERR	P0 RX DT3 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR
2D	DRR::DRESTA6							
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR
2E	DRR::DRESTAB							
	P0 AC PLRC ERR	P0 DT PLRC ERR	P0 STATUS0 PLRC ERR	P0 STATUS1 PLRC ERR	P0 AC PLRC-IV ERR	P0 DT PLRC-IV ERR	P0 STATUS0 PLRC-IV ERR	P0 STATUS1 PLRC-IV ERR
2F	DRR::DRESTAB							
	P0 AC END CODE ERR	P0 DT END CODE ERR	P0 STATUS0 END CODE ERR	P0 STATUS1 END CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
30	DRR::DRESTA8							
	LA0/LA1 COMP ERR	LA2 COMP ERR	SYND(ECC) ERR	DT END CODE ERR	P0 ERRINT	P1 ERRINT	STATUS0 CARB/CMA ERR	STATUS1 CARB/CMA ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(3) Byte28 = 12

	0	1	2	3	4	5	6	7
28	SubCode (x'12' : DRR CHK2B - CHSN1 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA6							
	P0 TXX I-DT0 PARITY ERR	P0 TXX I-DT1 PARITY ERR	P0 TXX O-DT0 PARITY ERR	P0 TXX O-DT1 PARITY ERR	P1 TXX I-DT0 PARITY ERR	P1 TXX I-DT1 PARITY ERR	P1 TXX O-DT0 PARITY ERR	P1 TXX O-DT1 PARITY ERR
2C	DRR::DRESTA7							
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
2D	DRR::DRESTA7							
	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P1 RX DT2 PARITY ERR	P1 RX DT3 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
2E	DRR::DRESTAC							
	P1 AC PLRC ERR	P1 DT PLRC ERR	P1 STATUS0 PLRC ERR	P1 STATUS1 PLRC ERR	P1 AC PLRC-IV ERR	P1 DT PLRC-IV ERR	P1 STATUS0 PLRC-IV ERR	P1 STATUS1 PLRC-IV ERR
2F	DRR::DRESTAC							
	P1 AC END CODE ERR	P1 DT END CODE ERR	P1 STATUS0 END CODE ERR	P1 STATUS1 END CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
30	DRR::DRESTA8							
	LA0/LA1 COMP ERR	LA2 COMP ERR	SYND(ECC) ERR	DT END CODE ERR	P0 ERRINT	P1 ERRINT	STATUS0 CARB/CMA ERR	STATUS1 CARB/CMA ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(4) Byte28 = 13

	0	1	2	3	4	5	6	7
28	SubCode (x'13' : DRR CHK2B - DRR&CHSN0 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(5) Byte28 = 14

	0	1	2	3	4	5	6	7
28	SubCode (x'14' : DRR CHK2B - DRR&CHSN1 DATA ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(6) Byte28 =20

	0	1	2	3	4	5	6	7
28	SubCode (x'20' : DRR CHK2B - DRR DATA ERROR2)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(7) Byte28 =30

	0	1	2	3	4	5	6	7
28	SubCode (x'30' : DRR CHK2A - DRR CTL ERROR)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRERR							
	DRR CTL ERR	P0 CTL ERR	P1 CTL ERR	DRR DT ERR	P0 DT ERR	P1 DT ERR	STATUS0 CARB/CMA ERR	STATUS1 CARB/CMA ERR
2C	DRR::DRESTA0							
	CMD A/B SEQ ERR	TRANS SEQ ERR	DRB-CBUF SEQ ERR	CBUF-DM0 SEQ ERR	DM0-BUFF SEQ ERR	CBUF-CHSN SEQ ERR	CBUF→PBUF WR-PNT PARITY ERR	CBUF→DM0 PK-CNT PARITY ERR
2D	DRR::DRESTA0							
	DRB→CBUF PK-CNT PARITY ERR	CBUF→PBUF PK-CNT PARITY ERR	PBUF→CBUF PK-CNT PARITY ERR	TL CNT PARITY ERR	PL CNT PARITY ERR	TL/PL PRM ERR CMD A	TL/PL PRM ERR CMD B	DRB WT-ADR CNT PARITY ERR
2E	DRR::DRESTA1							
	DRB RD-ADR CNT PARITY ERR	SB-BLK DT-CNT PARITY ERR	C0BUF WT-ADR CNT PARITY ERR	C0BUF RD-ADR CNT PARITY ERR	C1BUF WT-ADR CNT PARITY ERR	C1BUF RD-ADR CNT PARITY ERR	BMP0 DT PERR	BMP1 DT PERR
2F	DRR::DRESTA1							
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK PARITY ERR	P0 SYNC1 CLOCK PARITY ERR	P0 TX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX RD PNT PARITY ERR
30	DRR::DRESTA2							
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK PARITY ERR	P1 SYNC1 CLOCK PARITY ERR	P1 TX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX RD PNT PARITY ERR
31	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(8) Byte28 =40

	0	1	2	3	4	5	6	7
28	SubCode (x'40' : DRR CHK2D - ARBITER TIMER ERROR)							
29	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE
2A	DRR::P0ETM0							
	P0 ENT-TIMER (High)							
2B	DRR::P0ETM0							
	P0 ENT-TIMER (High)							
2C	DRR::P0ETM1							
	P0 ENT-TIMER (Low)							
2D	DRR::P0ETM1							
	P0 ENT-TIMER (Low)							
2E	DRR::P0ATM0							
	P0 ACK-TIMER (High)							
2F	DRR::P0ATM0							
	P0 ACK-TIMER (High)							
30	DRR::P0ATM1							
	P0 ACK-TIMER (Low)							
31	DRR::P0ATM1							
	P0 ACK-TIMER (Low)							

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(9) Byte28 =A0

	0	1	2	3	4	5	6	7
28	SubCode (x'A0' : DRR NO ERR - TIME OVER)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(10) Byte28 =B0

	0	1	2	3	4	5	6	7
28	SubCode (x'B0' : DRR CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(11) Byte28 =B1

	0	1	2	3	4	5	6	7
28	SubCode (x'B1' : P0 CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte28-31 Detail
(12) Byte28 =B2

	0	1	2	3	4	5	6	7
28	SubCode (x'B2' : P1 CHK2C)							
29	DRR::STATS							
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer End	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
2A	DRR::STATS							
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	Abort Detected	Force Err Detected
2B	DRR::DRESTA2							
	P0 TX SEQ PARITY ERR	P1 TX SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRC-GEN DT PARITY ERR0	AC PLRC-GEN DT PARITY ERR1	DT PLRC-GEN DT PARITY ERR0	DT PLRC-GEN DT PARITY ERR1
2C	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE ERR	LA DT PARITY ERR
2D	DRR::DRESTA3							
	DM0 DT0 PARITY ERR	DM0 DT1 PARITY ERR	DM0 DT2 PARITY ERR	DM0 DT3 PARITY ERR	DM0 DT4 PARITY ERR	DM0 DT5 PARITY ERR	DM0 DT6 PARITY ERR	DM0 DT7 PARITY ERR
2E	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
2F	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
30	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
31	DRR::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 10, 20, 30, 40, A0, B0 (1/4)

	0	1	2	3	4	5	6	7
40	MMC::RCVINT							
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41	MMC::RCVINT							
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42	DRR::DRMODE1							
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43	DRR::DRMODE1							
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44	DRR::DRMODE5							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45	DRR::DRMODE5							
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46	DRR::CMD0A							
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47	DRR::CMD0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48	DRR::ADR0A							
	CMD A Slave 1 Cache Transfer Address (BYTE0)							
49	DRR::ADR0A							
	CMD A Slave 2 Cache Transfer Address (BYTE0)							
4A	DRR::ADR1A							
	CMD A Slave 1 Cache Transfer Address (BYTE1)							
4B	DRR::ADR3A							
	CMD A Slave 2 Cache Transfer Address (BYTE1)							
4C	DRR::TRMDA							
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D	DRR::TRMDA							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E	DRR::LA0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F	DRR::LA0A							
	CMD A Expect LA Value (BYTE0)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 10, 20, 30, 40, A0, B0 (2/4)

	0	1	2	3	4	5	6	7
50	DRR::LA1A							
	CMD A Expect LA Value (BYTE1)							
51	DRR::LA1A							
	CMD A Expect LA Value (BYTE2)							
52	DRR::LA2A							
	CMD A Expect LA Value (BYTE3)							
53	DRR::LA2A							
	CMD A Expect LA Value (BYTE4)							
54	DRR::CMD0B							
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55	DRR::CMD0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	DRR::ADR0B							
	CMD B Slave 1 Cache Transfer Address (BYTE0)							
57	DRR::ADR0B							
	CMD B Slave 2 Cache Transfer Address (BYTE0)							
58	DRR::ADR1B							
	CMD B Slave 1 Cache Transfer Address (BYTE1)							
59	DRR::ADR3B							
	CMD B Slave 2 Cache Transfer Address (BYTE1)							
5A	DRR::TRMDB							
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B	DRR::TRMDB							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C	DRR::LA0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	DRR::LA0B							
	CMD B Expect LA Value (BYTE0)							
5E	DRR::LA1B							
	CMD B Expect LA Value (BYTE1)							
5F	DRR::LA1B							
	CMD B Expect LA Value (BYTE2)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 10, 20, 30, 40, A0, B0 (3/4)

	0	1	2	3	4	5	6	7
60	DRR::LA2B							
	CMD B Expect LA Value (BYTE3)							
61	DRR::LA2B							
	CMD B Expect LA Value (BYTE4)							
62	DRR::RLALR0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	DRR::RLALR0							
	LA Value When LA ERR Occurred (BYTE0)							
64	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE1)							
65	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE2)							
66	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE3)							
67	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE4)							
68	DRR::D64CNTM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69	DRR::D64CNTM							
	Command Pointer(Low)							
6A	DRR::DRSEQM							
	DRSEQM							
6B	DRR::PBSEQM							
	PBSEQM							
6C	DRR::DMISQMREG							
	DMISQMREG							
6D	DRR::TRISQMREG							
	TRISQMREG							
6E	DRR::P0TXSQM							
	P0TXSQM							
6F	DRR::P0RXSQM							
	P0RXSQM							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(1) Byte28 = 10, 20, 30, 40, A0, B0 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::P1TXSQM						
		P1TXSQM						
71		DRR::P1RXSQM						
		P1TXSQM						
72		DRR::DRREV						
	QDTA FLAG (1:QDTA)	(RSV)	MP# '00':MP_A '01':MP_B '02':MP_A '03':MP_B		LSI Rev.			
73		DRR::DRREV						
	SELF MP ALARM	SELF MP MESSAGE	SELF MP CUDG3AFAIL	SELF MP CUDG3BFAIL	LSIMP ALARM	LSIMP MESSAGE	LSIMP CUDG3AFAIL	LSIMP CUDG3BFAIL
74		DRR::STATS						
	CMD A Transfer End	(RSV)	CMD A Transfer Start	CMD A Transfer Executing	CMD B Transfer END	(RSV)	CMD B Transfer Start	CMD B Transfer Executing
75		DRR::STATS						
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	ABORT Detected	Force Err Detected
76		DRR::DRESTAD						
	ARB SEQ PARITY ERR (M)	ARB SEQ PARITY ERR (S)	P0 ARB CMP CHK ERR	P1 ARB CMP CHK ERR	PKID CHK ERR	(RSV)	(RSV)	(RSV)
77		DRR::DRESTAD						
	CBUF0/1 DATA0 PARITY ERR	CBUF0/1 DATA1 PARITY ERR	CBUF0/1 DATA2 PARITY ERR	CBUF0/1 DATA3 PARITY ERR	CBUF0/1 DATA4 PARITY ERR	CBUF0/1 DATA5 PARITY ERR	CBUF0/1 DATA6 PARITY ERR	CBUF0/1 DATA7 PARITY ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(2) Byte28 = 11, 13, B1 (1/4)

	0	1	2	3	4	5	6	7
40	MMC::RCVINT							
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41	MMC::RCVINT							
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42	DRR::DRMODE1							
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43	DRR::DRMODE1							
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44	DRR::DRMODE5							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45	DRR::DRMODE5							
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46	DRR::CMD0A							
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47	DRR::CMD0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48	DRR::ADR0A							
	CMD A Slave 1 Cache Transfer Address (BYTE0)							
49	DRR::ADR0A							
	CMD A Slave 2 Cache Transfer Address (BYTE0)							
4A	DRR::ADR1A							
	CMD A Slave 1 Cache Transfer Address (BYTE1)							
4B	DRR::ADR3A							
	CMD A Slave 2 Cache Transfer Address (BYTE1)							
4C	DRR::TRMDA							
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D	DRR::TRMDA							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E	DRR::LA0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F	DRR::LA0A							
	CMD A Expect LA Value (BYTE0)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (2/4)

	0	1	2	3	4	5	6	7
50	DRR::LA1A							
	CMD A Expect LA Value (BYTE1)							
51	DRR::LA1A							
	CMD A Expect LA Value (BYTE2)							
52	DRR::LA2A							
	CMD A Expect LA Value (BYTE3)							
53	DRR::LA2A							
	CMD A Expect LA Value (BYTE4)							
54	DRR::CMD0B							
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55	DRR::CMD0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	DRR::ADR0B							
	CMD B Slave 1 Cache Transfer Address (BYTE0)							
57	DRR::ADR0B							
	CMD B Slave 2 Cache Transfer Address (BYTE0)							
58	DRR::ADR1B							
	CMD B Slave 1 Cache Transfer Address (BYTE1)							
59	DRR::ADR3B							
	CMD B Slave 2 Cache Transfer Address (BYTE1)							
5A	DRR::TRMDB							
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B	DRR::TRMDB							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C	DRR::LA0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	DRR::LA0B							
	CMD B Expect LA Value (BYTE0)							
5E	DRR::LA1B							
	CMD B Expect LA Value (BYTE1)							
5F	DRR::LA1B							
	CMD B Expect LA Value (BYTE2)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (3/4)

	0	1	2	3	4	5	6	7
60	DRR::LA2B							
	CMD B Expect LA Value (BYTE3)							
61	DRR::LA2B							
	CMD B Expect LA Value (BYTE4)							
62	DRR::RLALR0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	DRR::RLALR0							
	LA Value When LA ERR Occurred (BYTE0)							
64	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE1)							
65	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE2)							
66	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE3)							
67	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE4)							
68	DRR::D64CNTM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69	DRR::D64CNTM							
	Command Pointer(Low)							
6A	DRR::DRST10							
	CHSN STATUS0 BYTE0							
6B	DRR::DRST10							
	CHSN STATUS0 BYTE1							
6C	DRR::DRST11							
	CHSN STATUS0 BYTE1 (SUB)							
6D	DRR::DRST11							
	CHSN STATUS0 BYTE0 (SYB)							
6E	DRR::DRST20							
	CHSN STATUS1 BYTE0							
6F	DRR::DRST20							
	CHSN STATUS1 BYTE1							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(2) Byte28 = 11, 13, B1 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::DRST21						
		CHSN STATUS1 BYTE1 (SUB)						
71		DRR::DRST21						
		CHSN STATUS1 BYTE0 (SUB)						
72		DRR::DRESTA4						
	STS0 DT0 PARITY ERR	STS0 DT1 PARITY ERR	STS0 DT2 PARITY ERR	STS0 DT3 PARITY ERR	STS0 DT4 PARITY ERR	STS0 DT5 PARITY ERR	STS0 DT6 PARITY ERR	STS0 DT7 PARITY ERR
73		DRR::DRESTA5						
	P0 TX DT0 PARITY ERR	P0 TX DT1 PARITY ERR	P0 TX DT2 PARITY ERR	P0 TX DT3 PARITY ERR	P0 TX DT4 PARITY ERR	P0 TX DT5 PARITY ERR	P0 TX DT6 PARITY ERR	P0 TX DT7 PARITY ERR
74		DRR::DRESTA6						
	P0 RX DT0 PARITY ERR	P0 RX DT1 PARITY ERR	P0 RX DT2 PARITY ERR	P0 RX DT3 PARITY ERR	P0 RX DT4 PARITY ERR	P0 RX DT5 PARITY ERR	P0 RX DT6 PARITY ERR	P0 RX DT7 PARITY ERR
75		DRR::DRESTA6						
	P0 TXX I-DT0	P0 TXX I-DT1	P0 TXX O-DT0	P0 TXX O-DT1	P1 TXX I-DT0	P1 TXX I-DT1	P1 TXX O-DT0	P1 TXX O-DT1
76		DRR::DRESTAB						
	P0 AC PLRC ERR	P0 DT PLRC ERR	P0 STS0 PLRC ERR	P1 STS0 PLRC ERR	P0 AC INV-PLRC ERR	P0 DT INV-PLRC ERR	P0 STS0 INV-PLRC ERR	P0 STS1 INV-PLRC ERR
77		DRR::DRESTAB						
	P0 AC END-CODE ERR	P0 DT END-CODE ERR	P0 STS0 END-CODE ERR	P0 STS1 END-CODE ERR	P0 SLRC CHECK ERR	P0 SLRC CAL DT ERR	P0 SLRC RD DT ERR	P0 SBLK DCNT ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(3) Byte28 = 12, 14, B2 (1/4)

	0	1	2	3	4	5	6	7
40	MMC::RCVINT							
	SYSRST Interrupt Monitor	SELRST Interrupt Monitor	CHK1A Interrupt Monitor	CHK1B Interrupt Monitor	SMP Interrupt Monitor	LAN/SIO Interrupt Monitor	CHA/DRR Interrupt Monitor	ADP/SCA0 Interrupt Monitor
41	MMC::RCVINT							
	(RSV)	CHK3 Interrupt Monitor	(RSV)	SCA1 Interrupt Monitor	SCA2 Interrupt Monitor	SCA3 Interrupt Monitor	SCA4 Interrupt Monitor	SCA5 Interrupt Monitor
42	DRR::DRMODE1							
	DRR CUDG MODE	DRR SYSTEM CLK MASK	DRR FORCE ERR	(RSV)	(RSV)	DRB W/R ENABLE	SLRC CHK MASK	SUBBLOCK DT-NO
43	DRR::DRMODE1							
	64-CMD MODE	SLAVE 2 ADR SEL	DATA ERR REPORT ENABLE	CHSN ABORT	(RSV)	RNGOSC ENABLE	DRR ABORT	DRR CHK2RST ON
44	DRR::DRMODE5							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
45	DRR::DRMODE5							
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	(RSV)	(RSV)	(RSV)	(RSV)
46	DRR::CMD0A							
	CMD A SLRC CHK	(RSV)	(RSV)	CMD A SP MODE	CMD A DIAG MODE	(RSV)	(RSV)	(RSV)
47	DRR::CMD0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
48	DRR::ADR0A							
	CMD A Slave 1 Cache Transfer Address (BYTE0)							
49	DRR::ADR0A							
	CMD A Slave 2 Cache Transfer Address (BYTE0)							
4A	DRR::ADR1A							
	CMD A Slave 1 Cache Transfer Address (BYTE1)							
4B	DRR::ADR3A							
	CMD A Slave 2 Cache Transfer Address (BYTE1)							
4C	DRR::TRMDA							
	CMD A SYND CHK	(RSV)	CMD A MRCF FUNCTION	CMD A DOUBLE WT MODE	CMD A Transfer Command			
4D	DRR::TRMDA							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
4E	DRR::LA0A							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
4F	DRR::LA0A							
	CMD A Expect LA Value (BYTE0)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(3) Byte28 = 12, 14, B2 (2/4)

	0	1	2	3	4	5	6	7
50	DRR::LA1A							
	CMD A Expect LA Value (BYTE1)							
51	DRR::LA1A							
	CMD A Expect LA Value (BYTE2)							
52	DRR::LA2A							
	CMD A Expect LA Value (BYTE3)							
53	DRR::LA2A							
	CMD A Expect LA Value (BYTE4)							
54	DRR::CMD0B							
	CMD B SLRC CHK	(RSV)	(RSV)	CMD B SP MODE	CMD B DIAG MODE	(RSV)	(RSV)	(RSV)
55	DRR::CMD0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
56	DRR::ADR0B							
	CMD B Slave 1 Cache Transfer Address (BYTE0)							
57	DRR::ADR0B							
	CMD B Slave 2 Cache Transfer Address (BYTE0)							
58	DRR::ADR1B							
	CMD B Slave 1 Cache Transfer Address (BYTE1)							
59	DRR::ADR3B							
	CMD B Slave 2 Cache Transfer Address (BYTE1)							
5A	DRR::TRMDB							
	CMD B SYND CHK	(RSV)	CMD B MRCF FUNCTION	CMD B DOUBLE WT MODE	CMD B Transfer Command			
5B	DRR::TRMDB							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
5C	DRR::LA0B							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
5D	DRR::LA0B							
	CMD B Expect LA Value (BYTE0)							
5E	DRR::LA1B							
	CMD B Expect LA Value (BYTE1)							
5F	DRR::LA1B							
	CMD B Expect LA Value (BYTE2)							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail

(3) Byte28 = 12, 14, B2 (3/4)

	0	1	2	3	4	5	6	7
60	DRR::LA2B							
	CMD B Expect LA Value (BYTE3)							
61	DRR::LA2B							
	CMD B Expect LA Value (BYTE4)							
62	DRR::RLALR0							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
63	DRR::RLALR0							
	LA Value When LA ERR Occurred (BYTE0)							
64	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE1)							
65	DRR::RLALR1							
	LA Value When LA ERR Occurred (BYTE2)							
66	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE3)							
67	DRR::RLALR2							
	LA Value When LA ERR Occurred (BYTE4)							
68	DRR::D64CNTM							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Command Pointer(High)	
69	DRR::D64CNTM							
	Command Pointer(Low)							
6A	DRR::DRST10							
	CHSN STATUS0 BYTE0							
6B	DRR::DRST10							
	CHSN STATUS0 BYTE1							
6C	DRR::DRST11							
	CHSN STATUS0 BYTE1 (SUB)							
6D	DRR::DRST11							
	CHSN STATUS0 BYTE0 (SYB)							
6E	DRR::DRST20							
	CHSN STATUS1 BYTE0							
6F	DRR::DRST20							
	CHSN STATUS1 BYTE1							

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Byte27 = 8B (DRR CHK2) Byte40-7F Detail
(3) Byte28 = 12, 14, B2 (4/4)

	0	1	2	3	4	5	6	7
70		DRR::DRST21						
		CHSN STATUS1 BYTE1 (SUB)						
71		DRR::DRST21						
		CHSN STATUS1 BYTE0 (SUB)						
72		DRR::DRESTA5						
	STS1 DT0 PARITY ERR	STS1 DT1 PARITY ERR	STS1 DT2 PARITY ERR	STS1 DT3 PARITY ERR	STS1 DT4 PARITY ERR	STS1 DT5 PARITY ERR	STS1 DT6 PARITY ERR	STS1 DT7 PARITY ERR
73		DRR::DRESTA6						
	P0 TXX I-DT0	P0 TXX I-DT1	P0 TXX O-DT0	P0 TXX O-DT1	P1 TXX I-DT0	P1 TXX I-DT1	P1 TXX O-DT0	P1 TXX O-DT1
74		DRR::DRESTA7						
	P1 TX DT0 PARITY ERR	P1 TX DT1 PARITY ERR	P1 TX DT2 PARITY ERR	P1 TX DT3 PARITY ERR	P1 TX DT4 PARITY ERR	P1 TX DT5 PARITY ERR	P1 TX DT6 PARITY ERR	P1 TX DT7 PARITY ERR
75		DRR::DRESTA7						
	P1 RX DT0 PARITY ERR	P1 RX DT1 PARITY ERR	P1 RX DT2 PARITY ERR	P1 RX DT3 PARITY ERR	P1 RX DT4 PARITY ERR	P1 RX DT5 PARITY ERR	P1 RX DT6 PARITY ERR	P1 RX DT7 PARITY ERR
76		DRR::DRESTAC						
	P1 AC PLRC ERR	P1 DT PLRC ERR	P1 STS0 PLRC ERR	P1 STS0 PLRC ERR	P1 AC INV-PLRC ERR	P1 DT INV-PLRC ERR	P1 STS0 INV-PLRC ERR	P1 STS1 INV-PLRC ERR
77		DRR::DRESTAC						
	P1 AC END-CODE ERR	P1 DT END-CODE ERR	P1 STS0 END-CODE ERR	P1 STS1 END-CODE ERR	P1 SLRC CHECK ERR	P1 SLRC CAL DT ERR	P1 SLRC RD DT ERR	P1 SBLK DCNT ERR
78		Micro Information						
		List Number Expect to Execute						
79		Micro Information						
		List Number Expect to Execute						
7A		Micro Information						
		List Number Executed						
7B		Micro Information						
		List Number Executed						
7C		Micro Information						
		Job Restart Bits						
7D		Micro Information						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
7E		Micro Information						
		Error Devided Result Code						
7F		Micro Information						
		CHK2 Detected Counter (Low)						

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Byte27 = 8C (SVP Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘C’)			
28								
29	Error information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30	Error type code (Note 1)							
31								
32								
33	Error information (See following pages)							
34								
35								
36	Symptom code (x‘FF8C’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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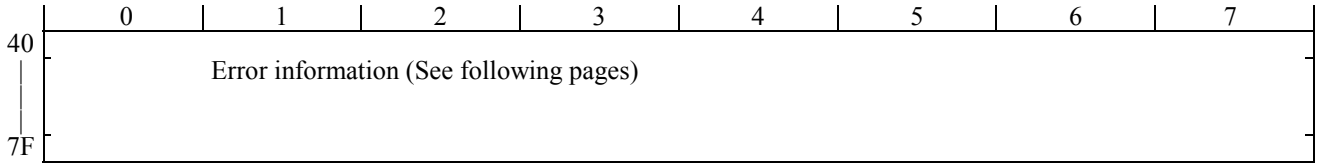
Byte27 = 8C (SVP Failure) (2/2)



(Note 1) Error type code

x‘0000’ : Logical inconsistency
x‘0001’ : HEAP related error
x‘0002’ : File related error
x‘0003’ : LAN failure
x‘0004’ : SSVP failure
x‘0005’ : Windows failure
x‘0006’ : CUDG detected error
x‘0009’ : BOOT detected error
x‘000A’ : SVP message

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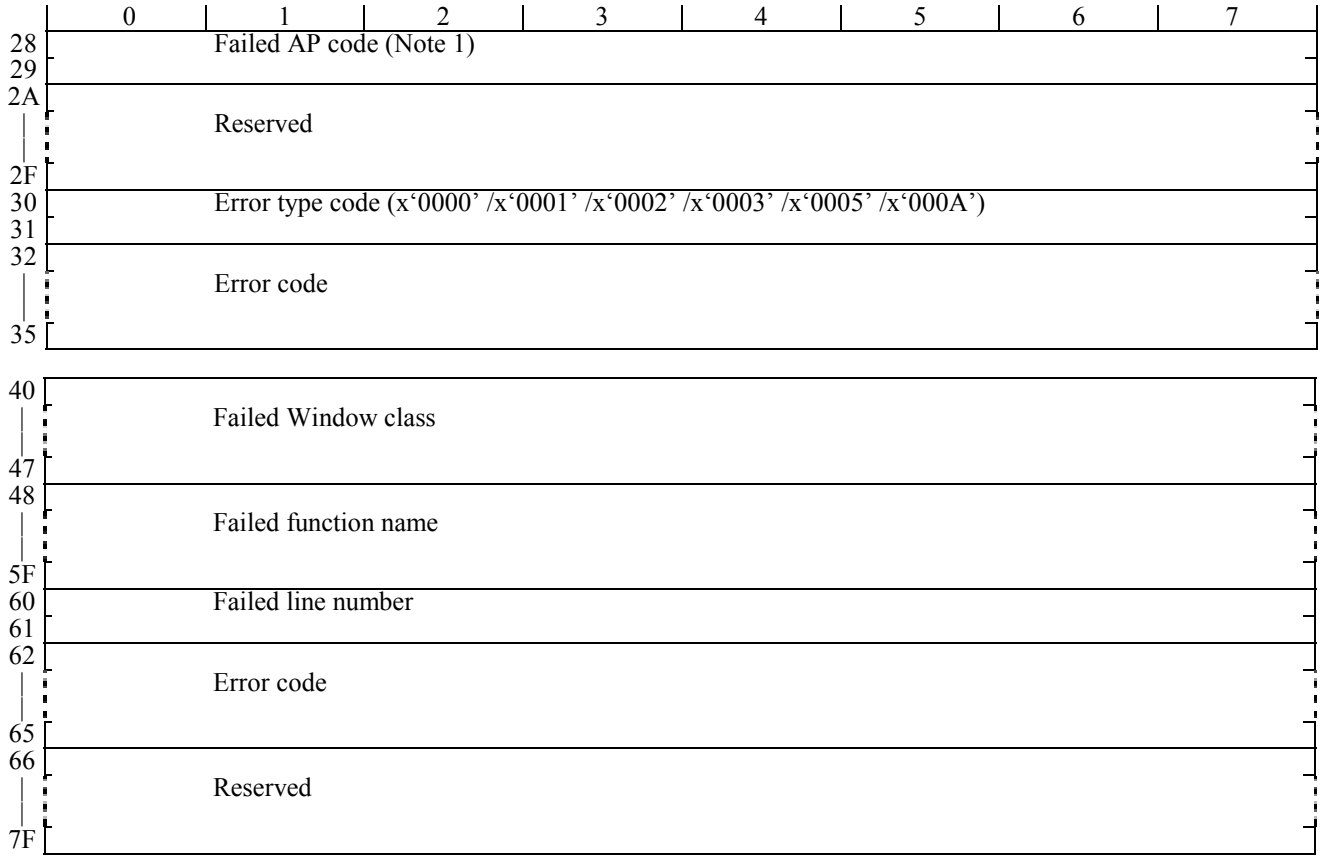
Byte27 = 8 C (SVP Failure) Byte28-35,40-7F detail

(1) Logical inconsistency / HEEP/File/LAN/Windows failure/SVP message



(Note 1) Failed AP code

x‘0000’ : Dump task
x‘0001’ : DKU inline
x‘0002’ : Microprogram change (online)
x‘0003’ : Information
x‘0004’ : LOGOUT
x‘0005’ : PATH inline
x‘0006’ : Back ground
x‘0007’ : DIAG
x‘0008’ : Install
x‘0009’ : On-line
x‘000A’ : Micro-program change (off-line)
x‘000B’ : Special package change
x‘000C’ : Common function for communication
x‘00FF’ : Others

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Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(2) SSVP failure

	0	1	2	3	4	5	6	7
28	Failed AP code (x‘000C’)							
29								
2A	Reserved							
2F								
30	Error type code (x‘0004’)							
31								
32	Reserved							
33								
34	SSVP Error code							
35								
40	SSVP IMPL Sequence							
41	Detect Code							
42	Part Code							
43								
44	SSVP Error							
45								
46	Detail Information							
4F								
50	Reserved							
57								
58	Reserved							
7F								

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Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(3) CUDG detected error

	0	1	2	3	4	5	6	7
28 29 2A 2B 2C 2D 2E 2F	‘CUDG ERR’ (x‘43 55 44 47 20 45 52 52’)							
30 31	Error type code (x‘0006’)							
32 33 34 35	Error code (x‘00000000’)							

40	Error occurred time (year)
41	Error occurred time (month)
42	Error occurred time (day)
43	Error occurred time (hour)
44	Error occurred time (minute)
45	Error occurred time (second)
46	Report MPID
47	Test object
48	Test type (x‘01’ : CUDG3, x‘10’ : LCDG3/FCDG3/PCDG3)
49	Failed LCP number
4A	Test contents
4B	Test contents
4C	Error code
4D	Error code
4E	Not used
4F	Not used
50	Cache module group number (slave 1)
51	Cache module group number (slave 1)
52	Cache module group number (slave 1)
53	Cache module group number (slave 1)
54	Cache module group number (slave 2)
55	Cache module group number (slave 2)
56	Cache module group number (slave 2)
57	Cache module group number (slave 2)
58	PCB location (main platter)
59	PCB location (main platter)
5A	PCB location (main platter)
5B	PCB location (cache platter 1)
5C	PCB location (cache platter 1)
5D	PCB location (cache platter 2)
5E	PCB location (cache platter 2)
5F	Run option
60 ⋮ 7F	Additional information (Note 1)

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Byte27 = 8C (SVP Failure) Byte28-35, 40-7F detail

(Note 1) Additional information (for LCDG3/FCDG3/PCDG3 only)

	0	1	2	3	4	5	6	7
60	Reserved							
61								
62								
63								
64	Record type (x‘0F’ : LCP IMPL diagnostic, x‘10’ : HTP IMPL diagnostic, x‘20’ : PCDG)							
65	Reserved							
66	MP ID (of CHP : x‘10’~x‘17’)							
67	LCP ID (LCP#A : x‘80’~LCP#H : x‘01’)							
68	Error code (Note 2)							
69	Process type (Note 3)							
6A	Error status 1 (Record type = x‘0F’ (Note 4), x‘10’ (Note 6), x‘20’ (Note 7))							
6B								
6C	Error status 2 (Note 5)							
6D								
6E								
6F								
70								
71								
72								
73								
74	Reserved							
|								
7F								

(Note 2) Error code

Code	Meaning	Function	Remarks
0A	LCDG3’/FCDG3’ load error	LCDG3’/FCDG3’	Make status in loading process
10	Memory clear and test error	LCDG3’/FCDG3’	Set LCP address into error status 1
18	LCDG3/FCDG3/PCDG3 MP detected error	LCDG3/FCDG3/ PCDG3	Detail information in error status 1 and 2
1A	LCDG3/FCDG3 load error	LCDG3/FCDG3	Make status in loading process
1F	LCDG3’ error before LCP loading	Main loading	LCDG 3 information in status
20	SCAN detected error	All	MP detected error
2A	LCP main load error	Main loading	Make status in loading process
30	LCP detected error	LCDG3’	Detail information in error status 1 and 2
| FF		LCDG3	

(Note 3) Process type

Code	Process	Remarks
01	LCDG3’/FCDG3’	Set loading error status when a loading error occurred.
02	LCDG3/FCDG3/ PCDG3	Set loading error status when a loading error occurred.
03	Loading	

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Byte27 = 8C (SVP Failure) Byte 28-35,40-7F detail

(Note 4) Error status 1

Code	Meaning
0101	LCDG3' activation failed.
010F	LCP terminated after LCDG3' activation.
0118	No notification after LCDG3' communication.
011F	LCP CHK1 occurred after LCDG3' activation.
0120	No REQM after LCDG3' completion.
0122	No notification after LCDG3' set CALM.
0123	No notification after LCDG3' set DGIN.
0125	LCP# ≠ Board#
0301	CRC check start error after loading.
030F	LCP terminated after CRC check completion.
0318	No notification for communication after CRC check completion.
031F	CHK1 occurred in CRC check.
0320	No REQM after CRC check completion.
0322	No notification after CRC check and CALM completion.
0323	No notification after CRC check and DGIN completion.
0325	LCP# ≠ Board#
032F	No CRC check status ID.
0340	CRC check error in LCDG3 loading/Main loading.
0380	No start address for CRC check routine.
0385	An error occurred in configuration/version information transfer for Main loading.
0401	LCDG3 activation for internal diagnosis failed.
040F	LCP terminated after LCDG3' activation.
0418	No notification after communication for internal diagnosis.
041F	LCP CHK1 occurred after internal diagnosis activation.
0420	No REQM after internal diagnosis completion.
0422	No notification after internal diagnosis and CALM.
0423	No notification after internal diagnosis and DGIN.
0425	LCP# ≠ Board#
042F	No status ID for internal diagnosis effect.
043F	No parameter ID for internal diagnosis activation.
044F	No activation address ID for internal diagnosis.
04F0	Controller in configuration is inconsistent with rea1 machine.
04F1	Controller in configuration is inconsistent with rea1 machine.
0501	LCDG3 activation for communication diagnosis failed.
050F	LCP terminated after LCDG3' activation.
0518	No notification after communication for communication diagnosis.
051F	LCP CHK1 occurred after communication diagnosis activation.
0520	No REQM after communication diagnosis completion.
0522	No notification after communication diagnosis and CALM.
0523	No notification after communication diagnosis and DGIN.
0525	LCP# ≠ Board#
052F	No effect status ID for communication diagnosis.
053F	No activation parameter ID for communication diagnosis.
054F	No activation address ID for communication diagnosis.
1000-FFFF	An error address of memory clear test (when error code = x'10')
1000-FFFF	LCDG3 error code for internal/communication diagnosis (when error code ≥ x'30')
XXXX	MP error code for LCDG3 communication diagnosis (when error code = x'18')

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(Note 5) Error status 2

(1) When process type = x‘01’ and error code ≥ x‘30’ and error status 1 ≥ x‘1000’, LCP error code for LCDG3’.
(2) When process type = x‘02’ and error code ≥ x‘30’ and error status 1 ≥ x‘1000’), LCP error code for LCDG3.
(3) When process type = x‘02’ and error code = x‘18’,
    Byte 6C-6D : Error register address
    Byte 6E-6F : Active register value.
    Byte 70-71 : Expected register value
    Byte 72-73 : Return sequence
(4) When other case, this value is invalid.

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(Note 6) Error status 1 (Record type (Byte 64) = x‘10’ :FCDG3)

Code	Meaning
0101	FCDG3’ Waiting for end of diagnosis timeout
0102	FCDG3’ SVC I/F error
0103	FCDG3’ ASTS Initialization Error
0104	FCDG3’ Invalid Parameter(s) Received
0105	FCDG3’ CHK1B Detected
0110	FCDG3’ Failure detected in preliminary diagnosis
0111	FCDG3’ Failure detected in Memory diagnosis (Fixed pattern)
0112	FCDG3’ Failure detected in Memory diagnosis (Sequential access)
0113	FCDG3’ Failure detected in Memory diagnosis (Byte increment data)
0114	FCDG3’ Failure detected in CS access diagnosis
08xx	FCDG3 HTP Processor Diagnosis
09xx	FCDG3 HTP → CHP Transfer diagnosis (Pointer Addressing Area)
0Axx	FCDG3 HTP → CHP Transfer diagnosis (Direct Addressing COMM Area)
0Bxx	FCDG3 HTP → CHP Transfer diagnosis (Direct Addressing DXBF Area)
0Cxx	FCDG3 CHP → HTP Transfer diagnosis
0Dxx	FCDG3 Hot Line Communication diagnosis
0Exx	FCDG3 IntReq diagnosis
0Fxx	FCDG3 Info Transmission diagnosis
10xx	FCDG3 Signal Diagnosis
11xx	FCDG3 Transfer diagnosis
12xx	FCDG3 Link Diagnosis/LSI Rev. Check
13xx	FCDG3 Synchronized Transfer diagnosis

xx: 01 ASTS Initialization Error
02 MPCK Detected
03 HTP Illegal Access Detected
10 SVC I/F Error
20 Time-out
21 Frame transmission time-out
22 Frame reception time-out
23 DXBF Access Time-out
24 XFS Time-out
25 PXSTS Time-out
30 CHK1B Detected
31 CHK2 Detected
32 CHK2E Detected
40 Compare Error
50 MMC Status Error
51 XFS Status Error
52 HTPSTS Status Error
53 ONLSTS Status Error
60 Frame transmission Error
61 Burst transmission Error
70 Invalid Parameter(s) Received

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(Note 7) Error status 1 (Record type = x‘20’ : PCDG3)

Code	Meaning
20xx	Micro Code Load Process (into Pentium)
21xx	Communication Memory Diagnosis
22xx	Door Bell Diagnosis
23xx	Direct Mapping Area Memory Diagnosis
24xx	DMA Diagnosis
25xx	NIC Diagnosis
26xx	Full Memory Access Diagnosis
27xx	(Reserved)
28xx	Memory Access Diagnosis
29xx	Loop Back Diagnosis (PCDG3 Not Supported)

xx: 01 Aborted Error in Pentium
10 ECC Error
20 Time-out
21 Time-out in Door Bell Send
22 Time-out in Door Bell Received
23 Door Bell Clear Error
30 CHK1B Detected
31 CHK2 Detected
32 CHK2E Detected
40 Compare Error
60 Data Transmit Error
61 Data Transmit/Receive Time-out
62 Illegal Parameter(s) Detected in Data Transmit
70 Illegal parameter(s) Detected (I/F Error)
71 Illegal parameter(s) Detected (Pentium Reported)
81 NIC : Data Parity Error
82 NIC : Parity Error
83 NIC : System Error
84 NIC : Aborted Error
85 NIC : Target Abort Error
8F NIC : etc.

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Byte27 = 8C (SVP Failure) Byte28-35,40-7F detail

(4) BOOT detected error

	0	1	2	3	4	5	6	7
28 29 2A 2B 2C 2D 2E 2F	‘BOOT ERR’ (x‘42 4F 4F 54 20 45 52 52’)							
30 31	Error type code (x‘0009’)							
32 33 34 35	Error code (x‘0000X000’ X:Processor number)							
40 | 4F	Error detection point							
50 51 52 53	Reserved							
54 55 56 57	Error code for loading error							
58 59 5A 5B	Error code of internal interface							
5C 5D 5E 5F	Error code of initialization function (Note 1)							
60 | 7F	Reserved							

(Note 1) Error code of initialization function.

x‘31000041’ : Forcible start with jumper pin.

x‘40000041’ : Load module ID in FM is incorrect.
(FM writing was failed or load module is incorrect)

x‘42000041’ : Sum check error of FM.
(Failure occurred at FM writing or input/output error of FM occurred)

x‘48000041’ : This MP has the micro-programs which type is different from the PCB name.
(In the MP-Install procedure, the package may have been set which type is different from one that is specified in the define configuration.)

x‘56000041’ : Sum check error of the load module.
(SVP Failure occurred)

Others : Loading for the load module impossible.
(The load module was incorrect)

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Byte27 = 8D (Power Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x‘8’)				Message (x‘D’)			
28								
29	Hardware information (See following pages)							
2A								
2B								
2C								
2D								
2E								
2F								
30								
31								
32	Not used							
33								
34	PCB							
35	SSID of self subsystem (low order)							
36	Symptom code (x‘FF8D’ : LDEV type = DKU87I/x‘EF8D’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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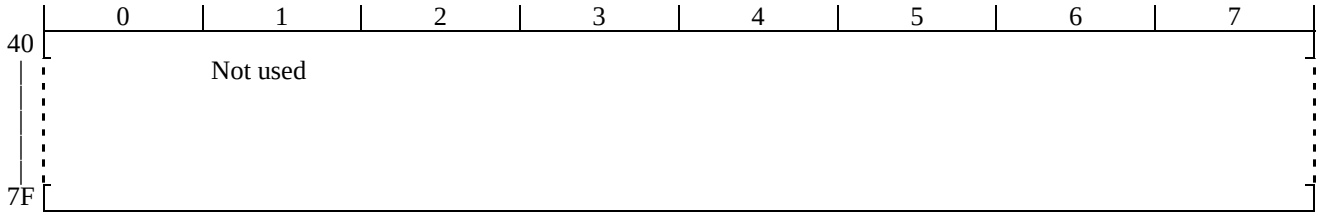
Byte27 = 8D (Power Failure) (2/2)



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Byte27 = 8D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x‘80’ : DKA detected DKU/HDU Power Failure							
29	Failure detected PDEV							
	0x10 ~ 0x1F: Detected RDEV# 0xFF: Detected by self-check							
2A	DKU Power Status							
	FSW#7 STATUS	FSW#6 STATUS	FSW#5 STATUS	FSW#4 STATUS	FSW#3 STATUS	FSW#2 STATUS	FSW#1 STATUS	FSW#0 STATUS
2B	Micro Information							
	SM control area information							
2C	Micro Information							
	SM control area information							
2D	Micro Information							
	SM control area information							
2E	Micro Information							
	SM control area information							
2F	Blocked HDU Bit Map							
	1st DKU				2nd DKU			
30	Blocked HDU Bit Map							
	3rd DKU				(RSV)	(RSV)	(RSV)	(RSV)
31	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)

(*) BYTE32 ~ 7F : Not Used

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Byte27 = 8D (DKU/HDU Power Failure) Hard information

	0	1	2	3	4	5	6	7
28	Subcode : x‘90’ : DKA detected DKU/HDU Power Failure Recover							
29	Failure detected PDEV							
2A	DKU Power Status							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2B	PDEV Power Status (SPC Pass#0, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2C	PDEV Power Status (SPC Pass#1, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2D	PDEV Powr Status (SPC Pass#1, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
2E	PDEV Power Status (SPC Pass#2,basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
2F	PDEV Power Status (SPC Pass#2, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)
30	PDEV Power Status (SPC Pass#3, basic DKU box)							
	PDEV (id# x‘F’)	PDEV (id# x‘E’)	PDEV (id# x‘D’)	PDEV (id# x‘C’)	PDEV (id# x‘B’)	PDEV (id# x‘A’)	PDEV (id# x‘9’)	PDEV (id# x‘8’)
31	PDEV Power Status (SPC Pass#3, extent DKU box)							
	PDEV (id# x‘7’)	PDEV (id# x‘6’)	PDEV (id# x‘5’)	PDEV (id# x‘4’)	PDEV (id# x‘3’)	PDEV (id# x‘2’)	PDEV (id# x‘1’)	PDEV (id# x‘0’)

(*) BYTE32 ~ 7F : Not Used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Note : Failed processor number for WCHK1

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Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'00'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::C1WSTS							
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at RMC	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
43	RMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
44	RMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	RMC::CHK1ASTS							
	Data CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	RMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer Hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
47	RMC::CHK1ASTS							
	MPU uncorrectable error	MPU fetch uncorrectable error	MPU write protect	MPU out of area	Not used	Not used	Other write protect	Other out of area
48	RMC::ERADR							
	Address from L bus							
49	RMC::ERADR							
	Address from L bus							
4A	RMC::ERADR							
	Address from L bus							
4B	RMC::ERADR							
	Address from L bus						Not used	Not used
4C	RMC::ERORD							
	Data before correction							
4D	RMC::ERORD							
	Data before correction							
4E	RMC::ERORD							
	Data before correction							
4F	RMC::ERORD							
	Data before correction							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) (3/5)

	0	1	2	3	4	5	6	7
50	RMC::ERORC							
	Check bit before correction							
51	RMC::ERORC							
	Check bit before correction							
52	RMC::ERRSYD							
	Syndrome before correction							
53	RMC::ERRSYD							
	Syndrome before correction							
54	RMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	WR signal Reg	WR signal value
55	RMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
56	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
57	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
58	MMC: LAST1IP							
	Last address before CHK1A occurred							
59	MMC: LAST1IP							
	Last address before CHK1A occurred							
5A	MMC: LAST1IP							
	Last address before CHK1A occurred							
5B	MMC: LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used
5C	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5D	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5E	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5F	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) (4/5)

	0	1	2	3	4	5	6	7
60	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
61	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
62	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
63	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
64	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
65	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
66	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
67	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
68	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
69	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6A	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6B	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	WR/RD flag in CHK1B	Not used
6C	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6D	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6E	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6F	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	WR/RD flag in CHK1B	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 20/30 (CHK1A) (5/5)

	0	1	2	3	4	5	6	7
70		MMC::CECNT						
		Correctable error counter (for upper address bank)						
71		MMC::CECNT						
		Correctable error counter (for upper address bank)						
72		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
73		MMC::CHK1BSTS						
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
74		Not used						
75		RMC::DRAMC1BSTS						
	MPU Correctable errors	MPU fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
76		RMC::DRAMC1BSTS						
	Other Correctable errors	Not used	Other access Uncorrectable error detected	Not used	Other incorrect address	Not used	Not used	Not used
77		RMC::DRAMC1BSTS						
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
78		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
79		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
7A		MMC::MICCHK1STS						
	Not used	Not used	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7B		MMC::MICCHK1STS						
	Not used	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error
7C		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7D		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7E		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7F		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B

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Format 8, Message E (processor failure: CHK1A)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘20’: DRAM hard error							
2A	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1 occurred	CHK1B occurred	CHK1A occurred
2B	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at RMC	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2C	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2D	MMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MMC::CHK1ASTS							
	DATA CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	IB WP ERR
2F	MMC::CHK1ASTS							
	IB RP ERR	IB HIT ERR	IB WTBL ERR	IB CNL ERR	MEM SEQ ERR	MEM INIT ERR	Not used	MEM ADR ERR
30	MMC::CHK1ASTS							
	MPU UNCER	MMC FETCH UNCER	MPU WR PROT	MPU ADR OVER	Not used	Not used	OTHER WR PROT	OTHER ADR OVER
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Format 8, Message E (processor failure: CHK1A)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘30’: DRAM CHK1A micro error							
2A	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1 occurred	CHK1B occurred	CHK1A occurred
2B	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at RMC	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2C	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2D	MMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MMC::CHK1ASTS							
	DATA CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	IB WP ERR
2F	MMC::CHK1ASTS							
	IB RP ERR	IB HIT ERR	IB WTBL ERR	IB CNL ERR	MEM SEQ ERR	MEM INIT ERR	Not used	MEM ADR ERR
30	MMC::CHK1ASTS							
	MPU UNCER	MMC FETCH UNCER	MPU WR PROT	MPU ADR OVER	Not used	Not used	OTHER WR PROT	OTHER ADR OVER
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Note : Failed processor number for WCHK1

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Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'01'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::C1WSTS							
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at RMC	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
43	RMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
44	RMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	RMC::CHK1ASTS							
	Data CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	RMC::CHK1ASTS							
	Fetch buffer read pointer error	Fetch buffer Hit error	Fetch buffer buffer size error	Fetch buffer buffer size error	SDRAM sequencer error	SDRAM initialize sequence error	Read word counter error	Read word counter error
47	RMC::CHK1ASTS							
	MPU uncorrectable error	MPU fetch uncorrectable error	MPU write protect	MPU out of area	Not used	Not used	Other write protect	Other out of area
48	RMC::FERADR							
	Address from L bus (fetch)							
49	RMC::ERADR							
	Address from L bus (fetch)							
4A	RMC::ERADR							
	Address from L bus (fetch)							
4B	RMC::ERADR							
	Address from L bus (fetch)						Not used	Not used
4C	RMC::FERORD							
	Data before correction (fetch)							
4D	RMC::FERORD							
	Data before correction (fetch)							
4E	RMC::FERORD							
	Data before correction (fetch)							
4F	RMC::FERORD							
	Data before correction (fetch)							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) (3/5)

	0	1	2	3	4	5	6	7
50	RMC::FERORC							
	Check bit before correction (fetch)							
51	RMC::FERORC							
	Check bit before correction (fetch)							
52	RMC::FERRSYD							
	Syndrome before correction (fetch)							
53	RMC::FERRSYD							
	Syndrome before correction (fetch)							
54	RMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	WR signal Reg	WR signal value
55	RMC::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	LM, XR Access error in scanning	DRAM control signal error	Not used
56	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
57	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
58	MMC: LAST1IP							
	Last address before CHK1A occurred							
59	MMC: LAST1IP							
	Last address before CHK1A occurred							
5A	MMC: LAST1IP							
	Last address before CHK1A occurred							
5B	MMC: LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used
5C	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5D	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5E	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
5F	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) (4/5)

	0	1	2	3	4	5	6	7
60	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
61	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
62	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
63	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
64	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
65	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
66	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
67	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
68	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
69	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6A	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred							
6B	MMC:: LAST1							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	WR/RD flag in CHK1B	Not used
6C	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6D	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6E	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred							
6F	MMC::LAST2							
	Execution address one generation older than the last one before CHK1A occurred				Not used	Not used	WR/RD flag in CHK1B	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 31 (CHK1A) (5/5)

	0	1	2	3	4	5	6	7
70		MMC::CECNT						
		Correctable error counter (for upper address bank)						
71		MMC::CECNT						
		Correctable error counter (for upper address bank)						
72		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
73		MMC::CHK1BSTS						
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
74		Not used						
75		RMC::DRAMC1BSTS						
	MPU Correctable errors	MPU fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
76		RMC::DRAMC1BSTS						
	Other Correctable errors	Not used	Other access Uncorrectable error detected	Not used	Other incorrect address	Not used	Not used	Not used
77		RMC::DRAMC1BSTS						
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
78		MMC::MPCERRSTS						
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
79		MMC::MICCHK1STS						
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
7A		MMC::MICCHK1STS						
	Not used	Not used	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7B		MMC::MICCHK1STS						
	Not used	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error
7C		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7D		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7E		MMC::CHK1BADRS						
		Address when CHK1B occurred						
7F		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B

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Format 8, Message E (processor failure: CHK1A)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'32': FETCH UNCORRECTABLE error							
2A	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1 occurred	CHK1B occurred	CHK1A occurred
2B	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at RMC	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2C	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2D	MMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MMC::CHK1ASTS							
	DATA CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	IB WP ERR
2F	MMC::CHK1ASTS							
	IB RP ERR	IB HIT ERR	IB WTBL ERR	IB CNL ERR	MEM SEQ ERR	MEM INIT ERR	Not used	MEM ADR ERR
30	MMC::CHK1ASTS							
	MPU UNCER	MMC FETCH UNCER	MPU WR PROT	MPU ADR OVER	Not used	Not used	OTHER WR PROT	OTHER ADR OVER
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

Note : Failed processor number for WCHK1

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Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’02’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::C1WSTS							
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at RMC	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
43	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
44	RMC::MPIFERR							
	ECC UNC B0	ECC ENC B1	ECC UNC B2	ECC ENC B3	CMDPE B0	CMDPE B1	CMDPE B2	CMDPE B3
45	RMC::MPIFERR							
	STATUSPE	Not used	Not used	Not used	Not used	Not used	Not used	Not used
46	RMC::MPIFERR							
	OUTDT UNCOR	Not used	Not used	Not used	Not used	Not used	Not used	Not used
47	Not used							
48	RMC::MPSHDERR1							
	CMD OVRUN	INBUF SEQ error	INCNT error	OUTCNT error	ECC error B0	ECC error B1	ECC error B2	ECC error B3
49	RMC::MPSHDERR1							
	ACMPEV error	ACMPNO SEL	XRAW BCPE	XRDW BCPE	LMAW BCPE	LMDW BCPE	IBAW BCPE	IBDW BCPE
4A	RMC::MPSHDERR1							
	IRBFC CMDPE	IRBFC EXADRPE	IRBFC ADRPE	Not used	XRBFC CMDPE	XRBFC EXADRPE	XRBFC ADRPE	Not used
4B	RMC::MPSHDERR1							
	LMBFC CMDPE	LMBFC EXADRPE	LMBFC ADRPE	Not used	IBBFC CMDPE	IBBFC EXADRPE	IBBFC ADRPE	Not used
4C	RMC::MPSHDERR2							
	IRBFC ADCPE	IRBFC ARCPE	IRBFC AWCPE	IRBFC DDCPE	IRBFC DRCPE	IRBFC DWCPE	IRBFC SEQ error	IRBFC SEQPE
4D	RMC::MPSHDERR2							
	XRBFC ADCPE	XRBFC ARCPE	XRBFC AWCPE	XRBFC ASEQPE	XRBFC DDCPE	XRBFC DRCPE	XRBFC DWCPE	XRBFC DSEQPE
4E	RMC::MPSHDERR2							
	LMBFC ADCPE	LMBFC ARCPE	LMBFC AWCPE	LMBFC ASEQPE	LMBFC DDCPE	LMBFC DRCPE	LMBFC DW CPE	LMBFC DSEQPE
4F	RMC::MPSHDERR2							
	IBBFC ADCPE	IBBFC ARCPE	IBBFC AWCPE	IBBFC ASEQPE	IBBFC DDCPE	IBBFC DRCPE	IBBFC DWCPE	IBBFC DSEQPE

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Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) (3/5)

	0	1	2	3	4	5	6	7
50	RMC::MPMHDERR							
	DTC UMATCH	DTC OVER	DTC PE	OBWC SEQ error	DM SEQPE	CM SEQPE	EREG SEQPE	OUTDT ERR
51	RMC::MPMHDERR							
	OBC WCPE	OBC ECPE	OBC DCPE	Not used	OBD WCPE	OBD ECPE	OBD DCPE	BLKCPE
52	RMC::MPMHDERR							
	CMDPE	OBC2 CPE	OBD2 CPE	LASTDTER	OBC CMDPE	CMDPE2	REQNO RST error	RECNO SET error
53	RMC::IRCHDERR							
	CMDPE	ADRPE	IR MSEQPE	IR SSEPQE	RMWSEQPE	Not used	DMA SEQPE	IMADPE
54	RMC::XRCHDERR1							
	WBC ADCPE	WBC ARCPE	WBCA WCPE	WBC DDCPE	WBC DRCPE	WBC DWCPE	WBC CMDOVR	WBC SEQER
55	RMC::XRCHDERR1							
	WBC SEQER	WBC DTOVR	Not used	Not used	ADRPE	CMDPE	EXAPE	Not used
56	RMC::XRCHDERR1							
	XRRBC ADCPE	XRRBC ARCPE	XRRBC AWCPE	XRRBC DDCPE	XRRBC DRCPE	XRRBC DWCPE	XRRBC SEQPE	Not used
57	RMC::XRCHDERR1							
	RDCMDPE	BFOVRD	BFOVWR	RDBUF CNTPE	Not used	Not used	Not used	Not used
58	RMC::XRCHDER2							
	XRADRPE	XPCMDPE	ADRCNTPE	Not used	Not used	Not used	Not used	DTPCNTPE
59	RMC::XRCHDER2							
	XRSEQER	WADCNTPE	WDDCNTPE	RADCNTPE	RDDCNTPE	XDACNTPE	BCNTPE	LCNTPE
5A	RMC::XRCHDER2							
	SLV CNTOV	SLV CNTUMT	SLV CNTER	SLV SEQER	Not used	Not used	Not used	Not used
5B	RMC::LMCHDERR1							
	WBC ADCPE	WBC ARCPE	WBC AWCPE	WBC DDCPE	WBC DRCPE	WBC DWCPE	WBC CMDOVR	BLKCPE
5C	RMC::LMCHDERR1							
	WBC SEQPE	WBC DTOVR	Not used	Not used	ADRPE	CMDPE	Not used	Not used
5D	RMC::LMCHDERR1							
	XRRBC ADCPE	XRRBC ARCPE	XRRBC AWCPE	XRRBC DDCPE	XRRBC DRCPE	XRRBC DWCPE	XRRBC SEQPE	XRRBC CMDLTE
5E	RMC::LMCHDERR1							
	RDCCMDPE	Not used	Not used	Not used	Not used	Not used	Not used	BLKCPE
5F	RMC::LMCHDERR2							
	LMCS ADRPE	LMCS CMDPE	LMCS ACNTPE	LMCS PCNTPE	Not used	LMCS SEQPE	LMCS PFERR	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) (4/5)

	0	1	2	3	4	5	6	7
60	MMC: LAST1IP							
	Last address before CHK1A occurred							
61	MMC: LAST1IP							
	Last address before CHK1A occurred							
62	MMC: LAST1IP							
	Last address before CHK1A occurred							
63	MMC: LAST1IP							
	Last address before CHK1A occurred				Not used	Not used	Not used	Not used
64	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
65	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
66	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred							
67	MMC: LAST2IP							
	Address one generation older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
68	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
69	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
6A	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred							
6B	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used
6C	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
6D	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
6E	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred							
6F	MMC:: LAST4IP							
	Address three generations older than the last one before CHK1A occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 21 (CHK1A) (5/5)

	0	1	2	3	4	5	6	7
70	RMC::ERREGADR							
	Reg address when CHK1A occurred							
71	RMC::ERREGADR							
	Reg address when CHK1A occurred							
72	RMC::ERREGADR							
	Reg address when CHK1A occurred							
73	RMC::ERREGADR							
	Reg address when CHK1A occurred						Not used	Not used
74	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
75	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
76	RMC::DRAMC1BSTS							
	MPU Correctable errors	MPU fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
77	RMC::DRAMC1BSTS							
	Other Correctable errors	Not used	Other access Uncorrectable error detected	Not used	Other incorrect address	Not used	Not used	Not used
78	RMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
79	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
7A	MMC::MICCHK1STS							
	Not used	Not used	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7B	MMC::MICCHK1STS							
	Not used	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error
7C	MMC::CHK1BADRS							
	Address when CHK1B occurred							
7D	MMC::CHK1BADRS							
	Address when CHK1B occurred							
7E	MMC::CHK1BADRS							
	Address when CHK1B occurred							
7F	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B

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Format 8, Message E (processor failure: CHK1A)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘21’: RMC CHK1A error							
2A	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1 occurred	CHK1B occurred	CHK1A occurred
2B	MMC::C1WSTS							
	CHK1A occurred	WCHK1 occurred	CHK1A occurred in MPCHK	CHK1A occurred at RMC	CHK1A occurred at DRAM	WCHK1 occurred in MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
2C	MMC::DRAMCTRLERR							
	Not used	Not used	DRAM control signal RAMADR error	DRAM control signal CS error	DRAM control signal RAS error	DRAM control signal CAS error	DRAM control signal WE error	DRAM control signal DQM error
2D	MMC::CHK1ASTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
2E	MMC::CHK1ASTS							
	DATA CNTPE	Not used	Not used	Not used	Not used	Not used	Not used	IB WP ERR
2F	MMC::CHK1ASTS							
	IB RP ERR	IB HIT ERR	IB WTBL ERR	IB CNL ERR	MEM SEQ ERR	MEM INIT ERR	Not used	MEM ADR ERR
30	MMC::CHK1ASTS							
	MPU UNCER	MMC FETCH UNCER	MPU WR PROT	MPU ADR OVER	Not used	Not used	OTHER WR PROT	OTHER ADR OVER
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	'03'							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
4A	MMC::XRADRPERR							
	XR bus address parity error reset	Not used	XR bus address parity error reset	Not used	XR bus address parity error reset			
	<14-17>		<30-35, BE>		<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5D	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5E	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
5F	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	MMC::DBUGPIN							
	UVP data							
62	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
63	MPA::REV							
	Chip revision of MPA_LSI							
64	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
65	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
66	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CHK1BLOG1							
	CHK1B log address							
69	MPA::CHK1BLOG1							
	CHK1B log address							
6A	MPA::CHK1BLOG1							
	CHK1B log address							
6B	MPA::CHK1BLOG1							
	CHK1B log address							
6C	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	Not used	COM_IF write address parity error			COM_IF write data parity error			
		Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

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Byte27 = 8E & Byte34 = X0 & Byte28 = 40/50/60/70 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	MPA::CNT00/01ER							
	CNT#00 parity error				CNT#01 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
71	MPA::CNT02/03ER							
	CNT#02 parity error				CNT#03 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
72	MPA::CNT04/05ER							
	CNT#04 parity error				CNT#05 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
73	MPA::CNT06/07ER							
	CNT#06 parity error				CNT#07 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
74	MPA::CNT08/09ER							
	CNT#08 parity error				CNT#09 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
75	MPA::CNT10/11ER							
	CNT#10 parity error				CNT#11 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
76	MPA::CNT12/13ER							
	CNT#12 parity error				CNT#13 parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
77	MPA::CNT14ER							
	CNT#14 parity error				Not used	Not used	Not used	Not used
	Byte 0	Byte 1	Byte 2	Byte 3				
78	MPA::FMCTLERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
79	MPA::FMCTLERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
7A	MPA::FMCTLERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DIAG CRC error
7B	MPA::FMCTLERR							
	Not used	FMHDERR	WACS error	AREA error	WPRT error	EXL read error	EXL write error	NOEXL
7C	MPA::ILACSER							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	ILACSER
7D	MPA::RDSTSFLG							
	Not used	Not used	Not used	Not used	Not used	ATMIC FLG	IRDADR FLG	IRD FLG
7E	Not used							
7F	Not used							

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'40': MPA XR CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'50': MPA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'60': MPA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'70': MPA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71(CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		'04'						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::LAST1IP						
		Last address before CHK1B occurred						
43		MMC::LAST1IP						
		Last address before CHK1B occurred						
44		MPA::FMXCSV_U						
		FMEXL_U						
45		MPA::FMXCSV_U						
		FMEXL_U						
46		MPA::FMXCSV_U						
		FMEXL_U						
47		MPA::FMXCSV_U						
		FMEXL_U						
48		MPA::FMXCSV_L						
		FMEXL_L						
49		MPA::FMXCSV_L						
		FMEXL_L						
4A		MPA::FMXCSV_L						
		FMEXL_L						
4B		MPA::FMXCSV_L						
		FMEXL_L						
4C		MPA::FMCTLERR						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4D		MPA::FMCTLERR						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4E		MPA::FMCTLERR						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DIAG CRC error
4F		MPA::FMCTLERR						
	Not used	FMHDERR	WACS error	AREA error	WPRT error	EXL read error	EXL write error	NOEXL

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Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71(CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MPA::CHK1BLOG1							
	CHK1B log address							
51	MPA::CHK1BLOG1							
	CHK1B log address							
52	MPA::CHK1BLOG1							
	CHK1B log address							
53	MPA::CHK1BLOG1							
	CHK1B log address							
54	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
55	MPA::FM_DGSQE1							
	DIAG sequencer log parity error				Not used	SERR_SQ	Not used	PERR_SQ
56	MPA::FM_SQERR							
	DIAG sequencer log parity error				Not used	SERR_SQ	Not used	PERR_SQ
57	MPA::WRADRCNT_ERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DIAG read counter parity error
58	MPA::FM_SIG_ERR1							
	SIGERR_CS							
59	MPA::FM_SIG_ERR1							
	SIGERR_WE				SIGERR_OE			
5A	MPA::FM_DIAG_SQS							
	DIAGSQ_ST_S							
5B	MPA::FM_SQS							
	FMSQ_ST_S							
5C	MPA::FM_SIG_ERR2							
	SIGERR_DT							
5D	MPA::FM_SIG_ERR2							
	Not used	Not used	SIGERR_AD					
5E	MPA::FM_SIG_ERR2							
	SIGERR_AD							
5F	MPA::FM_SIG_ERR2							
	SIGERR_AD							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MPA::FM_DIAG_LOG							
	DIAG main sequencer state log < 3rd >							
61	MPA::FM_DIAG_LOG							
	DIAG main sequencer state log < 2nd >							
62	MPA::FM_DIAG_LOG							
	DIAG main sequencer state log < 1st >							
63	MPA::FM_DIAG_LOG							
	DIAG main sequencer state log < last >							
64	MPA::FM_SQ_LOG							
	DIAG main sequencer state log < 3rd >							
65	MPA::FM_SQ_LOG							
	DIAG main sequencer state log < 2nd >							
66	MPA::FM_SQ_LOG							
	DIAG main sequencer state log < 1st >							
67	MPA::FM_SQ_LOG							
	DIAG main sequencer state log < last >							
68	MPA::DIAGCNT_ERR							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	DIAG read counter parity error
69	MPA::FM_DIAG_CNT							
	DIAG main sequencer state log < 2nd >							
6A	MPA::FM_DIAG_CNT							
	DIAG main sequencer state log < 1st >							
6B	MPA::FM_DIAG_CNT							
	DIAG main sequencer state log < last >							
6C	MPA::FM_EXCLSV_SET							
	EXLSET							
6D	MPA::FM_EXCLSV_SET							
	EXLSET							
6E	MPA::FM_EXCLSV_SET							
	EXLCODE							
6F	MPA::FM_EXCLSV_SET							
	EXLCODE							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 41/51/61/71 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	MPA::FMSTS							
	MP 0 lock	MP 1 lock	MP 2 lock	MP 3 lock	Not used	WR_WAIT	FM sequencer busy	FM busy
71	MPA::FMSTS							
	Not used	Not used	DIAG INI	FM 4M SEL	FM write2 wait	FM write3 wait	FM read2 wait	FM read3 wait
72	MPA::FMSTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
73	MPA::FMSTS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
74	MPA::FMAREA							
	FM area							
75	MPA::FMAREA							
	FM area							
76	MPA::FMAREA							
	FM area							
77	MPA::FMAREA							
	FM area							
78	MPA::FM_BNKEXL_SET							
	FM0 BNK00	FM0 BNK01	FM0 BNK02	FM0 BNK03	FM0 BNK10	FM0 BNK11	FM0 BNK12	FM0 BNK13
79	MPA::FM_BNKEXL_SET							
	FM1 BNK00	FM1 BNK01	FM1 BNK02	FM1 BNK03	FM1 BNK10	FM1 BNK11	FM1 BNK12	FM1 BNK13
7A	MPA::FM_BNKEXL_SET							
	FM2 BNK00	FM2 BNK01	FM2 BNK02	FM2 BNK03	FM2 BNK10	FM2 BNK11	FM2 BNK12	FM2 BNK13
7B	MPA::FM_BNKEXL_SET							
	FM3 BNK00	FM3 BNK01	FM3 BNK02	FM3 BNK03	FM3 BNK10	FM3 BNK11	FM3 BNK12	FM3 BNK13
7C	MPA::FM_WR_PRTL							
	FMWPL							
7D	MPA::FM_WR_PRTL							
	FMWPL							
7E	MPA::FM_WR_PRTL							
	FMWPL							
7F	MPA::FM_WR_PRTL							
	FMWPL							

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'41': FM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘51’: FM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'61': FM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘71’: FM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
2D	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
2E	MPA::XWER							
	XR write address parity error				XR write data parity error			
	byte0	byte1	byte2	byte3	byte0	byte1	byte2	byte3
2F	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					byte0	byte1	byte2	byte3
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’05’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
4A	MMC::XRADRPERR							
	XR bus address parity error reset	Not used	XR bus address parity error reset	Not used	XR bus address parity error reset			
	<14-17>		<30-35, BE>		<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5D	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5E	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
5F	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	MMC::DBUGPIN							
	UVP data							
62	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
63	MPA::REV							
	Chip revision of MPA_LSI							
64	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
65	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
66	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CHK1BLOG1							
	CHK1B log address							
69	MPA::CHK1BLOG1							
	CHK1B log address							
6A	MPA::CHK1BLOG1							
	CHK1B log address							
6B	MPA::CHK1BLOG1							
	CHK1B log address							
6C	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	Not used	COM_IF write address parity error			COM_IF write data parity error			
		Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

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Byte27 = 8E & Byte34 = X0 & Byte28 = 42 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	XPA::PNXRR0							
	Not used	PX read response count error	XR DMA access error	XR DMA count error	PX RD RSP timeout	XR DMA LRC error	XR address parity error	XR write data parity error
71	XPA::PnISTAT							
	Not used	Not used	Not used	Not used	ORCA CHK2 OTHER	Not used	Not used	Other PCI Master error
72	XPA::PnISTAT							
	Not used	Not used	Not used	Not used	ORCA CHK2 OWN	PCI SERR IN	PCI Config error	XPA error
73	XPA::PNXRR1							
	XR target address parity error 3	XR target address parity error 2	XR target address parity error 1	XR target address parity error 0	XR target write data parity error 3	XR target write data parity error 2	XR target write data parity error 1	XR target write data parity error 0
74	XPC::PNDIAG2							
	DIAG resister 2							
75	XPC::PNDIAG2							
	DIAG resister 2							
76	XPC::PNDIAG2							
	DIAG resister 2							
77	XPC::PNDIAG2							
	DIAG resister 2							
78	XPC::PNDIAG1							
	DIAG resister 1							
79	XPC::PNDIAG1							
	DIAG resister 1							
7A	XPC::PNDIAG1							
	DIAG resister 1							
7B	XPC::PNDIAG1							
	DIAG resister 1							
7C	XPC::PNDIAG0							
	DIAG resister 0							
7D	XPC::PNDIAG0							
	DIAG resister 0							
7E	XPA::PNSC							
	Detected parity error	Signaled system error	Received master abort	Received target abort	Not used	DEVSEL timing	DEVSEL timing	Data parity report
7F	XPA::PNSC							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
7	Format (x‘8’)				Message (x‘E’)			
8	Subcode x’42’: XPA CHK1B							
9	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
10	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
11	XPA:PNXERRO							
	Not used	PX read response count error	XR DMA access error	XR DMA count error	PX RD RSP timeout	XR DMA LRC error	WR address parity error	XR wirte date parity error
12	XPA:PNXERRO							
	Not used	Not used	PCI master address counter parity error	PCI master address parity error	PCI master SEQ error	PCI master read parity error	PCI master PERR in	PCI master PERR out
13	XPA:PNXERRO							
	Not used	PCI target100 address counter error	PCI target66 address counter error	PCI target SEQ error	Not used	PCI target read parity error	PCI target PERR in	PCI target PERR out
14	XPA:PNXERRO							
	XR TRG SEQ error	Not used	Not used	XR master address parity error	XR target cnt parity error	XR DMA read parity error	XR time over	XR read parity error
15	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
16	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
17	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’06’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
4A	MMC::XRADRPERR							
	XR bus address parity error reset	Not used	XR bus address parity error reset	Not used	XR bus address parity error reset			
	<14-17>		<30-35, BE>		<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5D	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5E	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
5F	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	MMC::DBUGPIN							
	UVP data							
62	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
63	MPA::REV							
	Chip revision of MPA_LSI							
64	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
65	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
66	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CHK1BLOG1							
	CHK1B log address							
69	MPA::CHK1BLOG1							
	CHK1B log address							
6A	MPA::CHK1BLOG1							
	CHK1B log address							
6B	MPA::CHK1BLOG1							
	CHK1B log address							
6C	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	Not used	COM_IF write address parity error			COM_IF write data parity error			
		Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

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Byte27 = 8E & Byte34 = X0 & Byte28 = 43 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	XCLM::CHK1B							
	Local bus address parity error 0	Not used	Local bus address parity error 2	Local bus address parity error 3	Local bus input data parity error 0	Local bus input data parity error 1	Local bus input data parity error 2	Local bus input data parity error 3
71	XCLM::CHK1B							
	Local bus output data parity error 0	Local bus output data parity error 1	Local bus output data parity error 2	Local bus output data parity error 3	Not used	Not used	Not used	Not used
72	XCLM::CHK1B							
	DBF CHK1B	PK CHK1B	Not used	Not used	EXPTRUD	SRPTRUD	RIPTRUD	Not used
73	XCLM::CHK1B							
	SVC EXEC error	SCVP error	Not used	Not used	Not used	Not used	Not used	Not used
74	XCLM::XFC							
	ENB XFR	EXE XFR	Not used	Not used	Not used	CBP IN CSTP	CACHE IO REG	SSD MODE
75	XCLM::XFC							
	Data path				UMODE	Not used	Not used	WRFBA
76	Not used							
77	Not used							
78	XCLM::XFS0							
	Transfer end	Not used	Not used	PFC status	CHK2	CHK2A	CHK2B	CHK2C
79	XCLM::XFS0							
	CHK2D	Truncation	Halt I/O	Search EQ	Search Hi	Search Lo	Not used	Aborted
7A	XCLM::XFS1							
	Not used	Not used	Not used	Not used	MP aborted	HW aborted	PCHK1ST	PCHK2ST
7B	XCLM::XFS1							
	Next segment address REG stasus	Not used	Not used	Not used	Not used	Next Segment address REG wait	PFC zero	Not used
7C	XCLM::CK21							
	SROPE	CM WADPER	CM WDPER	TSEQPER	Not used	Not used	Not used	Not used
7D	XCLM::CK22							
	LABUSERA	LABUSERB	LABUSERC	LABUSERD	LABUSERE	LABUSERF	LABUSERG	LABUSERH
7E	XCLM::LSTA							
	LCP busy	LCP stop	ADRCMPEQ	TR stop	IFER	DCHK1	PDSBL	PARACH
7F	Not used							

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x’43’: ESCON/FICON CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	XLCM::CHK1B							
	IA0 parity error	Not used	IA2 parity error	IA3 parity error	ID0 parity error	ID1 parity error	ID2 parity error	ID3 parity error
2D	XLCM::CHK1B							
	OD0 parity error	OD1 parity error	OD2 parity error	OD3 parity error	Not used	Not used	Not used	Not used
2E	XLCM::CHK1B							
	CBF CHK1B	PL CHK1B	Not used	Not used	EXPTRUD	SRPTRUD	RIPTRUD	Not used
2F	XLCM::CHK1B							
	SVCEXEC error	SCVP error	Not used	Not used	Not used	Not used	Not used	Not used
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74(CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74(CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’07’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74(CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
55	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
56	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
57	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
58	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
59	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
5A	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
5B	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
5C	MMC::LAST1							
	Last execution address before CHK1B occurred							
5D	MMC::LAST1							
	Last execution address before CHK1B occurred							
5E	MMC::LAST1							
	Last execution address before CHK1B occurred							
5F	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74(CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
61	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
62	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
63	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
64	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
65	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
66	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
67	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
68	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
69	RMC::DRAMC1BSTS							
	MPU→LM access Correctable errors	MPU→LM access fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
6A	RMC::DRAMC1BSTS							
	LANC→LM access Correctable errors	Not used	LANC→LM access Uncorrectabl error detected	Not used	LANC→XR incorrect address	Not used	Not used	Not used
6B	RMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
6C	RMC::ERADR							
	Address from L bus							
6D	RMC::ERADR							
	Address from L bus							
6E	RMC::ERADR							
	Address from L bus							
6F	RMC::ERADR							
	Address from L bus						Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 44/54/64/74(CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	RMC::ERRDGADR							
	Error Reg address							
71	RMC::ERRDGADR							
	Error Reg address							
72	RMC::ERRDGADR							
	Error Reg address							
73	RMC::ERRDGADR							
	Error Reg address						Not used	Not used
74	RMC::ERWR							
	Not used	Not used	Not used	Not used	Not used	Not used	WR signal Reg	WR signal value
75	RMC::CECNT							
	Correctable error counter (for upper address bank)							
76	RMC::CECNT							
	Correctable error counter (for upper address bank)							
77	MMC::DBUGPIN							
	UVP data							
78	MMC::RCVINT							
	Not used	Not used	Not used	Not used	LEDBUS (FCA) signal monitor bit	Not used	PCI signal monitor bit	Not used
79	MMC::RCVINT							
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	BC (MPA) signal monitor bit	Not used	CHK2 signal monitor bit	CHA signal monitor bit
7A	MMC::RCVINT							
	Not used	CHK3 signal monitor bit	Not used	FCA signal monitor bit	Not used	DTA signal monitor bit	MPCOM (MPA) signal monitor bit	CHK3 (MPA) signal monitor bit
7B	MMC::RCVINT							
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7C	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
7D	Not used							
7E	Not used							
7F	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'44': MMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2D	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2F	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
	MMC::MMCPERR							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
30	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer7 parity error
31	MMC::LBUSPER							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
32								

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'54': MMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2D	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2F	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
30	MMC::MMCPERR							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
31	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
32	MMC::LBUSPER							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'64': MMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2D	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2F	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
30	MMC::MMCPERR							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
31	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
32	MMC::LBUSPER							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'74': MMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
2D	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
2E	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error
2F	MMC::MPCERRSTS							
	Not used	Not used	WCHK1 at MPCHK	CHK1A at MPCHK	Timeout monitor timer parity error	A/B REG inconsistent check error	A/B REG write time-out	A/B REG access sequence error
30	MMC::MMCPERR							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
31	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer7 parity error
32	MMC::LBUSPER							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>

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Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75 (CHK1B)(2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’08’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75(CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5E	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5F	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred

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Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75(CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	RMC::DRAMC1BSTS							
	MPU→LM access Correctable errors	MPU→LM access fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
62	RMC::DRAMC1BSTS							
	LANC→LM access Correctable errors	Not used	LANC→LM access Uncorrectabl error detected	Not used	LANC→XR incorrect address	Not used	Not used	Not used
63	RMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	RMC::ERADR							
	Address from L bus							
65	RMC::ERADR							
	Address from L bus							
66	RMC::ERADR							
	Address from L bus							
67	RMC::ERADR							
	Address from L bus						Not used	Not used
68	RMC::ERORD							
	Data before correction							
69	RMC::ERORD							
	Data before correction							
6A	RMC::ERORD							
	Data before correction							
6B	RMC::ERORD							
	Data before correction							
6C	MMC::ERORC							
	Check bit before correction							
6D	MMC::ERORC							
	Check bit before correction							
6E	RMC::ERCRD							
	Data after correction							
6F	RMC::ERCRD							
	Data after correction							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 45/55/65/75 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		RMC::ERCRD						
		Data after correction						
71		RMC::ERCRD						
		Data after correction						
72		RMC::ERCRC						
		Check bit after correction						
73		RMC::ERCRC						
		Check bit after correction						
74		RMC::ERRSYD						
		Syndrome before correction						
75		RMC::ERRSYD						
		Syndrome before correction						
76		RMC::ERWA						
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	WR signal value
77		RMC::RMCC1BSTS						
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
78		RMC::CECNT						
		Correctable error counter(Low)						
79		RMC::CECNT						
		Correctable error counter(High)						
7A		MMC::RCVINT						
	Not used	Not used	Not used	Not used	LEDBUS (FCA) signal monitor bit	Not used	PCI signal monitor bit	Not used
7B		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	BC (MPA) signal monitor bit	Not used	CHK2 signal monitor bit	CHA signal monitor bit
7C		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	FCA signal monitor bit	Not used	DTA signal monitor bit	MPCOM (MPA) signal monitor bit	CHK3 (MPA) signal monitor bit
7D		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7E		MMC::DBUGPIN						
		UVP data						
7F		MPA::MPASTS						
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF $\overline{\text{CHK1B}}$ occurred	COM_IF $\overline{\text{CHK1B}}$ occurred	XR_IF $\overline{\text{CHK1B}}$ occurred	MPINT status bit

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘45’: MMC DRAM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM							
31	MMC::ERADR							
	Error address in LM							
32	MMC::ERADR							
	Error address in LM						Not used	Not used

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘55’: MMC DRAM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM							
31	MMC::ERADR							
	Error address in LM							
32	MMC::ERADR							
	Error address in LM						Not used	Not used

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘65’: MMC DRAM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM							
31	MMC::ERADR							
	Error address in LM							
32	MMC::ERADR							
	Error address in LM						Not used	Not used

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘75’: MMC DRAM CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM							
31	MMC::ERADR							
	Error address in LM							
32	MMC::ERADR							
	Error address in LM						Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B)(2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’09’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::MICPERSTS							
	Not used	Not used	Not used	Not used	Data parity err in MMC <00-07>	Data parity err in MMC <10-17>	Data parity err in MMC <20-27>	Data parity err in MMC <30-37>
4A	MMC::XRADRPERR							
	Not used	Not used	Not used	XR bus address parity error reset				
				<30-35, BE>	<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
5D	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5E	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5F	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred

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Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	RMC::DRAMC1BSTS							
	MPU→LM access Correctable errors	MPU→LM access fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
62	RMC::DRAMC1BSTS							
	LANC→LM access Correctable errors	Not used	LANC→LM access Uncorrectabl error detected	Not used	LANC→XR incorrect address	Not used	Not used	Not used
63	RMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
64	RMC::FERADR							
	Address from L bus (fetch)							
65	RMC::FERADR							
	Address from L bus (fetch)							
66	RMC::FERADR							
	Address from L bus (fetch)							
67	RMC::FERADR							
	Address from L bus (fetch)						Not used	Not used
68	RMC::FERORD							
	Data before correction (fetch)							
69	RMC::FERORD							
	Data before correction (fetch)							
6A	RMC::FERORD							
	Data before correction (fetch)							
6B	RMC::FERORD							
	Data before correction (fetch)							
6C	RMC::FERORC							
	Check bit before correction (fetch)							
6D	RMC::FERORC							
	Check bit before correction (fetch)							
6E	RMC::FERCRD							
	Data after correction (fetch)							
6F	RMC::FERCRD							
	Data after correction (fetch)							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 46/66 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70		RMC::FERCRD						
		Data after correction (fetch)						
71		RMC::FERCRD						
		Data after correction (fetch)						
72		RMC::FERCRC						
		Check bit after correction (fetch)						
73		RMC::FERCRC						
		Check bit after correction (fetch)						
74		RMC::FERRSYD						
		Syndrome before correction (fetch)						
75		RMC::FERRSYD						
		Syndrome before correction (fetch)						
76		RMC::CECNT						
		Correctable error counter(Low)						
77		RMC::CECNT						
		Correctable error counter(High)						
78		MMC::RCVINT						
	Not used	Not used	Not used	Not used	LEDBUS (FCA) signal monitor bit	Not used	PCI signal monitor bit	Not used
79		MMC::RCVINT						
	SYSRST signal monitor bit	SELRST signal monitor bit	CHK1A signal monitor bit	CHK1B signal monitor bit	BC (MPA) signal monitor bit	Not used	CHK2 signal monitor bit	CHA signal monitor bit
7A		MMC::RCVINT						
	Not used	CHK3 signal monitor bit	Not used	FCA signal monitor bit	Not used	DTA signal monitor bit	MPCOM (MPA) signal monitor bit	CHK3 (MPA) signal monitor bit
7B		MMC::RCVINT						
	TIMER0 signal monitor bit	TIMER1 signal monitor bit	TIMER2 signal monitor bit	TIMER3 signal monitor bit	TIMER4 signal monitor bit	TIMER5 signal monitor bit	TIMER6 signal monitor bit	SYNC STOP signal monitor bit
7C		RMC::RMCC1BSTS						
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
7D		MMC::DBUGPIN						
		UVP data						
7E		MPA::MPID						
		PKID#			Not used	Not used	MPID#	
7F		MPA::MPASTS						
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF $\overline{\text{CHK1B}}$ occurred	COM_IF $\overline{\text{CHK1B}}$ occurred	XR_IF $\overline{\text{CHK1B}}$ occurred	MPINT status bit

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘46’: MMC FETCH CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::FERADR							
	Error address in fetch to LM							
30	MMC::FERADR							
	Error address in fetch to LM							
31	MMC::FERADR							
	Error address in fetch to LM							
32	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'66': MMC FETCH CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	MMC::DRAMC1BSTS							
	MPU correctable error	MMC FETCH correctable error	MPU XR read incorrect	MPU XR write incorrect	Not used	Not used	Not used	Not used
2D	MMC::DRAMC1BSTS							
	Other correctable error	Not used	Other uncorrectable error	Not used	Not used	Not used	Not used	Not used
2E	MMC::DRAMC1BSTS							
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
2F	MMC::FERADR							
	Error address in fetch to LM							
30	MMC::FERADR							
	Error address in fetch to LM							
31	MMC::FERADR							
	Error address in fetch to LM							
32	MMC::FERADR							
	Error address in fetch to LM						Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		’0A’						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::C1WSTS						
	CHK1A detected	WCHK1 detected	CHK1A at MPCHK	CHK1A at RMC	CHK1A at DRAM	WCHK1 at MPCHK	WCHK1 by CHK1A in CHK1A	Micro-force WCHK1
43		RMC::RMCC1BSTS						
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
44		RMC::DRAMC1BSTS						
	MPU→LM access Correctable errors	MPU→LM access fetch Correctable errors	MPU XR read incorrect address	MPU XR write incorrect address	Not used	Not used	Not used	Not used
45		RMC::DRAMC1BSTS						
	LANC→LM access Correctable errors	Not used	LANC→LM access Uncorrectabl error detected	Not used	LANC→XR incorrect address	Not used	Not used	Not used
46		RMC::DRAMC1BSTS						
	Not used	Refresh request timer error	Not used	Refresh time out	Not used	Not used	Not used	Not used
47		Not used						
48		RMC::MPSCRECT						
	ECC COR B0	ECC COR B1	ECC COR B2	ECC COR B3	Not used	Not used	Not used	Not used
49		RMC::MPSCRECT						
	OUT CORR	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4A		RMC::IBCPERR						
	IBM ADRER	IBM AFIFOER	IBM DFIFOR	IBM REGER	IB BUSER	Not used	Not used	Not used
4B		RMC::IBCPERR						
	IBS WBWCPE	IBS WBRCPE	IBS RBWCPE	IBS RBRCPE	IBS TRFWERR	Not used	Not used	Not used
4C		RMC::DTERR1						
		Not used		Not used				Not used
4D		RMC::DTERR1						
		Not used	Not used	Not used			Not used	Not used
4E		RMC::DTERR1						
	RMW REGPE	RMW DTPE	RMW RDTPE	RMW FAILED	DMW REGPE	DMA DTPE	MPI MWRER	Not used
4F		Not used						

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Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	RMC::DTERR2							
	XRW BDTPE	XRW DTPE	XRW DTERR	Not used	RDDTPE	XRR BDTPE	Not used	Not used
51	RMC::DTERR2							
	WBDT0PE	WBDT1PE	LMW RDTERR	LMW RDTPE	LMW D0CMPER	LMW D1CMPER	LMW DS1ER	LMW DUCER
52	RMC::DTERR2							
	LMR D0PE	LMR D1PE	Not used	Not used	Not used	Not used	LMD MALMT OVR	DULMYPE
53	RMC::DTERR2							
	DLLMTPE	CULMTPE	CLLMTPE2	LMXRACM PER	AMD MAA CPE	LMD MAL CPE	LMD MAX CPE	LMD MASEQ PE
54	RMC::IBCPERR							
	IBM WDPE	IBM RDPE	IBS PER0	IBS PER1	IBS PER2	IBS PER3	INBUS ERR	Not used
55	RMC::IBCPERR							
	LMIBPE	Not used	CTXFCPE	CRXFCPE	CDMA DTPE0	CDMA DTPE1	CDMA DTPE2	CDMA DTPE3
56	RMC::IBCPERR							
	CMDT PE0	CMDT PE1	CMDT PE2	CMDT PE3	CSDT PE0	CSDT PE1	CSDT PE2	CSDT PE3
57	RMC::IBCPERR							
	E2C PE0	E2C PE1	E2C PE2	E2C PE3	SI0 PE0	SI0 PE1	SI0 PE2	SI0 PE3
58	MMC::LAST1IP							
	Last address before CHK1B occurred							
59	MMC::LAST1IP							
	Last address before CHK1B occurred							
5A	MMC::LAST1IP							
	Last address before CHK1B occurred							
5B	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used
5C	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
5D	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
5E	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
5F	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
61	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
62	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred							
63	MMC:: LAST3IP							
	Address two generations older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
64	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
65	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
66	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred							
67	MMC:: LAST4IP							
	Address two generations older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
68	MMC::LAST1							
	Last execution address before CHK1B occurred							
69	MMC::LAST1							
	Last execution address before CHK1B occurred							
6A	MMC::LAST1							
	Last execution address before CHK1B occurred							
6B	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
6C	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
6D	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
6E	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
6F	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 47/67(CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	RMC::ERRDGADR							
	Error Reg address							
71	RMC::ERRDGADR							
	Error Reg address							
72	RMC::ERRDGADR							
	Error Reg address							
73	RMC::ERRDGADR							
	Error Reg address						Not used	Not used
74	MMC::CHK1BADRS							
	Address when CHK1B occurred							
75	MMC::CHK1BADRS							
	Address when CHK1B occurred							
76	MMC::CHK1BADRS							
	Address when CHK1B occurred							
77	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
78	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
79	MMC::MICCHK1STS							
	Not used	Not used	MPCHK counter parity error	MIC internal bus parity error	MPU reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
7A	MMC::MICCHK1STS							
	Not used	Wait timeout	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus parity error	XR data parity error
7B	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
7C	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
7D	MMC::DBUGPIN							
	UVP data							
7E	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
7F	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF $\overline{CHK1B}$ occurred	COM_IF $\overline{CHK1B}$ occurred	XR_IF $\overline{CHK1B}$ occurred	MPINT status bit

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘47’:RMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	Not used							
2D	MMC::ERADR							
	Error address in LM							
2E	MMC::ERADR							
	Error address in LM							
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM						Not used	Not used
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x‘8’)				Message (x‘E’)			
29	Subcode x‘67’:RMC CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	Not used							
2D	MMC::ERADR							
	Error address in LM							
2E	MMC::ERADR							
	Error address in LM							
2F	MMC::ERADR							
	Error address in LM							
30	MMC::ERADR							
	Error address in LM						Not used	Not used
31	RMC::RMCC1ASTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7
32	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40		FREE AREA FORMAT No.						
		’0C’						
41		MMC::ERRSTS						
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42		MMC::CHK1BSTS						
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43		MMC::CHK1BSTS						
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44		MMC::CHK1BADRS						
		Address when CHK1B occurred						
45		MMC::CHK1BADRS						
		Address when CHK1B occurred						
46		MMC::CHK1BADRS						
		Address when CHK1B occurred						
47		MMC::CHK1BADRS						
		Address when CHK1B occurred					WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48		MMC::CHK1BBE						
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49		MMC::LBUSPERR						
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
4A		MMC::XRADRPERR						
	XR bus address parity error reset	Not used	XR bus address parity error reset	Not used	XR bus address parity error reset			
	<14-17>		<30-35, BE>		<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B		MMC::XBUSDTPERR						
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C		MMC::LAST1IP						
		Last address before CHK1B occurred						
4D		MMC::LAST1IP						
		Last address before CHK1B occurred						
4E		MMC::LAST1IP						
		Last address before CHK1B occurred						
4F		MMC::LAST1IP						
		Last address before CHK1B occurred			Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5D	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5E	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
5F	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	MMC::DBUGPIN							
	UVP data							
62	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
63	MPA::REV							
	Chip revision of MPA_LSI							
64	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
65	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
66	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CHK1BLOG1							
	CHK1B log address							
69	MPA::CHK1BLOG1							
	CHK1B log address							
6A	MPA::CHK1BLOG1							
	CHK1B log address							
6B	MPA::CHK1BLOG1							
	CHK1B log address							
6C	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	Not used	COM_IF write address parity error			COM_IF write data parity error			
		Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

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Byte27 = 8E & Byte34 = X0 & Byte28 = 48/58 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	XPA::PNXRR0							
	Not used	Not used	PCI master address counter parity error	PCI master address parity error	PCI master SEQ error	PCI master read parity error	PCI master PERR IN	PCI master PERR OUT
71	XPA::PNXRR0							
	Not used	PCI target100 address counter error	PCI target66 address counter error	PCI target SEQ error	Not used	PCI target read parity error	PCI target PERR IN	PCI target PERR OUT
72	XPA::PNXRR0							
	XR TRG SEQ error	Not used	Not used	XR master address parity error	XR target address CNT parity error	XR DMA read rarity error	XR time over	XR read parity error
73	XPA::PNXRR1							
	XR target address parity error 3	XR target address parity error 2	XR target address parity error 1	XR target address parity error 0	XR target write data parity error 3	XR target write data parity error 2	XR target write data parity error 1	XR target write data parity error 0
74	XPC::PNDIAG2							
	DIAG resister 2							
75	XPC::PNDIAG2							
	DIAG resister 2							
76	XPC::PNDIAG2							
	DIAG resister 2							
77	XPC::PNDIAG2							
	DIAG resister 2							
78	XPC::PNDIAG1							
	DIAG resister 1							
79	XPC::PNDIAG1							
	DIAG resister 1							
7A	XPC::PNDIAG1							
	DIAG resister 1							
7B	XPC::PNDIAG1							
	DIAG resister 1							
7C	XPC::PNDIAG0							
	DIAG resister 0							
7D	XPC::PNDIAG0							
	DIAG resister 0							
7E	XPA::PNSC							
	Detected parity error	Signaled system error	Received master abort	Received target abort	Not used	DEVSEL timing	DEVSEL timing	Data parity report
7F	XPA::PNSC							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
7	Format (x‘8’)				Message (x‘E’)			
8	Subcode x’48’: XMPA CHK1B							
9	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
10	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
11	XPA:PNXCK1B							
	PCI Config error	PX Read Response Count error	XR DMA Access error	XR DMA Count error	PX RD RSP timeout	XR DMA LCR error	XR address Parity error	XR write data parity error
12	XPA:PNXCK1B							
	Not used	Not used	Not used	Not used	Not used	NMI	IERR	SMBALERT
13	XPA:PNXCK1B							
	Not used	Not used	Not used	Not used	Not used	Not used	CMEN XR ECC2bit error	CMEM PCI ECC2bit error
14	XPA:PNISTAT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	XPA error
15	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
16	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
17	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: CHA CHK1B)

	0	1	2	3	4	5	6	7
7	Format (x‘8’)				Message (x‘E’)			
8	Subcode x’58’: XMPA CHK1B							
9	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
10	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
11	XPA:PNXCK1B							
	PCI Config error	PX Read Response Count error	XR DMA Access error	XR DMA Count error	PX RD RSP timeout	XR DMA LCR error	XR address Parity error	XR write data parity error
12	XPA:PNXCK1B							
	Not used	Not used	Not used	Not used	Not used	NMI	IERR	SMBALERT
13	XPA:PNXCK1B							
	Not used	Not used	Not used	Not used	Not used	Not used	CMEN XR ECC2bit error	CMEM PCI ECC2bit error
14	XPA:PNISTAT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	XPA error
15	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
16	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
17	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) (1/5)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	Reserved							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	SP no. 2^1	SP no. 2^0	CTLR no.	DKU physical device no.				
25	Cylinder address (low order)							
26	Cylinder address (high order)							
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode							
29	Hardware information (See following pages)							
|								
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = 6587/x‘EF8E’ : LDEV type = 6586)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) (2/5)

	0	1	2	3	4	5	6	7
40	FREE AREA FORMAT No.							
	’0B’							
41	MMC::ERRSTS							
	Not used	Not used	Not used	Not used	Not used	WCHK1	CHK1B	CHK1A
42	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHK1B at CHA	CHK1B at MPA	CHK1B at MMC
43	MMC::CHK1BSTS							
	CHK1B at QDTA	Not used	Not used	Not used	Not used	Not used	CHK1B at RMC	CHK1B in DRAM controller
44	MMC::CHK1BADRS							
	Address when CHK1B occurred							
45	MMC::CHK1BADRS							
	Address when CHK1B occurred							
46	MMC::CHK1BADRS							
	Address when CHK1B occurred							
47	MMC::CHK1BADRS							
	Address when CHK1B occurred						WR/RD flag in CHK1B	Command/ Data flag in CHK1B
48	MMC::CHK1BBE							
	Not used	Not used	Not used	Not used	BE0 in CHK1B	BE1 in CHK1B	BE2 in CHK1B	BE3 in CHK1B
49	MMC::LBUSPERR							
	Not used	Not used	Not used	Not used	L bus data parity error <00-07>	L bus data parity error <10-17>	L bus data parity error <20-27>	L bus data parity error <30-37>
4A	MMC::XRADRPERR							
	XR bus address parity error reset	Not used	XR bus address parity error reset	Not used	XR bus address parity error reset			
	<14-17>		<30-35, BE>		<Byte 0>	<Byte 1>	<Byte 2>	<Byte 3>
4B	MMC::XBUSDTPERR							
	Not used	Not used	Not used	Not used	XR bus data parity error <00-07>	XR bus data parity error <10-17>	XR bus data parity error <20-27>	XR bus data parity error <30-37>
4C	MMC::LAST1IP							
	Last address before CHK1B occurred							
4D	MMC::LAST1IP							
	Last address before CHK1B occurred							
4E	MMC::LAST1IP							
	Last address before CHK1B occurred							
4F	MMC::LAST1IP							
	Last address before CHK1B occurred				Not used	Not used	Not used	Not used

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Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) (3/5)

	0	1	2	3	4	5	6	7
50	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
51	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
52	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred							
53	MMC::LAST2IP							
	Address one generation older than the last one before CHK1B occurred				Not used	Not used	Not used	Not used
54	MMC::LAST1							
	Last execution address before CHK1B occurred							
55	MMC::LAST1							
	Last execution address before CHK1B occurred							
56	MMC::LAST1							
	Last execution address before CHK1B occurred							
57	MMC::LAST1							
	Last execution address before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
58	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
59	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5A	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred							
5B	MMC::LAST2							
	Execution address one generation older than the last one before CHK1B occurred				Not used	Not used	CHK1A occurred in LAN OP	Not used
5C	MMC::TIMERR							
	Timer 0 parity error	Timer 1 parity error	Timer 2 parity error	Timer 3 parity error	Timer 4 parity error	Timer 5 parity error	Timer 6 parity error	Timer 7 parity error
5D	MMC::RSTSTS							
	Not used	Not used	Micro CHK1B occurred	Micro CHK1A occurred	Micro MCNRST2 occurred	Micro MCNRST1 occurred	Micro MPRST occurred	Micro MNTRST occurred
5E	MMC::RSTSTS							
	Not used	Not used	SCAN mode set occurred	CHK1A occurred	WCHK1 occurred	SELRST occurred	SYSRST occurred	Power-on reset occurred
5F	RMC::RMCC1BSTS							
	RMC INT0	RMC INT1	RMC INT2	RMC INT3	RMC INT4	RMC INT5	RMC INT6	RMC INT7

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Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) (4/5)

	0	1	2	3	4	5	6	7
60	MMC::CHK3STS							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CHK3 error in SMP, LSI
61	MMC::DBUGPIN							
	UVP data							
62	MPA::MPID							
	PKID#				Not used	Not used	MPID#	
63	MPA::REV							
	Chip revision of MPA_LSI							
64	MPA::MPASTS							
	MPAINT status bit	Master CHK3 occurred	Slave CHK3 occurred	Not used	PROM_IF CHK1B occurred	COM_IF CHK1B occurred	XR_IF CHK1B occurred	MPINT status bit
65	MPA::XWER							
	Access to not use address	Access to not use address	Access to not use address	Not used	Not used	Not used	Not used	XR byte access error
66	MPA::XWER							
	XR write address parity error				XR write data parity error			
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
67	MPA::XRER							
	Not used	Not used	Not used	Not used	XR read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3
68	MPA::CHK1BLOG1							
	CHK1B log address							
69	MPA::CHK1BLOG1							
	CHK1B log address							
6A	MPA::CHK1BLOG1							
	CHK1B log address							
6B	MPA::CHK1BLOG1							
	CHK1B log address							
6C	MPA::CHK1BLOG2							
	BE0	BE1	LOCK	WT	A0P	A1P	A2P	A3P
6D	MPA::CWER							
	Not used	Not used	Not used	Not used	Not used	Access to not use register	Access to not use register	Access to not use register
6E	MPA:: CWER							
	Not used	COM_IF write address parity error			COM_IF write data parity error			
		Byte 1	Byte 2	Byte 3	Byte 0	Byte 1	Byte 2	Byte 3
6F	MPA::CRER							
	Not used	Not used	Not used	Not used	COM_IF read data parity error			
					Byte 0	Byte 1	Byte 2	Byte 3

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Byte27 = 8E & Byte34 = X0 & Byte28 = 62/63/72/73 (CHK1B) (5/5)

	0	1	2	3	4	5	6	7
70	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
	Byte0	Byte1	Byte2	Byte3				
71	FCA::FCHK10							
	TLM read data parity error	PCI S error	Not used	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
72	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
73	FCA::FCHK10							
	TLM address counter parity error	ELM address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
74	QDTA::QDTASTS							
	Transfer end (A/64CMD)	Not used	(A/64CMD) Exec wait/ Executing	(A/64CMD) Data transferring	Transfer END B	Not used	Command B Exec wait/ Executing	Command B Data transferring
75	QDTA::QDTASTS							
	CHK2 occurred	CHK2 occurred at transferring	CHK2 in DRR controller	CHK2 in CACHE /CARB	Arbiter/ timer error	CHK1B occurred	Forceddata transferring end	Force error occurred
76	QDTA::DRERR							
	DRR control error	P0 control error	P1 control error	DRR DT error	P0 DT error	P1 DT error	ST0 CARB/ CMA error	ST1 CARB/ CMA error
77	QDTA::DRERR							
	P0 error INT	P1 error INT	DT error	Time over error	ST0 valid	ST1 valid	P0 use flag	P1 use flag
78	QDTA::ESTA9							
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
79	QDTA::ESTA9							
	Input DT0 parity error	Input DT0 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error
7A	QDTA::ESTAA							
	DRR M-ACS error	P0BF M-ACS error	P1BF M-ACS error	CHSN XR S-error	EXECA	ERRA	ERRB	ERRC
7B								
	Not used	Not used	Not used	Not used	Not used	Not used	System #1 FCA/QDTA error	System #0 FCA/QDTA error
7C	QDTA::P0EST0							
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	Not used	RD DEF SEQ ERR	Not used	Not used	WT DT-CNT P-ERR
7D	QDTA::P0EST0							
	WT DEF SEQ ERR	Not used	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	Not used
7E	QDTA::P1EST1							
	RX SEQ ERR	PRB RD-PNT P-ERR	RD DT-CNT P-ERR	Not used	RD DEF SEQ ERR	Not used	Not used	WT DT-CNT P-ERR
7F	QDTA::P1EST1							
	WT DEF SEQ ERR	Not used	PBF WAD-CNT P-ERR	PBF RAD-CNT P-ERR	Not used	Not used	Not used	Not used

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'62': FCA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
2D	Byte0	Byte1	Byte2	Byte3				
2E	FCA::FCHK10							
	TLM read data parity error	PCI S error	Not used	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
2F	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
30	FCA::FCHK10							
	TLM address counter parity error	ELM write address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
31	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
32	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
17	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'63': QDTA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	Not used							
2D	QDTA::ESTA9							
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
2E	QDTA::ESTA9							
	Input DT1 parity error	Input DT2 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error
2F	QDTA::ESTAA							
	DRB M-ACS error	P0 BUF M-ACS error	P1 BUF M-ACS error	CHSN XR SEQ error	EXEXA TRANSFER	ERR AT EXECA	ERR AT EXECB	ERR AT EXECC
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'72': FCA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	FCA::FCHK10							
	XR read data parity error				33MHz clock error	25MHz clock error	SEQ10 error	SEQ19 error
2D	Byte0	Byte1	Byte2	Byte3				
2E	FCA::FCHK10							
	TLM read data parity error	PCI S error	Not used	Diagnose CHK1 occurred	PCI Devsel timeout	PCI TLM read address counter parity error	PCI target abort	PCI target ready
2F	FCA::FCHK10							
	XR address parity error				XR write data parity error			
	Byte0	Byte1	Byte2	Byte3	Byte0	Byte1	Byte2	Byte3
30	FCA::FCHK10							
	TLM address counter parity error	ELM write address counter parity error	Not used	Not used	Not used	Not used	Not used	Not used
31	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
32	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
17	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Format 8, Message E (processor failure: DKA CHK1B)

	0	1	2	3	4	5	6	7
28	Format (x'8')				Message (x'E')			
29	Subcode x'73': QDTA CHK1B							
2A	MMC::CHK1BSTS							
	Not used	Not used	Not used	Not used	Not used	CHA CHK1B	MPA CHK1B	MMC CHK1B
2B	MMC::CHK1BSTS							
	FCA CHK1B	DTA CHK1B	Not used	Not used	Not used	Not used	RMC CHK1B	DRAM CHK1B
2C	Not used							
2D	QDTA::ESTA9							
	Write to unused register	Write to read-only register	Set A at CMD-A execute	Set B at CMD-B execute	Set C at 64CMD execute	Address2 parity error	Address3 parity error	Byte access error
2E	QDTA::ESTA9							
	Input DT1 parity error	Input DT2 parity error	Address DEC parity error	Output DT0 parity error	Output DT1 parity error	DRR4 clock phase error	CHSN4 clock phase error	CHSN6 clock phase error
2F	QDTA::ESTAA							
	DRB M-ACS error	P0 BUF M-ACS error	P1 BUF M-ACS error	CHSN XR SEQ error	EXEXA TRANSFER	ERR AT EXECA	ERR AT EXECB	ERR AT EXECC
30	MMC::MICCHK1STS							
	Not used	Not used	Not used	Not used	Not used	Not used	XR decoder error (3B0)	XR decoder error (3B1)
31	MMC::MICCHK1STS							
	Not used	Not used	MP CHK counter parity error	Parity error in MMC internal bus	MP reset counter parity error	Hard timer parity error	Wait timer parity error	Hold timer parity error
32	MMC::MICCHK1STS							
	Not used	Wait time-out	XR decoder error (2A)	Not used	Not used	XR address parity error	Local bus data parity error	XR data parity error

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Byte27 = 8E & Byte34 = X0 & Byte28 = F0 (Microprogram detected WCHK1) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘F0’)							
29	Hardware information (Micro information)							
31								
32	Module ID							
33	Routine ID							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Free area							
7F								

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Byte27 = 8E & Byte34 = X0 & Byte28 = F1 (Microprogram CHK1A) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Subcode (x‘F1’)							
29	Hardware information (See following pages)							
31								
32	Module ID (See following pages)							
33	Routine ID (See following pages)							
34	PCB number				Message code (x‘0’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)							
37	(This information is not fixed until DKC reports SSB to HOST.)							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40								
7F	Free area							

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Byte27 = 8E (Microprogram CHK1A) Byte28-31 Detail

(1) Byte32·33 = x‘165X’ : Microprogram simulated CHK1A for error recovery by REBOOT.

	0	1	2	3	4	5	6	7
28	Subcode : x‘F1’ : Microprogram CHK1A							
29	RCHK::ERADR							
	Address (0) from L bus							
2A	RCHK:: ERADR							
	Address (1) from L bus							
2B	RCHK:: ERADR							
	Address (2) from L bus							
2C	RCHK:: ERADR							
	Address (3) from L bus						Not used	Not used
2D	RCHK::LMADRLMT							
	Not used	Not used	Not used	Not used	Upper limit address of LM			
2E	RCHK::LMADRLMT							
	Upper limit address of LM mounting area (lower order)				Not used	Not used	Not used	Not used
2F	RCHK::ERSTS0							
	Not used	Not used	Not used	CHK1A cause detected	CHK1B cause detected	Scan→ LM/XR access error	DRAM control error	Not used
30	RCHK::SCANER							
	Scan→Uncorrectable error in LM		Not used	Scan→out of LM area	Not used	Scan→ Invalid write XR address	Not used	Not used
	Bank0	Bank1						
31	RCHK::CHK1ASTS							
	MPU UNCER	MMC FETCH UNCER	MPU WR PROT	MPU ADR OVER	Not used	Not used	OTHER WR PROT	OTHER ADR OVER

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Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (‘00’)							
29	DCN status							
	Force device busy	Channel connect request	Command chain execute	Path reserve	Stack status	Sense pending	Long Busy (Command process)	Processor connect
2A	DCN status							
	Single path mode	Gurant path mode	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	Garant path MP
2B	DCN flag							
	RST NTF/ RST ALG SSB PND	Pin Data pending	(RSV)	(RSV)	ODE pending	RSQ pending	SCI/SCE pending	PCH pending
2C	LCT initiation cause							
	0:Ready 1:Not ready	0:Disable 1:Enable	0:No SNS 1:64SNS pending	0:Mount 1:Not mount	0:No RST ALG LPN 1:Exist	0:No SYS RST LPN 1:Exist	0:No stack 1:Exist	0:No wait SNS 1:Exist
2D	LCT initiation cause							
	0:No wait-RI 1:Exist	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	0:Others 1:DEV BSY JOB

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Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (2/3)

	0	1	2	3	4	5	6	7
2E	Command interface flag							
	Pending exist	SCE(RSP)	(RSV)	(RSV)	ODE pending	RSQ pending	SCI pending	PCH pending
2F	Command code							
30	Internal SSB log number							
31								
32	Related reset detailed log number							
33								
34	PCB number				Message code (x'1')			
35	SSID (low) of self subsystem							
36	Symptom code (x'FF8E' : LDEV type = DKU87I/x'EF8E' : LDEV type = DKU86I)*							
37								
38	Log and message control (x'00')							
39	Program action code (x'00')							
3A	Configuration information							
3B								
3C	Not used (x'00')							
3D	Cylinder address							
3E								
3F	Head address							
40	Not used							
41	Not used							
42	Initialize interface information							
43								
44	Reset type code							
45								
46	1st reset type code							
47	Reset SSB type code							
48	Interrupt task code							
49	Self CHK1A difference code							
4A	Multi reset type code							
4B								
4C	Interrupted address							
4D								
4E								
4F								
50	Interrupted operation code							
51								
52								
53								
54	Current LDEV number							
55								
56	Current LPN number							
57								
58	Initiation cause code							
59								
5A	Command interface							
5B	DSB (from LCT)							
5C	sys status							
5D	REQ ID (from LCT)							
5E	JCB ID (from LCT)							
5F								
60	wchklmpbitmap (from LCT)							
61								
62								
63								

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 1 (Selective Reset) (3/3)

	0	1	2	3	4	5	6	7
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		EXITFLAG AREA						
6D								
6E								
6F								
70		DCN (wldcn1l)						
71								
72								
73								
74		DCN (wldcn2l)						
75								
76								
77								
78		RIW						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 3 (wait SENSE Timeout) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used (‘00’)							
29	LDEV#							
2A	24-byte format	Basic SSB			32-byte format	Basic SSB		
2B								
2C						Exception code		
2D		F/M						
2E		System error code				System error code		
2F								
30	Reset internal SSB number							
31								
32	Detail log number for RESET							
33								
34	PCB number				Message code (x‘3’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 3 (Wait SENSE Timeout) (2/2)

	0	1	2	3	4	5	6	7
40								
41		Not used						
42								
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56		LPN						
57								
58		Not used						
5F								
60								
61		Timeout SSB						
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 5 (CHK1B Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Related internal SSB log number							
29								
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Related RESET detail log number							
33								
34	PCB number				Message code (x‘5’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 5 (CHK1B Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN number						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 6 (DKC Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29								
2A								
2B								
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘6’)			
35	SSID (Low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 6 (DKC Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 7 (LCP Internal Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29	Not used							
2A	Internal Sel ective Reset cause							
2B								
2C	For Hotline	Old PSW			For INT SEL RST	LCP error code		
2D								
2E						x‘00’		
2F						x‘00’		
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘7’)			
35	SSID (Low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 7 (LCP Internal Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 8 (Force Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29	Not used							
2A	Not used							
2B	Not used							
2C	Old PSW							
2D								
2E								
2F								
30	Internal SSB log number (RESET)							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘8’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 8 (Foece Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8E & Byte34 : bit4-7 = 9 (Logical Inconsistency Reset) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	Internal SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘E’)			
28	Not used							
29								
2A								
2B								
2C	OLD PSW (Interruption source address)							
2D								
2E								
2F								
30	Internal SSB log number							
31								
32	Reset detail log number							
33								
34	PCB number				Message code (x‘9’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF8E’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8E & Byte34 : bit4-7 = 9 (Logical Inconsistency Reset) (2/2)

	0	1	2	3	4	5	6	7
40		Not used						
41		Not used						
42		Initialize interface information						
43								
44		Reset type code						
45								
46		1st reset type code						
47		Reset SSB type code						
48		Interrupt task code						
49		Self CHK1A difference code						
4A		Multi reset type code						
4B								
4C		Interrupted address						
4D								
4E								
4F								
50		Interrupted operation code						
51								
52								
53								
54		Current LDEV number						
55								
56		Current LPN						
57								
58		Initiation cause code						
59								
5A		Command interface						
5B		DSB (from LCT)						
5C		sys status						
5D		REQ ID (from LCT)						
5E		JCB ID (form LCT)						
5F								
60		wchklmpbitmap (from LCT)						
61								
62								
63								
64		jcb id						
65								
66		req id						
67		Job type code						
68		job status						
69		Executing processor number						
6A		Initiation cause code						
6B		Initiation detail code						
6C		Command code						
6D		Channel sequence						
6E		Reserved						
6F								
70		DCN						
⋮		⋮						
77								
78		DKCMAIN program counter						
79								
7A								
7B								
7C		SLV-DCN (slvdcnr)						
7D								
7E								
7F								

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Byte27 = 8F (Logical Inconsistency) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘8’)				Message (x‘F’)			
28	Module ID							
29	Routine ID							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number				Not used (x‘00’)			
35	SSID(low) of self subsystem							
36	Symptom code (x‘FF8F’ : LDEV type = DKU87I/x‘EF8E’ : LDEV type = DKU86I)*							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

* : This information is not fixed until DKC reports SSB to HOST.

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Byte27 = 8F (Logical Inconsistency) (2/2)

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Byte27 = 9F (Trace data/Log data) (1/2)

All of F/M = 9F SSB informations are no problem on DKC performance.

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘9’)				Message (x‘F’)			
28	Module ID (Note 3)							
29	Routine ID (Note 3)							
2A	Error information							
2B								
2C								
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number				Not used (x‘00’)			
35	SSID (low) of self subsystem							
36	Symptom code (x‘FF9F’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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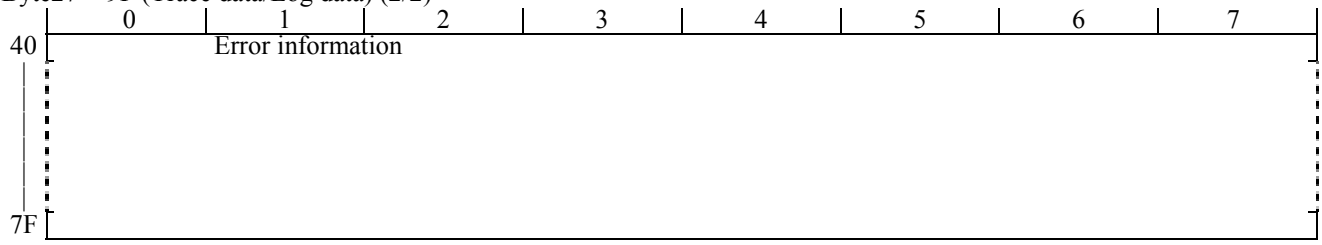
Byte27 = 9F (Trace data/Log data) (2/2)



(Note 1)

The pare of system error code x‘AE5A’ (Drive not Ready) and x‘A772’ are reported even when one of the following processes has completed successfully. These indicate the PDEV spin down executed correctly and do not mean the error condition. Please ignore them.

- PDEV replace
- DKU Inline execution at Installation or at PDEV expansion.

(Note 2)

System error code x‘AE5B’ (Unit Attention) is reported even after one of the following processes has completed successfully. It indicates the PDEV was reset correctly and does not mean the error condition. Please ignore it.

- DKA replace
- DKA expansion
- PDEV expansion
- DKA micro-program exchange
- PDEV micro-program exchange

(Note3)

The details information of every Module ID & Routine ID

•Module ID & Routine ID=0xC3A5 ; The Specified R-VOL of HRC is still Online from the HOST.
(Add Pair operation from the host was rejected)

Check the SSB.LOG on SVP of the specified MCU. SSB containing EC=C3A5 on the specified R-VOL number should be logged.

(1) Analyze the SSB.LOG

Refer to the case of Byte27=0X(X≠8/A) for the way of tracing an on-line host.
But, only the Byte position of BitMap information is different. Refer to Byte100(0x64)-103(0x67) of SSB for the BitMap information.

(Note 4)

System error code x‘507F’ is LOG which shows that the function of MODE277 is not effective. PS OFF/ON is required in order to confirm the function of MODE277.

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Byte27 = EC (Environment Monitor Detected DKC Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘E’)				Message (x‘C’)			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number (don’t care)				Message code (don’t care)			
35	SSID(low) of self subsystem (don’t care)							
36	Symptom code (x‘FFEC’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = EC (Environment Monitor Detected DKC Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code							
41	Error Component Code							
42	Error Reason Code							
43								
|	Not used							
7F								

(Note 1) Error Detection Code

Code	Detection
10	DKCMN1
20	DKCMN2
30	SSVP
00	SSVP

(Note 2) Error Component Code

Code	Component	Code	Component	Code	Component
10	Logic 1	D0	ACBOX-R10	E2	DKC AcBox1(30A)
11	Logic 2	D1	ACBOX-R11	E3	DKC AcBox2(30A)
A0	DKCMN1	D2	ACBOX-R10(30A)		
A1	DKCMN2	D3	ACBOX-R11(30A)		
A2	SSVP	E0	DKC AcBox1		
A3	CE Panel	E1	DKC AcBox2		

(Note 3) Error Reason Code

Code	Reason
10	Abnormal temperature (over60°C) is detected in the front side.
11	Abnormal temperature (over60°C) is detected in the back side.
12	Abnormal temperature (over45°C) is detected in the front side.
13	Abnormal temperature (over45°C) is detected in the back side.
20	5V voltage has dropped below 80%.
21	3V voltage has dropped below 80%.
22	12V voltage has dropped below 80%.
30	Voltage for shared memory has dropped below 80%.
31	Voltage for cache memory has dropped below 80%.
35	12V voltage warning.
40	5/3VPS A box abnormality has been detected.
41	5/3VPS B box abnormality has been detected.
42	3VPS A box abnormality has been detected.
43	3VPS B box abnormality has been detected.
44	3VPS C box abnormality has been detected.
45	3VPS D box abnormality has been detected.
46	SUB PS box abnormality has been detected.
50	Battery0 or BATT-CTR0 abnormality has been detected.
51	Battery1 or BATT-CTR1 abnormality has been detected.
52	Battery2 or BATT-CTR2 abnormality has been detected.
5A	Battery0 abnormality has been detected. (DIAG)
5B	Battery1 abnormality has been detected. (DIAG)
5C	Battery2 abnormality has been detected. (DIAG)
60	AC power off/interruption of breaker box occurred.

(Continue)

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Code	Reason
70	Low rotation speed of FLGFAN12B has been detected when Error Detection Code 1 is 10.
70	Low rotation speed of FLGFAN21B has been detected when Error Detection Code 1 is 11.
71	Low rotation speed of FLGFAN12A has been detected when Error Detection Code 1 is 10.
71	Low rotation speed of FLGFAN21A has been detected when Error Detection Code 1 is 11.
72	Low rotation speed of FLGFAN11B has been detected when Error Detection Code 1 is 10.
72	Low rotation speed of FLGFAN22B has been detected when Error Detection Code 1 is 11.
73	Low rotation speed of FLGFAN11A has been detected when Error Detection Code 1 is 10.
73	Low rotation speed of FLGFAN22A has been detected when Error Detection Code 1 is 11.
74	Low rotation speed of RLGFAN11B has been detected when Error Detection Code 1 is 10.
74	Low rotation speed of RLGFAN22B has been detected when Error Detection Code 1 is 11.
75	Low rotation speed of RLGFAN11A has been detected when Error Detection Code 1 is 10.
75	Low rotation speed of RLGFAN22A has been detected when Error Detection Code 1 is 11.
76	Low rotation speed of RLGFAN12B has been detected when Error Detection Code 1 is 10.
76	Low rotation speed of RLGFAN21B has been detected when Error Detection Code 1 is 11.
77	Low rotation speed of RLGFAN12A has been detected when Error Detection Code 1 is 10.
77	Low rotation speed of RLGFAN21A has been detected when Error Detection Code 1 is 11.
78	Low rotation speed of RPSFAN11B has been detected when Error Detection Code 1 is 10.
78	Low rotation speed of RPSFAN22B has been detected when Error Detection Code 1 is 11.
79	Low rotation speed of RPSFAN11A has been detected when Error Detection Code 1 is 10.
79	Low rotation speed of RPSFAN22A has been detected when Error Detection Code 1 is 11.
7A	Low rotation speed of RPSFAN12B has been detected when Error Detection Code 1 is 10.
7A	Low rotation speed of RPSFAN21B has been detected when Error Detection Code 1 is 11.
7B	Low rotation speed of RPSFAN12A has been detected when Error Detection Code 1 is 10.
7B	Low rotation speed of RPSFAN21A has been detected when Error Detection Code 1 is 11.
7C	Low rotation speed of FPSFAN11B has been detected when Error Detection Code 1 is 10.
7C	Low rotation speed of FPSFAN21B has been detected when Error Detection Code 1 is 11.
7D	Low rotation speed of FPSFAN11A has been detected when Error Detection Code 1 is 10.
7D	Low rotation speed of FPSFAN21A has been detected when Error Detection Code 1 is 11.
7E	Low rotation speed of FPSFAN12B has been detected when Error Detection Code 1 is 10.
7E	Low rotation speed of FPSFAN22B has been detected when Error Detection Code 1 is 11.
7F	Low rotation speed of FPSFAN12A has been detected when Error Detection Code 1 is 10.
7F	Low rotation speed of FPSFAN22A has been detected when Error Detection Code 1 is 11.
80	JP for voltage control.
81	JP for DKC ALARM remains.
85	JP for SVP PS INH remains.
90	Environment monitor register access error.
91	Environment monitor register BUSY error.
92	Battery diagnostic mode setting failure.
93	DKCMN Type unmatched.
98	MPS P/S On error
99	MPS P/S On error
A0	An environment monitors alarm disagreement..
A1	An environment monitors P/S On disagreement.
A2	An environment monitors P/S Off disagreement.
E0	SVP P/S abnormal.
E1	SVP P/S Box input abnormal.
E2	SVP P/S Box output abnormal.
E3	Duplex SVP Setup fail.

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Byte27 = EE (Environment Monitor Detected DKU Failure) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘E’)				Message (x‘E’)			
28	Error detection code (Note 1)							
29	Error detection code (Note 2)							
2A	Error reason code (Note 3)							
2B								
2C	Reserved area							
2D								
2E								
2F								
30								
31								
32								
33								
34	PCB number (don’t care)				Message code (don’t care)			
35	SSID(low) of self subsystem (don’t care)							
36	Symptom code (x‘FFEC’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = EE (Environment Monitor Detected DKU Failure) (2/2)

	0	1	2	3	4	5	6	7
40	Error Detection Code(Note 1)							
41	Error Component Code(Note 2)							
42	Error Reason Code(Note 3)							
43								
|	Not used							
7F								

(Note 1) Error Detection Code

Code	Detection	Code	Detection	Code	Detection	Code	Detection
10	DKCMN1	40	DKA-1B	80	HDU-0 FSWXXX-L1	C0	HDU-4 FSWXXX-L1
20	DKCMN2	41	DKA-1C	81	HDU-0 FSWXXX-R1	C1	HDU-4 FSWXXX-R1
1A	DKCMN1	42	DKA-1D	82	HDU-0 FSWXXX-L2	C2	HDU-4 FSWXXX-L2
2A	DKCMN2	43	DKA-1E	83	HDU-0 FSWXXX-R2	C3	HDU-4 FSWXXX-R2
11	DKUMN-R1F	44	DKA-2H	90	HDU-1 FSWXXX-L1	D0	HDU-5 FSWXXX-L1
21	DKUMN-R1R	45	DKA-2J	91	HDU-1 FSWXXX-R1	D1	HDU-5 FSWXXX-R1
12	DKUMN-R2F	46	DKA-2K	92	HDU-1 FSWXXX-L2	D2	HDU-5 FSWXXX-L2
22	DKUMN-R2R	47	DKA-2L	93	HDU-1 FSWXXX-R2	D3	HDU-5 FSWXXX-R2
15	DKUMN-L1F			A0	HDU-2 FSWXXX-L1	E0	HDU-6 FSWXXX-L1
25	DKUMN-L1R			A1	HDU-2 FSWXXX-R1	E1	HDU-6 FSWXXX-R1
16	DKUMN-L2F			A2	HDU-2 FSWXXX-L2	E2	HDU-6 FSWXXX-L2
26	DKUMN-L2R			A3	HDU-2 FSWXXX-R2	E3	HDU-6 FSWXXX-R2
30	SSVP			B0	HDU-3 FSWXXX-L1	F0	HDU-7 FSWXXX-L1
				B1	HDU-3 FSWXXX-R1	F1	HDU-7 FSWXXX-R1
				B2	HDU-3 FSWXXX-L2	F2	HDU-7 FSWXXX-L2
				B3	HDU-3 FSWXXX-R2	F3	HDU-7 FSWXXX-R2

(Note 2) Error Component Code

Code	Component	Code	Component	Code	Component	Code	Component
10	Logic 1	40	HDU-R20	A0	DKCMN1	B0	DKUMN-R1F (DKUMN1)
11	Logic 2	41	HDU-R21	A1	DKCMN2	B1	DKUMN-R1R (DKUMN2)
20	HDU-R10(HDU-0)	42	HDU-R22	A2	SSVP	B2	DKUMN-L1F
21	HDU-R11(HDU-1)	43	HDU-R23	A3	CE Panel	B3	DKUMN-L1R
22	HDU-R12(HDU-2)	44	HDU-R24	A8	DKA-1B	B4	DKUMN-R2F
23	HDU-R13(HDU-3)	45	HDU-R25	A9	DKA-1C	B5	DKUMN-R2R
24	HDU-R14	46	HDU-R26	AA	DKA-1D	B6	DKUMN-L2F
25	HDU-R15	47	HDU-R27	AB	DKA-1E	B7	DKUMN-L2R
26	HDU-R16	50	HDU-L20	AC	DKA-2H	B8	DKUMN-R3F
27	HDU-R17	51	HDU-L21	AD	DKA-2J	B9	DKUMN-R3R
30	HDU-L10	52	HDU-L22	AE	DKA-2K	BA	DKUMN-L3F
31	HDU-L11	53	HDU-L23	AF	DKA-2L	BB	DKUMN-L3R
32	HDU-L12	54	HDU-L24			D0	ACBOX-R10
33	HDU-L13	55	HDU-L25			D1	ACBOX-R11
34	HDU-L14	56	HDU-L26			D2	ACBOX-R10(30A)
35	HDU-L15	57	HDU-L27			D3	ACBOX-R11(30A)
36	HDU-L16					E0	DKC AcBox1
37	HDU-L17					E1	DKC AcBox2
						E2	DKC AcBox1(30A)
						E3	DKC AcBox2(30A)

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(Note 3) Error Reason Code

Code	Reason
22	DKU AC/DC alarm
4A	HDU MPS-0 abnormality has been detected.
4B	HDU MPS-1 abnormality has been detected.
70	Low rotation speed of FAN has been detected.
83	JP for HDU-0-HDU-3 voltage alarm inhibit remains
84	JP for HDU-4-HDU-7 voltage alarm inhibit remains
90	Environment monitor register access error.
94	FSW access error. FSWXXX-R1
95	FSW access error. FSWXXX-L1
96	FSW access error. FSWXXX-R2
97	FSW access error. FSWXXX-L2
98	PS/ON signal abnormal. (CL-1)
99	PS/ON signal abnormal. (CL-2)
A0	An environment monitors alarm disagreement..
A4	a FSW alarm disagreement. (FSWXXX-R1)
A5	a FSW alarm disagreement. (FSWXXX-L1)
A6	a FSW alarm disagreement. (FSWXXX-R2)
A7	a FSW alarm disagreement. (FSWXXX-L2)
C0	FSW fuse blow. (FSWXXX-R1)
C1	FSW fuse blow. (FSWXXX-L1)
C2	FSW fuse blow. (FSWXXX-R2)
C3	FSW fuse blow. (FSWXXX-L2)
C4	JMP P/K fuse blow. (FSWXXX-R1)
C5	JMP P/K fuse blow. (FSWXXX-L1)
C6	JMP P/K fuse blow. (FSWXXX-R2)
C7	JMP P/K fuse blow. (FSWXXX-L2)

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Byte27 = F0 (Operation Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low)							
26	Cylinder address (high)				Head address			
27	Format (x‘F’)				Message (x‘E’)			
28	Not used (x‘00’)							
29	Not used (x‘00’)							
2A	Not used (x‘00’)							
2B	Hardware level (Note 1)							
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Not used (x‘00’)							
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF0’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘1D’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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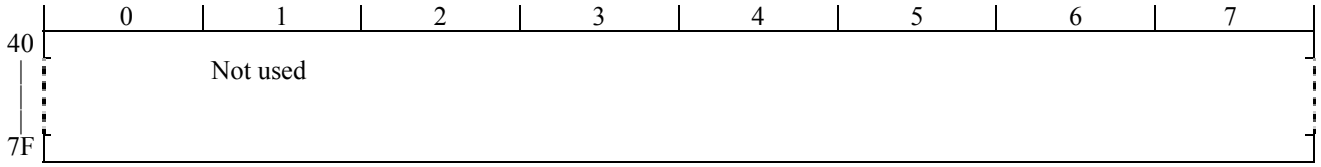
Byte27 = F0 (Operation Terminated) (2/2)



(Note 1) Hardware level

Bit0 : Hardware level flag

For bit0=0

Bit 1	: Not used
Bit 2 ~ 3	: SP number
Bit 4 ~ 5	: CHLs per Cluster
	00 : 4
	01 : 8
	10 : Not used
	11 : Not used
Bit 6	: NVS
	0 : Without NVS
	1 : With NVS
Bit 7	: Not used
Bit 8 ~ 10	: Cache size
	000 : Non cache
	001 : 256MB
	010 : 512MB
	011 : 768MB
	100 : 1024MP
	101 : 1280MP
	110 : 1536MP
	111 : Over 1536MB
Bit11 ~ 13	: Cluster hardware level
Bit14 ~ 15	: Cache/NVS hardware level

For bit0=1

Bit 1	: Not used
Bit 2 ~ 3	: SP number
Bit 4 ~ 5	: CHLs per Cluster
	0000 : Parallel=4, Serial=0
	0001 : Parallel=8, Serial=0
	0010 : Parallel=4, Serial=2
	0100 : Parallel=4, Serial=4
	0110 : Parallel=0, Serial=2
	1000 : Parallel=0, Serial=4
	1010 : Parallel=0, Serial=8
	1100 : Parallel=0, Serial=8
Bit 8	: DUAL FRAME
	0 : DUAL FRAME
	1 : MODULAR POWER
Bit 9 ~ 11	: Cache size
	000 : Non cache
	001 : 256MB
	010 : 512MB
	011 : 768MB
	100 : 1024MB
	101 : 1280MB
	110 : 1536MB
	111 : Over 1536MB
Bit12 ~ 13	: Cluster hardware level
Bit14 ~ 15	: Cache/NVS hardware level

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Byte27 = F1 (Micro-program Detected Cache Failure) (1/2)

	0	1	2	3	4	5	6	7	
00	Time stamp								
05									
06	Format Message								
07	PCB type		Processor ID (Note)						
08	System error code								
09									
0A	JCB ID								
0B									
0C	REQ ID								
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log	
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0	
0F	SEMI-SYNC	RCU SIM	0	0	RCU#				
10	LDEV number								
11									
12	CDEV#								
13	RDEV#								
14	RCU LDEV number								
15									
16	SSB log number								
17									
18	Related failure log number								
19									
1A	Related SIM log number								
1B									
1C	Related SSB log number								
1D									
1E	(Reserved)								
1F	SCB								
20	Basic SSB								
21									
22									
23	Count								
24	Device address								
25	Cylinder address (low)								
26	Cylinder address (high)				Head address				
27	Format (x‘F’)				Message (x‘1’)				
28	Queue transition in progress (Side A)	Queue transition in progress (Side B)	Free SGCB queue operation in progress	Free SLCB queue operation in progress	Free GRPT queue operation in progress	Not used			
29	Not used								*
	VDEV number								*
2A	Queue type								*
	VDEV number		Slot number						*
2B	Queue number								*
	Slot number								*
2C	Queue number								*
	Slot number								*
2D	SSID of mate subsystem (x‘0000’ for EDCC)								
2E									
2F	Maker code & Manufacture code (x‘00’)								
30	Not used (x‘00’)								

* : When byte 28, bit2-4 = 000, upper value is valid.
: When byte 28, bit2-4 ≠ 000, lower value is valid.

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Byte27 = F1 (Micro-program Detected Cache Failure) (2/2)

	0	1	2	3	4	5	6	7
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF1’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Error information							
7F								

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Byte27 = F2 (CACHE CHK2)

	0	1	2	3	4	5	6	7
00	Time Stamp							
|								
05								
06	Format Message							
07	P/K Type		Processor ID					
08	System Error Code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	HOST Report	SVP Report	Force Log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	PORT#		RCU#			
10	LDEV#							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV#							
15								
16	Internal SSB Log Number							
17								
18	Related Failure Log Number							
19								
1A	Related SIM Log Number							
1B								
1C	Related SSB Log Number							
1D								
1E	(Reserved)							
1F	SCB							
20	Inf valid	Err Code						
21	Segment Number							
22	Filemark	ECM	ILI	Reserved	Sense Key			
23	Information Bytes							
24								
25								
26								
27	Format (x‘F’)				Message (x‘2’)			
28	SubCode							
29	Detail Information (See Following Pages.)							
|								
2C								
2D	SSID for Other Subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker Code						Factory Code	
30	Detail Information (See Following Pages.)							
31	Module ID							
32	Routine ID							
33	P/K ID				Err Code (Don’t Care)			
34	SSID for Self Subsystem							
35								
36	Symptom Code (x‘FF89’:LDEV Type=DKU87I / x‘EF89’: LDEV Type=DKU86I)							
37								
38	Log and Message Control (x‘00’)							
39	Program Action Control (x‘00’)							
3A	Configuration Information							
3B								
3C	Not Used							
3D	Cylinder Address							
3E								
3F	Head Address							
40	Detail Information (See Following Pages.)							
|								
7F								

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Byte27 = F2 (CACHE CHK2) Byte28-31 Detail

	0	1	2	3	4	5	6	7
28	SubCode							
	Error Detected: ‘1’ = P PATH ERR(DTA) ‘2’ = P or C PATH ERR(DTA) ‘3’ = P PATH ERR(CSW) ‘4’ = P or C PATH ERR(CSW) ‘5’ = C PATH ERR(CSW) ‘7’ = C PATH ERR(CMA) ‘8’ = CACHE BOARD ERR ‘9’ = CACHE MEMORY ERR				CARB BOARD ERR ‘0’ = NO ‘1’ = YES	CMA BOARD ERR ‘0’ = NO ‘1’ = YES	CARB REG LOG RESULT ‘0’ = OK ‘1’ = NG	CMA REG LOG RESULT ‘0’ = OK ‘1’ = NG
29	Transfer Information							
	Transfer P/K Type and Master Path ‘0’ = ESCON CHA, ‘1’= FICON CHA ‘3’ = FIBRE CHA(PMA), ‘4’ = FIBRE CHA(DMA0) ‘5’ = FIBRE CHA(DMA1) ‘6’ = FIBRE DKA(FCA0), ‘7’ = FIBRE DKA(FCA1) ‘8’ = FIBRE DKA(DRR) ‘A’ = ENAS CHA(DMA0/2), ‘B’=ENAS CHA(DMA1/3)				Transfer Mode ‘0’ = NORMAL WRITE ‘1’ = NORMAL READ ‘2’ = 2SLAVE WRITE ‘3’ = CACHE COPY(CtoC) ‘4’ = CACHE COPY(CinC)			
2A	Using Path Code							
	XFR P PATH# ‘0’ = P#0 ‘1’ = P#1	SLAVE#1 CACHE P/K# (‘0’ - ‘3’)		SLAVE#1 CMA# (‘0’ - ‘1’)	LOG P PATH# ‘0’=ORIGIN ‘1’=OTHER	SLAVE#2 CACHE P/K# (‘0’ - ‘3’)		SLAVE#2 CMA# (‘0’ - ‘1’)
2B	STATUS0(SLAVE 1) byte0							
	STATUS0 ERR	STATUS0 CARB ERR	STATUS0 CMA ERR	STATUS0 CMA STATUS ID ERR	STATUS0 CMA STATUS NG	STATUS0 CMA FIFO MODE	STATUS0 CMA WARNING	STATUS0 CARB UNINITIAL
2C	STATUS1(SLAVE 2) byte0							
	STATUS1 ERR	STATUS1 CARB ERR	STATUS1 CMA ERR	STATUS1 CMA STATUS ID ERR	STATUS1 CMA STATUS NG	STATUS1 CMA FIFO MODE	STATUS1 CMA WARNING	STATUS1 CARB UNINITIAL

30	STATUS0(SLAVE 1) byte1				
	STATUS0 Reserved	STATUS0 PATH ID#	STATUS0 CMA UNINITIAL	STATUS0 Answer CACHE P/K#	STATUS0 Answer CMA#

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B		CMA::MEMADLOG450CAS						
	(RSV)	Error Access BA Address		Error Access CAS Address (High)				
5C		CMA::MEMADLOG450CAS						
		Error Access CAS Address (Low)						
5D		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR1							
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WT CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRAN CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61	CARB::MixREG							
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO END CODE ERR	Pn FIFO SLRC ERR	(RSV)
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	CHA::CNFSN0							
	(RSV)	PKID#			FORCE PATHSEL	(RSV)	BFRTN	PATHX
6B	CHA::LPEN							
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE
6C	Reserved							
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
6D	CHA::MONITOR							
	MODE_1F	XCLM_2F	(RSV)	(RSV)	(RSV)	P0 SYNC ERR	P1 SYNC ERR	P2 SYNC ERR
6E	CMA::LASTXFRPATH / IMPZREF0							
	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	(RSV)	(RSV)	IMP Setting VALID
6F	CHA::IMPZREF0							
	IMP Setting Value for HIGH-LEVEL of LSI_UP Side				IMP Setting Value for LOW-LEVEL of LSI_UP Side			

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(1) Byte29 bit0 - 3 = 0 and Byte31 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70		CHA_CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
71		CHA_CHK2ASTS						
	P0 Receive PARITY ERR	P1 Receive PARITY ERR	X0 Receive PARITY ERR	X1 Receive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
72		CHA_CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
73		CHA_CHK2ASTS						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74		CHA_CHK2CSTS						
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
75		CHA_CHK2CSTS						
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	(RSV)	(RSV)	STATUS0 PKID ERR	STATUS1 PKID ERR
76		CHA_CHK2CSTS						
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
77		CHA_CHK2CSTS						
	X1 Send PARITY ERR	STATUS0 CARB PARITY ERR	STATUS0 CMA PARITY ERR	STATUS1 CARB PARITY ERR	STATUS1 CMA PARITY ERR	(RSV)	(RSV)	(RSV)
78		CHA_CHK2DSTS						
	STATUS0 ERR ON	STATUS1 ERR ON	CARB ERRINT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
79		CHA_MCSA00						
		Slave 1 Cache Transfet Address (BYTE0)						
7A		CHA_MCSA10						
		Slave 2 Cache Transfet Address (BYTE0)						
7B		CHA::CSPGR						
	Slave 1 REG ACCESS FLAG	Slave 1 CARB ACCESS FLAG	(RSV)	(RSV)	Slave 2 REG ACCESS FLAG	Slave 2 CARB ACCESS FLAG	(RSV)	(RSV)
7C		CHA_PCMD2						
	(RSV)	PK ID			Transfer Command			
7D		CHA::XFC0 / XFS0						
		Data Transfer Path			CHK2A	CHK2B	CHK2C	CHK2D
7E		CHA_CHK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNMENT ERR
7F		CHA_CHK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 1 and Byte31 = 58/59 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 1 and Byte31 = 58/59 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B		CMA::MEMADLOG450CAS						
	(RSV)	Error Access BA Address		Error Access CAS Address (High)				
5C		CMA::MEMADLOG450CAS						
		Error Access CAS Address (Low)						
5D		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 1 and Byte31 = 58/59 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR1							
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WT CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRAN CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61	CARB::MixREG							
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO END CODE ERR	Pn FIFO SLRC ERR	(RSV)
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	CHA::LPEN							
	C PATH#01 ENABLE	C PATH#03 ENABLE	C PATH#05 ENABLE	C PATH#07 ENABLE	C PATH#11 ENABLE	C PATH#13 ENABLE	C PATH#15 ENABLE	C PATH#17 ENABLE
6B	CHA::LPEN							
	C PATH#00 ENABLE	C PATH#02 ENABLE	C PATH#04 ENABLE	C PATH#06 ENABLE	C PATH#10 ENABLE	C PATH#12 ENABLE	C PATH#14 ENABLE	C PATH#16 ENABLE
6C	CHA::IMPZREF0							
	IMP Setting VALID	(RSV)	(RSV)	IMP Setting Value for HIGH-LEVEL of LSI_UP Side				
6D	CHA::MONITOR							
	MODE_1F	XCLM_2F	(RSV)	(RSV)	(RSV)	P0 SYNC ERR	P1 SYNC ERR	P2 SYNC ERR
6E	CMA::LASTXFRPATH / CNFSN0							
	(RSV)	(RSV)	P0 USE FLAG	P1 USE FLAG	(RSV)	PKID#		
6F	CHA::IMPZREF0							
	(RSV)	(RSV)	(RSV)	IMP Setting Value for LOW-LEVEL of LSI_UP Side				

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(2) Byte29 bit0 - 3 = 1 and Byte31 = 58/59 (4/4)

	0	1	2	3	4	5	6	7
70		CHA_CHK2ASTS						
	WRBF RD ADR PNT PARITY ERR	RDBF WT ADR PNT PARITY ERR	SC CNT PARITY ERR	LOS CNT PARITY ERR	HARD TIMER PARITY ERR	WRBF PLRC ERR	HSN ADR PARITY ERR	WRBF OUT DT PARITY ERR
71		CHA_CHK2ASTS						
	P0 Receive PARITY ERR	P1 Receive PARITY ERR	X0 Receive PARITY ERR	X1 Receive PARITY ERR	ADRM PARITY ERR	ADRS PARITY ERR	ADRP PARITY ERR	CMD PARITY ERR
72		CHA_CHK2ASTS						
	XFR CNT PARITY ERR	ILPRM0	ILPRM1	ILPRM2	ILPRM3	ILPRM4	ILPRM5	ILPRM6
73		CHA_CHK2ASTS						
	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
74		CHA_CHK2CSTS						
	TIME OUT0	TIME OUT1	TIME OUT2	HSN RD PLRC ERR	STATUS0 PLRC ERR	STATUS1 PLRC ERR	HSN RD PLRC-INV ERR	STATUS0 PLRC ERR
75		CHA_CHK2CSTS						
	STATUS1 PLRC ERR	HSN RD END-CODE ERR	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	(RSV)	(RSV)	STATUS0 PKID ERR	STATUS1 PKID ERR
76		CHA_CHK2CSTS						
	STATUS0 BYTE0/1 ERR	STATUS1 BYTE0/1 ERR	ACK ERR	ERRINT	LOS	P0 Send PARITY ERR	P1 Send PARITY ERR	X0 Send PARITY ERR
77		CHA_CHK2CSTS						
	X1 Send PARITY ERR	STATUS0 CARB PARITY ERR	STATUS0 CMA PARITY ERR	STATUS1 CARB PARITY ERR	STATUS1 CMA PARITY ERR	(RSV)	(RSV)	(RSV)
78		CHA_CHK2DSTS						
	STATUS0 ERR ON	STATUS1 ERR ON	CARB ERRINT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
79		CHA_MCSA00						
		Slave 1 Cache Transfet Address (BYTE0)						
7A		CHA_MCSA10						
		Slave 2 Cache Transfet Address (BYTE0)						
7B		CHA::CSPGR						
	Slave 1 REG ACCESS FLAG	Slave 1 CARB ACCESS FLAG	(RSV)	(RSV)	Slave 2 REG ACCESS FLAG	Slave 2 CARB ACCESS FLAG	(RSV)	(RSV)
7C		CHA_PCMD2						
	(RSV)	PK ID			Transfer Command			
7D		CHA::XFC0 / XFS0						
		Data Transfer Path			CHK2A	CHK2B	CHK2C	CHK2D
7E		CHA_CHK2AST0						
	RDBF PLRC ERR	SLRC ERR	LA ERR	CBUF DT PARITY ERR	SEARCH ERR	SEARCH DT ERR	WRBF INPUT DT PARITY ERR	BYTE ALIGNMENT ERR
7F		CHA_CHK2AST0						
	LCM OUTPUT DT PARITY ERR	(RSV)	LA PARITY ERR	RDBF OUTPUT DT PARITY ERR	HSN PACKET LEN PARITY ERR	(RSV)	(RSV)	(RSV)

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(3) Byte29 bit0 - 3 = 0,1 and Byte31 ≠ 58/59 and Byte42 = 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		VDEV and slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		Information of Micro Program						
4D								
4E								
4F								
50		Internal Siearch Parameter (Cylinder number)						
51								
52		Internal Siearch Parameter (Head number)						
53		Internal Siearch Parameter (Reacord number)						
54		Information of Micro Program						
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C		Record number in CBUF						
7D		Key Length in CBUF						
7E		Data Length in CBUF						
7F								

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(4) Byte29 bit0 - 3 = 0,1 and Byte31 ≠ 58/59 and Byte42 ≠ 58/59

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		Information of Micro Program						
45								
46								
47								
48								
49								
4A								
4B								
4C								
4D								
4E								
4F								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E		Curent Command Code						
5F		Old Command Code						
60		Information of Micro Program						
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(5) Byte29 bit0 - 3 = 4 or 5 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(5) Byte29 bit0 - 3 = 4 or 5 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B		CMA::MEMADLOG450CAS						
	(RSV)	Error Access BA Address		Error Access CAS Address (High)				
5C		CMA::MEMADLOG450CAS						
		Error Access CAS Address (Low)						
5D		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(5) Byte29 bit0 - 3 = 4 or 5 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR1							
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WT CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRAN CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61	CARB::MixREG							
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO END CODE ERR	Pn FIFO SLRC ERR	(RSV)
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	FDTA/M::HADR1UCNT							
	Slave 1 Cache Transfer Address (BYTE0)							
6B	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE1)							
6C	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE2)							
6D	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE3)							
6E	FDTA/M::HADR1LCNT							
	Slave 1 Cache Transfer Address (BYTE4)							
6F	FDTA/M::HADR2UCNT							
	Slave 2 Cache Transfer Address (BYTE0)							

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(5) Byte29 bit0 - 3 = 4 or 5 (4/4)

	0	1	2	3	4	5	6	7
70		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE1)						
71		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE2)						
72		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE3)						
73		FDTA/M::HADR2LCNT						
		Slave 2 Cache Transfer Address (BYTE4)						
74		FDTA/M::HCMD						
		Cache Transfer Command (BYTE0)						
75		FDTA/M::HCMD						
		Cache Transfer Command (BYTE1)						
76		FDTA/M::HxCHK2AST0						
	TX1 ERRINT	TX2 ERRINT	RX ERRINT	TX1 ERREND	TX2 ERREND	RX ERREND	PACK OFF ERR	HSNRDT PARITY ERR
77		FDTA/M::HxCHK2AST0						
	TX1 ENT LOOP BACK ERR	TX2 ENT LOOP BACK ERR	RX ENT LOOP BACK ERR	PRB PARITY ERR	(RSV)	(RSV)	RX PLRC PARITY ERR	RX LRC PARITY ERR
78		FDTA/M::HxCHK2AST0						
	(RSV)	(RSV)	TX1 TIME OUT	(RSV)	TX2 TIME OUT 0	TX2 TIME OUT 1	RX TIME OUT 0	RX TIME OUT 1
79		FDTA/M::HCHK2AST1						
	STATUS1 END-CODE ERR0	STATUS1 END-CODE ERR1	STATUS1 END-CODE ERR2	STATUS1 END-CODE ERR3	STATUS1 INV-PLRC ERR0	STATUS1 INV-PLRC ERR1	STATUS1 CMP ERR0	STATUS1 CMP ERR1
7A		FDTA/M::HCHK2AST1						
	P0 USE FLG	P1 USE FLG	HSN STATUS FLG	STATUS1 PARITY ERR	(RSV)	STATUS1 PLRC ERR0	STATUS1 PLRC ERR1	STATUS1 PKID ERR
7B		FDTA/M::HCHK2AST2						
	STATUS2 END-CODE ERR0	STATUS2 END-CODE ERR1	STATUS2 END-CODE ERR2	STATUS2 END-CODE ERR3	STATUS2 INV-PLRC ERR0	STATUS2 INV-PLRC ERR1	STATUS2 CMP ERR0	STATUS2 CMP ERR1
7C		FDTA/M::HCHK2AST2						
	(RSV)	(RSV)	HSN STATUS FLG	STATUS2 PARITY ERR	(RSV)	STATUS2 PLRC ERR0	STATUS2 PLRC ERR1	STATUS2 PKID ERR
7D		FDTA/M::HCHK2CST2						
	(RSV)	(RSV)	PNTR0 PARITY ERR	PNTR1 PARITY ERR 0	SYNC CMP ERR0	SYNC CMP ERR1	SYNC CMP ERR2	SYNC CMP ERR3
7E		FDTA/M::CBEN						
	C PATH#00 ENABLE	C PATH#01 ENABLE	C PATH#02 ENABLE	C PATH#03 ENABLE	C PATH#04 ENABLE	C PATH#05 ENABLE	C PATH#06 ENABLE	C PATH#07 ENABLE
7F		FDTA/M::CBEN						
	C PATH#10 ENABLE	C PATH#11 ENABLE	C PATH#12 ENABLE	C PATH#13 ENABLE	C PATH#14 ENABLE	C PATH#15 ENABLE	C PATH#16 ENABLE	C PATH#17 ENABLE

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(6) Byte29 bit0 - 3 = 6 or 7 (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(SLAVE 2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41	STATUS0(SLAVE 1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(SLAVE 1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43	STATUS0(SLAVE 1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(SLAVE 1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(SLAVE 2) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(SLAVE 2) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47	STATUS0(SLAVE 2) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(SLAVE 2) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(6) Byte29 bit0 - 3 = 6 or 7 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B		CMA::MEMADLOG450CAS						
	(RSV)	Error Access BA Address		Error Access CAS Address (High)				
5C		CMA::MEMADLOG450CAS						
		Error Access CAS Address (Low)						
5D		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(6) Byte29 bit0 - 3 = 6 or 7 (3/4)

	0	1	2	3	4	5	6	7
60	CARB::PnERR1							
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WT CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRAN CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61	CARB::MixREG							
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO END CODE ERR	Pn FIFO SLRC ERR	(RSV)
62	CARB::CxERR0							
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63	CARB::CxERR0							
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64	CARB::CxERR1							
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65	CARB::CxERR1							
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66	CARB::CyERR0							
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67	CARB::CyERR0							
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68	CARB::CyERR1							
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69	CARB::CxERR1							
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A	FCA::CHK2F40							
	BBUF OUT DATA PARITY ERR	CC2 SLRC ERR	SLV0 STS PATH ID ERR	SLV1 STS PATH ID ERR	CC3 SLRC ERR	CC3 DATA PLRC0 ERR	CC3 DATA PLRC1 ERR	CC3 DATA INV-PLRC0 ERR
6B	FCA::CHK2F40							
	CC3 INV-PLRC1 ERR	CC3 DATA ENDCODE ERR	CC4 SLRC ERR	SLV0 STS PLRC0 ERR	SLV0 STS PLRC1 ERR	SLV0 STS INV-PLRC0 ERR	SLV0 STS INV-PLRC1 ERR	SLV1 STS PLRC0 ERR
6C	FCA::CHK2F40							
	SLV1 STS PLRC1 ERR	SLV1 STS INV-PLRC0 ERR	SLV1 STS INV-PLRC1 ERR	SLV0 STS ENDCODE ERR	SLV1 STS ENDCODE ERR	SLV0 STS ANY ERR	SLV1 STS ANY ERR	QDTA STS ANY ERR
6D	FCA::CHK2F40							
	DTN TX BUF0A PARITY ERR	DTN TX BUF1A PARITY ERR	DTN TX BUF2A PARITY ERR	DTN TX BUF3A PARITY ERR	DTN TX BUF0B PARITY ERR	DTN TX BUF1B PARITY ERR	DTN TX BUF2B PARITY ERR	DTN TX BUF3B PARITY ERR
6E	FCA::CHK2F41							
	DTN RX BUF0 PARITY ERR	DTN RX BUF1 PARITY ERR	DTN RX BUF2 PARITY ERR	DTN RX BUF3 PARITY ERR	DTN RX BUF4 PARITY ERR	DTN RX BUF5 PARITY ERR	DTN RX BUF6 PARITY ERR	DTN RX BUF7 PARITY ERR
6F	FCA::CHK2G40							
	CC2 LA ERR	CC2 LBA ERR	CC2 LLRC ERR	CC3 LA ERR	CC3 LBA ERR	CC3 LLRC ERR	CC4 LA ERR	CC4 LBA ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(6) Byte29 bit0 - 3 = 6 or 7 (4/4)

	0	1	2	3	4	5	6	7
70		FCA::CHK2G40						
	CC4 LLRC ERR	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
71		FCA::CWCSA00						
		Slave 1 Cache Write Address (BYTE0)						
72		FCA::CWCSA0104						
		Slave 1 Cache Write Address (BYTE1)						
73		FCA::CWCSA10						
		Slave 2 Cache Write Address (BYTE0)						
74		FCA::CWCSA1114						
		Slave 2 Cache Write Address (BYTE1)						
75		FCA::CRCSA00						
		Cache Read Address (BYTE0)						
76		FCA::CRCSA0104						
		Cache Read Address (BYTE1)						
77		FCA::QDSTS0						
	ANT ERROR	CHK2A/2B	CHK2C	CHK2D	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
78		FCA::QDSTS0						
	P0 ERRINT	P1 ERRINT	STATUS0 C-ERR	STATUS1 C-ERR	DT0 PLRC ERR	DT1 PLRC ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR
79		FCA::QDSTS0						
	STATUS0 END-CODE ERR	STATUS0 PLRC ERR ERR	STATUS0 INV-PLRC ERR	STATUS0 END-CODE ERR	(RSV)	(RSV)	I/O DT0 ERR	I/O DT1 ERR
7A		FCA::QDSTS0						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
7B		FCA::QDSTS1						
	DTN SEQ ERR	DTN INPUT CTL ERR	DTN RD CTL ERR	DTN WT CTL ERR	P0 SYNCI PNT ERR	P1 SYNCI PNT ERR	P0 SYNCI CLOCK ERR	P1 SYNCI CLOCK ERR
7C		FCA::QDSTS1						
	P0 SLRC CNT ERR	P0 SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX WT PNT PARITY ERR	P1 SLRC CNT ERR	P1 SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX WT PNT PARITY ERR
7D		FCA::QDSTS1						
	I/O DT2 ERR	I/O DT3 ERR	STATUS0 DT0-3 PARITY ERR	STATUS0 DT4-7 PARITY ERR	STATUS1 DT0-3 PARITY ERR	STATUS1 DT4-7 PARITY ERR	TIME OUT	ABT ERR
7E		FCA::QDSTS1						
	TRANS MODE ERR	ADR/CMD PLRC ERR	ADR/CMD END-CODE ERR	ADR/CMD DT PARITY ERR	DTN DT0-3 PARITY ERR	DTN DT4-7 PARITY ERR	P0 PLRC ERR	P1 PLRC ERR
7F		DRR::D0ESTA8						
	P0 ENT TOV	P0 ACK TOV	P1 ENT TOV	P1 ACK TOV	P0 STATUS TOV	P1 STATUS TOV	(RSV)	(RSV)

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(7) Byte29 bit0 - 3 = 8 (1/4)

	0	1	2	3	4	5	6	7
40		STATUS1(SLAVE 2) byte1						
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41		STATUS0(SLAVE 1) byte2						
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42		STATUS0(SLAVE 1) byte3						
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43		STATUS0(SLAVE 1) byte4						
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44		STATUS0(SLAVE 1) byte5						
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45		STATUS0(SLAVE 2) byte2						
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46		STATUS0(SLAVE 2) byte3						
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47		STATUS0(SLAVE 2) byte4						
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48		STATUS0(SLAVE 2) byte5						
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49		CMA:: ADDRESSERR1 / DATAERR1						
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A		CMA::ADDRESSERR1						
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B		CMA::ADDRESSERR2						
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C		CMA::ADDRESSERR2						
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D		CMA::DATAERR1						
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E		CMA::DATAERR2						
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F		CMA::PORTBRDERR1						
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(7) Byte29 bit0 - 3 = 8 (2/4)

	0	1	2	3	4	5	6	7
50		CMA::PORTBRDERR1						
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51		CMA::PORTBRDERR2 / BOARDEXPTERR						
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52		CMA::SETUPERR / BOARDEXPTERR						
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53		CMA::BOARDERR0 / BOARDERR2						
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54		CMA::BOARDERR2						
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55		CMA::BOARDERR3 / PSCTL						
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56		CMA::BOARDERR4 / PD_SROM						
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57		CMA::PD_SROM						
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58		CMA::BOARDERR3						
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59		CMA::BOARDERR4						
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A		CMA::MODULEERR						
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B		CMA::MEMADLOG450CAS						
	(RSV)	Error Access BA Address		Error Access CAS Address (High)				
5C		CMA::MEMADLOG450CAS						
		Error Access CAS Address (Low)						
5D		CARB::PnERR0						
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E		CARB::PnERR0						
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F		CARB::PnERR1						
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(7) Byte29 bit0 - 3 = 8 (3/4)

	0	1	2	3	4	5	6	7
60		CARB::PnERR1						
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WT CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRAN CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61		CARB::MixREG						
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO END CODE ERR	Pn FIFO SLRC ERR	(RSV)
62		CARB::CxERR0						
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63		CARB::CxERR0						
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		CARB::CxERR1						
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65		CARB::CxERR1						
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66		CARB::CyERR0						
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67		CARB::CyERR0						
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68		CARB::CyERR1						
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69		CARB::CxERR1						
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A		DRR::STATS						
	CMD A TRANSFER END	(RSV)	CMD A Transfer Start	CMD A Transfer Excuting	CMD B TRANSFER END	(RSV)	CMD B Transfer Start	CMD B Transfer Excuting
6B		DRR::STATS						
	CHK2 Detected	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK1B Detected	ABORT Detected	Force Err Detected
6C		DRR::DRERR						
	DRR CTL ERR	P0 CTL ERR	P1 CTL ERR	DRR DATA ERR	P0 DT ERR	P1 DT ERR	STATUS0 CARB/CMA ERR	STATUS1 CARB/CMA ERR
6D		DRR::DRERR						
	P0 ERR INT	P1 ERR INT	DT ERR	TIME OVER ERR	STATUS0 VALID	STATUS1 VALID	P0 USE FLAG	P1 USE FLAG
6E		DRR::DRESTA1						
	P0 SYNC0 PNT PARITY ERR	P0 SYNC1 PNT PARITY ERR	P0 SYNC0 CLOCK PARITY ERR	P0 SYNC1 CLOCK PARITY ERR	P0 TX SEQ ERR	P0 TX RD PNT PARITY ERR	P0 RX SEQ ERR	P0 RX RD PNT PARITY ERR
6F		DRR::DRESTA2						
	P1 SYNC0 PNT PARITY ERR	P1 SYNC1 PNT PARITY ERR	P1 SYNC0 CLOCK PARITY ERR	P1 SYNC1 CLOCK PARITY ERR	P1 TX SEQ ERR	P1 TX RD PNT PARITY ERR	P1 RX SEQ ERR	P1 RX RD PNT PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(7) Byte29 bit0 - 3 = 8 (4/4)

	0	1	2	3	4	5	6	7
70	DRR::DRESTA2							
	P0 SEQ PARITY ERR	P1 SEQ PARITY ERR	SLRC CAL-DT PARITY ERR	SLRC DT PARITY ERR	AC PLRCGEN DT PARITY ERR0	AC PLRCGEN DT PARITY ERR1	DT PLRCGEN DT PARITY ERR0	DT PLRCGEN DT PARITY ERR1
71	DRR::DRESTA3							
	STATUS0 PLRC ERR	STATUS0 INV-PLRC ERR	STATUS1 PLRC ERR	STATUS1 INV-PLRC ERR	DT PLRC ERR	DT INV-PLRC ERR	DT END-CODE	LA DT PARITY ERR
72	DRR::DRESTA4							
	ELA/CLA DT PARITY ERR	CMD PARITY ERR AT 64-CMD	STATUS0 END-CODE ERR	STATUS1 END-CODE ERR	SLAVE1 CMD-A ADR PARITY ERR	SLAVE1 CMD-B ADR PARITY ERR	SLAVE2 CMD-A ADR PARITY ERR	SLAVE2 CMD-B ADR PARITY ERR
73	DRR::DRESTA4							
	STATUS0 DT0 PARITY ERR	STATUS0 DT1 PARITY ERR	STATUS0 DT2 PARITY ERR	STATUS0 DT3 PARITY ERR	STATUS0 DT4 PARITY ERR	STATUS0 DT5 PARITY ERR	STATUS0 DT6 PARITY ERR	STATUS0 DT7 PARITY ERR
74	DRR::DRESTA5							
	STATUS1 DT0 PARITY ERR	STATUS1 DT1 PARITY ERR	STATUS1 DT2 PARITY ERR	STATUS1 DT3 PARITY ERR	STATUS1 DT4 PARITY ERR	STATUS1 DT5 PARITY ERR	STATUS1 DT6 PARITY ERR	STATUS1 DT7 PARITY ERR
75	FCA::DRESTA8							
	P0 ENT TIME OVER	P0 ACK TIME OVER	P1 ENT TIME OVER	P1 ACK TIME OVER	P0 USE FLAG	P1 USE FLAG	SLRC ERR	MRCF DOUBLE EXCUTE
76	DRR::DRESTAD							
	ABT SEQ PARITY ERR (M)	ABT SEQ PARITY ERR (S)	P0 ABT CMP CHK ERR	P1 ABT CMP CHK ERR	PKID CHK ERR	(RSV)	(RSV)	(FSV)
77	DRR::DRESTAD							
	CBUF0/1 DATA0 PARITY ERR	CBUF0/1 DATA1 PARITY ERR	CBUF0/1 DATA2 PARITY ERR	CBUF0/1 DATA3 PARITY ERR	CBUF0/1 DATA4 PARITY ERR	CBUF0/1 DATA5 PARITY ERR	CBUF0/1 DATA6 PARITY ERR	CBUF0/1 DATA7 PARITY ERR
78	DRR::TRMDA							
	CMD A SYND CHK	(RSV)	CMD A MRCF Function	CMD A Double WT	CMD A Transfer Command			
79	DRR::TRMDA							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
7A	DRR::ADR0A							
	CMD A Slave 1 Cache Transfer Address (BYTE0)							
7B	DRR::ADR0A							
	CMD A Slave 2 Cache Transfer Address (BYTE0)							
7C	DRR::TRMDB							
	CMD B SYND CHK	(RSV)	CMD B MRCF Function	CMD B Double WT	CMD B Transfer Command			
7D	DRR::TRMDB							
	LA0(LBA) COMP CHK ENABLE	LA1 COMP CHK ENABLE	LA2 COMP CHK ENABLE	(RSV)	EXLA COUNT UP STOP	(RSV)	(RSV)	(RSV)
7E	DRR::ADR0B							
	CMD B Slave 1 Cache Transfer Address (BYTE0)							
7F	DRR::ADR0B							
	CMD B Slave 2 Cache Transfer Address (BYTE0)							

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(8) Byte29 bit0 - 3 = A or B (1/4)

	0	1	2	3	4	5	6	7
40	STATUS1(Slave2) byte1							
	STATUS1 Reserved	STATUS1 PATH ID			STATUS1 CMA UNINITIAL	STATUS1 Answer CACHE P/K#		STATUS1 Answer CMA#
41	STATUS1(Slave1) byte2							
	STS0 CARB PXDR INDPE	STS0 CARB PXLRCE	STS0 CARB PXDR OUTDPE	STS0 CARB PXOR INDPE	STS0 CARB PXTME	STS0 CARB ABTE	STS0 CARB PXHE	STS0 CARB PXMAE
42	STATUS0(Slave1) byte3							
	STS0 CARB CXOR INDPE	STS0 CARB CXDR INDPE	STS0 CARB CXLRCE	STS0 CARB CXDR OUTDPE	STS0 CARB CXTME	STS0 CARB CXHE	STS0 CARB FIFO INDPE	STS0 CARB CMA ERRINT
43	STATUS0(Slave1) byte4							
	STS0 CMA BOARD DISABLE	STS0 CMA MEM NOT RDY	STS0 CMA MODULE DISABLE	STS0 CMA MEM BACKUP MODE	STS0 CMA DIAG UMNT	STS0 CMA SP UMNT	STS0 CMA REG CODE ERR	STS0 CMA INVLD COM
44	STATUS0(Slave1) byte5							
	STS0 CMA PKID PEER	STS0 CMA GSLRCER	STS0 CMA DT PKT ER	STS0 CMA CMD PKT ER	STS0 CMA MODULE ER	STS0 CMA HCTL ER	STS0 CMA MCTL ER	STS0 CMA BRD ER
45	STATUS0(Slave1) byte2							
	STS1 CARB PXDR INDPE	STS1 CARB PXLRCE	STS1 CARB PXDR OUTDPE	STS1 CARB PXOR INDPE	STS1 CARB PXTME	STS1 CARB ABTE	STS1 CARB PXHE	STS1 CARB PXMAE
46	STATUS0(Slave1) byte3							
	STS1 CARB CXOR INDPE	STS1 CARB CXDR INDPE	STS1 CARB CXLRCE	STS1 CARB CXDR OUTDPE	STS1 CARB CXTME	STS1 CARB CXHE	STS1 CARB FIFO INDPE	STS1 CARB CMA ERRINT
47	STATUS0(Slave1) byte4							
	STS1 CMA BOARD DISABLE	STS1 CMA MEM NOT RDY	STS1 CMA MODULE DISABLE	STS1 CMA MEM BACKUP MODE	STS1 CMA DIAG UMNT	STS1 CMA SP UMNT	STS1 CMA REG CODE ERR	STS1 CMA INVLD COM
48	STATUS0(Slave1) byte5							
	STS1 CMA PKID PEER	STS1 CMA GSLRCER	STS1 CMA DT PKT ER	STS1 CMA CMD PKT ER	STS1 CMA MODULE ER	STS1 CMA HCTL ER	STS1 CMA MCTL ER	STS1 CMA BRD ER
49	CMA:: ADDRESSERR1 / DATAERR1							
	SLAVE1 ADR PARITY ERR	SLAVE1 CMD PARITY ERR	SLAVE1 ADR/CMD 0 PARITY ERR	SLAVE1 ADR/CMD 1 PARITY ERR	ADR/CMD PLRC ERR	WRITE DATA PARITY ERR	WRITE LOOP DATA PARITY ERR	WRITE DATA PLRC ERR
4A	CMA::ADDRESSERR1							
	SLAVE1 LEN ZERO	SLAVE1 LEN BNDER	SLAVE1 LEN OVER	SLAVE1 CMD CNSTER	CP CMD ERR	NOT SEL ERR	END-CODE ERR	ENT OFF
4B	CMA::ADDRESSERR2							
	SLAVE2 ADR PARITY ERR	SLAVE2 CMD PARITY ERR	SLAVE2 ADR/CMD 0 PARITY ERR	SLAVE2 ADR/CMD 1 PARITY ERR	END-CODE PARITY ERR	(RSV)	(RSV)	(RSV)
4C	CMA::ADDRESSERR2							
	SLAVE2 LEN ZERO	SLAVE2 LEN BNDER	SLAVE2 LEN OVER	SLAVE2 CMD CNSTER	INVL CMD ERR	ONE SLAVE ERR	PATH ERR	HEAD TIME OUT
4D	CMA::DATAERR1							
	PLRC ERR	PAD ERR	WRITE DATA0 PARITY ERR	WRITE DATA1 PARITY ERR	TX PLRC ERR	TX PAD ERR	TX BYTE0 PARITY ERR	TX BYTE1 PARITY ERR
4E	CMA::DATAERR2							
	WRITE SLRC ERR	READ SLRC ERR	MEM UNCORRECT ERR	MEM CORRECT ERR	MEM DATA ERR	REG PATH ERR	MEM WRITE UNDER RUN ERR	(RSV)
4F	CMA::PORTBRDERR1							
	TIME OUT CNT1(M) PARITY ERR	TIME OUT CNT2(M) PARITY ERR	TIME OUT CNT1(PR) PARITY ERR	TIME OUT CNT2(PR) PARITY ERR	HSEQ PARITY ERR	RXSEQ PARITY ERR	TXSEQ PARITY ERR	FIFO READ DATA LEN ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(8) Byte29 bit0 - 3 = A or B (2/4)

	0	1	2	3	4	5	6	7
50	CMA::PORTBRDERR1							
	FIFO WRITE DATA LEN ERR	FIFO READ PNT PARITY ERR	FIFO WRITE PNT PARITY ERR	PR PARITY ERR	MCT PARITY ERR	CMCT PARITY ERR	(RSV)	PCNV ERR
51	CMA::PORTBRDERR2 / BOARDEXPTERR							
	DATA TIME OUT	ARB TIME OUT	HCTL-MCTL I/F ERR	HTCL-RCTL I/F ERR	MCTL HARD ERR	PATH CLOCK ERR	MEM CLOCK ERR	RCTL HARD ERR
52	CMA::SETUPERR / BOARDEXPTERR							
	BOARD DISABLE	MEM NOT RDY	MODULE DISABLE	BACK UP BUSY	DIAG UNMATCH	SP UNMATCH	REG CODE ERR	PKID PARITY ERR
53	CMA::BOARDERR0 / BOARDERR2							
	READ ECC UNCORRECT ERR	READ ECC CORRECT ERR	WRITE ECC CORRECT ERR	REGCLT ADR CNT PARITY ERR	REGCLT TF CNT PARITY ERR	REGCLT CNT OVER	(RSV)	(RSV)
54	CMA::BOARDERR2							
	PORT ADR ERR	PORT CNT	PORT PLRC ERR	PORT WRITE DATA PARITY ERR	OTHER PORT ADR ERR	OTHER PORT CNT	OTHER PORT PLRC ERR	OTHER PORT WRITE DATA PARITY ERR
55	CMA::BOARDERR3 / PSCTL							
	MCTL MAINSEQ ERR	MCTL INISEQ ERR	MCTL PWDSEQ ERR	MCTL REFSEQ ERR	MCTL REGSEQ ERR	MCTL MEMSEQ ERR	(RSV)	CACHE P/K PS DOWN
56	CMA::BOARDERR4 / PD_SROM							
	PATH CLOCK ERR	MEM CLOCK ERR	(RSV)	PDCTL ERR	(RSV)	(RSV)	SCK ERR	SDA ERR
57	CMA::PD_SROM							
	SEQ1 ERR	SEQ2 ERR	(RSV)	WRITE DATA PARITY ERR	ACNT ERR	TCNT ERR	BCNT ERR	TIME ERR
58	CMA::BOARDERR3							
	MCTL TIMECNT ERR	MCTL IREFCNT ERR	MCTL SELFCNT ERR	(RSV)	MCTL TFCNT ERR	ARB ERR	(RSV)	GTL INI TIMER PARITY ERR
59	CMA::BOARDERR4							
	MEM ADR CNT ERR	ADR CTL ERR	ADR CNT OVER	ADR PARITY ERR	TAG ERR	ECC HARD ERR	REF CNT ERR	REF TIME OUT
5A	CMA::MODULEERR							
	MG#0 ECC UNCORRECT ERR	MG#1 ECC UNCORRECT ERR	MG#2 ECC UNCORRECT ERR	MG#3 ECC UNCORRECT ERR	MG#4 ECC UNCORRECT ERR	MG#5 ECC UNCORRECT ERR	MG#6 ECC UNCORRECT ERR	MG#7 ECC UNCORRECT ERR
5B	CMA::MEMADLOGCAS							
		Error Access BA Address		Error Access CAS Address (High)				
5C	CMA::MEMADLOGCAS							
	Error Access CAS Address (Low)							
5D	CARB::PnERR0							
	Pn DR IN DATA PARITY ERR	Pn PATH LRC ERR	Pn PATH END-CODE ERR	Pn PATH SLRC ERR	Pn DR OUT DATA ERR	Pn OR IN DATA PARITY ERR	Pn WR1 TIMER TIME OUT	CLK ERR
5E	CARB::PnERR0							
	ABT CMP ERR	ABT SEQ PARITY ERR	Pn SEQA PARITY ERR	Pn IP-CX DR PNT PARITY ERR	Pn SEQA TRF CNT PARITY ERR	Pn SEQB PARITY ERR	CXDR-P0OR PNT PARITY ERR	P0DR-CXOR PNT PARITY ERR
5F	CARB::PnERR1							
	Pn SEQB TRF CNT PARITY ERR	Pn SEQD PARITY ERR	Pn SYNC0 CNT PARITY ERR	Pn SYNC1 CNT PARITY ERR	Pn WR1 TIMER PARITY ERR	Pn MICRO ERR	Pn I/O ACS ERR	T6 PARITY ERR

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(8) Byte29 bit0 - 3 = A or B (3/4)

	0	1	2	3	4	5	6	7
60		CARB::PnERR1						
	Pn DEF WR CNT PARITY ERR	Pn DEF RD CNT PARITY ERR	Pn FIFO WR CNT PARITY ERR	Pn FIFO RD CNT PARITY ERR	Pn SEQE PARITY ERR	Pn SEQE J4 CNT PARITY ERR	Pn SEQE TRF CNT PARITY ERR	Pn FIFO IN DATA PARITY ERR
61		CARB::MixREG						
	Pn ACK LOOP CHK ERR	Pn ERRINT LOOP CHK ERR	Pn CLKSEQ PARITY ERR	Pn STEN ERR	Pn FIFO VRC ERR	Pn FIFO ENDCODE ERR	Pn FIFO SLRC ERR	(RSV)
62		CARB::CxERR0						
	Cx OR IN DATA PARITY ERR	Cx DR IN DATA PARITY ERR	Cx PLRC ERR	Cx END-CODE ERR	Cx SLRC ERR	Cx DR OUT DATA PARITY ERR	Cx ENT LOOP CHK ERR	Cx STEN LOOP CHK ERR
63		CARB::CxERR0						
	Cx DR1 TIMER TIME OUT	Cx DR2 TIMER TIME OUT	Cx WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
64		CARB::CxERR1						
	Cx SEQC PARITY ERR	Cx TRF CNT PARITY ERR	Cx DR PNT PARITY ERR	Cx SEQD PARITY ERR	Cx IP PNT0 PARITY ERR	Cx IP PNT1 PARITY ERR	(RSV)	(RSV)
65		CARB::CxERR1						
	Cx RD1 TIMER PARITY ERR	Cx RD2 TIMER PARITY ERR	Cx WT2 TIMER PARITY ERR	Cx STM CNT PARITY ERR	Cx SCN CNT PARITY ERR	(RSV)	(RSV)	(RSV)
66		CARB::CyERR0						
	Cy OR IN DATA PARITY ERR	Cy DR IN DATA PARITY ERR	Cy PLRC ERR	Cy END-CODE ERR	Cy SLRC ERR	Cy DR OUT DATA PARITY ERR	(RSV)	(RSV)
67		CARB::CyERR0						
	Cy DR1 TIMER TIME OUT	Cy DR2 TIMER TIME OUT	Cy WR2 TIMER TIME OUT	(RSV)	(RSV)	(RSV)	(RSV)	(RSV)
68		CARB::CyERR1						
	Cy SEQC PARITY ERR	Cy TRF CNT PARITY ERR	Cy DR PNT PARITY ERR	Cy SEQD PARITY ERR	Cy IP PNT0 PARITY ERR	Cy IP PNT1 PARITY ERR	(RSV)	(RSV)
69		CARB::CxERR1						
	Cy RD1 TIMER PARITY ERR	Cy RD2 TIMER PARITY ERR	Cy WT2 TIMER PARITY ERR	Cy STM CNT PARITY ERR	Cy SCM CNT PARITY ERR	(RSV)	(RSV)	(RSV)
6A		NDTM::CHK2CSTS0/1						
	P0 RD DATA0 PARITY ERR	P0 RD DATA1 PARITY ERR	P0 RD DATA2 PARITY ERR	P0 RD DATA3 PARITY ERR	(RSV)	(RSV)	(RSV)	(RSV)
6B		NDTM::CHK2CSTS0/1						
	(RSV)	(RSV)	P0 SYNC ERR	P0 RD END-CODE ERR	P0 STATUS1 END-CODE ERR	P0 STATUS2 END-CODE ERR	P0 RD PLRC ERR	P0 STSTUS1 PLRC ERR
6C		NDTM::CHK2CSTS0/1						
	P0 STATUS2 PLRC ERR	P0 RD INV-PLRC ERR	P0 STATUS1 INV-PLRC ERR	P0 STATUS2 INV-PLRC ERR	P0 STATUS1 ST0,1 CMP ERR	P0 STATUS2 ST0,1 CMP ERR	P0 STATUS1 PKID ERR	P0 STATUS2 PKID ERR
6D		NDTM::CHK2CSTS0/1						
	P0 ERRINT ERR	P0 ACK ERR	P0 ENTOUT ERR	P0 STENOUT ERR	(RSV)	P0 TIMER1 TIME OUT	P0 TIMER2 TIME OUT	P0 TIMER3 TIME OUT
6E		NDTM::CHK2DSTS						
	P0 ERRINT Received	P1 ERRINT Received	(RSV)	(RSV)	(RSV)	(RSV)	HSN STATUS1 ERR ON	HSN STATUS2 ERR ON
6F		NDTM::HSNMADRU						
		Slave1 CACHE XFR Address (BYTE0)						

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Byte27 = F2 (CACHE CHK2) Byte40-7F Detail
(8) Byte29 bit0 - 3 = A or B (4/4)

	0	1	2	3	4	5	6	7
70	NDTM::HSNMADRL							
	Slave1 CACHE XFR Address (BYTE1)							
71	NDTM::HSNMADRL							
	Slave1 CACHE XFR Address (BYTE2)							
72	NDTM::HSNMADRL							
	Slave1 CACHE XFR Address (BYTE3)							
73	NDTM::HSNMADRL							
	Slave1 CACHE XFR Address (BYTE4)							
74	NDTM::HSNSADRU							
	Slave2 CACHE XFR Address (BYTE0)							
75	NDTM::HSNSADRL							
	Slave2 CACHE XFR Address (BYTE1)							
76	NDTM::HSNSADRL							
	Slave2 CACHE XFR Address (BYTE2)							
77	NDTM::HSNSADRL							
	Slave2 CACHE XFR Address (BYTE3)							
78	NDTM::HSNSADRL							
	Slave2 CACHE XFR Address (BYTE4)							
79	NDTM::CHSNCTL							
	C Path #00 ENABLE	C Path #01 ENABLE	C Path #02 ENABLE	C Path #03 ENABLE	C Path #04 ENABLE	C Path #05 ENABLE	C Path #06 ENABLE	C Path #07 ENABLE
7A	NDTM::CHSNCTL							
	C Path #10 ENABLE	C Path #11 ENABLE	C Path #12 ENABLE	C Path #13 ENABLE	C Path #14 ENABLE	C Path #15 ENABLE	C Path #16 ENABLE	C Path #17 ENABLE
7B	NDTM::CHSNPHASE / NDTM::CHSNCTL							
	ADR/CMD PHASE	WR DATA PHASE	RD DATA PHASE	STATUS1 PHASE	(RSV)	PKID		
7C	NDTM::XFC							
	Data XFR Path	0,1: PCI=>CACHE, 2,3: DBF=>CACHE 6,7: CACHE FORMAT, 8: CACHE=>PCI 9: CACHE=> DBF, C,D: CACHE COPY			PCI MODE 0:Mastr 1:Target	PBF MODE 0:No Fetch 1:Fetch	(RSV)	(RSV)
7D	NDTM::XFC							
	(RSV)	(RSV)	PNTR0 PARITY ERR	PNTR1 PARITY ERR 0	SYNC CMP ERR0	SYNC CMP ERR1	SYNC CMP ERR2	SYNC CMP ERR3
7E	NDTM::XFS							
	TRANSFER END	ABORT	(RSV)	(RSV)	(RSV)	(RSV)	WCHK1 Detected	CHK2 Detected
7F	NDTM::XFS							
	CHK2A Detected	CHK2B Detected	CHK2C Detected	CHK2D Detected	CHK2E Detected	(RSV)	(RSV)	(RSV)

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Byte27 = F6 (CFW Access not Authorized) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘6’)			
28	Reason code (x‘01’ : CFW ID unmatch)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Maker code & Manufacture code (x‘00’)							
30	Not used							
31	Module ID							
32	Routine ID							
33	PCB number				Not used			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFF6’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = F6 (CFW Access not Authorized) (2/2)

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Byte27 = FA (NVS Terminated) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder addres (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘A’)			
28	Reason code (x‘02’ : NVS failure)							
29	Not used							
2A								
2B								
2C								
2D	SSID of mate subsystem (x‘0000’ for EDCC)							
2E								
2F	Mader code & Manufacture code (x‘00’)							
30	Not used							
31	Module ID							
32	Routine ID							
33	PCB number				Error code (x‘F’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFFA’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not usde (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte27 = FA (NVS Terminated) (2/2)

	0	1	2	3	4	5	6	7
40	Key cede (for reconnection)							
41	Format/Message (for reconnection)							
42	Module ID (for reconnection)							
43	Routine ID(for reconnection)							
44								
	Not used							
7F								

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Byte27 = FB (HRC/HODM Pair suspend) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (low order)							
26	Cylinder address (high order)				Head address			
27	Format (x‘F’)				Message (x‘B’)			
28	R-Vol Suspended	R-Vol failed	Reason code(Note)					
29	RCU device address							
2A	RCU Manufacture code/Factory code							
2B								
2C								
2D	RCU Sequence No.							
2E								
2F	MCU Manufacture code/Factory code							
30								
31								
32	MCU Sequence No.							
33								
34	SSID of self subsystem							
35								
36	Symptom code (x‘FE’)							
37	Symptom code (same byte #28)							
38	Not used (x‘00’)							
39	Not used (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Not used (x‘00’)							
3E	Reference code(x‘FFFB’)							
3F								

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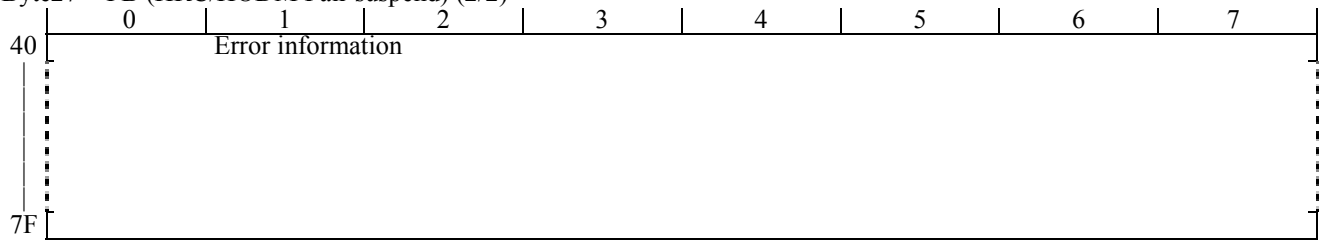
Byte27 = FB (HRC/HODM Pair suspend) (2/2)



(Note) Reason code

x‘14’-x‘2F’	: Reserved
x‘30’	: Pair suspended. MCU device write error.
x‘31’	: Pair suspended. RCU subsystem error/or MCU subsystem error.
x‘32’	: Pair suspended. RCU device communication error.
x‘33’	: Pair suspended (Critical device status). All write command is rejected until the pair is re-established.
x‘34’	: Pair suspended. RCU device is not ready (intervention required).

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB (x‘35’)							
20	Basic SSB							
21								
22								
23	Count							
24	Device address							
25	Cylinder address (Low)							
26	Cylinder address (High)				Head address			
27	Format (x‘F’)				Message (x‘F’)			
28	Subcode (See following pages)							
29	Hardware information (See following pages)							
30								
31	Module ID							
32	Routine ID							
33	PCB number				Message code (x‘0’)			
34	SSID of self subsystem							
35								
36	Symptom code (x‘FFFF’)							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Not used (x‘00’)							
3D	Cylinder address							
3E								
3F	Head address							
40	Hardware information (See following pages)							
7F								

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(1) Byte28 = 02 : Cache 1 symbol error

	0	1	2	3	4	5	6	7
28	Subcode : x‘02’ : Cache 1 symbol error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30								

40 | 7F	Common information (See “Type 1”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(2) Byte28 = 04 : Shared memory 1 symbol error

	0	1	2	3	4	5	6	7
28	Subcode : x‘04’ : Shared memory 1 symbol error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory (Side A:x‘00’, Side B:x‘01’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 2”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(3) Byte28 = 08/09 :Three SM DISABLE lines inconsistent

	0	1	2	3	4	5	6	7
28	Subcode : x‘08’ : Three SM (A) DISABLE lines inconsistent x‘09’ : Three SM (B) DISABLE lines inconsistent							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Threshold counter for the warning							
2C	MPA::HOUT							
	SMDA(0-2) signal all	SMDA0 signal	SMDA1 signal	SMDA2 signal	SMDB(0-2) signal all	SMDB0 signal	SMDB1 signal	SMDB2 signal
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPA::HIN							
	SMDA(0-2) MV	SMDA0 status	SMDA1 status	SMDA2 status	SMDB(0-2) MV	SMDB0 status	SMDB1 status	SMDB2 status

40 | 7F	Common information (See “Type 3”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(4) Byte28 = 10 : SMA slave error

	0	1	2	3	4	5	6	7
28	Subcode : x‘10’ : SMA slave error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Scan slave MPID							

40 | 7F	Common information (See “Type 4”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(5) Byte28 = 11 : MPA slave error

	0	1	2	3	4	5	6	7
28	Subcode : x‘11’ : MPA slave error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Transfer SMA (2:Side A, 1:Side B)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	PKID (Reported SSB)							

40 | 7F	Common information (See “Type 5”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(6) Byte28 = 12 : SMA SCINT error

	0	1	2	3	4	5	6	7
28	Subcode : x‘12’ : SMA SCINT error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPID (Reported SSB)							

40 | 7F	Common information (See “Type 9”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(7) Byte28 = 13 : SMA BCINT error

	0	1	2	3	4	5	6	7
28	Subcode : x‘13’ : SMA BCINT error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Slot number of shared memory							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	MPID (Reported SSB)							

40 | 7F	Common information (See “Type 10”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(8) Byte28 = 20 : FSW LED BUS test error

	0	1	2	3	4	5	6	7
28	Subcode : x‘20’ : FSW LED BUS test error							
29	MPID (Reported SSB)							
2A	FCA::LEDADRDT							
	Address of LED BUS							
2B	FCA::LEDADRDT							
	Data of LED BUS							
2C	FCA::LEDCMD							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR CMD
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	FCA::LEDSTAT							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used

40 | 7F	Common information (See “Type 6”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(9) Byte28 = 40 : Abnormal DC CTL warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘40’ : Abnormal DC CTL warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 7”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(10) Byte28 = 41 : Abnormal CEMODE warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘41’ : Abnormal CEMODE warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 7”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(11) Byte28 = B0 : CARB error : Warning

	0	1	2	3	4	5	6	7
28	Subcode : x‘B0’ : CARB error : Warning							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Used P-PATH No. (00 : P-PATH0, 01 : P-PATH1)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30	Not used (x‘00’)							

40 | 7F	Common information (See “Type 8”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(12) Byte28 = 01 : CHM DXBF correctable error

	0	1	2	3	4	5	6	7
28	Subcode : x‘01’ : CHM DXBF correctable error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30								

40 | 7F	Common information (See “Type 11”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(13) Byte28 = 03 : CHF DXBF correctable error

	0	1	2	3	4	5	6	7
28	Subcode : x‘03’ : CHF DXBF correctable error							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30								

40 | 7F	Common information (See “Type 12”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning : Error handling support) Hardware detail information

(14) Byte28 = 07 : DRAM/MCH/P64H2 error detection

	0	1	2	3	4	5	6	7
28	Subcode : x‘07’ : (DRAM/MCH/P64H2 error detection)							
29	MPID (Reported SSB)							
2A	Not used (x‘00’)							
2B	Not used (x‘00’)							
2C	Not used (x‘00’)							
2D	Not used (x‘00’)							
2E	Not used (x‘00’)							
2F	Not used (x‘00’)							
30								

40 | 7F	Common information (See “Type 13”)

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for cache memory 1 symbol error							
	Module group #0 - H							
41	Threshold counter for cache memory 1 symbol error							
	Module group #0 - L							
42	Threshold counter for cache memory 1 symbol error							
	Module group #1 - H							
43	Threshold counter for cache memory 1 symbol error							
	Module group #1 - L							
44	Threshold counter for cache memory 1 symbol error							
	Module group #2 - H							
45	Threshold counter for cache memory 1 symbol error							
	Module group #2 - L							
46	Threshold counter for cache memory 1 symbol error							
	Module group #3 - H							
47	Threshold counter for cache memory 1 symbol error							
	Module group #3 - L							
48	Threshold counter for cache memory 1 symbol error							
	Module group #4 - H							
49	Threshold counter for cache memory 1 symbol error							
	Module group #4 - L							
4A	Threshold counter for cache memory 1 symbol error							
	Module group #5 - H							
4B	Threshold counter for cache memory 1 symbol error							
	Module group #5 - L							
4C	Threshold counter for cache memory 1 symbol error							
	Module group #6 - H							
4D	Threshold counter for cache memory 1 symbol error							
	Module group #6 - L							
4E	Threshold counter for cache memory 1 symbol error							
	Module group #7 - H							
4F	Threshold counter for cache memory 1 symbol error							
	Module group#7 - L							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for cache memory 1 symbol error							
	Module group #8 - H							
51	Threshold counter for cache memory 1 symbol error							
	Module group #8 - L							
52	Threshold counter for cache memory 1 symbol error							
	Module group #9 - H							
53	Threshold counter for cache memory 1 symbol error							
	Module group #9 - L							
54	Threshold counter for cache memory 1 symbol error							
	Module group #10 - H							
55	Threshold counter for cache memory 1 symbol error							
	Module group #10 - L							
56	Threshold counter for cache memory 1 symbol error							
	Module group #11 - H							
57	Threshold counter for cache memory 1 symbol error							
	Module group #11 - L							
58	Threshold counter for cache memory 1 symbol error							
	Module group #12 - H							
59	Threshold counter for cache memory 1 symbol error							
	Module group #12 - L							
5A	Threshold counter for cache memory 1 symbol error							
	Module group #13 - H							
5B	Threshold counter for cache memory 1 symbol error							
	Module group #13 - L							
5C	Threshold counter for cache memory 1 symbol error							
	Module group #14 - H							
5D	Threshold counter for cache memory 1 symbol error							
	Module group #14 - L							
5E	Threshold counter for cache memory 1 symbol error							
	Module group #15 - H							
5F	Threshold counter for cache memory 1 symbol error							
	Module group#15 - L							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (3/4)

	0	1	2	3	4	5	6	7
60	CMA::WARNING							
	MG#00 1 symbol error	MG#01 1 symbol error	MG#02 1 symbol error	MG#03 1 symbol error	MG#04 1 symbol error	MG#05 1 symbol error	MG#06 1 symbol error	MG#07 1 symbol error
61	CMA::WARNING							
	MG#08 1 symbol error	MG#09 1 symbol error	MG#10 1 symbol error	MG#11 1 symbol error	MG#12 1 symbol error	MG#13 1 symbol error	MG#14 1 symbol error	MG#15 1 symbol error
62	CMA::MGxxHERRSTAT0							
	byte11 High order 4 bits warning	byte11 Low order 4 bits warning	Not used	Not used	Not used	Not used	Not used	Not used
63	CMA::MGxxHERRSTAT0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
64	CMA::MGxxHERRSTAT0							
	byte0F High order 4 bits warning	byte0F Low order 4 bits warning	byte0E High order 4 bits warning	byte0E Low order 4 bits warning	byte0D High order 4 bits warning	byte0D Low order 4 bits warning	byte0C High order 4 bits warning	byte0C Low order 4 bits warning
65	CMA::MGxxHERRSTAT0							
	byte0B High order 4 bits warning	byte0B Low order 4 bits warning	byte0A High order 4 bits warning	byte0A Low order 4 bits warning	byte09 High order 4 bits warning	byte09 Low order 4 bits warning	byte08 High order 4 bits warning	byte08 Low order 4 bits warning
66	CMA::MGxxLERRSTAT0							
	byte10 High order 4 bits warning	byte10 Low order 4 bits warning	Not used	Not used	Not used	Not used	Not used	Not used
67	CMA::MGxxLERRSTAT0							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
68	CMA::MGxxLERRSTAT0							
	byte07 High order 4 bits warning	byte07 Low order 4 bits warning	byte06 High order 4 bits warning	byte06 Low order 4 bits warning	byte05 High order 4 bits warning	byte05 Low order 4 bits warning	byte04 High order 4 bits warning	byte04 Low order 4 bits warning
69	CMA::MGxxLERRSTAT0							
	byte03 High order 4 bits warning	byte03 Low order 4 bits warning	byte02 High order 4 bits warning	byte02 Low order 4 bits warning	byte01 High order 4 bits warning	byte01 Low order 4 bits warning	byte00 High order 4 bits warning	byte00 Low order 4 bits warning
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type1 (4/4)

	0	1	2	3	4	5	6	7
70	Cache module number							
71	Cache PCB number							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM00							
41	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM01							
42	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM02							
43	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM03							
44	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM04							
45	Threshold counter for shared memory 1 symbol error							
	SMA-DIMM05							
46	Not used							
47	Not used							
48	Not used							
49	SMA::DIMM SIGNAL ERROR DIMM							
	DIMM00 control error	DIMM01 control error	DIMM02 control error	DIMM03 control error	DIMM04 control error	DIMM05 control error	Not used control error	Not used control error
4A	SMA::UNCOR ERROR DIMM							
	DIMM00 uncorrectable error	DIMM01 uncorrectable error	DIMM02 uncorrectable error	DIMM03 uncorrectable error	DIMM04 uncorrectable error	DIMM05 uncorrectable error	Not used	Not used
4B	SMA::COR ERROR DIMM							
	DIMM00 correctable error	DIMM01 correctable error	DIMM02 correctable error	DIMM03 correctable error	DIMM04 correctable error	DIMM05 correctable error	Not used	Not used
4C	SMA::COR ERROR DIMM00 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
4D	SMA::COR ERROR DIMM00 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
4E	SMA::COR ERROR DIMM01 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
4F	SMA::COR ERROR DIMM01 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::COR ERROR DIMM02 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
51	SMA::COR ERROR DIMM02 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
52	SMA::COR ERROR DIMM03 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
53	SMA::COR ERROR DIMM03 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
54	SMA::COR ERROR DIMM04 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
55	SMA::COR ERROR DIMM04 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
56	SMA::COR ERROR DIMM05 LOCATION							
	Correctable error in memory element 0 (for data)	Correctable error in memory element 1 (for data)	Correctable error in memory element 2 (for data)	Correctable error in memory element 3 (for data)	Correctable error in memory element 4 (for data)	Correctable error in memory element 5 (for data)	Correctable error in memory element 6 (for data)	Correctable error in memory element 7 (for data)
57	SMA::COR ERROR DIMM05 LOCATION							
	Correctable error in memory element 8 (for data)	Correctable error in memory element 9 (for data)	Correctable error in memory element 10 (for data)	Not used	Not used	Not used	Not used	Not used
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLECAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PARITY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type2 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	SMA::DIMM ENABLE							
	DIMM00 EN	DIMM01 EN	DIMM02 EN	DIMM03 EN	DIMM04 EN	DIMM05 EN	Not used	Not used
79	SMA::DIMM KIND							
	DIMM00 KIND 0:64MB 1:128mb	DIMM01 KIND 0:64MB 1:128MB	DIMM02 KIND 0:64MB 1:128MB	DIMM03 KIND 0:64MB 1:128MB	DIMM04 KIND 0:64MB 1:128MB	DIMM05 KIND 0:64MB 1:128MB	Not used	Not used
7A	SMA::DIMM CHECK ENABLE							
	DIMM00 CHKEN	DIMM01 CHKEN	DIMM02 CHKEN	DIMM03 CHKEN	DIMM04 CHKEN	DIMM05 CHKEN	Not used	Not used
7B	SMA::REWRITE INHIBIT							
	DIMM00 REW INH	DIMM01 REW INH	DIMM02 REW INH	DIMM03 REW INH	DIMM04 REW INH	DIMM05 REW INH	Not used	Not used
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for the warning							
	MPID 0							
41	Threshold counter for the warning							
	MPID 1							
42	Threshold counter for the warning							
	MPID 2							
43	Threshold counter for the warning							
	MPID 3							
44	Threshold counter for the warning							
	MPID 4							
45	Threshold counter for the warning							
	MPID 5							
46	Threshold counter for the warning							
	MPID 6							
47	Threshold counter for the warning							
	MPID 7							
48	Threshold counter for the warning							
	MPID 8							
49	Threshold counter for the warning							
	MPID 9							
4A	Threshold counter for the warning							
	MPID 10							
4B	Threshold counter for the warning							
	MPID 11							
4C	Threshold counter for the warning							
	MPID 12							
4D	Threshold counter for the warning							
	MPID 13							
4E	Threshold counter for the warning							
	MPID 14							
4F	Threshold counter for the warning							
	MPID15							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for the warning							
	MPID 16							
51	Threshold counter for the warning							
	MPID 17							
52	Threshold counter for the warning							
	MPID 18							
53	Threshold counter for the warning							
	MPID 19							
54	Threshold counter for the warning							
	MPID 20							
55	Threshold counter for the warning							
	MPID 21							
56	Threshold counter for the warning							
	MPID 22							
57	Threshold counter for the warning							
	MPID 23							
58	Threshold counter for the warning							
	MPID 24							
59	Threshold counter for the warning							
	MPID 25							
5A	Threshold counter for the warning							
	MPID 26							
5B	Threshold counter for the warning							
	MPID 27							
5C	Threshold counter for the warning							
	MPID 28							
5D	Threshold counter for the warning							
	MPID 29							
5E	Threshold counter for the warning							
	MPID 30							
5F	Threshold counter for the warning							
	MPID 31							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (3/4)

	0	1	2	3	4	5	6	7
60	Threshold counter for the warning							
	MPID 32							
61	Threshold counter for the warning							
	MPID 33							
62	Threshold counter for the warning							
	MPID 34							
63	Threshold counter for the warning							
	MPID 35							
64	Threshold counter for the warning							
	MPID 36							
65	Threshold counter for the warning							
	MPID 37							
66	Threshold counter for the warning							
	MPID 38							
67	Threshold counter for the warning							
	MPID 39							
68	Threshold counter for the warning							
	MPID 40							
69	Threshold counter for the warning							
	MPID 41							
6A	Threshold counter for the warning							
	MPID 42							
6B	Threshold counter for the warning							
	MPID 43							
6C	Threshold counter for the warning							
	MPID 44							
6D	Threshold counter for the warning							
	MPID 45							
6E	Threshold counter for the warning							
	MPID 46							
6F	Threshold counter for the warning							
	MPID 47							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type3 (4/4)

	0	1	2	3	4	5	6	7
70	Threshold counter for the warning							
	MPID 48							
71	Threshold counter for the warning							
	MPID 49							
72	Threshold counter for the warning							
	MPID 50							
73	Threshold counter for the warning							
	MPID 51							
74	Threshold counter for the warning							
	MPID 52							
75	Threshold counter for the warning							
	MPID 53							
76	Threshold counter for the warning							
	MPID 54							
77	Threshold counter for the warning							
	MPID 55							
78	Threshold counter for the warning							
	MPID 56							
79	Threshold counter for the warning							
	MPID 57							
7A	Threshold counter for the warning							
	MPID 58							
7B	Threshold counter for the warning							
	MPID 59							
7C	Threshold counter for the warning							
	MPID 60							
7D	Threshold counter for the warning							
	MPID 61							
7E	Threshold counter for the warning							
	MPID 62							
7F	Threshold counter for the warning							
	MPID 63							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (1/4)

	0	1	2	3	4	5	6	7
40	Scan type							
	04 : MP status read 02 : Scan read 01 : Scan write							
41	Not used							
42	Threshold counter for the scan group							
	Scan path group A							
43	Threshold counter for the scan group							
	Scan path group B							
44	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#0	SC_MASK MPA#1	SC_MASK MPA#2	SC_MASK MPA#3	SC_MASK MPA#4	SC_MASK MPA#5	SC_MASK MPA#6	SC_MASK MPA#7
45	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#8	SC_MASK MPA#9	SC_MASK MPA#A	SC_MASK MPA#B	SC_MASK MPA#C	SC_MASK MPA#D	SC_MASK MPA#E	SC_MASK MPA#F
46	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
47	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
48	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
49	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
4A	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4B	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4C	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#0	SCCNT_PERR MPA#1	SCCNT_PERR MPA#2	SCCNT_PERR MPA#3	SCCNT_PERR MPA#4	SCCNT_PERR MPA#5	SCCNT_PERR MPA#6	SCCNT_PERR MPA#7
4D	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#8	SCCNT_PERR MPA#9	SCCNT_PERR MPA#A	SCCNT_PERR MPA#B	SCCNT_PERR MPA#C	SCCNT_PERR MPA#D	SCCNT_PERR MPA#E	SCCNT_PERR MPA#F
4E	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#0	VALCNT_PERR MPA#1	VALCNT_PERR MPA#2	VALCNT_PERR MPA#3	VALCNT_PERR MPA#4	VALCNT_PERR MPA#5	VALCNT_PERR MPA#6	VALCNT_PERR MPA#7
4F	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#8	VALCNT_PERR MPA#9	VALCNT_PERR MPA#A	VALCNT_PERR MPA#B	VALCNT_PERR MPA#C	VALCNT_PERR MPA#D	VALCNT_PERR MPA#E	VALCNT_PERR MPA#F

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#0	SCSEQ_ERR MPA#1	SCSEQ_ERR MPA#2	SCSEQ_ERR MPA#3	SCSEQ_ERR MPA#4	SCSEQ_ERR MPA#5	SCSEQ_ERR MPA#6	SCSEQ_ERR MPA#7
51	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#8	SCSEQ_ERR MPA#9	SCSEQ_ERR MPA#A	SCSEQ_ERR MPA#B	SCSEQ_ERR MPA#C	SCSEQ_ERR MPA#D	SCSEQ_ERR MPA#E	SCSEQ_ERR MPA#F
52	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#0	SINT_OUT_ ERR MPA#1	SINT_OUT_ ERR MPA#2	SINT_OUT_ ERR MPA#3	SINT_OUT_ ERR MPA#4	SINT_OUT_ ERR MPA#5	SINT_OUT_ ERR MPA#6	SINT_OUT_ ERR MPA#7
53	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#8	SINT_OUT_ ERR MPA#9	SINT_OUT_ ERR MPA#A	SINT_OUT_ ERR MPA#B	SINT_OUT_ ERR MPA#C	SINT_OUT_ ERR MPA#D	SINT_OUT_ ERR MPA#E	SINT_OUT_ ERR MPA#F
54	SMA::SCINT SIGNAL							
	SINT_SIG MPA#0	SINT_SIG MPA#1	SINT_SIG MPA#2	SINT_SIG MPA#3	SINT_SIG MPA#4	SINT_SIG MPA#5	SINT_SIG MPA#6	SINT_SIG MPA#7
55	SMA::SCINT SIGNAL							
	SINT_SIG MPA#8	SINT_SIG MPA#9	SINT_SIG MPA#A	SINT_SIG MPA#B	SINT_SIG MPA#C	SINT_SIG MPA#D	SINT_SIG MPA#E	SINT_SIG MPA#F
56	Not used							
57	Not used							
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA -BLE ERROR	UNCORREC -TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PTY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type4 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	MPA::RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA::RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA::RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA::RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA::RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA::RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA::RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA::RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (1/4)

	0	1	2	3	4	5	6	7
40	MPA::MPASTS							
	MPA INT	CHK3 MST	CHK3 SLV	0	0	CHK1B COM	CHK1B XR	MPINT
41	Not used							
42	Not used							
43	Not used							
44	MPA::SLVCHK3STS							
	SCANIF#0 ERR	SCANIF#1 ERR	SCANIF#2 ERR	SCANIF#3 ERR	0	0	CHK3 SLV A	CHK3 SLV B
45	Not used							
46	Not used							
47	Not used							
48	Not used							
49	Not used							
4A	Not used							
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (2/4)

	0	1	2	3	4	5	6	7
50	MPA::SCANIF0 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
51	MPA::SCANIF0 CNTER							
	0	0	0	0	0	0	0	PERR
52	MPA::SCANIF0 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
53	MPA::SCANIF0 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
54	MPA::SCANIF1 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
55	MPA::SCANIF1 CNTER							
	0	0	0	0	0	0	0	PERR
56	MPA::SCANIF1 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
57	MPA::SCANIF1 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
58	MPA::SCANIF2 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
59	MPA::SCANIF2 CNTER							
	0	0	0	0	0	0	0	PERR
5A	MPA::SCANIF2 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5B	MPA::SCANIF2 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5C	MPA::SCANIF3 ADRER							
	0	0	0	SCAN_ ACSERR	0	0	PERR2	PERR3
5D	MPA::SCANIF3 CNTER							
	0	0	0	0	0	0	0	PERR
5E	MPA::SCANIF3 INER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3
5F	MPA::SCANIF3 OUTER							
	0	0	0	0	PERR0	PERR1	PERR2	PERR3

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (3/4)

	0	1	2	3	4	5	6	7
60	MPA::SLVA SCSQER							
	ILGLMD	TMOUT	TMPER	TMPER	TMPER	TMPER	SQPER1	SQPER0
61	Not used							
62	Not used							
63	Not used							
64	MPA::SLVB SCSQER							
	ILGLMD	TMOUT	TMPER	TMPER	TMPER	TMPER	SQPER1	SQPER0
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type5 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (1/4)

	0	1	2	3	4	5	6	7
40	FCA::LEDSTAT							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
41	FCA::LEDADRDT (After PK_STAT read)							
	Address of LED BUS							
42	FCA::LEDADRDT (After PK_STAT read)							
	Data of LED BUS							
43	FCA::LEDCMD (After PK_STAT read)							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR DMD
44	FCA::LEDSTAT (After PK_STAT read)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	FCA::LEDSTAT (After PK_STAT read)							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
46	FCA::LEDADRDT (After LBUS_ERR read)							
	Address of LED BUS							
47	FCA::LEDADRDT (After LBUS_ERR read)							
	Data of LED BUS							
48	FCA::LEDCMD (After LBUS_ERR read)							
	Not used	Not used	Not used	Not used	Not used	Not used	LED BUS RD CMD	LED BUS WR DMD
49	FCA::LEDSTAT (After LBUS_ERR read)							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
4A	FCA::LEDSTAT (After LBUS_ERR read)							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
4B	Not used							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (2/4)

	0	1	2	3	4	5	6	7
50	Not used							
51	Not used							
52	Not used							
53	Not used							
54	Not used							
55	Not used							
56	Not used							
57	Not used							
58	Not used							
59	Not used							
5A	Not used							
5B	Not used							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	Not used							
62	Not used							
63	Not used							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type6 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (1/4)

	0	1	2	3	4	5	6	7
40	Threshold counter for the warning							
	CHA-1P							
41	Threshold counter for the warning							
	CHA-1Q							
42	Threshold counter for the warning							
	CHA-1R							
43	Threshold counter for the warning							
	CHA-1S							
44	Threshold counter for the warning							
	DKA-1B							
45	Threshold counter for the warning							
	DKA-1C							
46	Threshold counter for the warning							
	DKA-1D							
47	Threshold counter for the warning							
	DKA-1E							
48	Threshold counter for the warning							
	CSW-1A							
49	Threshold counter for the warning							
	CSW-1N							
4A	Threshold counter for the warning							
	CACHE-1T							
4B	Threshold counter for the warning							
	CACHE-1U							
4C	Not used							
4D	Not used							
4E	Not used							
4F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (2/4)

	0	1	2	3	4	5	6	7
50	Threshold counter for the warning							
	CHA-2V							
51	Threshold counter for the warning							
	CHA-2W							
52	Threshold counter for the warning							
	CHA-2X							
53	Threshold counter for the warning							
	CHA-2Y							
54	Threshold counter for the warning							
	DKA-2H							
55	Threshold counter for the warning							
	DKA-2J							
56	Threshold counter for the warning							
	DKA-2K							
57	Threshold counter for the warning							
	DKA-2L							
58	Threshold counter for the warning							
	CSW-2M							
59	Threshold counter for the warning							
	CSW-2Z							
5A	Threshold counter for the warning							
	CACHE-2F							
5B	Threshold counter for the warning							
	CACHE-2G							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (3/4)

	0	1	2	3	4	5	6	7
60		CHA-1P						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
61		CHA-1Q						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
62		CHA-1R						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
63		CHA-1S						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
64		DKA-1B						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
65		DKA-1C						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
66		DKA-1D						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
67		DKA-1E						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
68		CSW-1A						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
69		CSW-1N						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
6A		CACHE-1T						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
6B		CACHE-1U						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
6C		Not used						
6D		Not used						
6E		Not used						
6F		Not used						

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type7 (4/4)

	0	1	2	3	4	5	6	7
70		CHA-2V						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
71		CHA-2W						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
72		CHA-2X						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
73		CHA-2Y						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
74		DKA-2H						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
75		DKA-2J						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
76		DKA-2K						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
77		DKA-2L						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
78		CSW-2M						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
79		CSW-2Z						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
7A		CACHE-2F						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
7B		CACHE-2G						
	CEMODE	0	DC CTL (1.5V +10%)	DC CTL (1.5V -10%)	DC CTL (1.8V +10%)	DC CTL (1.8V -10%)	DC CTL (2.5V +10%)	DC CTL (2.5V -10%)
7C		Not used						
7D		Not used						
7E		Not used						
7F		Not used						

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (1/4)

	0	1	2	3	4	5	6	7
40	CARB::P0ERR0							
	P0DRINP-ERR	P0LRCERR	P0ENDC-ERR	P0SLRCERR	P0DROUT PERR	P0ORINP-ERR	P0WR1TO-ERR	CLKERR
41	CARB::P0ERR0							
	ABTCMP-ERR	ABTSEQP-ERR	P0SEQAP-ERR	P0SEQAC PERR	P0SEQAT PERR	P0SEQBT-ERR	P0J1CNT PERR	P0J4CNT PERR
42	CARB::P0ERR0							
	P0SEQBT PERR	P0SEQDP-ERR	P0S0CNT PERR	P0S1CNT PERR	P0WR1P-ERR	P0MICERR	P0MACS-ERR	T6PERR
43	Not used							
44	CARB::P1ERR0							
	P1DRINP-ERR	P1LRCERR	P1ENDC-ERR	P1SLRCERR	P1DROUT PERR	P1ORINP-ERR	P1WR1TO-ERR	CLKERR
45	CARB::P1ERR0							
	ABTCMP-ERR	ABTSEQP-ERR	P1SEQAP-ERR	P1SEQAC PERR	P1SEQAT PERR	P1SEQBT-ERR	P1J1CNT PERR	P1J4CNT PERR
46	CARB::P1ERR0							
	P1SEQBT PERR	P1SEQDP-ERR	P1S0CNT PERR	P1S1CNT PERR	P1WR1P-ERR	P1MICERR	P1MACS-ERR	T6PERR
47	Not used							
48	CARB::P2ERR0							
	P2DRINP-ERR	P2LRCERR	P2ENDC-ERR	P2SLRCERR	P2DROUT PERR	P2ORINP-ERR	P2WR1TO-ERR	CLKERR
49	CARB::P2ERR0							
	ABTCMP-ERR	ABTSEQP-ERR	P2SEQAP-ERR	P2SEQAC PERR	P2SEQAT PERR	P2SEQBT-ERR	P2J1CNT PERR	P2J4CNT PERR
4A	CARB::P2ERR0							
	P2SEQBT PERR	P2SEQDP-ERR	P2S0CNT PERR	P2S1CNT PERR	P2WR1P-ERR	P2MICERR	P2MACS-ERR	T6PERR
4B	Not used							
4C	CARB::P3ERR0							
	P3DRINP-ERR	P3LRCERR	P3ENDC-ERR	P3SLRCERR	P3DROUT PERR	P3ORINP-ERR	P3WR1TO-ERR	CLKERR
4D	CARB::P3ERR0							
	ABTCMP-ERR	ABTSEQP-ERR	P3SEQAP-ERR	P3SEQAC PERR	P3SEQAT PERR	P3SEQBT-ERR	P3J1CNT PERR	P3J4CNT PERR
4E	CARB::P3ERR0							
	P3SEQBT PERR	P3SEQDP-ERR	P3S0CNT PERR	P3S1CNT PERR	P3WR1P-ERR	P3MICERR	P3MACS-ERR	T6PERR
4F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (2/4)

	0	1	2	3	4	5	6	7
50		CARB::P4ERR0						
	P4DRINP-ERR	P4LRCERR	P4ENDC-ERR	P4SLRCERR	P4DROUT PERR	P4ORINP-ERR	P4WR1TO-ERR	CLKERR
51		CARB::P4ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P4SEQAP-ERR	P4SEQAC PERR	P4SEQAT PERR	P4SEQBT-ERR	P4J1CNT PERR	P4J4CNT PERR
52		CARB::P4ERR0						
	P4SEQBT PERR	P4SEQDP-ERR	P4S0CNT PERR	P4S1CNT PERR	P4WR1P-ERR	P4MICERR	P4MACS-ERR	T6PERR
53		Not used						
54		CARB::P5ERR0						
	P5DRINP-ERR	P5LRCERR	P5ENDC-ERR	P5SLRCERR	P5DROUT PERR	P5ORINP-ERR	P5WR1TO-ERR	CLKERR
55		CARB::P5ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P5SEQAP-ERR	P5SEQAC PERR	P5SEQAT PERR	P5SEQBT-ERR	P5J1CNT PERR	P5J4CNT PERR
56		CARB::P5ERR0						
	P5SEQBT PERR	P5SEQDP-ERR	P5S0CNT PERR	P5S1CNT PERR	P5WR1P-ERR	P5MICERR	P5MACS-ERR	T6PERR
57		Not used						
58		CARB::P6ERR0						
	P6DRINP-ERR	P6LRCERR	P6ENDC-ERR	P6SLRCERR	P6DROUT PERR	P6ORINP-ERR	P6WR1TO-ERR	CLKERR
59		CARB::P6ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P6SEQAP-ERR	P6SEQAC PERR	P6SEQAT PERR	P6SEQBT-ERR	P6J1CNT PERR	P6J4CNT PERR
5A		CARB::P6ERR0						
	P6SEQBT PERR	P6SEQDP-ERR	P6S0CNT PERR	P6S1CNT PERR	P6WR1P-ERR	P6MICERR	P6MACS-ERR	T6PERR
5B		Not used						
5C		CARB::P7ERR0						
	P7DRINP-ERR	P7LRCERR	P7ENDC-ERR	P7SLRCERR	P7DROUT PERR	P7ORINP-ERR	P7WR1TO-ERR	CLKERR
5D		CARB::P7ERR0						
	ABTCMP-ERR	ABTSEQP-ERR	P7SEQAP-ERR	P7SEQAC PERR	P7SEQAT PERR	P7SEQBT-ERR	P7J1CNT PERR	P7J4CNT PERR
5E		CARB::P7ERR0						
	P7SEQBT PERR	P7SEQDP-ERR	P7S0CNT PERR	P7S1CNT PERR	P7WR1P-ERR	P7MICERR	P7MACS-ERR	T6PERR
5F		Not used						

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (3/4)

	0	1	2	3	4	5	6	7
60		CARB::C0ERR0						
	C0 ORINPER	C0 DRINPER	C0 PLRC ERR	C0 ENDC ERR	C0SLRC ERR	C0 DROPERR	0	0
61		CARB::C0ERR0						
	C0 RD1TMO	C0 RD2TMO	C0 WR2TMO	0	0	0	0	0
62		CARB::C0ERR1						
	C0 SEQCPERR	C0 TCNTPERR	C0 DRPINPERR	C0 SEQDPERR	C0 IPPINPERR0	C0 IPPINPERR1	0	0
63		CARB::C0ERR1						
	C0 RD1TMR-PER	C0 RD2TMR-PER	C0 WR2TMR-PER	C0 STMPERR	C0 SCNPERR	0	0	0
64		CARB::C1ERR0						
	C1 ORINPER	C1 DRINPER	C2 PLRC ERR	C1 ENDC ERR	C1SLRC ERR	C1 DROPERR	0	0
65		CARB::C1ERR0						
	C1 RD1TMO	C1 RD2TMO	C1 WR2TMO	0	0	0	0	0
66		CARB::C1ERR1						
	C1 SEQCPERR	C1 TCNTPERR	C1 DRPINPERR	C1 SEQDPERR	C1 IPPINPERR0	C1 IPPINPERR1	0	0
67		CARB::C1ERR1						
	C1 RD1TMR-PER	C1 RD2TMR-PER	C1 WR2TMR-PER	C1 STMPERR	C1 SCNPERR	0	0	0
68		CARB::C2ERR0						
	C2 ORINPER	C2 DRINPER	C2 PLRC ERR	C2 ENDC ERR	C2SLRC ERR	C2 DROPERR	0	0
69		CARB::C2ERR0						
	C2 RD1TMO	C2 RD2TMO	C2 WR2TMO	0	0	0	0	0
6A		CARB::C2ERR1						
	C2 SEQCPERR	C2 TCNTPERR	C2 DRPINPERR	C2 SEQDPERR	C2 IPPINPERR0	C2 IPPINPERR1	0	0
6B		CARB::C2ERR0						
	C2 RD1TMR-PER	C2 RD2TMR-PER	C2 WR2TMR-PER	C2 STMPERR	C2 SCNPERR	0	0	0
6C		CARB::C3ERR0						
	C3 ORINPER	C3 DRINPER	C3 PLRC ERR	C3 ENDC ERR	C3SLRC ERR	C3 DROPERR	0	0
6D		CARB::C3ERR1						
	C3 RD1TMO	C3 RD2TMO	C3 WR2TMO	0	0	0	0	0
6E		CARB::C3ERR1						
	C3 SEQCPERR	C3 TCNTPERR	C3 DRPINPERR	C3 SEQDPERR	C3 IPPINPERR0	C3 IPPINPERR1	0	0
6F		CARB::C3ERR1						
	C3 RD1TMR-PER	C3 RD2TMR-PER	C3 WR2TMR-PER	C3 STMPERR	C3 SCNPERR	0	0	0

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type8 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (1/4)

	0	1	2	3	4	5	6	7
40	Not used							
41	Not used							
42	SMA:: BCAST REG5 MASK							
	BC REG5 MASK bit 20	BC REG5 MASK bit 21	BC REG5 MASK bit 22	BC REG5 MASK bit 23	BC REG5 MASK bit 24	BC REG5 MASK bit 25	BC REG5 MASK bit 26	BC REG5 MASK bit 27
43	SMA:: BCAST REG5 MASK							
	BC REG5 MASK bit 30	BC REG5 MASK bit 31	BC REG5 MASK bit 32	BC REG5 MASK bit 33	BC REG5 MASK bit 34	BC REG5 MASK bit 35	BC REG5 MASK bit 36	BC REG5 MASK bit 37
44	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#0	SC_MASK MPA#1	SC_MASK MPA#2	SC_MASK MPA#3	SC_MASK MPA#4	SC_MASK MPA#5	SC_MASK MPA#6	SC_MASK MPA#7
45	SMA::SCINT OUTPUT MASK							
	SC_MASK MPA#8	SC_MASK MPA#9	SC_MASK MPA#A	SC_MASK MPA#B	SC_MASK MPA#C	SC_MASK MPA#D	SC_MASK MPA#E	SC_MASK MPA#F
46	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
47	SMA::MP STATUS TIMEOUT DATA							
	MPST_TODT							
48	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
49	SMA::VALID TIMER TIMEOUT DATA							
	VAL_TODT							
4A	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4B	SMA::SCINT TIMEOUT DATA							
	SC_TODT							
4C	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#0	SCCNT_PERR MPA#1	SCCNT_PERR MPA#2	SCCNT_PERR MPA#3	SCCNT_PERR MPA#4	SCCNT_PERR MPA#5	SCCNT_PERR MPA#6	SCCNT_PERR MPA#7
4D	SMA::SCAN COUNTER PARITY ERROR							
	SCCNT_PERR MPA#8	SCCNT_PERR MPA#9	SCCNT_PERR MPA#A	SCCNT_PERR MPA#B	SCCNT_PERR MPA#C	SCCNT_PERR MPA#D	SCCNT_PERR MPA#E	SCCNT_PERR MPA#F
4E	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#0	VALCNT_PERR MPA#1	VALCNT_PERR MPA#2	VALCNT_PERR MPA#3	VALCNT_PERR MPA#4	VALCNT_PERR MPA#5	VALCNT_PERR MPA#6	VALCNT_PERR MPA#7
4F	SMA::VALID COUNTER PARITY ERROR							
	VALCNT_PERR MPA#8	VALCNT_PERR MPA#9	VALCNT_PERR MPA#A	VALCNT_PERR MPA#B	VALCNT_PERR MPA#C	VALCNT_PERR MPA#D	VALCNT_PERR MPA#E	VALCNT_PERR MPA#F

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (2/4)

	0	1	2	3	4	5	6	7
50	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#0	SCSEQ_ERR MPA#1	SCSEQ_ERR MPA#2	SCSEQ_ERR MPA#3	SCSEQ_ERR MPA#4	SCSEQ_ERR MPA#5	SCSEQ_ERR MPA#6	SCSEQ_ER R MPA#7
51	SMA::SCAN SEQUENCER ERROR							
	SCSEQ_ERR MPA#8	SCSEQ_ERR MPA#9	SCSEQ_ERR MPA#A	SCSEQ_ERR MPA#B	SCSEQ_ERR MPA#C	SCSEQ_ERR MPA#D	SCSEQ_ERR MPA#E	SCSEQ_ER R MPA#F
52	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#0	SINT_OUT_ ERR MPA#1	SINT_OUT_ ERR MPA#2	SINT_OUT_ ERR MPA#3	SINT_OUT_ ERR MPA#4	SINT_OUT_ ERR MPA#5	SINT_OUT_ ERR MPA#6	SINT_OUT_ ERR MPA#7
53	SMA::SCINT OUT ERROR							
	SINT_OUT_ ERR MPA#8	SINT_OUT_ ERR MPA#9	SINT_OUT_ ERR MPA#A	SINT_OUT_ ERR MPA#B	SINT_OUT_ ERR MPA#C	SINT_OUT_ ERR MPA#D	SINT_OUT_ ERR MPA#E	SINT_OUT_ ERR MPA#F
54	SMA::SCINT SIGNAL							
	SINT_SIG MPA#0	SINT_SIG MPA#1	SINT_SIG MPA#2	SINT_SIG MPA#3	SINT_SIG MPA#4	SINT_SIG MPA#5	SINT_SIG MPA#6	SINT_SIG MPA#7
55	SMA::SCINT SIGNAL							
	SINT_SIG MPA#8	SINT_SIG MPA#9	SINT_SIG MPA#A	SINT_SIG MPA#B	SINT_SIG MPA#C	SINT_SIG MPA#D	SINT_SIG MPA#E	SINT_SIG MPA#F
56	Not used							
57	Not used							
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA -BLE ERROR	UNCORREC -TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PTY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type9 (4/4)

	0	1	2	3	4	5	6	7
70	MPA:: MPAINTSTS							
	0	0	0	0	0	0	SCINT0	SCINT1
71	MPA:: MPAINTSTS							
	XR BC0	XR BC1	XR BC2	XR BC3	XR BC4	BCREQ	BCINT0	BCINT1
72	SMA:: SMACNTRL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA:: SMACNTRL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA:: SMASTATS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA:: SMASTATS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA:: SMASTATS							
	PK VER				LSI VER			
78	MPA:: RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA:: RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA:: RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA:: RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA:: RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA:: RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA:: RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA:: RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (1/4)

	0	1	2	3	4	5	6	7
40	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 00	BC REG0 MASK bit 01	BC REG0 MASK bit 02	BC REG0 MASK bit 03	BC REG0 MASK bit 04	BC REG0 MASK bit 05	BC REG0 MASK bit 06	BC REG0 MASK bit 07
41	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 10	BC REG0 MASK bit 11	BC REG0 MASK bit 12	BC REG0 MASK bit 13	BC REG0 MASK bit 14	BC REG0 MASK bit 15	BC REG0 MASK bit 16	BC REG0 MASK bit 17
42	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 20	BC REG0 MASK bit 21	BC REG0 MASK bit 22	BC REG0 MASK bit 23	BC REG0 MASK bit 24	BC REG0 MASK bit 25	BC REG0 MASK bit 26	BC REG0 MASK bit 27
43	SMA:: BCAST REG0 MASK							
	BC REG0 MASK bit 30	BC REG0 MASK bit 31	BC REG0 MASK bit 32	BC REG0 MASK bit 33	BC REG0 MASK bit 34	BC REG0 MASK bit 35	BC REG0 MASK bit 36	BC REG0 MASK bit 37
44	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 00	BC REG1 MASK bit 01	BC REG1 MASK bit 02	BC REG1 MASK bit 03	BC REG1 MASK bit 04	BC REG1 MASK bit 05	BC REG1 MASK bit 06	BC REG1 MASK bit 07
45	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 10	BC REG1 MASK bit 11	BC REG1 MASK bit 12	BC REG1 MASK bit 13	BC REG1 MASK bit 14	BC REG1 MASK bit 15	BC REG1 MASK bit 16	BC REG1 MASK bit 17
46	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 20	BC REG1 MASK bit 21	BC REG1 MASK bit 22	BC REG1 MASK bit 23	BC REG1 MASK bit 24	BC REG1 MASK bit 25	BC REG1 MASK bit 26	BC REG1 MASK bit 27
47	SMA:: BCAST REG1 MASK							
	BC REG1 MASK bit 30	BC REG1 MASK bit 31	BC REG1 MASK bit 32	BC REG1 MASK bit 33	BC REG1 MASK bit 34	BC REG1 MASK bit 35	BC REG1 MASK bit 36	BC REG1 MASK bit 37
48	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 00	BC REG2 MASK bit 01	BC REG2 MASK bit 02	BC REG2 MASK bit 03	BC REG2 MASK bit 04	BC REG2 MASK bit 05	BC REG2 MASK bit 06	BC REG2 MASK bit 07
49	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 10	BC REG2 MASK bit 11	BC REG2 MASK bit 12	BC REG2 MASK bit 13	BC REG2 MASK bit 14	BC REG2 MASK bit 15	BC REG2 MASK bit 16	BC REG2 MASK bit 17
4A	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 20	BC REG2 MASK bit 21	BC REG2 MASK bit 22	BC REG2 MASK bit 23	BC REG2 MASK bit 24	BC REG2 MASK bit 25	BC REG2 MASK bit 26	BC REG2 MASK bit 27
4B	SMA:: BCAST REG2 MASK							
	BC REG2 MASK bit 30	BC REG2 MASK bit 31	BC REG2 MASK bit 32	BC REG2 MASK bit 33	BC REG2 MASK bit 34	BC REG2 MASK bit 35	BC REG2 MASK bit 36	BC REG2 MASK bit 37
4C	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 00	BC REG3 MASK bit 01	BC REG3 MASK bit 02	BC REG3 MASK bit 03	BC REG3 MASK bit 04	BC REG3 MASK bit 05	BC REG3 MASK bit 06	BC REG3 MASK bit 07
4D	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 10	BC REG3 MASK bit 11	BC REG3 MASK bit 12	BC REG3 MASK bit 13	BC REG3 MASK bit 14	BC REG3 MASK bit 15	BC REG3 MASK bit 16	BC REG3 MASK bit 17
4E	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 20	BC REG3 MASK bit 21	BC REG3 MASK bit22	BC REG3 MASK bit 23	BC REG3 MASK bit 24	BC REG3 MASK bit 25	BC REG3 MASK bit 26	BC REG3 MASK bit 27
4F	SMA:: BCAST REG3 MASK							
	BC REG3 MASK bit 30	BC REG3 MASK bit 31	BC REG3 MASK bit 32	BC REG3 MASK bit 33	BC REG3 MASK bit 34	BC REG3 MASK bit 35	BC REG3 MASK bit 36	BC REG3 MASK bit 37

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (2/4)

	0	1	2	3	4	5	6	7
50	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 00	BC REG4 MASK bit 01	BC REG4 MASK bit 02	BC REG4 MASK bit 03	BC REG4 MASK bit 04	BC REG4 MASK bit 05	BC REG4 MASK bit 06	BC REG4 MASK bit 07
51	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 10	BC REG4 MASK bit 11	BC REG4 MASK bit 12	BC REG4 MASK bit 13	BC REG4 MASK bit 14	BC REG4 MASK bit 15	BC REG4 MASK bit 16	BC REG4 MASK bit 17
52	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 20	BC REG4 MASK bit 21	BC REG4 MASK bit 22	BC REG4 MASK bit 23	BC REG4 MASK bit 24	BC REG4 MASK bit 25	BC REG4 MASK bit 26	BC REG4 MASK bit 27
53	SMA:: BCAST REG4 MASK							
	BC REG4 MASK bit 30	BC REG4 MASK bit 31	BC REG4 MASK bit 32	BC REG4 MASK bit 33	BC REG4 MASK bit 34	BC REG4 MASK bit 35	BC REG4 MASK bit 36	BC REG4 MASK bit 37
54	SMA::BCINT OUT ERROR							
	BINT_OUT_ERR MPA#0	BINT_OUT_ERR MPA#1	BINT_OUT_ERR MPA#2	BINT_OUT_ERR MPA#3	BINT_OUT_ERR MPA#4	BINT_OUT_ERR MPA#5	BINT_OUT_ERR MPA#6	BINT_OUT_ERR MPA#7
55	SMA::BCINT OUT ERROR							
	BINT_OUT_ERR MPA#8	BINT_OUT_ERR MPA#9	BINT_OUT_ERR MPA#A	BINT_OUT_ERR MPA#B	BINT_OUT_ERR MPA#C	BINT_OUT_ERR MPA#D	BINT_OUT_ERR MPA#E	BINT_OUT_ERR MPA#F
56	SMA::BCINT SIGNAL							
	BINT_SIG MPA#0	BINT_SIG MPA#1	BINT_SIG MPA#2	BINT_SIG MPA#3	BINT_SIG MPA#4	BINT_SIG MPA#5	BINT_SIG MPA#6	BINT_SIG MPA#7
57	SMA::BCINT SIGNAL							
	BINT_SIG MPA#8	BINT_SIG MPA#9	BINT_SIG MPA#A	BINT_SIG MPA#B	BINT_SIG MPA#C	BINT_SIG MPA#D	BINT_SIG MPA#E	BINT_SIG MPA#F
58	Not used							
59	SMA::PATH0 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
5A	SMA::PATH0 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
5B	SMA::PATH0 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
5C	SMA::PATH0 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
5D	SMA::PATH0 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
5E	SMA::PATH0 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
5F	SMA::PATH0 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	SMA::PATH1 ERROR STATUS							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
62	SMA::PATH1 ERROR STATUS							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
63	SMA::PATH1 ERROR STATUS							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	Not used	Not used	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
64	SMA::PATH1 ERROR DETAIL							
	RX CMD PARITY ERROR	RX ADR PARITY ERROR	RX WDT PARITY ERROR	Not used	SYNC0 UNDER ERROR	SYNC1 UNDER ERROR	SYNC0 OVER ERROR	SYNC1 OVER ERROR
65	SMA::PATH1 ERROR DETAIL							
	LRC ERROR	LRC COMPERE ERROR	LOCK COMMAND ERROR	R/W COMMAND ERROR	ILLEGAL LOCK DBL ERROR	DOUBLE LOCK ERROR	LOCK ACCESS OVER(ENT)	Not used
66	SMA::PATH1 ERROR DETAIL							
	CMD PGEN ERROR	ADR PGEN ERROR	WDT PGEN ERROR	PCB PARITY ERROR	PAB PARITY ERROR	PWB PARITY ERROR	PCB LOCK COMMAND ERROR	PCB R/W COMMAND ERROR
67	SMA::PATH1 ERROR DETAIL							
	Not used	Not used	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	Not used	PATH SEQUENCE R ERROR	REQ COUNTER PARITY ERROR	LOCK COUNTER PATH ERROR
68	SMA::BOARD ERROR STATUS							
	MCB PARITY ERROR	MAB PARITY ERROR	MWB PARITY ERROR	SIMMSEL PARITY ERROR	MEMPATHA DR PARITY ERROR	RDTLT NOTHING ERROR	ICB PARITY ERROR	IAB PARITY ERROR
69	SMA::BOARD ERROR STATUS							
	IWB PARYTY ERROR	I/O PATHADR PARITY ERROR	PDADR OUTPUT ERROR	LOCK ADR PARITY ERROR	LOCK WAIT TIMEOUT	LOCK PROTOCOL ERROR	ANSWER PATH UNMATCH	SLOT PARITY ERROR
6A	SMA::BOARD ERROR STATUS							
	CLOCK ERROR	REFRESH ERROR	TIMER PARITY ERROR	ARBITER ERROR	WT WEQ PARITY ERROR	RD SEQ PARITY ERROR	MEM SEQ PARITY ERROR	I/O SEQ PARITY ERROR
6B	SMA::BOARD ERROR STATUS							
	ECC GENERATE ERROR	SMDT OUTPUT ERROR	BSSWEN OUTPUT ERROR	VALID CNT PARITY ERROR	SCAN CNT PARITY ERROR	SCAn SEQ ERROR	BCINT OUTPUT ERROR	SCINT OUTPUT ERROR
6C	Not used							
6D	Not used							
6E	SMA::BOARD ERROR DETAIL							
	Not used	Not used	Not used	Not used	Not used	MEMORY ARBITER ERROR	LOCK ARBITER ERROR	I/O ARBITER ERROR
6F	SMA::BOARD ERROR DETAIL							
	Not used	CLOCK GENERATE ERROR	CLOCK CNT PTY ERROR	CLOCK FREQUEN-CY ERROR	Not used	INITIAL CNT PARITY ERROR	REFRESH CNT PARITY ERROR	REFRESH PROTCOL ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type10 (4/4)

	0	1	2	3	4	5	6	7
70	MPA:: MPAINTSTS							
	0	0	0	0	0	0	SCINT0	SCINT1
71	MPA::MPA INTSTS							
	XR BC0	XR BC1	XR BC2	XR BC3	XR BC4	BCREQ	BCINT0	BCINT1
72	SMA::SMA CONTROL							
	DBG SIG	Not used	Not used	Not used	Not used	BSSW CHK EN	ENT WAIT EN	ENTOFF RST EN
73	SMA::SMA CONTROL							
	SMPSDWN EN	CLK CHK EN	ECC ADR MSK	DIAG EN	DUMP MODE	PWR DWN EN	DT RVS INH	REF MODE
74	Not used							
75	SMA::SMA STATUS							
	Not used	Not used	Not used	Not used	SLOT (Side B)	SLOT (Side A)	DISC MODE	PWR DWN MODE
76	SMA::SMA STATUS							
	DISC REQ	SELF REF	SMPS DWN	PS DTCT	TIM EN	ALL LOCK	MEM PDY	SM EN
77	SMA::SMA STATUS							
	PK VER				LSI VER			
78	MPA:: RXAEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
79	MPA:: RXAEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7A	MPA:: RXAEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7B	MPA:: RXAEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR
7C	MPA:: RXBEDT							
	MPST INT	MPST STATUS FLAG	MPST VALID	MPST TIMEOUT	SCAN INT	SCAN READDATA FLAG	SCAN STATUS FLAG	SCAN TIMEOUT
7D	MPA:: RXBEDT							
	ALL LOCK BUSY	MEMORY NOT READY	BACKUP BUSY	ALL LOCK ERROR	MEMORY DISCONNE-CT BUSY	ILLEGAL ADDRESS ERROR	DIMM INVALID ERROR	ILLEGAL LOCK ERROR
7E	MPA:: RXBEDT							
	REQUEST TIMEOUT	PRB TIMEOUT	LOCK WAIT TIMEOUT	LOCK OFF TIMEOUT	PRB PARITY ERROR	CHECK CODE ERROR	PATH ANY ERROR	PATH BORAD ERROR
7F	MPA:: RXBEDT							
	CORRECTA-BLE ERROR	UNCORREC-TABLE ERROR	I/O REG PARITY ERROR	0	0	SM PS DOWN	MCTL SIGNAL ERROR	COMMON BOARD ERROR

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type11 (1/4)

	0	1	2	3	4	5	6	7
40	CMF::DXBFERR0							
	DSEQPER	DTPCHKERR	CACRDSPE	CACRDAPE	CACRDCPE	CACRDDPE	Not used	Not used
41	CMF::DXBFERR0							
	Not used	Not used	CACWRSPE	CACWRAPE	CACWRCPE	Not used	CACWRWER	CACWRECE
42	CMF::DXBFERR0							
	DSEQPERR	DTPCHKERR	PBFSTSPE	PBFSTAPE	PBFSTCPE	PBFSTDPE	Not used	Not used
43	CMF::DXBFERR0							
	Not used	Not used	PBFF00ESPE	PBFFEAPE	PBFFECPE	Not used	PBFFEWER	PBFFEECE
44	CMF::DXBFERR1							
	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used
45	CMF::DXBFERR1							
	0	DKUSTAT	ACKERR	STSPERR	RDTPERR	DKUERR-OUT	RDBSY	WTBSY
46	CMF::DXBFERR1							
47	CMF::DXBFERR1							
48	CMF::DXBFERR2							
	ECC Error Address							
49	CMF::DXBFERR2							
	ECC Error Address							
4A	CMF::DXBFERR2							
	ECC Error Address							
4B	CMF::DXBFERR2							
	ECC Error Address							
4C	CMF::DXBFERR3							
	ECC Error Data							
4D	CMF::DXBFERR3							
	ECC Error Data							
4E	CMF::DXBFERR3							
	ECC Error Data							
4F	CMF::DXBFERR3							
	ECC Error Data							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type11 (2/4)

	0	1	2	3	4	5	6	7
50	CMF::DXBFERR4							
	ECC Error ECC Code							
51	CMF::DXBFERR4							
	ECC Error ECC Code							
52	CMF::DXBFERR4							
	ECC Error ECC Code							
53	CMF::DXBFERR4							
	ECC Error ECC Code							
54	Not used							
55	Not used							
56	Not used							
57	Not used							
58	Not used							
59	Not used							
5A	Not used							
5B	Not used							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type11 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	Not used							
62	Not used							
63	Not used							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type11 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type12 (1/4)

	0	1	2	3	4	5	6	7
40	ORCA::DXBF_ERR0							
	SEQPER	TIMPER	CACRSPE	CACRAPE	CACRCPE	CACRDPE	Not used	Not used
41	ORCA::DXBF_ERR0							
	Not used	Not used	CACWSPE	CACWAPE	CACWCPE	Not used	CACWWER	CACWECE
42	ORCA::DXBF_ERR0							
	SEQPER	TIMPER	PCIWSPE	PCIWAPE	PCIWCPE	PCIWDPE	Not used	Not used
43	ORCA::DXBF_ERR0							
	Not used	Not used	PCIRSPE	PCIRAPE	PCIRCPE	Not used	PCIRWER	PCIRECE
44	ORCA::DXBF_ERR0_MO							
	SEQPER	TIMPER	CACRSPE	CACRAPE	CACRCPE	CACRDPE	Not used	Not used
45	ORCA::DXBF_ERR0_MO							
	Not used	Not used	CACWSPE	CACWAPE	CACWCPE	Not used	CACWWER	CACWECE
46	ORCA::DXBF_ERR0_MO							
	SEQPER	TIMPER	PCIWSPE	PCIWAPE	PCIWCPE	PCIWDPE	Not used	Not used
47	ORCA::DXBF_ERR0_MO							
	Not used	Not used	PCIRSPE	PCIRAPE	PCIRCPE	Not used	PCIRWER	PCIRECE
48	ORCA::DXBF_ERR2							
	ECC Error Address							
49	ORCA::DXBF_ERR2							
	ECC Error Address							
4A	ORCA::DXBF_ERR2							
	ECC Error Address							
4B	ORCA::DXBF_ERR2							
	ECC Error Address							
4C	ORCA::DXBF_ERR3							
	ECC Error Data							
4D	ORCA::DXBF_ERR3							
	ECC Error Data							
4E	ORCA::DXBF_ERR3							
	ECC Error Data							
4F	ORCA::DXBF_ERR3							
	ECC Error Data							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type12 (2/4)

	0	1	2	3	4	5	6	7
50	ORCA::DXBF_ERR4							
	ECC Error ECC Code							
51	ORCA::DXBF_ERR4							
	ECC Error ECC Code							
52	ORCA::DXBF_ERR4							
	ECC Error ECC Code							
53	ORCA::DXBF_ERR4							
	ECC Error ECC Code							
54	Not used							
55	Not used							
56	Not used							
57	Not used							
58	Not used							
59	Not used							
5A	Not used							
5B	Not used							
5C	Not used							
5D	Not used							
5E	Not used							
5F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type12 (3/4)

	0	1	2	3	4	5	6	7
60	Not used							
61	Not used							
62	Not used							
63	Not used							
64	Not used							
65	Not used							
66	Not used							
67	Not used							
68	Not used							
69	Not used							
6A	Not used							
6B	Not used							
6C	Not used							
6D	Not used							
6E	Not used							
6F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type12 (4/4)

	0	1	2	3	4	5	6	7
70	Not used							
71	Not used							
72	Not used							
73	Not used							
74	Not used							
75	Not used							
76	Not used							
77	Not used							
78	Not used							
79	Not used							
7A	Not used							
7B	Not used							
7C	Not used							
7D	Not used							
7E	Not used							
7F	Not used							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type13 (1/4)

	0	1	2	3	4	5	6	7
40	Faulure part 3							
	Not used							
41	Faulure part 2							
	Not used							
42	Faulure part 1							
	Not used							
43	Faulure part 0							
	DRAM failure	MCH failure	P64H2 failure	Not used	Not used	Not used	Not used	Not used
44	DRAM error Detection time 3							
45	DRAM error Detection time 2							
46	DRAM error Detection time 1							
47	DRAM error Detection time 0							
48	DRAM_NERR							
49	DRAM_FERR							
4A	DRAM_CELOG_SYNDROME Register value 1							
4B	DRAM_CELOG_SYNDROME Register value 0							
4C	DRB Register value 13							
	DRB0 Register value = Total memory in row0 (in 64MB increments) (Pentium will store the DRAM address information here (DRAM Row Boundary Register))							
4D	DRB Register value 12							
	DRB1 Register value = Total memory in row0+row1 (in 64MB increments)							
4F	DRB Register value 11							
	DRB1 Register value = Total memory in row0+row1+row2+row3 (in 64MB increments)							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type13 (2/4)

	0	1	2	3	4	5	6	7
50	DRB Register value 03							
	DRB1 Register value = Total memory in row0+row1+row2+row3+row4 (in 64MB increments)							
51	DRB Register value 02							
	DRB1 Register value = Total memory in row0+row1+row2+row3+row4+row5 (in 64MB increments)							
52	DRB Register value 01							
	DRB1 Register value = Total memory in row0+row1+row2+row3---+row6 (in 64MB increments)							
53	DRB Register value00							
	DRB7 Register value = Total memory in row0+row1+row2+row3---+row7 (in 64MB increments)							
54	DRAM_CELOG_ADD3							
55	DRAM_CELOG_ADD2							
56	DRAM_CELOG_ADD1							
57	DRAM_CELOG_ADD0							
58	Hub Interface B / MCH Side Detection time 3							
59	Hub Interface B / MCH Side Detection time 2							
5A	Hub Interface B / MCH Side Detection time 1							
5B	Hub Interface B / MCH Side Detection time 0							
5C	(Reserved)							
5D	(Reserved)							
5E	HIB_NERR							
5F	HIB_FERR							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type13 (3/4)

	0	1	2	3	4	5	6	7
60	Hub Interface B / P64H2 Side Detection time 3							
61	Hub Interface B / P64H2 Side Detection time 2							
62	Hub Interface B / P64H2 Side Detection time 1							
63	Hub Interface B / P64H2 Side Detection time 0							
64	(Reserved)							
65	RAS_STS2							
66	RAS_STS1							
67	RAS_STS0							
68	RAS_HAL3							
69	RAS_HAL2							
6A	RAS_HAL1							
6B	RAS_HAL0							
6C	RAS_HAH3							
6D	RAS_HAH2							
6E	RAS_HAH1							
6F	RAS_HAH0							

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Byte27 = FF (Cache Memory/Shared Memory/SM Side/Scan/LED BUS/Abnormal MODE/ CARB error/Correctable error /Warning) Byte 40-7F Common detail information : Type13 (4/4)

	0	1	2	3	4	5	6	7
70	RAS_D03							
71	RAS_D02							
72	RAS_D01							
73	RAS_D00							
74	RAS_D13							
75	RAS_D12							
76	RAS_D11							
77	RAS_D10							
78	RAS_D23							
79	RAS_D22							
7A	RAS_D21							
7B	RAS_D20							
7C	RAS_D33							
7D	RAS_D32							
7E	RAS_D31							
7F	RAS_D30							

*: When an error occurs in register access, treat the value as ‘FF’.

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Byte0D : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x‘6’)				Format (x‘3’)			
27	Operation byte of LR/LRE command parameter							
28	Auxiliary byte of LR/LRE command parameter							
29	Byte 2 for LR/LRE command							
2A	Reserved							
2B								
2C	Search parameter of LR command(CCHHR)							
2D	or							
2E	Record ID of re-execution command(R)							
2F								
30	Sector number to re-execute the LR command							
31	TLF for LR/LRE command							
32								
33	Operation byte = 0x3F :LRE External operation byte others :Reserved							
34	SSID (Low) of self subsystem							
35								
36	Exception code (x‘08C1’)							
37								
38	Log and message control (x‘05’)							
39	Program action code (x‘10’)							
3A	Configuration information							
3B								
3C	Not used (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

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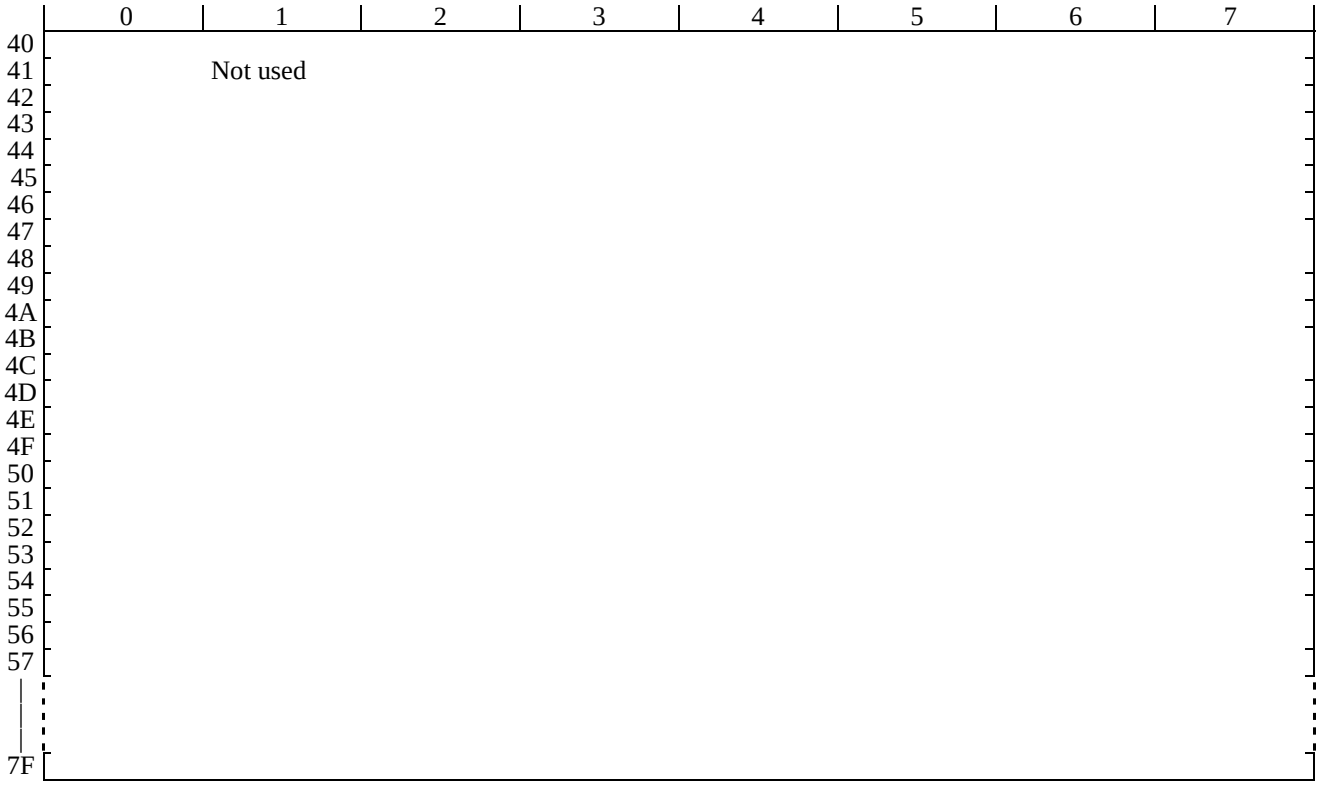
Byte0D : Bit1 = 1 & Byte36-37 = 08C1 (Machine Condition Exception) (2/2)



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Byte0D : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception: Incomplete Domain) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Content (x‘6’)				Format (x‘4’)			
27	Operation byte of LR/LRE command parameter							
28	Extension operation byte of LR/LRE command parameter							
29	Head address of extent (DX command parameter)							
2A								
2B								
2C								
2D								
2E	Path group ID (byte 1 to 7 of the ID by the last Set Path Group ID command)							
2F								
30								
31								
32								
33								
34	SSID (Low) of self subsystem							
35								
36	Exception code (x‘0212’)							
37								
38	Log and message control (x‘05’)							
39	Program action code (x‘10’)							
3A	Configuration information							
3B								
3C	Not used (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

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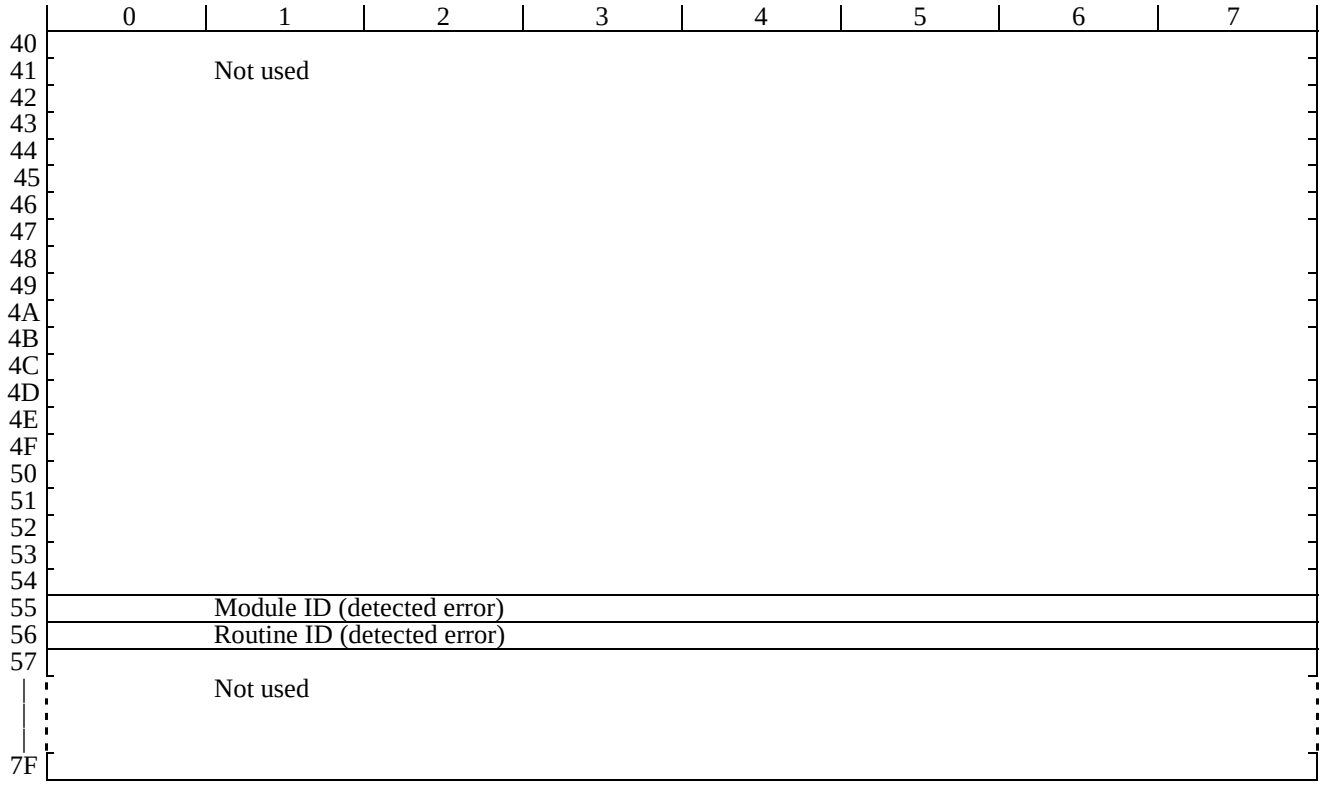
Byte0D : Bit1 = 1 & Byte36-37 = 0212 (Command Sequence Exception : Incomplete Domain) (2/2)



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Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type (x‘24’ :DKU87I-3)							
26	Content				Format (x‘1’)			
27	Sector number (Note 1)							
28	Cylinder address (Note 1)							
29								
2A	Head address (Note 1)							
2B								
2C	Record number (Note 1)							
2D	Error displacement (Note 1)							
2E								
2F	Drive serial number (x‘0C’) +							
30	(x‘24’) +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception class (x‘4’)				Message (Note 2)			
37	Correction flag (Note 3)							
38	Log and message control (x‘08’)							
39	Program action code (x‘91’)							
3A	Configuration information							
3B								
3C	Not used (x‘01’)							
3D	Cylinder address							
3E								
3F	Head address							

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Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (2/3)

	0	1	2	3	4	5	6	7
40		Causal Key code						
41		Causal Format/Message						
42		Causal Module ID						
43		Causal Routine ID						
44		VDEV number, slot number						
45								
46								
47								
48		Slot status						
49								
4A								
4B								
4C		Staging bit map/Dirty bit map						
4D								
4E								
4F								
50		Current subblock number						
51		EXIT falg (Note 4)						
52		Slot failure information (Note 5)						
53		Obtained information flat (Note 6)						
54		Head subblock number for HIT/MISS decision + Remain subblock count						
55		(when byte36 is x‘40/41/42/43’) / PACC in CBUF (when byte36 is x‘45’)						
56		Not used (when byte36 is x‘40/41/42/43’) /						
57		PAHF in CBUF (when byte36 is x‘45’)						
58		Not used (when byte36 is x‘40/41/42/43’) /						
59		Current CC in JCB (when byte36 is x‘45’)						
5A		Not used (when byte36 is x‘40/41/42/43’) /						
5B		Current HH in JCB (when byte36 is x‘45’)						
5C								
⋮		Reserved						
7F								

(Note 1) Not determined for occurrence in HA or RO

(Note 2) Contents of message

x'0' : Data check in HA field
x'1' : Data check in C field
x'2' : Data check in K field
x'3' : Data check in D field
x'4' : Missing SYNC byte in HA field
x'5' : Missing SYNC byte in C field (PA error)
x'6' : Missing SYNC byte in K field
x'7' : Missing SYNC byte in D field
x'8' : Not used
x'9' : Missing AM during retry
x'A'to x'F' : Not used

(Note 3) Contents of correctionflag

Bits 0 and 1 : ECC correction bit
10 : Correctable (Recovered)
11 : Uncorrectable
Bit 2 : offset active
Bits 3 to 7 : Not used

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Byte0D : Bit1 = 1 & Byte36-37 = 4XXX (Data exception) (3/3)

(Note 4) EXIT flag

x'08' : CHL I/F CHK2 timeover
x'0D' : EOF
x'0E' : DSB=0E requested
x'0F' : Logical error
x'1E' : Make sense only
x'1F' : Logical error (make sense only)
x'30' : Selective reset requested
x'40' : 'Staging' requested
x'41' : 'Waiting free segment' requested
x'42' : 'Timeover of waiting for staging' requested
x'43' : 'Staging for PA mismatch' requested
x'45' : 'Destaging' requested
x'46' : 'High priority destaging' requested
x'47' : 'Pseud-through process' requested
x'4B' : 'DSB=4E retry' requested (data transfer)
x'4E' : 'DSB=4E retry' requested (DSB=4E retry)
x'4F' :STG requested (Read or STG in progress)

(Note 5) Slot failure

x'80' : Sector write error
x'40' : Sector read error
x'20' : ECC/LRC error
x'10' : Incomplete data
x'08' : No decision

(Note 6) Obtained information flag

bit0-1 : Block type
- 00 : Data block
- 01 : HA/RO block
- 10 : Bit map block

bit2-3 : Side
- 00 : Cache write side
- 01 : NVS write side
- 10 : Cache read side

bit4 : Segment
- 0 :No segment
- 1 :Segment exist

bit5-7 : Reserved

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Byte36 = 6F (Subsystem Information) (1/1)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cace DKC)							
23	Command overrun threshold exceeded							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Unused(0)	Format (x‘1’)			
27	Data overrun threshold exceeded							
28	Seek count							
29								
2A	Drive serial number (x‘0C’) +							
2B	(x‘24’) +							
2C	(DKU sequence number)							
2D								
2E								
2F	DKC serial number (x‘0C’) +							
30	(x‘24’) +							
31	(x‘00’) +							
32	(DKC sequence number : high) +							
33	(DKC sequence number : low)							
34	SSID of self subsystem							
35								
36	Exception code Y : 0 : Statistics/RRBL command, 2 : Channel data overrun							
37	(x‘6FXY’) X : For serial CHL : LCP#, For parallel CHL : CHL#							
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Read/search byte count							
3F								
40	Not used							
7F								

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARATE	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘111’ : FPC Detected Failure)			0				
28	Not used							
29	Not used							
2A	SCSI command code (See SSBLOG05-3760)							
2B	Threshold type (See SSBLOG05-3760)							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C24’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘DYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 0 (FPC Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x'00')							
41	Not used							
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	(x'AB')							
4D	(x'CD')							
4E	CMD BLK number							
4F	Data transfer end flag							
50	I/O status							
51								
52	PDEV status							
53								
54	LOOP status							
55								
56								
57								
58	Frame Manager status							
59								
5A								
5B								
5C	TL status							
5D								
5E								
5F								
60	IO issued status 1							
61								
62	IO issued status 2							
63								
64	Not used							
65								
66								
67								
68	JOB require info							
69								
6A								
6B								
6C	Data transfer status							
6D								
6E								
6F								
70	Not used							
71								
72								
73								
74								
75								
76								
77								
78								
79								
7A								
7B								
7C								
7D								
7E								
7F								

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
|								
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARATE	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘111’ : FPC Detected Failure)			0				
28	Internal Failure Part							
29								
2A	Not used							
2B	Threshold type							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C24’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘DYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘00’)							
39	Program action code (x‘00’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 7 & Byte40 : Bit7 = 1 (FPC Detected Failure : FBP) (2/2)

	0	1	2	3	4	5	6	7
40	SSB edit format form (x'01')							
41	Not used							
42								
43								
44	ERQ index							
45								
46								
47								
48	IMQ index							
49								
4A								
4B								
4C	IO request information							
4D								
4E								
4F								
50	FPC Config/Control register							
51								
52								
53								
54	FPC Status register							
55								
56								
57								
58	FM Configuration register							
59								
5A								
5B								
5C	FM Status register							
5D								
5E								
5F								
60	FM Link Status 1 register							
61								
62								
63								
64	FM Link Status 2 register							
65								
66								
67								
68	FCA register 1							
69								
6A								
6B								
6C	FCA register 2							
6D								
6E								
6F								
70	FPC PCI register							
71								
72	AL_PA							
73								
74	FPC Config Command							
75								
76								
77								
78	Fibre status							
79								
7A								
7B								
7C	Fibre error count							
7D								
7E								
7F								

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SCSI command code

Code	Command name
00	TEST UNIT READY
03	REQUEST SENSE
04	FORMAT UNIT
07	REASSIGN BLOCKS
12	INQUIRY
15	MODE SELECT
1A	MODE SENSE
1B	START/STOP UNIT
1C	RECEIVE DIAGNOSTIC RESULT
1D	SEND DIAGNOSTIC
28	READ (EXTEND)
2A	WRITE (EXTEND)
2E	WRITE AND VERIFY
3B	WRITE BUFFER

Threshold type

Code	Threshold (failure) type
40	Fibre port failure
41	Drive mechanism recovered error
42	Drive mechanism unrecovered error
43	Drive media recovered error
44	Drive media unrecovered error
45	Drive R/W recovered error
46	Drive R/W unrecovered error
47	Drive interface recovered error
48	Drive interface unrecovered error
49	Controller recovered error
4A	Controller unrecovered error
4B	Fibre interface recovered error
4C	Fibre interface unrecovered error
4D	Drive I/O read error
4E	Drive I/O write error
FF	Invalid threshold type

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 0 (Drive Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return COde : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARATE	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘000’ : Driver Detected Failure)			0	Sense key			
28	Additional Sense Code							
29	Additional Sense Code Qualifier							
2A	SCSI command code							
2B	Threshold type							
2C	Module ID							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C24’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘EYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘92’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36 : Bit0-3 = D & Byte26 : Bit4-7 = 1 & Byte27 : Bit0-2 = 0 (Drive Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41								
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	Not used							
4D								
4E								
4F								
50								
51								
52								
53								
54	SCSI extend sense data							
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74	Error LBA number							
75								
76								
77								
78	Logical LBA number							
79								
7A								
7B								
7C	Physical LBA number							
7D								
7E								
7F								

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Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format ID							
07	PCB type		MP number					
08	System error code							
09	(Return Code : Low 2 Byte)							
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPT	ECKD32	SRAID	RCOPY	SEPARATE	HSTREP	HST REP	EXPLS
0E	LDEV#VL	PDEV#VL	SSB#VL	LOG#VL	SIM#VL	RSSB#VL	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	0	Format (x‘1’)			
27	Type code (‘000’ : Driver Detected Failure)			0	Sense key			
28	Additional Sense Code							
29	Additional Sense Code Qualifier							
2A	SCSI command code							
2B	Threshold type							
2C	Module ID (≠ 5X/6X)							
2D	Routine ID							
2E	Not used							
2F	Drive serial number (x‘0C24’) + (DKU sequence number)							
30	This information is not fixed until DKC reports SSB to HOST.							
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘EYZZ’) Y : CDEV number ZZ : RDEV number							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘92’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP) (2/2)

	0	1	2	3	4	5	6	7
40	Not used							
41								
42	CDB							
43								
44								
45								
46								
47								
48								
49								
4A								
4B								
4C	Not used							
4D								
4E								
4F								
50								
51								
52								
53								
54	SCSI extend sense data							
55								
56								
57								
58								
59								
5A								
5B								
5C								
5D								
5E								
5F								
60								
61								
62								
63								
64								
65								
66								
67								
68								
69								
6A								
6B								
6C								
6D								
6E								
6F								
70								
71								
72								
73								
74	Error LBA number							
75								
76								
77								
78	Logical LBA number							
79								
7A								
7B								
7C	Physical LBA number							
7D								
7E								
7F								

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Byte36 : Bit0-3 = E & Byte2C : Bit0-7 ≠ 5X/6X (Drive Detected Failure : DSP)

(Note 2) Threshold type

Code	Meaning
00	CHA CHK1A failure
01	CHA CHK1B failure
02	CHA CHK3 failure
03	CHA CHK2 failure
04	CHA ADP temporary failure
05	LCM hardware error
06	BSA F bus open
07	BSA LIVEINS
08	BSA check error
09	SMP M bus open
0A	SMP M bus check error
0B	SMP H/L check error
10	DKA CHK1A failure
11	DKA CHK1B failure
12	DKA CHK3 failure
13	DKA SCA temporary failure
14	DKA DRR temporary failure
16	BSA F bus open
17	BSA LIVEINS
18	BSA check error
19	SMP M bus open
1A	SMP M bus check error
1B	SMP H/L check error
20	Shared memory correctable error
21	Shared memory uncorrectable error
22	SMC M bus open
23	SMC H/L bus open
30	Cache one bit correctable error
31	Cache uncorrectable error
32	Cache two bits correctable error
33	CPC check error
40	SCSI port failure
41	Drive recovered error (mechanism)
42	Drive unrecovered error (mechanism)
43	Drive recovered error (media)
44	Drive unrecovered error (media)
45	Drive recovered error (read/write)
46	Drive unrecovered error (read/write)
47	Drive interface recovered error
48	Drive interface unrecovered error
49	Controller recovered error
4A	Controller unrecovered error
4B	SCSI interface recovered error
4C	SCSI interface unrecovered error
4D	Drive I/O read error
4E	Drive I/O write error
60	SVP interface error
FF	Invalid threshold type

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Byte36 = E0 & Byte2C = 5X/6X & Byte20 : Bit3 = 1 (LDEV blockade/Pin VOL detected/Write inhibited) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used		Format (x‘1’)		
27	Type code (b‘000’)			Not used		Not used		
28	Ready	Enable	SSB pending		Not used			
29	Not used							
2A	M.M. RSV	PIN VOL	Write INH		Not used			
2B	Not used							
2C	Module ID (Note 1)							
2D	Routine ID (Note 1)							
2E	Not used							
2F	Drive serial number (x‘0C’) + (x‘24’) + (DKU sequence number)							
30								
31								
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘E000’)							
37								
38	Log and message control (x‘08’)							
39	Program action code (x‘92’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36 = E0 & Byte 2C = 5X/6X & Byte20 : Bit3 = 1 (LDEV blockade/Pin VOL detected/Write inhibited) (2/2)

(Note 1) Module ID·Routine ID

x‘5011/501C/5202’	; LDEV blockade
x‘501A/501B’	; Pin VOL detected
x‘6605/6697/6705/6784/6805/6853/6909/6953’	; Write inhibited

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Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : Bit1 = 1 (Intervention requested : LDEV not ready) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0		RCU#		
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB							
21								
22	Storage control type (x‘06’ : Cache DKC)							
23	Count							
24	Device address							
25	Device type							
26	Unit flag	DEV ADR V	TRK ADR V	Not used		Format (x‘2’)		
27	Type code (b‘000’)			Not used		Not used		
28	Ready	Enable	SSB PEND	0	0	0	0	0
29		x‘00’						
2A	M.M RSV	PIN VOL	0	0	0	0	0	0
2B	Host type	DKC type	0	0		DKU type		
2C	Module ID¥Routine ID							
2D	(x‘501C/5202’ : LDEV not ready)							
2E	Command code							
2F	Drive serial number (x‘0C’) +							
30	(x‘24’) +							
31	(DKU sequence number)							
32								
33								
34	SSID of self subsystem							
35								
36	Exception code (x‘E210’)							
37								
38	Log and message control (x‘01’)							
39	Program action code (x‘02’)							
3A	Configuration information							
3B								
3C	Message code							
3D	Cylinder address							
3E								
3F	Head address							

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Byte36-37 = E210 & Byte 2C = 5X/6X & Byte20 : Bit1 = 1 (Intervention requested : LDEV not ready) (2/2)

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Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SIM sense record ID (x‘E0’)							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure SPs (Note 5)	SPs in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	‘0000000’						
2B	Hardware level (Note 11)							
2C								
2D	Isolation code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number(x‘0C’) + (x‘24’) + (x‘00’) + (DKC sequence number : high) + (DKC sequence number : low)*							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

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Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See “Reference code “ table)								
37									
38	Log and message control (Note 15’)*								
39	Program action code (x‘10’)*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x‘F1’)								
3D	Affected SSID*								
3E									
3F	Not used								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) Range subject to the error

x‘0’ : Not used
x‘1’ : Error range not known
x‘2’ : SP error
x‘3’ : CHL-I error
x‘4’ : Not affect performance
x‘5~F’ : Not used

(Note 3) Range affected by repair

x‘0’ : Not used
x‘1’ : Repair range not known
x‘2’ : Repair dose not affect performance
x‘3’ : SP disabled during repair
x‘4’ : SSID disabled during repair
x‘5~F’ : Not used

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Failure SPs

0 : 1SP
1 : 2SP

(Note 6) SPs in SSID

0 : 2SP
1 : 4SP

(Note 7) Failure SSIDs

0 : 1SSID
1 : 2SSID

(Note 8) Affected SSIDs

0 : 1SSID
1 : 2SSID

(Note 9) Status

0 : Reduction
1 : Stop

(Note 10) Resent SIM

0 :Unresent SIM
1 : Resent SIM

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Byte26 : Bit4-7 = F & Byte3C = F1 (DKC SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
- 00 : 4
- 01 : 8
- 10 : Not used
- 10 : Not used
- 11 : Not used

Bit 6 :NVS
- 0 : Without NVS
- 1 : With NVS

Bit 8-10 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MP
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
- 0000 : Parallel=4, serial=0
- 0001 : Parallel=8, serial=0
- 0010 : Parallel=4, serial=2
- 0100 : Parallel=4, serial=4
- 0110 : Parallel=0, serial=2
- 1000 : Parallel=0, serial=4
- 1010 : Parallel=0, serial=8
- 1100 : Parallel=0, serial=6

Bit 8 : Dual frame
- 0 : Dual frame
- 1 : Single frame

Bit 9-11 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MB
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

(Note 12) Isolation code

Byte 2D ≠ x’ 00’ : Byte 36 and 37 are a symptom code.
Byte 2D = x’ 00’ : Byte 36 and 37 are a symptom code.
This byte is byte 2 of the isolation code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don’t log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

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Byte26 : Bit4-7 = F & Byte3C = F2 (CACHE SIM) (1/3)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SIM sense record ID (x‘E0’)							
28	Range subject to the error (Note 2)				Range affected by repair (Note 3)			
29	Failure level (Note 4)		Failure Sps (Note 5)	Sps in SSID (Note 6)	Failure SSIDs (Note 7)	Affected SSIDs (Note 8)	Status (Note 9)	0
2A	Resent SIM (Note 10)	‘0000000’						
2B	Hardware level (Note 11)							
2C								
2D	Isolation code (Note 12)							
2E	SSB ID (Note 13)	SIM sequence number						SVP ID (Note 14)
2F	DKC serial number(x‘0C’) + (x‘24’) + (x‘00’) + (DKC sequence number : high) + (DKC sequence number : low)*							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

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Byte26 : Bit4-7 = F & Byte3C = F2 (CACHE SIM) (2/3)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See “Reference code” table)								
37									
38	Log and message control (Note 15’)*								
39	Program action code (x‘10’)*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x‘F1’)								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) Range subject to the error

x‘0’ : Not used
x‘1’ : Error range not known
x‘2’ : SP error
x‘3’ : CHL-I error
x‘4’ : Not affect performance
x‘5~F’ : Not used

(Note 3) Range affected by repair

x‘0’ : Not used
x‘1’ : Repair range not known
x‘2’ : Repair dose not affect performance
x‘3’ : SP disabled during repair
x‘4’ : SSID disabled during repair
x‘5~F’ : Not used

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Failure SPs

0 : 1SP
1 : 2SP

(Note 6) SPs in SSID

0 : 2SP
1 : 4SP

(Note 7) Failure SSIDs

0 : 1SSID
1 : 2SSID

(Note 8) Affected SSIDs

0 : 1SSID
1 : 2SSID

(Note 9) Status

0 : Reduction
1 : Stop

(Note 10) Resent SIM

0 :Unresent SIM
1 : Resent SIM

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Byte26 : bit4-7 = F & Byte3C = F2 (CACHE SIM) (3/3)

(Note 11) Hardware level

① When bit 0 is 0.

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs PER CLUSTER
- 00 : 4
- 01 : 8
- 10 : Not used
- 10 : Not used
- 11 : Not used

Bit 6 :NVS
- 0 : Without NVS
- 1 : With NVS

Bit 8-10 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MP
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 11-13 : Cluster hardware level (‘000’)
Bit 14-15 : Cache/NVS hardware level (‘000’)

② When bit 0 is 1,

Bit 1 : Not used
Bit 2-3 : SP number
Bit 4-5 : CHLs per cluster
- 0000 : Parallel = 4, serial = 0
- 0001 : Parallel = 8, serial = 0
- 0010 : Parallel = 4, serial = 2
- 0100 : Parallel = 4, serial = 4
- 0110 : Parallel = 0, serial = 2
- 1000 : Parallel = 0, serial = 4
- 1010 : Parallel = 0, serial = 8
- 1100 : Parallel = 0, serial = 6

Bit 8 : Dual frame
- 0 : Dual frame
- 1 : Single frame

Bit 9-11 : Cache size
- 000 : Non cache
- 001 : 256MB
- 010 : 512MB
- 011 : 768MB
- 100 : 1024MB
- 101 : 1280MB
- 110 : 1536MB
- 111 : Over 1536MB

Bit 12-13 : Cluster hardware level (‘00’)
Bit 14-15 : Cache/NVS hardware level (‘00’)

(Note 12) Isolation code

Byte 2D ≠ x‘00’ : Byte 36 and 37 are a symptom code.
Byte 2D = x‘00’ : Byte 36 and 37 are a symptom code.
This byte is byte 2 of the isolation code.

(Note 13) SSB ID

0 : SVP
1 : SP

(Note 14) SVP ID

0 : SVP1
1 : SVP2

(Note 15) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
- 00 :Don’t log
- 01 : Unconditional log
- 10 : Log only once
- 11 : Log only if persistent

bit 6-7 : Operator message
- 00 : No message
- 01 : Unconditional message
- 10 : Send only once
- 11 : Send only if persistent

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Byte26 : Bit4-7 = F & Byte3C = FE (Device SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x‘1’)				Service message (x‘1’ : Action, x‘C’ : No action)			
29	Failure level (Note 4)		‘000000’					
2A	Resent SIM (Note 5)	‘0000000’						
2B	Exception class FRU list code (x‘80’)							
2C	Hardware and microcode corequisite indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (x‘05’)							
2F	Drive serial number* (x‘0C’) + (x‘24’) + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

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Byte26 : Bit4-7 = F & Byte3C = FE (Device SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See “Reference code” table)								
37									
38	Log and message control (Note 6’)*								
39	Program action code (x‘10’)*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x‘FE’)								
3D	Affected SSID*								
3E									
3F	Not used*								
40	Not used								
7F									

* : This information is not fixed until DKC reported SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2)SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don’t log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

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Byte26 : Bit4-7 = F & Byte3C = FF (Media SIM) (1/2)

	0	1	2	3	4	5	6	7
00	Time stamp							
05								
06	Format Message							
07	PCB type		Processor ID (Note)					
08	System error code							
09								
0A	JCB ID							
0B								
0C	REQ ID							
0D	24CMPAT	ECKD32	SCSI-RAID	RCOPY	SEPARATE	Host report	SVP report	Force log
0E	LDEV#VLD	PDEV#VLD	SSB#VLD	LOG#VLD	SIM#VLD	RSSB#VLD	0	0
0F	SEMI-SYNC	RCU SIM	0	0	RCU#			
10	LDEV number							
11								
12	CDEV#							
13	RDEV#							
14	RCU LDEV number							
15								
16	SSB log number							
17								
18	Related failure log number							
19								
1A	Related SIM log number							
1B								
1C	Related SSB log number							
1D								
1E	(Reserved)							
1F	SCB							
20	Basic SSB*							
21								
22	Storage control type (x‘06’ : Cache DKC)*							
23	Count (x‘00’)*							
24	Device address*							
25	Device type*							
26	Content (Note 1)				Format (x‘F’)			
27	SSB ID (Note 2)	SIM sequence number						SVP ID (Note 3)
28	Device exception (x‘1’)				Service message (x‘1’)			
29	Failure level (Note 4)	Media maintenance procedure number (Correctable : x‘07’, Uncorrectable : x‘05’)						
2A	Resend SIM (Note 5)	‘0000000’						
2B	Exception class FRU list code (x‘80’)							
2C	Hardware and microcode corequisite indicator (x‘01’)							
2D	Device address (See reference code)							
2E	Action flag (Correctable : x‘87’ , Uncorrectable : x‘85’)							
2F	Drive serial number* (x‘0C’) + (x‘24’) + (DKU sequence number)							
30								
31								
32								
33								

* : This information is not fixed until DKC reports SIM to HOST.

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Byte26 : Bit4-7 = F & Byte3C = FF (Media SIM) (2/2)

	0	1	2	3	4	5	6	7	
34	SSID of self subsystem								
35									
36	Exception code (See “Reference code” table)								
37									
38	Log and message control (Note 6’)*								
39	Program action code (x‘10’)*								
3A	Dual frame	EDCC mode	0	0	NONSYNC operation	Serial channel	Report output	Permanent path ERR	*
3B	32Byte SSB (0)	0	0	0	0	Extended path	Storage path number		*
3C	SIM message code (x‘FF’)								
3D	Cylinder address*								
3E									
3F	Head address*								
40	Not used								
7F									

* : This information is not fixed until DKC reports SIM to HOST.

(Note 1) Content

bit0 : Serial number valid (0:Invalid,1:Valid)
bit1 : Device address valid (0:Invalid,1:Valid)
bit2 : Track address valid (0:Invalid,1:Valid)
bit3 : Not used (0)

(Note 2) SSB ID

0 : SVP
1 : SP

(Note 3) SVP ID

0 : SVP1
1 : SVP2

(Note 4) Failure level

00 : Service Alert
01 : Moderate Alert
10 : serious Alert
11 : Acute Alert

(Note 5) Resent SIM

0 : Unresent SIM
1 : Resent SIM

(Note 6) Log and message control

bit 0-2 : Not used
bit 3 : Log mode (0)
bit 4-5 : Logging action
00 :Don’t log
01 : Unconditional log
10 : Log only once
11 : Log only if persistent
bit 6-7 : Operator message
00 : No message
01 : Unconditional message
10 : Send only once
11 : Send only if persistent

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SIM Reference Codes Detected by the Processor (1/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
LCP/FCP error	LCM Hardware error	21	3Z	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#1 (*3) Z: LCP#2 (*3)
	ADP permanent error	21	70	X0	F1	Moderate	Yes	X: CHA PCB# (*1)
	ADP temporary error	21	71	XY	F1	Service	No	X: CHA PCB# (*1) Y: LCP#0 (*3)
	ADP blocking	21	72	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#0 (*3)
	AL_PA value conflict	21	90	XY	F1	Service	No	X: CHA PCB# (*1) Y: PORT# in PCB
CHA Processor error	CHK1A threshold over	30	70	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	CHK1B threshold over	30	71	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	CHK3 threshold over	30	72	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	Processor blocking	30	73	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	FM threshold over	30	74	XY	F1	Service	No	X: CHA PCB# (*1) Y: MP# in PCB
	FM error	30	75	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	Incorrect SUM value of FM	30	76	XY	F1	(*27)	No	X: CHA PCB# (*1) Y: MP# in PCB
	LDEV blockade (Effect of processor blockade)	30	90	XY	F1	Serious	Yes	X: CHA PCB# (*1) Y: MP# in PCB
	P/S OFF impossible	38	8F	00	F1	Moderate	No	
	P/S OFF impossible (Device reserved)	38	9F	00	F1	Moderate	No	
	Undefined Package is mounted	39	90	XY	F1	Moderate	No	X: CHA PCB# (*1,5) Y: MP# in PCB
	V-R or serial number is inconsistent	39	91	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Replace failed	39	93	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Micro-program version up	39	94	X0	F1	Service	No	X: MP version after replacing (*23)
	Micro-program version up impossible	39	95	XY	F1	Service	No	X: Present MP version (*23) Y: reason code (*13)

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SIM Reference Codes Detected by the Processor (2/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
CHA Processor error	Warning of SM DISABLE (MPA detected)	39	9A	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: 0 = Side A, 1 = Side B (*2)
	SMA slave error	39	9B	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	MPA slave error	39	9C	XY	F1	Moderate	No	X: CHA PCB# (*1) Y: MP# in PCB
	Injustice DC voltage control	39	9D	X0	F1	Moderate	No	X: CHA PCB# (*1)
	Injustice CE MODE	39	9E	X0	F1	Moderate	No	X: CHA PCB# (*1)
	CHT PCB exchange impossible (4GL ↔ 4GS)	39	9F	X0	F1	Moderate	No	X: CHA PCB# (*1)

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SIM Reference Codes Detected by the Processor (3/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
DKA Processor error	CHK1A threshold over	31	70	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	CHK1B threshold over	31	71	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	CHK3 threshold over	31	72	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	Processor blocking	31	73	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	FM threshold over	31	74	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	FM error	31	75	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	Incorrect SUM value of FM	31	76	XY	F1	(*27)	No	X: DKA PCB# (*1) Y: MP# in PCB
	LDEV blockade (Effect of processor blockade)	31	90	XY	F1	Serious	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	P/S OFF impossible	3C	8F	00	F1	Moderate	No	
	P/S OFF impossible (Device reserved)	3C	9F	00	F1	Moderate	No	
	Undefined Package is mounted	3D	90	XY	F1	Moderate	No	X: DKA PCB# (*1,5) Y: MP# in PCB
	V-R or serial number is inconsistent	3D	91	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Replace failed	3D	93	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Micro-program version up	3D	94	X0	F1	Service	No	X: MP version after replacing (*23)
	Micro-program version up impossible	3D	95	XY	F1	Service	No	X: Present MP version (*23) Y: reason code (*13)
	Warning of SM DISABLE (MPA detected)	3D	9A	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: 0 = Side A, 1 = Side B (*2)
	SMA slave error	3D	9B	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	MPA slave error	3D	9C	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB
	Injustice DC voltage control	3D	9D	X0	F1	Moderate	No	X: DKA PCB# (*1)
	Injustice CE MODE	3D	9E	X0	F1	Moderate	No	X: DKA PCB# (*1)
	FSW LED BUS test	3D	AZ	XY	FE	Moderate	No	X: DKA PCB# (*1) Y: MP# in PCB Z: FSW PCB#
	Tachyon error	3D	B0	XY	FE	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
SHSN error	Logical path blockade (CHA Processor)	32	8Z	XY	F1	Moderate	No	X: CHA PCB# (*1,31) Y: MP# in PCB Z: PATH# 0: A0 PATH 1: A1 PATH 2: B0 PATH 3: B1 PATH

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SIM Reference Codes Detected by the Processor (4/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
SHSN error	Logical path blockade (DKA Processor)	33	8Z	XY	F1	Moderate	No	X: DKA PCB# (*1,31) Y: MP# in PCB Z: PATH# 0: A0 PATH 1: A1 PATH 2: B0 PATH 3: B1 PATH
CHSN error	Logical path blockade (CHA Processor/CARB0)	32	0Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA Processor/CARB1)	32	1Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA/PMA/CARB0)	32	4Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (CHA/PMA/CARB1)	32	5Z	XY	F1	Moderate	No	X: CHA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/DRR/CARB0)	33	0Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/DRR/CARB1)	33	1Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/FCA/CARB0)	33	2Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
	Logical path blockade (DKA/FCA/CARB1)	33	3Z	XY	F1	Moderate	No	X: DKA PCB# (*1,29) Y: MP# in PCB Z: C path bitmap
CHA, CHK2 (processor)	RCHA temporary error	3F	84	X0	F1	Service	No	X: CHA PCB# (*1)
	RCHA blocking	3F	85	X0	F1	Serious	Yes	X: CHA PCB# (*1)
DKA CHK2 (processor)	Pinned slot	CF	4X	YY	F1	Moderate	No	X: CU# (*34) YY: LDEV#
	DRR temporary error	CF	80	XY	F1	Service	No	X: DKA PCB# (*1) Y: MP# in PCB
	FCA temporary error	CF	81	XY	F1	Service	No	X: DKA PCB# (*1) Y: Port# (*4)
	DRR blocking	CF	82	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: MP# in PCB
	FCA blocking (0-3)	CF	83	XY	F1	Moderate	Yes	X: DKA PCB# (*1) Y: Port# (*4)
	Fibre port blocking (Effect of PATH INLINE failed)	CF	84	XY	F1	Moderate	No	X: DKA PCB# (*1) Y: Port# (*4)
	LDEV blockade (Effect of FCA blockade)	CF	90	XY	F1	Serious	Yes	X: DKA PCB# (*1) Y: Port# (*4)

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SIM Reference Codes Detected by the Processor (5/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
Cache data error	Pinned slot	FF	4X	YY	F2	Moderate	No	X: CU# (*34) YY: LDEV#
Cache error	Area is volatized	FF	CD	0X	F2	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Package is volatized	FF	CE	0X	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Module group is volatized	FF	CF	YX	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Correctable error	FF	F0	YX	F2	Service	No	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Cache temporary error	FF	F1	YX	F2	Service	Yes	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Module group blocking	FF	F2	YX	F2	Moderate	Yes	X: PCB# (*1) Side A:Even, Side B:Odd Y: Module group# (*10)
	Package blocking	FF	F3	0X	F2	Moderate	Yes	X: PCB# (*1) Side A:Even, Side B:Odd
	Area blocking	FF	F4	0X	F2	Serious	Yes	X: 0 = Side A, 1 = Side B (*2)
	Both area failed	FF	F5	0X	F2	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Injustice DC voltage control	FF	F6	0X	F2	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Injustice CE MODE	FF	F7	0X	F21	Moderate	No	X: PCB# (*1) Side A:Even, Side B:Odd
	Module group error in On-demand area	FF	FD	YX	F2	Moderate	No	X: PCB# (*1) Y: Module group#
Shared memory error	Loss of duplicated information	FF	DE	XX	F1	Service	No	XX: Lost information type (*25)
	One side Area is volatized	FF	DF	0X	F1	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Correctable error	FF	E0	YX	F1	Service	No	X: 0 = Side A, 1 = Side B Y: Module# (*2,10)
	Area blocking	FF	E2	0X	F1	Serious	Yes	X: 0 = Side A, 1 = Side B (*2,10)
	Real memory size inconsistent	FF	E3	XY	F1	Serious	No	X:Number of module (side A) Y:Number of module (side B) (*8)
	Replace failed (*20)	FF	E4	0X	F1	Serious	No	X: 0 = Side A, 1 = Side B (*2)
	Both side invalid	FF	E5	00	F1	Acute	No	
	Configuration information compare error (*22)	FF	E6	00	F1	Acute	No	
	Shared memory is volatized.	FF	E7	00	F1	Serious	No	
	Configuration mismatch	FF	E8	00	F1	Acute	No	
	“DKCMAIN” micro lost	FF	E9	00	F1	Serious	No	(*30)
	HPAV micro lost	FF	E9	01	F1	Serious	Yes	
	CHK3 threshold over	FF	EC	0X	F1	Service	No	X: 0 = Side A, 1 = Side B (*2)
	Area temporary blocking (*19)	FF	EE	0X	F1	Service	Yes	X: 0 = Side A, 1 = Side B (*2)
	Rebooted without volatilization after an instantaneous down	FF	EF	00	F1	Service	No	
	Module error in On-demand area	FF	ED	YX	F1	Service	No	X: 0 = Side A, 1 = Side B (*2) Y: Module#

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SIM Reference Codes Detected by the Processor (6/7)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
Drive error (normal R/W)	Drive port temporary error (Drive path: Boundary 0)	DF	6X	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port temporary error (Drive path: Boundary 1)	DF	7X	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive temporary error	EF	AX	XX	FE	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive media error	43	4X	XX	FF	Service (*32)	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port blockade (Drive path: Boundary 0)	DF	8X	XX	FE	Moderate (*32)	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port blockade (Drive path: Boundary 1)	DF	9X	XX	FE	Moderate (*32)	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Drive path: Boundary 0/ Effect of SCSI blockade) *15	DF	AX	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Drive path: Boundary 1/ Effect of SCSI blockade) *15	DF	BX	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (drive)	EF	1X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (Effect of Dynamic sparing normal end)	EF	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	LDEV blockade (Effect of drive blockade) *15	EF	9X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive blockade (media)	43	CX	XX	FF	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Correction copy start *7	45	1X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy normal end *7	45	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy abnormal end *7	45	3X	XX	FE	Serious	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy discontinued *7	45	4X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Correction copy warning end* *7 (With blockade LDEV or some error)	45	5X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing start *7 (Drive copy)	46	1X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing normal end *7 (Drive copy)	46	2X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)

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SIM Reference Codes Detected by the Processor (7/7)

Error			REF CODE 22	REF CODE 23	REF CODE 13	SIM 28	Level of error	Host report	Remarks
Drive error (normal R/W)	Dynamic sparing abnormal end (Drive copy) *7		46	3X	XX	FE	Moderate	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing discontinued *7		46	4X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Dynamic sparing warning end* (With blockade LDEV or some error) (Drive copy) *7		46	5X	XX	FE	Service	Yes **	XXX: Drive number (CDEV#:4b+RDEV#:8b) (Source side drive)
	Pinned slot		EF	4X	YY	FE	Moderate	No	X: CU# (*34) YY: LDEV#
Drive error (ORM)	Drive port temporary error (Drive path: Boundary 0)		50	0X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive port temporary error (Drive path: Boundary 1)		50	1X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive temporary error		50	2X	XX	FE	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
	Drive media error		50	3X	XX	FF	Service	No	XXX: Drive number (CDEV#:4b+RDEV#:8b)
CSW error	Injustice DC voltage control		FF	20	0X	F1	Moderate	No	X: CSW PCB# (*1)
	Injustice CE MODE		FF	21	0X	F1	Moderate	No	X: CSW PCB# (*1)
SVP interface error (CHA side)	Ethernet error for SVP		14	00	X0	F1	Moderate	Yes	X: CHA PCB# (*1)
	SIM transfer failure to SVP		14	01	X0	F1	Serious	Yes	X: CHA PCB# (*1)
SVP interface error (DKA side)	Ethernet error for SVP		15	00	X0	F1	Moderate	Yes	X: DKA PCB# (*1)
	SIM transfer failure to SVP		15	01	X0	F1	Serious	Yes	X: DKA PCB# (*1)
Power error	Multi Cabinet Model	HDU power off	AC	50	XY	F1	Moderate	Yes	X: DKU number (*12) Y: HDU number (*12)
		HDU power recovered	AC	51	XY	F1	Service	No	X: DKU number (*12) Y: HDU number (*12)
	Single Cabinet Model	HDU power off	AC	50	0X	F1	Moderate	Yes	X: HDU number
		HDU power recovered	AC	51	0X	F1	Service	No	X: HDU number
	DKC was set to power error mode		AC	60	00	F1	Moderate	No	
	DKC was released from power error mode		AC	61	00	F1	Service	No	
	When DKC was set to power error mode, Urgent Destaging start succeeded.		AC	62	00	F1	Service	No	
	When DKC was set to power error mode, Urgent Destaging start failed.		AC	63	00	F1	Moderate	No	

* : Warning end : (1) LDEV blockade status is detected, and copy process for the LDEV is skipped.

(2) Some failures are detected, and copy process is complete.

** : When the drive is 3880 emulation mode, the SIM is not reported to host.

*** : The SIM is not reported to SVP.

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SIM Reference Codes Detected by the Processor for HRC/HODM (1/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
LCP/FCP error (Remote Control Port)	Logical path(s) on the remote copy connections was logically blocked (Due to an error conditions)	21	80	XY	F1	Moderate	Yes	X: CHA PCB# (*1) Y: LCP#1 (*3)
	The logical path has been recovered from blocked condition on the remote copy conditions.	21	81	XY	F1	Service	Yes (*17)	X: CHA PCB# (*1) Y: LCP#1 (*3)
Pair volume status error	HRC started the initial copy or out of sync for this volume.	D0	0X	YY	FE	Service	Yes (*17)	X: CU# YY: LDEV#
	HRC completed the initial copy for this volume.	D0	1X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HRC for this volume was deleted. (Operation from an SVP/remote console or a host processor)	D0	2X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	MCU changed volume pair status. (Operation from an SVP/remote console or a host processor)	D0	3X	YY	FE	Service	No	X: CU# (*34) YY: LDEV#
	Status of the R-VOL is changed.	D1	ZX	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV# Z: (*16)
	RCU changed status of R-VOL to suspend. (Operation from an SVP/remote console or a host processor.)	D2	0X	YY	FE	Service	No	X: CU# (*34) YY: LDEV#
	Status of the R-VOL was changed from suspend to simplex. (Operation from an SVP/remote console or a host processor.)	D2	1X	YY	FE	Service	No	X: CU# (*34) YY: LDEV#
	Status of R-VOL was changed from duplex to simplex. (Operation from an SVP/remote console or a host processor.)	D2	2X	YY	FE	Service	No	X: CU# (*34) YY: LDEV#
	Status of the R-VOL was changed from pendingduplex to simplex. (Operation from an SVP/remote console or a host processor.)	D2	3X	YY	FE	Service	No	X: CU# (*34) YY: LDEV#
	HODM started the migration copy or out of sync for this volume.	D3	0X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HODM completed the migration copy for this volume.	D3	1X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HODM for this volume was deleted. (Operation from an SVP/remote console)	D3	2X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HODM started the erase operation for the R-VOL.	D3	AX	YY	FE	Service	No (*17)	X: CU# (*34) YY: LDEV#
	HODM completed the erase operation for the R-VOL.	D3	BX	YY	FE	Service	No (*17)	X: CU# (*34) YY: LDEV#
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the remote copy connections.)	D4	0X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#

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SIM Reference Codes Detected by the Processor for HRC/HODM (2/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
Pair volume status error	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	D4	1X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	HRC/HODM for this volume was suspended (Due to an unrecoverable failure on the R-VOL)	D4	2X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	HRC for this volume was suspended (Caused by DFW to the R-VOL was prohibited)	D4	3X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	HRC for this volume was suspended (Due to an internal error condition detected by the RCU)	D4	4X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	HRC for this volume was suspended (Caused by Delete pair operation was issued to the R-VOL)	D4	5X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	Erase operation for this volume was not completed. (Due to error conditions)	D4	8X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	MCU detected a Moderate Level SIM for RCU.	D4	DX	YY	FE	Moderate	Yes (*18)	X: CU# YY: LDEV# (*34)
	MCU detected an Acute or Serious Level SIM for RCU.	D4	EX	YY	FE	Serious	Yes (*18)	X: CU# YY: LDEV# (*34)
	Status of the M-VOL was not consistent with the R-VOL.	D4	FX	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)

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SIM Reference Codes Detected by the Processor for HRC/HORC (Asynchronous) (1/2)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
Pair volume status error	HRC started the initial copy or out of sync for this volume.	D5	0X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HRC completed the initial copy for this volume.	D5	1X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HRC for this volume was accepted delete pair operation. (Operation from an SVP/remote console or a host processor)	D5	2X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	HRC for this volume was accepted suspend pair operation. (Operation from an SVP/remote console or a host processor)	D5	3X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	Delete pair operation for this HRC volume has completed.	D5	4X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	Suspend pair operation for this HRC volume has completed.	D5	5X	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV#
	The R-VOL status has changed as requested by MCU.	D6	ZX	YY	FE	Service	Yes (*17)	X: CU# (*34) YY: LDEV# Z: (*16)
	The R-VOL has accepted/completed state change as requested by operation. (Operation from an SVP/remote console or a host processor.)	D7	ZX	YY	FE	Service	No	X: CU# (*34) YY: LDEV# Z: (*26)
	The M-VOL has suspended. (Due to an unrecoverable failure on the remote copy connections.)	DB	0X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#
	The M-VOL has suspended. (Due to an unrecoverable failure on the M-VOL or the remote copy connections)	DB	1X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#
	The M-VOL has suspended. (Due to an unrecoverable failure on the R-VOL)	DB	2X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#
	The M-VOL has suspended. (Caused by DFW to the R-VOL was prohibited)	DB	3X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#
	The M-VOL has suspended. (Caused by Suspend pair operation was issued to the R-VOL)	DB	4X	YY	FE	Serious	Yes (*17)	X: CU# (*34) YY: LDEV#

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SIM Reference Codes Detected by the Processor for HRC/HORC (Asynchronous) (2/2)

Error		REF CODE 22	REF CODE 23	REF CODE 13	SIM 28	Level of error	Host report	Remarks
Pair volume status error	The M-VOL has suspended. (Caused by Delete pair operation was issued to the R-VOL)	DB	5X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	The R-VOL has suspended. (Due to an unrecoverable failure on the remote copy connections)	DB	6X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	The R-VOL has suspended. (Due to an unrecoverable failure on the R-VOL)	DB	7X	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)
	The R-VOL has suspended. (Due to an MCU power-off event)	DB	8X	YY	FE	Service	No	X: CU# YY: LDEV# (*34)
	MCU detected a Service Level SIM for RCU.	DB	CX	YY	FE	Service	Yes	X: CU# YY: LDEV# (*34)
	MCU detected a Moderate Level SIM for RCU.	DB	DX	YY	FE	Moderate	Yes	X: CU# YY: LDEV# (*34)
	MCU detected an Acute or Serious Level SIM for RCU.	DB	EX	YY	FE	Serious	Yes	X: CU# YY: LDEV# (*34)
	Status of the M-VOL was not consistent with the R-VOL.	DB	FX	YY	FE	Serious	Yes (*17)	X: CU# YY: LDEV# (*34)

Notice : SIM which REF.CODE is DB7XXX may be reported in the following case.

- When the Suspend Pair operation with the Drain option is accepted by the MCU/RCU under the host I/O.
- When the Delete Pair operation with the Group option is accepted by the RCU under the host I/O.

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SIM Reference Codes Detected by the Processor for HMRCF/HOMRCF/HIHSM/HXRC/HRCA (1/1)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
HMRCF error or HOMRCF error	Copy abnormal end	47	DY	XX	FE	Moderate	Yes	XX:T-Vol# Y: CU# (*34)
HIHSM error	HIHSM Volume Migration Abnormal End	47	FY	XX	FE	Moderate	No	XX:S-Vol# Y: CU# (*34)
HXRC/ HRCA error	Sidefile 'sleep wait' threshold over	49	0X	YY	FE	Service	Yes	X: CU# (*34) YY: LDEV#

SIM Reference Codes Detected by the Processor for DCR (1/1)

Error		REF CODE			SIM	Level of error	Host report	Remarks
		22	23	13	28			
DCR Status	PreStaging abnormal end	48	21	XX	FE	Service	No	XX: Reason code *11

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(*1)

Multi Cabinet Model

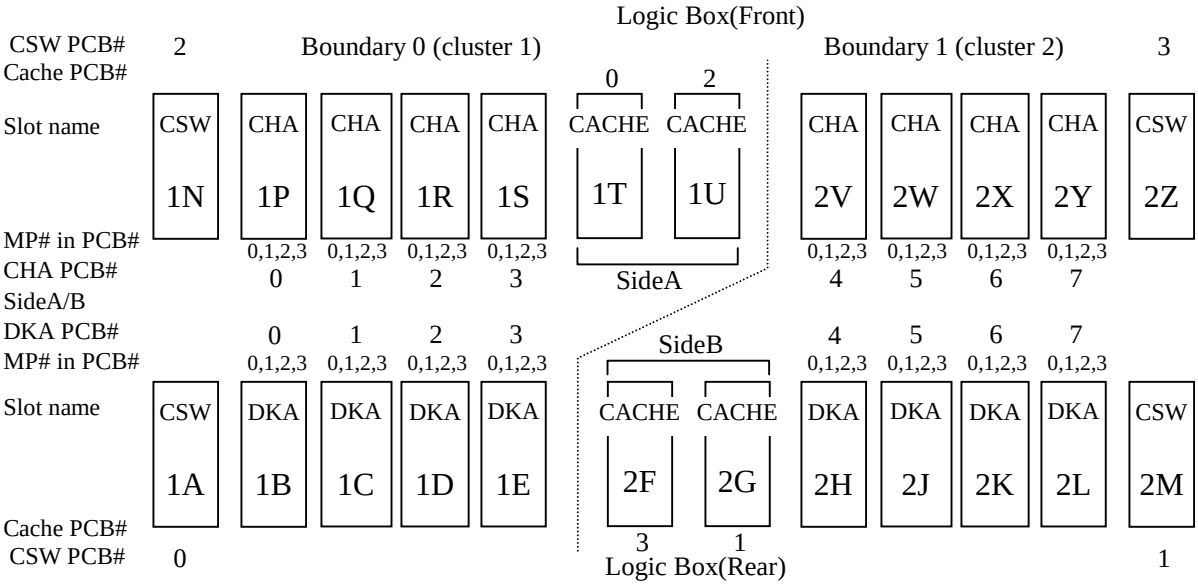
CHA PCB#: x‘0’ to x‘7’ indicates the CHA PCB number. See the figure below.
DKA PCB#: x‘0’ to x‘7’ indicates the DKA PCB number. See the figure below.
CSW PCB#: x‘0’ to x‘3’ indicates the CSW PCB number. See the figure below.
Cache PCB#: x‘0’ to x‘3’ indicates the Cache PCB number. See the figure below.

Single Cabinet Model

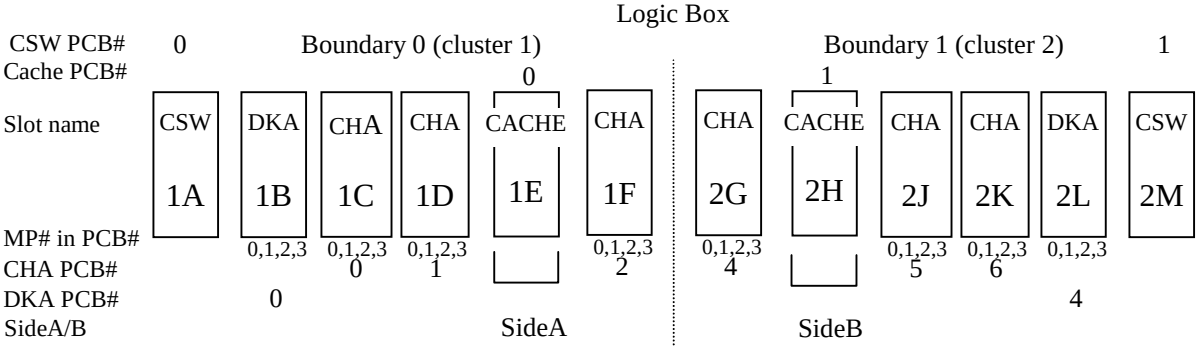
CHA PCB#: x‘0’ to x‘6’ indicates the CHA PCB number. See the figure below.
DKA PCB#: x‘0’ to x‘4’ indicates the DKA PCB number. See the figure below.
CSW PCB#: x‘0’ to x‘1’ indicates the CSW PCB number. See the figure below.
Cache PCB#: x‘0’ to x‘1’ indicates the Cache PCB number. See the figure below.

(*2) Side A/B: Indicates the side of cache/shared memory. See the figure below.

Multi Cabinet Model



Single Cabinet Model



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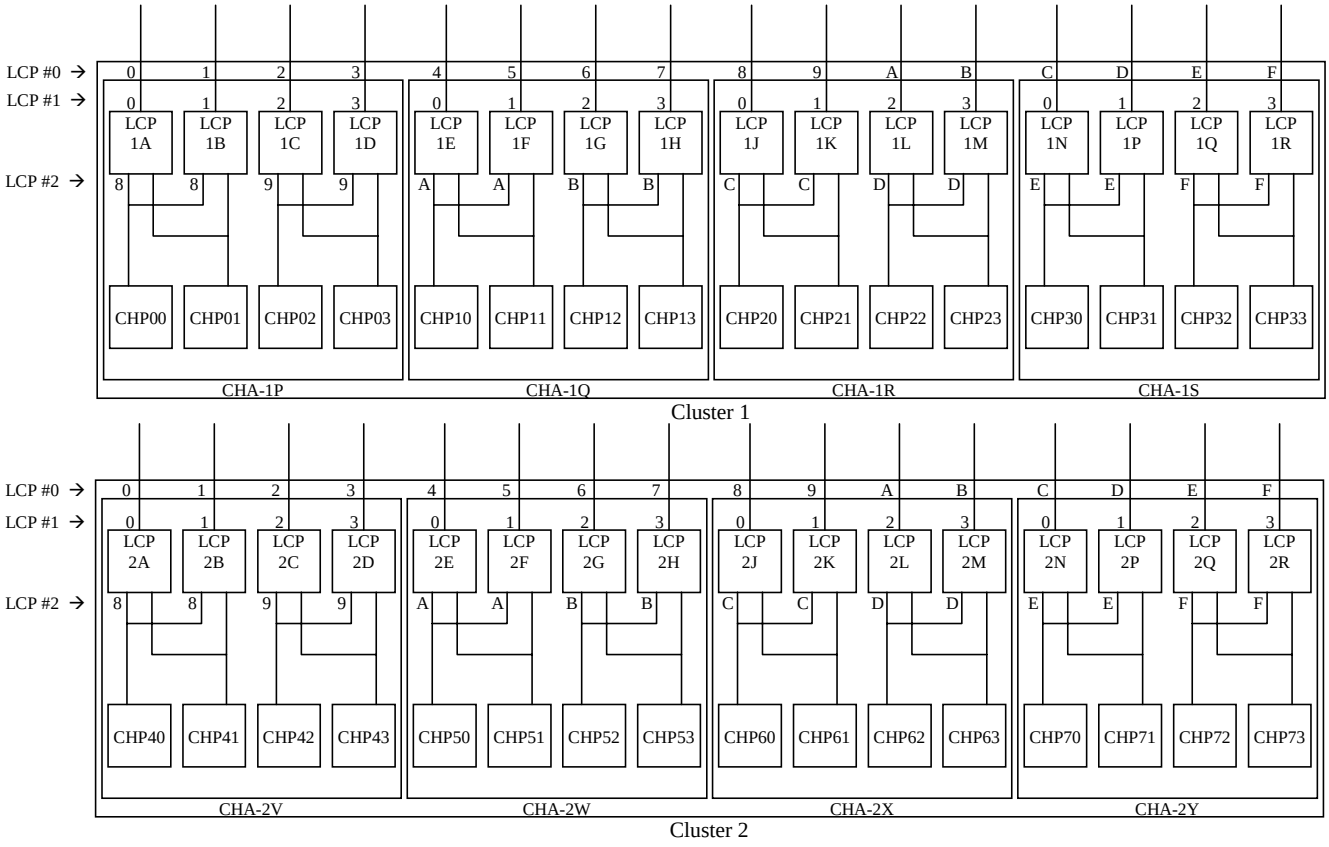
(*3)

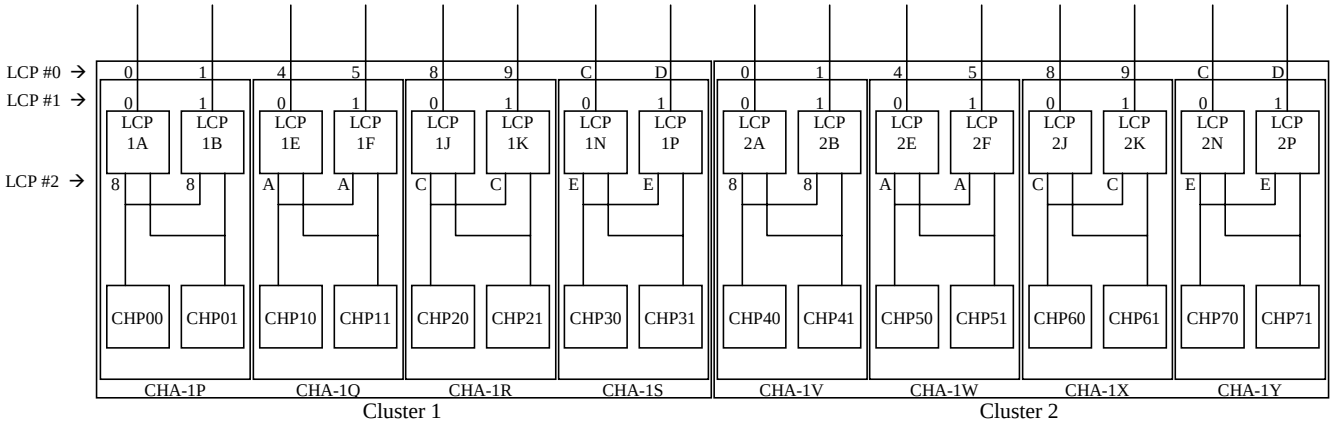
Multi Cabinet Model

LCP #0: x‘0’ to x‘F’ indicates the LCP number.
LCP #1: x‘0’ to x‘3’ indicates the LCP number.
LCP #2: x‘8’ to x‘F’ indicates the LCP number.

-DKC-F460I-8S-



-DKC-F460I-4S-



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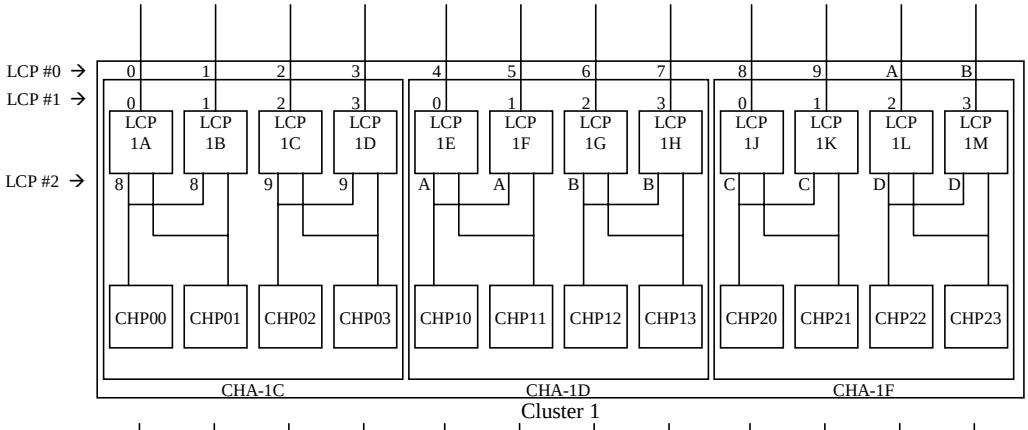
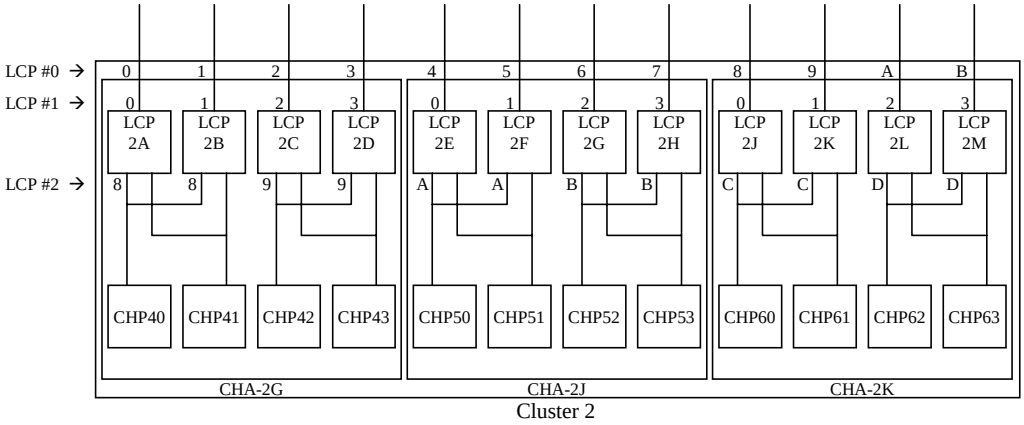
Single Cabinet Model

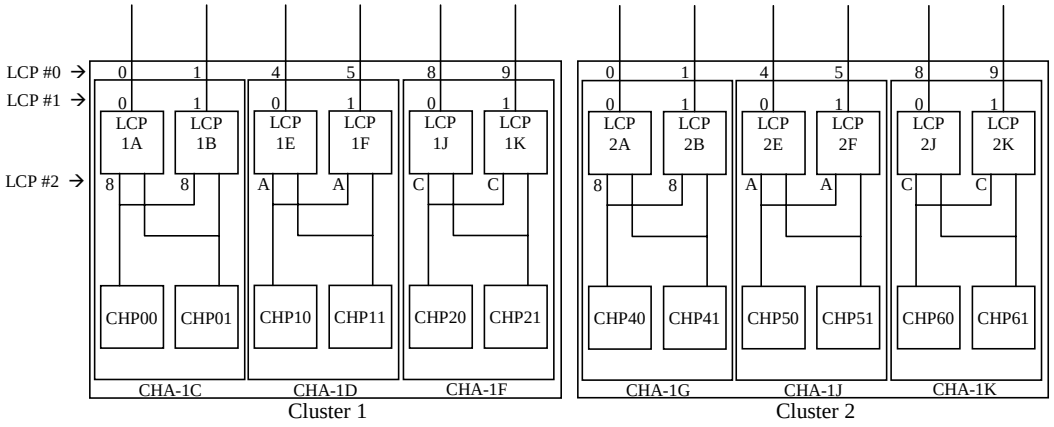
LCP #0: x‘0’ to x‘D’ indicates the LCP number.
LCP #1: x‘0’ to x‘3’ indicates the LCP number.
LCP #2: x‘8’ to x‘D’ indicates the LCP number.

-DKC-F460I-8S-





-DKC-F460I-4S-



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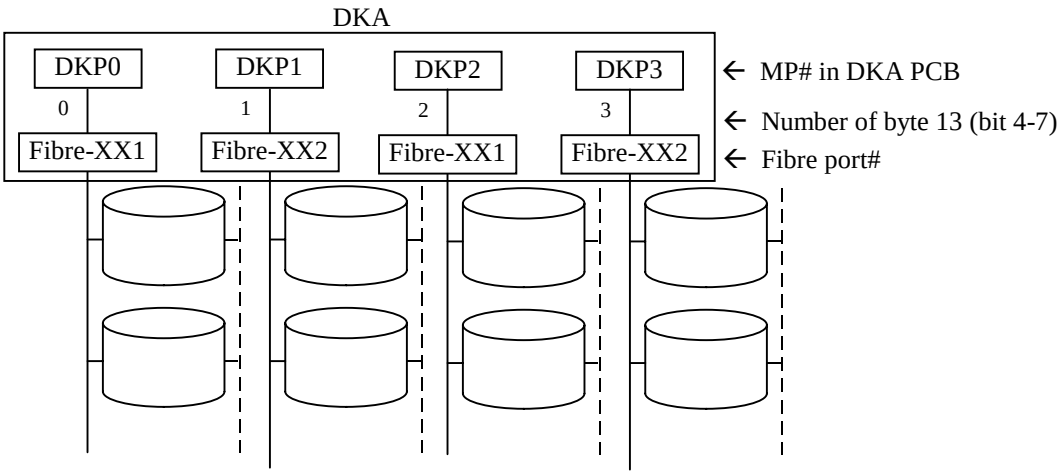
(*4) Port #: x‘0’ to x‘3’ indicates the FIBRE port number. See the figure below.



(*5) The package that is not defined in the configuration information exists.
If it is prepared for new installation, it is necessary to do the new installation procedure.
Otherwise it should be pulled out by executing P/S off.

(*7) Isolate the error according to the procedure shown in TRBL05-170.

(*8) Recover the error according to the procedure shown in TRBL05-270.

(*10) Perform error isolation according to the procedure given in the two separate pages attached to TRBL05-300.

(*11) Reason Code
x‘10’: No DCR PP
x‘20’: Subsystem busy
x‘40’: Staging time over
x‘50’: Cache blockade
x‘60’: LDEV blockade
x‘70’: Staging failure
x‘80’: P/S OFF
x‘90’: PreStaging canceled
x‘a0’: Cache over loaded

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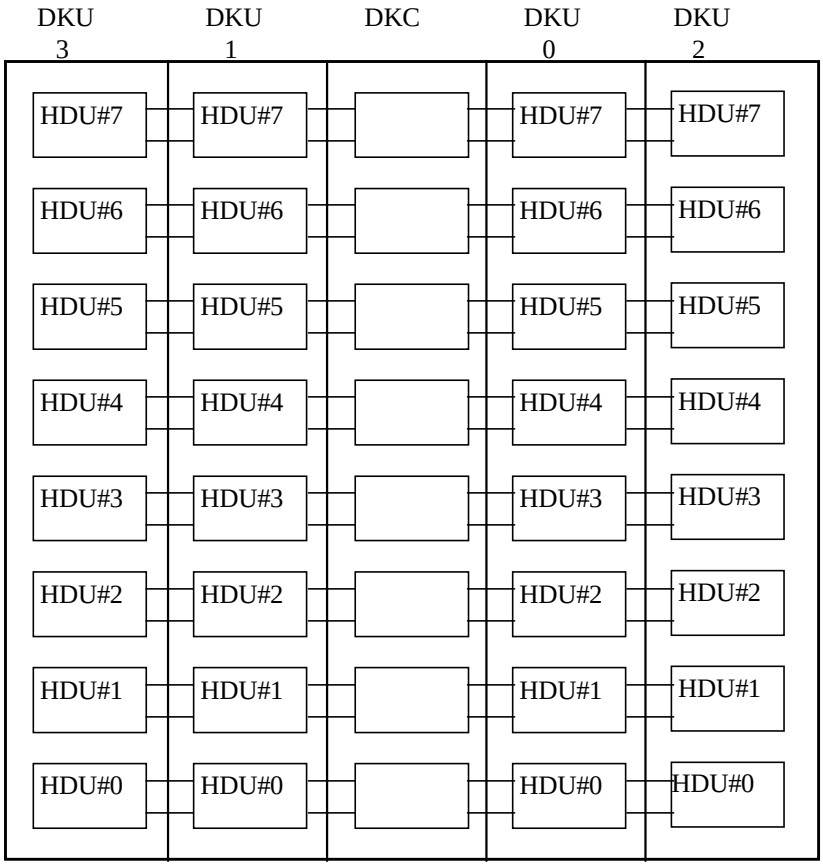
(*12) DKU#: x‘0’ to x‘3’ indicates DKU number. See the figure below.
HDU#: x‘0’ to x‘7’ indicates HDU number. See the figure below.



(*13) reason code
x‘0’ : Pinned data exist
x‘1’ : The shutdown of the power supply was occurred
x‘2’ : Invalid Version/Revision exists

(*15) Recover LDEVs according to the procedure shown in TRBL05-330.

(*16) Change pair status number
x‘0’: From simplex to duplex pending
x‘1’: From simplex to duplex
x‘2’: From pending duplex to duplex
x‘3’: From pending duplex to suspend
x‘4’: From duplex to suspend
x‘5’: From duplex to simplex
x‘6’: From pending duplex to simplex
x‘7’: From suspend to simplex
x‘8’: From suspend to duplex pending

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(*17) You can suppress reporting the HRC/HODM Service SIM to the HOST by RCU Option operation (PPRC support by HOST and Service SIM of HRC/HODM).

- Service level SIM -

PPRC support by HOST	Service SIM or HRC/HODM	level of error	HRC	HODM
Yes	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Not Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report
No	Report	DKC_SIM	Host Report	Host Report
		DEV_SIM	Host Report	Host Report
	Not Report	DKC_SIM	Not Host Report	Not Host Report
		DEV_SIM	Not Host Report	Not Host Report

- Moderate or Serious level SIM -

PPRC support by HOST	level of error	HRC	HODM
Yes	DKC_SIM	Host Report	Host Report
	DEV_SIM	Not Host Report	Host Report
No	DKC_SIM	Host Report	Host Report
	DEV_SIM	Host Report	Host Report

(*18) For SIMs of REF.CODE D4DX, D4EX are reported in case of HODM.
In case of HRC, SIMs reported from RCU are reported to the host by MCU.

Severity Level	RC of reported SIM for HRC	RC of reported SIM for HODM
Acute or Serious	No modification	D4EX
Moderate	No modification	D4DX
Service (Not HRC SIM)	No modification	Not reported
Service (HRC SIM)	Not reported	Not reported

(*19) This temporary blocking is to recover the logical table on SM and be automatically recovered.

(*20) In case of the replacement of the cache memory PCB on the side having blocked SM (see REP01-160 work ID = RCA1), insert the removed cache memory PCB again.

(*21) Isolate the error according to the procedure shown in TRBL05-200.

(*22) The LDEV is blocked because of an error (inconsistency between data on the A and B sides) of configuration information stored in the SM. Recover the error following the instruction of the Technical Support Center.

(*23) X represents the X in a program version “?X-??-??/??”.

(*24) Cache SIMM sizes of sides A and B are different because the replacement of the cache memory has been performed on one side only. Perform the replacement left referring to the description in the remark column.

(*25) Type of the lost information is reported according to the bit position. (There may be the case that two or more bits are set.)

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(*26) Change pair status number
x‘0’: Accepted Suspend Pair operation
x‘1’: Accepted Delete Pair operation (The R-VOL is in suspended status)
x‘2’: Accepted Delete Pair operation (The R-VOL is in duplex status)
x‘3’: Accepted Delete Pair operation (The R-VOL is in pending duplex status)
x‘4’: Completed Suspend Pair operation
x‘5’: Completed Delete Pair operation

(*27) In the case that the error is detected in the area of ROM, the level of error is “Moderate” in other case “Service”.

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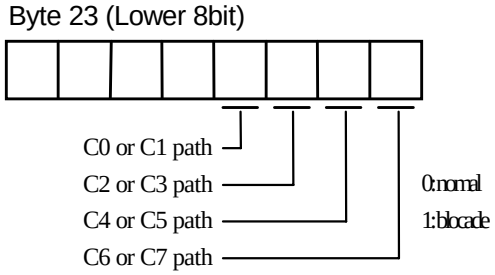
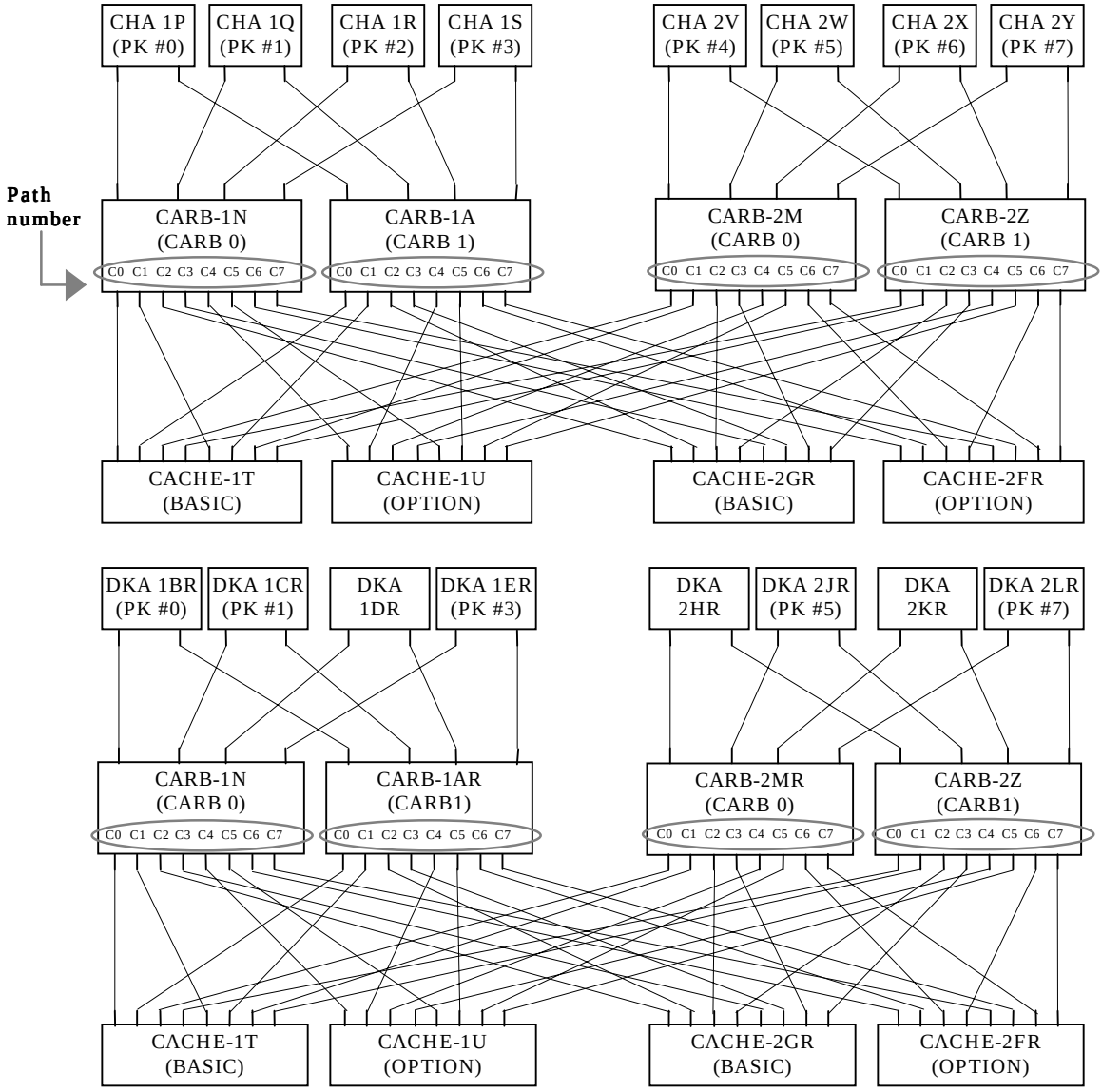
(*29) C path bitmap indicates status of C path. See the figure below.



Multi Cabinet Model

CHSN Logical path layout



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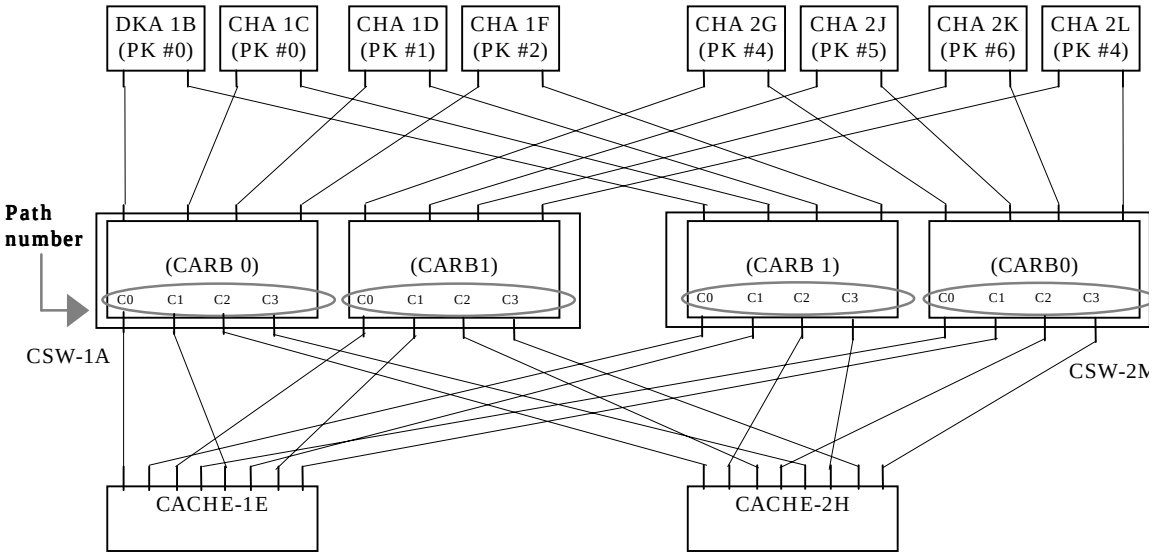
Single Cabinet Model

CHSN Logical path layout

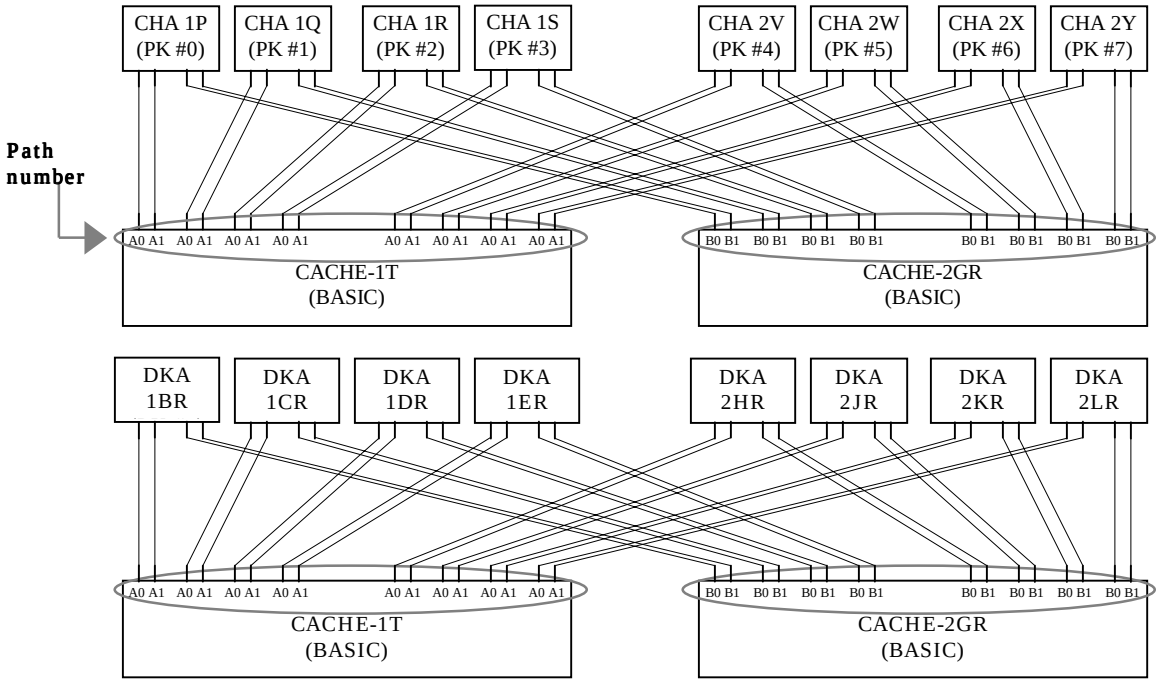


(*30) If this reference code is reported, execute the micro-program exchange procedure (On-line) of the micro type “DKCMAIN”. (MICRO-FC04-10 to 04-120)

(*31) PATH# A0, A1, B0, B1 indicates the SHSN Logical path number. See the figure below.

Multi Cabinet Model

SHSN Logical path layout



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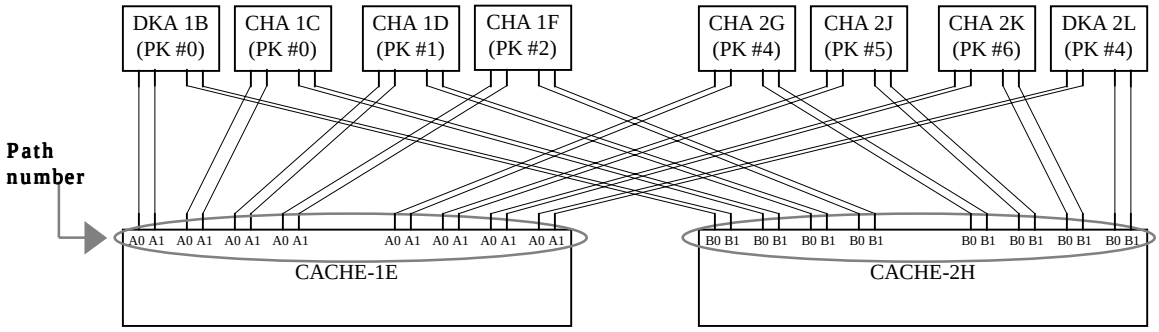
Single Cabinet Model

SHSN Logical path layout



(*32) In the case that there are no redundancy of drive the level of error is “Serious”.

(*34) CU# is detected only lower figure in SIM-RC.(CU# 0x0 ~ 0xF)
Look at the SVP information – Content SIM – Error Location

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