

# ***GLOSSARY SECTION***

**ACC (Action Code)**

Refer to the ACC section.

**ACP (Array Control Processor)****BATCTR (Battery Control PCB)****CHA (Channel Adapter)**

Provides the channel interface control functions and intercache data transfer functions. It is used to convert the data format between CKD and FBA. The CHA contains an internal processor and 128 bytes of edit buffer memory.

**CHK1A**

An internal failure has occurred in the processor.

**CHK1B**

A failure has occurred near the processor.

**CHK2**

A failure has occurred while accessing the Cache Memory.

**CHK3**

A failure has occurred while accessing Shared Memory.

**CHSN (Cache memory Hierarchical Star Network)****CM (Cache Memory Module)**

Intermediate buffer between the channels and drives. CACHE has a maximum of 128 GB (64 GB × 2 areas) of capacity. It is available and controlled as two areas of cache (cache A and cache B). It is fully battery-backed (48 hours or 24 hours).

**CM PATH (Cache Memory Access Path)**

Access Path from the processors of CHA, DKA PCB to Cache Memory.

**CSW (Cache Switch PCB)**

The cache switch (CSW) has a function to connect the channel adapter or disk adapter to the cache. Each of them is connected to the cache by the Cache Memory Hierarchical Star Net (C-HSN) method.

Each cluster is provided with the two CSWs, and each CSW can connect four caches. The CSW switches any of the cache paths to which the channel adapter or disk adapter is to be connected through an arbitration.

**CUDG (Control Unit Diagnosis)****CVS (Customizable Volume Size)****DCR (Dynamic Cache Residency)****DKA (Disk Adapter)**

Provides the control functions for data transfer between drives and cache. The DKA contains DRR (Data Recover and Reconstruct), a parity generator circuit. It supports eight FIBRE path and offers 32 KB of buffer for each FIBRE path.

**DKCMN (Disk Controller Monitor)****DKUMN (Disk Unit Monitor)****DRR (Data Recovery and Reconstruction)****DTA (Data Adapter)****EPO SW (Emergency Power Off Switch)****ESCD (ESCON Director)****FAL (File Access Library)**

**FCA (Fibre Control Adapter)**

**FCU (File Conversion Utility)**

**FLGFAN (Front Logic Box Fan Assembly)**

**FLOGIC BOX (Front Logic Box)**

**FM (Flash Memory)**

Each microprocessor has FM. FM is non-volatile memory which contains microcodes.

**FPC (Failure Parts Code)**

Refer to the ACC section.

**FSW (Fibre Channel Interface Switch PCB)**

**HIHSM (Hitachi Internal Hierarchy Storage Management)**

**HMDE (Hitachi Multiplatform Data Exchange)**

**HMRCF (Hitachi Multiple RAID Coupling Feature)**

**HMRS (Hitachi Multiplatform Resource Sharing)**

**HODM (Hitachi Online Data Migration)**

**HOMRCF (Hitachi Open Multiple RAID Coupling Feature)**

**HORC (Hitachi Open Remote Copy)**

**HRC (Hitachi Remote Copy)**

**HXRC (Hitachi Extended Remote Copy)**

**LCDG (Link Control Module Diagnosis)**

**LCP (Link Control Processor)**

Controls the optical links. LCP is located in the LCM.

**LDEV (Logical Device)**

**LU (Logical Unit)**

**LUSE (Logical Unit Size Expansion)**

**MCU (Main Disk Control Unit)**

**MFC (Main Failure Code)**

Refer to the ACC section.

**MP (Micro-Processor)**

**MPA (Micro-Processor Path Adapter)**

**ORM (Online Read Margin)**

**P-VOL (Primary Volume)**

**PBC (Port Bypass Circuit)**

**PCB (Printed Circuit Board)**

**PCI CON (Power Control Interface Connector Board)**

**RCP (Remote Control Port)**

**RCU (Remote Disk Control Unit)**

**RLGFAN (Rear Logic Box Fan Assembly)**

**RLOGIC BOX (Rear Logic Box)**

**RPSFAN (Rear Power Supply Fan Assembly)**

**RS CON (RS232C/RS422 Interface Connector)**

**S-VOL (Secondary Volume)**

**SHSN (Shared memory Hierarchical Star Network)**

**SIM (Service Information Message)**

**SIM RC (Service Information Message Reference Code)**

**SM (Shared Memory Module)**

Stores the shared information about the subsystem and the cache control information (director names). This type of information is used for the exclusive control of the subsystem. Like CACHE, shared memory is controlled as two areas of memory and fully non-volatile (sustained for approximately 7 days).

**SMC (Shared Memory Control)****SM PATH (Shared Memory Access Path)**

Access Path from the processors of CHA, DKA PCB to Shared Memory.

**SNMP (Simple Network Management Protocol)****SSB (Sense Byte)****SVP (Service Processor)**

Controls the communication with the SVP.

**T.S.D (Technical Support Division)****Tach (Tachyon)****THF (Front Thermostat)****THR (Rear Thermostat)****WWN (World Wide Name)**