Integrated Device Technology, Inc.

128KB/256KB SECONDARY CACHE MODULE FOR THE INTEL i486™

IDT7MP6104
IDT7MP6105

FEATURES

- 128KB/256KB direct mapped, write-through, non-sectored, zero-wait-state secondary cache module
- Ideal for use with i486-based systems
- Uses IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and IDT71B74 cache-tag RAM
- Operates with external i486™ speeds of 25 and 33MHz
- Concurrent snooping is supported
- Software Instruction flushing is supported
- Write-protect function is detailed in IDT Technical Note TN-14
- 64-position dual read-out SIMM (Single In-line Memory Module) with 128 leads
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

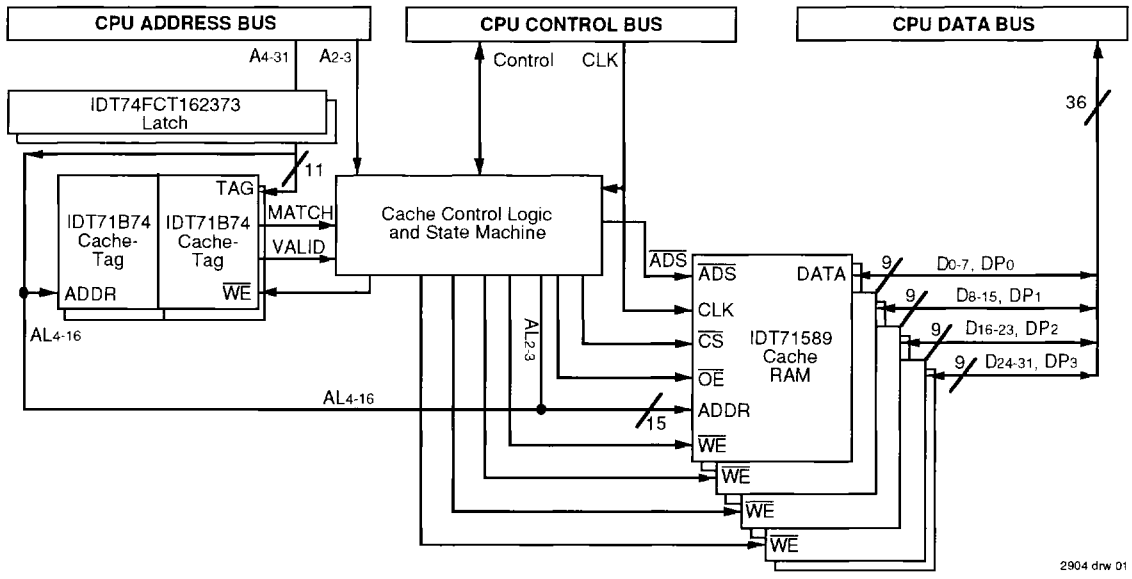
DESCRIPTION

The IDT7MP6104/7MP6105 is a 128KB/256KB direct-mapped, write-through, non-sectored, zero-wait-state secondary cache and is ideal for use with many i486-based systems. The IDT7MP6104/7MP6105 uses IDT71589 32K x 9 CacheRAMs, IDT71B74 8K x 8 cache-tag RAMs, IDT74FCT162373 Double-Density™ 16-bit latches along with cache control logic in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. Extremely high speeds are achieved using IDT's high-performance, -high-reliability BiCMOS and CMOS technologies.

The dual read-out SIMM package configuration allows 128 signal leads to be placed on a package 3.85" x 0.215" x 1.3" (LxWxH) for the 7MP6104 version while the 7MP6105 has a width of 0.420".

All inputs and outputs of the IDT7MP6104/7MP6105 are TTL-compatible and operate from a single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION[1]

GND	65	1	GND
RESET	66	2	CLK
V_{CC}	67	3	V_{CC}
NC	68	4	NC
M/$\overline{IO}$	69	5	D/$\overline{C}$
$\overline{FLUSH}$	70	6	$\overline{BLAST}$
$\overline{EADS}$	71	7	$\overline{BOFF}$
GND	72	8	GND
$\overline{ADS}$	73	9	W/$\overline{R}$
$\overline{BE_0}$	74	10	$\overline{BE_1}$
$\overline{BE_2}$	75	11	$\overline{BE_3}$
NC	76	12	$\overline{CS}$
$\overline{CRDY}$	77	13	$\overline{CKEN}$
GND	78	14	GND
$\overline{CBRDY}$	79	15	$\overline{BRDYO}$
$\overline{SKEN}$	80	16	$\overline{START}$
WP	81	17	NC
$\overline{PRSN}$	82	18	NC
NC	83	19	NC
NC	84	20	NC
A_2	85	21	A_3
V_{CC}	86	22	V_{CC}
A_4	87	23	A_5
A_6	88	24	A_7
A_8	89	25	A_9
A_{10}	90	26	A_{11}
A_{12}	91	27	A_{13}
A_{14}	92	28	A_{15}
A_{16}	93	29	A_{17}
GND	94	30	GND
A_{18}	95	31	A_{19}
A_{20}	96	32	A_{21}
A_{22}	97	33	A_{23}
A_{24}	98	34	A_{25}
A_{26}	99	35	A_{27}
A_{28}	100	36	A_{29}
A_{30}	101	37	A_{31}
GND	102	38	GND
D_0	103	39	D_1
D_2	104	40	D_3
D_4	105	41	D_5
V_{CC}	106	42	V_{CC}
D_6	107	43	D_7
GND	108	44	GND
DP_0	109	45	DP_1
D_8	110	46	D_9
D_{10}	111	47	D_{11}
D_{12}	112	48	D_{13}
GND	113	49	GND
D_{14}	114	50	D_{15}
D_{16}	115	51	D_{17}
D_{18}	116	52	D_{19}
D_{20}	117	53	D_{21}
GND	118	54	GND
D_{22}	119	55	D_{23}
DP_2	120	56	DP_3
D_{24}	121	57	D_{25}
D_{26}	122	58	D_{27}
GND	123	59	GND
D_{28}	124	60	D_{29}
D_{30}	125	61	D_{31}
V_{CC}	126	62	V_{CC}
ID_1	127	63	ID_0
GND	128	64	GND

SIMM
TOP VIEW

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NOTE:
1. Module pins 63 and 127 are used to identify the size of the cache present in the socket. Consult the ID Truth Table for more details.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2904 tbl 02

NOTE:
1. V_{IL} = –3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

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CAPACITANCE[1, 2]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	7MP6104/5	Unit
C_{IN}	Input Capacitance (Address, Control)	V_{IN} = 0V	15/25	pF
C_{IN}	Input Capacitance (CLK)	V_{IN} = 0V	45/80	pF
C_{OUT}	Output Capacitance (Control)	V_{IN} = 0V	15/15	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	10/20	pF

2904 tbl 04

NOTES:
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

ID TRUTH TABLE

ID1	ID0	Cache Size
1	1	128KB cache module
1	0	256KB cache module
0	1	512KB cache module
0	0	1MB cache module

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PIN DESCRIPTION

Symbol	Parameter	Type	Active	Description
CLK	Clock	Input	N/A	This input is the timing reference for all of the IDT7MP6104/5's functions. It is the same as the i486 CLK input.
RESET	Reset Cache	Input	HIGH	A synchronous positive-true reset input, which invalidates all cache locations and resets the cache control logic.
$\overline{ADS}$	Address Strobe	Input	LOW	$\overline{ADS}$ is connected to the ADS# pin of the i486 CPU. It is used by the IDT7MP6104/5 to start any read or write cycle. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	Memory/IO	Input	N/A	This pin is used by the i486 to indicate whether the current cycle is a memory or I/O cycle. I/O cycles are not cacheable by the IDT7MP6104/5.
W/$\overline{R}$	Write/Read	Input	N/A	Write cycles are indicated by a HIGH level on this pin, and read cycles are indicated by a LOW level.
D/$\overline{C}$	Data/Control	Input	N/A	This pin is connected to the D/C# pin of the i486 CPU. It is used by the IDT7MP6104/5 in conjunction with M/$\overline{IO}$, W/$\overline{R}$, and $\overline{BE}_{0-3}$ to determine when a software flush is being executed by the i486.
$\overline{START}$	Memory Start	Output	LOW	During a cache read miss cycle or a write cycle, the $\overline{START}$ pin signals that the main memory system should service the current access.
$\overline{BRDYO}$	Burst Ready Out	Output	LOW	This is the IDT7MP6104/5's means of signaling to the i486 that cache data is ready to be sampled.
$\overline{CBRDY}$	Cache Burst Ready In	Input	LOW	This is the system input to the IDT7MP6104/5 to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MP6104/5 during a burst access.
$\overline{CRDY}$	Cache Ready In	Input	LOW	This is the system input to the IDT7MP6104/7MP6105 to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MP6104/5 during a non-burst access.
$\overline{BLAST}$	Burst Last	Input	LOW	This i486 output indicates to the IDT7MP6104/5 cache control logic that the current cycle is the last cycle of a burst access.
$\overline{BOFF}$	Backoff	Input	LOW	This signal is used to stall the IDT7MP6104/5. The IDT7MP6104/5 will also put its data bus into a high-impedance state. The IDT7MP6104/5 will only recognize invalidation cycles when $\overline{BOFF}$ is asserted.
$\overline{PRSN}$	Presence	Output	LOW	This pin is hard-wired to ground. It tells the system logic that the IDT7MP6104/5 is plugged into the system.
A_2-A_{31}	Processor Addresses	Input	N/A	These are the address inputs to the IDT7MP6104/5.
$\overline{BE}_0$-$\overline{BE}_3$	Byte Enable	Input	LOW	The byte enable inputs are sampled only during CPU write cycles and are only used to control byte writes to valid cache lines during write hit cycles. The timing is the same as for the address input pins.
$\overline{CS}$	Chip Select	Input	LOW	Chip select can be used for depth expansion. $\overline{CS}$ must be asserted for $\overline{EADS}$ or $\overline{ADS}$ to be recognized by the IDT7MP6104/5.
D_0-D_{31}	Processor Data Lines	I/O	N/A	These are the data inputs from either the i486 or the system memory. D_0-D_7 define the least significant byte while D_{24}-D_{31} define the most significant byte.
DP_0-DP_3	Data Parity	I/O	N/A	These are the parity bits from either the i486 or the system memory. The timing requirements are the same as the data lines.
$\overline{CKEN}$	Cache Enable To CPU	Output	LOW	This signal is the cache enable signal generated by the IDT7MP6104/5. The IDT7MP6104/5 will always assert $\overline{CKEN}$ during T1 cycles and during read hit cycles before the last $\overline{BRDYO}$. The IDT7MP6104/5 will not assert $\overline{CKEN}$ during read miss cycles.
$\overline{SKEN}$	System Cache Enable	Input	LOW	This signal is generated by the system to indicate that a line is cacheable. The IDT7MP6104/5 will look for $\overline{SKEN}$ to be asserted at least one cycle before the first word transfer and the cycle before the last word transfer of a line fill.
$\overline{FLUSH}$	Flush Cache	Input	LOW	This signal causes the IDT7MP6104/5 to invalidate its entire cache contents.
WP	Write Protect	Input	HIGH	The write protect input is only sampled during the third transfer of a line fill. If a line is flagged as write protected during a line fill, it is considered non-cacheable.
$\overline{WPSTRP}$	Write Protect Strap	N/A	N/A	This signal is not used by the IDT7MP6104/5.
$\overline{EADS}$	Valid External Address	Input	LOW	This signal indicates that an invalidation address is present on the IDT7MP6104/5 address bus. $\overline{CS}$ must be asserted for $\overline{EADS}$ to be recognized by the IDT7MP6104/5.

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FUNCTIONAL DESCRIPTION

Basic Operation

The IDT7MP6104/7MP6105 is a complete secondary cache subsystem designed for use with the Intel i486 CPU. The IDT7MP6104/7MP6105 is designed to support zero-wait-state line reads, i.e. four words of data in five clocks. The IDT7MP6104/7MP6105 supports all of the following bus cycles: read hit, read miss, write hit, write miss, invalidation and backoff. The IDT7MP6104/7MP6105 also features single pin reset and cache flush capabilities.

The IDT7MP6104/7MP6105 latches the address at the input of the module at the beginning of any read, write or invalidation cycle. The address remains latched for one cycle after the initiation of a read or write, and the address remains latched for two cycles after the initiation of an invalidation.

Reset

The IDT7MP6104/7MP6105 is reset when RESET is asserted. Asserting RESET will invalidate the entire contents of the cache, and reset the control logic of the cache. The cache will be reset regardless of the state of other control signals when RESET is asserted.

Flush

The entire cache contents of the IDT7MP6104/7MP6105 is invalidated when the $\overline{FLUSH}$ input is asserted. The cache will be invalidated regardless of the state of other control signals when $\overline{FLUSH}$ is asserted. $\overline{FLUSH}$ will not reset the cache control logic.

The IDT7MP6104/7MP6105 is also flushed when the i486 executes an INVD or a WBINVD command. The IDT7MP6104/7MP6105 determines the execution of these commands by detecting when the i486 issues a flush special bus cycle. The flush special bus cycle is indicated by the i486 when the D/$\overline{C}$=0, M/$\overline{IO}$=0, W/$\overline{R}$=1, $\overline{BE}_3$=1, $\overline{BE}_2$=1, $\overline{BE}_1$=0, and $\overline{BE}_0$=1.

Read

The IDT7MP6104/7MP6105 recognizes the initiation of a read cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled LOW with M/$\overline{IO}$ HIGH and W/$\overline{R}$ LOW. As soon as the address is valid at the input of the module, the IDT7MP6104/7MP6105 begins its tag look-up. If the input address is not contained in the cache, then a miss has occurred, and the IDT7MP6104/7MP6105 will wait for the main memory system to service the current access. If the input address is present in the cache, then a hit has occurred, and the IDT7MP6104/7MP6105 will burst back a line of data to the CPU.

The IDT7MP6104/7MP6105 will not accept data returned in zero wait states. The earliest the IDT7MP6104/7MP6105 can accept data is the cycle after $\overline{START}$ is asserted.

The IDT7MP6104/7MP6105 will consider the data returned from the memory system as cacheable if $\overline{SKEN}$ is sampled LOW at least one cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first asserted. The IDT7MP6104/7MP6105 will load the data word returned from the memory system into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. If WP is sampled HIGH during the third word transfer of a line fill, the line is considered write protected, and the line of data is not validated. If the line is not write protected, the IDT7MP6104/7MP6105 will only validate the line of data returned from the memory system if $\overline{SKEN}$ is sampled LOW the cycle before the last data word is transferred from the memory system, i.e. the fourth time that $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW. The line fill is aborted if $\overline{BLAST}$ is sampled LOW concurrent with $\overline{CBRDY}$ or $\overline{CRDY}$ being sampled LOW prior to the last data word transfer.

The IDT7MP6104/7MP6105 will consider the data returned as non-cacheable if $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW before, or concurrently, with $\overline{SKEN}$ prior to the first word transfer. Therefore, to avoid a potential performance penalty, $\overline{SKEN}$ should not be asserted prior to $\overline{CBRDY}$ or $\overline{CRDY}$ if the data is considered non-cacheable, since the IDT7MP6104/7MP6105 will invalidate a line of data if $\overline{SKEN}$ is sampled LOW before $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled LOW during a read miss.

The IDT7MP6104/7MP6105 requires that the read miss address (i.e. the address that was valid at the beginning of the read cycle) is present when $\overline{SKEN}$ is sampled LOW at the beginning of a line fill and again when $\overline{SKEN}$ is sampled at the end of a line fill. The address must be valid because it is latched at these times to invalidate a line at the beginning of the fill and then to validate the line at the end of the line fill. When the address is latched at the end of the line fill, it will remain latched until the last data word of the line is written to the cache.

If the IDT7MP6104/7MP6105 detects that the input address is contained in the cache, the IDT7MP6104/7MP6105 will supply data to the CPU. The IDT7MP6104/7MP6105 starts bursting data back to the CPU in the first T2 cycle. The IDT7MP6104/7MP6105 then transfers a new data word in each subsequent T2 cycle until $\overline{BLAST}$ is asserted to the cache. The IDT7MP6104/7MP6105 also forces $\overline{START}$ HIGH and $\overline{BRDYO}$ LOW in the first T2 cycle. $\overline{CKEN}$ is asserted during the T1 cycle and again in the second, and subsequent, T2 cycles during a read hit.

Write

The IDT7MP6104/7MP6105 recognizes the initiation of a write cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled LOW with M/$\overline{IO}$ HIGH and W/$\overline{R}$ HIGH. As soon as the address is valid at the input of the module, the IDT7MP6104/7MP6105 begins its tag look-up. If the input address is contained in the cache, then a write hit has occurred, and the cache contents are updated when $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system. The IDT7MP6104/7MP6105 requires the address to be valid in the cycle that the data is written to the cache, i.e. when $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system; this requirement should have no impact at the system level since the i486 will maintain both the address and data on its outputs until the write cycle is completed. If the input address is not contained in the cache, then a write miss has occurred, the IDT7MP6104/7MP6105 ignores the write, and the cache contents are not updated. For both write hits and write misses the IDT7MP6104/7MP6105 will assert $\overline{START}$ until $\overline{CRDY}$ or $\overline{CBRDY}$ is returned from the system.

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Invalidation

An invalidation is initiated by the simultaneous assertion of $\overline{EADS}$ and $\overline{CS}$. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored since invalidations have priority. At the initiation of an invalidation, the IDT7MP6104/7MP6105 begins its tag look-up. If the line is found in the cache, the line will be invalidated. The IDT7MP6104/7MP6105 requires two cycles after the assertion of $\overline{EADS}$ to invalidate a line; therefore, invalidations can only occur every third cycle. The IDT7MP6104/7MP6105 ignores invalidations only if an address is currently latched in the address latch. Therefore, the IDT7MP6104/7MP6105 ignores invalidations at the following times: the cycle after the initiation of a read or write cycle, the cycle after $\overline{SKEN}$ is first sampled LOW during a line fill, the cycle(s) after sampling $\overline{SKEN}$ LOW concurrent with (or after) the third word transfer and prior to the fourth word transfer of a line fill, and the two cycles following a previous invalidation.

Backoff

A cache backoff is initiated by the assertion of $\overline{BOFF}$. $\overline{BOFF}$ interrupts any other cache cycle that the IDT7MP6104/7MP6105 is servicing. The cycle after $\overline{BOFF}$ is sampled LOW, the IDT7MP6104/7MP6105 will float its data bus, and the output control signals are driven to their idle levels, i.e. $\overline{CKEN}$ LOW, $\overline{START}$ HIGH and $\overline{BRDYO}$ HIGH. When $\overline{BOFF}$ is asserted, the IDT7MP6104/7MP6105 ignores all cache cycles except for invalidations; however, the IDT7MP6104/7MP6105 will still recognize the assertion of RESET or $\overline{FLUSH}$ when $\overline{BOFF}$ is asserted.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

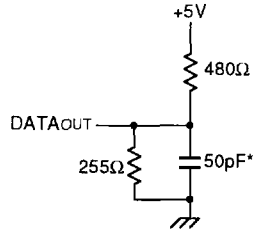
Symbol	Parameter	Test Condition	7MP6104/5 Min.	7MP6104/5 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Data)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10/20	µA
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage Current (Control)	V_{CC} = Max, V_{IN} = GND to V_{CC}	–10/–300	10/60	µA
$\|I_{LI}\|$	Input Leakage Current (CLK)	V_{CC} = Max, V_{IN} = GND to V_{CC}	–50/–380	50/140	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10/20	µA
V_{OLD}	Output Low Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OLC}	Output Low Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min.	—	0.5	V
V_{OHD}	Output High Voltage (Data)	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output High Voltage (Control)	I_{OH} = –2mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1350/3050	mA

2904 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2904 tbl 08



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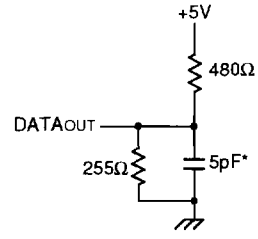
*including scope and jig

Figure 1. Output Load



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*including scope and jig

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

Symbol	Parameter	7MP6104/5S33M		Unit
		Min.	Max.	
t_1	Clock Period	30	—	ns
t_2	Clock HIGH Time	11	—	ns
t_3	Clock LOW Time	11	—	ns
t_4	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Set-up Time	13	—	ns
t_5	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Hold Time	10	—	ns
t_6	A_4-A_{31} Line Fill Set-up Time	5	—	ns
t_7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$, D/$\overline{C}$ Set-up Time	13	—	ns
t_8	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$, D/$\overline{C}$ Hold Time	3	—	ns
t_9	$\overline{BLAST}$, $\overline{CS}$ Set-up Time	9	—	ns
t_{10}	$\overline{BLAST}$, $\overline{CS}$ Hold Time	3	—	ns
t_{11}	$\overline{CRDY}$, $\overline{CBRDY}$ Set-up Time	11	—	ns
t_{12}	$\overline{CRDY}$, $\overline{CBRDY}$ Hold Time	3	—	ns
t_{13}	$\overline{SKEN}$ Set-up Time	9	—	ns
t_{14}	$\overline{SKEN}$ Hold Time	3	—	ns
t_{15}	D_0-D_{31}, DP_0-DP_3 Set-up Time	5	—	ns
t_{16}	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	ns
t_{17}	$\overline{EADS}$ Set-up Time	9	—	ns
t_{18}	$\overline{EADS}$ Hold Time	3	—	ns
t_{19}	A_4-A_{31} Set-up Time (Snoop)	6	—	ns
t_{20}	A_4-A_{31} Hold Time (Snoop)	10	—	ns
t_{21}	RESET, $\overline{FLUSH}$ Set-up Time	9	—	ns
t_{22}	RESET, $\overline{FLUSH}$ Hold Time	3	—	ns
t_{23}	RESET, $\overline{FLUSH}$ Pulse Width	80	—	ns
t_{24}	$\overline{BRDYO}$ Valid	—	16	ns
t_{25}	$\overline{CKEN}$ Valid	—	15	ns
t_{26}	$\overline{START}$ Valid	—	16	ns
t_{27}	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit)	—	24	ns
t_{28}	WP Set-up Time	9	—	ns
t_{29}	WP Hold Time	3	—	ns
t_{30}	$\overline{BOFF}$ Set-up Time	9	—	ns
t_{31}	$\overline{BOFF}$ Hold Time	3	—	ns

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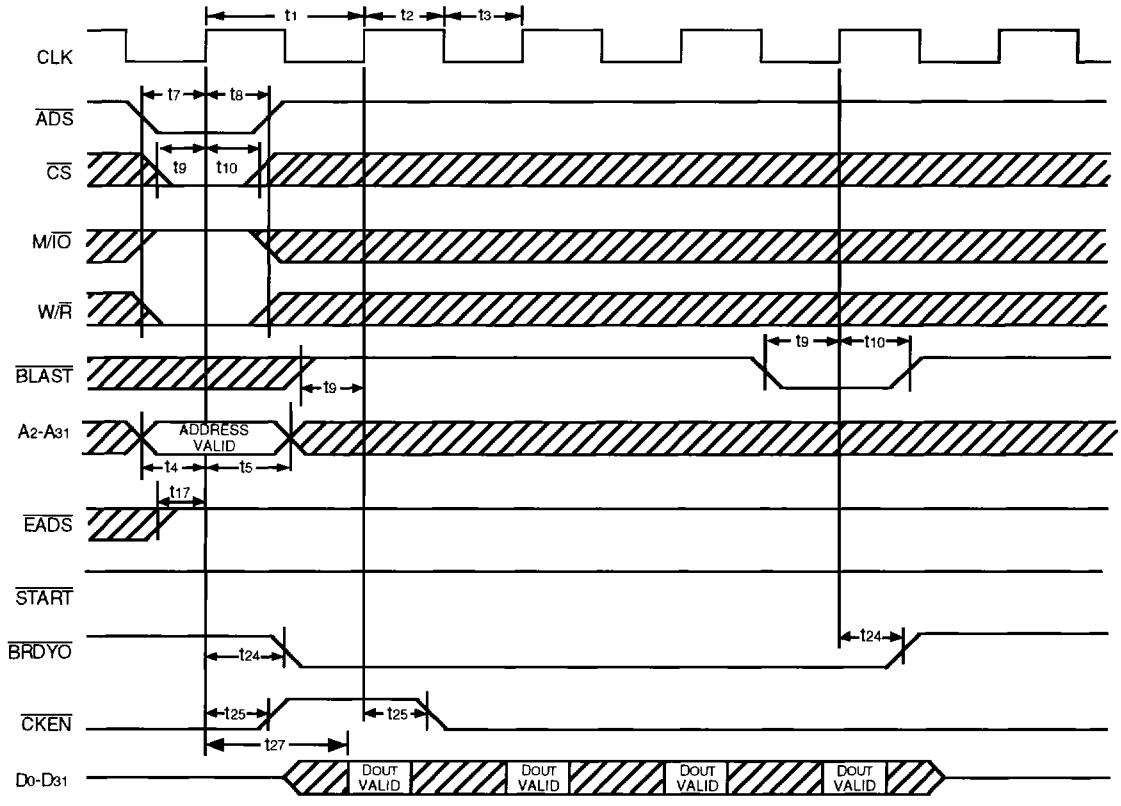
TIMING WAVEFORM OF A READ HIT CYCLE (READ LINE)(1)



NOTE:
1. RESET is held LOW, FLUSH is held HIGH, BOFF is held HIGH.

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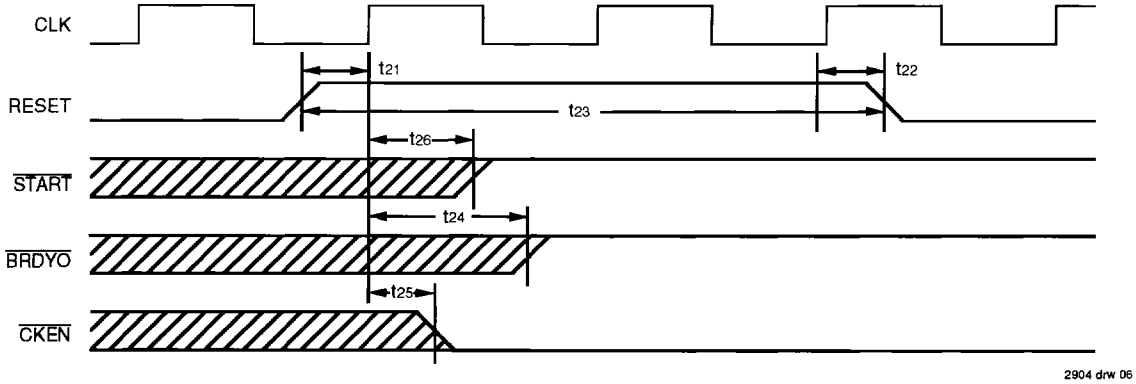
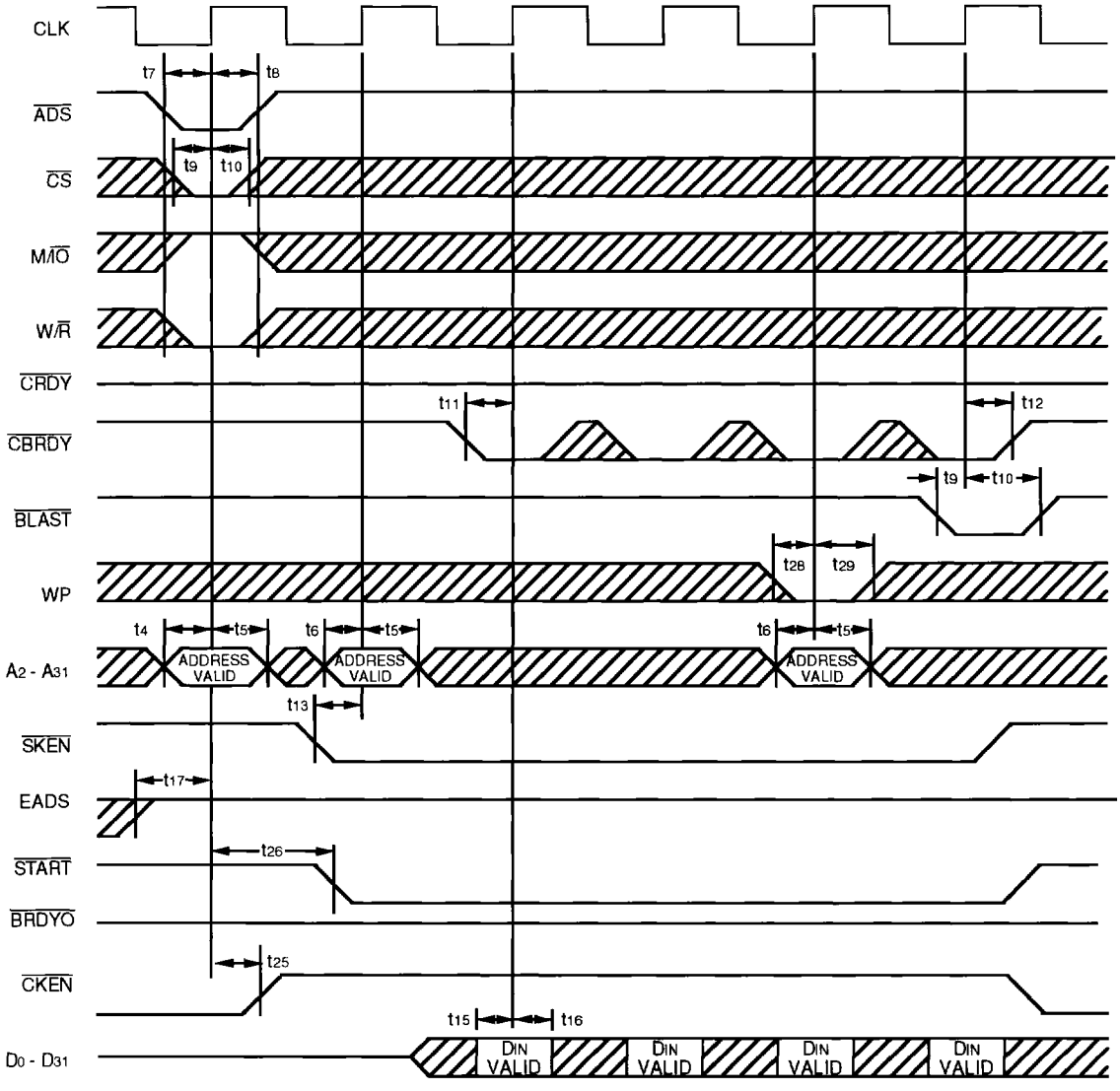
TIMING WAVEFORM OF A RESET OPERATION



2904 drw 06

TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)(1)

(NON-WRITE PROTECTED)

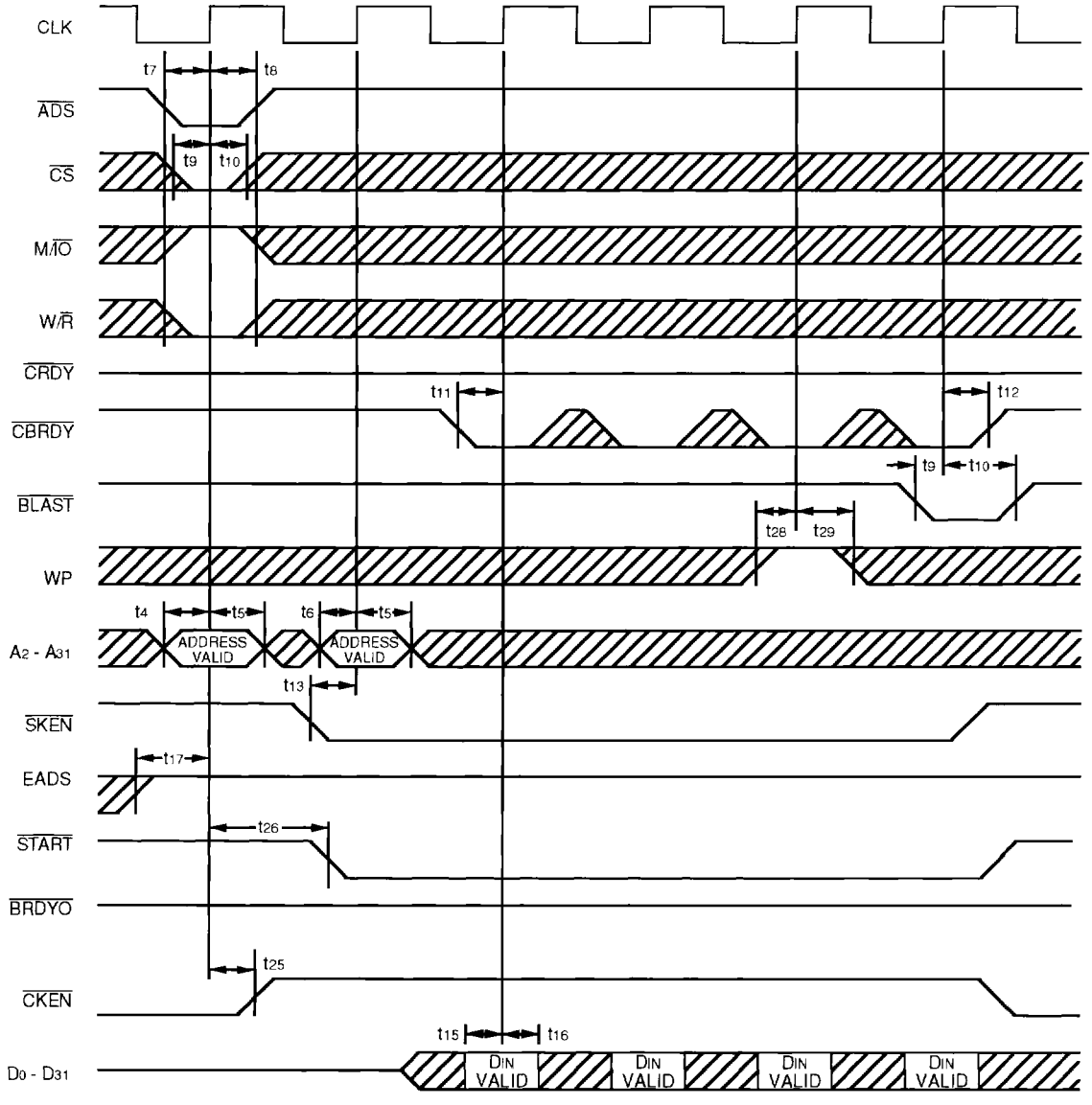


NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

2904 drw 07

TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)[1]

(WRITE PROTECTED)

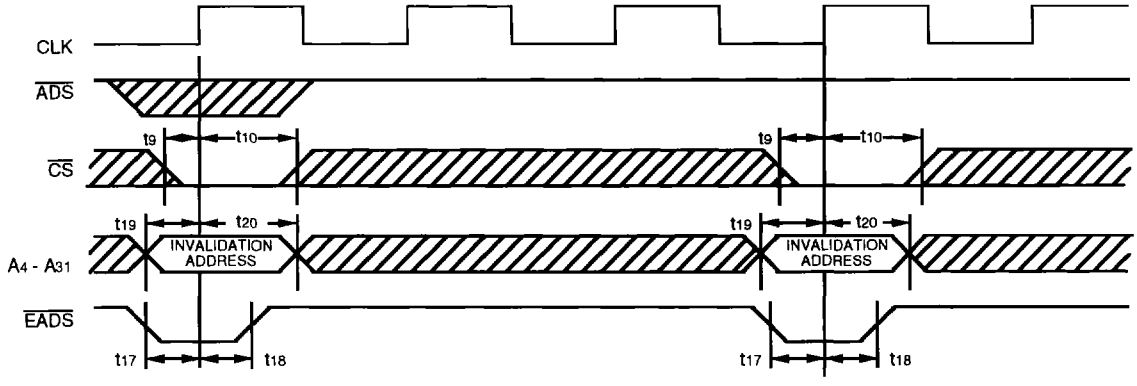


NOTE:

1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

2904 drw 08

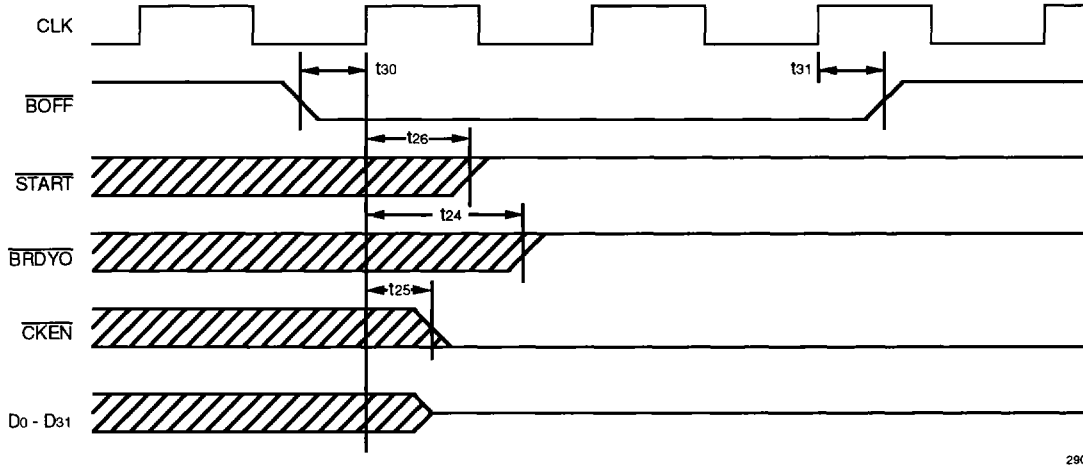
TIMING WAVEFORM OF A CACHE INVALIDATION(1)



2904 drw 09

NOTE:
1. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored.

TIMING WAVEFORM OF A BACKOFF OPERATION



2904 drw 10

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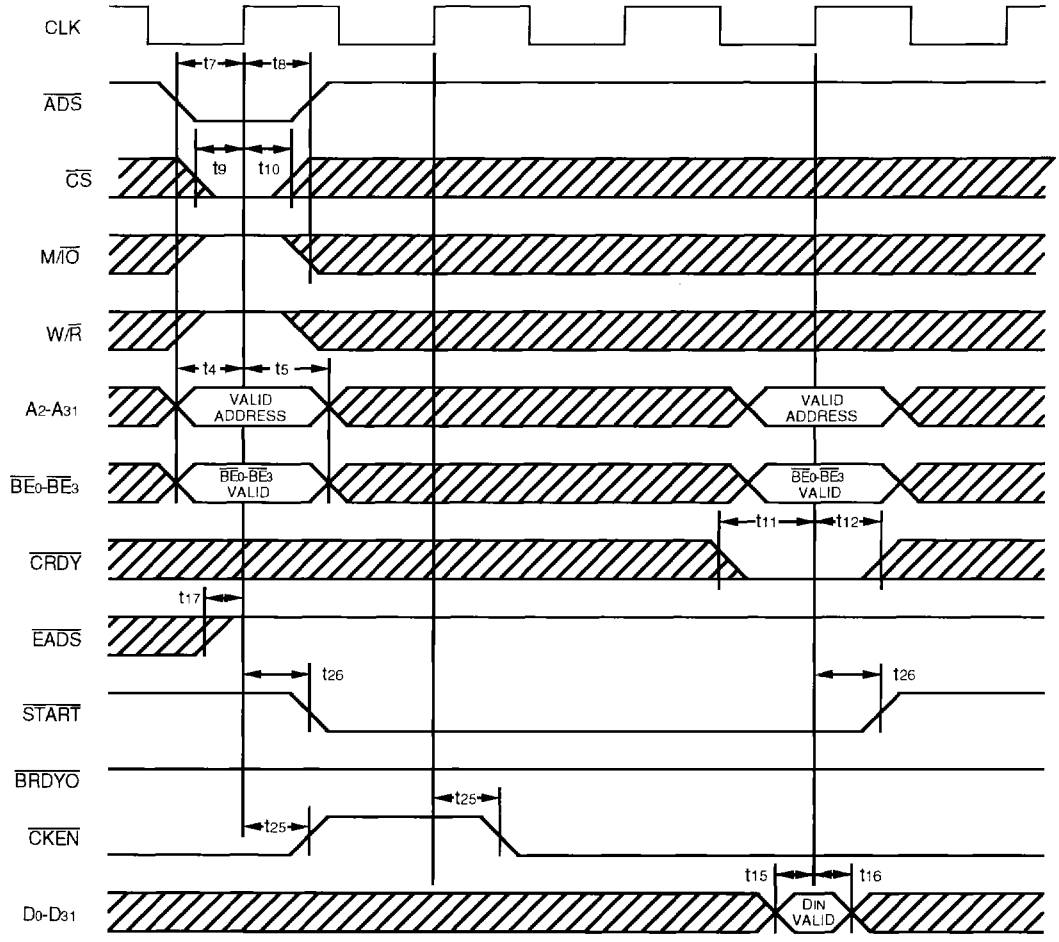
TIMING WAVEFORM OF A WRITE CYCLE(1, 2)

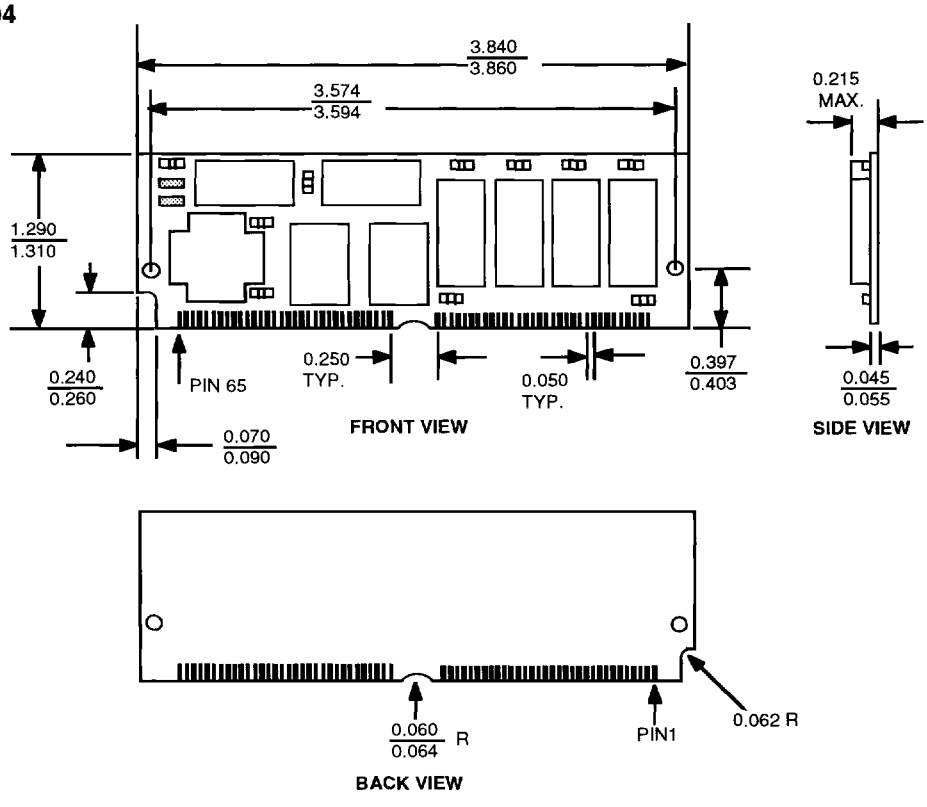


2904 drw 11

NOTES:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.
2. For a write hit, data in the IDT7MP6104/7MP6105 is updated.

PACKAGE DIMENSIONS

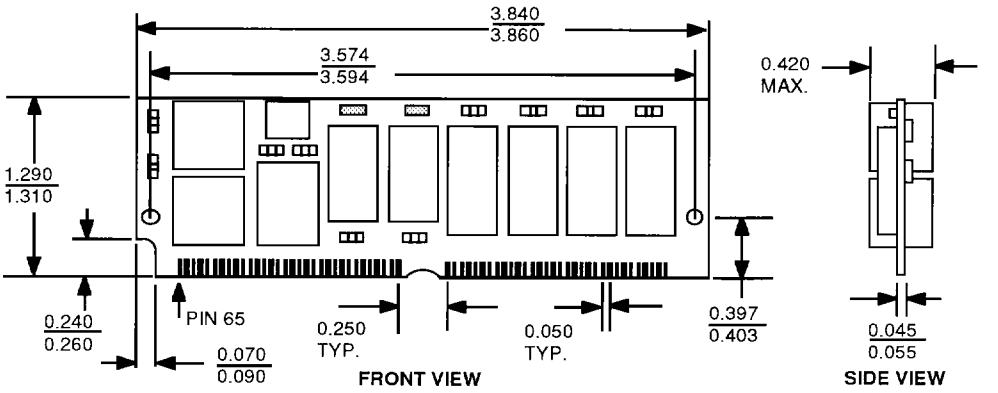
7MP6104

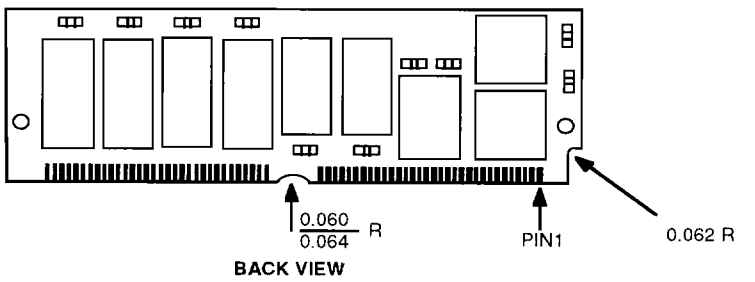


2904 drw 12

7

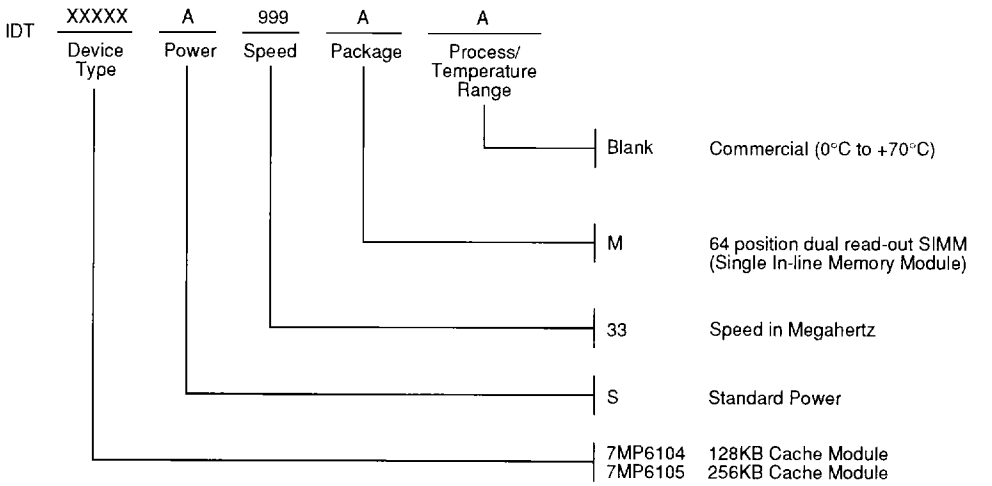
7MP6105





2904 drw 13

ORDERING INFORMATION



2904 drw 14