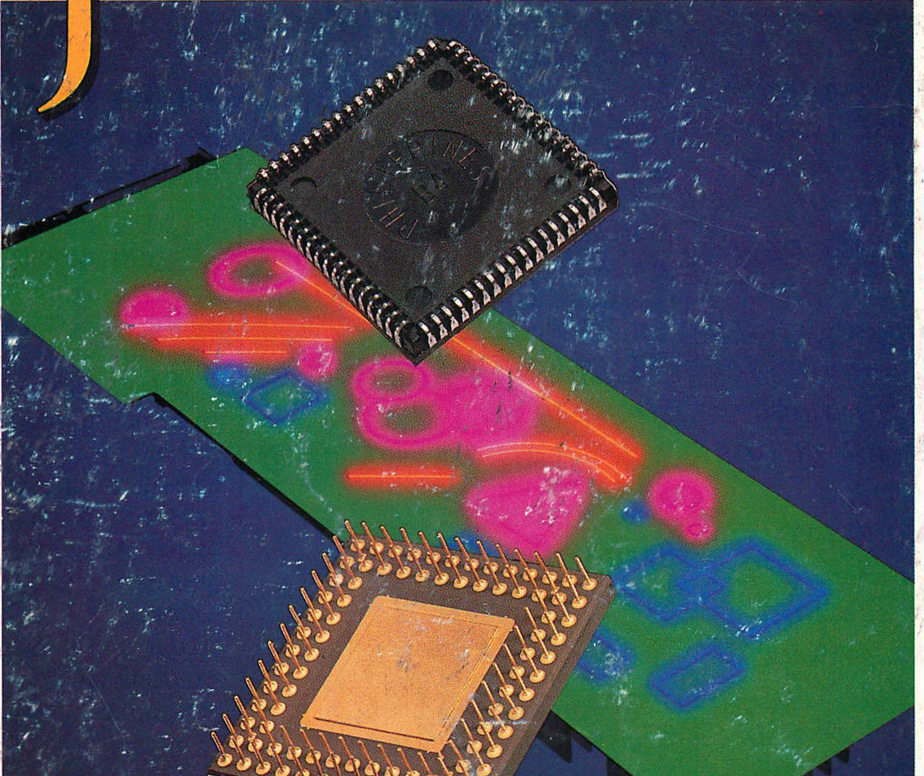
JULY 1987 VOL. 5 NO. 7 $3.95

FOR THE SYSTEMS PROFESSIONAL

PC TECH JOURNAL



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Our technology is so advanced, it's easy to use

With Turbo Pascal® we invented fast compilers, and followed that technological breakthrough with Turbo Prolog®, then Turbo Basic®, then Turbo C.® Building these fast compilers is not an easy task. It was and is "the little guy" taking a giant step. And having transformed Languages with our new superfast compiler technology, we've turned the same power loose onto our Business products like SideKick® and Reflex®:The Database Manager.

> *SideKick continues to influence not only the utilities market but the entire software industry.*
>
> William Urschel, PC World

When Borland was founded 4 years ago, the software industry technology level was about C– on a scale of A to F. Which was and is a perfect opportunity for a technology-driven company like Borland. Call us "techies," but we're developers, technicians, tinkerers who know how to make programs run faster, do more, be more and let you fully use the hardware power you've paid for.

At Borland, Price is one thing, but Technology is the main thing

There's no sense in the "price being right" if the product is wrong. A useless product is something you can't give away. Technical excellence and superiority always comes ahead of Price. Always has. Always will at Borland. Our technical leadership began when we invented fast compilers and hasn't been matched since.

Turbo Pascal: The worldwide standard

Pascal was asleep before we transformed it with a technical shot in the arm. Our unique ability to create spectacularly fast compilers was the driving force behind Turbo Pascal's worldwide success.

> *For the IBM PC, the benchmark Pascal compiler is undoubtedly Borland International's Turbo Pascal.*
>
> Garry Ray, PC WEEK

Turbo Basic: BASIC raised to a new power

We've raised BASIC from the dead with our recent high-speed Turbo Basic. Of course, Microsoft will try to sell you their "QuickBASIC," but we think you're interested in "fast," not "quick." Because we're a smaller company, we had to make Turbo Basic the "best BASIC development environment ever written." Otherwise, we'd be out of business. We try harder.

> *Borland International's Turbo Basic is unquestionably an outstanding software product.*
>
> Giovanni Perrone, PC WEEK

> *Turbo Basic is a compiled BASIC. This gives it execution speeds that leave standard interpretive BASICs like BASICA and GW BASIC in the dust.*
>
> William Zachmann
> COMPUTERWORLD

Turbo Prolog: The natural language of Artificial Intelligence

Turbo-charging Prolog was an enormous challenge. Creating a development environment on an ordinary PC that would rival those found on dedicated AI workstations like Sun and Apollo was deemed impossible. Enter Turbo Prolog. Exit the rest.

> *Turbo Prolog has one of the most powerful user interfaces ever seen in a software development system.*
>
> Tom Swan
> Programmer's Journal

> *If you're at all interested in artificial intelligence, databases, expert systems, or new ways of thinking about programming, by all means plunk down your $100 and buy a copy of Turbo Prolog.*
>
> Bruce Webster, Byte

Turbo C: Perhaps the most powerful professional development environment ever written

We've brought tomorrow's technology to Turbo C, which is so fast that it makes the rest look like dead Cs. We've given Turbo C a revolutionary user interface making it a wonderful productivity booster. And in keeping with our commitment to open architectures, we are even offering our users the opportunity to license the source code to Turbo C's runtime library.

> “ *Turbo C does look like What We've All Been Waiting For: a full-featured compiler that produces excellent code in an unbelievable hurry . . .*
> *. . . moves into a class all its own among full-featured C compilers . . .*
> *. . . Turbo C is indeed for the serious developer . . . One heck of a buy—at any price.*
>
> Michael Abrash
> Programmer's Journal ”

> “ *Borland International's Turbo Pascal, Turbo Basic and Turbo Prolog automatically identify themselves, by virtue of their "Turbo" forenames, as superior language products with a common programming environment. The apellation also means, to many PC users, a "must have" language . . .*
> *. . . To us, Turbo C looks like a coup for Borland.*
>
> Garry Ray, PC Week ”

Reflex: The Database Manager

With Reflex, we brought new eyes and understanding to spreadsheets with unheard-of graphics, charts, plots and analysis. And just as we do in our Language products, we've added our Reflex Workshop™, a "business toolbox" which gives you everything you need to set up and run more than 20 different kinds of business.

> “ *Reflex actually improves on 1-2-3 in several respects.*
>
> William Casey, PC Tech Journal ”

> “ *Reflex and Reflex Workshop may be the best bargain in software today. Highly recommended.*
>
> Jerry Pournelle, Byte ”

Eureka™: The equation solver for Scientists, Engineers, Students and Professionals

Eureka is as much a step forward in equation solving as spreadsheets have been for accounting and planning. Using Eureka with your PC gives you high performance in desktop engineering. A must!

> “ *Eureka is fast, and simple to use.*
>
> Michael Miller, InfoWorld ”

Sprint®: Bringing all that technology together

Word Processors? There are a lot of good ones around. WordPerfect™, WordStar® 4.0, and MicroSoft® Word are good products. But to compete, we had to build a better product. And using some of the technology we pioneered in our fast compilers, we set out to build the best professional word processor ever written.

We spent a lot of time listening to word processor users. Finding out what they liked, and what they really didn't like about the programs they were using.

We looked at all the features of current word processors and figured out how to make them better. That's how we designed Sprint: The Professional Word Processor, which you'll soon discover is faster, easier, smarter than the rest, and probably the most powerful word processor ever written. Sprint is well worth the wait—and you won't be waiting long.

> “ *Sprint: The Word Processor is a many-splendored package.*
>
> Ken Greenberg, PC World ”

Why it's good for you that Borland's in the business of Business

At Borland, small is actually beautiful. Either Joy or Anne or Dyane will answer the phone—but don't get fresh, because they're all happily married. Call Borland and you talk to an actual human being who doesn't give you the big corporate runaround, but the right extension number. You'll get help, whether it's tech support, questions about new products, or whatever. (We've always had a 60-day money-back guarantee, so we don't get too many calls about that.)

When you're small, you try harder, so what we've done is just that.

Borland has to be a whole lot better because our competition is a whole lot bigger

At Borland we're competing with giants like Microsoft and Lotus, so we have to try harder. Out-think them, out-smart them, out-pace them, out-perform them—because we obviously can't out-spend them.

What that means to you—which is all that really matters—is that you now have access to the world's fastest compilers, because we were forced to invent them to compete with the giants. We may be smaller than they are, but we're absolutely, positively not slower than they are.

In the long run what really counts is technological excellence.

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Turbo Pascal Numerical Methods Toolbox™
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The new collection of efficient, "smart" tools for use with our highly-acclaimed Turbo Prolog,® the natural language of Artificial Intelligence
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It's the high-speed BASIC you'd expect from Borland. A complete development environment including an amazingly fast compiler, interactive editor and trace debugging system. Compatible with BASICA
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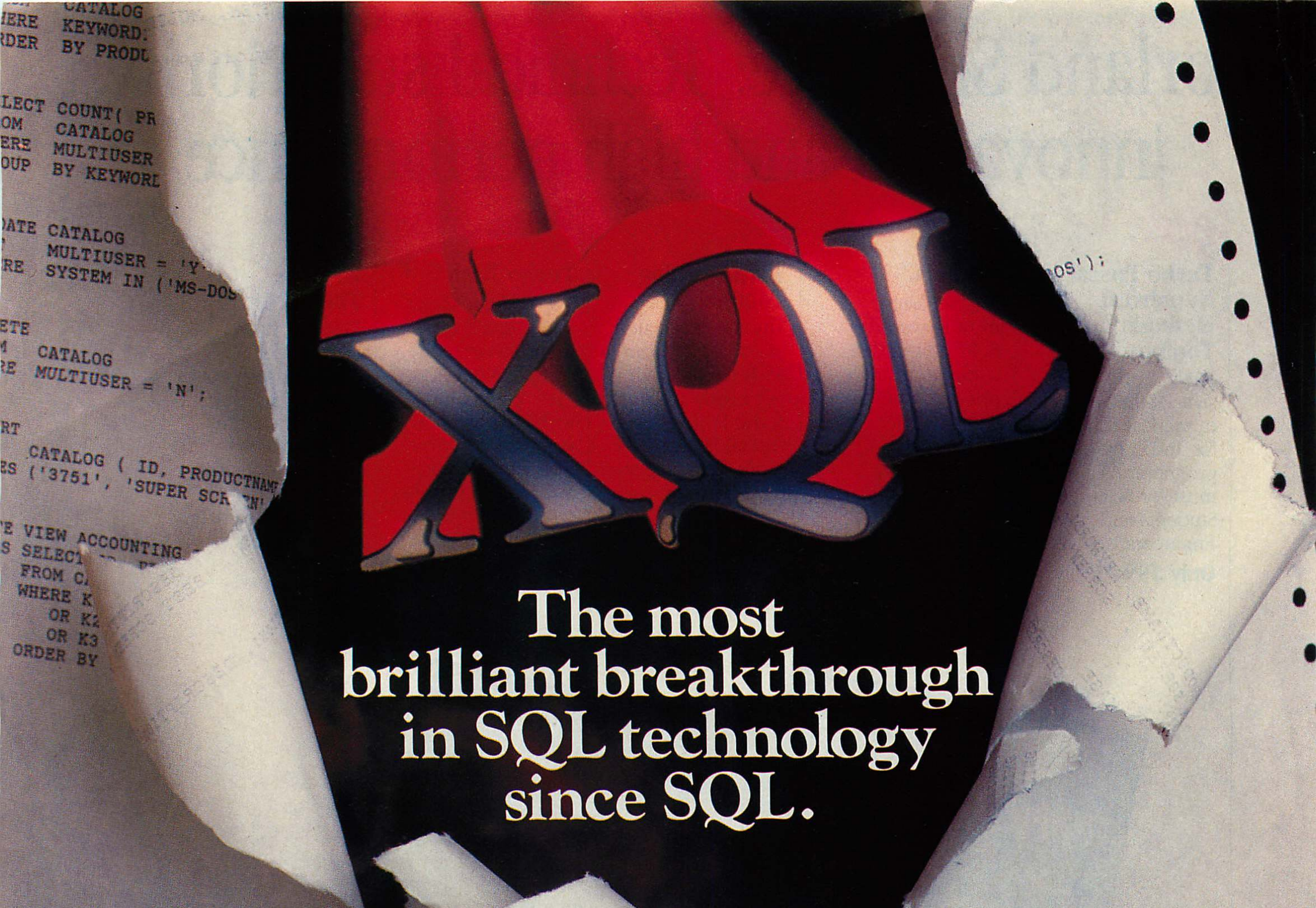

The most brilliant breakthrough in SQL technology since SQL.

XQL is a dramatic step forward in the history of SQL. It's the one unique SQL solution that helps programmers break through to even higher levels of productivity. Powerful yet easy to use, XQL minimizes your coding time and lets you focus on building better applications.

XQL extends the power of Btrieve, SoftCraft's high-performance file manager, by allowing access to multiple records at a time. It frees your application from physical file characteristics by providing true relational capabilities with data independence, data descriptions, data integrity and security.

XQL's three interface levels are a major advance in SQL technology. The first two levels, XQL primitives for maximum efficiency or full SQL statements for maximum convenience, are callable subroutines from BASIC, Pascal and C. The third level lets you enter SQL statements interactively without ever having to write a program.

XQL's extensive DBMS features let you access data by name. Field order is independent of physical location within the Btrieve record. Only records that pass your restrictions are returned—in the sort order you specify. Fields can be computed from other fields or constants. And you can manipulate composite records built from multiple, joined Btrieve files.

XQL offers all the performance and reliability you've come to expect from Btrieve, including LAN support, fault tolerance, comprehensive documentation and expert technical support for trouble-free software development.

Plus, you never pay royalties on your XQL applications.

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XQL, $595; Btrieve, $245; multiuser Btrieve, $595. XQL requires Btrieve and PC-DOS or MS-DOS 2.X or 3.X. XQL is a trademark and Btrieve is a registered trademark of SoftCraft, Inc.

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JULY 1987

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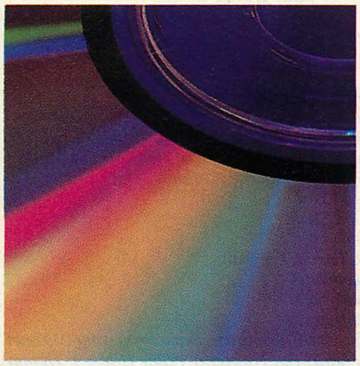

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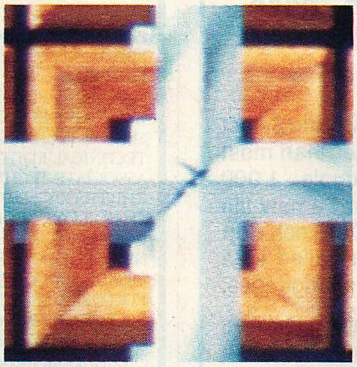
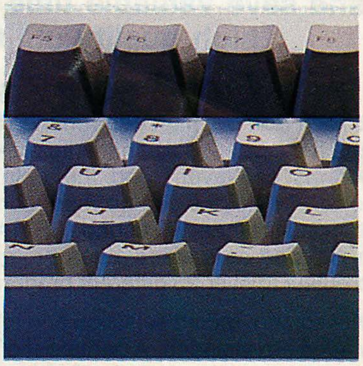


Database Design Techniques 112



Keying on a Standard 134

Cover photograph · Marc David Cohen

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INTRODUCING

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Quickly and thoroughly debug your software with this new real-time hardware breakpoint debugger. You'll be amazed at how easily you track down the most elusive bugs!

A new generation of debugging is here! Nowhere else can you invest less than $1000 and get the power of the new Periscope III board's hardware breakpoints and real-time trace buffer! The same board works on both PC- and AT-class machines, so you don't have to buy two boards just because you have two computer systems.

Now almost anyone doing serious software development can afford the most powerful debugging tool available short of a $10,000 in-circuit emulator!

Imagine the competitive edge this gives you when you're developing commercial software. Think of the time you'll have to devote to new development instead of debugging current software.

Make real-time software solid. You can track down bugs in time-sensitive systems that can only be found when you're running your program at full speed.

Save lots of debugging time. You'll find those uninitialized pointers, intermittent errors, and other subtle bugs that would take too long to find with a software-only debugger.

Optimize your code. Using the bus cycle information saved in the real-time trace buffer and Periscope's high-resolution timer, you can find and eliminate the bottlenecks in your code.

Explore your system. When you need to understand what's going on in your system, you can examine it thoroughly with Periscope III.

Features to whet your appetite. Periscope III is the most comprehensive, flexible, and easy-to-use product of its kind! Here are just a few of its features:

The new Periscope III board is extremely powerful, yet easy to use. Debug your program at full speed with its hardware breakpoints, then examine what's happened in its large real-time trace buffer. You don't have to worry about zapping Periscope's code, because it's in write-protected RAM!

- Set hardware breakpoints on up to 16 ranges of memory and I/O ports
- Qualify breakpoints with data values and a real-time pass counter
- Don't worry about zapping the Periscope software—the 64K of write-protected RAM protects it from runaway programs
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- Display the real-time trace buffer in any of three formats; position the trigger event at the top, center, or bottom of the buffer

Protect your investment. Order Periscope with confidence because it's a proven product—it does its job and does it well. Periscope's been on the market for over two years and it keeps getting better. The only debugger ever chosen Product of the Month by PC Tech Journal, Periscope is used daily by thousands of developers who depend on its flexibility and robustness.

Under our 30-day money-back guarantee, you get your money back if Periscope doesn't perform to your liking. There's a full one-year warranty on the hardware.

You get technical support and your first software update free of charge. We notify you of subsequent updates for which there's a nominal charge, currently $20.

Once you learn Periscope's commands, you can easily use any model. Only when extra commands are needed to deal with model-specific hardware (there are an additional dozen commands in Periscope III) are there any differences.

You can always trade up to another model of Periscope for the difference in price plus a small fee, currently $10. With the release of Periscope III, there's a model that fits virtually every developer's needs and budget.

Can you afford not to try Periscope?

Ask current users about Periscope's price/performance. They tell us that Periscope pays for itself in a matter of hours, and that they can't live without it!

Periscope III includes a board with 64K of protected program memory, hardware breakpoints, & a real-time trace buffer; a break-out switch; software; a 200-page manual; & a quick-reference card, all for $995 (8 MHz) or $1095 (10 MHz).

Note: Periscope III works on the IBM PC, XT, & AT, the Compaq 286, and other 100% compatible machines. Please call to confirm compatibility with your machine.

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Periscope I (Board & Switch)	**$345**
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CIRCLE NO. 215 ON READER SERVICE CARD

Introducing the Hercules InColor Card.

It runs more software at a higher resolution than any other color graphics card.

The Hercules® InColor™ Card offers everything you'd expect from a high resolution color graphics card from Hercules — and more.

Compatibility: The InColor Card is compatible with the thousands of programs that run on our monochrome cards.

Color: The InColor Card gives color capability to Hercules-compatible software like 1-2-3® and AutoCAD®.

Resolution: The InColor Card's resolution of 720x348 is the highest of any widely supported standard.

RamFont: The InColor Card has our unique RamFont mode — in color.

Better graphics.

Hercules is known for bringing high resolution monochrome text and graphics to programs like 1-2-3® and AutoCAD®.

Now the InColor Card gives you the same high resolution 720x348 graphics in up to 16 colors using an IBM® Enhanced Color Display, multi-sync monitor, or equivalent.

That's the highest resolution of any widely supported graphics standard.

And no other color graphics card allows you to move back and forth between color and monochrome systems *without changing drivers.*

Runs more software.

All Hercules-compatible text, graphics and RamFont software runs on the InColor Card in black and white, or at least two colors.

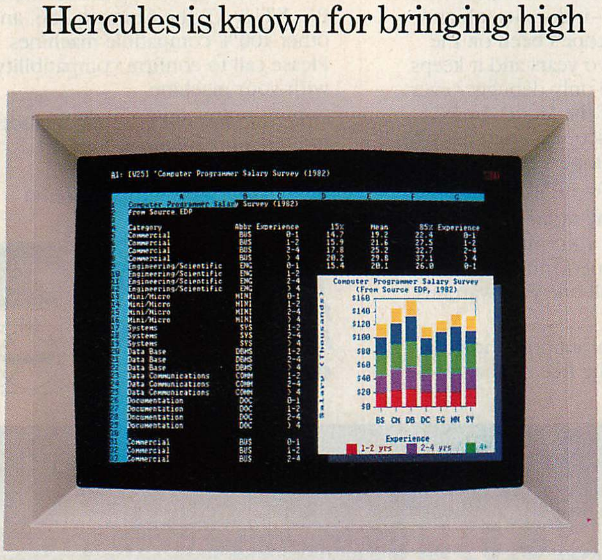
And many popular programs like 1-2-3, Symphony®, AutoCAD and Microsoft® Windows that use graphics or RamFont, run in full color.

More powerful RamFont.

RamFont is a new mode developed by Hercules that gives your software the ability to display multiple fonts at lightning fast speeds.

RamFont transforms advanced word processors like Microsoft Word from slow to text-mode fast.

Technical word processors like Lotus Manuscript™ use RamFont



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A1: [W25] 'Computer Programmer Salary Survey (1982)

             A                      B      C          D         E         F     G
 1  Computer Programmer Salary Survey (1982)
 2  From Source EDP
 3
 4  Category                   Abbr Experience       15%      Mean       85% Experience
 5  Commercial                  BUS        0-1      14.7      19.2      22.4      0-1
 6  Commercial                  BUS        1-2      15.9      21.6      27.5      1-2
 7  Commercial                  BUS        2-4      17.8      25.2      32.7      2-4
 8  Commercial                  BUS        > 4      20.2      29.8      37.1      > 4
 9  Engineering/Scientific      ENG        0-1      15.4      20.1      26.0      0-1
10  Engineering/Scientific      ENG        1-2
11  Engineering/Scientific      ENG        2-4
12  Engineering/Scientific      ENG        > 4
13  Mini/Micro                  MINI       0-1
14  Mini/Micro                  MINI       1-2
15  Mini/Micro                  MINI       2-4
16  Mini/Micro                  MINI       > 4
17  Systems                     SYS        1-2
18  Systems                     SYS        2-4
19  Systems                     SYS        > 4
20  Data Base                   DBMS       1-2
21  Data Base                   DBMS       2-4
22  Data Base                   DBMS       > 4
23  Data Communications         COMM       1-2
24  Data Communications         COMM       2-4
25  Data Communications         COMM       > 4
26  Documentation               DOC        0-1
27  Documentation               DOC        1-2
28  Documentation               DOC        2-4
29  Documentation               DOC        > 4
30
31  Commercial                  BUS        0-1
32  Commercial                  BUS        1-2
33  Commercial                  BUS        2-4
```

The InColor Card's RamFont mode gives Lotus 1-2-3 a pop-up graphics window and lets you view nearly twice as much spreadsheet data—all in full color.

to display onscreen the text you want to print.

Even 1-2-3 uses RamFont to almost double the size of the spreadsheet picture.

And now, with the InColor Card, you get an enhanced RamFont with 3,072 programmable characters in up to 16 colors.

All the way up to 12,288 characters in four colors.

With the InColor Card's RamFont, no program should run out of speed, color or fonts ever again.

What the InColor Card could mean to your company.

The InColor Card allows you to run a program in color, and then move to a Hercules Graphics Card Plus and run the same program in monochrome.

Without changing drivers.

Compatibility between the InColor Card and our monochrome card allows you to network around one standard—Hercules. At last your PCs will have compatible graphics, in color or monochrome.

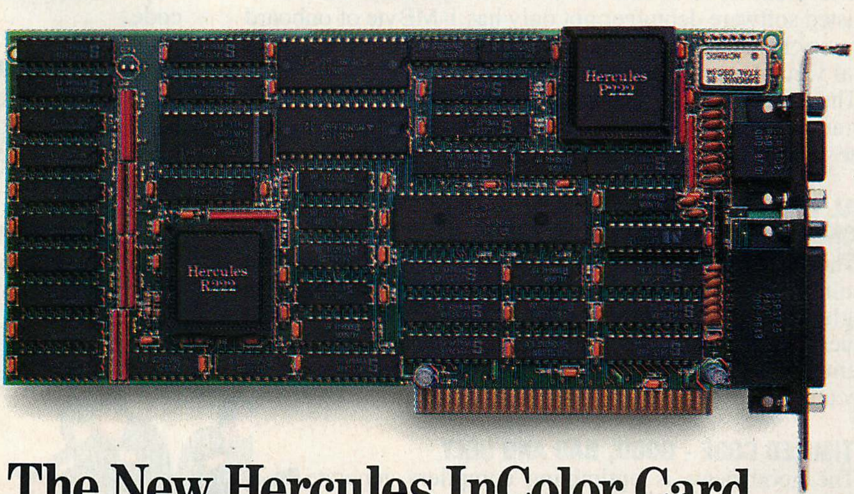
Remember, only the InColor Card has color-to-monochrome compatibility, high resolution text and graphics, and the power of color RamFont.

Call 1-800-532-0600, or 1-800-323-0601 in Canada, Ext. 511 to find out more on how the Hercules InColor Card can improve your software.

AutoCAD gets the same high resolution 720x348 graphics as our famous monochrome cards—only now in full color on an IBM Enhanced Color Display.

Features of the Hercules InColor Card

- Hi-res text with 9x14 character size in up to 16 colors with attributes
- 720x348 Hercules graphics in 16 colors selected from 64 color palette
- Special RamFont mode displays 3,072 programmable characters in 16 colors with attributes, up to 12,288 characters in 4 colors
- Runs Hercules-compatible graphics software in b&w or any two background colors
- Designed for use with the IBM Enhanced Color Display, multisync monitors, or equivalents
- Software diskette includes font editor, sample fonts, and Hercules utilities
- Parallel printer port
- Two year warranty



The New Hercules InColor Card.

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CIRCLE NO. 242 ON READER SERVICE CARD

WHO YA GONNA CALL? BUGBUSTERS!

This is how PROBE displays real-time trace data. Trace information includes C source code, assembly language and data which was read or written during instruction execution. PROBE software simplifies the display by tossing out prefetched but unexecuted instructions.

PROBE knows all about your local and complex variables. You can display and change an array of structures as easily as shown in this display.

PROBE's menu window means you do not have to look up debug commands in the manual. Entering the command name shows you command syntax.

```
         OP                        -- (<enter> for next page)
   ADDR  CODE   OPERAND(S)         -- (Any other key to exit trace)
 ------------------------------
 69.          (*Ptr). Worker [1]. IQ = 199;
  0A175  MOV    BX,WORD PTR [BP+FFFE]
  0AF82     READ     - 09C2
  0A178  MOV    BYTE PTR [BX+001A],C7
  0AF7C     WRITE    -   C7

 70.          (*Ptr). Worker [1]. Salary = 100000;
  0A17C  MOV    BX,WORD PTR [BP+FFFE]
  0AF82     READ     - 09C2
 ----------------------------------------------------------------
[.PTR].WORKER[1].NAME          = 0036
0A5A:0036   48 65 6E 72 79 00 00 03-FF FF FE 09 22 0A 5A 0A  *Henry...  ■.".Z.*
[.PTR].WORKER[1].AGE           = BD01
[.PTR].WORKER[1].SALARY        = 000186A0
[.PTR].WORKER[1].IQ            = C7
[.PTR].WORKER[1].NEXTOFKIN     = 0011
[.PTR].WORKER[1].EYECOLOR      = BROWN

_
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FLAg  FLOat Go IF   INIt    INTerpt LIst   LOAd LOOp MAcro MEnu MODule MOVe MORe
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```

> ***"Real-time source-level debugging of very large programs simply can't be done without Atron's AT PROBE."*** *Ed Oates, Director of PC Software Development, Oracle Corporation*

The good news with your new Microsoft 4.0 or Lattice* C compilers is that they're providing more symbolic debugging information than ever. The bad news is you can't fit your program, a software debugger and that monster symbol table into memory - at least at the same time.

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WILL FASTIE

Neural Overload

You're going to need more memory anyway; you might as well start collecting it now.

I got into an interesting frame of mind the other day, thinking about how I used my PC in its pre-hard-disk days.

Somehow I managed to run everything in 256KB, allocating the remaining 384KB to a RAM disk—my first drive C:. I had this down to a science; my two-diskette boot procedure got DOS running and then copied whatever was on drive B: directly to the RAM disk using Tall Tree System's JET program. This was all in a batch file, of course.

I also had a complete set of batch files for unloading C: or putting a different set of programs on it. The type of process determined whether programs or data files lived on C: and therefore whether unloading the RAM disk simply meant deleting the current contents and overwriting or updating a diskette with new files. Thus, I ran the word processor from C: and sometimes could even keep the documents there, too. By contrast, loading the C compiler passes from diskette turned out to be faster when reading and writing source and temporary files in RAM.

It took some time to develop a consistent, organized strategy for handling a diskette-sized RAM disk. My hard disk, on the other hand, was a model of simplicity. Having both programs and data so readily available without having to swap diskettes was a boon. I quickly forgot all about RAM disks.

Of course, forgetting about RAM disks was not hard to do. With the advent of hard disks came programs that actually needed more than 256KB, sometimes approaching even 640KB. With all of main memory gone, not much room was left for RAM disks. They were no longer an option.

A few companies, most notably Tall Tree, offered expanded memory products that allowed RAM disks that were megabytes in size, and a few companies offered less general-purpose RAM configured as a mass-storage device. This allowed those who truly needed RAM-disk performance (software developers, for example) to get it.

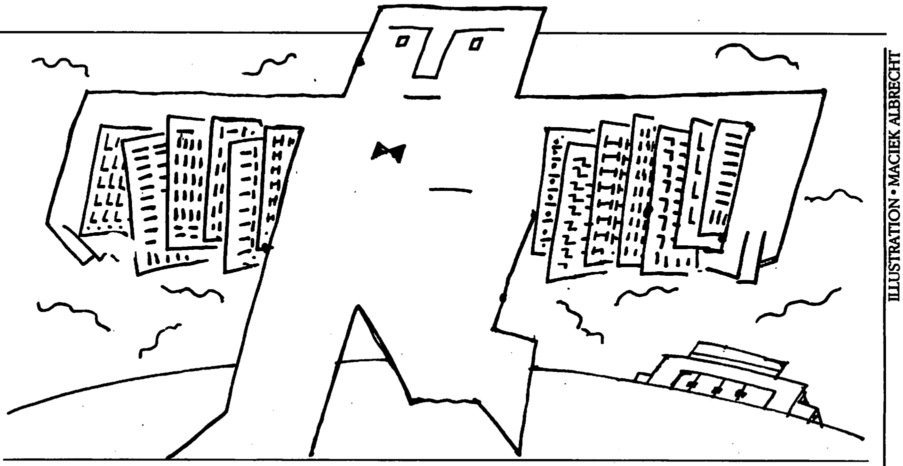

ILLUSTRATION • MACIEK ALBRECHT

However, not until the emergence of the Lotus/Intel/Microsoft Expanded Memory Specification (EMS) and its cousin, the AST/Quadram/Ashton-Tate Enhanced EMS (EEMS), did a basic method of providing more than 640KB of memory become standardized. With multiple vendors supplying boards meeting the specification for either EMS or the superset EEMS, software developers could enhance their programs to exploit additional memory resources.

While many users have found the extra memory necessary for large spreadsheets under Lotus 1-2-3 or faster compile times with C, I would wager that most expanded memory boards have been used to fill out the bottom 640KB when the machine comes with 512KB or less; the rest of the memory goes begging. With the new generation of machines coming standard with 640KB or 1MB, more memory may not seem necessary at all.

HOGGING MEMORY

Don't believe it. There are good reasons to start buying memory now so that you will have a suitable collection for the future.

Because the EMS provides a de facto standard for the industry, software developers can shoot for the moon, and many already have. Lotus, not surprisingly, was one of the first, adding expanded memory support in release 2 of 1-2-3. The EMS lets the data grow beyond the 640KB limit with a barely noticeable performance hit. Lotus is not the only software provider that has revised its product to expanded the data storage capacity. It is a quick way for vendors to enhance their products.

WordPerfect Corporation, for example, has exploited the memory for different reasons. WordPerfect and PlanPerfect (WP's spreadsheet program) never had a data limitation to begin with because the programs virtualize data to the disk. However, WP ships a product called the Library, which includes SHELL, a context-switching manager. SHELL uses EMS to allow more programs to be in memory at the same time; it swaps even non-WordPerfect Corporation programs between main and expanded memory.

Microsoft Windows version 2.0 exploits EMS, EEMS, or IBM's XMA (Expanded Memory Adapter) by allowing each program running under Windows to have slightly more memory, a differing amount depending on the type of board (up to 128KB more with EEMS). The Windows strategy allows both data *and code* in the extra memory. Even though Windows uses swapping, it is highly desirable to avoid swapping as long as possible by getting more programs in main memory. Of course, additional EMS memory or standard 80286 extended memory can be used as a RAM disk for swapping. These solutions are still not terribly fast, but they are better than swapping to hard disk.

Other programs, such as Living Videotext's Ready!, are terminate-and-stay-resident programs that are almost entirely resident in EMS and even execute there. Imagine loading a program 10 times bigger than Borland's SideKick but having it live entirely outside the base memory. Executing in EMS is not very simple, however, so only a few products are in this category.

Even now, applications and environments are demanding greater quantities of memory. *PC Tech Journal*'s technical editors have machines with about 4MB of EMS or EEMS memory; this is the only way to be sure that a software product under evaluation can be operated to its full extent. In some cases (expert systems, for example), even more memory is required; GoldWorks, an expert system building tool from Gold Hill Computers, Inc., wants 5MB of standard, extended memory.

When products like these are in use, the amount of memory can still be limited. Looking ahead just a bit reveals that memory systems of 4MB or so are going to be very important.

DISK CACHING

IBM, of course, opened the floodgates when it decided to make disk-caching software a standard component of every Personal System/2 machine. IBM based its competitive performance analysis of the PS/2 line on machines operating with the cache. Compaq quickly responded with caching software for its 80386 and 80286 machines because, obviously, it did not want its machines to appear slow in comparison to IBM. You can expect every vendor of desktop systems, even Apple, to respond in kind.

Disk caching is a technique of using *memory* to hold often-used portions of disk files to improve disk access times. Memory is needed to achieve this performance improvement and, usually, more is better. In our own tests of the PS/2 family and of other machines with caching, *PC Tech Journal* used a 256KB cache. IBM-supplied PS/2 software supports up to 512KB of cache.

If the performance comes only with cache, everyone is sure to want it, and that means more memory. If I were a memory board manufacturer, I would be jumping for joy and building cache software to go along with every XT or AT board that I sold.

MEMORY FOR OS/2

The memory requirement for cache pales in comparison to the amount required for IBM's newly announced Operating System/2.

OS/2 Standard Edition requires, at minimum, 1.5MB of RAM. This estimate includes the operating system, the Presentation Manager, and room for a reasonable mix of applications. Even so, it is about three times more than DOS plus Windows requires today.

But wait! There's more! OS/2 Standard Edition requires 2MB in order to use the compatibility box. I assume that many people will, indeed, wish to take advantage of this facility, so 2MB is probably the bottom line.

But wait! OS/2 Extended Edition requires 3MB! Presumably, the additional megabyte is for the data management and communications facilities that are built into that version of OS/2. Assuming some of us do not opt for IBM's solution to these problem areas, other vendors will surely offer substitutes requiring similar quantities of RAM.

Do you think you are through at 3MB? Not quite. If you still need EMS (there is reason to think, even in an extended memory environment, that EMS provides some useful function), that adds to the total. And how about cache? Oh, and RAM disks are always faster than hard disks and, therefore, very useful for many of us. 4MB? 5MB? More?

This is just for computers sitting on our desks. Local area network servers or other dedicated machines will want loads of memory, too. Servers on 80286-based machines with 3MB are not unheard of today, so we can expect much larger ones to come.

COLLECT THEM ALL

A friend of mine recently expanded his home PC to include a hard disk. He also needed to upgrade his memory from 256KB and asked me to suggest solutions to both problems. For memory, I suggested an EMS board with 512KB; although this was more than he needed, it filled out the first 640KB and left a bit for use as general expanded memory. The board, however, still has sockets for another 1MB. Even at the 512KB level, convincing my friend of the long-term benefit of this strategy was not easy, especially as other, less expensive memory solutions were staring at him in the same mail-order ad.

Buying large memory systems today may seem extravagant. Whether or not the requirement exists today, it is certainly the case that vast amounts of memory are going to be required for the software applications of tomorrow. Memory-eating data management applications are on the rise at a very rapid pace, and more and more machines are getting networked, another memory consumer. Integrated environments, such as WP's SHELL program, Quarterdeck Office Systems' DESQview, The Software Link's MultiLink Advanced, and Microsoft Windows, are becoming more popular, especially in light of IBM's acceptance of Windows as the OS/2 Presentation Manager.

In short, you just can't have too much memory on hand.

COMING UP: PS/2

PC Tech Journal does not usually speculate about forthcoming issues, but next month's magazine is an especially exciting one for us.

The bulk of the August issue will be devoted to IBM's Personal System/2 family of computers. Besides offering commentary on the new family, we will provide our standard, in-depth reviews of the Models 30, 50, and 60. We will do our best with the Model 80, although they are as scarce as Japanese laptops at the moment.

We will have articles on IBM's new bus, the Micro Channel, as well as the Video Graphics Array (VGA). We will tell you all we can about IBM's new LAN products, and we will overview the 3270 announcements, a somewhat overlooked but extremely important aspect of IBM's recent announcements. IBM DOS 3.3 will be reviewed, and we will provide the facts and figures about performance measurement using disk caching.

Most of the articles are being written by members of *PC Tech Journal*'s technical staff. We have really been working hard to get this issue to you as quickly as possible without sacrificing our usual depth and accuracy, so we all hope you find our August issue both interesting and informative.

We've certainly had a lot of fun getting it ready for you.

—*WF*

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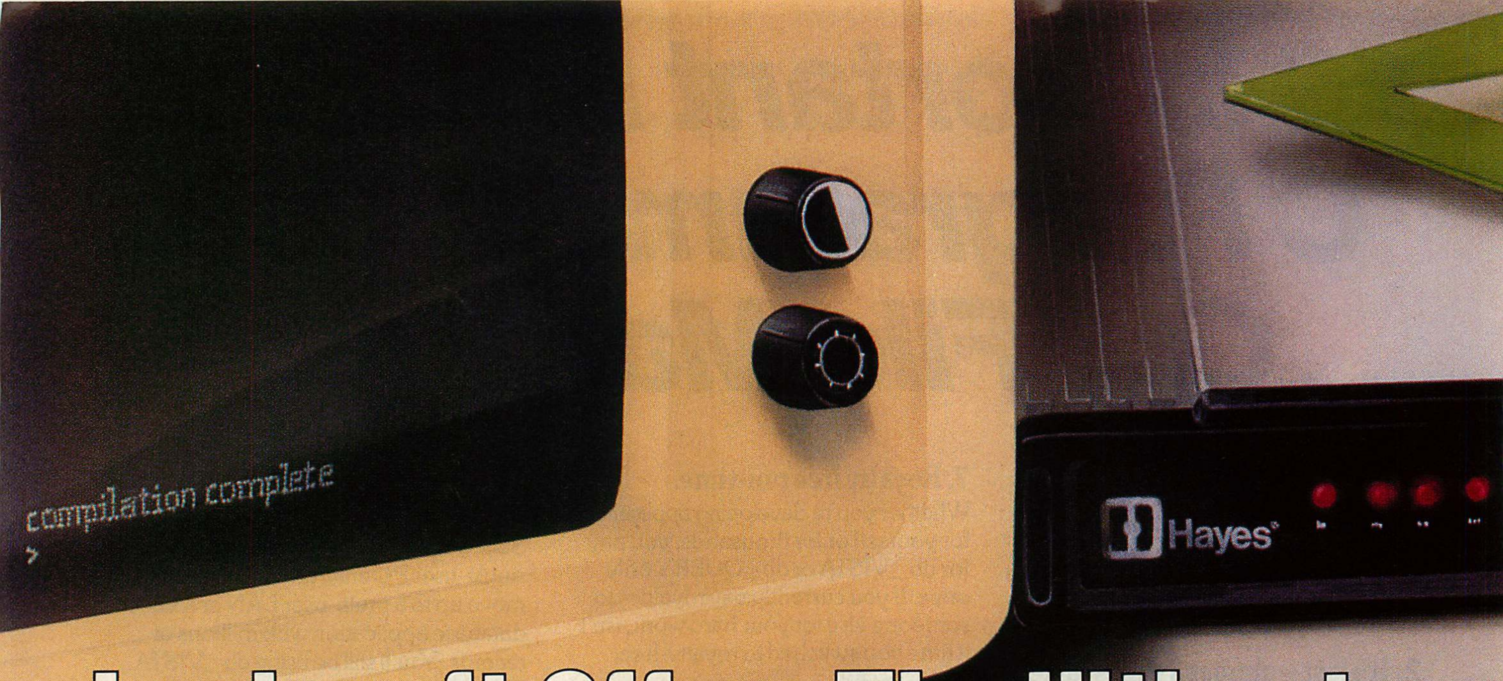

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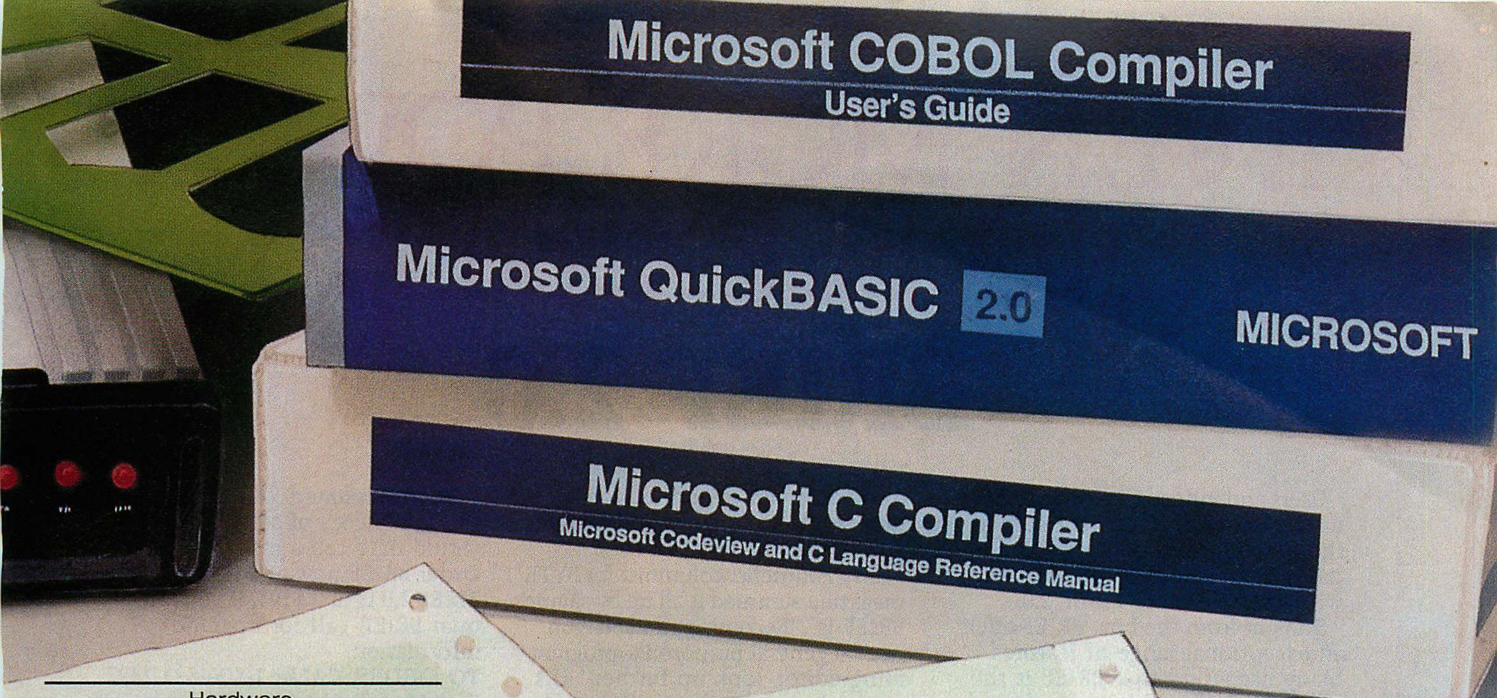

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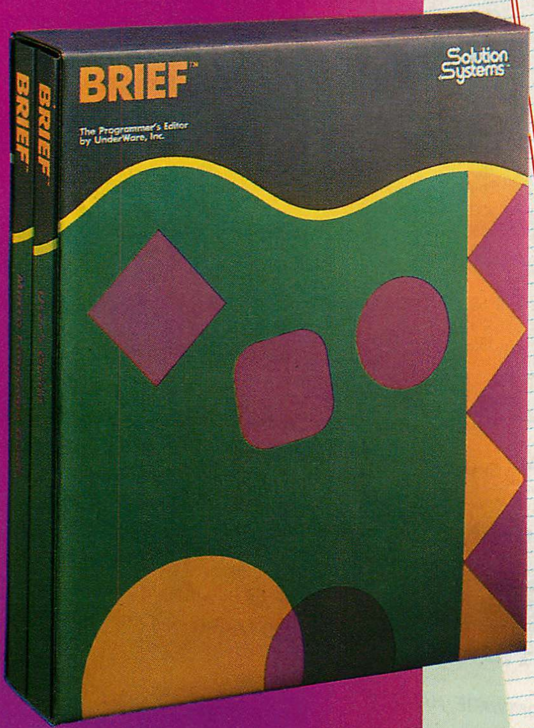

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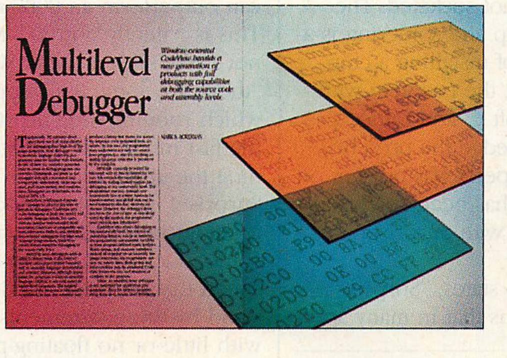

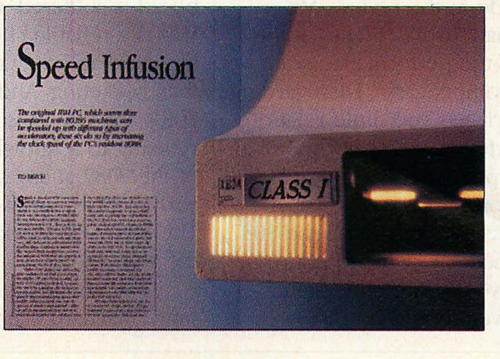

DECODING CODE

The article "Multilevel Debugger" (Mark S. Ackerman, March 1987, p. 90) was seriously marred by a confusion among the concepts of "assembler," "machine," and "object" code.

Assembly language, assembler code, and so on are generic terms referring to languages with certain characteristics. These are machine-oriented languages that allow symbolic references not only to the opcodes of instructions, but also to their operands. They commonly include not only statements for generating constants and individual instructions, but also some sort of macroinstruction facility.

Object code, the output of a language translator (compiler) is not normally assembly language. In many compilers that can generate assembler code, the object code is difficult to read (full of nonsymbolic offsets), and does not resemble an assembly language program written by a human being. In the case of an assembler, object code is normally machine code, along with control information, in a format determined by the software (both the compiler and the linker).

Machine code is the actual code that is executed by the compiler. Its characteristics are determined by the computer architecture.

The "assembly language listing" produced by many compilers is really machine language in disguise. Although some compilers (for example, IBM's PL/1 Optimizing Compiler) can produce excellent object listings, this is an exception, especially in the microcomputer world. The majority of PC compilers might as well have thrown away their symbol tables when they produce object-code listings. These listings are normally full of calculated offsets instead of variable names.

Rumors to the contrary notwithstanding, DEBUG is not appropriate for programs written in assembly language. Even though the software exists to retain the symbol table in the object code, DEBUG is not able to read the symbol table. In fact, DEBUG is a machine-level debugging tool. In addition, it does not allow the assembler programmer to do source-level debugging.

SYMDEB is not much better. Its symbol-table support is limited to those symbols declared GLOBAL. I hope that CodeView offers source-level debugging for the assembler programmer, but use of the term "assembly level" for commands that clearly are not assembly level leads me to doubt it.

Several features should be available in any software that is billed as a source-level debugger. If I am patching a C program, I want to patch it in C, not in object code. I already have text editors to search my source code: a regular-expression search of storage would be much more useful than the same search of the source file.

Finally, why was no mention made of CodeView's unfortunate limitations?

Seymour J. Metz
Annandale, VA

*Admittedly, the terms "assembly" and "object" have been used when "machine code" might have been more appropriate. However, as the article shows, CodeView's assembly language listing is not machine language in disguise. In photo 2 (on page 92 of the CodeView article), the line **p_space = NULL** is shown translated to **MOV p_space,0000**. To the left of this translation is the machine code **BE0000**, which translates to a nonsymbolic **MOV SI,0**. In the photo, only the reference to **&buf[0]** is shown nonsymbolically. (Incidentally, references to structure members also are not symbolic.)*

On another point, DEBUG and SYMDEB can be quite suitable for debugging assembly language programs. Virtually all assemblers generate listings that include machine code. No real change is made in the abstraction the programmer sees: instructions, registers, flags, and memory locations.

CodeView does lack some useful amenities such as source code patching. An interpreter or incremental compiler should undoubtedly provide them, but CodeView is a debugger, not a programming environment. The 640KB limitation of DOS also comes into play when considering what features to add; the 200KB size of the current product already precludes debugging large programs. Finally, the limitations of CodeView were mentioned throughout the article and they were summarized in the next-to-last paragraph.

—DM

SURPRISING RESULTS

After reading your review of PC accelerators boards ("Speed Infusion, Part 1," Ted Mirecki, February 1987, p. 126), I felt it important to correct some misconceptions about our company's Surprise! accelerator board.

Surprise! works in a totally unique way to accelerate the PC. First, the bus speed is increased not by running the bus at a higher speed, but by eliminating the fourth state of the processor bus cycle. This is why BUSPERF gives a reading of 32-percent speed improvement. Second, the wait states added to the Surprise! board's 9.54-MHz processor allows its processor to run at a higher speed for a reason. Running the processor at 9.54 MHz greatly reduces the amount of time the system bus has to wait for the processor on execution-intensive work, such as jumps, calls, pushes, pops, multiplies, divides, and so on. This shows up in the board's excellent performance compared with the other boards when running real applications. Remember, also, that the other boards in this survey achieve their speed by shortening state times, and therefore access times, thus increasing the risk of errors.

I also take issue with some specific statements made in the review. Mr Mirecki says that Surprise! falls "at the bottom end of the performance scale among these competitors." Disregarding BUSPERF, which has very little relationship to the performance of normal programs, the Surprise! performs at least average in a normal PC, as shown in your tables, except when using the 8087 numeric coprocessor (which I address below). Also, we did not understand why the reviewer should find it "strange" that the V20 on the Surprise! board is soldered, not socketed. The V20 is a reliable chip and soldering is a more reliable way of installing a chip than socketing. And, the problem with Lotus 1-2-3, Microsoft C, and Lattice C refusing to acknowledge the presence of the 8087 at any speed was present on early boards, but it has been corrected. The 8087 will work with Surprise! in the slow mode.

The article also states, "Surprisingly, Maynard claims that in many applications. . .a V20 running at 10 MHz can outperform an 8087 running at 5. This is patently untrue." Maynard does not make such a claim. We do state that "there are some 8087 applications in which running the Surprise! by itself in the fast mode will be faster than running the application with the 8087 and Surprise! in the slow mode." We go on to admit in the same document that some functions run with the 8087 "at a speed that Surprise! cannot match." We stand by these statements. Spreadsheets with little or no floating-point arithmetic, trigonometric functions, and logarithmic functions typically will run faster with Surprise! on and the 8087 off. Finally, we would like to point out that the price of the Surprise! board has been reduced to $149.95.

In summary, we were upset by what we feel was an unfair comparative review of our product.

Maynard K. Knapp, president
Maynard Electronics
Casselberry, FL

The Surprise! is indeed unique in the way it approaches accelerating the PC, and it represents a sizable engineering effort. The point I tried to make is that the results are not commensurate with this effort, especially with the high price as compared with the other accelerators. I apologize for stating that Surprise! falls at the bottom end of the performance scale; I meant to indicate that it had the lowest price/performance ratio of those reviewed. Of course, this is changed by the price reduction—which came after the article went to press.

As was plainly stated, BUSPERF was never meant to be a benchmark of real-world performance, but a measuring tool for averaging bus transfer times over a longer time frame than could be measured by a logic analyzer.

I found it strange that the V20 microprocessor on the Surprise! was soldered because, in the vast majority of microcomputers that I have seen, the microprocessor is socketed. As a matter of fact, the very existence of most accelerator boards, Surprise! included, depends on the ability to remove the original microprocessor from the PC.

As far as compatibility with the 8087 goes, the reported results were obtained with a replacement unit that was received after we notified Maynard of problems with the original unit. We could only assume that this second one was the latest version. Subsequent tests with yet another unit have confirmed that an 8087 is used when Surprise! is

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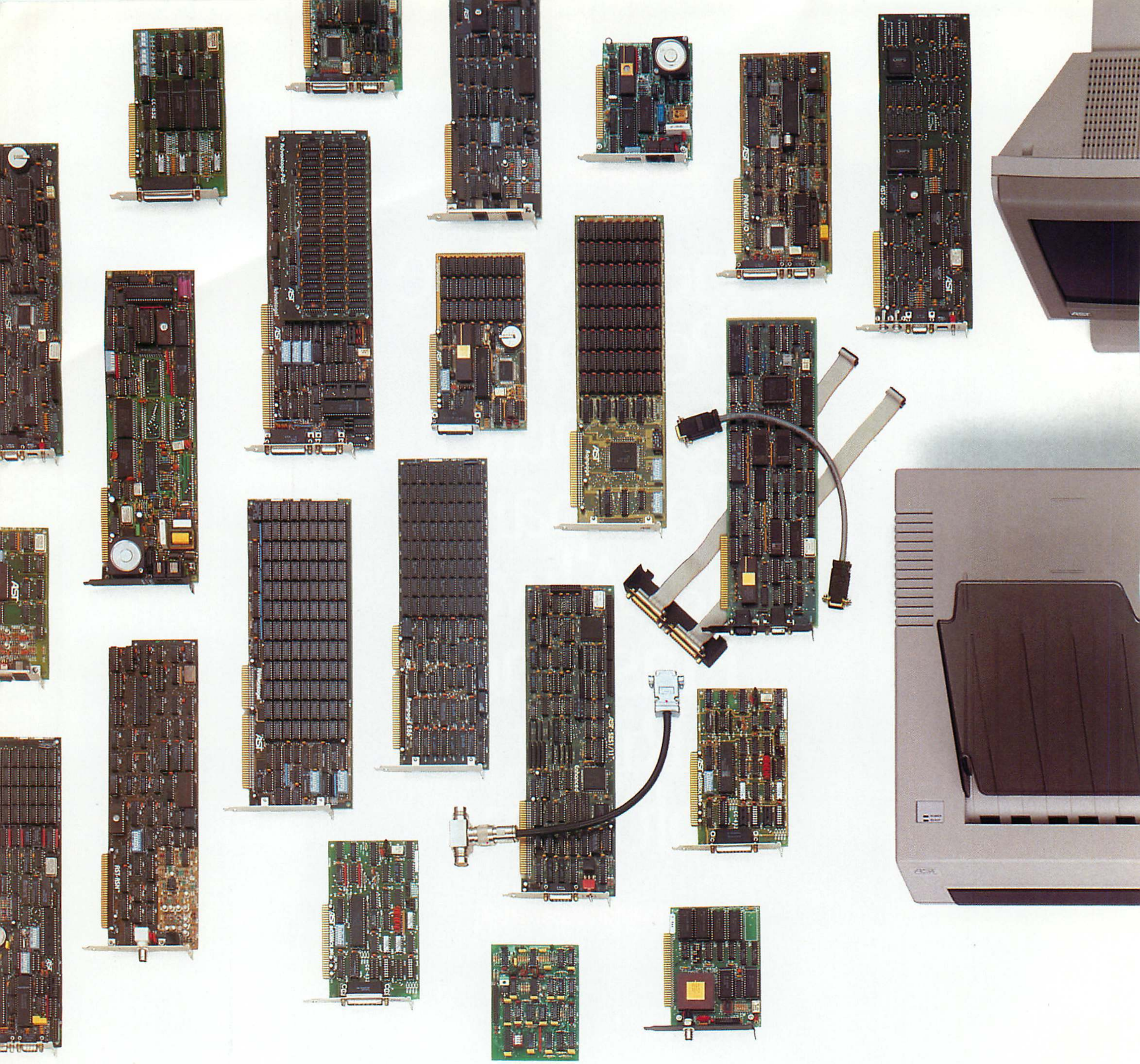

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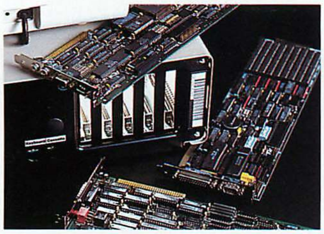

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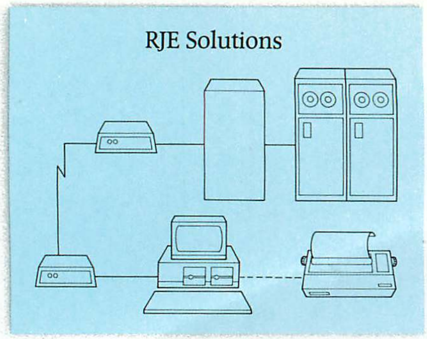

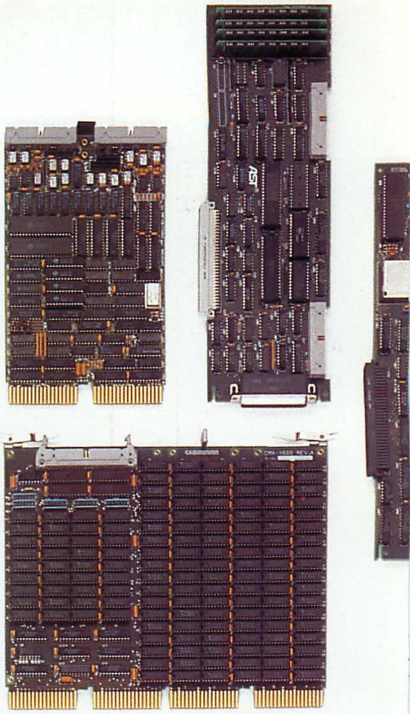

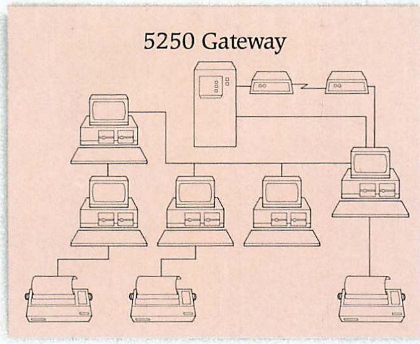

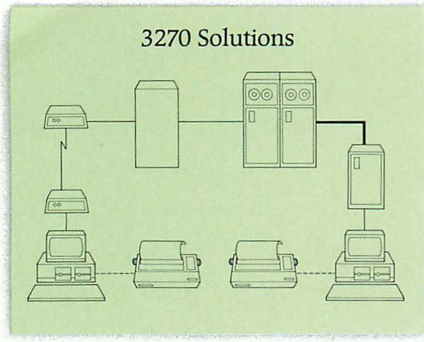

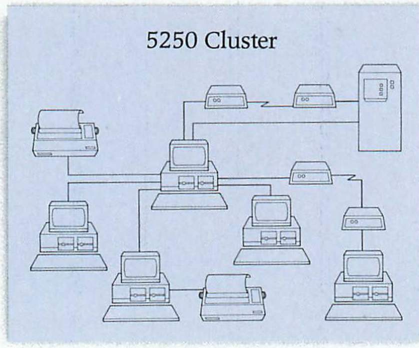

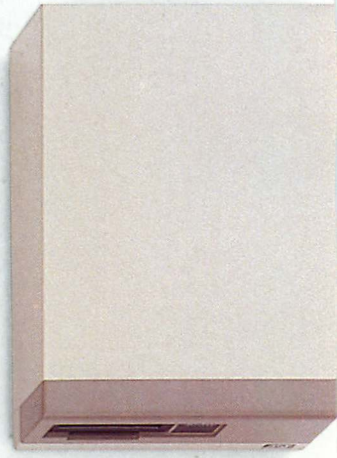

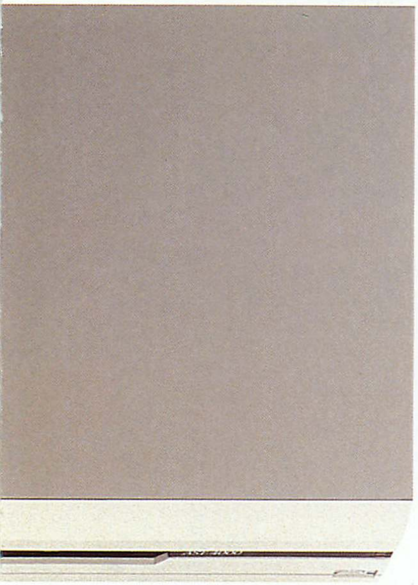

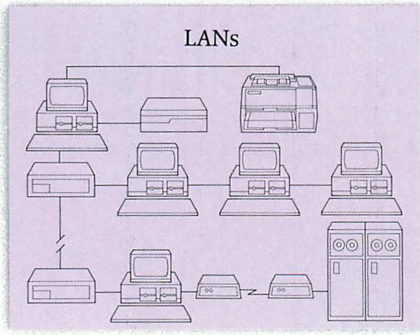

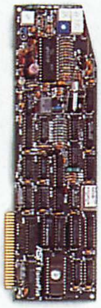

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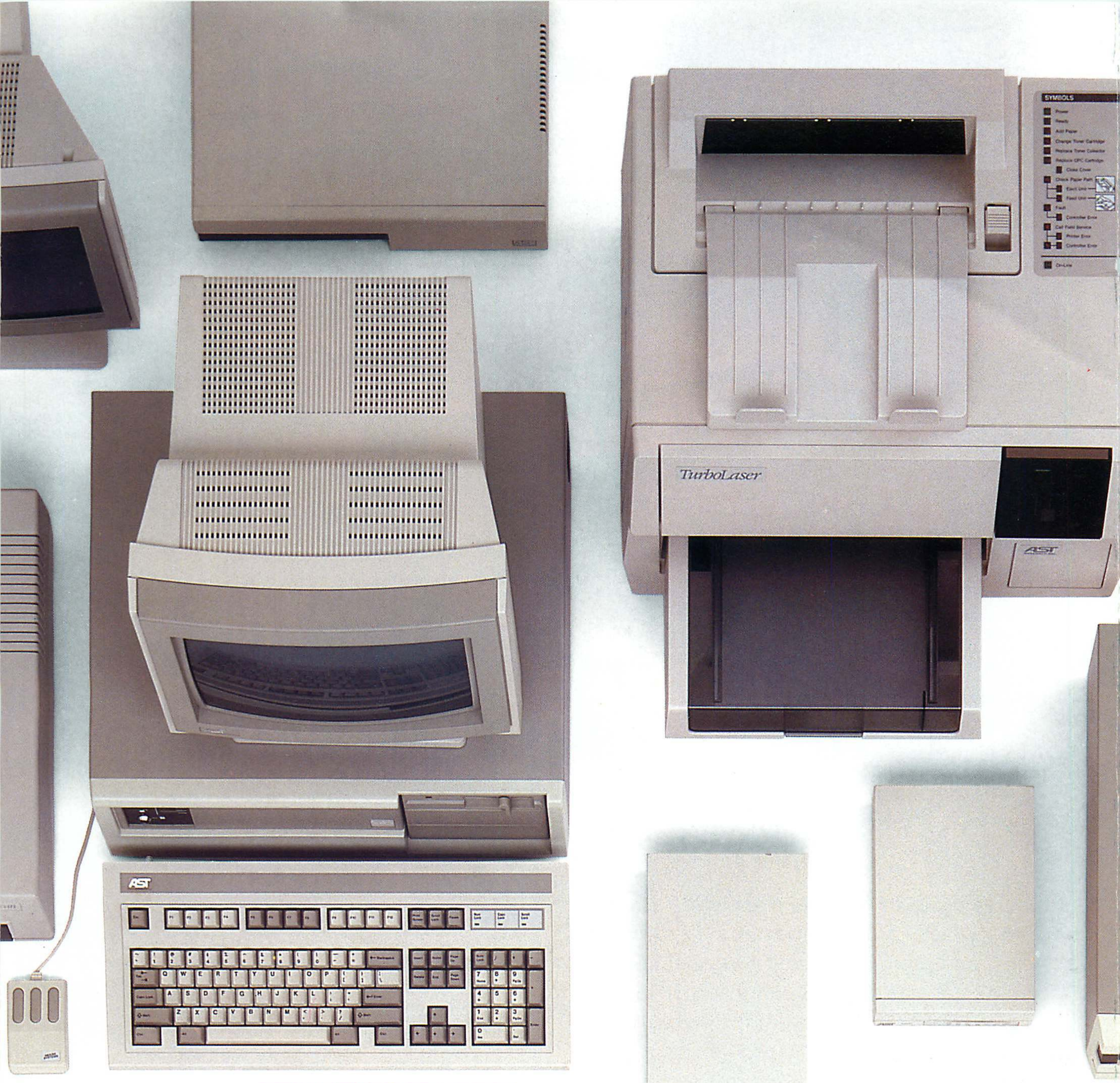

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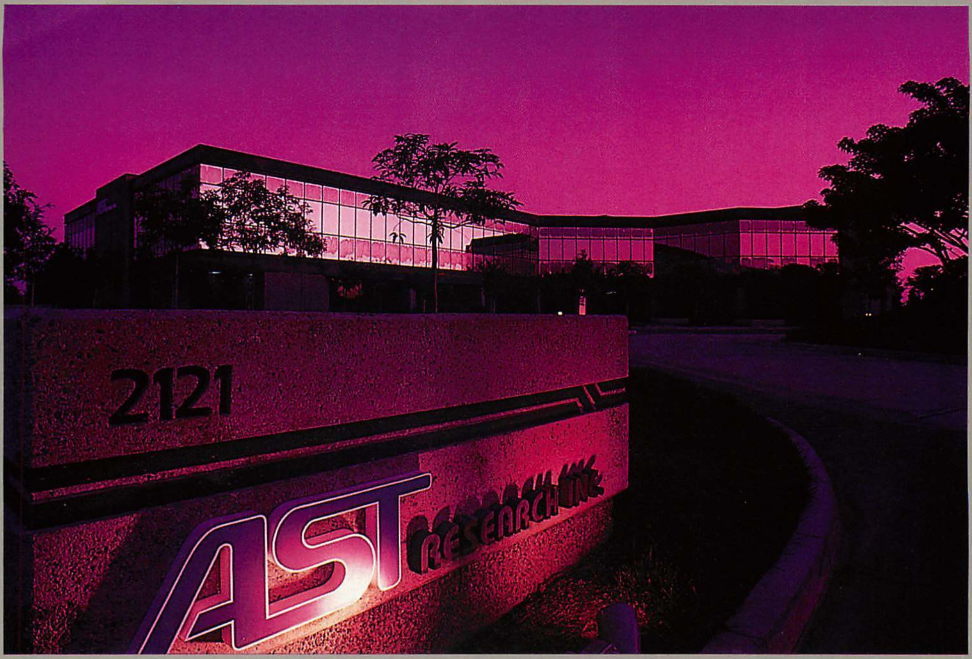

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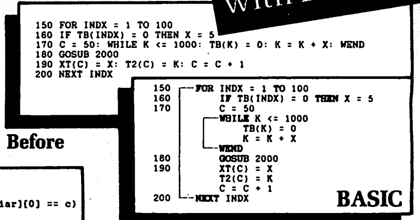


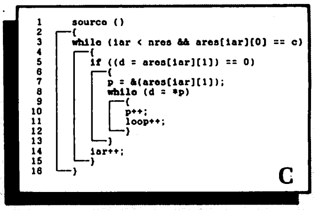
```
150 FOR INDX = 1 TO 100
160 IF TB(INDX) = 0 THEN X = 5
170 C = 50: WHILE K <= 1000: TB(K) = 0: K = K + X: WEND
180 GOSUB 2000
190 XT(C) = X: T2(C) = K: C = C + 1
200 NEXT INDX
```

Before

```
150  ┌──FOR INDX = 1 TO 100
160  │       IF TB(INDX) = 0 THEN X = 5
170  │       C = 50
     │   ┌───WHILE K <= 1000
     │   │        TB(K) = 0
     │   │        K = K + X
     │   └───WEND
180  │       GOSUB 2000
190  │       XT(C) = X
     │       T2(C) = K
     │       C = C + 1
200  └──NEXT INDX
```

BASIC

After



```
      source ()
 ┌────{
 │    while (iar < nres && ares[iar][0] == c)
 │ ┌──────{
 │ │      if ((d = ares[iar][1]) == 0)
 │ │ ┌────────{
 │ │ │        p = &(ares[iar][1]);
 │ │ │        while (d = *p)
 │ │ │ ┌──────────{
 │ │ │ │          p++;
 │ │ │ │          loop++;
 │ │ │ └──────────}
 │ │ └────────}
 │ │      iar++;
 │ └──────}
 └────}
```

C

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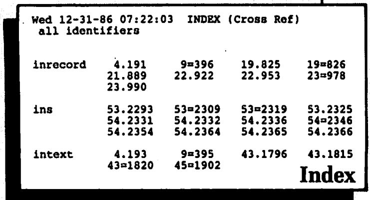

```
Wed 12-31-86 07:22:03  INDEX (Cross Ref)
 all identifiers

inrecord     4.191     9=396     19.825    19=826
            21.889    22.922     22.953    23=978
            23.990

ins         53.2293   53=2309   53=2319   53.2325
            54.2331   54.2332   54.2336   54=2346
            54.2354   54.2364   54.2365   54.2366

intext       4.193     9=395    43.1796   43.1815
            43=1820   45=1902
```

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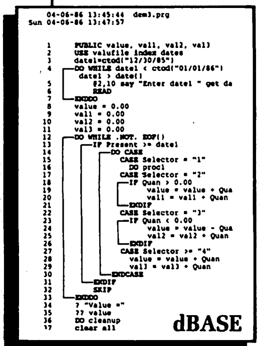

```
    04-06-86 13:45:44  dem3.prg
Sun 04-06-86 13:47:57

      PUBLIC value, val1, val2, val3
      USE valufile index dates
      date1=ctod("12/30/85")
   ┌──DO WHILE date1 < ctod("01/01/86")
   │   date1 > date()
   │     @2,10 say "Enter date1 " get da
   │     READ
   └──ENDDO
      value = 0.00
      val1 = 0.00
      val2 = 0.00
      val3 = 0.00
   ┌──DO WHILE .NOT. EOF()
   │ ┌──IF Present >= date1
   │ │ ┌──DO CASE
   │ │ │     CASE Selector = "1"
   │ │ │       DO proc1
   │ │ │     CASE Selector = "2"
   │ │ │   ┌──IF Quan > 0.00
   │ │ │   │      value = value + Qua
   │ │ │   │      val1 = val1 + Quan
   │ │ │   └──ENDIF
   │ │ │     CASE Selector = "3"
   │ │ │   ┌──IF Quan < 0.00
   │ │ │   │      value = value - Qua
   │ │ │   │      val2 = val2 + Quan
   │ │ │   └──ENDIF
   │ │ │     CASE Selector >= "4"
   │ │ │       value = value + Quan
   │ │ │       val3 = val3 + Quan
   │ │ └──ENDCASE
   │ └──ENDIF
   │     SKIP
   └──ENDDO
      ? "Value ="
      ?? value
      DO cleanup
      clear all
```

dBASE

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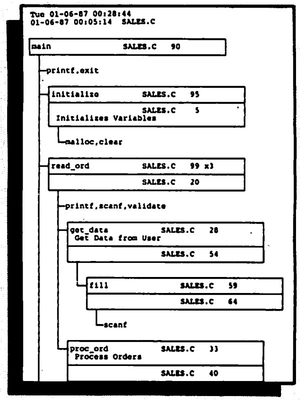

```
Tue 01-06-87 00:28:44
01-06-87 00:05:14  SALES.C

main                    SALES.C   90
  printf,exit
  initialize              SALES.C   95
                          SALES.C    5
   Initializes Variables
    malloc,clear
  read_ord                SALES.C   99 x3
                          SALES.C   20
    printf,scanf,validate
    get_data                SALES.C   28
     Get Data from User
                            SALES.C   54
      fill                    SALES.C   59
                              SALES.C   64
        scanf
    proc_ord                SALES.C   33
     Process Orders
                            SALES.C   40
```

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running in slow mode. In any case, of 27 real-world spreadsheet applications that I tested, 24 ran faster with the 8087 at 5 MHz than with the Surprise! at 10 MHz; thus, I stand by my contention that for this type of application, a slower numeric processor is preferable to a faster general microprocessor. Having Surprise! run with the 8087 at high speed would be a great improvement.

The problems with Surprise! cited in the review were its high price, incompatibility with some DOS utilities such as PRINT ECHO, and an inability to use a 8087. The correction of two of these problems makes the Surprise! a much more desirable product than it was at the time of the review.

—TM

LIBRARY RESOURCES

Your review of dBASE III compilers was very good ("Dialects of dBASE," Ted Mirecki, April 1987, p. 46). I have been using Clipper for some time to develop a multiuser database system that we run on our Alloy PC/Slave system. Earlier versions of Clipper did not support multiuser access and we had a great many problems until I discovered a little library called NETLIB. NETLIB is an add-in library for Clipper, produced by a company called Communications Horizons. It added multiuser functions to Clipper long before Nantucket did and solved my problems admirably.

Even with the new version of Clipper, I still must use NETLIB since Clipper supports only those networks that use the standard DOS calls. Nonstandard networks, such as Multilink or the Alloy Slave network ATNX, do not use these DOS calls, and the Clipper network functions simply do not work.

Art Mena
Rockwell International
Downey, CA

GENERATION GAP

I find it strange to see in this magazine recommendations for using the 80286 rather than the 80386 for the next PC software generation.

Even though the 80286 can address 16MB in protected mode, it still deals with 64KB segments, which I find disturbing when working with my 640KB PC/XT compatible. That some word processors can handle a maximum 64KB of text is a nuisance. Far more disturbing were my attempts to compile two C programs that I had compiled and run successfully on my old Kaypro II (with the Aztec C compiler running in only 64KB RAM). The deSmet C compiler found both compiling tasks too big. I bought a Datalight C kit (with the large memory model) and tried again, only to get the same result—both compilation tasks aborted with messages about the program being too big. It seems that one 64KB data segment during compilation was too small.

If 80286 software tries to use megabytes of RAM, it will use a large number of segments, each able to cause mysterious crashes when its 64KB limit is exceeded. This nightmare of segments would only cause a migration to 68000-based microcomputers.

The solution is a new microprocessor, software-compatible with the 80386 and pin-compatible with the 80286. PC/AT owners simply replace their 80286 with the new chip to get 16MB of the problem-free linear addressing, and the 8088 software generation can be followed by an 80386 software generation.

Olav Naess
Naess-Data
Bergen, Norway

PC Tech Journal *does not suggest the use of the 80286 for the next software generation. Rather, we suggest that the considerable hardware investment in*

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CIRCLE NO. 102 ON READER SERVICE CARD

80286-based systems (about 3.5 million units installed to date with millions more on the way) be matched by operating systems and applications software that can exploit the 80286's features.

It is rumored that Intel will introduce an 80386 chip compatible with the 80286 pin-outs. Given Intel's past history (chips such as the 8088 and 80188), the rumor is easy to believe, although we have been unable to confirm it. Personally, I am hopeful for such an elegant upgrade path.

—WF

SOUNDING OFF

The SOUNDS program published in "Creating Sound with the Timer" by Augie Hansen (Programming Practices, February 1987, p. 173) contains a serious flaw. A user who is unlucky enough to run SOUNDS just before midnight will be left with a PC that is hung, sounding a continuous tone, and not responsive to Ctrl-Break. This occurs because the **delay** and **getticks** functions incorrectly handle the clock overflow that occurs at midnight.

It is apparent that Mr. Hansen does not understand the BIOS time-of-day (TOD) service. He assumes that the BIOS **read clock** functions will return a nonzero timer overflow flag in AL on all of the calls after midnight. In fact, it returns a nonzero overflow flag only on the first call after midnight, and returns zero for all other calls. This means that **getticks** returns TICKS_PER_DAY once, just after the clock has overflowed at midnight, and returns zero on the next call. If the **delay** function has computed a **then** value that is greater than TICKS_PER_DAY, the delay loop will be never ending.

It would be possible to add code to **delay** to detect overflow of the clock and adjust the **then** value. This would fix the hang problem but introduce a new one: DOS would not know that the clock had overflowed (**getticks** swallowed the only nonzero overflow flag of the day) and would not increment its date. Files and reports created subsequent to this would be stamped with the wrong date until the user manually incremented the date or rebooted the PC. Because of this problem, I recommend that programs never call the BIOS **get time** function. A program that needs to read the clock should either call the appropriate DOS function, or read directly from the BIOS data area at 40:6C. (It should also take suitable precautions against timer interrupt in the middle of the read).

I find it very disturbing that a program with such a serious flaw would find its way into an award-winning magazine. Did Mr. Hansen test his program around midnight? Did you at *PC Tech Journal* test the program? I know that you did not test the typeset version because it contains additional errors, both syntax—lack of blank lines to separate target lines in the **makefile**, and semantic—need to cast **(outregs.x.cx << 16)** to **(long)** in **getticks**.

I know that you cannot guarantee to publish only perfect programs. Perhaps you should consider requiring your contributors to submit a formal test plan and test report along with their programs so that you could judge whether the testing already done was sufficient to meet your standards. Then, if you re-executed the test plan against the typeset version of the program, you would be able to give your readers a high degree of confidence in the programs that you publish.

Robert D. Vavra
Roseville, MN

*Mr. Vavra has described a problem with the **getticks** function that my testing failed to detect. Although I did extensive testing of the SOUNDS program to check machine independence of delay periods and various boundary conditions related to the TOD clock overflow, I never experienced the machine lock-up and shortened delay period problems that are described by Mr. Vavra. Further testing revealed the reason.*

My testing of the overflow detection and compensation was done on an AT&T PC6300 (running DOS 3.1), which maintains the time-of-day differently than the IBM PC. (I did not know this at the time I wrote the program.) On the IBM, when the time is set using the TIME command, the TOD count in the BIOS data area is set to a number of timer ticks that represents the offset since the previous midnight. The PC6300, on the other hand, maintains a count of timer ticks that have occurred since the machine was turned on. The value is unaffected by the TIME command, and both the time-of-day and date values are handled independently of the BIOS TOD count.

The moral of this story is that regardless of how compatible a non-IBM microcomputer may appear, programs designed for use on the PC should be tested on real IBM PC hardware.

*The solution here is relatively simple. I merely replaced the original **getticks** source code with that shown in*

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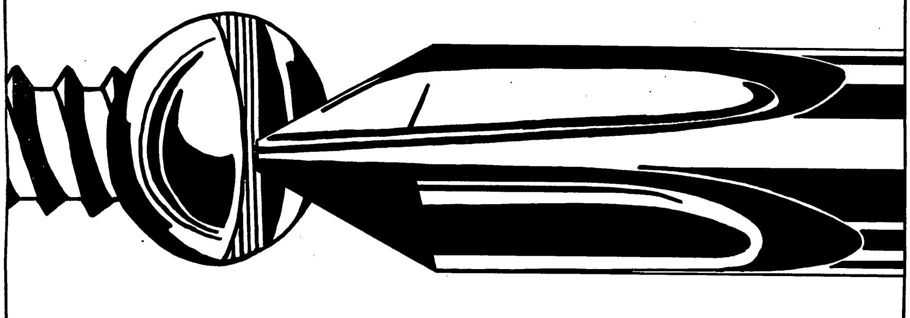

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CIRCLE NO. 119 ON READER SERVICE CARD

the accompanying listing. The new version directly queries the BIOS TOD count in the BIOS data area and then stores the result in ***count****. It also keeps*

```
/*                getticks
 *   get the current BIOS clock ticks value
 */

#include <dos.h>
#define BIOS_DATA_SEG    0x40
#define TIMER_DATA       0x6C
#define TICKS_PER_DAY    0x01800B0L

long
getticks()
{
    static long total = 0;  /* total ticks */
    long count;             /* current TOD */
    long far *lp;           /* far pointer */

    /* set up pointer to BIOS TOD counter */
    FP_SEG(lp) = BIOS_DATA_SEG;
    FP_OFF(lp) = TIMER_DATA;

    /* read the BIOS TOD count */
    while (1) {
      count = *lp;
      if (*lp == count)
        break;
    }

    /* adjust clock roll-over, if needed */
    total = (count < total) ? count
              + TICKS_PER_DAY : count;
    return (total);
}
```

an accumulated count called ***total*** *in a static variable. When the TOD value wraps back to 0 at midnight (or whenever the TOD count overflow occurs on a given machine), a day's worth of timer ticks is added to the raw count to get the new accumulated count.*

If ***getticks*** *attempts to read the TOD count at exactly the same time that the timer interrupt (INT 1CH) occurs, the delay period could be altered by a corrupted reading. My first attempt to solve the problem involved writing an interrupt-immune data-copy function (a replacement for the* ***movedata*** *function in the Microsoft runtime library) in assembly language, but I wanted to provide a solution coded entirely in C. Mr. Vavra suggested comparing the results of two successive reads of the TOD count using the* ***movedata*** *function to ensure a valid reading.*

My revised version of ***getticks*** *sets up a far pointer using FP_SEG and FP_OFF macros contained in the* ***dos.h*** *header file. It reads the TOD counter twice in quick succession, compares the results, and, if necessary, repeats the process until the results are equal. The job done by* ***getticks*** *could be handled within* ***delay*** *to eliminate function-call overhead, but I kept* ***getticks*** *separate because it has other uses.*

LAN REPORT 6

LAN Communications.

An Expanding LAN Connectivity Picture.

Initially, personal computer LANs were a means of sharing departmental PC resources. Early LAN connectivity products were designed to meet the needs of the individual workgroup.

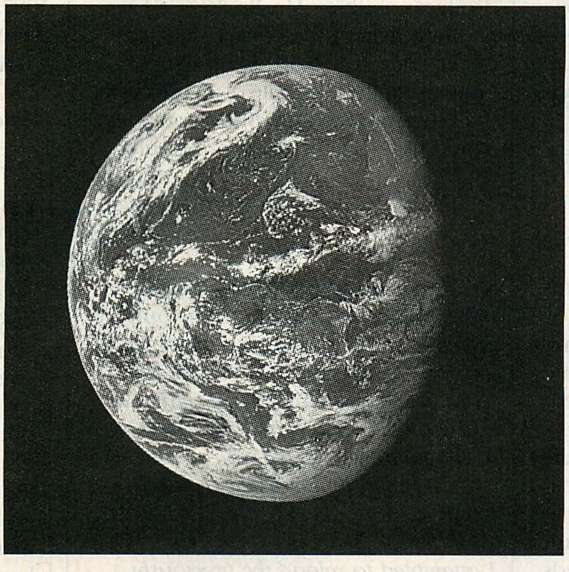
But today's information structures require LANs to integrate easily into a wide variety of external computing resources. In fact, LANs are quickly becoming the focal point for many corporate-wide computing systems. Connectivity has become a primary issue.

As LANs become central to corporate information systems, users have a critical need to connect LANs with other LANs, and to connect LANs with a full spectrum of host computing systems. And not only must LANs provide a variety of high-performance connections, but they must often provide these connections over a broad geographic area.

Novell is prepared to meet this new level of needs through the NetWare series of LAN Communications products. Using industry-proven protocols and communications standards, Novell provides LAN communications in three key areas: 1) local and remote LAN bridges, 2) host gateways, and 3) remote PC connections.

Local and Remote LAN Bridges.

Through NetWare Bridge Software, users can link all departmental LANs into a single, comprehensive internetwork, that could encompass as many as 17 brands of network media. Users can communicate with any file server on the internet, regardless of which network they are logged into or what hardware they are using.



"Not only must LANs provide a variety of high-performance connections, but they must often provide these connections over a broad geographic area."

For LANs that require remote bridge connections, NetWare's Asynchronous Remote Bridge provides connections to remote LANs at speeds of up to 19.2K baud. To the user, the remote LAN connection appears just like a local bridge.

And the NetWare X.25 Remote Bridge allows users to connect with multiple remote LANs, all over the world, and to share data at speeds up to 64K bps. The X.25 Bridge includes its own advanced routing capabilities. NetWare X.25 Remote Bridges can connect any variety of NetWare LANs, using either dial-up or leased line connections, through private or public data networks such as Telenet or Tymnet.

Host Gateways.

NetWare host gateways provide high-performance connections to a variety of local or remote computer systems. NetWare Asynchronous Connection Services (NACS) allows NetWare LANs to connect to a wide variety of asynchronous resources. The NetWare X.25 Gateway allows a network to run terminal emulation for either 32 or 256 sessions, over a single port connection.

And not only can the X.25 Gateway connect a LAN to a company's local host computers, but it can provide remote gateway connections for many popular host resources through public data networks.

Novell's LAN gateway products also include CXI's LAN-to-mainframe connections, emulating both IBM 3270 and 5250 systems. These highly advanced LAN gateways can operate either locally or remotely, supporting as many as 64 sessions and operating at speeds up to 64K bps.

Remote PC Connections.

NetWare's communication services allow remote personal computers, through the NetWare AnyWare software package, to have access to a NetWare LAN just as if they were local. This service supports as many as 12 concurrent sessions, using one local workstation on the LAN for the duration of each remote connection.

Putting It All Together.

Today's advanced LAN capabilities make it feasible for NetWare users to connect entire corporations, over broad distances, through LANs. Novell's LAN Communications series of products is designed to make your network expansion easier.

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CIRCLE NO. 109 ON READER SERVICE CARD

I extend thanks to Mr. Vavra for bringing the problem to my attention (and for taking the time to discuss my proposed solutions).

—Augie Hanson

The missing blank lines to which Mr. Vavra refers were, unfortunately, removed from MAKEFILE in the edit process. PC Tech Journal *regrets the error.*

Mr. Vavra's suggestion that authors submit a test plan of their programs is a good one. We are working to put such a plan into effect.

—JA

PROFILE OF A PROFILER

With regard to Ralph G. Brickner's review of the Profiler in the February 1987 issue ("Execution Profilers for the PC, Part 2," p. 166), I would like to thank Mr. Brickner for an excellent article. He presented a fair assessment of the execution profilers on the market. However, he did leave out some facts.

First, the Profiler by dwb Associates includes the source code to the product. We feel that a tool of this nature can be of higher value to a programmer if it can be tailored to individual needs. A **makefile** is included to show how the product is built.

Second, although Mr. Brickner has valid points about the desired functionality of an execution profiler, the Profiler has been through eight revisions in three years to incorporate functions and changes to the product as requested by our sophisticated users..

Lastly, the example of the Profiler's output is not a fair assessment of the product's abilities. Mr. Brickner shows a partition map of the default values of the Profiler. If he had set up the partitions using the .MAP file as he did with the other products, the histogram would have given meaningful results.

Jeff B. Erwin, president
dwb Associates
Portland, OR

Mr. Erwin is correct that the Profiler offers source code, and it is the only reviewed product that does; however, the code is not supplied with the software. Instead, the user must return a request letter (that is included with the package) to receive the source code.

As noted in the article, I did attempt to set up the partitions using the .MAP file of the example program. When I attempted to reload the previously saved partition limits from disk, the result was an error message that said "Invalid hex number in partition file." The documentation gave no hint about the problem or its solution. Thus, I simply presented its default display.

—Ralph G. Brickner

ERRATUM

In the Product Watch on "Diskit 2 Plus" and "Durapak" (Peter G. Aitken, May 1987, p 197), in table 2 on page 205, the unit for effective transfer rate under ATDISK should be milliseconds/KB (ms/KB). Thus, a smaller number would indicate a better result.

COMMENT AT WILL

All letters to the editor should be directed to Editor, *PC Tech Journal*, Suite 800, 10480 Little Patuxent Parkway, Columbia, MD 21044. Correspondence also can be submitted over MCI Mail to PCTECH.

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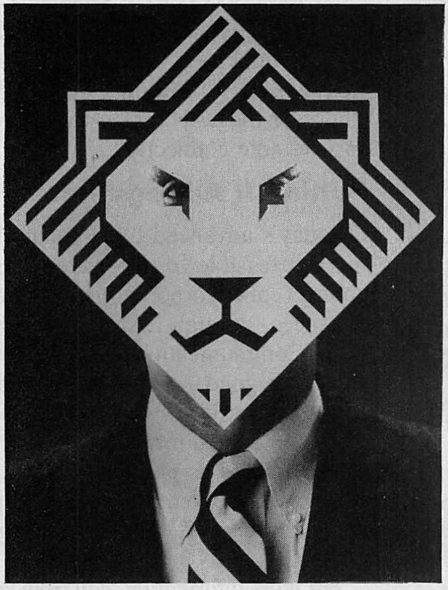

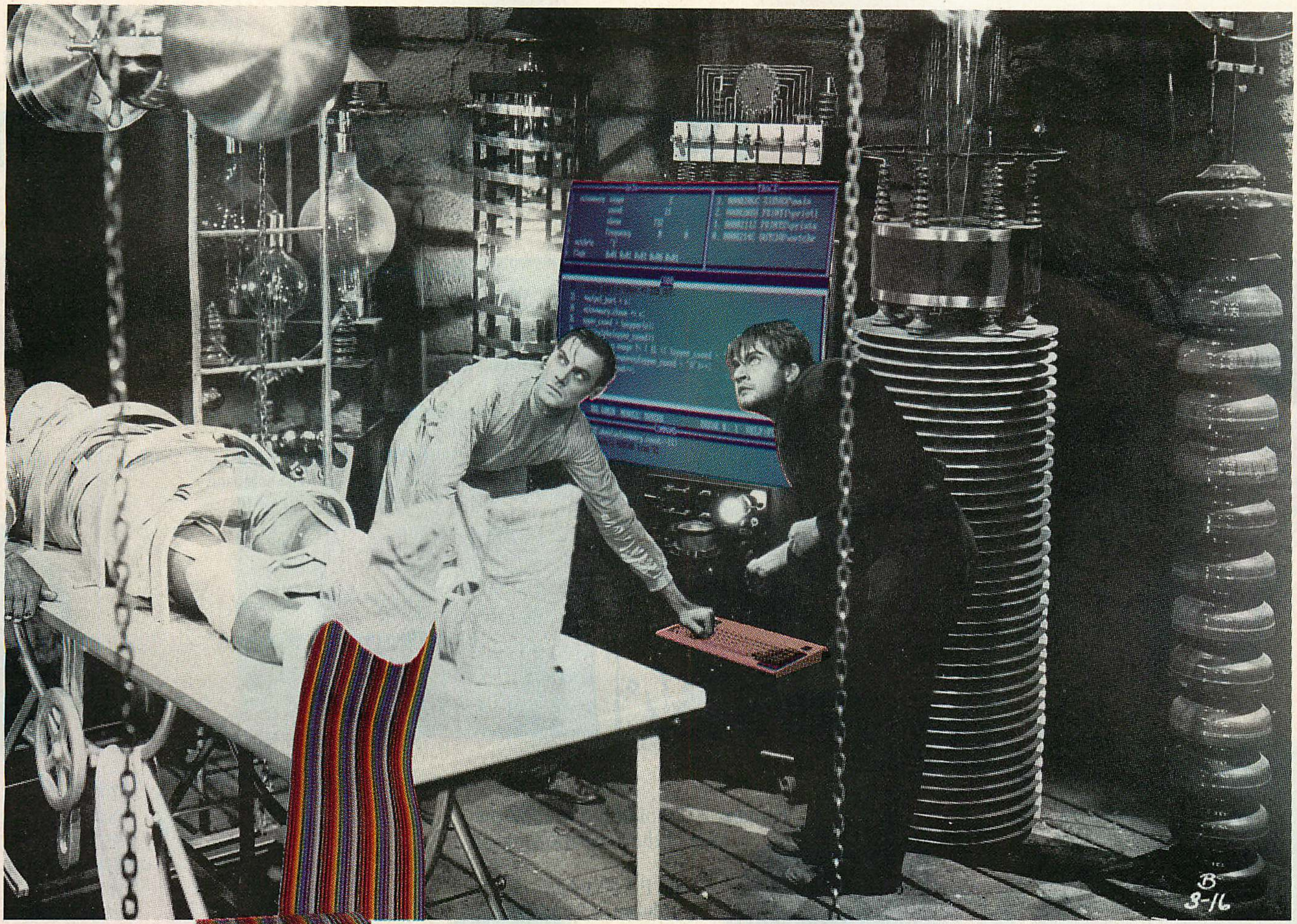

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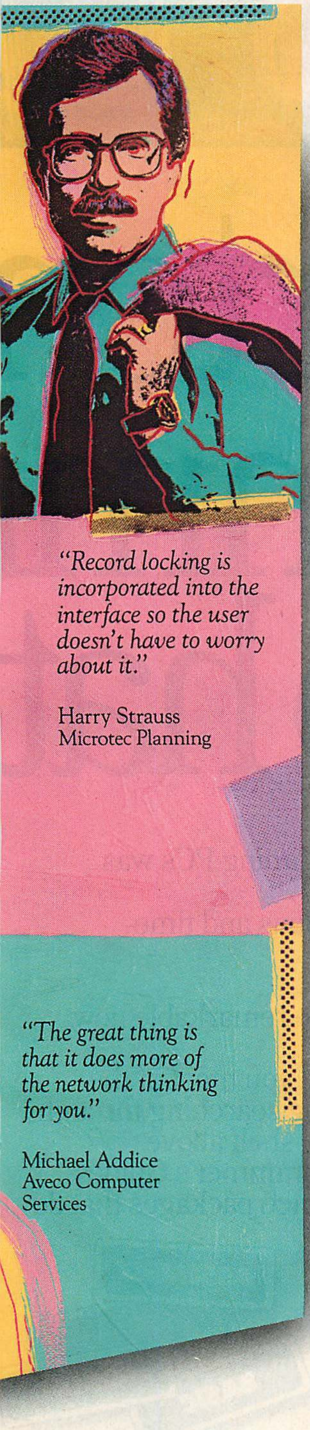

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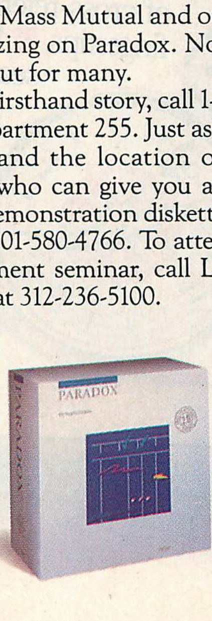

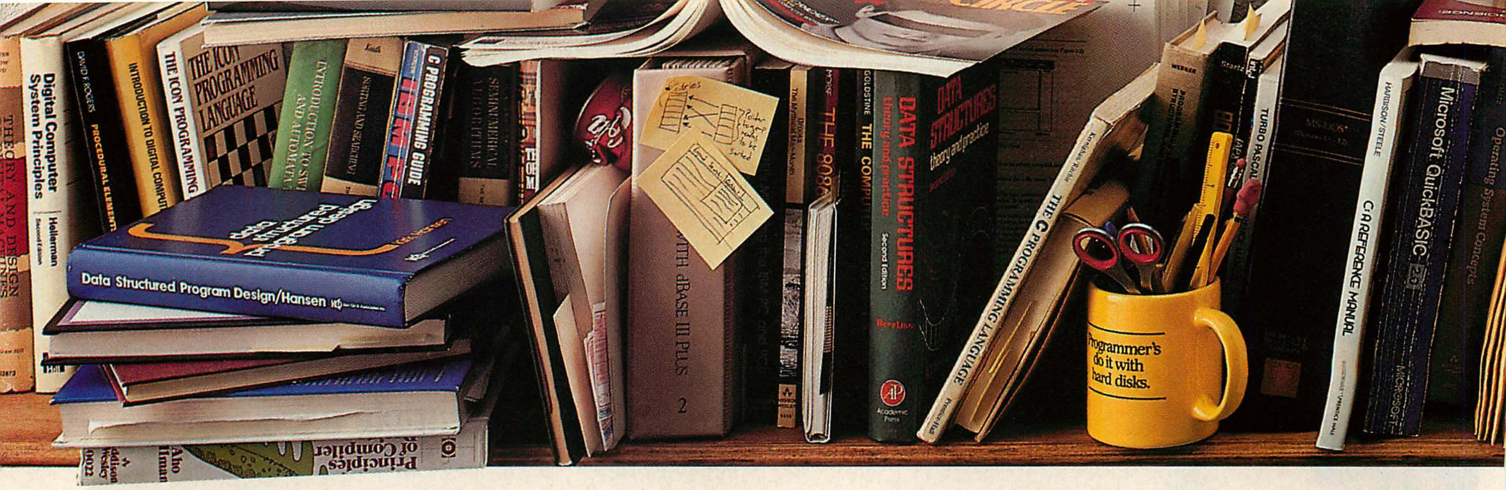

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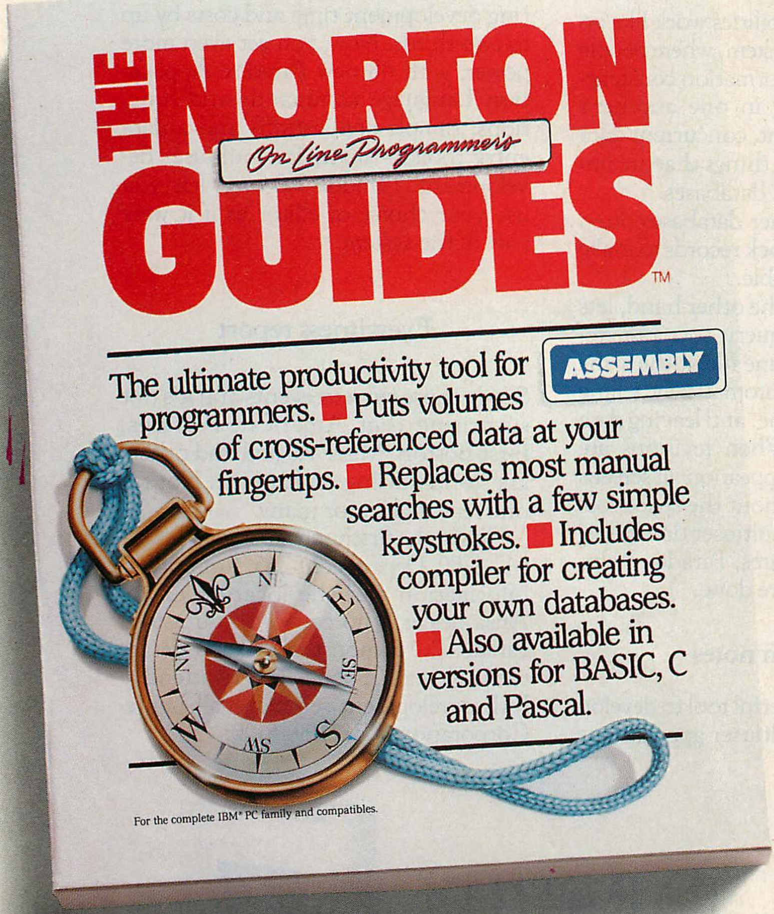

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Not since the arrival of the remarkable new program on the left.

Which is designed to save you most of the time you're currently spending searching through the books and manuals on the shelf above.

The Norton On-Line Programmer's Guides™ are a quartet of pop-up reference packages that do the same things in four different languages.

Each package consists of two parts: A memory-resident instant access program. And a comprehensive, cross-referenced database crammed with just about everything you need to know to program in your favorite language.

And when we say everything, we mean everything.

Everything from information about language

Designed for the IBM® PC, PC-AT and DOS compatibles. Available at most software

announces a g tool for people e manual labor.

syntax to a variety of tables, including ASCII characters, line drawing characters, error messages, memory usage maps, important data structures and more.

How much more?

Well, the databases for BASIC, C and Pascal give you detailed listings of all built-in and library functions.

While the Assembly database delivers a complete collection of DOS service calls, interrupts and ROM BIOS routines.

You can, of course, find most of this information in the books and manuals on our shelf.

But Peter Norton—who's written a few books himself—figured you'd rather have it on your screen.

In seconds.

In full-screen or moveable half-screen mode.

Popping up right next to your work. Right where you need it.

```
        SBB     BX,[BP].HI
        MOV     [SI],AX
        MOV     SI,[BP].HI_ADDR
        MOV     [SI],BX
        MOV     AX,0                    ;Return 0 if no borrow
        RCL     AX,1                    ;Return 1 if borrow
        POP     SI
```

```
AAA                 ASCII Adju
AAD                 ASCII Adju
AAM                 ASCII Adju
AAS                 ASCII Adju
ADC                 ADD with C
ADD                 Addition
AND                 Logical AND
CALL                CALL Procedure
```

```
_DWORD_ADD      PROC    NEAR
        PUSH    BP
        MOV     BP,SP
        PUSH    SI
FinalWord V2.01              C:\LIBS\CLIB\misc.asm  11   42/155       7:11pm
```

A Guides reference summary screen (shown in blue) pops up on top of the program you're working on (shown in green).

```
RCL        Rotate Through Carry Left          Flags affected:  O S Z A P C
                                                               x         x
RCL destination,count

   RCL moves the bits in its destination left by either 1 bit, or by the
   number given in CL.  The Carry Flag is included in the rotation -- that
   is, the high bit of the destination is transferred into the Carry Flag
   and the Carry Flag is transferred into the low-order bit (bit 0) of
   the destination.  The destination may be a word or a byte.

Operands              Clocks          Transfers   Bytes    Example
                    byte(word)
  register, 1           2                 -         2      RCL CX,1
  register, CL       8 + 4/bit            -         2      RCL AL,CL
  memory, 1         15(23) + EA           2        2-4     RCL ALPHA,1
  memory, CL      20(28)+EA+4/bit         2        2-4     RCL [BP].PARM,CL
```

Summary data expands on command into extensive detail. And you can select from a wide variety of information.

This, you're probably thinking, is precisely the kind of thinking that produced the classic Norton Utilities.™

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dealers, or direct from Peter Norton Computing, Inc., 2210 Wilshire Blvd., #186, Santa Monica, CA 90403. 213-453-2361, Fax 213-453-6398, MCI Mail: PNCI ©1987 Peter Norton Computing

CIRCLE NO. 192 ON READER SERVICE CARD

Developments for the systems professional

Novation, Inc.'s Parrot 1200 external modem

Apricot XEN-i 386 from Apricot Computers

SYSTEMS

The **RDS 3000** workstation from **MAD Intelligent Systems, Inc.** is a 80386-based unified hardware and software system for integrating artificial intelligence technology with conventional computing. The RDS 3000 includes MAD's proprietary software RelationalLisp, a powerful extension to Common LISP. RelationalLisp provides AI techniques for expert system development and the ability to access relational databases. The RDS 3000 workstation runs UNIX V.3 and DOS; it includes X-Windows as well as several implementations of Common LISP. Along with the Intel 80386, the RDS 3000 is designed with an AT-bus architecture, eight expansion slots, and an 85MB hard disk. It can be configured with up to 16MB of RAM. Prices start at $16,000 depending on workstation memory configuration.

MAD Intelligent Systems, Inc., 2950 Zanker Road, San Jose, CA 95134; 408/943-1711

CIRCLE 305 ON READER SERVICE CARD

A 32-bit microcomputer that has a small footprint (16½ by 13⅜ by 5¾ inches) is available from **American Mitac Corporation**. The **MPC 3000** has a 16-MHz clock speed and incorporates the 80386 chip set from Chips & Technologies. An on-board diskette drive controller, serial and parallel port, realtime clock, enhanced keyboard, eight expansion slots, and 1MB RAM are standard. Prices start at $2,500 based on configuration.

American Mitac Corporation, 3385 Viso Court, Santa Clara, CA 95054; 408/988-0258

CIRCLE 303 ON READER SERVICE CARD

A 16-MHz PC/AT compatible based on the Intel 80386 is offered by **PC Discount**. The speed of the **Noble 386** is keyboard selectable at either 8 or 16 MHz. The machine comes standard with a 1.2MB diskette drive, a 40MB hard-disk drive, an enhanced keyboard, a socket on the system board for an 80387, and 1MB RAM (expandable to 4GB). $3,999.

PC Discount, 2758 Bingle Road, Houston, TX 77055; 713/984-1177

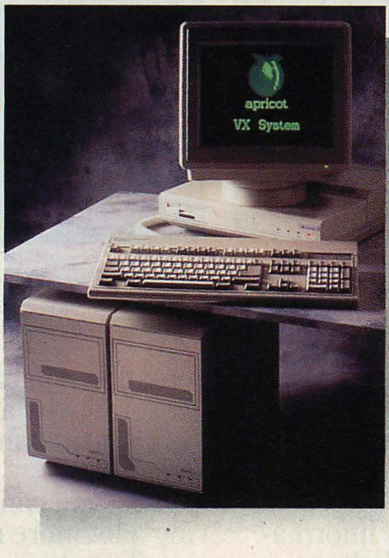
CIRCLE 304 ON READER SERVICE CARD

The 80386 arena has been entered by **Apricot Computers**. Using a Phoenix ROM BIOS and Intel's 80386, the **Apricot XEN-i 386** features one 1.2MB 5¼-inch diskette drive, 1MB of RAM, and a choice of a 30MB or 45MB hard-disk drive with an average access time of 25 ms (milliseconds). XEN-i 386/30, $9,995; XEN-i 386/45, $10,995.

A multiuser version, the **Apricot VX** features a 16-MHz Intel 80386 and support for the 80387. It comes with a single 1.2MB 5¼-inch diskette drive, and as many as four drive subsystem units can be connected in a daisy chain to provide a maximum drive capacity of 1.8GB per system. A choice of 70MB, 157MB, and 268MB hard-disk drives are available together with a 125MB ¼-inch tape back-up unit and an optional 800MB 5¼-inch write once, read many (WORM) optical cartridge for archiving. It is available with either Apricot Network or XENIX 80386. Prices range from $17,995 to $24,995.

Apricot Computers, Inc., 4 Director Court, Suite 105, Woodbridge, Ontario, Canada L4L 3Z5; 416/851-8511

CIRCLE 301 ON READER SERVICE CARD



Apricot VX multiuser system

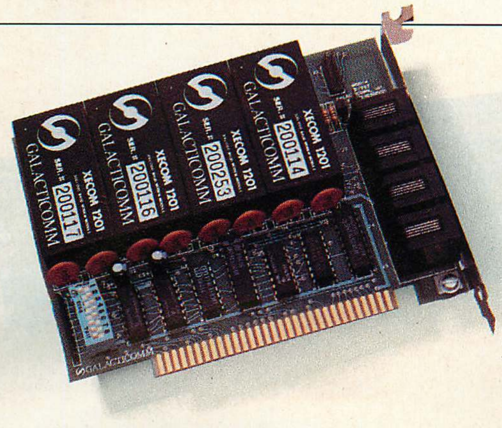
CONNECTIONS

An enhanced version of **The Major BBS**, a multiuser bulletin board system, has been released by **GALACTICOMM, Inc.** Added features of **version 3.0** include a file-upload option, a system-statistics display for the sysop (system operator), an XMODEM downloadable demonstration package, with direct log-on capability at the operator console, a sysop chat feature, and enhanced documentation. In addition to its existing 16-modem card, GALACTICOMM has added a 4-modem card, the **BREAKTHROUGH Model 4**, which provides full multiuser support for The Major BBS. BREAKTHROUGH provides voice synthesis capability as well as dual-tone multifrequency (DTMF) input decoding and full 300/1200 bps (bits per second) modem functions. The Major BBS, $59; BREAKTHROUGH Model 4, $1,988; voice synthesis, $38 per channel.

GALACTICOMM, Inc., 11360 Tara Drive, Plantation, FL 33325; 305/472-9560

CIRCLE 314 ON READER SERVICE CARD

A three-ounce, 300/1200-bps (bits per second) modem has been introduced by **Novation, Inc.** Measuring 4¼ by 2¾ by ⅝ inches, the **Parrot 1200** offers compatibility with the Hayes AT command set, full-duplex operation, asynchronous data format, built-in automatic self test, touch-tone or pulse dialing, and automatic answer. It also has analog, local digital, and remote digital



BREAKTHROUGH Model 4, GALACTICOMM's 4-modem card

American Mitac's 80386-based MPC 3000

loop-back testing. Options include adapter, cable, and software. $119.
Novation, Inc., 21345 Lassen Street, Chatsworth, CA 91311; 818/998-5060
CIRCLE 307 ON READER SERVICE CARD

Texas Instruments (TI) has made available the **IEEE 802.2 Logical Link Control** (LLC) for its **TMS380 Token Ring LAN Chipset**. The TMS380 is a VLSI (very large scale integration) chip set with IEEE 802.2 LLC. The chip set was the result of a joint development project of TI and IBM. IEEE 802.2 has been selected by IBM for the Token-Ring Network, by several major computer OEMs, and by the International Standards Organization for Open System Integration (OSI) LAN protocols. Because connection-oriented LLC protocols now can be handled on the TMS380, the host system is freed from time-consuming operations, such as sequencing, acknowledgments, link session control, and automatic retries. The **TMS380 LLC Evaluation Kit** is designed for developers and users of token-ring adapters for the PC who wish to evaluate the LLC software. License fee for IEEE 802.2 LLC and Adapter Handler Emulator software, $24,000; LLC software (quantities of 5,000), $13 each; TMS380 chip set (quantities of 100), $115 each; TMS380 LLC evaluation kit, $802; PC adapter card with LLC, $1,750; PC/AT adapter card with LLC, $1,750.
Texas Instruments, Semiconductor Group (SC-723), P.O. Box 809066; Dallas, TX 75380; 800/232-3200, ext. 700
CIRCLE 308 ON READER SERVICE CARD

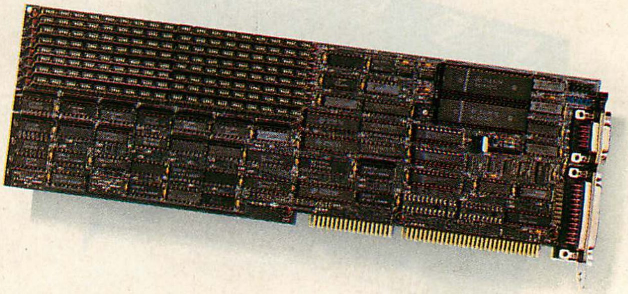
A LAN for workstations in small- to mid-sized businesses has been introduced by **Computer Pathways, Inc.** The 3.6 million bits per second (mbps) **Grapevine** LAN links as many as 50 IBM PCs without requiring a dedicated file server. Grapevine remains resident in the RAM of each user's PC, yet consumes less than 128KB of memory. Grapevine can communicate as far as 4,000 feet over coaxial cable or twisted-pair wire. All network functions can be performed from within an application. Grapevine is called up with a single keystroke and provides full on-screen information, such as the names of the printers and the number of jobs in each print queue. Users can send electronic mail and transfer files from within an application by using a single keystroke to reveal pull-down menus containing options for sending, receiving, or storing. Evaluation kit, $9.95; one-month rental for two-station system, $195.00; Grapevine, $595 per station (not including wiring or cabling).
Computer Pathways, Inc., 19102 N. Creek Parkway, Bothell, WA 98011; 206/487-1000
CIRCLE 310 ON READER SERVICE CARD

A data communications software package for the PC, **Carbon Copy PLUS** from **Meridian Technology, Inc.**, combines PC-to-PC remote control, PC-to-host terminal emulation, and Kermit and XMODEM file transfer protocols. The PLUS version has all of the remote-operation and control features found in the original Carbon Copy, plus additional remote control features, the ability to emulate a full complement of terminals for access to on-line databases, compatibility with Crosstalk script files, and support of Kermit and XMODEM protocols for file transfer. In terminal emulation mode, Carbon Copy PLUS emulates a number of asynchronous terminals, including a DEC VT-52, DEC VT-100, Televideo 920, and IBM 3101. It supports IRMA remote emulation boards and has 40 programmable function keys, a scrollable look-back window with retroactive capture, an on-line emulator configuration menu, command language for script-file creation, automatic script-file execution, and a point-and-choose scrollable call table, which is alphabetized and indexed. In remote-control mode, Carbon Copy PLUS can link two PCs over an asynchronous dial-up link or direct serial connection enabling the two PCs to act as one. $195.
Meridian Technology, Inc., 1101 Dove Street, Suite 120, Newport Beach, CA 92660; 714/476-2224
CIRCLE 311 ON READER SERVICE CARD

An enhanced version of **Waterloo PORT**, an advanced LAN program by **Waterloo Microsystems Corporation**, is available. **Version 2.4** provides improved speed and has full NETBIOS and foreign-language keyboard support. PORT runs all application programs written for DOS and can be used to interconnect stand-alone PCs or to connect PC networks to minicomputers and mainframes, as well as to provide internetworking between LANs, both locally and remote. Coaxial, twisted-pair, and fiber-optic cables as well as the IBM Cabling System can be used as transmission mediums in a Waterloo PORT PC LAN. In addition to a standard keyboard interface, PORT provides an optional icon-based user interface. $1,695.
Waterloo Microsystems Corporation, 3597 Parkway Lane, Suite 200, Norcross, GA 30092; 404/441-9252
CIRCLE 312 ON READER SERVICE CARD

Shipment has begun on **version 11.8** of **PCBoard**, a remote bulletin board software package from **Clark Development Company**. PCBoard 11.8 continues to provide complete support for the 9600-bps (bits per second) dial-up modems, including two full-flow protocols (Imodem and Ymodem-G), which take full advantage of built-in hardware error checking and provide high throughput rates without software slowdowns. PCBoard can act as a host for other software applications; the system operator can install many standard programs so that the users of the bulletin board can run them via modem from a remote location. PCBoard offers complete net-

3COM's 3Station dedicated network workstation



Elite 16, Profit Systems, Inc.'s 16-bit multifunction board

working support; it functions properly under any network software that supports DOS 3.0 (or later) file-sharing conventions. Additional features include enhanced color graphics capabilities, download file protection, file imports and exports from message bases, full 8-bit file transfer protocols including XMODEM, CRC XMODEM, Ymodem CRC, Imodem, and Ymodem-G, and complete conference support with separate messages, bulletins, files, and script questionnaires. PCBoard can store as many as 10,000 messages on line at once. Price range from $79.95 (standard version) to $999.95 (concurrent network support of 99 nodes).
Clark Development Company, P.O. Box 71365, Murray, UT 84107; 801/964-6692

CIRCLE 313 ON READER SERVICE CARD

A dedicated network workstation has been announced by **3Com Corporation**. The **3Station**, an IBM-compatible 80286-based Ethernet workstation that can be integrated with PCs on a network, features four graphics adapters, 1MB of main memory (that can be upgraded to 4MB), and Ethernet. Overall dimensions (14 by 14 by 3 inches) include a channel on the bottom of the unit for routing and collecting the cables. The 3Station also includes an enhanced keyboard, power cable, BNC connector, and user's guide. $1,895.

Also announced were **TokenLink** and **EtherLink II**, two products that expand 3Com's existing network interface line. TokenLink is the entry-level follow-up to TokenLink Plus, a high-performance adapter with an 80186 and 256KB of on-board RAM. EtherLink II is the successor to EtherLink, the industry-standard IEEE 802.3/Ethernet connection for PCs. These boards satisfy the connectivity requirements for the IBM Personal System/2 (PS/2) Model 30, as well as the PC, PC/XT, and PC/AT. An Ethernet adapter to support the Micro Channel architecture is under development for the other PS/2 models. Both of these adapters feature software-selectable DMA (direct memory access) and interrupt channels, allowing a network manager to adjust an adapter's parameters from the keyboard without disassembling the host machine. TokenLink Plus adapter, $895; TokenLink, $650; EtherLink II, $495; EtherLink, $495; TokenLink Software Starter Kit; $3,495.
3Com Corporation, 3165 Kifer Road, Santa Clara, CA 95052-8145; 408/562-6400

CIRCLE 306 ON READER SERVICE CARD

Two wiring products, the **Codex 4320 LAN Hub** and the **Codex 4303 Transceiver**, have been released by **Codex Corporation**. The Codex 4320 LAN Hub is an 8-to-1 LAN port-sharing device that features Codex's collision-avoidance technique. The Codex 4320 LAN Hub cascades to support a total of 64 LAN ports or, when implemented as a standalone LAN, as many as 4,096 LAN ports. The Codex 4303 Transceiver connects a LAN device to baseband coaxial cable and features a compact design. Both the 4320 and the 4303 support Open System Integration (OSI) levels 1 and 2 for Ethernet and IEEE 802.3 equipment. 4320, $1,095; 4303, $270.
Codex Corporation, 20 Cabot Blvd., Mansfield, MA 02048-1193; 617/364-2000

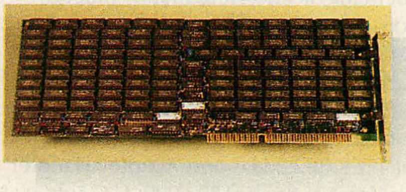
CIRCLE 315 ON READER SERVICE CARD

PERIPHERALS

An 80386 coprocessor that plugs into the PC/XT or PC/AT to give developers the power of a technical workstation in a DOS environment has been developed by **A.I. Architects**. The **386 HummingBoard** uses an Intel 32-bit 80386 running at 16 MHz or 20 MHz, an optional 80387, a high-speed cache memory for zero-wait-state operation and from 2MB to 24MB of parity-protected, dual-ported RAM. **OS/386**, a proprietary DOS-extension operating system, allows applications to run in protected mode on the 80386 while the host system's microprocessor concurrently handles I/O. Full 32-bit language support for C, Pascal, assembly language, FORTRAN, and LISP is available, thus many applications can harness the power of the 80386 simply by being recompiled. Prices start at $3,000.
A.I. Architects, Inc., One Kendall Square, Suite 2200, Cambridge, MA 02139; 617/577-8052

CIRCLE 317 ON READER SERVICE CARD

A 12-MHz memory board with 12MB of extended and expanded memory has been developed by **American Micronics, Inc.** The **Elephant-12** can run with zero wait states in a one-wait-state machine. Using programmable array logic (PAL) chips, this board automatically detects upgraded memory in sockets, thus the board is configured only once. The PAL chips also provide built-in security protection. With 0KB, $695; 2MB, $2,495; 12MB, $11,495.
American Micronics, Inc., 17831 Skypark Circle, Suite C, Irvine, CA 92714; 714/261-2428



Elephant-12, American Micronics' 12-MHz memory board

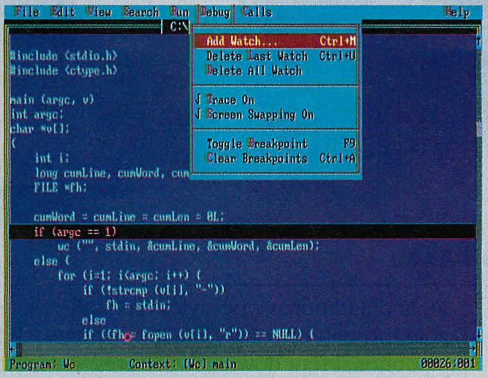
CIRCLE 319 ON READER SERVICE CARD

A multifunction board for 80286 applications with high memory and I/O requirements is offered by **Profit Systems, Inc.** Using either 256KB or 1MB modules (or any combination of the two) on-board memory of the **Elite 16**

MICROSOFT LANGUAGES NEWSLETTER VOL. 2, NO. 7

News about the Microsoft Language Family

New Microsoft® QuickC™ Compiler Provides Easy C Programming Through Total Integration



```
#include <stdio.h>
#include <ctype.h>

main (argc, v)
int argc;
char *v[];
{
    int i;
    long cumLine, cumWord, cum
    FILE *fh;

    cumWord = cumLine = cumLen = 0L;
    if (argc == 1)
        wc ("", stdin, &cumLine, &cumWord, &cumLen);
    else {
        for (i=1; i<argc; i++) {
            if (!strcmp (v[i], "-"))
                fh = stdin;
            else
            if ((fh = fopen (v[i], "r")) == NULL) {
```

Microsoft QuickC at Work.

Many of you have been waiting for a $99 C compiler designed to help get your programs running quickly. Microsoft QuickC Compiler Version 1.0, being released in the third quarter of 1987, comes with a completely integrated development environment allowing you to edit, compile and debug your programs without ever leaving QuickC.

The key features of QuickC include an in-memory compiler, an integrated source-level debugger, an in-memory MAKE utility and a full-screen editor. A supplied graphics library with a wide range of screen-control functions allows you to take advantage of the extensive graphics capabilities of the IBM® Personal Computer. A stand-alone MAKE utility, completely compatible with the in-memory MAKE, is provided. QuickC includes a LIB utility for creating, organizing and maintaining object module libraries and a LINK utility for combining relocatable object modules into an executable program.

Write Bug-free C Programs More Easily with the Microsoft QuickC Integrated Debugger

Microsoft QuickC has an integrated source-level debugger that lets you see exactly what your program is doing. This makes writing bug-free C programs easier than ever before. Borrowing from the CodeView™ debugger technology in Microsoft C, the QuickC debugger lets you pinpoint errors by stepping through the source code while it executes, using animate, trace, or single-step mode. Set, examine and clear dynamic breakpoints to stop execution as needed so you can take a closer look at what your program is doing. And find out how you got to a particular point in your program by backtracing within the stack to check past history. The Watch Window lets you observe the contents of both local and global variables and see them change as your program executes. Use the screen-swapping feature for screen-intensive applications, switching between the source code and program output as you debug. Best of all, when the bug is fixed just hit the ‹F5› key and your program compiles and runs until the first breakpoint is reached.

In-Memory Compiling and Editing Speed Up Programming

In-memory compilation makes Microsoft QuickC extremely fast: On an IBM PC AT, it compiles and links at 7,000 lines per minute. It can catch up to 26 errors during a single compilation, allowing you to fix all problems before recompiling. During recompilations, the in-memory MAKE utility saves you additional time by creating the MAKE file for you and recompiling only the changed modules.

At the end of a compilation, the editor helps you by placing the cursor at the point of the first error and subsequent errors. It also speeds the correction process by providing detailed information about the nature of each error.

The compiler's integrated full-screen editor includes a broad range of helpful functions, including Cut, Copy, Paste, Undo, Search and Replace, Overtype, and Insert. A "hot key" allows you to toggle between two program modules when editing multiple-module programs. And there's context-sensitive, on-line help to answer your C language and library questions.

For more information on the products and features discussed in the Newsletter, **write to: Microsoft** Languages Newsletter 16011 NE 36th Way, Box 97017, Redmond, WA 98073-9717. **Or phone:** (800) 426-9400. In Washington State and Alaska, call (206) 882-8088. In Canada, call (416) 673-7638.

Latest DOS Versions:	
Microsoft C Compiler	4.00
Microsoft COBOL	2.20
Microsoft FORTRAN	4.00
Microsoft Macro Assembler	4.00
Microsoft Pascal	3.32
Microsoft QuickBASIC	3.00

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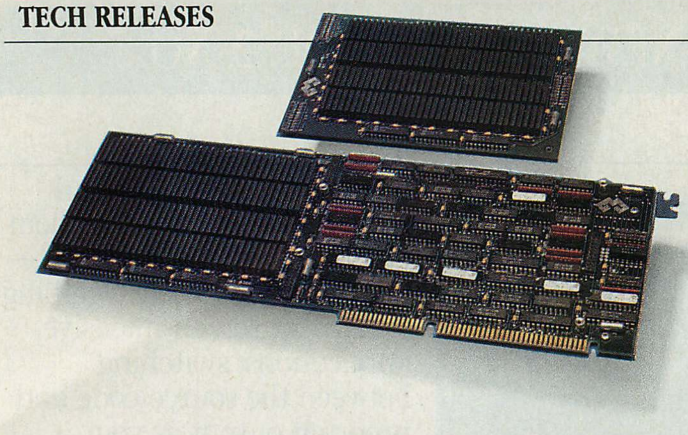
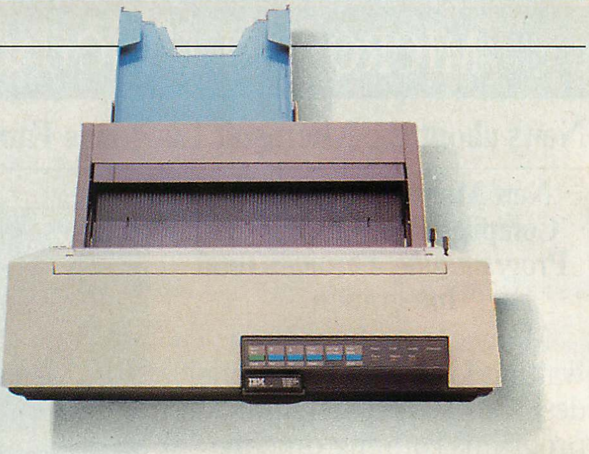
Look for the Microsoft Languages Newsletter every month in this publication. **Microsoft®**



Monolith Systems' JustRAM (front) with mezzanine array board



IBM Quietwriter III printer

can be increased from 512KB to a maximum of 16MB. Expanded memory is supported with true 16-bit data transfer. High-speed AT-compatible systems are supported at speeds of 6, 8, 10, or 12 MHz. Both 6-MHz and 8-MHz zero-wait-state systems are supported. One parallel port is standard and two RS-232 serial ports are supported. AutoRAM software is included for automatic installation, flexible memory and I/O configuration, and expanded memory support. With 512KB RAM, $695.

Profit Systems, Inc., 30150 Telegraph Road, Birmingham, MI 48010; 313/647-5010

CIRCLE 323 ON READER SERVICE CARD

Four printer models have been enhanced by **IBM Corporation**. The **IBM Proprinter II** is an upgraded version of the IBM Proprinter. It features a 9-wire, dot-matrix technology, all-points-addressable (APA) graphics, double-high characters, near-letter-quality (NLQ) switch, tear-off assist, set-up mode, and quiet mode. It prints at 240 cps in Fastfont mode, 200 cps in data-processing (DP) mode, 120 cps in emphasized mode, and 40 cps in NLQ mode. $549.

The **IBM Proprinter X24** and **XL24** (wide-carriage version) uses 24-wire, dot-matrix technology and accommodates the full IBM PC character set. The printers' speeds are 240 cps in DP mode and 80 cps in NLQ mode. Both printers feature switches to select NLQ, quiet mode, pitch/font selection, and push-button controls to select condensed text, oversized characters, emphasized print, forms load assist, store settings in memory, zero slash, and reset. X24, $799; XL24, $1,049.

The **IBM Quietwriter III** printer offers executive-quality print at 120 cps and NLQ print at 192 cps. The printer also provides high-resolution APA graphics. The sound level is 45 decibels while printing. This printer supports eight on-line fonts. Four fonts are built in, and additional type styles are available through optional plug-in cartridges or optional font download features. Other options include a dual-drawer sheet feed and envelope handler. $1,699; bidirectional pinwheel forms feed, $99; one-drawer sheet feed, $350; dual-drawer sheet feed, $849; sheet-feed adapter kit, $35; envelope handler, $299.

IBM Corporation, Information Systems Group, 900 King Street, Rye Brook, NY 10593; 800/426-2468

CIRCLE 318 ON READER SERVICE CARD

A combination accelerator/Enhanced Graphics Adapter (EGA) has been created by **PC Technologies, Inc.** The **286 Rainbow Plus** combines a 10-MHz 80286 accelerator with 16KB cache memory, a high-resolution EGA, and a clock/calendar with battery back-up. A daughterboard is available with a parallel port and a Microsoft InPort mouse interface. The accelerator has a socket for an optional 80287, and external switch for 80286 or 8088 operation, and a hot key to enable or disable cache RAM at any time without rebooting. $945; daughterboard, $50.

PC Technologies, Inc., 704 Airport Blvd., P.O. Box 2090, Ann Arbor, MI 48106; 800/821-3086; in Michigan, 313/996-9690

CIRCLE 321 ON READER SERVICE CARD

Up to 8MB of additional memory in a single slot is possible with **JustRAM** (Model MSC 4940), a memory expansion module for the PC/AT. Introduced by **Monolithic Systems Corporation**, JustRAM provides either 4MB or 8MB of additional parity-checked memory; it may be used as conventional, expanded, or extended memory. The board operates at 12 MHz with wait states or at 8 MHz with zero wait states. Users of other operating systems that address memory directly (such as XENIX), can access a full 16MB of conventional memory with two boards. On-board switch settings allow DOS users to select I/O addresses and give them the option to back-fill conventional memory from 512KB to 640KB. Switches allow XENIX users to set the starting address and capacity. Using 256KB RAM chips soldered in a zipper-like arrangement, JustRAM consists of a 4MB motherboard. A mezzanine RAM array board provides another 4MB. The motherboard can operate independently of the mezzanine array board. JustRAM, $1,495; mezzanine board, $1,195; 8MB combination module, $2,690.

Monolithic Systems Corporation, 84 Inverness Circle E, Englewood, CO 80112; 303/790-7400

CIRCLE 320 ON READER SERVICE CARD

A coprocessor board for the PC bus that features Texas Instruments TMS32020 has been released by **Symmetric Research**. The 5 million instructions per second (mips) chip computes 16-bit by 16-bit multiples in one clock cycle, making it ideal for computationally intensive graphics and numerical applications. The TMS32020 board can be completely populated with the full 256KB of memory addressable by the 32020, and is mapped into one 64KB PC segment. This allows for fast data movement on and off the board. Included with the package is a monitor/debugger that features breakpoint execution and disassembly, a utilities library for controlling board execution from C and a number of application programs. With 32KB RAM, $900; with 256KB, $1,100.

Symmetric Research, 15 Central Way, Suite 9, Kirkland, WA 98033; 206/828-6560

CIRCLE 322 ON READER SERVICE CARD

DATABASE MANAGEMENT

A stand-alone relational database management system (DBMS), **Professional ORACLE** from **Oracle Corporation**

Recipe for

DESKTOP PUBLISHING DELIGHT

Main Ingredient:

1 JLASER PLUS (EMS memory board with combination printer/scanner interface)

Other Ingredients:

1 PC, XT, or AT style desktop personal computer

1 Canon-based 300 DPI laser printer

1 Canon IX-12 300 DPI scanner

Connecting cables

4 Banks of 256K RAM chips minimum. Total of 8 banks is optional if you like extra chips.

1 or more software programs that support JLASER or JLASER PLUS.

Directions:

Install JLASER PLUS with RAM chips in a single slot of the computer. Hook up scanner and laser printer with cables. Install desired software packages. Scan pictures of graphics. Mix with text and print out tasteful, professional-looking documents, newsletters, and graphic designs at full 300 DPI resolution and maximum speed.

Combined scanning and printing with JLASER PLUS. It lets you have your cake and eat it too.

Desktop publishing can be a piece of cake when you have the right ingredients. The quality of the ingredients will make all the difference. Don't be fooled by high-priced substitutes. Follow our recipe exactly. You'll be delighted with the results.

It makes desktop publishing a piece of cake!

Tall Tree Systems introduces another breakthrough in desktop publishing with JLASER PLUS. We've combined a 2 MB EMS memory board and an interface to both a Canon®-based laser printer and scanner. JLASER PLUS increases the performance of both devices and gives you a low-cost solution to the limitations you've been experiencing with them.

Furthermore, the same memory that is made available to your printer and scanner is also available for all your other conventional applications. You get system memory, expanded LIM memory, extended memory in an AT-type machine, RAM Disk and print spooler — all in a single slot!

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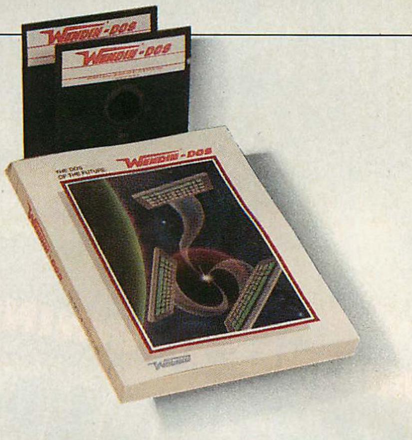
D—The Data Language from Caltex Software Ltd.



Wendin-DOS, a multiuser/multitasking operating system

takes advantage of the protected mode features of the 80286 and 80386 without waiting for IBM's announced Operating System/2 (OS/2). Professional ORACLE is a complete implementation of ORACLE version 5.1 and is compatible with ANSI SQL (structured query language) standard as well as IBM's SQL-based DB2. Using the protected mode of the 80286 and 80386, Professional ORACLE's DBMS kernel executes above the 640KB limit of DOS, allowing application programs and ORACLE tools to occupy as much as 500KB of standard memory.

Another product from Oracle is **LANserver ORACLE**, a dedicated, distributed multiuser DBMS for 80286 and 80386 PC LANs. The LANserver ORACLE kernel and data reside in one PC and can be accessed by applications and ORACLE tools running elsewhere on the LAN.

Networkstation ORACLE allows PCs to become true distributed application processors. The database can be either ORACLE or IBM DB2; it can reside on a minicomputer or mainframe and can be connected by asynchronous, 3270 coaxial, or Ethernet lines—all transparent to the application program running on the PC under Networkstation ORACLE. Professional ORACLE, $1,295; COBOL precompiler option, $395; network option, $395; LANserver ORACLE, $2,495; Networkstation ORACLE, $695.
Oracle Corporation, 20 Davis Drive, Belmont, CA 94002; 800/345-3267; in California, 415/598-8000

CIRCLE 325 ON READER SERVICE CARD

A relational DBMS (database management system) from **Caltex Software Ltd.** boasts mainframe-level capabilities. **D—The Data Language** supports data input, data manipulation, and data processing techniques. Characteristic of relational databases, data are entered and stored naturally, and all queries are made equally probable. Through a D developed scenario of Isolate-Arrange-Report, D isolates data into collections, arranges the data according to the user-specified criteria, and reports the data in a user-defined form. D allows importing of files from dBASE II, dBASE III, UNIX ASCII, DOS ASCII, and DIF. $550.
Caltex Software Ltd., 3131 Turtle Creek Blvd., Suite 1101, Dallas, TX 75219; 214/522-9840

CIRCLE 327 ON READER SERVICE CARD

A database library, **db/LIB**, is available from **Ingram Software**. The library is a set of assembly language procedures that give any Microsoft QuickBASIC application full relational database management capability. $99.
Ingram Software, Vertical Marketing Division, 900 W. Walnut Street, Compton, CA 90220; 818/985-3383

CIRCLE 326 ON READER SERVICE CARD

SOFTWARE DEVELOPMENT

An operating system that is compatible with DOS has been announced by **Wendin, Inc.** A self-bootable, multiuser, multitasking DOS replacement, **Wendin-DOS** supports all DOS commands and will run virtually all DOS applications. Based on the software architecture of the VAX/VMS operating system kernel, Wendin-DOS supports options such as multiuser shells. Wendin-DOS can automatically configure itself to support additional terminals through the TERMINAL command. A swapping feature allows more applications to run than can fit into memory. Wendin-DOS offers compatibility with any version of DOS via the VERSION statement. $99.
Wendin, Inc., P.O. Box 3888, Spokane, WA 99220-3888; 509/624-8088

CIRCLE 335 ON READER SERVICE CARD

With validated Ada compilers available for 80286 and 6800 computer architectures, **Alsys, Inc.** has announced an Ada compiler that exploits the protected mode on the Compaq Deskpro 386. The **Alsys 386 Ada Compiler** runs under DOS 3.1 and supports protected mode, allowing Ada applications to break the 640KB barrier of DOS. Direct access to as much as 16MB of main memory is supported. $3,095.
Alsys, Inc., 1432 Main Street, Waltham, MA 02154; 617/890-0030

CIRCLE 329 ON READER SERVICE CARD

An automatic knowledge acquisition system has been released by **IntelligenceWare**. Capturing the knowledge of an expert through interactive interviews, **Auto-Intelligence** distills the knowledge, then automatically generates an expert system. Rules are automatically generated. The expert systems generated by Auto-Intelligence can be executed with an inference engine and modified or embedded in other applications. Expert systems generated by Auto-Intelligence are royalty-free. $990.
IntelligenceWare, Inc., 9800 S. Sepulveda Blvd., Suite 730, Los Angeles, CA 90045; 213/417-8896

CIRCLE 330 ON READER SERVICE CARD

From **TurboPower Software** comes **Turbo Optimizer**, a series of three programs that make Turbo Pascal programs smaller and faster. By removing unused parts of the Turbo Pascal runtime library, the Turbo Compactor typically reduces medium-sized programs by 7KB. The Object Optimizer makes Turbo Pascal programs run as much as 30 percent faster by removing unnecessary instructions from compiled programs. The Object Librarian enables the storing of compiled versions of often-used procedures in an object library. $75; with source code, $125.

TurboPower Software also has revised **T-*Debug*PLUS**, the company's symbolic runtime debugger for Turbo Pascal. **Version 1.04** allows Turbo Pascal programmers to debug code in overlays and to access CPU registers and memory. Other improvements include

INTRODUCING PS/2 MEMORY EXPANSION FOR PEOPLE WHO THINK BIG.

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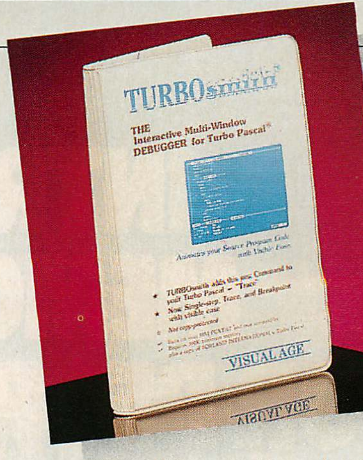
CIRCLE NO. 159 ON READER SERVICE CARD

Gold Hill Computers, Inc.'s GoldWorks expert system tool



TURBOsmith interactive debugger from Visual Age

easier customization of the debugger and a new MAKELST utility that creates a commented disassembly listing of Turbo Pascal programs. $60; upgrade, $10.
TurboPower Software, 3109 Scotts Valley Drive, Suite 122, Scotts Valley, CA 95066; 800/538-8157, ext. 830; in California, 800/672-3470, ext. 830 (orders); 408/438-8608 (information)
CIRCLE 331 ON READER SERVICE CARD

From **Gold Hill Computers, Inc.** comes **GoldWorks**, a building tool for developing and delivering knowledge-based expert systems on the Intel 80286- and 80386-based microcomputers. GoldWorks is a hybrid tool, combining a knowledge base; an inference engine that can reach conclusions using forward, backward, and goal-directed forward chaining; a multilevel, open architecture that provides developers with two programming and debugging environments based on their level of experience; external interfaces to Lotus 1-2-3, dBASE, and C; a screen toolkit for the quick design of end-user application screens; and on-line tutorials and help system. GoldWorks breaks the DOS-imposed 640KB barrier and can address up to 15MB of memory on the PC/AT, 14MB on the Compaq Deskpro 386, and up to 24MB on Gold Hill's 386 Hummingboard, a 80386-based, plug-in board. GoldWorks also runs on the IBM Personal System/2 models. $7,500.
Gold Hill Computers, Inc., 163 Harvard Street, Cambridge, MA 02139; 617/492-2071
CIRCLE 328 ON READER SERVICE CARD

A software library that implements an 8MB virtual-memory work space under DOS for programming in C is being offered by **Sapiens Software Corporation**. The library, **Sapiens V8**, requires no hardware support for virtual memory. The algorithm employed is a least-recently-used, demand-paging system. Each page contains 1KB of data and is organized into 128 64-bit words. The workspace is word addressable via a 32-bit structure containing page and address of the word. Macros and functions are provided to use this addressing schema. Swapping begins only when a predetermined number of pages have been allocated. This can be set at initialization from 1 to 64 pages. The work space can be configured from 1MB to 8MB. Each megabyte requires 8KB of physical memory. Included with Sapiens V8 is a set of libraries to assemble and use a virtual stack and heap. $300.
Sapiens Software Corporation, P.O. Box 7720, Santa Cruz, CA 95061-7720; 408/458-1990
CIRCLE 332 ON READER SERVICE CARD

A high-speed, source-code debugger for Turbo Pascal has been released by **Visual Age**. Based on CodeSmith-86 (the company's high-level assembly language symbolic debugger/disassembler), **TURBOsmith** runs as an invisible shell around the user's copy of Turbo Pascal, simply creating a new menu item on Turbo's main menu. The debugger provides four window types for different views into the Turbo Pascal code. TURBOsmith's Variable View Window allows viewing and changing of variables while a highlighted source-code statement is being executed, thus allowing a step through the program. $69.
Visual Age, 642 N. Larchmont Blvd., Los Angeles, CA 90004; 800/732-2345; in California, 213/534-4202
CIRCLE 333 ON READER SERVICE CARD

Designed to support the standard ANSI language, **BlackStar "C" Function Library** is available from **Sterling Castle Software**. BlackStar "C" is intended for Microsoft C 3.0 and 4.0, and Lattice C 3.0; it is adaptable to other C compilers. Among its 275 functions are device handlers for screen, graphics, keyboard, printer, and mouse; it also features interrupt, string, menu, date, time, and system functions. To optimize speed and memory usage, some functions are written in assembly language. $99.
Sterling Castle Software, 702 Washington Street, Suite 174, Marina del Rey, CA 90292; 800/722-7853; in California, 213/306-3020
CIRCLE 334 ON READER SERVICE CARD

A Prolog II artificial intelligence programming language from **ExperTelligence, Inc.** is available for the PC. **ExperProlog II** features the ability to implement infinite trees, or cyclic structures and the ability to freeze a predicate until all desired parameters are instantiated. First introduced for the Apple Macintosh, the ExperProlog II source code is PC compatible. $395.
ExperTelligence, Inc., 559 San Ysidro Road, Santa Barbara, CA 93108; 805/969-7871
CIRCLE 336 ON READER SERVICE CARD

A program has been developed by **MDS, Inc.** to create context-sensitive, on-line help screens for applications. **HELP/Control** consists of three parts: HELP/Generate, a help-screen compiler that reads screen definition files and writes the runtime help file; HELP/Runtime, a runtime module that interfaces to C (Microsoft and Lattice), BASIC (IBM), Pascal (Microsoft and Borland's Turbo), FORTRAN, COBOL (IBM and Realia), and assembly languages; and HELP/Popup, a stand-alone, application-specific help system. A separate utility is included to document dBASE (Ashton-Tate) and Lotus 1-2-3 applications. $125; HELP/Runtime source code, $125.
MDS, Inc., 160 Fox Street, P.O. Box 1237, Portland, ME 04104; 207/772-5436
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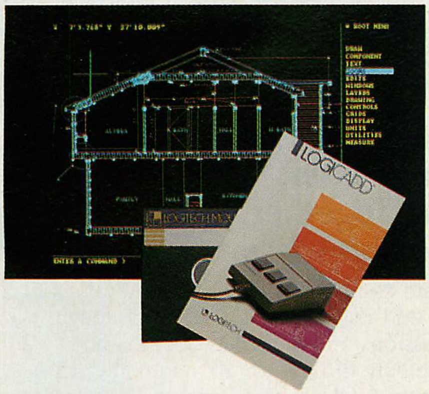

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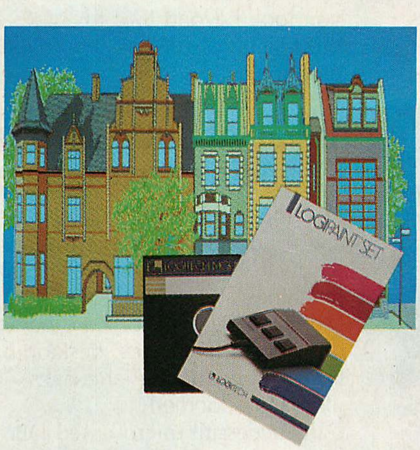

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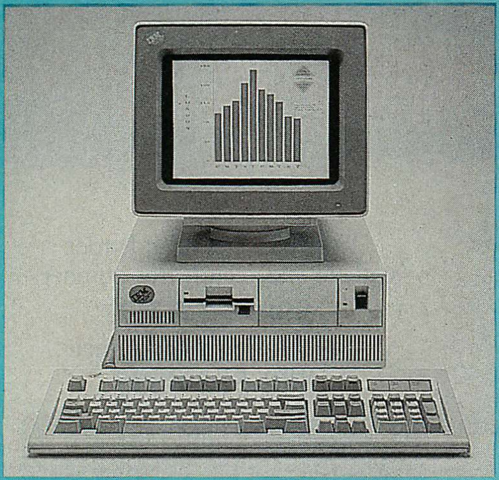
Join Us in September in San Diego to Tackle the Tough Systems Issues

Announcing the First Annual PC Tech Journal Systems Forum

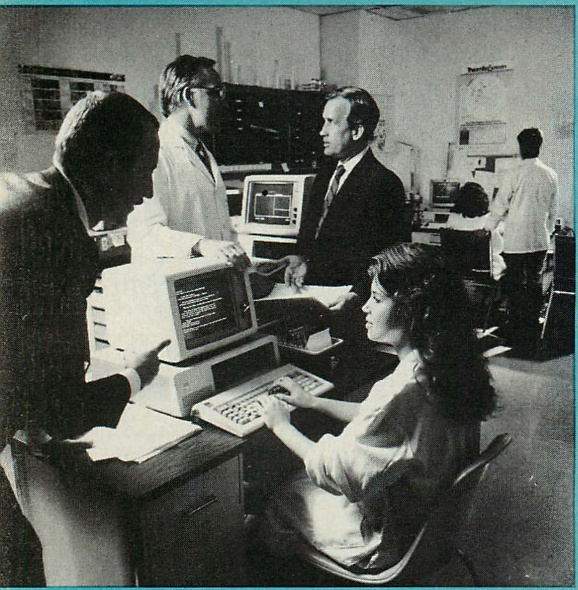


IBM Changes the Rules Again!

IBM challenges users and vendors alike to change what have become industry-standard computers and an industry-standard operating system. Whether or not you like the PS/2 workstations and now think you may need the undelivered benefits of the OS/2 operating system, your computer buying, development, and integration decisions will be affected by IBM's calculated risk.

What may have been prudent hardware and software decisions in March of 1987, may become dangerous by July. If you are involved in the selection, integration, and development of desktop computer products—particularly, if you operate in a connected environment—you probably have already begun to rethink your computing options for 1987 and beyond.

IBM has made a bid to recapture its market share by establishing new standards for desktop computing with higher performance machines and a new operating system (OS/2) with promised multitasking, multiuser capabilities, as well as integrated communications and an integrated SQL-compatible database.



Do You Need to Follow the Leader?

If AI/XT class machines and PC-DOS are soon to become obsolete, should you look beyond IBM for other advanced technology solutions? What about the Macintosh? What about UNIX—after all, it's already multiuser and multitasking?

What About Applications Development in a Changing Environment?

Desktop workstations will be at the heart of an increasingly complex applications development environment with different operating systems, different hardware systems, and an increasing need to link both like and unlike machines and software.

Moreover, applications are being built with powerful new tools: object-oriented/AI languages, desktop-based data management software. Are traditional programming languages—COBOL, FORTRAN, BASIC, and so on—ultimately doomed?

Can successful micro-based DBMS products migrate to the mainframe/mini universe or will the mainframe heavyweights such as Cullinet, Cincom, Oracle, etc. shove them aside as their own products migrate to the desktop computer?

The Systems Forum Brings User, Developer, and Integrator Organizations Together to Sort Through These Tough Systems Issues

Hundreds of members of the corporate computer community will join with manufacturers, developers, resellers, and consultants to tackle the tough issues in no-holds-barred panel discussions and audience question-and-answer sessions. You also will have plenty of time to talk informally with your peers who are building, integrating, and maintaining complex hardware and software systems. You can talk to the vendors whose products you are trying to make work, or which you may be considering for purchase.

Panel Discussions Will be Timely, Technical, Relevant, and Lively

Panel topics focus on real world problems that demand solutions. Your users, your clients, and your vendors share concerns about the best way to build, buy, and integrate desktop workstations within a connected environment. Stand alone issues are fading as multiuser and multitasking hardware and software reach the desktop. Here are some of the issues we'll be tackling:

1. *The PS/2: Rebirth of the IBM Standard.*

A horde of systems integration issues surround IBM's PS/2 workstations thanks to its new microchannel bus, its new graphics standard, and its 3½ inch diskette. Out with the old and in with the new? What is the short-term and long-term added value of the PS/2. Are clones still a viable alternative? What can add-on vendors add on?

2. *OS/2: Operating system of the 1990s?*

Is OS/2 the desktop operating system you've really been waiting for? Is it fast enough? Is multitasking enough? Will the compatibility box suffice for hundreds of DOS applications? Will new OS/2 applications offer enough value to justify an expensive conversion? Can you afford to wait until 1988 for release 1.0.

3. *The Macintosh: The Resurgence of an alternative standard.*

Has the Mac become a logical desktop choice in the corporate world? Do its new 32-bit architecture, open design, windowing, and inherent friendliness already exceed what's being promised by IBM and Microsoft for 1988 and beyond? Is IBM compatibility essential as long as you can communicate? Is Apple the only microcomputer vendor not hurt by IBM's new machines?

4. *UNIX: Not just for Techies anymore!*

It may be big and it may be complex, but it's already multiuser and multitasking—and its available now. On an 80386 machine equipped with UNIX do you really have an ideal platform for a host of workstation applications? Is UNIX the most intelligent applications bridge between unlike machines (no need to wait for APPC and LU 6.2)?

5. *Applications Development: Beyond 3rd Generation toward AI.*

Just how different are the new object-oriented/AI languages from COBOL, FORTRAN, C, BASIC, etc.? Are LISP, PROLOG, etc. necessary for expert systems? How are user companies building AI/expert system applications?

6. *Developing Applications in a Multiuser/Multivendor Environment.*

How do you build an application that must reside on more than one type and size of machine? What parts should fit where? How do you optimize performance in a connected environment? What is the ultimate developer's workstation?

7. *Optimizing LAN Performance.*

Getting acceptable performance from a local area network involves much more than hooking up the cables and installing the network software. Careful LAN selection is the first critical step and depends on the number and type of users, the intended applications, and the extent to which gateways and bridges are required. Once those choices are made, LAN tuning is critical.

8. *Linking Unlike Machines.*

IBM PC with PC-DOS to IBM PS/2 with OS/2 to IBM 370 with MVS to DEC VAX with UNIX to Macintosh to a 3-COM network to a Novell network. Making these kinds of connections is increasingly necessary—but still hazy after all these years. People, computers, data, and applications are widely distributed. IBM has some theoretical, announced and planned solutions—APPC, LU 6.2, SAA, SNA, and OS/2 extensions—but what are users and vendors doing right now to make the connections? What's blue sky and what's real world?

9. *Database Management on LANs.*

In principle, the number of MIPS available on the server and on individual desktops should yield impressive data management capabilities—rivaling multiuser micros, minis, and some mainframes. In fact, LAN and DBMS product limitations have greatly reduced the potential power of networked data management applications. What can you do right now to maximize DBMS performance? What new releases and new products will eliminate performance roadblocks?

10. *The Desktop-based DBMS as Production Database.*

Most PC-based data/file-management software in user hands is lightly used, if at all—and primarily as a simple file manager or decision support tool. But the best of the current database management products offer multifile/multiuser/transaction-processing capabilities. For companies of all sizes the potential exists to build powerful production applications with data management software that reside on PCs. Which products are worth considering? What are the limitations? What must be added to even the best DBMS products to give them full transaction-processing capability?

Panelists will include members of both the vendor and user community chosen for technical competence and real world experience—professionals like you. Here's a partial list of panelists already committed to participating in the SYSTEMS FORUM:

From User Organizations:

- Steve Ikard, Mgr. Advanced Systems Grp., Wells Fargo Bank
- Laurie Antonell, Dir. Systems and LANS, Merrill Lynch, Capital Mkts. Div.
- Mike Johnson, PC Systems Mgr., PC Systems Support Grp., Transok, Inc.
- Dr. James Nestor, Sr. Mgr. R&D, Ernst & Whinney

From Manufacturer/Publisher Organizations:

- Philippe Kahn, Pres., Borland Intl.
- William Casey, Div-Vice Pres., Product Architecture, Cullinet Software Corp.
- Alan Ashton, Pres., Word Perfect Corp.
- Steve Ballmer, Vice Pres., Microsoft Corp.
- Craig Burton, Vice Pres.-Mktg., Novell
- Safi Qureshey, Pres. & CEO, AST Research
- Chuck Hickey, Pres., Microport Systems, Inc.
- Peter Gabel, Pres., Arity
- Nat Goldhaber, Pres., Centram Corp.

From VAR/Reseller/Consultant Organizations:

- Mark Freund, Vice-Pres., Interconnect
- Rick Watkins, Co-Founder, Accelerated Learning Center

So join us in San Diego September 23, 24, and 25 at the Sheraton Harbor Island—We've got a lot to talk about.

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TECH NOTEBOOK 78

JOHN T. COCKERHAM

The Mouse-EGA Interface

The IBM Enhanced Graphics Adapter register interface allows proper screen handling in response to mouse activity.

Programs that use the mouse while an IBM Enhanced Graphics Adapter (EGA) operates in high-resolution-graphics display modes (EH, FH, and 10H) must manipulate the EGA registers in response to user actions, such as moving the mouse or pressing the buttons. After the program processes the mouse event, it must restore the registers to their state before the event. Because the EGA registers are write-only, the state of the registers when the event occurs cannot be easily determined. Therefore, the EGA interface portion of all currently available mouse drivers maintains images of the EGA's registers, called *shadow maps*.

The shadow maps provide a central repository for data reflecting the EGA's state. The EGA register interface intercepts all regular BIOS-video calls (interrupt 10H) that change the video-display mode, and it also updates the shadow maps accordingly. However, it does not intercept the video-service call that sets the color palette (AH = 0BH). Recording the color palette in the shadow map requires using the write-register-set function (AH = F5H).

When setting hardware registers to change the EGA's state, the program calls interrupt 10H specifying the appropriate interface function in AH after loading the appropriate values in the other CPU registers (as listed in table 1). Table 2 shows the possible values for the port-number parameter required by most of the functions. Care must be taken with the values passed to the interface because it performs no validation before writing the value to the EGA hardware.

John T. Cockerham, M.D., is a cardiologist at The Children's Hospital in Boston and is on the faculty of Harvard Medical School.

TABLE 1: *Interface Functions*

AH = F0H (READ SINGLE REGISTER)

Input	**Output**
BH = 0	BL = Data
BL = Pointer for pointer/data chips	
DX = Port number (see table 2)	

AH = F1H (WRITE SINGLE REGISTER)

Input

BH = Data for pointer/data chips
BL = Pointer for pointer/data chips
  Data for single registers
DX = Port number (see table 2)

AH = F2H (READ CONSECUTIVE REGISTER RANGE)

Input	**Output**
CH = Starting pointer value	ES:BX = Filled with 1-byte entries for range
CL = Number of registers	
DX = Port number (see table 2)	
ES:BX = Table	

AH = F3H (WRITE CONSECUTIVE REGISTER RANGE)

Input

CH = Starting pointer value
CL = Number of registers (>1)
DX = Port number (see table 2)
ES:BX = Table of 1-byte entries for range

AH = F4H (READ REGISTER SET)

Input

CX = Number of registers
ES:BX = Table of records
Bytes 0 and 1 = Port number (see table 2)
Byte 2 = Pointer value
Byte 3 = Filled in by read

AH = F5H (WRITE REGISTER SET)

Input

CX = Number of registers
ES:BX = Table of records
Bytes 0 and 1 = Port number (see table 2)
Byte 2 = Pointer value
Byte 3 = Data to be written to register

AH = F6H (REVERT TO DEFAULTS)

Input

None

AH = F7H (DEFINE DEFAULT TABLE FOR CHIP)

Input

DX = Port number (see table 2)
ES:BX = Table of entries for all registers

AH = FAH (INTERROGATE DRIVER)

Input	**Output**
BX = 0	BX = 0 if driver not present
	ES:BX = Pointer to version number

TABLE 2: *Port Number Parameters*

0H	CRT controller (3X4H)
8H	Sequencer (3C4H)
10H	Graphics controller (3CEH)
18H	Attribute controller (3C0H) Valid for single register calls only
20H	Miscellaneous output register (3C2H)
28H	Feature control register (3XAH)
30H	Graphics position 1 (3CCH)
38H	Graphics position 2 (3CAH)


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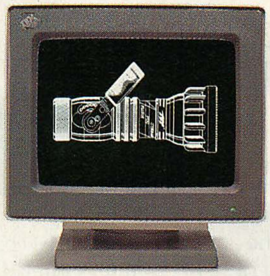
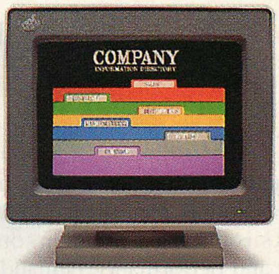


The IBM Personal System/2 Monochrome Display 8503.



The IBM Personal System/2 Color Display 8513.

The IBM Personal System/2 Color Display 8512.

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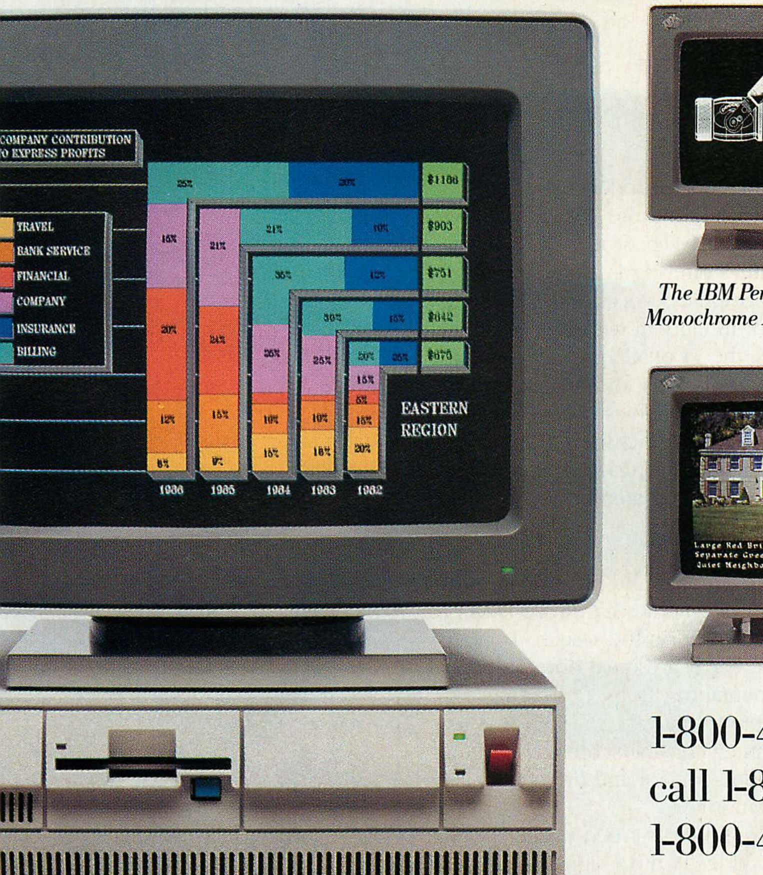

The IBM Personal System/2 Model 50 and the IBM Personal System/2 Color Display 8514.

Graphics Intelligence

Dedicated processors are bringing unprecedented speed and sophistication to PC graphics.

ED McNIERNEY

The increasing demand for high-resolution, sophisticated PC graphics is placing a premium on the quality and performance demanded of graphics displays, which play a critical role when evaluating an entire PC system. Because graphics display and management are now too complex to remain part-time tasks for the 8086-family CPUs, special-purpose processors designed to manipulate graphics have begun to appear on the market.

These "intelligent" graphics processors add a new level of complexity to the design of graphics hardware and low-level graphics software, and allow the developer to harness a subsystem of unprecedented speed and sophistication—essentially an independent graphics computer inside the PC. This subsystem provides a graphics environment more flexible and powerful than the current field of "unintelligent" graphics display adapters represented by the IBM Enhanced Graphics Adapter (EGA).

In this issue, *PC Tech Journal* explores the field of intelligent graphics processors with three articles, beginning with an overview of how the new processors have evolved, immediately followed by individual reviews of two of the first such products: the Intel 82786 (p. 56) and the Texas Instruments (TI) TMS34010 (p. 68).

Intel's offering is a highly integrated graphics processor that can easily work in tandem with Intel microprocessors; the TI product is actually a microprocessor itself, the first designed expressly for graphics processing. The distinction made between graphics processors and microprocessors is in their ability to be programmed: a microprocessor can be programmed whereas a graphics processor cannot.

The primary and most obvious function of graphics hardware is to produce a picture on the screen. To do this, the hardware must provide two fundamental functions: translating display memory into the color and intensity of pixels on the screen, and generating video-control and timing signals for the monitor.

The physical-screen image is generated by video-control signals based on a fundamental constant known as the *pixel* or *dot rate*—the number of pixels generated by the graphics system each second. Because most display monitors are not static, the screen image must be refreshed frequently, typically between

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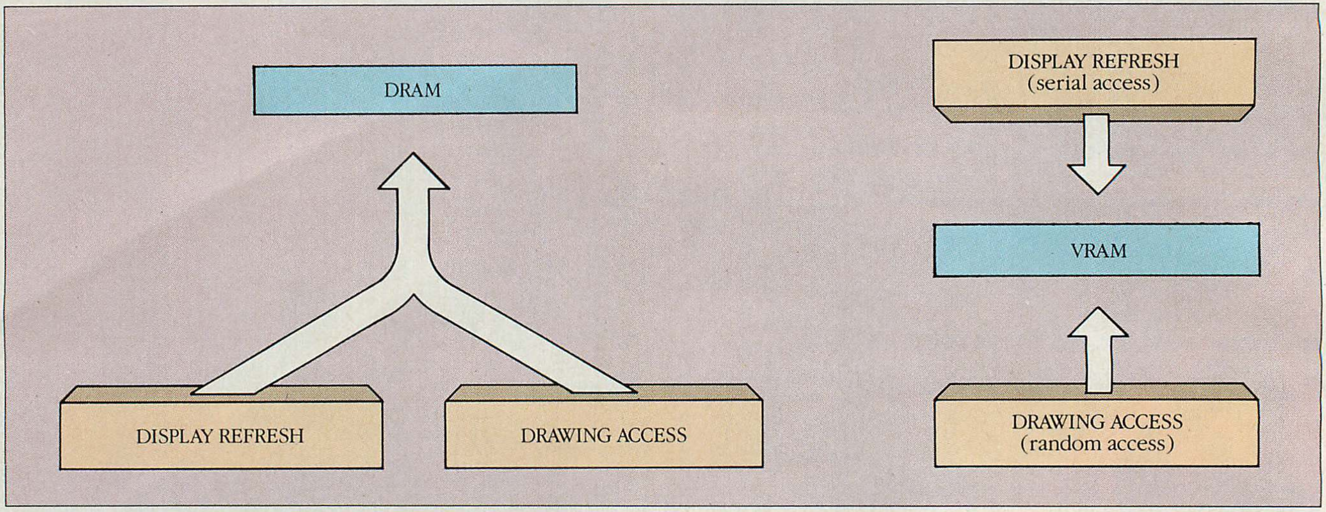
IBM
Personal Computer AT

FIGURE 1: *DRAM versus VRAM*



Dynamic RAM (DRAM) chips force the display refresh and CPU drawing to share a single path to memory. Dual-ported RAM used as video RAM (VRAM) allows the refresh and CPU accesses to occur without any interference from each other.

50 and 70 times a second. To complete one refresh cycle, each pixel on the screen must be extracted from graphics memory and sent to the display. Multiplying the number of pixels visible on the screen at any given time by the number of refresh cycles per second yields the pixel rate.

All video-timing signals provided to the monitor are based upon this fundamental clock; for an EGA in 640-by-350 mode the clock rate is 16.257 MHz. (The pixel rate is not the same as the system's *drawing rate*—the rate at which pixels in the display memory can be modified; an EGA in 640-by-350 mode transmits 16,257,000 pixels every second, even when the image on the screen is not changing.)

In addition to the pixels generated for screen display, the EGA produces almost 3 million *pixel ticks* per second; these do not display data on the screen. Pixel ticks are not real graphics data taken from memory, but rather are ticks of the pixel clock used by the monitor to generate time for other purposes. For example, an electron beam generates the image on the display monitor by scanning the screen from left to right and top to bottom. The beam takes time to jump back to the left edge and to the top of the screen after scanning a line or screen. This process consumes extra pixel ticks at the beginning and end of each line and at the top and bottom of each screen refresh. (For information about the monitor's operation, see "Synchronizing Graphics Standards," John C. Blair, Jr., May 1987, p. 146, and "Instant Screens," Augie Hansen, June 1986, p. 96.)

Each horizontal scan line consists of four portions, running from left to right across the screen: the horizontal back porch, the active-video period, the horizontal front porch, and the horizontal-synchronization signal. All portions except the active video period are used to move the beam to the next position for scanning. For the EGA in 640-by-350 mode, each horizontal scan line consumes 736 ticks of the pixel clock; of these, 640 are used for the active display of graphics data.

The four phases of the horizontal signal have exact counterparts in the vertical signals. Horizontal and vertical signals differ only in their units of measurement: horizontal signals are measured by the pixel clock; vertical signals are measured by scan lines.

For most monitors, however, the critical factor in these signals is their frequency of occurrence, not the number of pixels or scan lines they represent. A display adapter running at twice the pixel rate of the EGA could double the number of pixels in each horizontal scan period, obtaining a 1,280-pixel line on the same monitor, even though the actual display capabilities of the CRT's phosphor or shadowmask may be exceeded at that resolution.

RAM ARRANGEMENTS

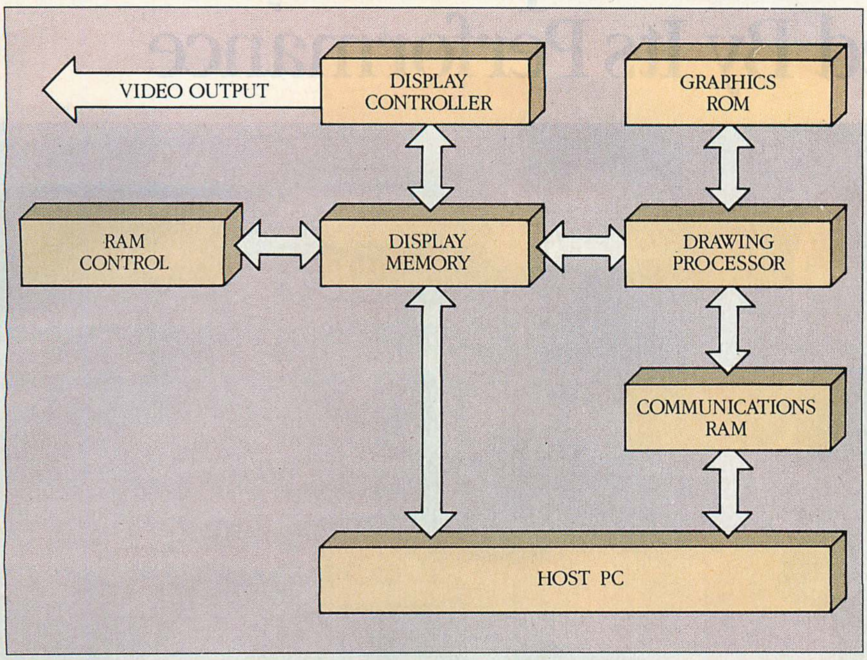
To display a screen image, a graphics system must have sufficient RAM to hold one screen of pixel information. This RAM must be readable and writable by the host CPU or the graphics processor and also be available to refresh the display. Any memory configuration that meets these requirements can be used in a display device. In addition, various memory arrangements should be provided for particular needs, such as an 8-bit or 16-bit data path to memory or maximum-burst access rates.

Although a variety of memory layouts is used to provide maximum performance, the fundamental distinction between graphics-memory systems is in the type of device used: either video RAM (VRAM) chips or conventional dynamic RAM (DRAM) chips. Figure 1 illustrates the difference between the two types. Traditionally, the RAM devices most commonly used were static RAM chips. More recently, DRAMs have become the memory chip of choice; they are found not only in the most popular graphics boards (such as the EGA and Hercules Graphics Card) but also in both standard PC system memory and expansion memory.

DRAMs can be accessed by only one external device at a time. This works well when system memory is being used only by the CPU. When a DRAM is used in a graphics board, however, it must be shared by two competing devices: display refresh and the CPU or graphics processor. In this case, the processor and display refresh must take turns accessing the display memory, with display refresh usually having priority: although the processor can be made to wait its turn by inserting wait states, any delay in refreshing the display would result in unacceptable disturbances on the monitor.

For most devices with lower resolutions than the EGA's, taking turns is not a problem because the bandwidth required to refresh the display is low

FIGURE 2: *Typical Graphics Processor*



An operation of a typical graphics processor is illustrated in this simple block diagram. Several of these functional blocks could be combined in a single component.

enough to be almost transparent to the processor. With increases in the display's resolution and *pixel depth*—the number of bits used to define the pixel—the demands placed on the DRAM increase proportionally. In high-resolution displays this demand can be more than 80 percent of available memory bandwidth, resulting in unacceptably slow access times for drawing and otherwise modifying display memory. If DRAMs were used in intelligent graphics systems, the performance gain produced by the graphics processor would be almost, if not entirely, outweighed by the limited amount of time available to the processor for drawing.

VRAMs, which TI designed to solve this problem, have a *serial* port and a *random* port for accessing memory. Both ports may be used at the same time, with each one having almost 100 percent access to the memory at all times. Because display-refresh systems require that pixel data be read from memory sequentially, the serial port is for display refresh. Because drawing and other graphics operations need not be accessed in order, the random port is used for the CPU and graphics processor. In this way, the processor can run at almost full speed, unhindered by memory limitations.

However, VRAMs are much more expensive than conventional DRAMs and are not available in high-density packages; the current commercially available DRAMs provide densities of 1 Mbit per chip, while VRAMs are still limited to 256 Kbits per device. These two factors tend to restrict the use of VRAMs to high-performance, high-resolution display systems.

COMMUNICATING WITH THE HOST

A processor-based graphics system must be able to transfer or share data between the host CPU and the graphics processor and to allow the two to interrupt each other. Although the processor may have its own memory, or even its own processor, it is useless as an independent system; it must be able to communicate with the host CPU to draw in display memory, send video-control parameters and drawing commands to the system, and read back information about the state of the system (see figure 2). Because most graphics processors have no independent drawing capabilities, the host CPU needs full access to display memory to perform any drawing operations at all. However, most video-control functions, such as setting synchronization rates and cursor positions, are read from and written to addresses in the host CPU's I/O space.

The Intel microprocessors used by IBM offer PC-based graphics a choice of memory-mapped or I/O-mapped communications. Most graphics systems use a combination of both methods: the display memory is mapped directly into the host CPU's address space, and the control and configuration functions are mapped into its I/O addresses.

In EGA systems, I/O mapping is used for a variety of access-control registers that set Boolean writing modes and plane masks that write-protect certain *bitplanes*, areas in which bits are stored according to their values. When the host CPU reads and writes from the memory-mapped display space, the data are modified dynamically by the EGA according to the current state of its control-register set. Although combining systems adds power to the graphics processor and partially offsets the problems of sharing one port between the CPU access and display refresh, the end result is complex and has made writing software for the EGA difficult.

Some intelligent graphics systems, such as IBM's Professional Graphics Controller, do not require—or permit—the host CPU to draw directly in display memory. Instead, the interface is memory-mapped but command-driven; the PC writes drawing commands to an on-board command buffer where they are read and interpreted by the graphics processor. Although these controllers greatly reduce the work load of the host CPU, they also restrict the types of drawing available.

Graphics processors are now available that receive commands for on-board execution, but still map display memory into the PC's address space for maximum flexibility. If an application requires a graphics primitive not provided in the processor's hardware, the CPU can synthesize the primitive by drawing directly in display memory.

Any system that supports multiple microprocessors must also provide for asynchronous communications. Memory-mapped and I/O-mapped techniques work well for the synchronous transfer of commands and data, but an interrupt mechanism must be provided so that each system can alert the other. Interrupts can be triggered by any number of events: an error requiring immediate attention; results becoming available from an asynchronous operation; or attainment of a desired state that is meaningful to the other processor.

The IBM EGA has a vertical-retrace interrupt that signals the host CPU at the end of each frame of the display. This type of interrupt is useful in animation or in timing a graphics event without depending on the speed of the host CPU. The PC provides a set of interrupt-request (IRQ) lines for this purpose: IRQ 2, 3, 4, and 5 on each expansion bus connector trigger interrupts 10, 11, 12, and 13 respectively.

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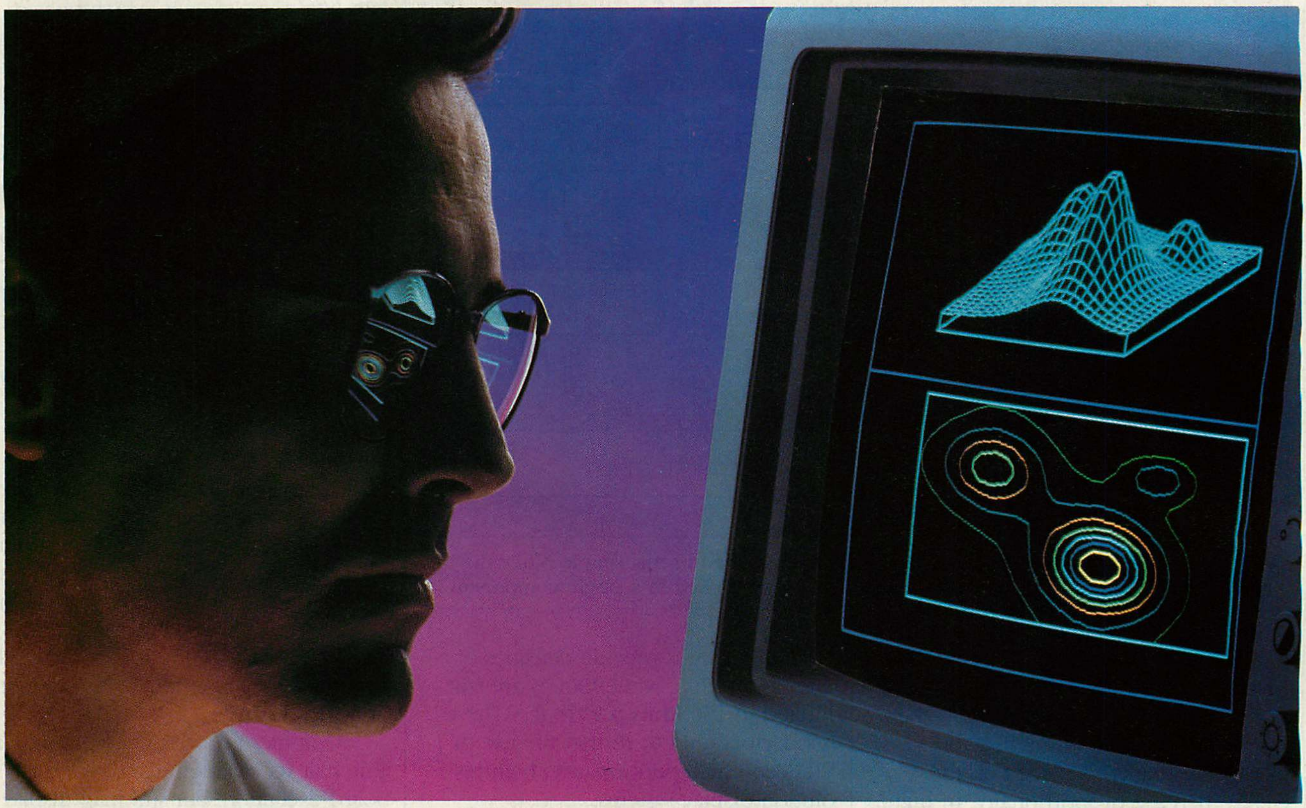

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Because such a limited range can become crowded, most devices that can generate these interrupts are identified by an interrupt-source signature. When an interrupt handler gains control, it checks the signature on the device it intends to service to determine whether that device generated the interrupt. If the signature is not found, the handler assumes another device caused the interrupt and passes control to the next handler in the chain.

An intelligent graphics system also requires an interrupt signal that flows in reverse, from the CPU to the graphics processor. For example, a paint application on a high-resolution screen may allow the user to fill in a selected area. If the user selects an incorrect starting point and begins filling the wrong area, the PC could interrupt the operation and instruct the processor to recover and undo the fill. Because the PC expansion bus does not have a general-purpose interrupt interface to a graphics board, the board can generate an internal interrupt signal in response to a command written by the host CPU.

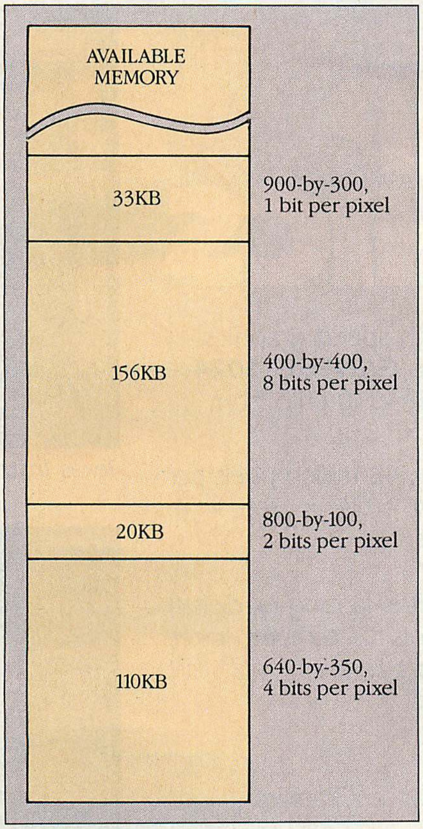
POWER-UP STATES

Because a graphics processor is essentially a stand-alone microcomputer, a hardware designer should consider the power-up state of both the processor and the host CPU. Minimum acceptable performance dictates that the start of display-synchronization signals and display refresh on the processor synchronize with initialization of the host CPU to protect the monitor.

For graphics systems without true microprocessors, these two steps often are all that are necessary. Systems that require special initialization by the PC can be provided with ROM that the PC executes during power-up. The EGA contains such a ROM that revectors and extends the normal video BIOS services of interrupt 10H. The BIOS searches for such extended-video ROMs and transfers control to them as part of the normal start-up process.

If the graphics system contains a microprocessor, it must start up in a halted state or have on-board ROM. Either the ROM can be limited, allowing the microprocessor to initialize the remainder of the system, or it can provide the microprocessor with a full graphics-command set—or even an operating system. Most processors with limited ROM have additional program memory into which software can be loaded dynamically by the host CPU.

FIGURE 3: *Bitmap Allocation*



Each bitmap has an independent size and pixel depth and may be located anywhere in the processor's memory.

An intelligent graphics system presents a more complex software environment than does a simple frame-buffer display. Applications developers must rethink old assumptions that, while useful in Color Graphics Adapter (CGA) or EGA environments, are no longer valid in intelligent graphics systems. Software will be as flexible as the graphics system, and thus will be applicable in a variety of graphics devices.

In developing software for intelligent graphics systems, it is convenient to consider display memory in terms of *bitmaps*—contiguous regions of memory that represent to the graphics system rectangular areas of specified pixel depths (see figure 3). Conventional display systems are rigid and modal in addressing and interpreting graphics memory: setting the current display mode determines the display resolution, size, and pixel depth for all bitmaps. In conventional systems, all these variables are interdependent—the settings then can be changed only by selecting another mode.

Intelligent systems, however, allow different bitmaps not only to have different *X* and *Y* dimensions, but also to vary in pixel depth. Text data can be stored as monochrome information: menus and selection screens might be stored at 4 bits per pixel for 16 colors, and the application's main display at 8 bits per pixel. The graphics processor understands each pixel depth and can mix operations freely on bitmaps.

In simpler display systems, such as the CGA or EGA, each page of display memory can be considered a separate bitmap. These systems are inflexible in using bitmaps; no provision exists for changing bitmap size, and pixel depth is fixed at the current display depth. Use of display memory not on screen is limited, if not impossible.

None of these restrictions applies to intelligent graphics systems. Display memory, which may be several megabytes in size, is typically much larger than the amount required to display one screen image and can be broken into a number of logical bitmaps, each providing a separate drawing area. Graphics memory can be handled as easily as system memory, with allocation and deallocation giving flexible access to data and drawing areas.

In designing any graphics system, the display data are also considered in terms of the physical pixel, including both its position on the screen and its value, or color. Memory can be stored either in a packed-pixel format in which all bits of a pixel are stored in the same byte or word of memory, or as bitplanes according to bit value.

Storing by bitplanes is becoming less popular as more intelligent graphics processors come into use; it makes more sense for a pixel-oriented processor to manipulate contiguous blocks of data. If the packed-pixel organization is used, then the order of bits within a packed pixel also must be determined: is the low-order bit sent to the display first or last? At a higher level, when the graphics system is designed, the order of pixels within a byte or a word must be decided as well.

These variables produce two effects: a graphics processor must be at least flexible enough to match the needs of a particular design, and it must be able to manipulate data by pixels instead of bytes or words as in the conventional CPU. Fortunately, the latest generation of graphics processors addresses both issues, allowing the applications developer to work in pixels and *X-Y* coordinate addressing.

VALUE AND COLOR

Pixel data are subject to intermediate modification before being displayed on the monitor. Low-resolution displays such as the CGA interpret pixels as

6 MIP GRAPHICS

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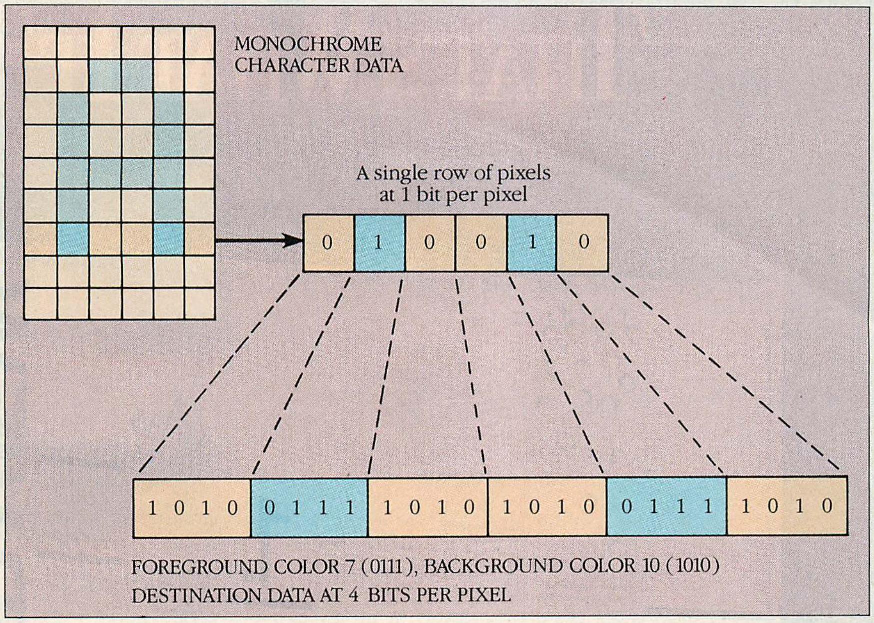
physical colors; a pixel of a particular value always appears on-screen as the same color. In the slightly more powerful EGA, the four bits used for each pixel do not represent a physical pixel value but are used instead as indexes into a look-up table of 64 possible colors. The appearance of the entire display can be changed merely by modifying the look-up table, without changing any pixel data (see figure 4).

FIGURE 4: *Look-up Tables*



Look-up tables allow graphics memory values to represent indexes into the tables rather than actual colors. The display can be changed by modifying the table.

The use of look-up tables greatly increases the flexibility of a graphics system. Offering high pixel depths for several thousand simultaneous colors is difficult and expensive, but most applications need only a few colors if these can be selected from a wide range. For example, a computer-aided design (CAD) system executing a wireframe drawing might require 16 distinct colors to identify various components, but the same system displaying a solid, shaded model might require 16 shades of the same color to render the same part realistically. A look-up table can easily provide 16 million colors from which to choose, providing powerful flexibility at relatively low cost.

Because an intelligent graphics system can manipulate data at a variety of pixel depths, the data must be converted from one pixel depth to another. This conversion is often used when drawing text on a color bitmap. Typically, text is stored in a monochrome bitmap, where each bit represents one pixel of the character—the actual display data may have four bits per pixel. The display-processor hardware can convert the bitmap to color by using programmable foreground and background colors, as shown in figure 5.

In copying the text from the monochrome source, information is read one bit (one pixel) at a time and inspected at any time by the processor. If the pixel has a value of 1, the currently defined foreground color is substituted for the source pixel and is written to the destination bitmap at its pixel depth. If the source pixel is 0, the background color is used. Color conversions between two bitmaps with pixel depths greater than one bit per pixel are not well defined. Such conversions are not as sophisticated as monochrome-to-color conversions and are accomplished either by truncating bits from a pixel value or by adding bits from within the application to fill out the pixel to the required destination depth.

Although its uses are less obvious than color expansion, color contraction is also helpful. For example, by contracting color on a display bitmap, a less-dense copy can be produced that retains a large amount of the original graphics information. A page-scanning system might be capable of scanning an image into 256 colors at 300 dots per inch on the display. At the required 8 bits per pixel, the entire image would require more than 8MB of storage for a single scanned sheet. By contracting the color as the image is scanned, pixels that match a chosen foreground color can be converted to 1s and all others can be converted to 0s. The result is a recognizable image that requires only 1MB of storage. The user can then view the decolorized image, select a small area of interest, and instruct the scanner to rescan the desired area at full color.

INDEPENDENT ALGORITHMS

An attractive feature of intelligent graphics processors is their ability to execute graphics algorithms independent of the host CPU. Lines, circles, ellipses, polygons, and filled areas all can be drawn without assistance or intervention. By providing these algorithms in the hardware, the graphics system frees the applications developer from such details.

Graphics processors handle drawing in one of two ways: either by algorithms designed into the hardware or by user-defined programs that implement algorithms. Algorithms designed into the hardware execute faster than software implementations. On the other hand, if the algorithms provided in the hardware are unacceptable for the current task, the functionality of the hardware cannot be extended and the host CPU must handle the task.

The software approach allows the user to design algorithms to suit an application's particular needs. If the application grows, the graphics support provided by the processor can grow with it. Although this method requires a greater investment of software development time at the start of a project, it can lead to the greatest possible graphics performance, but not necessarily the greatest speed. In effect, the host software can operate as if it had a graphics board designed exactly to its specifications; no command conversion is necessary, and the amount of information transmitted to and from the board is kept to a minimum.

As the graphics processor attempts to meet the host CPU's graphics needs, some degree of synchronization between the two is required. This synchronization is especially important in two areas: user interaction and host CPU assistance. Interactive graphics systems are demanding and unforgiving; when the user moves a mouse or other input device, the results must appear instantaneously. Although most graphics processors are capable of drawing fast enough to satisfy these needs, intermediate buffering of graphics commands may interfere. The host not only must be able to force an update of the display, but also must be able to interrupt a fill operation, move an on-screen cur-

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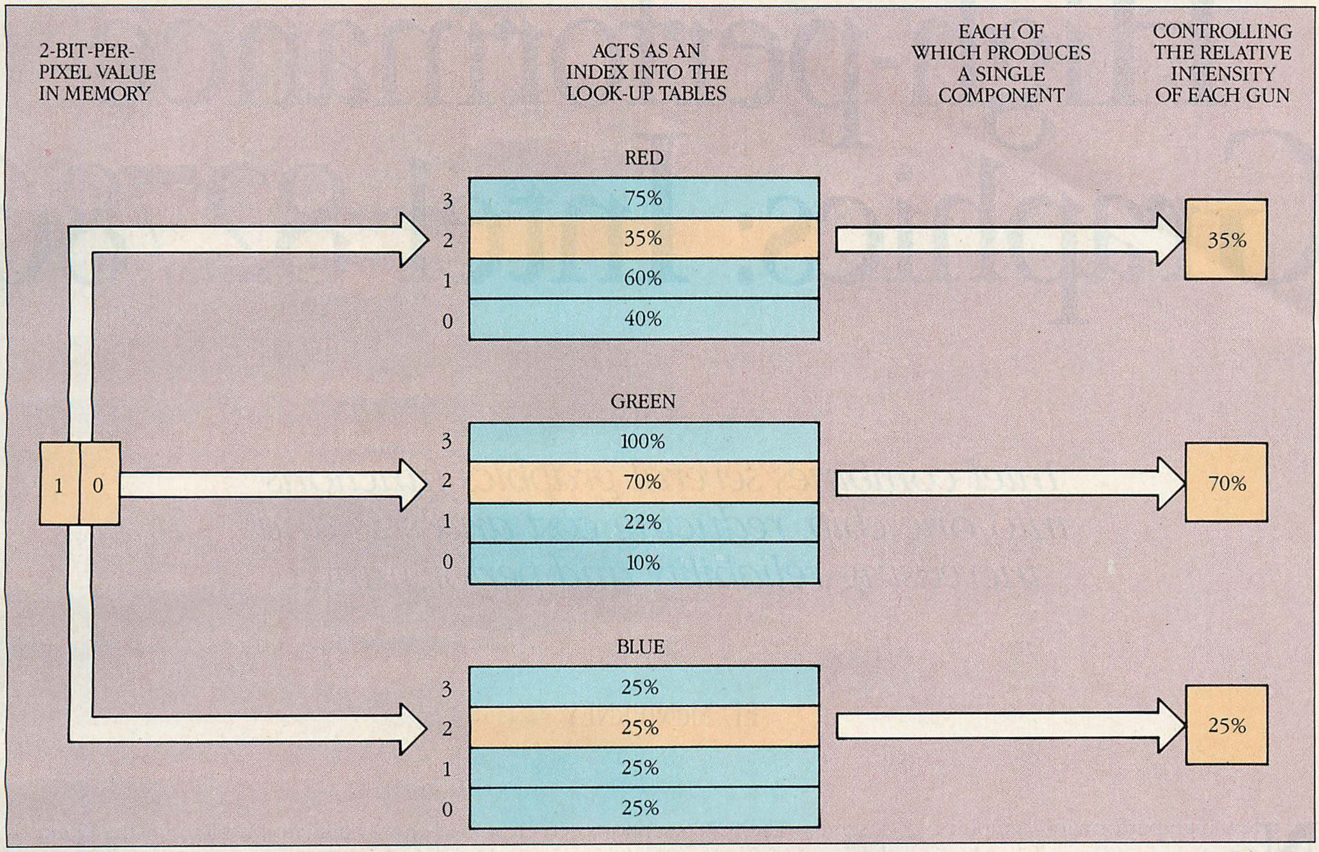
FIGURE 5: *Color Conventions*



	RED
3	75%
2	35%
1	60%
0	40%

	GREEN
3	100%
2	70%
1	22%
0	10%

	BLUE
3	25%
2	25%
1	25%
0	25%

Monochrome data that are stored where each bit represents one pixel of the character can be copied to a multiple-bit-per-pixel bitmap by expanding the bits that are set to 0 to a background color and 1-bits to a foreground color.

sor in response to user input, and then resume the fill. Careful design of the graphics system can maximize the total graphics performance while giving immediate feedback to the user.

Far more host-CPU assistance is required when the graphics system does not include a programmable microprocessor. In such cases the host CPU not only must have memory-mapped access to the display buffer, but also must work with the graphics processor because the two operate asynchronously.

For example, if a user draws an overlapping rectangle and circle, and the graphics system requires assistance to draw the circle, the host CPU must be certain that the rectangle has been completely drawn before attempting to draw the portions of the circle that intersect the rectangle. Usually, the host CPU simply waits for the graphics processor to become idle, but a well-designed interrupt mechanism can allow the host to attend to other operations and then be alerted by the graphics system when the drawing is complete. For maximum performance, graphics data and drawing commands should be transferred between the host CPU and the graphics processor with a minimum of overhead and delay.

The graphics processor often can work so quickly that most drawing operations are performed faster than the host application can request them. However, transferring image data, large bitmaps, complicated command streams, or large amounts of applications software can place a heavy burden on the communications channel between the host CPU and the graphics processor. Even direct memory-to-memory transfers are limited by the speed of the expansion bus.

Well-designed systems minimize data transfer by building complex graphics operations from available primitives. These systems take advantage of the operations that contain the greatest semantic content in the smallest quantity of data. Instead of requiring the host PC to move large amounts of data back and forth, an intelligent graphics system can implement an operation such as "drag the icon smoothly to point *X,Y*." In less than a dozen bytes of information, the host CPU can cause a complex operation to be performed by the graphics system.

GRAPHICS POWER

Graphics processors have increased flexibility in PC graphics systems, allowing them to compete with expensive graphics workstations. Intelligent graphics systems incorporating these special-purpose processors will soon dominate the PC marketplace. A solid understanding of their features will enable hardware and software developers to make maximum use of their powerful capabilities. In particular, display control, drawing performance, and host CPU communications are critical in determining a processor's applicability and power in a PC graphics system.

Each graphics processor or microprocessor has its own strengths, which should be considered in terms of the intended use of the graphics system. Attempts to discriminate on the basis of display resolution or drawing speed alone oversimplify the issue and obscure the significance of intelligent, programmable graphics systems that can be highly tuned to meet an application's precise display requirements.

Ed McNierney is director of software development at Number Nine Computer Corp.

High-performance Graphics: Intel 82786

Intel combines several graphics functions into one chip, reducing cost and size and increasing reliability and performance.

ED McNIERNEY

New high-performance graphics processors, once restricted to professional workstations and expensive PC graphics controllers, are now generally available for business, design, and home applications. As prices have dropped, demand has increased for sophisticated graphics processors such as the Intel 82786.

Intel's new graphics processor, which lists for $198, is a highly integrated component that, in one chip, provides graphics-display functions that traditionally have required discrete components or external microprocessor support; this not only lowers the cost and size of the processor, but also increases its reliability and performance.

The Intel 82786 is packaged as an 88-pin, ceramic pin grid array. Power, ground, and external-control signals are supplied to it, and address and data lines for controlling graphics memory are provided as outputs. Video signals can be configured either as outputs or as inputs slaved to an external video-synchronization source.

The 82786 executes many drawing operations and provides sophisticated hardware windowing. These windows allow the placement of any portion of graphics-display memory onto any portion of the screen, entirely eliminating traditional hardwiring between display addresses and pixel positions on the screen. The 82786 supports screen resolutions of 640-by-480 pixels at eight bits per pixel, and even higher resolutions if display depth is reduced. Multiple 82786 processors can be combined in applications requiring high resolution and color depth.

For example, an 82786 implementation might include one or more megabytes of dynamic RAM (DRAM), the 82786 itself, normal palette and output support, and a small amount of ROM. Because the 82786 executes graphics using fixed commands, relatively little ROM is needed. A much larger amount (32KB or more) of host-computer ROM may be included in the system for such uses as a subroutine package for calculating display parameters or constructing graphics-instruction sets. This kind of implementation is particularly well suited to a multitasking text and graphics workstation arrangement.

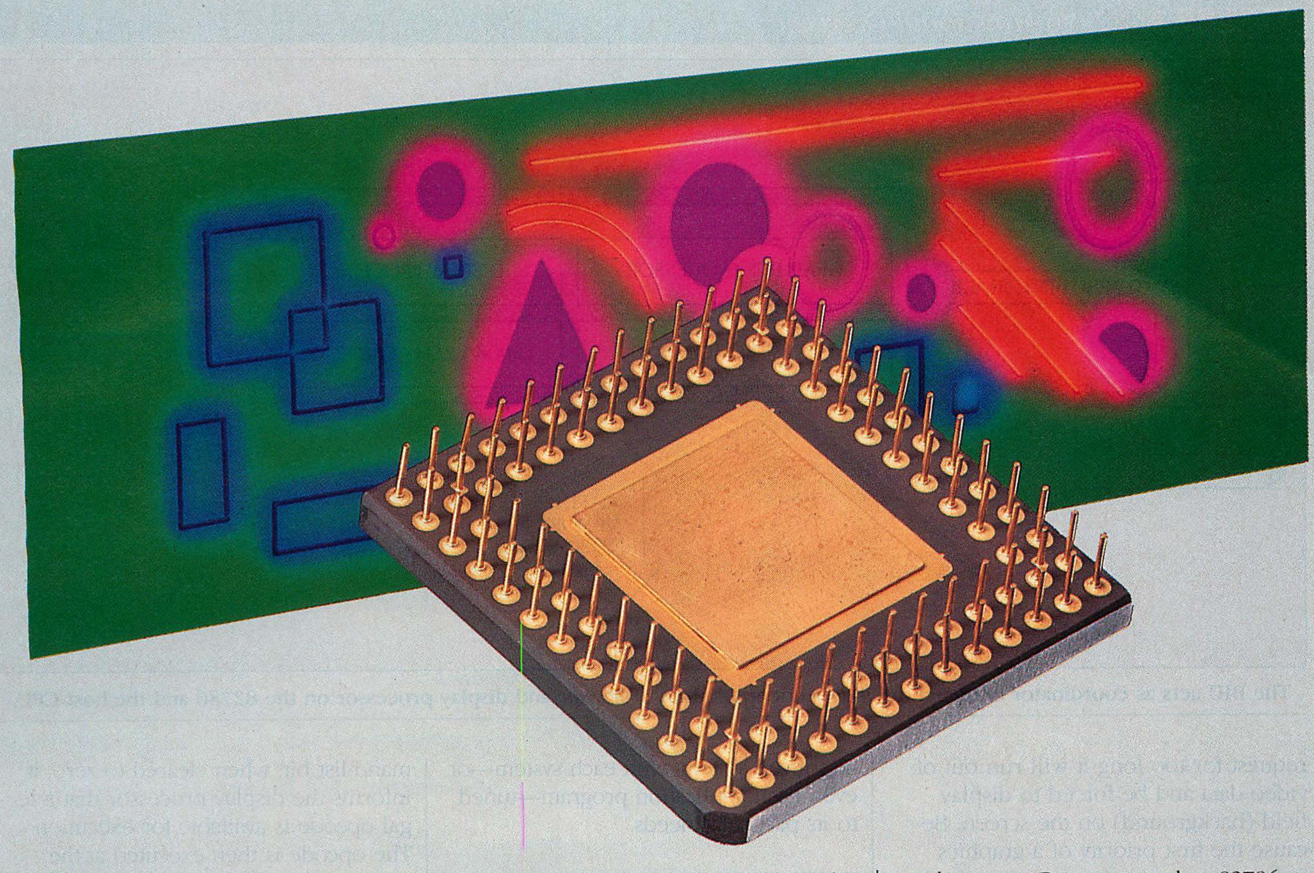
The 82786 sets graphical boundaries between tasks in the same way that multitasking systems such as the Intel 80386 use hardware to separate tasks. A task running in a specific window is entirely self-contained; it has a specified display size and depth and a data buffer at a particular address in display memory. Because it does not know what other tasks are in the system—or the location of critical parameters—it is hindered from interfering with them.

A difficult problem for the operating system in managing multitasking DOS applications is controlling arbitration between various programs that all write directly to display memory. The 82786 solves this problem by providing each application with its own private *bitmap*, contiguous memory representing a rectangular area of specified pixel depth. The application can write to that bitmap whenever it desires, because its data are shared by no other application. The data are positioned dynamically in a screen window as the display is refreshed, a process that is transparent to the applications modifying graphics memory.

The 82786 uses three independent processors: the display and graphics processors contained in the 82786 itself and the host CPU. The display processor extracts graphics data from the 82786's local memory and converts it to video-data output that appears in windows on the monitor. The graphics processor is responsible for performing all of the 82786's drawing operations.

The three processors communicate with each other and are coordinated by means of an on-chip bus called the bus-interface unit (BIU). Together, these processors, possibly coupled with one or more external microprocessors, perform the complete set of Intel 82786 functions (see figure 1).

PHOTOGRAPH • MARC DAVID COHEN



The entire system is driven by two independent clocks: CLK and VCLK. CLK is a general CPU clock that controls all processor operations; VCLK is the fundamental pixel clock that controls all video-output signals. Because the two clocks operate independently, video rates may be modified without affecting overall graphics performance.

BIU CONTROL

The BIU not only arbitrates among multiple requests for bus access from the 82786's display and graphics processors and the CPU, but also provides a complete memory-controller system for either video RAM (VRAM) or conventional DRAM chips. The 82786 itself has an address space of 4MB that is divided between dedicated-graphics memory and the host CPU's memory spaces. When the host CPU accesses graphics memory, the BIU acts as a slave to the host, providing graphics data directly from the 82786's memory space. Conversely, the BIU also can act as a bus master in the host CPU's address space, allowing the 82786 processor to draw directly into the host CPU's memory.

Operation of the BIU itself is controlled by local registers occupying 128 bytes of memory and including BIU control, relocation, refresh control, VRAM/DRAM control, and three programmable priority registers (see table 1). These registers, like all others in the 82786, can be mapped into the host CPU's memory- or I/O-address space. They also can be programmed to access either an 8-bit or 16-bit host interface, allowing the host CPU to configure its access to suit the PC's bus size.

The BIU's relocation register controls the location of the register block. At RESET, this register block appears to occupy the entire I/O space of the 82786: any I/O anywhere in the 82786's memory is written to it. Once this register is written, the register set is anchored in the address space at whatever location has been specified.

A flag bit in the register determines whether it is mapped into memory or I/O. If the register is memory-mapped, the host CPU reads the registers instead of the graphics memory when it accesses the register's addresses. Thus, any physical memory is hidden from the host CPU. Drawing operations can still be performed on that memory, and display- or graphics-processor instruction sets may be stored there.

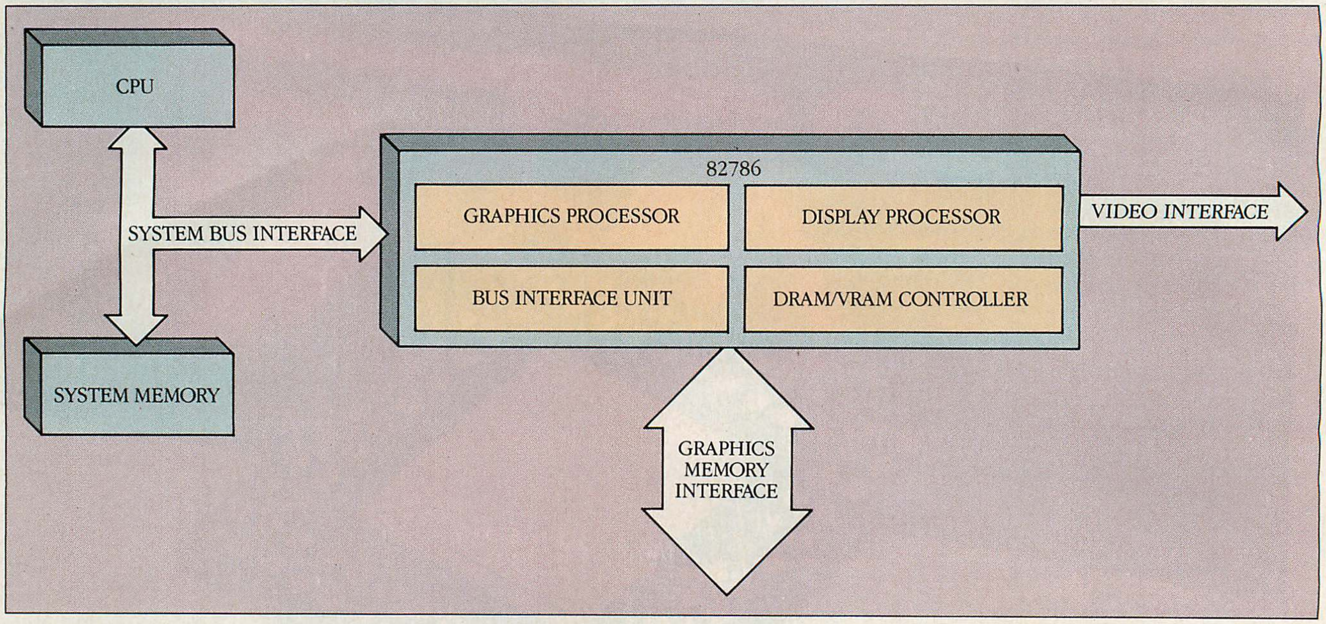
The BIU's memory interface is controlled by two of its internal registers: refresh control and VRAM/DRAM control. The six-bit refresh control register determines the frequency of memory refresh cycles; its programmed value is decremented every 16 clock cycles, and a refresh is generated when the value reaches zero. Because another 82786 memory cycle may be active when the refresh is signaled, refreshes must occur with sufficient frequency to tolerate any delay-causing latency.

The VRAM/DRAM control register defines the size, type, and number of memory devices supported in the 82786's graphics-memory space. Because this information defines the actual amount of display RAM installed, it sets the boundary between the 82786's graphics- and system-memory spaces.

The BIU's three priority registers (graphics, display, and external) determine the relative priorities assigned to competing processors during memory arbitration. The BIU can get bus requests from three separate sources: the display and graphics processors within the 82786 itself, each operating as an independent processor, and the external host CPU. In addition, both the display processor and graphics processor may wish to transfer blocks to and from graphics memory. These competing demands are arbitrated on the basis of programmable priorities that are assigned to each competitor for its first request and any subsequent requests.

Certain performance functions, such as display refresh, impose restrictions on setting these priorities: the display processor retrieves the data to refresh the screen; if it is denied a bus

FIGURE 1: *82786 Functional Overview*



Adapted from Intel 82786 User's Manual (1986)

The BIU acts as coordinator between the independent graphics processor and display processor on the 82786 and the host CPU.

request for too long it will run out of video data and be forced to display field (background) on the screen. Because the first priority of a graphics system is to maintain an undisturbed image on the screen, such disruptions are unacceptable to the user. Therefore, display refresh has a fixed priority higher than all programmable priorities.

The external CPU also can impose constraints on the amount of latency permitted to a device in the I/O channel: in the IBM PC, any request made to memory in an external, plug-in device must receive a response in 2.7 microseconds or less. Excessive bus latency can cause unpredictable behavior and corrupt the PC's local memory. Fortunately, the graphics processor is flexible; so long as it gains access to graphics memory to perform its drawing operations, it may be delayed for long periods without causing problems.

Each processor also has a priority register, in which 6 bits are used to assign two 3-bit priorities. Bits 5 through 3 determine the priority of a processor's first request for a bus cycle, and bits 2 through 0 determine the priority for subsequent requests made in a block transfer. Because the external CPU is not permitted to initiate block transfers, the low-order 3 bits in the external priority register are not used.

By adjusting the values used in the first priority level and the subsequent priority level, a trade-off can be obtained between maximum block-transfer performance and maximum bus latency in a given system, with each system—or even each application program—tuned to its particular needs.

DISPLAY PROCESSOR

The display processor extracts bitmap information from graphics memory and displays it in hardware windows on the graphics monitor, supplying all video-timing and synchronization signals from information stored in programmable video-control registers. It provides normal display data, zoomed displays, and hardware cursor control, plus an instruction set for defining new display formats. The display processor also fetches the descriptor information used to determine the size and position of hardware windows on the screen; this is done transparently.

The hardware windows displayed on the monitor are arranged as a number of horizontal strips, each running the entire width of the screen. Each strip is composed of tiles the height of the strip. A strip can be as small as one scan line high; up to 16 tiles can be placed horizontally across a single strip.

The display processor is controlled by a set of internal registers: display opcode, display address, default video, interrupt mask, and display status. The display opcode and display address registers allow the processor to execute its command set; the opcode indicates which operation, and the address is set to point to the data used by that operation. The low-order bit of display opcode is called the display-end-of-command-list bit; when cleared to zero, it informs the display processor that a legal opcode is available for execution. The opcode is then executed at the next vertical blank period, using the data that are identified in the display address register. When the command has been completed, the display processor sets the display-end-of-command-list bit and continues with display output.

The display processor uses the default video register to define the data to be driven on the video-data output pins during blanking periods. These data can be used as an overscan color or to signal other portions of the graphics system, such as a palette-load facility, that a blanking period is active.

The interrupt mask and display status registers are exact duplicates of each other (see table 2). When the host CPU requests that it be interrupted under a particular condition, the corresponding bit is set in the interrupt mask register; setting that bit in the display status register causes the interrupt. The host CPU reads the display status register to determine which event caused the interrupt. This reading clears any interrupt flag that was set.

A much larger register block within the display processor—display control—provides video and cursor control and defines where in graphics memory the hardware-window data descriptors can be read (see table 3). The display opcodes supported by the display processor are simple: load register, dump register, load all registers, and dump all

TABLE 1: *BIU Register Set*

MNEMONIC	FUNCTION	DESCRIPTION
BIU CONTROL		
WP2	Write-protect 2	Write-protects entire BIU register set
WP1	Write-protect 1	Write-protects certain BIU registers
DI	Display interrupt	Display processor causes interrupt
GI	Graphics interrupt	Graphics processor causes interrupt
BCP	Byte control	Determines if host accesses are 8/16 bits
WT	Wait	Wait states on host accesses of 82786 memory
VR	Video RAM	Selects video RAM refresh cycles
RELOCATION		
REL	Relocation	Sets location where register set is addressed
REFRESH		
REF	Refresh	Controls frequency of RAM refresh cycles
VRAM/DRAM CONTROL		
HT	Height	RAM device height (8K-by-*N* to 1M-by-*N*)
DC	DRAM control	Selects RAM interleave and page mode accesses
RW	Row	Number of rows of RAM devices
PRIORITY		
GPRIOR	Graphics	Priority of graphics processor bus cycles
DPRIOR	Display	Priority of display processor bus cycles
XPRIOR	External	Priority of external CPU bus cycles

The overall operation of the BIU is governed by the BIU control, relocation, refresh, VRAM/DRAM control, and three programmable priority registers.

TABLE 2: *Display Processor Status Registers*

MNEMONIC	FUNCTION	DESCRIPTION
ECL	End of command list	Set when processor finishes command list
ODD	Odd field	Interlaced display is showing odd field
EVEN	Even field	Interlaced display is showing even field
BLANK	Blank status	Video output is currently being blanked
FMT	FIFO empty	Display FIFO has run out of video data
DOV	Descriptor overrun	Tiles define too many pixels on one line
RCD	Reserved command	An undefined opcode is encountered
FRI	Frame interrupt	Set when a frame count has elapsed

The display processor status and interrupt mask registers are mapped parallel to one another, thus allowing events to be polled or interrupt-signaled.

registers. Each display opcode executes during the next vertical blank period, allowing modifications to window arrangement on the screen to occur smoothly and without interruption.

Only one register defines the layout of hardware windows on the display screen; in fact, it is only a pointer to the actual window-descriptor list. The descriptor list is arranged in memory as a linked list of strip descriptors, each of which points to its own list of tile descriptors. The strip descriptors and tile descriptors together define the display's hardware windows, which are set dynamically during the display refresh cycle (see figure 2).

Each tile descriptor defines a horizontal strip of uniform vertical format across the screen. To help reduce the bus bandwidth required for reading descriptors, the tile descriptors used with a given strip descriptor occupy consecutive memory locations immediately following the strip descriptor.

The first strip descriptor whose address is in the register is read during vertical retrace. This descriptor is used for as many scan lines as are specified in its definition; the next strip descriptor is fetched during the horizontal retrace preceding its first scan line.

The strip descriptor begins with a simple four-word header block. The first word of the descriptor defines the number of scan lines occupied by the entire strip. This number must match the height of the screen as defined by the video-control registers in the display processor. The next two words contain the address to be used beneath the current one. The last word defines the number of horizontal tiles in the strip—and therefore the number of tile descriptors that follow the header.

Each tile descriptor is a six-word definition of a single tile on the display. These tiles are the fundamental unit of screen output; each displays data from one bitmap in graphics memory. The first word of the descriptor defines the width of the displayed bitmap in bytes. Because the actual bitmap can be much larger than the tile used to display it, the display processor needs this value to determine how much the display-data fetch address must be incremented for each scan line of the tile.

The next two words specify the start address for the bitmap data being displayed; the start address controls which portion of the bitmap is displayed in the tile. By properly calculating the offset-start address for a given tile, it can be made to pan and scroll across a bitmap, displaying different portions of graphics data (see figure 3).

The fourth word determines the window's pixel depth and defines the start and stop bits to be used in each scan line. Because the addresses and fetch counts used by the display processor must all be even word counts, these start- and stop-bit fields are needed to give single-pixel resolution to the starting position and width of the window.

The fifth word—the fetch count—lets the display processor know the number of bytes of data to fetch for the display of the tile. Along with the pixel depth and start- and stop-bit fields, it also determines the actual displayed width of the tile in pixels.

The last word of each tile descriptor contains an assortment of flag bits. The four high-order bits control the display of a single-pixel border along any of the tile's four edges; a bit set to 1 turns on the border along that tile edge. Two window-status bits provide output on the window-status pins while this tile is being displayed. These bits are not used by the 82786, but are provided only for possible use by external display-board logic.

The zoom bit indicates whether the window should be zoomed by the factors defined in the display processor's ZoomX and ZoomY registers. The field bit determines whether actual bitmap

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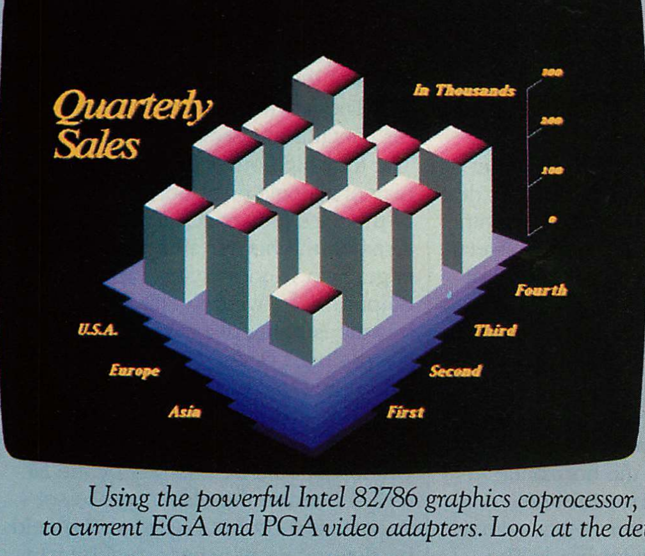

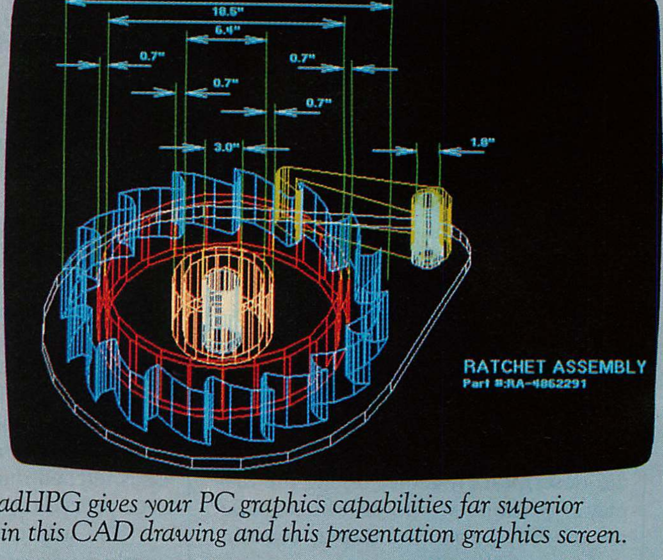

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data should be displayed in the window or whether no bitmap data should be fetched, leaving the window filled with the current field color.

The remaining two bits in the flag word determine the format of the bitmap data displayed by the tile. The 82786 can display data in formats compatible with a number of currently popular display adapters. The native 82786 format consists of data bytes stored sequentially and linearly in graphics memory; a single word is defined with its high-order byte appearing at a lower address than its low-order byte. The Intel 8086 microprocessors do not use this format; instead, they store words as low byte followed by high byte. In addition, the Hercules Graphics Card (HGC), the IBM Color Graphics Adapter (CGA), and the IBM PC*jr* interleave banks of display data, with consecutive lines of data in memory appearing every second or every fourth scan line on the screen, depending on the display adapter and the display mode.

The 82786's graphics processor can perform drawing operations only on bitmap data defined in its own native format. However, it can easily emulate current display adapters because each tile on the display is able to define its own memory format.

On power-up, the display processor does not execute any commands; all display outputs and interrupts are disabled and default video is generated on the video-data output pins. At a minimum, the host CPU must program the video-control registers for the 82786 to start generating synchronization signals to display a stable, if empty, image. The strip descriptors and tile descriptors need not be programmed until the applications software (or operating system) begins to define windows for its use. Because the strip descriptors are read and interpreted dynamically, the format of the entire display can be changed instantaneously.

TABLE 3: *Display Control Registers*

MNEMONIC	FUNCTION	DESCRIPTION
VSTAT	Video status	Controls cursor and video display enable
INTMSK	Interrupt mask	Selects conditions that cause interrupts
TRIPPT	Trip point	Controls frequency of FIFO fill accesses
FRINT	Frame interrupt	Number of frames between interrupts
CRTMODE	CRT mode	Flag bit register
IL	Interlace	Selects interlaced/noninterlaced display
W	Window status	Selects output of window status pins
S	Sync slave	Selects sync pins as inputs or outputs
B	Blank slave	Selects blank pins as inputs or outputs
AA	Acceleration	Number of pixels emitted each dot clock
HSYNSTP	Horizontal sync stop	Width of horizontal sync signal in dots
HFLSTRT	Horizontal field start	Time from sync to active video in dots
HFLDSTP	Horizontal field stop	Time from start to end of active video
LINELEN	Line length	Length of each scan line in dot clocks
VSYNST	Vertical sync stop	Width of vertical sync signal in lines
VFLSTRT	Vertical field start	Time from sync to active video in lines
VFLDSTP	Vertical field stop	Time from start to end of active video
FRMELEN	Frame length	Height of entire display in scan lines
DAP	Descriptor pointer	Address of first strip/tile descriptor set
ZOOMX	*X*-zoom scale	Amount zoomed tiles are *X*-zoomed
ZOOMY	*Y*-zoom scale	Amount zoomed tiles are *Y*-zoomed
FLDCOLR	Field color	Color when no window is present
BDRCOLR	Border color	Color of window borders
1BPPPAD	1 bit/pixel pad	Padding 1-bit data to 8 output bits
2BPPPAD	2 bit/pixel pad	Padding 2-bit data to 8 output bits
4BPPPAD	4 bit/pixel pad	Padding 4-bit data to 8 output bits
CSRMODE	Cursor mode	Flag bits controlling the cursor
S	Size	Selects 8-by-8 or 16-by-16 pixel cursor
X	Crosshair	Selects a block or crosshair cursor
T	Transparency	Controls whether cursor is transparent
CST	Cursor status	Value on window status pins under cursor
CSRPAD	Cursor pad	Padding cursor to 8 output bits
CSRPOSX	Cursor position *X*	*X* coordinate of cursor position on screen
CSRPAT0	Cursor pattern 0	First word of 16-word cursor pattern
CSRPATF	Cursor pattern F	Last word of 16-word cursor pattern

The display control registers provide control for the overall state of the 82786's video output and determine the appearance of the graphics display.

GRAPHICS PROCESSOR

The graphics processor, which is responsible for all 82786 drawing operations, provides graphics primitives for drawing lines, rectangles, arcs, and circles; incremental procedures for rapidly drawing or filling in complex figures; as well as a complete set of 16 binary Boolean drawing operations. The graphics processor also supports rectangular clipping and picking, in which pointing devices of some kind are used to select a portion of the display.

The processor operates on bitmaps of programmable size and characteristics. It can draw on any number of distinct bitmap areas in memory, each of which can have its own pixel depth. It also can execute general bit-block-transfer (bit-BLT) operations plus specialized character-BLTs that convert a one-bit-per-pixel source-character mask into a multiple-bit colored character.

Overall operation of the graphics processor is controlled by six memory-mapped registers: opcode, link address (two words), status, and instruction pointer (two words). These registers direct execution of commands and allow monitoring by the host CPU.

The graphics processor has 22 internal registers, two of which are status mask registers: graphics poll mask (GPOEM) and graphics interrupt mask (GIMR). The GPOEM and GIMR have flag bits corresponding to the bits in the graphics status register (see table 4). If a bit is set in GIMR, then a graphics-processor interrupt to the host CPU is generated whenever the corresponding flag bit is set in the graphics status register. If a flag is set in graphics status, and its corresponding bit is also set in GPOEM, the graphics processor immediately enters the poll state, in effect aborting the current command list.

The graphics count (GCNT) register provides a count of characters being drawn during a character-string draw, and the graphics stack pointer (GSP) register is used while executing command lists. Because blocks of graphics commands can be defined as subroutines and called from other graphics-command lists, a stack pointer, defined by the application, is used to indicate the region of memory to be used for

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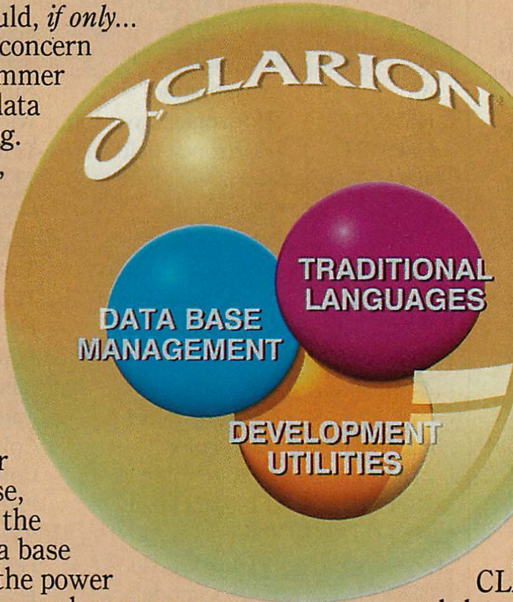

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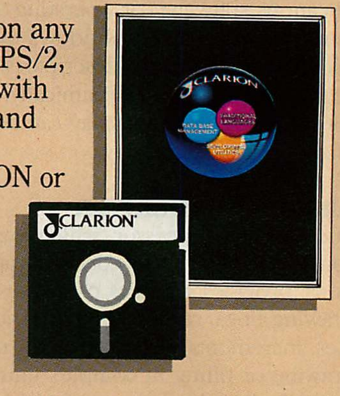

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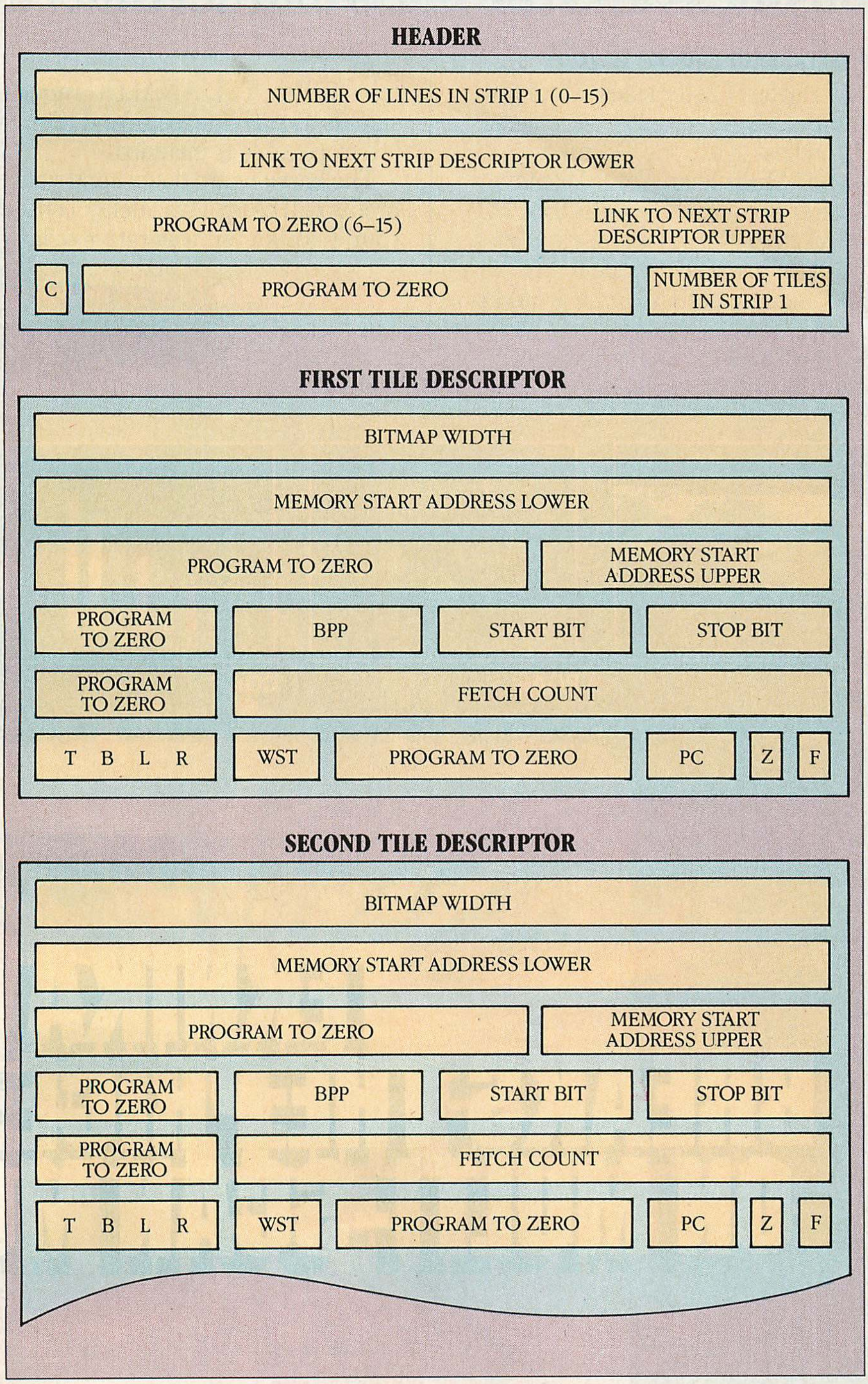
storing return addresses. If no subroutines are used, this register does not have to be initialized.

The instruction set of the graphics processor is divided into four functional groups: drawing-environment control, geometric drawing, BLT, and execution-control instructions (see table 5). The graphics processor usually fetches commands from a sequential list in memory with its starting address programmed into the graphics control register. In order to begin executing a command list, the graphics control opcode must contain a LINK (or GOTO) command. LINK is followed by the address of the new command list; as soon as execution begins, the graphics processor jumps to the new command list.

Each instruction consists of an opcode word followed by a varying number of words of data specific to that opcode. The opcode itself occupies only the high eight bits of the opcode word; the low-order bit is the graphics-end-of-command-list (GECL) bit. Whenever an opcode with the GECL bit is fetched, the command is considered to be last on the list. Its parameters are fetched and the command is executed, but the GECL bit is copied into the graphics poll (GPOLL) bit in the graphics status register and the graphics processor enters a poll state. It remains in that state until a new link address is programmed into the graphics control register and the GPOLL bit is reset to 0.

Once the graphics processor has established the graphics environment, drawing can take place. Each application must initialize all aspects of its drawing environment. As a graphics-processor instruction list is executed, the flow of control from one group of graphics commands to another is governed by execution-control instructions. The 82786 provides no conditional test-and-branch instruction, but can jump to new addresses only to fetch instructions and call other blocks of instructions as subroutines. The host CPU is responsible for determining which graphics operations are to be performed and for programming the 82786 appropriately.

FIGURE 2: *Strip and Tile Descriptors*



The combination of the strip and tile descriptors defines the display's hardware windows, which are set dynamically during the course of the display refresh cycle.

Adapted from Intel 82786 User's Manual (1986)

LOCAL MEMORY

The 82786's 4MB address space contains no dedicated or reserved locations for special data. Each processor uses local registers to store pointers to its current command lists. Local graphics memory holds the actual bitmap-display data, as well as the bitmaps required by a multitasking workstation.

Local 82786 graphics memory extends from the beginning of the address space to a memory size programmed by the host processor at power-up. Addresses within this local range refer to memory locations controlled by the BIU and are accessed at high speed by either the graphics processor or the display processor. The 82786 makes the assumption that any addresses exceeding the programmed memory size are in external memory, which is controlled by the host CPU.

When the 82786 generates an address that exceeds its memory, the BIU requests system memory from the CPU. This allows the 82786 to retrieve display data, execute command lists, or draw upon bitmaps stored in system memory rather than graphics memory.

This feature is also a good alternative to other methods: traditional systems using graphics controllers for drawing either must use the host CPU

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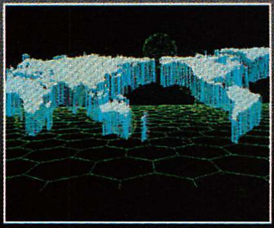
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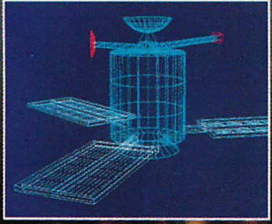
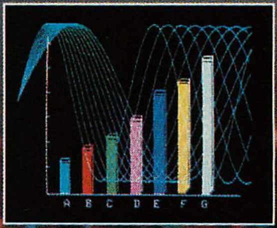
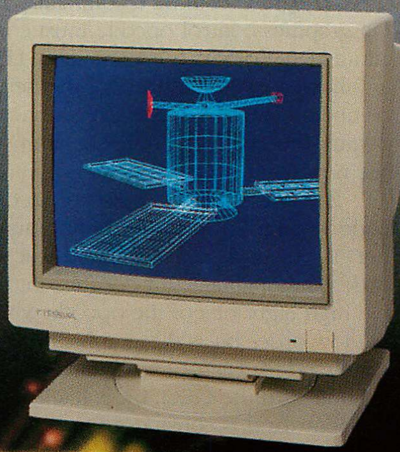

PGA



CGA



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to precisely emulate the controllers, or they must copy system memory to display memory, allow the controller to draw on it, and then copy the modified data back to their original location. For example, the Enhanced Graphics Adapter (EGA) display driver in Microsoft Windows includes two transparent routines to set a pixel, both of which are required: one sets a pixel in the EGA memory, and the other sets a pixel in the system memory.

The 82786 can support up to 32 VRAM and DRAM devices. Its flexible memory interface supports a variety of RAM technologies, memory organizations, and device densities, allowing the designer to trade-off cost with performance to build the system most appropriate to the application.

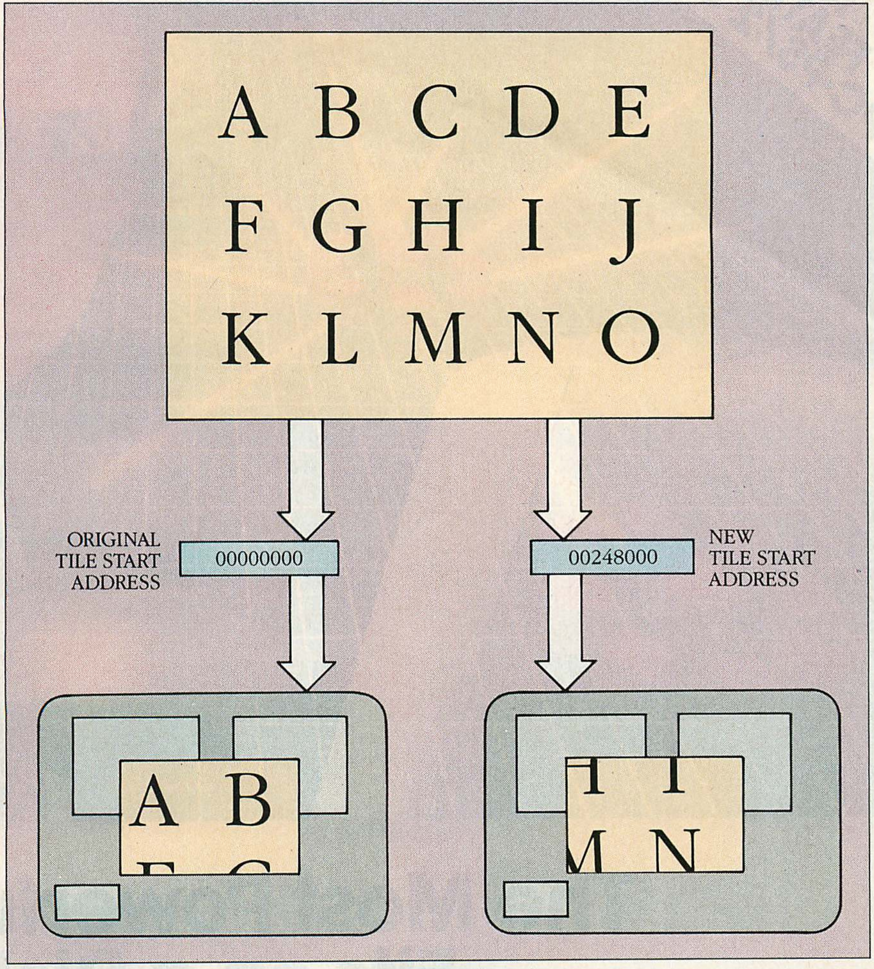
It also supports standard-page and fast-page modes, static column, and Intel's Ripplemode DRAMs, providing cycle times of 100 nanoseconds for the faster devices. Memory can be interleaved or noninterleaved. Devices can have one, four, or eight bits in sizes from 16KB to 1MB per chip. Even more memory devices can be installed if external drivers are there for support.

SLAVES AND MASTERS

The host CPU and the 82786 can exchange information by reading and writing data in each other's address space. The exchanges may vary from simple command lists or instructions to large chunks of data. In a multitasking system, the host CPU can implement virtual bitmap memory by moving display data to local address space and then writing the data to disk for later retrieval into the 82786's memory.

The 82786 operates in slave mode when it responds to a request from the host CPU either to read or to write graphics memory. This interface can be synchronous or asynchronous, with either an 8-bit or 16-bit interface. The host CPU can access the 82786's memory by asserting the Chip Select Low input line on the 82786; the 82786 activates the Slave Enable output line, which indicates the 82786 is ready to accept write data from the data lines or provide read data to the lines. Slave Enable is brought high by the 82786 when the slave transfer is complete. The host CPU's request is arbitrated according to the setting of the external priority register and is not queued by the BIU; if the host CPU wishes to initiate several slave transfers, it must assert the Chip Select Low input line for each one, wait until the 82786 completes its current cycles and arbitrates in favor of the external CPU, perform the operation, and then restart the process.

FIGURE 3: *Graphic Bitmap Panning*



The tile's bitmap start address controls which portion of the bitmap is displayed in the tile. By changing the start address, the tile can be panned across the bitmap.

TABLE 4: *Graphics Processor Status Registers*

MNEMONIC	FUNCTION	DESCRIPTION
GIBMD	Illegal bitmap	Current bitmap definition is not valid
GCTP	Character trap	Signals character larger than 16-by-16 pixels
GBMOV	Bitmap overflow	A drawing command crossed the clip rectangle
GBCOV	Character overflow	Text or bit-BLT crossed the clip rectangle
GPSC	Pick successful	Drawing in PICK mode found desired object
GINT	Graphics interrupt	82786 generated a software interrupt
GP GRCD	Reserved opcode	82786 found an undefined opcode
GPOLL	Graphics poll state	Commands finished and 82786 is idle

The status register is written to by the 82786 and is read by external devices; the GPOEM and GIMR are written to by external devices and read by the 82786.

The 82786 processor also can act as a bus master to access memory not under its control; usually this memory resides in the host CPU's address space. Local and external memory are differentiated on the basis of installed memory in the 82786 system—all addresses beyond the configured size of graphics memory initiate transfers in which the 82786, acting as master, requests memory from the host CPU.

The 82786 pulls the Hold Request line high to the host CPU or bus arbiter to indicate that it wishes to become the bus master. The 82786 waits for a Hold Acknowledge and then drives the address, data, read or write lines, and Master Enable High to initiate the cycle

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TABLE 5: *Graphics Processor Instruction Set*

MNEMONIC	FUNCTION	DESCRIPTION
ENVIRONMENT		
DEF_BIT_MAP	Define bitmap	Set drawing area size and depth
DEF_CLIP_RECT	Define clip rectangle	Set size of clip rectangle
DEF_COLORS	Define colors	Foreground and background colors
DEF_TEXTURE	Define texture	Pattern used in line drawing
DEF_LOGICAL_OP	Define logical operation	Boolean raster operation used in drawing
DEF_CHARSET	Define character set	Address of character set to use
DEF_CHARORIENT	Define character orient	Path and rotation of characters
DEF_CHARSPACE	Define character spacing	Added spacing between characters
ABS_MOV	Absolute move	Move drawing pointer absolutely
REL_MOV	Relative move	Move drawing pointer relatively
ENTER_PICK	Enter pick mode	Stop drawing, select objects
EXIT_PICK	Exit pick mode	Leave pick mode, resume drawing
GEOMETRIC DRAWING		
POINT	Point	Draw a single pixel
INCRPOINT	Incremental points	Draw a complex figure of pixels
CIRCLE	Circle	Draw a circle
LINE	Line	Draw a single line segment
RECT	Rectangle	Draw a rectangle
POLYLINE	Polyline	Draw a set of line segments
POLYGON	Polygon	Draw an outlined polygon
ARC	Arc	Draw a circular arc
SCANLINES	Draw horizontal scan lines	Fill a set of adjacent scan lines
BLOCK TRANSFER		
BIT_BLT	Bit-BLT	Copy rectangle inside a bitmap
BIT_BLT_M	Bit-BLT between bitmaps	Copy data between two bitmaps
CHAR	Draw character string	Draw a series of characters
CONTROL		
LINK	Link	Unconditional jump to new address
CALL	Call subroutine	Jump to graphics subroutine
RETURN	Return from subroutine	Return from graphics subroutine
INTR_GEN	Generate interrupt	Cause a graphics software interrupt
DUMP_REG	Dump register	Store a graphics processor register in memory
LOAD_REG	Load register	Load a graphics processor register from memory

The graphics processor's instruction set is broken down into four groups: environment, geometric drawing, BLTs, and control.

and indicate that it is now controlling the bus. Master Enable High is asserted for as long as the 82786 requires the bus; Hold Request is deactivated as soon as the transfer is complete.

The 82786 still responds to slave accesses by the host CPU when it is waiting for acknowledgment of a Hold Request. This prevents a lockout if the 82786 starts a master request at the same time the host CPU initiates a slave request; the host CPU does not respond with a Hold Acknowledge until its slave cycle has been completed.

Normally the 82786 processor can occupy the external bus for an extended period, particularly if the graphics processor is performing a drawing operation on system memory. It is interrupted only by local memory-refresh requests. If the 82786 occupies the bus for too long, the host CPU can withdraw the Hold Acknowledge to interrupt the 82786. The 82786 then removes its Hold Request after completing the current cycle to indicate it has freed the external bus. After waiting two cycles, the 82786 again attempts a Hold Request to complete its operation. If the host CPU cannot respond in less than two cycles, external logic must be supplied to extend the delay time.

HEART OF MULTITASKING

The Intel 82786 provides a powerful, low-cost approach to graphics-display system design. Its high level of integration and design makes it especially suitable for coupling with other Intel 8086-family microprocessors. Although geometric and character-graphics operations are fully supported, the 82786's strongest advantage is its hardware-windowing capability.

For the first time in PC graphics, restrictions have been removed between graphics memory and display output. A powerful graphics presentation system is the result of this progressive move. As PCs begin to provide more sophisticated multitasking environments, the 82786 offers a display-management facility that supports the same concepts of display-memory management and protection that the multitasking operating system provides to the application program.

The popularity of these multitasking environments is growing; expect to see the 82786 processor at the heart of low-cost multitasking PC workstations in the very near future.

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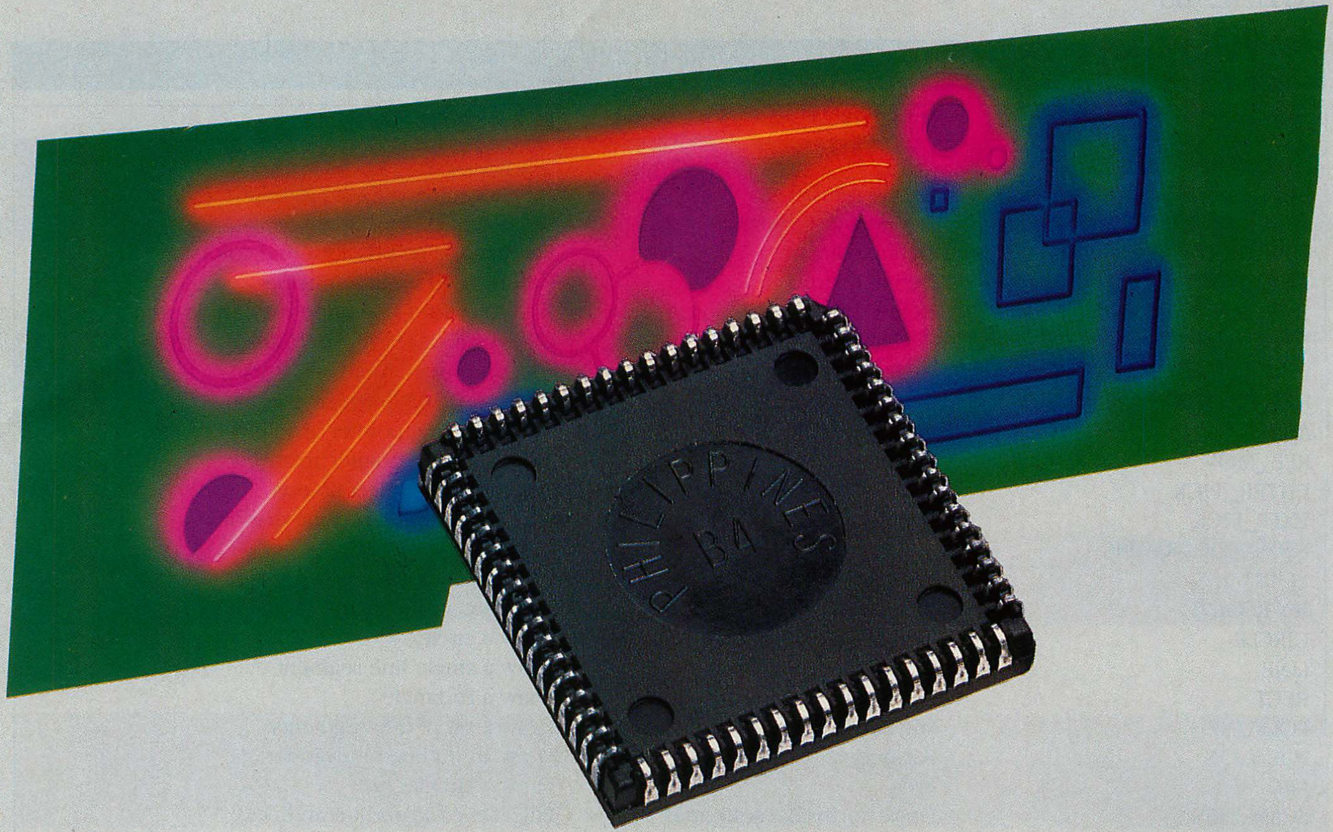

PHOTOGRAPH • MARC DAVID COHEN

Texas Instruments' TMS34010 Graphics System Processor is the first 32-bit microprocessor designed expressly to be used for graphics. It provides almost no built-in graphics primitives, but instead supports customized graphics that are explicitly programmed for each application. Its ability to be programmed qualifies the TMS34010 as a microprocessor; this distinguishes it from the Intel 82786, a graphics processor that cannot be programmed. In addition to graphics, the TI microprocessor, which lists for $180, provides a complete hardware environment, including RAM control, video timing, and host-CPU communications.

This full 32-bit microprocessor with a 32-bit address space is unique because it is bit-addressable; incrementing an address by one refers it to the next bit in memory.

Memory accesses are controlled by two programmable field sizes that can be set to between 1 and 32 bits with or without sign extension. This flexibility permits the user to manipulate memory by field boundaries rather than byte or word boundaries, allowing direct processor support of pixel depths lower than 8 bits per pixel. Internal hardware logic handles all necessary mask and shift operations. This feature alone provides a powerful increase in graphics performance over conventional graphics methods. (See figure 1 for a memory map of the TMS34010.)

The TMS34010's other major advantage over conventional graphics adapters is its ability to address memory in not only traditional linear format, but also a new *X-Y* addressing format. This direct support for a graphics model in display memory gives the applications software the ability to select the most natural addressing mode instruction by instruction, and in most cases, even by each operand of the instruction.

Addresses in linear format are 32 bits in length; *X-Y* addresses are two 16-bit values packed into one double word with the low-order 16 bits assigned to the *X* coordinate and the high-order 16 bits assigned to the *Y* coordinate. Each coordinate is a signed number that can range between –32,768 and +32,767. Instructions are provided for converting addresses from linear format to the *X-Y* addressing format.

Because the TMS34010 is programmable, a typical graphics implementation would provide only a small amount of video RAM (VRAM)—about enough to store one screen's worth of information. Much more ROM and dynamic RAM (DRAM) would be required: the ROM to store the start-up code, including a set of prepackaged subroutines or even an entire operating system; and the several megabytes of DRAM to provide program space for very sophisticated applications that require large amounts of graphics software or storage for complex geometric descriptions.

For example, the TMS34010 works well in a dedicated PC graphics workstation that is used to render three-dimensional simulations. Such uses are computation-intensive; the initial object data must be transformed, clipped, and lighted before they are displayed on the screen; these are functions the TMS34010 can support from a graphics environment that is self-contained in one chip. The PC maintains a geometric model of the object to be displayed and defines the current viewing conditions, and the TMS34010 determines the appearance of the object.

INTERNAL ARCHITECTURE

The TMS34010 has a highly pipelined internal architecture, a high-speed arithmetic logic unit (ALU), and a 32-bit barrel shifter that allows it to fetch instructions in parallel with executing instructions and accessing registers and local memory (see figure 2). It also has a programmable, 256-byte instruction cache (see figure 3). Because each instruction set is 16 bits, this cache can hold 128 instructions at once, a size well suited to the inner loops of most graphics algorithms implemented on the TMS34010. The cache can be pro-

Custom-tailored Graphics: TMS34010

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grammed so that software controls when it is flushed, enabled, or disabled.

The ALU is designed for high-speed operations on data available in on-chip registers. The TMS34010's instruction set is similar to those in many reduced-instruction-set computers (RISC) in that only move instructions can access memory locations. Unlike PC processors, the TMS34010 requires separate instructions to read data into registers, operate on them, and then write the data to memory. However, the TMS34010 has a large general-purpose register set so that most algorithms can read their entry data into registers once, manipulate all data within the register set, and then write only the final results to memory.

The TMS34010's barrel shifter can shift a 32-bit quantity up to 32 bit positions in a single machine state. It is used internally by the microcode for high-speed, 32-by-32-bit multiply, divide, and modulo instructions.

The TMS34010 has thirty-one 32-bit internal registers that can be accessed by the entire instruction set. They are divided into two register files, labeled A and B. Each file contains 15 registers that are numbered 0 through 14; a stack pointer, essentially the 16th register in each set, is shared by the two files. The entire A file is available for applications software; no dedicated tasks are assigned to its registers.

The B-file registers control graphics context and are implied operands in graphics-operation instructions. Many of the B-file registers define programmable values that are not likely to change often. Because a graphics operation such as a bit-block transfer (bitBLT) can have many operands, storing the operands in registers is more efficient than fetching them from memory each time the operation is executed.

The B-file registers also define the current graphics state and provide additional information by means of canonical definitions; these definitions allow the TMS34010 to work with a wide variety of graphics-memory layouts under software control (see table 1).

In addition to the A and B files, the TMS34010 has two dedicated 32-bit registers used for the program counter and the status register. These registers are managed independently and can be manipulated only by special instructions that transfer them to and from the general-purpose register files.

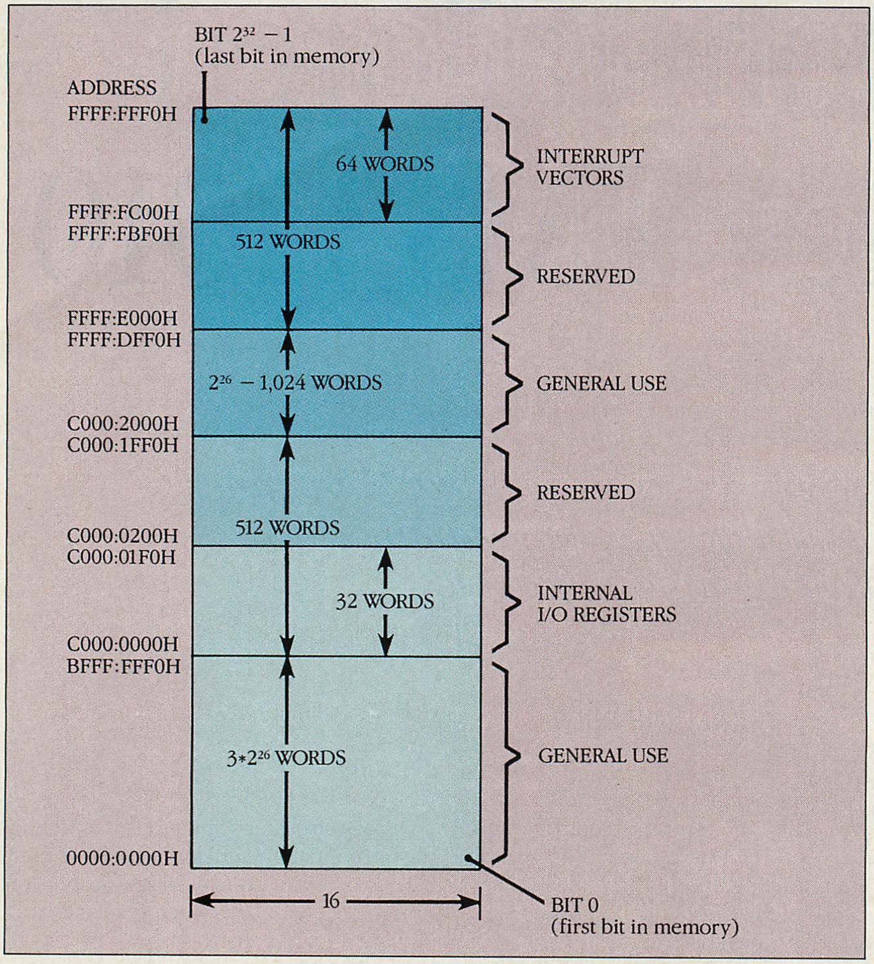
I/O REGISTERS

The I/O register set, which is memory mapped into TMS34010 address space, contains the registers that control global system behavior: local-memory-interface parameters, interrupts, video-control parameters, and the host interface. The local-memory-interface registers manage DRAM refresh and functions that define graphics parameters (see table 2). These registers function as an extension of the B file and also help execute various graphics instructions.

The programmable interrupt-control registers determine which conditions generate hardware interrupts in the TMS34010; each interrupt also can be programmed to signal the CPU (see table 3). The video-control parameters determine the complete state of graphics refresh and the video system, including the master/slave state and video-synchronization timings (see table 4).

The host interface allows the host CPU to be able to communicate with the TMS34010. The memory interface is indirect, mediated by the TMS34010 itself: to write to or read from graphics memory, the host CPU writes the desired address to a 32-bit address register that is mapped into PC address space and then reads or writes the desired data through a 16-bit data register. The actual mapping of the address and data registers depends on the implementation and may use the PC's memory or I/O address space. The host interface requires that the host CPU use only four words of memory or I/O in order to access all the graphics memory, thus allowing the graphics system to fit into the PC's crowded memory space (see table 5).

FIGURE 1: *TMS34010 Memory Map*



Adapted from TMS34010 User's Guide (1986)

The memory of the TMS34010 is divided into three regions: trap vectors, I/O registers, and general use. The memory can be physically accessed 16 bits at a time.

DATA TYPES

Perhaps the TMS34010's chief distinction from other graphics processors is that it is a 32-bit microprocessor that executes algorithms based upon these graphics elements: packed-pixel arrays, *X-Y* coordinates, rectangular windows, and variable-width bit fields. Packed-pixel arrays allow the TMS34010 to rapidly manipulate large graphics blocks in a single operation; these arrays are especially useful for operations that require a pixel to be read, combined with a new value according to some specified algorithm, and then rewritten.

This support of packed-pixel arrays is similar to that provided in IBM's Color Graphics Adapter (CGA) and its new IBM Personal System/2 Multicolor Graphics Array (MCGA) and Video Graphics Array (VGA): all bits that define a pixel are stored contiguously in the same byte; pixels that are adjacent on the screen are also adjacent in memory; and subsequent scan lines of the image are stored consecutively.

The *X-Y* coordinate pairs supported by the TMS34010 have 16 bits per coordinate. A rectangular window, defined by two X-Y coordinate pairs, is used for clipping and for determining whether a given point is inside the window. Each point in the coordinates is stored as a 16-bit half of a 32-bit double word with the *Y* coordinate contained in the high-order word. This format is supported by graphics instructions that perform moves, arithmetic operations, and comparisons of *X-Y* pairs directly.

Variable-width bit fields are supported by the TMS34010 primarily for inserting and extracting pixel-size elements of data to and from memory. Any instruction that addresses memory contains an opcode bit that specifies which fields are to be used. Field sizes, which range from 1 to 32 bits, are programmable. When memory is accessed, the word containing the desired bits is read from memory, masked as required, and rotated into the least significant position in the destination register; all these operations are transparent to the executing software. In addition, the field size determines the amount that a pointer register is updated in postincrement addressing modes; each pointer register can be incremented by whatever field size is required.

The TMS34010's eight addressing modes provide complete flexibility in designing algorithms. Although its RISC-like architecture allows only move and drawing instructions to directly address external memory, all memory instructions can use all supported addressing modes. Available modes include:

Immediate. The source operand of a move-to-register instruction is stored as part of the instruction opcode.

Absolute. The TMS34010 stores all memory references as absolute 32-bit addresses immediately following the instruction opcode.

Register direct. A register's contents can be used as either the source or destination operand.

Register indirect. A register's contents can be used as the 32-bit linear address of the source or destination operand.

Register *X-Y* indirect. The specified register contains the *X-Y* address of either the source or destination operand.

Register indirect with displacement. The contents of a specified register are added to a fixed displacement in order to obtain the effective source or destination address.

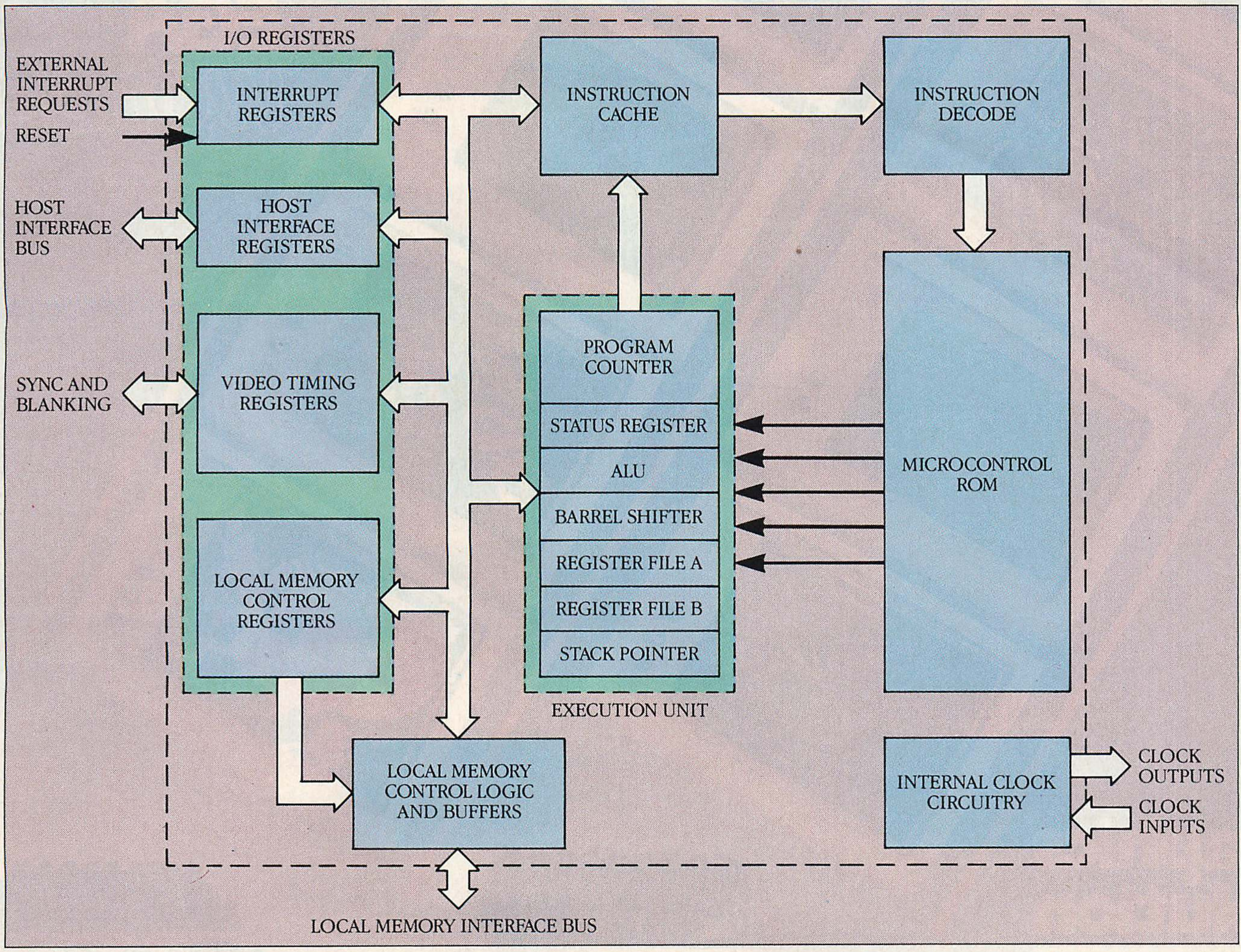
Register indirect with predecrement. A specified register is used as a pointer to the source or destination data, but its contents are decremented by the field size that is in use before the address is calculated.

Register indirect with postincrement. This addressing mode is similar to register indirect with predecrement, except that the field size is added to the register after the address is calculated.

Status flags are stored in a 32-bit status register (ST) external to both the A and B files. The ST defines the current field size (1 to 32 bits) for fields 0 and 1, the current interrupt enable flag, the condition code bits for the overflow (V), zero (Z), carry (C), and negative (N) flags, and a special interrupt flag used by an interrupt-service routine to determine if the interrupted instruction was PIXBLT or FILL.

The ST's contents can be examined by loading them into a processor register in either the A or B file or by storing them on the stack and examining the data that are in memory. The state of the TMS34010 can be modified by changing the local copy of the ST and then recopying it to the real ST.

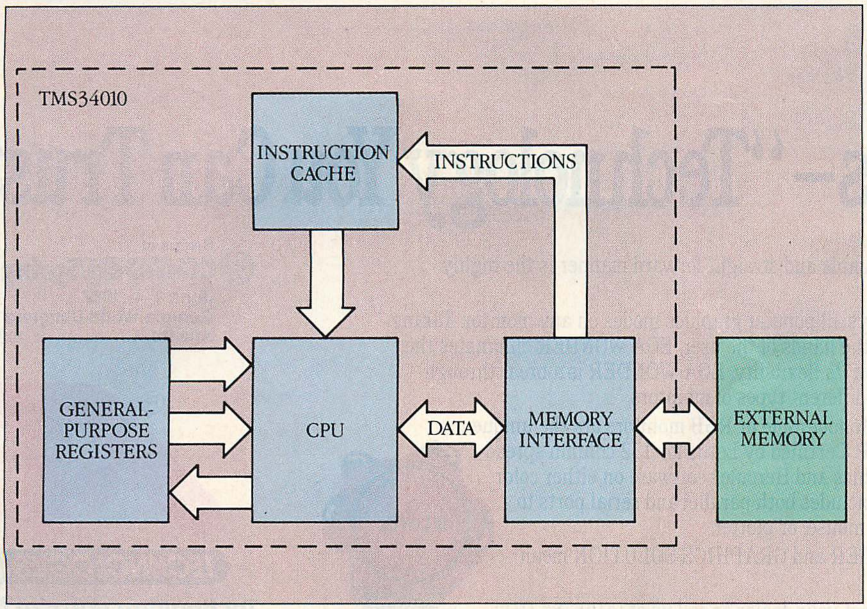
FIGURE 2: *TMS34010 Block Diagram*



Adapted from TMS34010 User's Guide (1986)

Internal hardware logic handles all mask and shift operations needed for direct support of pixel depths less than eight bits.

FIGURE 3: *Internal Parallelism*



Adapted from TMS34010 User's Guide (1986)

The ability of the TMS34010 to fetch instructions from a programmable 256-byte cache in parallel with data accesses from memory improves its execution speed.

INSTRUCTION SET

More than 120 instructions that affect the flow of software execution are included in the TMS34010's complex and powerful instruction set. They can be divided into four categories: graphics, move, general, and program control instructions (see table 6).

Control-flow instructions perform arithmetic and graphic conditional tests, modifying the control flow based on test results. CALL instructions allow direct or indirect calls of subroutines; JUMP instructions allow direct or indirect jumps based on the current state of the ST flags. Conditional jumps also can decrement a register and test for branching after the decrement, much like LOOP in the Intel 8086 processors, except that any register may be used. The TRAP instruction can trigger up to 32 software interrupts. Instructions also are provided to return from subroutines and interrupts and to transfer the program counter and ST to and from program-accessible registers.

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TABLE 1: *B-file Registers*

MNEMONIC	FUNCTION	DESCRIPTION
SADDR	Source address (B0)	Defines bit-BLT source address
SPTCH	Source pitch (B1)	Width of the source bitmap in pixels
DADDR	Destination address (B2)	Bit-BLT destination address
DPTCH	Destination pitch (B3)	Width of destination bitmap
OFFSET	*X-Y* offset (B4)	Bitmap address from start of memory
WSTART	Window start (B5)	First corner of clipping rectangle
WEND	Window end (B6)	Opposite corner of clipping rectangle
DYDX	Delta *Y* / Delta *X* (B7)	Size of bit-BLT, FILL, or LINE operation
COLOR0	Color 0 (B8)	Drawing background color
COLOR1	Color 1 (B9)	Drawing foreground color
Reserved	B10 - B14	Reserved for future expansion

The registers in the B file are directly accessible through the TMS34010's instruction set; they control the implied state of the current graphics environment.

TABLE 2: *Local Memory Interface*

MNEMONIC	FUNCTION	DESCRIPTION
CONTROL	Memory control	Global memory control flags
RM	Refresh mode	Selects type of refresh signal
RR	Refresh rate	Frequency of RAM refreshes
W	Window mode	Enable/disable clipping
PBH	PixBlt horizontal	Sets BLTs to run right or left
PBV	PixBlt vertical	BLT up or down direction
PPOP	Pixel processing option	Sets pixel raster writing mode
CD	Cache disable	Disable the 34010 instruction cache
CONVDP	Convert destination pitch	Destination *X-Y*/linear conversion
CONVSP	Convert source pitch	Source *X-Y*/linear conversion
PMASK	Plane mask	Bitplane write-protect mask
PSIZE	Pixel size	Defines current pixel depth
REFCNT	Refresh count	Address of next RAM refresh

The local-memory-interface I/O registers are responsible for controlling the manner in which the TMS34010's on-board graphics memory is managed and maintained.

TABLE 3: *Interrupt Control Registers*

MNEMONIC	FUNCTION	DESCRIPTION
INTENB	Interrupt enable	Interrupt enable mask
X1	External interrupt 1	Interrupt 1 from host CPU
X2	External interrupt 2	Interrupt 2 from host CPU
HI	Host interrupt	Host software interrupt
DI	Display interrupt	Set at a given scan line refresh
WV	Window violation	Drawing has the clip rectangle
INTPEND	Interrupt pending	Parallels the INTENB register; bits set when each interrupt occurs

Hardware interrupts to the TMS34010 can be programmed to occur under certain conditions that are controlled by the state of the interrupt control registers.

A full set of add, subtract, multiply, divide, and modulo instructions, as well as optimizations for early-out algorithms and parallel multiplication operations, are included in the TMS34010 instruction set. All arithmetic operations must be performed on values held in registers; the source and destination operands for each instruction must be in the same register file. Absolute value, addition (register-to-register and immediate-to-register), division, multiplication, modulo (signed and unsigned), arithmetic negation, and subtraction are provided, as well as sign and zero extension of registers. Divide and multiply provide full 32-by-32-bit multiplicands with a 64-bit result. If a 32-bit result is not required (both operands, for example, may be known to be only 8 bits), multiplications may be performed in parallel by storing two 8-bit values, one in each of the high and low words of each operand register. For graphics algorithms, registers holding *X-Y* addresses can be added to or subtracted from each other with the flags set to reflect the values held in *X* and *Y*.

The TMS34010 supports primitives to set a pixel to a given color, set a pixel and move it incrementally, move blocks of pixels, and execute the inner loop of any simple line-drawing algorithm. All graphics instructions combine the source and destination data pixels according to the current writing mode. The graphics instructions include:

DRAV (draw-and-advance). Set the pixel at the *X-Y* position specified in the first operand and move *X* and *Y* by the increments specified in the second operand; use the color in the COLOR1 register (holding bits set to 1).

FILL. Fill a rectangle defined by the DYDX (delta-*y*/delta-*x*) register using the color in the COLOR1 register.

PIXBLT (pixel-block transfer). Copy a rectangle that is defined by the DYDX register to the DADDR (destination-address) register.

PIXBLT B (pixel-block transfer binary). Copy a rectangle from a monochrome (1-bit-per-pixel) area of memory to a colored (multiple-bits-per-pixel) area. Bits set to 0 in the source are converted to COLOR0; bits set to 1 are converted to COLOR1 before combining with the destination-pixel values.

PIXT (pixel transfer). Copy a pixel from a specified source address to a destination address. Both source and destination addresses may be registers, linear, or *X-Y* addresses.

LINE (line draw). Calculate the inner loop and set the pixels for a line-draw algorithm. All line-draw parameters must be specified explicitly by storing them in registers before executing the LINE instruction; this gives the applications software complete control over the drawing process.

The processor is controlled by stack operations and interrupt-enable and disable instructions. The ST can be directly removed from the stack, and multiple register-stack transfers can be achieved by MMTM (move-multiple-to-memory) and MMFM (move-multiple-from-memory) instructions, each of which takes a 16-bit field as an operand; each bit corresponds to a register in the same register file as the destination memory pointer. MMTM and MMFM allow the entire contents of the A or B file to be moved to or from memory using one instruction. All interrupts except RESET and the nonmaskable interrupt (NMI) can be enabled or disabled

TABLE 4: *Video Control Registers*

MNEMONIC	FUNCTION	DESCRIPTION
DPYSTRT	Display start	Address of start of display memory
DPYADR	Display address	Current screen refresh address
DPYCTL	Display control	Bit flags for display control
HSD	Horiz. sync direction	Sets HSYNC as input or output
DUDATE	Display update	Screen refresh update amount
ORG	Display origin select	Sets *Y* increasing up or down screen
SRT	Shift register enable	Display cycles modify VRAM data
SRE	Screen refresh enable	Turns on screen display refresh
DXV	Disable external video	Sets VSYNC as input or output
NIL	Noninterlaced	Selects noninterlaced display
ENV	Enable video	Starts sync and video output
DPYINT	Display interrupt	Scan line at which interrupt occurs
DPYTAP	Display tap point	VRAM tap point for screen panning
HCOUNT	Horizontal count	Current pixel position on display
HESYNC	Horizontal end sync	Width of horizontal sync pulse
HEBLNK	Horizontal end blank	Time from sync to active video
HSBLNK	Horizontal start blank	Position of end of active video
HTOTAL	Horizontal total	Total dot clocks per scan line
VCOUNT	Vertical count	Current vertical scan line
VESYNC	Vertical end sync	Size of vertical sync pulse
VEBLNK	Vertical end blank	Time from sync to active video
VSBLNK	Vertical start blank	End of active video display
VTOTAL	Vertical total	Total scan lines in one screen

The video-control parameters determine the state of the video system.

TABLE 5: *Host Interface Registers*

MNEMONIC	FUNCTION	DESCRIPTION
HSTADRL	Host address low	Low 16 bits of the 34010 address
HSTADRH	Host address high	High 16 bits of the 34010 address
HSTDATA	Host data	34010 local data to be read or written
HSTCTLL	Host control low	Host interface control bits
INTIN	Interrupt in	Set by host to interrupt 34010
INTOUT	Interrupt out	Set by 34010 to interrupt host
MSGIN	Message in	INTIN 3-bit identification field
MSGOUT	Message out	INTOUT 3-bit identification field
HSTCTLH	Host control high	Host interface control bits
NMI	Nonmaskable interrupt	Set by host to cause 34010 NMI
NMIM	NMI mode	NMI context save flag setting
INCW	Increment pointer write	Host address increments on writes
INCR	Increment pointer read	Host address increments on reads
LBL	Lower byte last	Sets 8-bit data high byte/low byte
CF	Cache flush	Flushes 34010 instruction cache
HLT	Halt GSP	Stop 34010 execution

The host interface is controlled through the use of the five I/O registers.

TABLE 6: *Instruction Set*

TYPE OF INSTRUCTION	DESCRIPTION
Graphics instructions	Used for manipulating graphics data.
Move instructions	Used for moving data, such as from a register to an absolute address
General instructions	Used for many general purposes, such as addition, comparison or shifting.
Program control	Used for functions such as calling subroutines or jumping.

The TMS34010's extensive instruction set consists of more than 120 instructions.

using the EINT (enable interrupts) or DINT (disable interrupts) instructions.

The TMS34010 also provides instructions for Boolean, shift, sign-extension, zero-extension, bit-testing, comparison, and flag-setting operations. Boolean instructions operate on full 32-bit register values; shift-and-rotate instructions can move data up to 31 bits in a single machine state.

The TMS34010 is designed to operate with a 50-MHz system clock. All instruction timings are specified in machine states, each of which is equal to eight system clock cycles. (Instruction timings are usually expressed as 160 nanoseconds, which equals 6.25 MHz.) Most logical, shift, and comparison operations can be performed in only one machine state; graphics operations such as fills can write one word to memory in two machine states. The actual calculation of graphics-instruction execution is complex; the timings depend heavily on the alignment of the source and destination data (where appropriate), the writing mode, and whether or not the clipping option is turned on.

FUTURE PROSPECTS

The TMS34010's future prospects as a true 32-bit graphics microprocessor are unequaled; it offers a remarkably flexible and powerful solution for graphics systems. It also reduces board space and cost by providing integrated support functions on one chip. Based on its past leadership in advancing VRAM technology, TI is likely to continue providing RAM solutions tightly coupled to its graphics microprocessor to produce a streamlined, high-performance graphics-display system.

If anything, the TMS34010's flexibility is a slight hindrance to initial developers—once the graphics system is designed, the support software must be added to complete the solution. Fortunately, many software libraries (including TI's) and graphics-operating systems are becoming available to ease the software development burden. As PC applications become more sophisticated and demanding in their graphics requirements, the TMS34010 will be able to track those requirements, providing a viable, upwardly compatible graphics system for years to come.

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Prolog-86 *from Solution Systems*		125	88
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cobol language

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Microsoft COBOL *See Microsoft Section*			
Realia COBOL with RealMENU	*New*	1145	899
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The DOS-LAN Juncture

The challenge of designing and maintaining PC-compatible DOS applications, never an easy task with the steady progression of machines and operating systems, is intensified by the LAN factor.

J. SCOTT HAUGDAHL

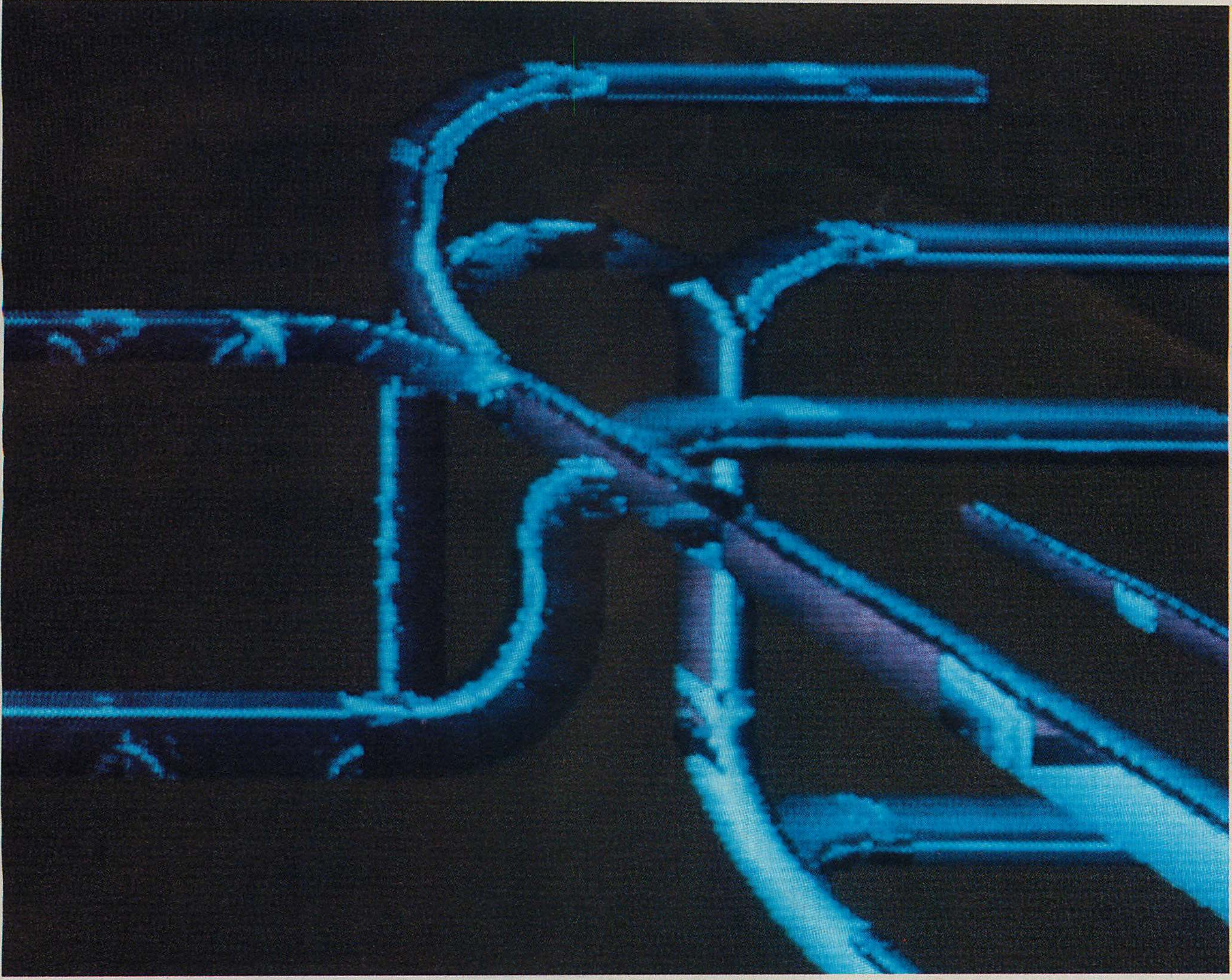
For software developers, it is not enough any more to keep pace with the IBM line of machines—the PC, PC/XT, PC/AT, IBM compatibles, IBM Personal System/2, not to mention DOS 1.x, 2.x, 3.x. Now the software developer also must ask: will the program run on a PC connected to a LAN, and can it use LAN resources?

The answer is yes, many DOS applications will run on a PC connected to a LAN, and these programs fall into two groups. Most applications fit into a first group that needs only to coexist with the LAN; they cannot use LAN files and devices. Fortunately for such programs, refinements to DOS in the LAN area have been made in an upwardly compatible manner. By following a few conventions and handling LAN-related errors from DOS, files can be accessed and devices connected to the LAN. A second group does exploit the LAN's data-sharing and communications capabilities using the rudimentary tools provided in the most recent versions of DOS for developing multiuser software. Although some desirable capabilities are absent, a few current DOS features can be used to craft substitutes.

The LAN-software situation is further complicated by many conflicting vendor implementations: IBM, Novell, 3Com, Nestar, Corvus, and others each defines its own unique interface to certain LAN facilities. Although support for NETBIOS (a peer-to-peer networking standard sired by IBM) is growing, many vendors support only a subset of its functionality. In addition, NETBIOS is inappropriate for applications that need only to share files. Thus, the route most likely to result in LAN-portable software is the one that uses only those few facilities offered by DOS.

This article examines the issues inherent to implementing multiuser applications within the scope of functions provided by DOS 3.1 or later (hereafter referred to as DOS 3.x). In addition, *application* will mean the traditional DOS programs invoked by the end user, such as word processors or data managers, not systems software, such as file servers, gateways, or communications servers. Note that a diminishing number of LANs do not use DOS to provide their services, but instead use a disk-server environment. Typically they intercept the BIOS disk I/O calls to provide virtual disk volumes on the server. Because DOS is unaware of the redirection taking place, these LANs cannot provide DOS networking functionality to applications. The Nestar and Tiara LANs fall into this category, as did earlier offerings from 3Com and Corvus.

IBM and Microsoft began to accommodate LANs with DOS 3.0 in August 1984. The new ATTRIB, SHARE, and LASTDRIVE commands support multiuser environments. File sharing, also introduced with DOS 3.0, requires executable (.COM and .EXE) files on a LAN server to be marked read-only so that multiple users can load the file simultaneously—ATTRIB performs this function. SHARE is used to install the DOS file-sharing support on servers that use DOS (such as IBM's PC LAN) for file services. LASTDRIVE (which is added to



COMPUTER GRAPHIC • DOV JACOBSON

CONFIG.SYS) allows the last accessible DOS drive (up to Z:) to be used as a virtual disk designator.

DOS 3.1 introduced the commands JOIN and SUBST, primarily to support stand-alone applications that want to share network resources. JOIN connects a drive to a directory on another drive to create a new directory structure; thus, only one drive specifier is necessary to access files from multiple drives or directories. This is useful if, for example, a hard disk becomes full and has to be divided across two disks. A directory subtree of the original disk would be moved to the new disk, and JOIN used to maintain the original directory structure. SUBST substitutes a drive letter for a drive or directory. Essentially, it provides a means of accessing files on that drive by referring to the drive letter. SUBST supercedes the ASSIGN command.

New LAN-related commands added with DOS 3.3 include FASTOPEN and APPEND. FASTOPEN is a terminate-and-stay-resident (TSR) command that supports file-name caching. It improves file-name search response times (one of the bottlenecks when using the DOS-based PC LAN Program as a server). APPEND is like a PATH command for data files. It allows an application to run in one subdirectory and find (that is, open) files in a different subdirectory without specifying the path name.

Although DOS provides some of the frills that are needed to work on a LAN, it stops short of providing standard commands to attach to remote resources and share files. Instead, each LAN vendor must provide a set of commands to manage LAN resource connections. Table 1 shows the command sequence for redirecting devices on various LANs. Many vendors also provide a menu-driven interface.

PROCESSING DOS CALLS

The manner in which LAN workstation software processes DOS function calls (the functions provided by interrupt 21H) also varies from vendor to vendor. For example, Novell's NetWare shell intercepts any interrupt 21H request, checks to see if it is for a local or remote device, and processes the call accordingly. Calls for remote services by the IBM PC LAN Program (as well as 3Com 3Plus and Microsoft Networks) must be previously "redirected." The Redirector software is licensed from Microsoft to original equipment manufacturers (OEM). The Redirector checks the interrupt 21H function call for redirection to the network. If the request is not for a redirected device, it is passed on to local DOS. Otherwise, the Redirector converts the call into a server message block (SMB) request and, in the case of PC LAN, calls NETBIOS. Figure 1 demonstrates the relation of network support components to DOS applications with the IBM and Novell approaches. Figure 2 shows the various functions added to interrupt 21H (from DOS 3.0 on) that enhance LAN application capabilities. These functions are discussed below.

At the heart of DOS LAN support is Open File (interrupt 21H, function call

3DH). Open File controls access to a file in two ways. The first control, made through *access mode*, specifies how the process making the Open File call will use the file, as read-only, write-only, or read-write. The second control, *sharing mode*, determines what access can be granted on subsequent file open attempts: compatibility, deny-read, deny-write, deny-read/write, or deny-none.

Upon entrance to interrupt 21H, the following registers must be set: AH is 3DH, DS:DX points to an ASCIIZ path name (just as it is typed in a DOS command, such as C:\WP\TEMP), and AL is the *open mode*. Upon return, AX will contain the file handle, if the file was successfully opened, or an error code.

The open mode defined in AL is subdivided into fields that specify inheritance (bit 7), sharing (bits 6, 5, 4), and access (bits 2, 1, 0). Bit 3 is reserved and should be set to zero. Specific values for the fields are shown in figure 3. If the inheritance bit is set to 0, the file is inherited (including all sharing and access restrictions) by a child process (one created by the DOS EXEC function). If the bit is set to 1, the file is private to the current process.

When the Open File function was initially introduced in DOS 2.0, the open mode included only the access mode information (bits 0 to 2); all other bits were to be left as zero. File sharing in DOS 3.0 was added by using these previously undefined bits. However, to retain some measure of compatibility with old programs, the sharing mode value of zero (in bits 4 to 6) is defined as *compatibility mode.*

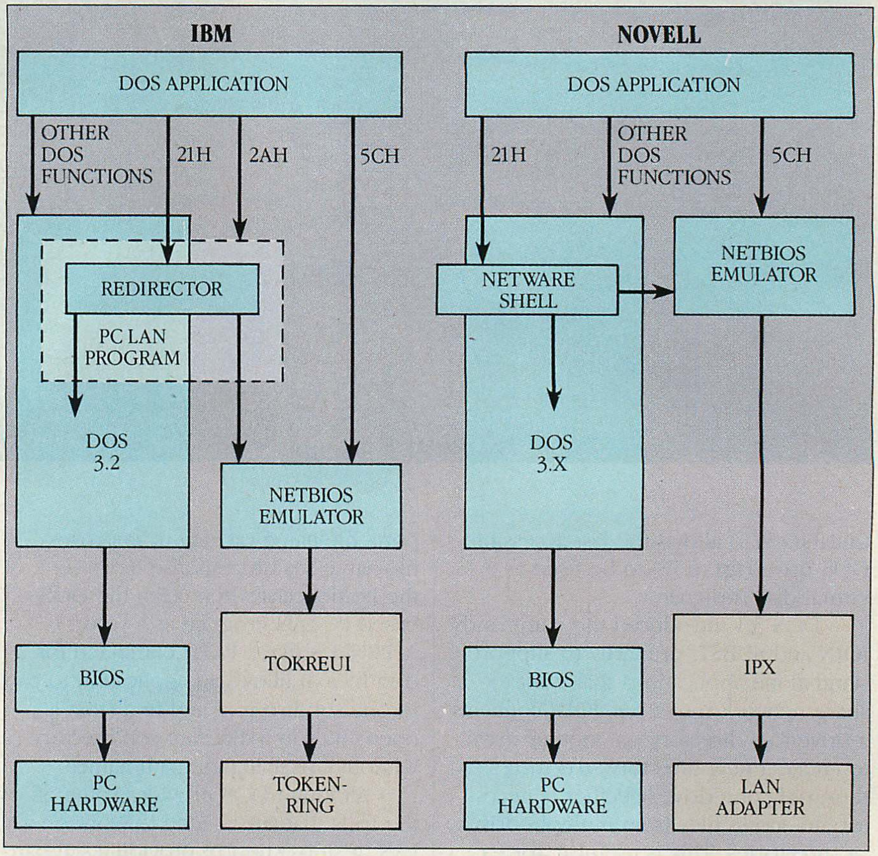
Compatibility mode enables old applications to share files without compromising the integrity of new applications. Mixing compatibility mode with other file sharing modes is allowed in only one case: a file that is made read-only (by DOS ATTRIB) can be opened multiple times for read-only access in compatibility mode, and can simultaneously be opened for read-only access in deny-write or deny-none sharing mode. This exception allows .COM, .EXE, and data files to be opened by both old and new programs if they first are made read-only. Any other attempt to open a file with a mix of compatibility mode and any of the deny modes will result in Open File returning error 5 (access denied), with an extended error code of 32 (sharing violation).

TABLE 1: *Typical LAN Commands*

LOCAL AREA NETWORK	COMMAND
CONNECT DRIVE E: TO SERVER SALES, DIRECTORY\CUSTOMER	
LOCAL AREA NETWORK	**COMMAND**
IBM PC LAN	NET USE E: \\SALES\CUSTOMER
Novell NetWare	MAP E:=SALES/SYS:CUSTOMER
3Com 3Plus	3F LINK \\SALES\CUSTOMER
DEFINE LPT2 AS PRINTER TAXFORM (PRINTER 3) ON SERVER ACCTING	
LOCAL AREA NETWORK	**COMMAND**
IBM PC LAN	NET USE LPT2: \\ACCTING\TAXFORM
Novell NetWare	SPOOL SERVER=ACCTING LOCAL=2 PRINTER=3
3Com 3Plus	3P LINK LPT2: \\ ACCTING\TAXFORM

Each vendor of a LAN environment uses a slightly different command sequence to establish a connection between a workstation and a server's devices.

FIGURE 1: *LAN Support Schemes*



The strategy diagrammed on the left uses the Microsoft Redirector to capture requests from within DOS and direct them towards the LAN. NETBIOS, or another vendor-specific protocol, is used to send requests through the network. At right, Novell uses a shell to intercept any LAN-related functions before they get to DOS.

Developers of new application programs (even programs that are not intended for use on a LAN) should not use compatibility mode, but instead should choose an appropriate deny mode. Indeed, the DOS method for flagging sharing violations would seem to be sufficient incentive not to use compatibility mode: when an attempt is made to open a file in compatibility mode, but that file is already open in a conflicting deny mode, an interrupt 24H (critical error) is generated. If the program has installed its own critical error handler, a call to DOS function 59H (Get Extended Error) will (again) return error 32. However, if the standard DOS error handler is in use, an obscure message such as the following

```
Sharing Violation error reading drive F:
Abort, Retry, Ignore?
```

will be returned on the screen. In contrast, a file open call with any of the deny modes will simply return an error

FIGURE 2: *LAN-related DOS Functions*

AH	AL	FUNCTION		DOS VERSION
3D		OPEN FILE (WITH SHARING)		3.0
44	09	IOCTL	IS DEVICE REDIRECTED?	3.0
	0A		IS HANDLE LOCAL OR REMOTE?	3.0
	0B		CHANGE SHARING RETRY COUNT	3.0
59		GET EXTENDED ERROR		3.0
5A		CREATE UNIQUE FILE		3.0
5B		CREATE NEW FILE		3.0
5C	00	LOCK BYTE RANGE		3.0
	01	UNLOCK BYTE RANGE		3.0
5E	00	GET MACHINE NAME		3.1
	02	SET PRINTER SETUP		3.1
	03	GET PRINTER SETUP		3.1
5F	02	GET REDIRECTION LIST ENTRY		3.1
	03	REDIRECT DEVICE		3.1
	04	CANCEL REDIRECTION		3.1
67		SET HANDLE COUNT		3.3
68		COMMIT FILE		3.3

Beginning with version 3.0, several DOS functions (as accessed through interrupt 21H) have been introduced to facilitate the interface to local area networks.

code that can be tested by program logic immediately following the call.

All other DOS file open and/or create functions, including the ancient FCB functions, use the equivalent of compatibility mode when opening a file. When using DOS functions such as 5AH (create unique file), it is advisable to use the call to obtain the name of the created file, then close the associated handle and open with function 3DH using the appropriate sharing mode. (Note that FCB functions are obsolete and should be avoided.)

The sharing matrix in figure 4, adapted from IBM's *PC-DOS Technical Reference*, shows the results of opening a file for the first time, then, while the file is open, opening it subsequent times. The sharing mode overrules the access mode whenever a subsequent application opens *the same file*. If the file is first opened with deny-write sharing and read/write access, then it may be read and written to freely for the first open, but subsequent opens will be denied write access to the file, regardless of how it was opened.

File sharing also seriously impacts DOS I/O performance. Typically, when DOS is asked to read data from a file, it will read a block of data from disk into an internal buffer, and satisfy the read request from the buffer. A subsequent read request might be satisfied by using the already filled buffer, rather than performing a disk read. Incidentally, these buffers are the ones specified by the BUFFERS statement in CONFIG.SYS.

When a file is being shared among multiple PCs, having each DOS buffer the file locally could produce unexpected results. If user A were to read data from a file that was locally buffered by DOS, and user B then wrote to that file, the new data written by user B would not be read by user A. DOS performs local buffering on shared files only when such a situation cannot occur. Thus, local buffering is used when a file is opened with deny-read/write sharing, or when a file is opened for read access and deny-write sharing. To accommodate older applications, DOS also performs local buffering on files opened in compatibility mode; in this case, the situation just described can occur and must be handled.

The recently announced DOS version 3.3 has added the COMMIT function, which flushes any locally buffered data to disk. Prior to this, the only way to flush the buffer was to close the file, then reopen it. This created a window of vulnerability in which another program could seize the file between the close and open functions, thus denying access to the original owner before processing of the file was complete. COMMIT is invoked through DOS function 68H. Upon entry, register BX holds the file handle; upon exit, AX contains an error code if the carry flag is set.

Another DOS 3.3 function that enhances file processing in LAN environments is Set Handle Count. Previously, an application was limited to 20 open file handles. Now this can be increased using DOS function 67H; register BX passes the maximum handle count. This function requires a 4KB memory block, so the program first must release memory using function 4AH (Set Block).

DOS REGION LOCKING

Many applications will want to obtain finer control over data sharing than Open File can provide. For example, a LAN database might contain all data records in the same file; multiple user would need some method to coordinate access to records in that file. A typical DOS implementation would have each user open the file in deny-none sharing mode, then use *region locking* to control access into the file.

Region locking is performed using DOS function 5CH (lock/unlock byte range). The registers that must be set upon entry are shown in table 2. Upon return, AX will contain an error code if the carry flag has been set; attempting to lock a previously locked region will result in error code 33 (lock violation). As little as a single byte or as much as the entire file may be locked depending on the offset into the file and the number of bytes. Locking beyond the physical end-of-file is allowed, and is valuable in certain situations, for example, when data are being appended to the file by multiple users.

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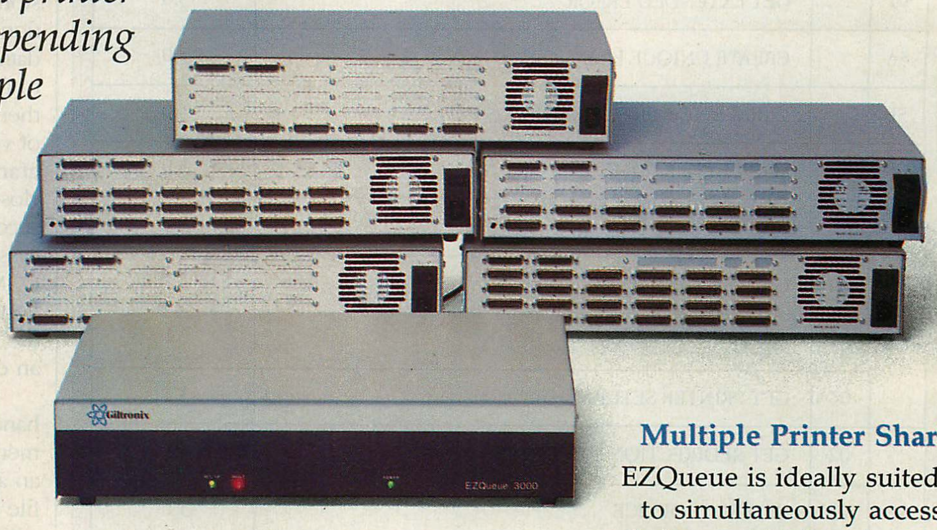

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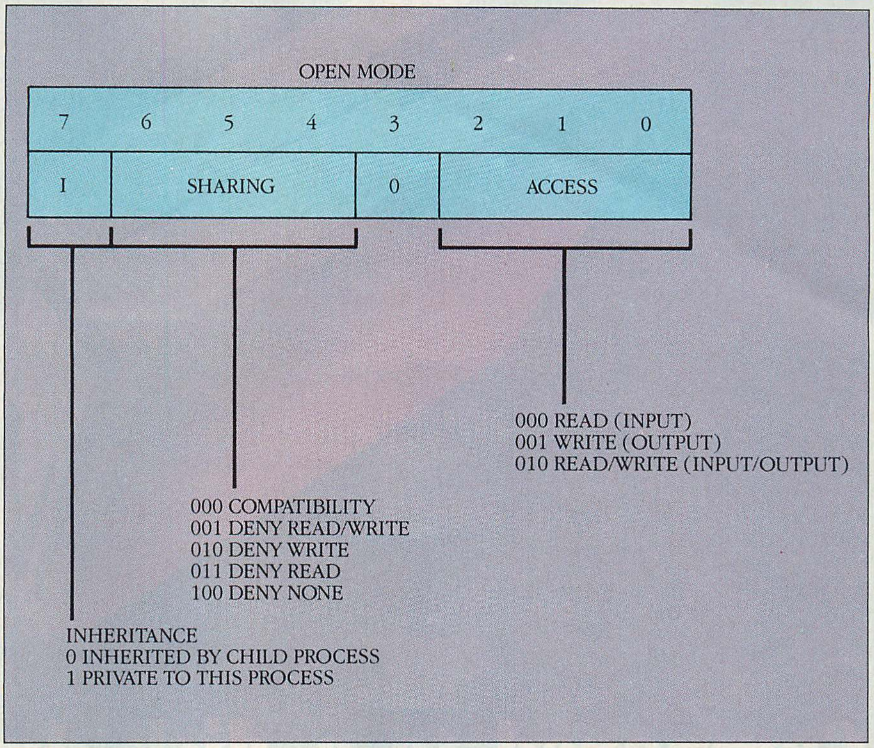
FIGURE 3: *Open File Mode Information*



The access field describes the intended use of the file by the opening program. DOS 3.0 augmented the open mode by adding two more fields. The sharing field specifies the maximum access that subsequent users can obtain. The inheritance field allows greater security when a child process is created using DOS EXEC.

DOS is designed to protect regions of a file that have been locked from reading, writing, and overlapping locks by other users of the file. If another application attempts to read, write, or lock an already-locked region, DOS will return failure, and the extended error code (from DOS function 59H) will be 33 (lock violation). Applications that open a file in compatibility mode and attempt to violate a lock by reading or writing are notified in a more assertive manner: a *critical* error (interrupt 24H) is generated, similar to the Open File situation described above.

DOS region locking is functional, but by no means friendly. A one-to-one match must be present between lock and unlock calls in an application; DOS *will not* permit multiple locks to be undone by a single unlock. The effect of closing a file (or exiting a program) with locks still in effect is undefined. Although some LANs will clean up locks when a file is closed, such amenities are not mandated by DOS. In extreme cases, the only way to clear a lock left in effect is to reboot the server.

To ensure that locks are released, applications should keep a table of active locks for each open file. Handlers should be installed for Ctrl-C exit (interrupt 23H) and critical error (interrupt 24H) so that abnormal exits (as well as normal exits) will perform lock cleanup. But all of this housekeeping is annoying, considering that DOS itself must keep a similar table to manage locks and certainly could improve system integrity by releasing abandoned locks from its own information.

Incidentally, the use of *record locking* for the DOS locking feature is a misnomer. DOS provides locking for a range of bytes in a file—nothing more. The application must determine which bytes to lock based on the file's logical structure: a record in a database, a screen of a word processor, a group of cells in a spreadsheet, or other application-defined data organization.

DOS supports automatic retries on both region locks and file opens. If a file open request conflicts with an existing open on the same file, or if a lock request overlaps a previously locked region, DOS will delay a short time, then retry the request. Because locks in many applications may be of short duration, this reduces the number of lock failures that must be explicitly handled within the application.

Retry counts and the delay between retries can be set with DOS function 44H (IOCTL), subfunction 0BH. Upon entry, AH contains 44H, AL contains 0BH, CX contains the number of times to execute a delay loop, and DX contains the number of retries. Upon return, AX will contain an error code if carry is set. In a default situation, DOS will retry three times before accepting failure, executing the delay loop once between each retry.

The time spent in the retry delay loop is machine-dependent, in that it depends on processor speed. The delay loop count set for an XT, for example, may be too fast for a Compaq Deskpro 386, causing retries to fail because they were made too quickly. Developers can disable retries (by setting them to zero) and use a machine-independent delay within the application.

Even developers who do not have access to a LAN can experiment with the file-sharing and region-locking features of DOS on a stand-alone PC. SHARE.EXE, a TSR program on the DOS distribution diskette, provides these features. Typically, it finds use on PCs that function as network servers. It performs equally well as a test bed for exploring LAN file-access questions.

TABLE 2: *Byte Lock/Unlock*

REGISTER	CONTENTS
AH	5CH
AL	0 to LOCK; 1 to UNLOCK
BX	File handle
CX	File offset high word
DX	File offset low word
SI	Length high word
DI	Length low word

Using DOS function 5CH, applications can lock and/or unlock any range of bytes in a file. Locations that are past the end-of-file also can be locked.

Deadlocks. In any kind of resource locking scheme, an application must be prepared for *deadlock*. This circular wait condition develops as follows: application A has a lock on record 100 in database X and application B has a lock on record 150, also in database X. To complete its transaction, application A needs to update information in record 150 that is related to information in record 100. Application A will attempt to lock record 150, but is rejected and must retry. But suppose that application B will not relinquish the lock for record 150 because it, too, must access record 100 to complete its transaction. A waits for B while B waits for A. The application must provide a means of backing out of such a transaction and retrying the en-

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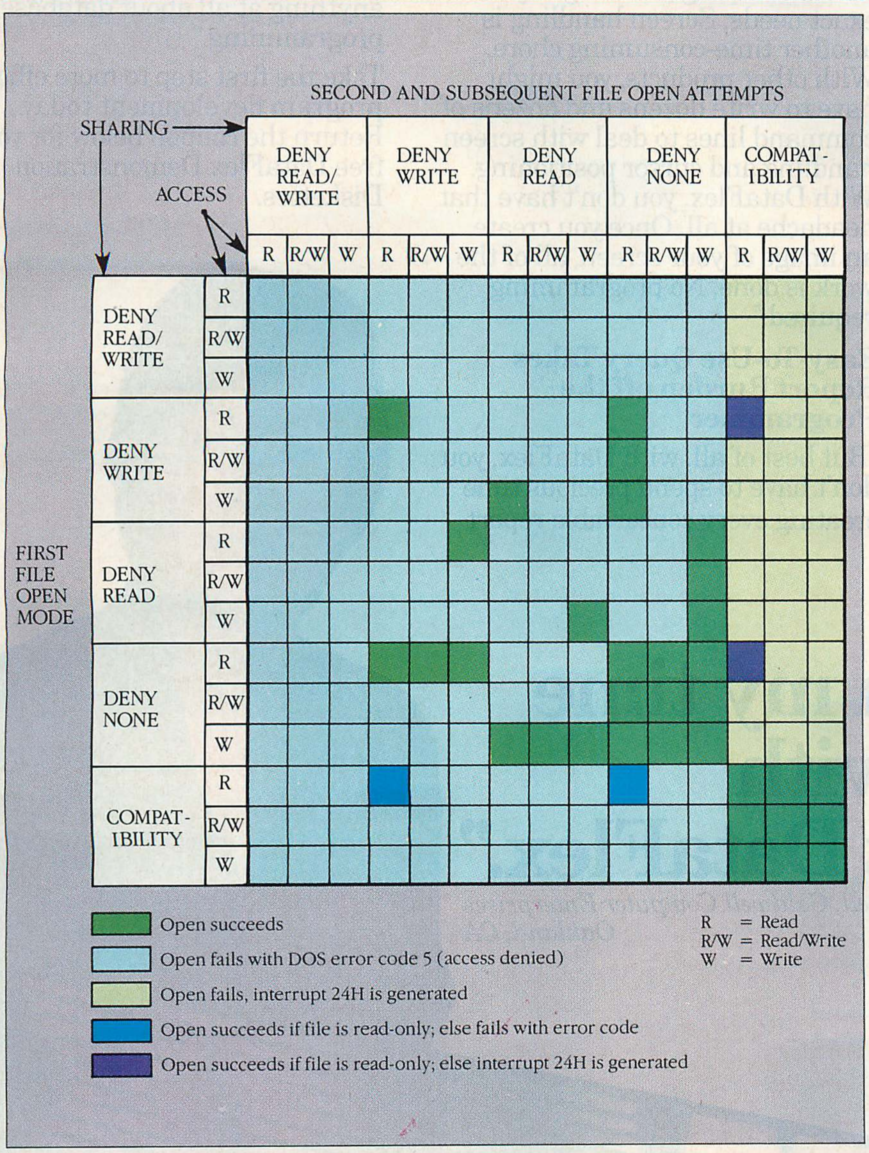
FIGURE 4: *File-sharing Matrix*



		SECOND AND SUBSEQUENT FILE OPEN ATTEMPTS														
	SHARING	DENY READ/ WRITE			DENY WRITE			DENY READ			DENY NONE			COMPAT- IBILITY		
	ACCESS	R	R/W	W	R	R/W	W	R	R/W	W	R	R/W	W	R	R/W	W
FIRST FILE OPEN MODE: DENY READ/ WRITE	R	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟨	🟨	🟨
	R/W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟨	🟨	🟨
	W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟨	🟨	🟨
DENY WRITE	R	🟦	🟦	🟦	🟩	🟦	🟦	🟦	🟦	🟦	🟩	🟦	🟦	🟪	🟨	🟨
	R/W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟦	🟦	🟨	🟨	🟨
	W	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟦	🟦	🟩	🟦	🟦	🟨	🟨	🟨
DENY READ	R	🟦	🟦	🟦	🟦	🟦	🟩	🟦	🟦	🟦	🟦	🟦	🟩	🟨	🟨	🟨
	R/W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟨	🟨	🟨
	W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟦	🟦	🟩	🟨	🟨	🟨
DENY NONE	R	🟦	🟦	🟦	🟩	🟩	🟩	🟦	🟦	🟦	🟩	🟩	🟩	🟪	🟨	🟨
	R/W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟩	🟩	🟨	🟨	🟨
	W	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟩	🟩	🟩	🟩	🟩	🟨	🟨	🟨
COMPAT- IBILITY	R	🟦	🟦	🟦	🔹	🟦	🟦	🟦	🟦	🟦	🔹	🟦	🟦	🟩	🟩	🟩
	R/W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟩	🟩
	W	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟦	🟩	🟩	🟩

🟩 Open succeeds

🟦 Open fails with DOS error code 5 (access denied)

🟨 Open fails, interrupt 24H is generated

🔹 Open succeeds if file is read-only; else fails with error code

🟪 Open succeeds if file is read-only; else interrupt 24H is generated

R = Read
R/W = Read/Write
W = Write

Most of the relationships in file sharing are predictable, as indicated above. Compatibility mode is quirky and should be avoided by newly written applications.

tire operation later. This deadlock situation is illustrated as follows:

Application A	Application B
WAIT(RECORD:100)	
	WAIT(RECORD:150)
	WAIT(RECORD:100)
WAIT(RECORD:150)	

A situation such as this points out a capability lacking in DOS 3.x—the ability to perform transaction processing efficiently and reliably. As a result, some LAN vendors provide proprietary calls to perform transaction processing. Novell, for example, supports the idea of an *atomic lock*, in which an application can request multiple record locks with a single call and will be rejected if even a single byte of any requested lock is being used by another application.

Semaphores. DOS also is lacking the synchronization operation known as a *semaphore*, a software "traffic light" that is visible to suitably written programs. The two fundamental operations of a semaphore are wait and signal. The wait operation checks to see if a semaphore is being used. If it is not, the applications can proceed and perform the operation. At the end of the operation, the application will signal the semaphore to indicate completion.

Applications must acknowledge the semaphore for it to work. Like a car running a red light, an application might choose to ignore a semaphore, which could lead to corrupted or lost data. For this reason, semaphores are more suitable for distributed applications that rely on multiple processes (such as simulation) rather than with applications that share a common database. Programs in the latter category are better served by DOS region locking.

Relatively speaking, a semaphore is a soft lock and DOS region locking is a hard lock. For region locking, the application must tell DOS where critical data are located within a file by specifying the offset into the file and how many bytes are to be locked. This allows DOS to reject a write request from a noncooperative application. In contrast, a semaphore's interpretation, and the compliance with that interpretation, depends entirely on the application.

One means of creating semaphores in DOS is to define a SEMAPHOR file stored on a certain server. Then, by always opening the file with Deny None sharing, the application could interpret each byte in the file as a semaphore number. For example, semaphore (byte) 10 could be interpreted to mean something like "wait until process *X* is completed." By invoking DOS function 5CH with a request to lock, the application, in effect, has performed a wait operation. The application would continue to attempt to lock the byte until DOS indicated the lock had succeeded. By invoking DOS function 5CH with a request to unlock, the application would perform a signal operation.

EXTENDED ERROR CODES

More exasperating than any feature missing from DOS is the variability of error information when using a LAN. Because much of the functionality of a LAN is not actually contained in DOS, the errors returned often reflect nuances in a vendor's implementation; thus, they must be treated carefully.

DOS 3.0 introduced function call 59H, which retrieves extended error information. Upon entry, register AH is set to 59H and BX to 0. Upon return, register AX obtains the extended error number, BH indicates the error class, BL indicates a suggested action, and CH, the locus. About 70 error codes exist that might be returned; the LAN error codes of note are listed in table 3. Interestingly, of the codes listed, only 32 (sharing violation) and 33 (lock violation) were defined in DOS 3.0.

Many of the error codes are fairly specific to PC LAN and/or NETBIOS and are returned only from NETBIOS emulators when writing applications for non-IBM LANs. The locus value in CH should be 3 when a network problem is detected, but all LAN-related errors may not set it consistently. Wherever possible, it is best to avoid creating de-

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pendencies on any but the most general error codes. (For more information, see "DOS Exception Handling," Dan Rollins, April 1987, p. 130).

OTHER LAN FUNCTIONS

Through interrupt 21H, DOS provides some LAN-related functions that are best avoided by portable LAN software. They are used by DOS itself or by networks such as IBM PC LAN. Access to the functions they provide is usually incorporated into each vendor's network shell.

DOS function 44H (IOCTL) includes three LAN-related subfunctions: 09H determines if a device has been redirected—programs such as CHKDSK use this call to avoid examining a network drive; 0AH determines if a file handle is local or remote; and 0BH sets retry counts and delays.

Function 5EH also has three LAN subfunctions. Subfunction 0 (get machine name) is supported by the IBM, Microsoft, Novell, and 3Com networks. Curiously, no corresponding function is offered for setting the machine name—that depends, instead, upon the implementation. This function would be useful in designing an electronic mail system in which a mailbox file for each user was created on a server using the machine name; however, because that name can contain 15 characters, a more complex scheme is needed.

Subfunctions 2 and 3 (set printer setup and get printer setup, respectively) set or get a printer set-up string that is sent to a printer just before the user output. The string could be used to select printer options, such as compressed or draft-quality output. Unfortunately, no "printer reset string" function exists to deselect options; subsequent printer users will be subject to the selections already existing from the previous print job unless they counter with their own printer set-up string.

DOS function 5FH contains two subfunctions to control device redirections. Calling subfunction 3 (redirect device) once a printer has been specified, the printer output is buffered and sent to the remote printer spooler for that device. Printers are redirected at the BIOS (interrupt 17H) level, not just the DOS level. If a file is specified, then a source drive letter is redirected to a destination network path. Device redirections are cancelled using subfunction 4 (cancel redirection).

TABLE 3: *LAN-related Error Codes*

CODE	ERROR
32	Sharing violation
33	Lock violation
50	Network request not supported
51	Remote computer not listening
52	Duplicate name on network
53	Network name not found
54	Network busy
55	Network device no longer exists
56	NETBIOS command limit exceeded
57	Network adapter hardware error
58	Incorrect response from network
59	Unexpected network error
60	Incompatible remote adapter
61	Print queue full
62	Not enough space for print file
63	Print file was deleted
64	Network name was deleted
65	Access denied
66	Network device type incorrect
67	Network name not found
68	Network name limit exceeded
69	NETBIOS session limit exceeded
70	Temporarily paused
71	Network request not accepted
72	Print or disk redirection is paused
84	Too many redirections
85	Duplicate redirection
86	Invalid password
87	Invalid parameter
88	Network device fault

These codes are returned from a call to DOS function 59H. Many are specific to NETBIOS or the IBM PC LAN Program, and should not be used for other vendors.

MULTIUSER DATABASES

Because virtually every true multiuser LAN application (including simultaneous file sharing, not just file lock out) is built on top of a DBMS (database management system) that, in turn, runs on top of DOS, LAN databases warrant discussion. Bringing a DBMS into a LAN opens up new capabilities, not the least of which is multiuser access. This can mean that an "unlimited" number of users have access to a database, but performance of the network and server will dictate otherwise. The vendor may restrict the number of users for licensing reasons. (See the accompanying sidebar "LAN Copy Protection." See also "Data Managers and LANs," Dave Browning, May 1987, p. 54.)

Whenever possible, the DBMS should also add value to DOS, such as providing additional user name/password security and audit trails of file usage. The security or integrity of a database file can be enhanced further by permitting different levels of access to records and even fields. Unfortunately, DOS provides no hooks for these features, so the application must supply its own methods of security.

If multiple servers are supported, then databases and index files may be split across servers for security, performance, or fail-safe operation. For example, an accounts receivable database may be on one server and the general ledger database on another, provided that the DBMS application integrates the two servers together. Under such an arrangement, failure of the general ledger server should not disrupt the operation of accounts receivable.

In a LAN environment, users are accessing records, changing them, adding new ones, and so on. In such a dynamic situation, the DBMS should provide an automatic retry mechanism on locked data. A user's request for data should not always be rejected the first time, because the desired data may become available a second or two later.

LANs provide some new choices to the designer of a data manager. One such choice is essentially an extension of the stand-alone PC design. The DBMS and the application both operate in the

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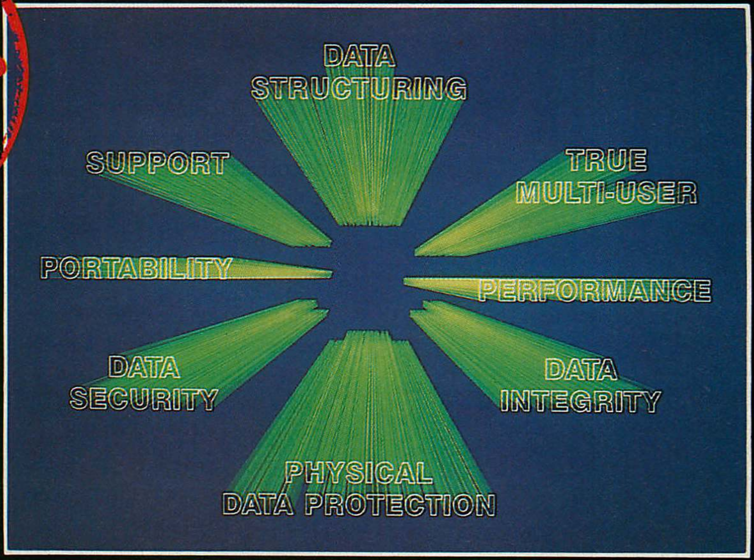

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LAN COPY PROTECTION

In the pre-LAN era of PCs, one copy of an application was sold for every user wanting to run it. A LAN presents pricing problems for software vendors because one copy of an application might be placed on a server and shared by many users. It is difficult to maintain a per-user price in a multiuser environment. Solutions include:

- Requiring each network user to purchase a copy of the package, even if it will be installed on a LAN.
- Site licensing—allowing the purchaser to make copies of the documentation for internal users and install it on any of their PCs or LANs.
- Providing an *N*-user package that has one set of diskettes and *N* manuals. Typically, the price is lower than for *N* single packages.

The first solution is straightforward, if not appealing, and the second one is more attractive to very large users. However, most LAN packages are sold under some variation of the third approach. Although most vendors of multiuser LAN software permit users to copy freely software to a server and to make backups, some use a copy-protection scheme in order to limit the maximum number of users that can access the application. This is accomplished in several ways.

The worst method (from a user standpoint) is to require a key diskette in the workstation. The application is loaded into a PC from a file server, executed, and then it checks for a key diskette in the PC's diskette drive or a *signature* on a hard disk. This technique is a carry-over from copy-protection schemes used on stand-alone PCs and is disappearing rapidly.

A better method is to license the software to a server and then have an installation procedure that reads the serial number from a key card or the unique LAN adapter address from the server. Most major vendors that market server hardware (Nestar, Novell, and 3Com, for example) offer this capability. Often, the LAN vendors themselves distribute their file server software in this manner. The major drawback to this approach is that the method varies among LAN vendors. The applications vendor must provide installation drivers for the different LANs in order to retrieve the file server's serial number (such as the NetWare file server key card number).

A LAN vendor could require that the software be installed for *N* number of PCs by having the purchaser supply the LAN adapter addresses of those PCs wishing to operate the software. Unfortunately, this multiplies the problem of the scheme above, as more different kinds of LAN hardware are available than are file servers.

The maximum number of users can be controlled: (1) via the fake semaphore scheme, (2) by creating a unique temporary file on a server each time the application is invoked and counting the number of open temporary files, or (3) by simply using a shared file with a length of one byte to indicate the number of current users. The user must be careful, however, to resolve problems such as users turning their machines off without exiting an application. DOS locks are not necessarily released when a PC is turned off. The second scheme is attractive because many vendor LANs occasionally poll a workstation to make sure it is still alive, and they close its files and release locks once they determine it is not.

The most interesting aspect of the various techniques to connect an application to a LAN is that they do not involve physically encrypting or changing the format of a diskette. Software can easily be copied onto the network from diskettes, but it will run only under certain conditions.

—J. Scott Haugdahl

same PC. This means that, in addition to the DBMS being loaded into every PC operating the application and consuming a lot of RAM (memory overhead), the DBMS must handle all of the file-access, record-locking details (CPU and LAN I/O overhead). (Ashton-Tate's dBASE III PLUS falls into this category.) A better approach has the PC acting as a back-end DBMS and handling all transactions in an orderly fashion as they are received from application PCs. This "DBMS server," or *back-end database*, may have its own hard disk or use a file server's disk. Security is also enhanced because users will not be able to modify the DBMS code. Some drawbacks are that the developer has to use interprocess communications protocols not provided by DOS but unique to a particular LAN, and that a failed DBMS server may mean that users will not be able to run the application.

OPERATIONAL PITFALLS

The predicaments that arise in operating DOS applications on LANs generally result from a misunderstanding of the use of an application (assuming it can be used on a LAN in the same way it is used on a stand-alone PC) or a procedural problem (thus the need for LAN administrators). Often, a vendor's LAN application is simply a warmed-over version of its original stand-alone offering. Mostly, DOS is not the culprit.

One procedural problem arises with the use of RAM disks. Users may find a particular operation too slow on a LAN and resort to temporarily copying a file from a server to a local RAM disk. If more than one user does this, obviously the last user to copy it back to the server has made that file the permanent copy. In such a case, the file-sharing safeguards imposed by DOS are circumvented and therefore nullified.

Shared printers seem to cause more problems than any other component. LANs give users access to a large variety of printers, including laser printers, and even plotters. In a common situation, the user sends a job to a printer that includes control strings to select unusual printer options, leaving the printer in some unknown state. The next print job may be interpreted as dot graphics when it should have been text. DOS addresses this problem with function 5EH, but in an incomplete and vendor-dependent fashion.

Fortunately, this situation has many acceptable non-DOS solutions, the simplest of which is to require all users to attach a printer reset string to the top of every print job. Another is to have the word processor automatically send a control string to the printer before the text (WordPerfect allows for such an action). Still another approach is to have the server include, in its banner page, a printer reset sequence.

This leads to another issue: control over printer selection. Most LANs can specify parameters such as printer type, where it is located, what type of form should be used, number of copies, and whether a banner page is desired. The most LAN-portable means to use these features is to configure them (using LAN-specific commands) before entering the application and to assign to one of the standard DOS printers (LPT1, LPT2, or LPT3) or communications ports

(COM1, COM2). However, not all LANs support network printing to all devices; some redirect only LPT1.

Some LANs, such as Novell's NetWare, require the user (not the application) to set these parameters before they are to use the network printers. Others, such as Nestar's system, allow an application to insert a control string (before the printer control string discussed above) to select which printer to use, number of copies, type of form, priority of job, and so on. The LAN-provided software that drives the shared printer must have operator control for setting forms, name of printer, etc.

Because output to LAN printers is spooled, the user often must decide when to actually send the spooled output to the remote printer. Many LANs provide an explicit command for this function. Some experience a time-out after so many seconds of not receiving data and automatically send the spooled output that has been received; this can lead to fragmented output jobs. Others (Novell, for example) automatically send the spooled output when DOS function calls are used and the printer handle is closed. Most networks offer some combination of these techniques.

Applications that directly access the printer or communications port hardware are not LAN-compatible: printer output cannot be redirected. A possible solution for such ill-behaved programs is to send printer output to a disk file, then print that file. Although many LANs redirect the BIOS printer interface and the DOS interface, the most portable strategy is to use DOS file open, write, and close calls for the printer.

Printers, however, are not the only difficulties confronting a LAN-compatible program. Suppose a text editor creates and uses a temporary file called EDIT.TMP in the current directory while it is running. If two operators on a LAN are using this editor in the same directory, they will both try to use this file, with undesirable results. Even a temporary file name based on the name of the file being edited is not guaranteed to be unique. The best assurance of creating a unique temporary file name is to use DOS function 5AH.

Another problem involves application defaults. If the defaults are not contained with the file itself, users may be faced with default settings they do not like or some that are not applicable to that file. In a single-user environment, defaults typically are placed in the directory where the application is installed, or possibly in the current directory. If the application is installed on a server, or multiple users operate in the same directory, this approach prevents users from selecting personal defaults. Worse, a change of defaults by one user affects all other users. One possible solution is to use DOS environment variables to specify the configuration settings or the location of a configuration file. This method also can be convenient to control the location of temporary files so the user can have them placed on a RAM disk.

THE MISSING LINKS

For most applications, DOS support for LANs is summarized by just two functions: open file and lock/unlock. To fit the model DOS provides, all information shared by a multiuser LAN application must be communicated through files. No functions are available in DOS that would allow, for example, two programs to communicate data by sending messages to each other.

It is hard to build a LAN environment with current DOS services. Some issues must be addressed using DOS and server processes.

Moreover, DOS currently offers no facilities for establishing sessions between applications. Protocols such as IBM's Advanced Program-to-Program Communications (APPC) or NETBIOS can be used, but then the application is, in essence, bypassing DOS. DOS provides but a tiny bit of the functions required at layer 7 (application services) of the Open Systems Interconnect (OSI) reference model as defined by the International Standards Organization (ISO)—the layer that supports end-user applications in a network. (The OSI model defines seven layers of architecture for use in the design of heterogeneous networks).

These missing links will only become standardized in future releases of DOS. As information becomes available about IBM's new Operating System/2 (OS/2, the recently announced 80286 protected-mode version of DOS), perhaps some of the gaps will be filled. Until then, de facto standards such as NETBIOS will have to suffice. Other issues that need to be resolved include security, audit trails, and fault tolerance.

For the present; it is difficult to build an efficient LAN environment entirely with DOS services (the infamous PC LAN Program versus Novell NetWare argument). Thus, these issues should be addressed using a combination of DOS and server processes. This is precisely the approach taken by OS/2, which can be used as a server to DOS-based workstations, as well as other OS/2 workstations. OS/2 also will support interprocess communications with other OS/2 workstations (but not with DOS 3.x).

But even though OS/2 is a major improvement, it would seem that DOS could add LAN support features without becoming overly complex. A wish list for DOS features includes interprocess communications, transaction support, and semaphores. In spite of OS/2, DOS 3.x will continue to serve well into the future as a platform for both stand-alone and LAN-based applications.

Ensuring that DOS applications are transportable from LAN to LAN requires the avoidance of dependencies on individual LAN workstation and server software. This signals the need for the creation of functions that are already available in some vendor's services, as was shown with semaphores.

Applications that merely need to access LAN resources can coexist with LANs if they follow some basic rules. They should open files using the new file sharing modes rather than compatibility mode. Wherever possible, they should use DOS services in preference to BIOS or hardware interfaces, especially for printers. Ambitious applications that want to use the multiuser potential of a LAN may find DOS seriously lacking. Although the file-sharing and locking features of DOS can mediate multiuser access to files, DOS cannot provide true interprocess communications. Operations such as semaphores and transaction processing must be implemented primarily by the application.

The practical implementation of LANs was hampered initially by DOS's lack of functionality. Now that DOS supports the bare LAN essentials, such as file and device sharing, it defines a standard for these functions. However, LANs are becoming more sophisticated, and DOS is again being pushed beyond its capabilities. Users can look to progressive developments in DOS (and its new sibling, OS/2) to deliver the next level of standardization.

J. Scott Haugdahl is a senior systems specialist at Architecture Technology Corporation, a Minneapolis-based consulting, publications, and seminar firm for data communications.

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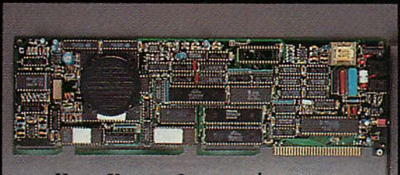
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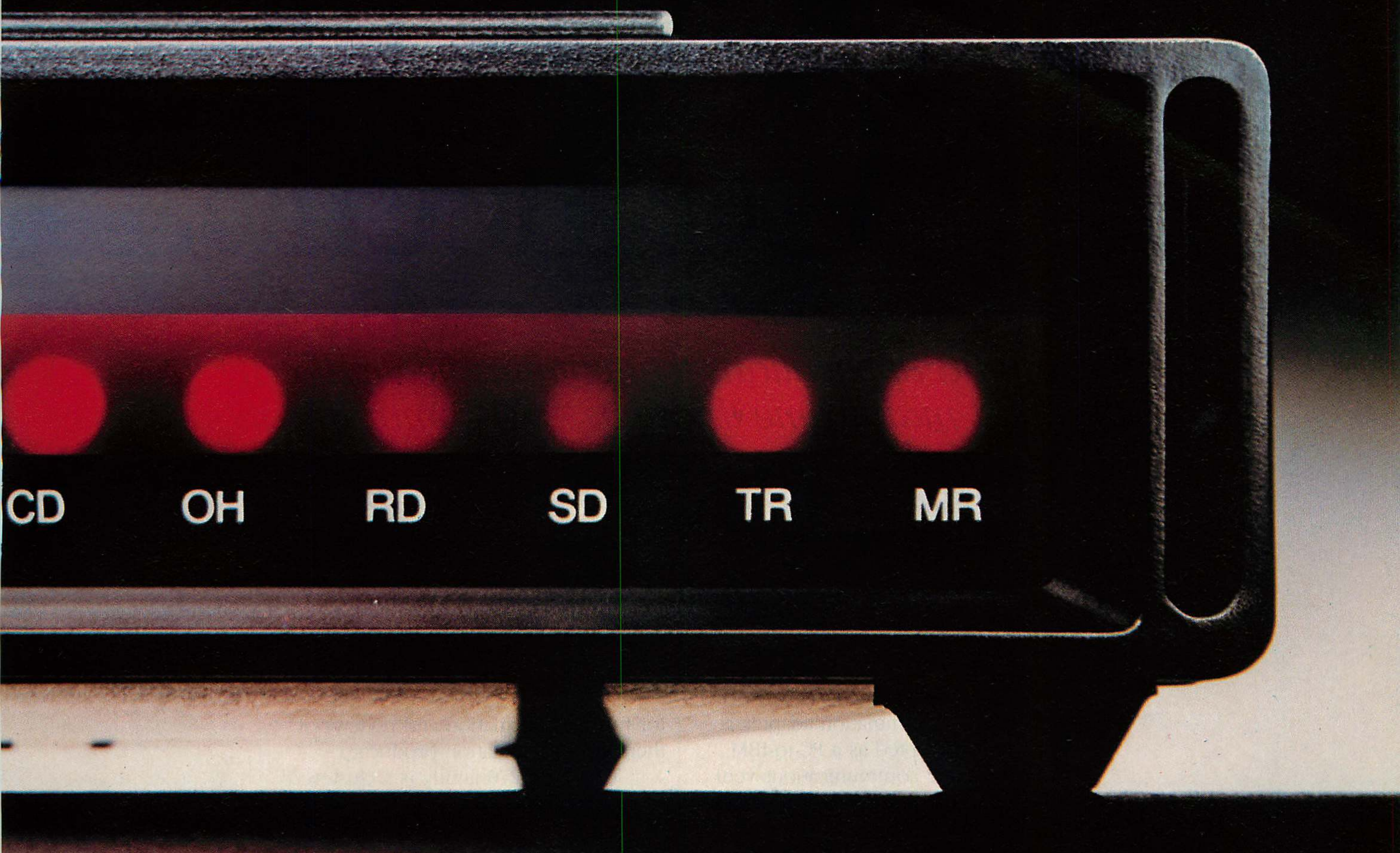

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Exploiting the 3270 Connection

Writing PC applications that communicate directly with a host mainframe through 3270 communication channels can be most effective, as long as potential problems are anticipated.

MARY DEWOLF

The 3278/79 emulation adapter is widely accepted as a PC-to-IBM mainframe communications vehicle largely because it works with an existing terminal network with no signal wiring or network changes. Although these boards generally are packaged with 3270 terminal emulator programs, powerful micro-to-mainframe applications can be developed by designing PC software that uses the adapter board to communicate directly with host applications. Unfortunately, many of the same features that have made the IBM 3270 terminal subsystem successful create unique challenges for the PC programmer implementing such a micro-to-mainframe application. The intention here is to highlight those areas in which associated program design decisions will be required, and to offer suggestions for avoiding common pitfalls.

To escape becoming "optioned" into immobility by the multiplicity of hardware and software alternatives available, this article will focus on the most common variety of coaxial connections: a 3278 emulator board, coaxially connected to an IBM 3274 cluster controller. (See "Emulating the 3278," Roger Addelson, February 1986, p. 48 for further information and reviews of then-current emulation products.)

The IBM 3270 family is a clustered system, in that 3278 terminals are cabled directly to a cluster controller, which serves as a concentrator/gateway to the host communications network. Cluster controllers usually are connected directly or by modem and telephone line to a 3705/25 communications controller, which serves as a communications front end to the mainframe. The cluster controller accesses the transmission line, sends and receives all data between terminal and host, and performs error recovery.

The 3278 terminal maintains the display buffer and accepts keyboard input for forwarding to the controller. The cluster controller accepts each keystroke, echoes it back to the display buffer, and forwards the assembled message to the host (when a key requesting transmission is pressed). On the output side, the controller accepts messages from the host and forwards them to the terminal for display. The 3278 emulator boards have microprocessors that perform the functions of a 3278 while maintaining dependence on the cluster controller. See figure 1.

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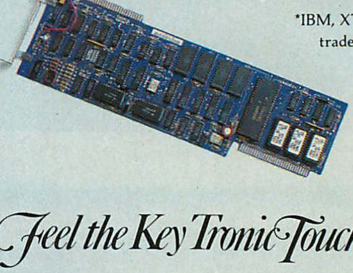

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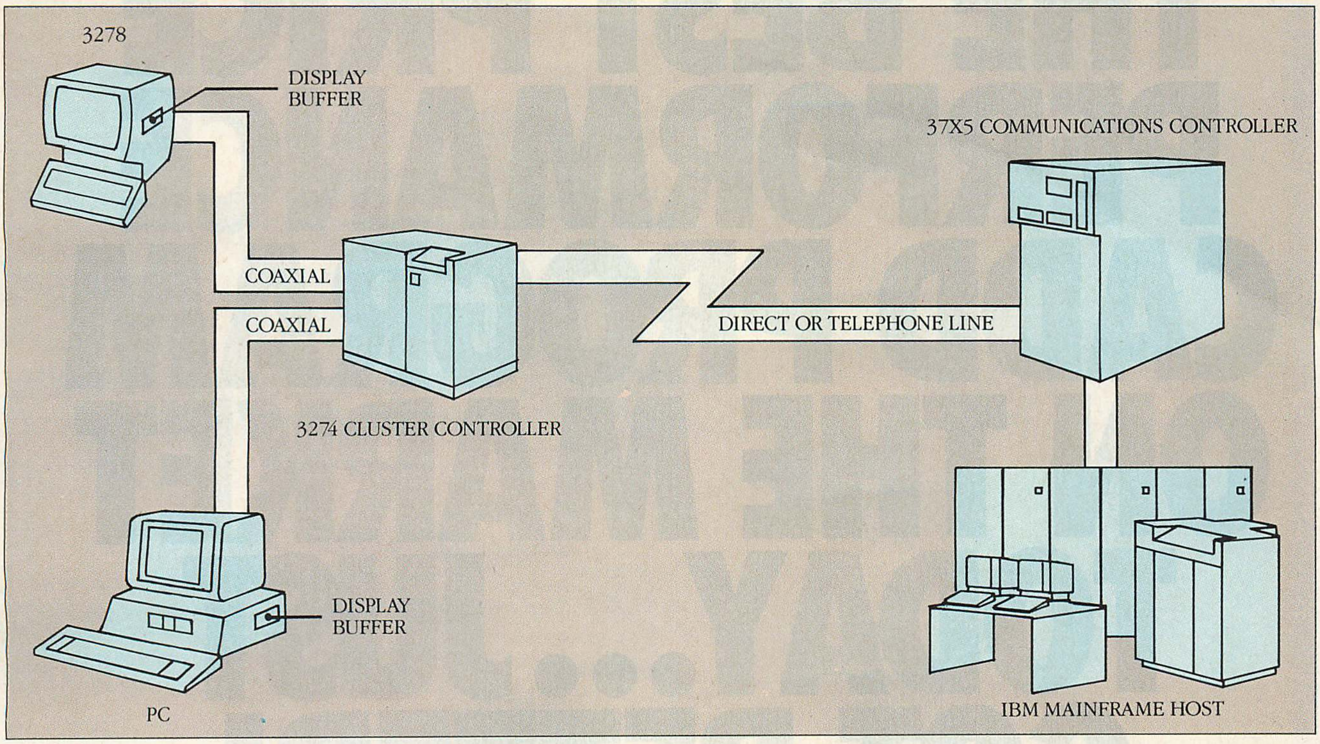
FIGURE 1: *IBM 3270 Terminal Subsystem*



The 3278 terminals and PCs that emulate the 3278/79 are connected via coaxial cable to a cluster controller, which serves as a concentrator/gateway to the mainframe host. Data are exchanged with the host via the terminal display buffer.

From the created PC application's viewpoint, this environment is very different from an asynchronous communications program. Instead of building a message in PC memory, the PC program simulates keystrokes (including the Enter key). Instead of receiving a host response, the program monitors the display buffer. The board emulates the 3278 terminal, but the application emulates the 3278 terminal operator. By so doing, the PC application is able to exchange data with a host partner application with no need for concern about the various protocol layers that connect them. See figure 2.

All of this is accomplished by posting commands to the coaxial board with OUT instructions and retrieving results with IN instructions, and each manufacturer's board requires its own coding. API (application program interface) support is available for some boards, but even that interface is likely to be manufacturer-specific. In general, coaxial board code should be isolated so that alternate versions can be supplied for other boards. And, because IN and OUT do not make use of DOS services, the PC application must explicitly check for and handle Ctrl-Breaks. Failure to do so can result in a program that cannot be interrupted without first rebooting the PC system.

Commands to the coaxial board include Simulate Keystroke, Read Display, Write Display, and more exotic functions such as Simulate Power-off. The PC application can do anything a 3278 operator can do, but little else. For example, it can inquire about cursor location, but no "position cursor" command is available because cursor position on a 3278 is controlled by the cluster controller, not the terminal.

A coaxial board is generally bundled with a terminal emulator program, the purpose of which is to transmit PC keyboard input to the cluster controller as 3270 keystrokes and to display the 3270 display buffer contents on the PC screen. A PC application interfaces with the coaxial board in the same way the emulator program does—but any relationship between data keyed at the PC or displayed on the PC screen and data keyed to the cluster controller or displayed in the coaxial board's display buffer, is optional. The PC keyboard and display are for communications with the PC user; the simulated 3270 keyboard and display are for communication with the host application.

In 3270 communications, the host gets its input from the display buffer, rather than from the keyboard. Keystrokes and most screen display activity is handled locally by the cluster controller. Data can be entered/erased/altered, the cursor moved, and endless strikeovers performed off-line from the host until the user is satisfied. Only when a specific transmission key is pressed will any host communications occur.

Host input from a 3270 is a uniquely formatted message containing a transmission key code, current cursor position, and the location/content of each transmitted data element. The host uses the screen location of a data element to identify the item; PC programs have no access to this data stream.

3270 KEYBOARD

The 3270 keyboard has three types of keys: text (alphanumeric), local control, and host transmission. Local control keys are handled by the cluster controller; they include cursor movement, erase, print, and some local-selection options such as cursor style and keyboard click. Host transmission keys request the cluster controller to transfer information to the host; these keys include Program Function (PF) keys, Program Attention (PA) keys, Clear, Enter, and SysReq. The Enter and PF keys send data with their transmission; other keys send cursor location and their own key code, but no text. Some of the transmission keys, such as Clear and SysReq, will be handled by other protocol

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layers in the network and never reach the host application.

Cursor movement is not context-sensitive because it is performed beyond the knowledge of the host application. The cursor keys always move one position in a given direction and the tab keys always move from field to field. (More about fields later.)

The Insert key does not push data out of a field, thus any attempts to insert data into a full-screen field will cause the keyboard to lock. *Filled* positions are screen locations containing anything other than a *null* character (00H), which, to a 3270, is quite different from a *blank* (EBCDIC 40H). Both the null and the blank display as spaces, however a blank is considered data whereas a null is not. All Erase keys, and Delete, replace data with nulls, never blanks. In cases where the host transmits trailing blanks to the display buffer, these must be deleted before insertion can take place.

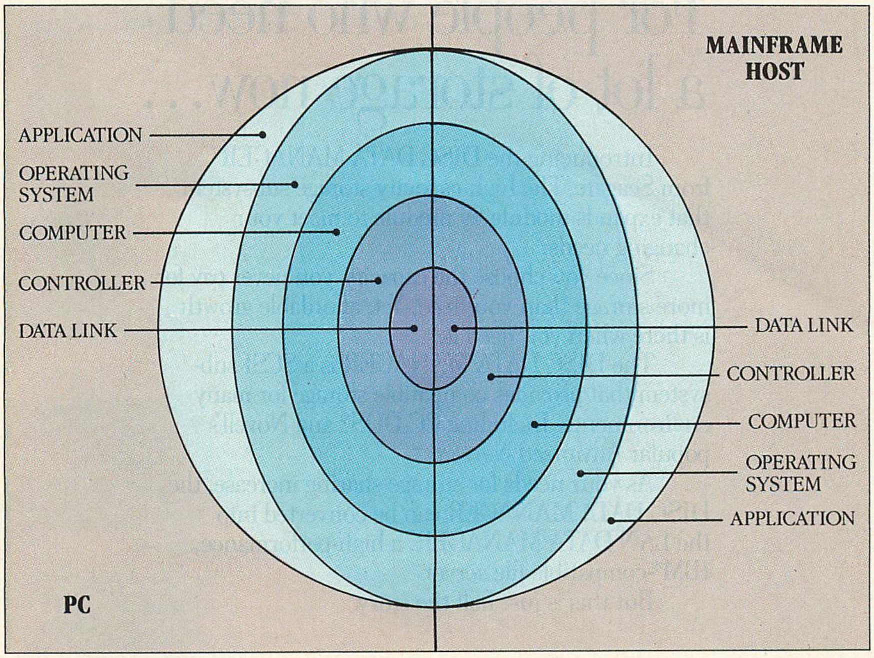
The 3278 sends keystrokes to the cluster controller as *scan codes*; the controller, in turn, forwards EBCDIC to the host. But with the variety of keyboards available for the 3278, a given scan code may not always represent the same key. (Further, on a half dozen or so foreign-language keyboards currently available, a given EBCDIC value does not represent the same character.)

As a result, scan codes are translated by the controller according to which keyboard it "thinks" a terminal is using, and at that point things get fuzzy. Older cluster controllers defined keyboard types when the controller was initially configured. Newer cluster controllers employ "I am a ________ cluster controller, what are you?" exchanges when terminals are switched on, but some coaxial boards do not respond to such identification queries. If certain scan codes are not working as expected (particularly PA keys, Clear, FieldMark), users should suspect a keyboard-type mismatch. To be certain, try the same key with the terminal emulator software provided with the coaxial board.

THE 3270 DISPLAY

A 3270 display is divided into *fields*. The field is a unit of data basic to all 3270 behavior: host transmission, erase, insert/delete, and tab functions all work on a field-by-field basis. Each field begins with an attribute byte that applies to the entire field, and ends when the next attribute byte is encountered. A field may extend across multiple lines, and, in fact, may cover the entire display area. Attributes, and thus field locations, are defined by host transmission, not from the terminal.

FIGURE 2: *Micro-to-mainframe Data Flow*



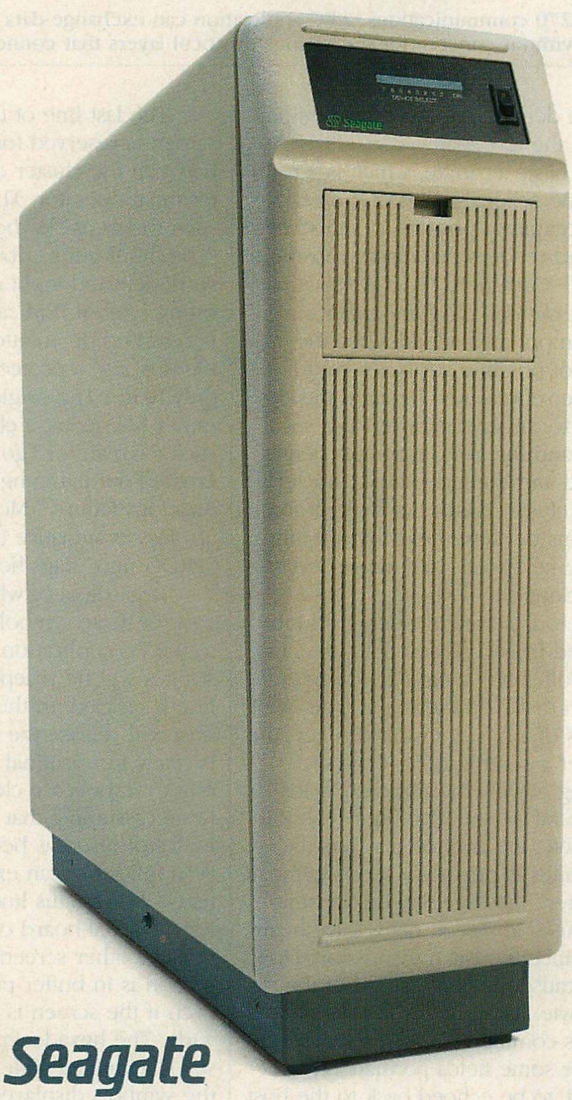
Using 3270 communications, a PC application can exchange data with a host application without concern for the various protocol layers that connect them.

The basic attribute, which is a remnant of the original 3270s of the early 1970s, occupies a position in the screen buffer and renders that display position protected. Current 3270 terminals also have an *extended attribute buffer*, a separate memory area added when the number of possible attributes could no longer be represented by eight bits. In addition to display characteristics such as color and intensity, attributes define protected and numeric-only characteristics. The cluster controller will enforce restrictions on these fields by rejecting ineligible keystrokes and, more severely, by locking the keyboard.

When data are either entered into or deleted from a screen field, the cluster controller sets a *modified data tag* (MDT) in that field's attribute byte. With the press of a host transmission key, the controller assembles a host message consisting of only those screen fields that have MDTs set. When transmission is complete, the controller resets the tags. If Enter is pressed a second time, a "null Enter" message will be transmitted because no screen fields have been altered since the last transmission. However, because the MDT is part of the attribute byte, it can be turned on by the host. It is common for host applications to render some fields permanently modified, to be echoed back to the host with every input.

The last line of the 3270 display screen is reserved for communications between the cluster controller and the terminal operator. This display indicates such things as "keyboard locked," "communications down," and some network-detected input errors. (One interesting symbol IBM calls "go elsewhere," is returned on an attempt to key ineligible text into a protected or numeric-only field.) The original symbols were rather like icons: a clock for "wait," a stick flagman for "go elsewhere," a crossed-out lightning bolt for "communications failure." More recent symbols are less imaginative (for example, "PROG nnn" flags host-detected errors).

Regardless of what they indicate, each of these symbols means one thing to the PC application: no further keystrokes will be accepted until the status line is cleared. In the case of "wait," the host will release the keyboard when it is ready for terminal input. Most of the other symbols are cleared by pressing Reset (assuming that the *cause* of the indicator also has been corrected). The PC application can examine the contents of the status line using the same Read coaxial-board commands used to retrieve other screen data. Status information is in buffer positions 0 to 79, even if the screen is more than 80 bytes wide. The hexadecimal values in the status area bear little resemblance to the symbols displayed on the screen, and may not even be in the same posi-



tions. These codes are undocumented, however, a little experimenting along with some examination of terminal-emulator source code, is usually sufficient to determine their meanings.

The status line also displays connect information in the lower left corner of the screen. The first position identifies the cluster controller (3274s display a 4). In SNA (System Network Architecture) networks, the second position identifies the host-connection level (PU-to-PU, PU-to-LU, LU-to-LU). If it shows a solid box, the user is logged onto a host system (IMS, CICS, TSO, or VM). If it shows a little face character, he is still at the VTAM level. And if the first position is blank, no cluster controller connection is present at all.

HANDLING HOST RESPONSES

Whenever the PC application sends a keystroke that requests transfer of information to the host, it should wait for a host response of some sort. That response may be data, a cleared screen, a repositioned cursor, or simply an unlocked keyboard. The program will receive no indication of host data arrival; it is up to the PC program to request data from the coaxial board's display buffer. It will need a watch loop to monitor the display buffer for changes. Host responses are interesting because of the variety possible and the realtime nature of the display buffer. The watch loop will need to provide for certain of the following conditions.

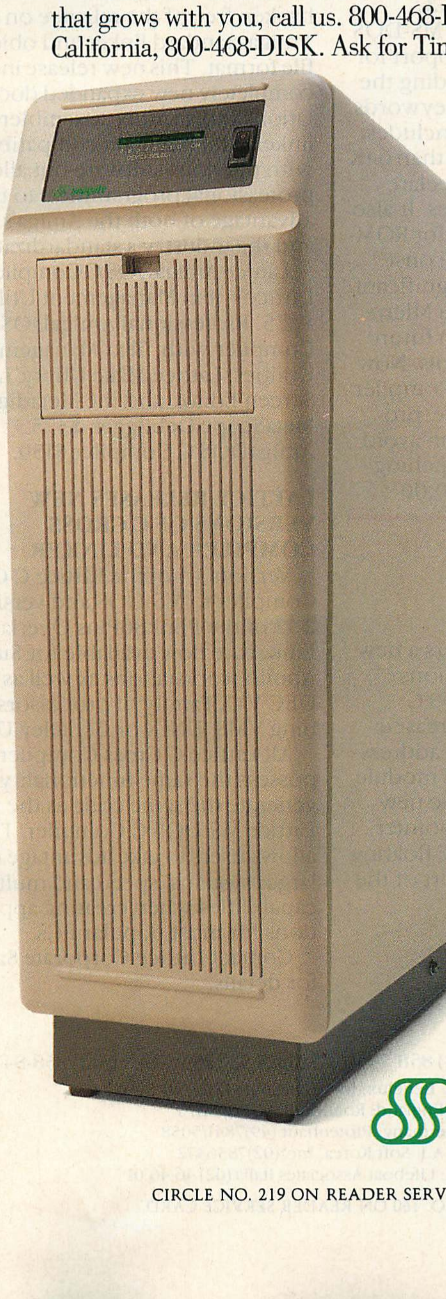
First, the host is not required to transmit a display panel in screen-position sequence. The middle lines of a display may appear first, followed by the upper and lower portions. Even if the host message is received in screen-position order, SNA does not require that an entire message arrive at once, or that segmented messages arrive in any particular sequence. On a heavily loaded controller, a screen may be filled in pieces. This happens because SDLC protocol allows the cluster controller to perform error recovery on one message segment without requesting retransmission of the others. Those segments of a display received correctly are forwarded immediately to the terminal/coaxial board; the erroneous segment is retransmitted, then forwarded out of sequence to the display.

Next, the message the PC application receives may not be intended for it. The mainframe host partner application (to which the PC is connected) is not the only program sending messages to the terminal. Batch programs often send Notify messages to TSO users upon completion. Messages from other terminal users may arrive after any Enter. Electronic mail systems transmit message-waiting prompts on an unsolicited basis. IMS/DC, in particular, is notorious for saving up yesterday's leftover messages and delivering them in response to today's input. Thus, the PC application must determine not only that a response has been received, but also whether it is the expected response. Once the message has been identified as being for the terminal, the PC program may then need to determine whether it is the current response or a response left over from an earlier input. (Leftover messages are discussed in more detail below.)

In addition, multiple messages may be received in response to one input, each one potentially overwriting its predecessor in the display buffer. This is most common during LOGON, when messages are being received from more than one network layer. TSO is prone to multiple transmissions when operating in line-by-line display mode.

Finally, the controller locks the keyboard when a host-transmission key is pressed, and releases it when the physical transmission is acknowledged by the host. Most host systems send a Keyboard Lock command back to the controller upon receipt of a message, in effect locking the keyboard until the actual host application responds. But a microinterval does occur between the ACK (acknowledgement) for the sent message and the execution of the host's Keyboard Lock, during which time the keyboard is free. A PC program can easily be misled into keying between the locks. It is generally necessary to provide a double-layer wait loop that first waits for a clear status line in the display buffer, then waits again to see if the keyboard is really unlocked before sending keystrokes. This is a difficult choice—the longer an operator waits, the more certain he can be, but such waiting takes a toll on performance.

In essence, the PC program must answer two questions: how will it know when the host has finished responding, and how will it know that the response received is the one it was waiting for? The best way to handle the first question is to watch for cursor movement. The controller executes Cursor Position commands only after the host's entire message has been successfully received and displayed. If the host application guarantees a change in cursor position, then the PC program can be sure that when the cursor moves, the host response is complete.



The Clear key is a special case. Clear precipitates host transmission, so a program should wait for the host's response before proceeding. But if the screen is already blank, the host's response will not cause any display-screen changes and the program will never know when that response occurs. This problem is solved either by inserting some meaningless characters into the display buffer, so that Clear results in display buffer changes, or by moving the cursor so that the host's Clear response will change the cursor position.

The second question is more complicated. The most common approach is to establish some sort of signature in the host message—a sequence number, a time stamp, or a certain attribute in an unusual location. This will depend on how much control the PC programmer has over the host application. Ideally, this signature will tell the PC application not only that this is indeed the message is intended for it, but also that it is the response to the last input.

Many coaxial boards provide a Write Data command that lets the PC application input data directly to the 3278 display buffer. Buffer input is performed independent of the cluster controller. Data input to the display buffer do not move the cursor and do not set the MDT; however, because the display's character set is constant across keyboard types, buffer input may be a better choice over the standard key simulation in multiple-language situations.

This technique improves performance, but it is also a bit like working on a tight-rope without a net. The controller assumes that values in the display buffer are either text bytes (which can be keyed) or attributes. Using direct Write Buffer commands, an operator can insert items that are neither. An actual 3278 cannot produce such values, so the cluster controller is not well defended against them. Especially in the case of corrupted attribute bytes, bad buffer data can crash a cluster controller, which can seriously inconvenience a number of operators in addition to the programmer. Because it is highly unusual, a crashed cluster controller signals vulnerability rather suddenly. However, with direct access to the cluster controller, recovery is a simple matter of pushing the IMPL button.

HOST SYSTEM INFLUENCE

Of the most common on-line systems, CMS and TSO are fully interactive, while CICS and IMS/DC are transaction-oriented. On-line production applications will execute more often under CICS or IMS/DC, while ad-hoc activities, such as editing, electronic mail, or end-user computing generally are based on TSO or CMS. Each of these systems includes its own terminal operator protocols. A PC application does not require great expertise in this area, but it will need to be able to respond to system prompts, request the next host display, and predict cursor locations.

TSO and CMS offer line-oriented input and output, but data will not be scrolled off the screen without permission from the user. When all lines are full, a permission-to-clear prompt is issued. If the user responds affirmatively, the screen clears and begins filling again at the top. TSO displays three asterisks in the lower left corner and waits for the Enter key to be pressed. CMS displays MORE or HOLDING in the lower right corner, and waits for the depression of a Clear key.

These protocols can occur with any host response that happens to fall at the bottom of the screen. In multiline responses, the permission-to-clear cycle can occur between lines. If the host ap-

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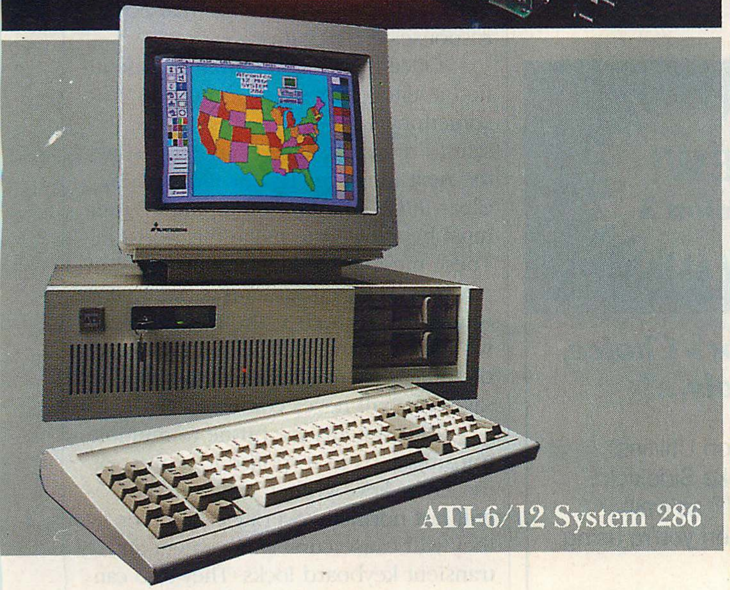

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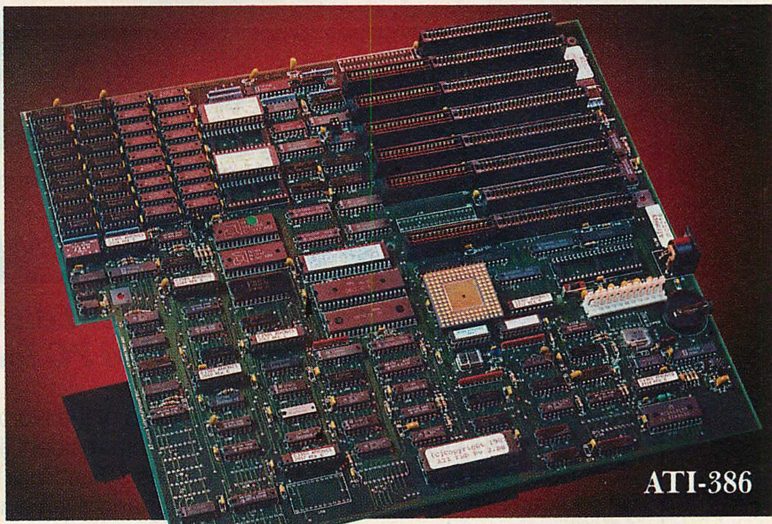

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plication is guaranteed to return less than a screen's worth of data, the PC application can avoid full screens by pressing Clear before each input. This will position an input message at the top of the display buffer, and ensure that 20-plus lines are available for the host response. It also provides predictable locations for received data.

LEFTOVER MESSAGES

The CICS and IMS/DC systems assume that a single input generates a single output, and that each host output will supply a full-screen display. Leftover messages occur when an application terminates prematurely, when a user shuts off the terminal before a response is received, when a message is sent to an unavailable terminal, or when a single application sends multiple messages in response to a single input.

IMS/DC is a queued message system. The keyboard is left unlocked during host processing, thereby allowing multiple inputs between responses. But IMS never sends more than one response to a single input. Thus, leftover messages can build up in the queue, and the response actually received by the PC application may have nothing to do with the last input. However, IMS has assigned the PA1 key for catch-up facilities. Pressing PA1 retrieves backlogged messages without creating a new host response.

In CICS, the keyboard is normally locked until the application responds. However, certain network definition options can leave keyboards unlocked before a response is received. The operator cannot assume in CICS that an unlocked keyboard signifies that no responses are pending.

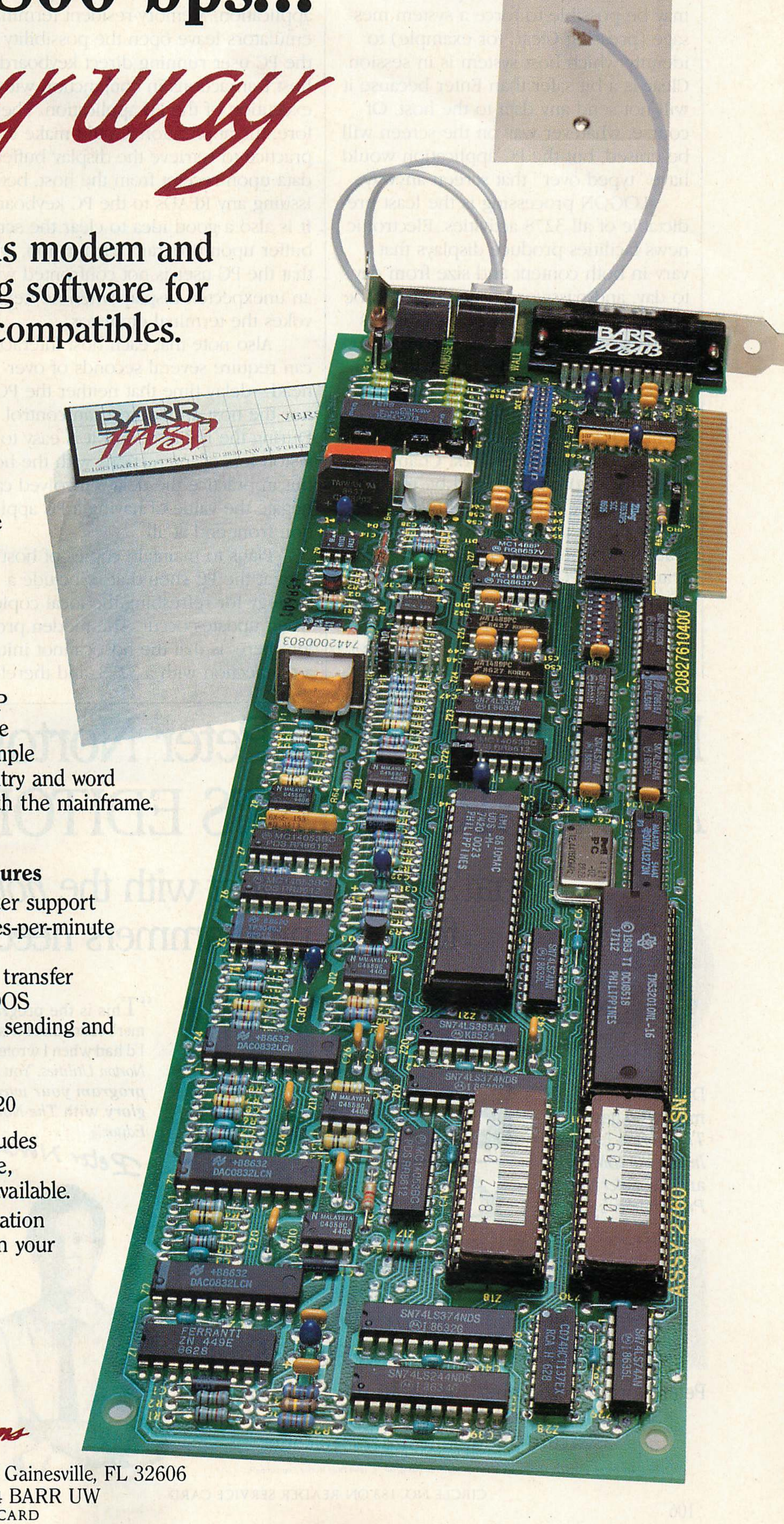
Once the PC application has identified a leftover message, it must do something with it. In some cases, it is safe to discard a leftover by requesting the next message (PA1 or PA2 in IMS, Clear in CICS); more often, the PC user must be allowed to make this decision. These messages seldom require host input from the PC user, and certainly not immediate response. The real problem with leftover messages is the possibility of endless waiting for an expected message that will never come.

TSO systems are prone to multiple transmissions in response to a press of the Enter key. While these messages will not normally overlay each other, they will cause cursor movement and transient keyboard locks. They also can mean that host-transmitted data are not at the expected display buffer location. When working in line-by-line mode in a TSO system, the PC application should wait for the "Ready" prompt instead of the host application's response. Ready is a dependable indicator that no further host transmissions will ensue before the PC application's Enter.

LOGON PROCESSING

Users that are connected by coaxial cable tend to LOGON to the host once, and stay logged on throughout the day, so the operator should not assume or require a connect/disconnect envelope around the PC application. The simplest approach is to let the user do his own connect and LOGON before executing the PC application. Of course this does not necessarily protect against program failure caused by a forgotten LOGON. A couple of methods are available to accomplish this.

If the PC is connected to an SNA network, the PC application can determine connect status from the status line. However, many host machines include more than one on-line system, and the status line will not indicate which of those systems is currently in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session. (Sending IMS transactions to a CMS session will not produce the expected host response.)

Depending on the application, it may be possible to force a system message (pressing Clear, for example) to identify which host system is in session. Clear is a bit safer than Enter because it will not send any data to the host. Of course, whatever was on the screen will be erased, but the PC application would have "typed over" that screen anyway.

LOGON processing is the least predictable of all 3278 activities. Electronic news facilities produce displays that vary in both content and size from day to day, and password processing can be a Pandora's box of responses (such as "This Password will expire in 5 days."). Mainframe security concerns will require user interaction during the connection process, and VTAM protocols will be different, even for separate nodes in the same network. Changes to the LOGON procedure will be made casually, since it is assumed that the instructions on the display screen will lead the user through the process. Programming a PC application to handle all of these possibilities is not an easy task. Programmers should, at a minimum, provide for escape from interminable "wait for response" loops.

EXTERNAL CONSIDERATIONS

Once the logistics have been resolved, some external considerations must be taken into account in designing the PC application. Memory-resident terminal emulators leave open the possibility of the PC user running direct keyboard-to-host transactions in conjunction with execution of the PC application. Therefore, the application should make it a practice to retrieve the display buffer data upon receipt from the host, before issuing any READs to the PC keyboard. It is also a good idea to clear the screen buffer upon program termination, so that the PC user is not confronted with an unexpected display when he next invokes the terminal emulator.

Also note that each host interaction can require several seconds of overhead—delay time that neither the PC nor the host application can control. During the initial design it is easy to envision lots of interactions with the host, but in practice the delays involved can negate the value of having a PC application front-end at all.

Plans to maintain copies of host data at the PC should also include a strategy for refreshing the local copies when updates occur. The hidden problem here, is that the host cannot initiate a connection with a 3278, and therefore cannot automatically update PC copies. In addition, unattended log on to the host by the PC will usually be disallowed on security grounds.

Because the host program's terminal output screen has been supplanted by the emulation board's display buffer, the host program has no direct access to the user. The PC application thus should include some provision to display host system error messages. Such a facility should be limited to unexpected error situations, and should not used for normal data-validation errors. In this triangle of host program/PC program/user, the PC application is responsible for the PC display screen. A pass-through message should not disrupt the logic or coherence of that display.

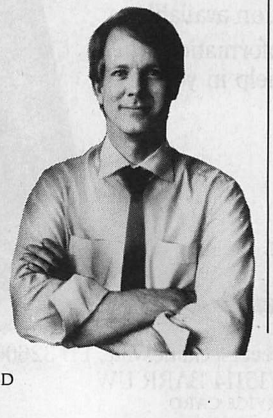
If the PC application is sending data to the host, controls must be built in to avoid duplicate transmissions. At the same time, retransmission must be provided for in the case of failed connections or data being rejected by the host. The simplest approach to this situation involves two rules:

1. The receiving program either accepts or rejects a transmission as a unit. Accepting part of a message, and rejecting another part, invites either duplication or lost data.
2. The sending program retains the transmitted data until acknowledgement is received from the receiver, and then deletes the data immediately. In a situation such as this, IF ERRORLEVEL tests in .BAT files can be used to great advantage.

Finally, PC programmers should be prepared for concern about security from the mainframe contingency, although most requirements can be met easily. Concerns include LOGON procedures (passwords must be entered at the keyboard, not displayed, written to disk, or maintained in memory), updating mainframe databases from remote copies (a data-integrity, rather than security, issue), and an agreement to simply not keep sensitive data in PC files.

The local interactivity possible with a PC can amplify the value of a mainframe application, and the power and data availability of the mainframe can significantly enhance a PC application. Both are possible with a coaxially connected application. The key to success is a good understanding of what the PC application should expect from the 3270 "display," and what the host application expects from its "user."

Mary DeWolf is the proprietor of This is How, a Morristown, New Jersey, consulting firm specializing in PC-host applications.



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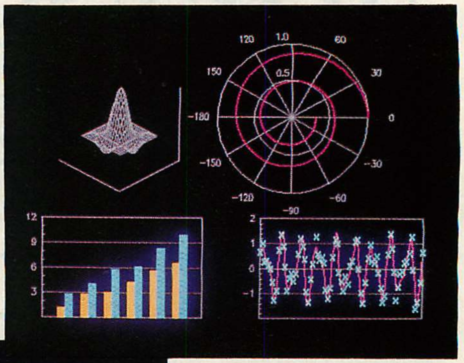

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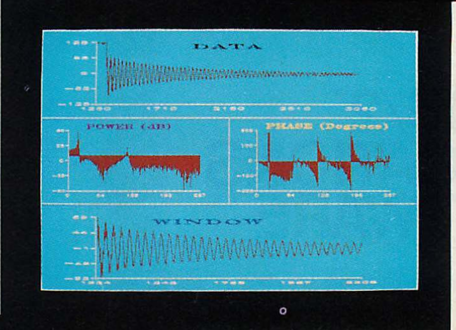

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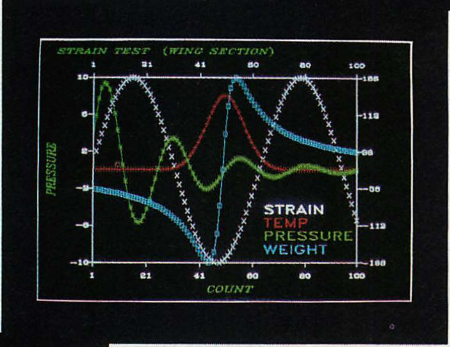

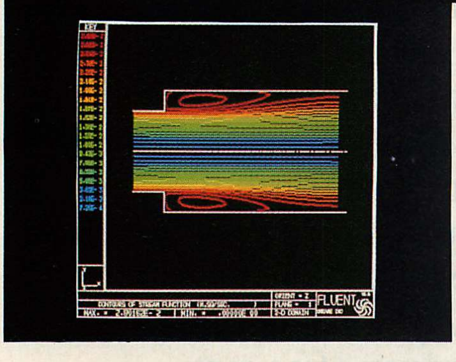

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The Windows for C subset has all the windowing functions without data entry. Unlimited windows, defined in C structures for reference throughout your program, can be made either to pop up or permanently overwrite the screen. Routines scroll and highlight lists with arrow keys, read and scroll ASCII files both ways in windows. Logical treatment of video attributes permits unchanged programs to run on color or monochrome. Colors of windows are set individually. All functions are in separate modules. Only those used are linked. Only buffers holding on-screen or temporarily obscured windows occupy RAM; others released dynamically. Clear documentation.

Specify compiler:	List:	PC Brand:
Windows for Data	**$195**	**$149**
Windows for C	**$295**	**$259**

INTERACTIVE-C

Intrepreter, Editor, Debugger

Interactive-C™ is a fully integrated environment: a complete K&R interpreter bound to its own editor and "the best debugging facilities of any," says *Computer Language*, 2/87. Adjustable edit, command, and status windows, second screen for program output. Or twin CRTs. Can load object code of your compiled functions or commercial libraries. Immediate mode, syntax checking both when you type and run, and cursor that points precisely at errors. Debugger includes breakpoints, watchvalues, stepping options, interactive changing of variables. List: **$249**, PC Brand: **$219**.

LATTICE C COMPILER

The Most Widely Used C Compiler by Far

The compiler that put C on the PC. More programmers use Lattice than any other. Its huge libraries (325 functions!) enable the file-sharing and record-locking provisions of DOS 3.1, provide full transcendentals, and utilities to mimic the UNIX™ and XENIX™ environments. Embraces key UNIX enhancements: void functions, enumerated data types, data passing between structures by assignment. Defaults to the ANSI proposed standard, but command line options offer leniency. Also ANSI checking of external data types to swat bugs at link up.

You get small .EXE files, very fast link times and efficient aliasing. New options generate code to use 80186 and 80286 features; 88087 sensed and utilized. *PC Journal* review of 12 compilers called Lattice "a fine product to consider for the production of important applications." Ask for: S0100. List: **$500**, PC Brand: **$299**.

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Outside the United States? Our prices have plunged! Look what has happened to prices of programming tools in these major currencies:

		9/1/85	Press Time
Btrieve	DM	550	355
GSS Kernel	FF	3,200	2,260
Windows/Data	SF	600	389
C-Tree	Yen	78.500	46.980

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BLAISE *C Tools Plus*

Nothing pays you back quicker than a function library, and Blaise has long been known as a great one. C Tools Plus, the top of the line, now has over 200 functions. Mature, tight, predominantly in C, they isolate hardware dependence, come in source and library, with no royalty. The rundown:

Screen Handling: either via BIOS or direct to video adapter; supports EGA, 43-line mode and multiple pages, twin monitors. Windows: any number, stackable, writable, wordwrapable, and erasable. Interrupts: well known for interrupt service routines in C, from which you can now access DOS functions. Directories: Create, change, or search directories, rename files, get and change their date/times. Memory: control DOS memory allocation, load a "child" process alongside your program, even create memory-resident programs—and remove them. Strings: international money, dates and character sets, plus superfunctions to perform several tasks with a single call. General: BIOS and DOS gates for direct access, memory copy, speaker control, it goes on. Our complete Blaise line:

	List:	PC Brand:
C Tools Plus	**$175**	**$117**
Asynch Manager	**$175**	**$117**
View Manager	**$275**	**$164**
Turbo Asynch Plus	**$100**	**$ 67**
Turbo Power Tools +	**$100**	**$ 67**

BTRIEVE

ASK US ABOUT XTRIEVE & REPORT OPTION

Queen B-tree File Manager Abdicates Royalties

There's no longer a tithe to incorporate Btrieve™ in applications, a welcome proclamation if royalties would ruin your profit margins. Btrieve takes complete charge of all file creation, indexing, reading, writing, insertion, deletion, space recapture, forward and backward searching. It builds function call "commands" right into the language you use: interfaces to C, Pascal, BASIC, and COBOL, with sample programs in all four, come with each copy.

Btrieve has mainframe specifications! Its balanced-tree indexing scheme finds any key in a million in four or less accesses. Files may have up to 24 indexes; fixed record length to 4090 characters; indexes up to 255 characters; files of 4 billion bytes. Can even extend a file across two drives — even two hard disks!

Version 4.x speeds DOS interaction for large multiply-keyed files; enables variable length records of virtually any length; verifies accuracy (optionally) with read after write, useful in gritty environments; offers password and data encryption.

There's also Xtrieve, for Btrieve file inquiry and data manipulation, and Rtrieve for report writing. All three in versions for any network that supports the MS-DOS 3.1 file sharing function.

Ask for:	List:	PC Brand:
S0650	**$250**	**$195**
S0652 Network Version	**$595**	**$465**

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SUPER SOURCE

Two great debugging and documentation tools that support C, Modula, Pascal, BASIC, and dBASE:

Source Print

Author Alan Simpson writes "the best overall debugging technique is to... draw lines to connect all the IFs and DO WHILEs etc. with their ENDIFs and ENDDOs. Use a pen or pencil to..." Well thanks, Alan, but we'll let Source Print do it for us. It draws vertical lines to connect all such beginnings and endings in a vivid display of your program's organization. And it can print programs with page numbers, headings, line numbers, indent automatically, throw in a table of contents and a cross-reference index. About Source Print *PC Magazine* said, "Occasionally a utility comes along that makes a programmer's life much easier." List: **$75**, Ours: **$60**.

..and Tree Diagrammer

Tree Diagrammer prints an organization chart of your program's structure showing the hierarchy of function, procedure, and subroutine calls. Shows at a glance what routines call each other for clearer debugging. Every shop should have this important documentation tool. List: **$55**, Ours: **$45**.

GREENLEAF

Functions

C source, assembler source, and binary libraries of 225 functions for many compilers. Stresses tight functional groupings to minimize loading code your application may never use. Manual's 250 pages help select functions, as do demos, bulletin board. Has DOS extensions, powerful string pointer manipulations, screen tools even to the pixel level, graphics primitives, keyboard, register and memory status, F-key assignment, time/date, peek, poke, plenty more. Specify compiler. List: **$185**, Here: **$139**.

Communications

Communicate from within your own C programs! Over 120 functions and demo programs in C and assembler source to set up interrupt-driven asynch communications for up to 16 channels. Up to 9600 baud, ASCII or binary, any parity or word length, 8250 UARTs, Xon/Xoff and Xmodem, WideTrack receive. Specify compiler. List: **$185**, Us: **$139**.

BASTOC OPTIMIZES!

Translates BASIC Into C

For a trifling price, BASTOC™ moves truckloads of BASIC over to C. It's a translator which takes in Microsoft Extended BASIC and emits pure K&R C for Microsoft or Lattice. Structures even convoluted BASIC code. Optimized to dramatically reduce execution time. Dynamic string allocation ends BASIC's catatonic garbage collection. Huge worksaver. List: **$495**, PC Brand: **$399**.

RYAN-McFARLAND

Killer FORTRAN OPTIMIZES!

Complete implementation of FORTRAN-77, the first PC FORTRAN certified by the GSA at the highest level. Why? It's a mainframe compiler moved to PCs. Your programs can wander between all sizes of machines. Programs up to 640k (bigger with overlays), arrays over 64k, long list of VS, VAX and FORTRAN-66 extensions. Has debugger, overlay linker. R-M has written FORTRAN compilers for IBM, DEC, etc. for 20 years. No greater expert. List: **$595**, Us: **CALL**.

PANEL PLUS *Library Source Code Gives It Complete Portability*

NEW! NO ROYALTIES!

There are no end of tools for screen design and data entry, but none quite like Panel Plus. Design a screen under program control, use Panel's utility to "run" and test it field by field, then pass it to Panel's code generator which delivers C source code. Options style the code to your compiler's liking, and you can of course do what you like to the source afterward. The code calls Panel Plus's function library, but now *the library comes in source*, so everything produced is highly portable. Not like other screen managers delivered as object libraries and which leave *you* to write the detailed code.

Panel Plus will operate in graphics mode via interfaces to graphics products it supports and can utilize the EGA's 43-line screen. Low-level I/O functions adapt it to various keyboards, screens, operating systems.

Panel's newest incarnation has every imaginable feature. A single screen design can have 1000 fields stacked as visual overlays up to 127 levels deep or as pop-ups. Groups of fields can be moved between levels. Screens can be output as compilable code or stored on disk for loading at run-time. Each field can be boxed, colored, multi-row, word-wrapped, and scrolled horizontally and vertically if larger than its on-screen view aperture. It can be assigned its own help and error message, can be told to accept certain characters, or to match a picture, and to check data after entry—proper dates, number ranges, etc.—using Panel's or your own validation routines. You can add your routines to Panel's test utility because even it comes as source. Fields are accessed in any order and control reverts to your application program after each field for choice of action.

For past Panelists, the *new version has* smaller and faster field and screen functions, tighter granularity, and an enhanced, reworked library. Major tool for the serious developer. List: **$495**, PC Brand: **$395**.

Shopping List for the Power Workbench

ASSEMBLERS & DEBUGGERS	LIST	US
Advanced Trace-86 *Morgan, ASM Interpreter*	175	119
C-Sprite Debugger *by Lattice, source level*	175	139
Microsoft Macro Assembler *with Utilities*	150	109
PASM86 *by Phoenix, Macro Assembler*	195	125
Periscope I Debugger *from The Periscope Co.*	345	299
Periscope II *w/NMI Breakout Switch*	175	139
Periscope II-X *software only*	145	105
Pfix86 Plus *by Phoenix, Symbolic Debugger*	395	235
BASIC LANGUAGE		
Microsoft BASIC Interpreter *for XENIX*	350	295
Microsoft QuickBASIC Compiler *full BASICA*	99	79
BORLAND PRODUCTS		
Reflex & Reflex Workshop	200	129
Reflex *Data Base System*	150	89
Reflex Workshop	70	45
Turbo Basic...*New*	100	64
Turbo C Compiler...*New*	100	64
Turbo Lightning	100	64
Turbo Pascal & Tutor...*New*	125	85
Turbo Pascal with 8087 & BCD	100	64
Turbo Tutor	40	28
POLYTRON PRODUCTS		
PVCS Corporate...*Source Code Control Syst.*	395	309
PVCS Personal	149	109
PVCS Network	Call	Call
PolyMake *Complete Make Utility*	149	109
PolyLibrarian *Library Manager*	99	73
PolyLibrarian II *Library Manaer*	149	109
PolyShell *UNIX-like Command Shell*	149	109
PolyXREF *Complete Cross Ref Utility*	219	169
PolyXREF *One language only*	129	99
PolyBoost *The Software Accelerator*	80	64
PolyDesk III *3rd Generation Desktop Org*	99	73
PolyDesk III *Add On Tools*	Call	Call
DATA BASE MGMT		
BRIEF/dBRIEF...*Brief for DBASE III*	275	Call
CLIPPER...*from Nantucket*	695	Call
McMAX...*dBASE for MAC from Nantucket*	295	Call
dBx...*dBASE to C Translator by DESKTOP AI*	350	299
with Library Source Code	550	469
with Full Source Code	1000	855
dBC...*from Lattice...maintains DBASE files*	250	195
with source	500	390
dBC III Plus...*supports multi-user DBASE*	750	595
with source	1500	1185
C COMPILERS		
C86 PLUS *by Computer Innovations...New*	497	397
Lattice C Compiler *from Lattice*	500	299
Let's C Compiler *by Mark Williams*	75	55
with CSD Source Level Debugger	125	90
MWC-86: Mark Williams C Development	495	369
Microsoft C Compiler *4.0*	450	295
C INTERPRETERS		
C-Terp *by Gimpel Software*	300	249
Instant C *by Rational Systems*	500	395
Interactive-C *by IMPACC with debugging*	249	219
RUN/C Professional *from Lifeboat*	250	185
TEXT EDITORS		
Brief *from Solution Systems*	195	Call
Edix *by Emerging Tech...Multi-screen*	195	159
Epsilon *by Lugaru Software, like EMACS*	195	149
FirsTime *by Spruce Technology, C syntax*	295	229
Kedit *by Mansfield, similar to Xedit*	125	99
LSE, the Lattice Screen Editor *Multi Window*	125	100
Pmate *by Phoenix, with Macros*	195	115
Vedit *by Compuview*	150	99
Vedit Plus *by Compuview*	185	129
FILE MANAGERS		
Btrieve *by Softcraft, no royalties*	250	195
Btrieve Network *by Softcraft*	595	465
C-Tree *by FairCom - no royalties, source*	395	329
R-Tree *by FairCom-Report Generator*	295	245
	LIST	US
C-Tree & R-Tree Combo *by FairCom*	650	541
dbVista *single user DBMS by Raima*	195	139
dbVista *multi-user DBMS*	495	399
Opt-Tech Sort *Can sort Btrieve files*	149	105
SCREEN DESIGN		
Curses *by Lattice, UNIX screen designer*	125	99
with Source	250	199
Greenleaf Data Windows......*New*	225	169
with source	395	297
Panel Plus *by Round Hill, no royalties......New*	495	395
View Manager for C *by Blaise*	275	164
Vitamin C *by Creative Programming*	225	198
VC Screen *by Creative Programming*	100	81
Windows for C *Vermont Creative Software*	245	216
Windows for Data *includes Windows for C*	395	349
ZView *Data Management Consultants*	245	175
GRAPHICS		
Essential Graphics *by Essential, no royalties*	250	210
GSS Graphics Development Toolkit	495	375
GSS Kernel System *by Graphic Software*	495	375
GSS Metafile Interpreter	295	235
Halo *by Media Cybernetics*	300	219
with **Dr. Halo II**	440	299
Halo for Microsoft *includes all fonts*	595	434
COMMUNICATIONS		
Asynch Manager *by Blaise, for C or Pascal*	175	117
Greenleaf Communications *by Greenleaf*	185	139
PTel *by Phoenix, Binary File Communicator*	195	115
UTILITY LIBRARIES		
Blaise C Tools Plus	175	117
Blaise C Tools	125	84
Blaise C Tools 2	100	67
C Food Smorgasbord *by Lattice*	150	109
C Utility Library *by Essential, 300 functions*	185	139
Greenleaf Functions *by Greenleaf Software*	185	139
PforCe *by Phoenix, vast library*	395	235
DEVELOPMENT TOOLS		
Code Sifter *by David Smith Software, Profiler*	119	89
Dan Bricklin's Demo Program *Prototyper*	75	69
LMK from Lattice *by Lattice, "make" like UNIX*	195	149
Microsoft Window Development Toolkit	500	365
PC-Lint *by Gimpel Software, after UNIX's "lint"*	139	125
PFinish *by Phoenix, EXE performance analyzer*	395	235
Plink86 Plus *Utilizes memory for overlays*	495	325
Pmaker *by Phoenix, like UNIX "make"*	125	85
Pre-C *by Phoenix, UNIX "lint"-alike*	295	174
Pfantasy Pac *six Phoenix products...New Price*	995	Call
OTHER TOOLS		
BASTOC *by JMI, convert BASIC to C*	495	399
BASIC-C *BASIC's functions added to C*	175	139
Report Option *by Softcraft, Btrieve Report Gen.*	145	128
Xtrieve *by Softcraft, Query Utility for Btrieve*	245	220
FORTRAN COMPILERS & UTILITIES		
RM/FORTRAN *by Ryan McFarland*	595	Call
FORTRAN Libraries...*by Alpha Computer*	70	45
Microsoft FORTRAN *Links with Microsoft C*	450	281
Microsoft FORTRAN *for XENIX*	695	546
Scientific Subroutine Package *by Alpha*	295	239
OTHER LANGUAGES & UTILITIES		
RM/COBOL *by Ryan-McFarland*	950	Call
RM/COBOL-85 *ANSI 85 COBOL*	1250	Call
RM/NET + 5...*COBOL & COBOL 85 Network*	300	Call
Source Print...*source code formatter*	75	60
Tree Diagrammer...*source code diagrammer*	55	45
Microsoft COBOL Compiler	700	499
Microsoft COBOL Compiler *for XENIX*	995	795
Microsoft Lisp *New Common Lisp*	250	189
Microsoft MuMath *includes MuSimp*	300	199
Microsoft Pascal Compiler *Links with M'soft C.*	300	199
Microsoft Pascal Compiler *for XENIX*	695	546
PDisk *Phoenix's new disk manager*	195	125
Help/Control *by MDS...123 style Help*	125	109

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BRIEF *NEW! Version 2.0 Extends Lead*

Brief has come forth with version 2.0 offering editing templates for added languages, faster undo and search with matching over multiple lines, new types of block marking, large screen support, new documentation, and tutorials.

This runaway success has eclipsed all other editors by sporting every feature you've ever contemplated. Text, from keyboard or files, is housed in multiple buffers, and scrolled through one or more windows you open, close, resize. A text buffer may be called to different windows to view two areas at once. A change in one changes both. Text may be marked for printing, writing to files, movement to scrap buffers for cut and paste into other buffers or deletion, with as many backward "undos" as you want.

With a growing list of C compilers, you can compile without ever leaving Brief. It grabs the compiler's report of problem lines, and marches you through your source code for repairs.

Parts of Brief were written with its own Lisp-like macro language which has structure, 32-character variable names, conditional execution, loops, and even readability. Nothing like the hieroglyphs we've seen elsewhere. Bulletin board and public domain disks with macros. "One of the best investments you can make," *PC Magazine.* To top it off, there's a 30-day money-back trial period. List: **$195**, Us: **Call.**

CLIPPER *From Nantucket*

Compile dBASE for Speed, Protection

Clipper™ turns lumbering dBASE® into a speed dMON with benefits bobbing in its wake: your source code is submerged from public view, you can distribute your compiled application without royalties, and your customers don't even need copies of dBASE! The Spring '87 Clipper offers index files compatible with dBase III Plus, and networking capabilities to run compiled programs on major networks supporting DOS 3.1 with no restrictions on number of users. Clipper offers arrays, menu-building commands, user-defined functions, context-sensitive help techniques for applications, a debugger, and it supports Expanded Memory. It goes well beyond dBASE with 1,024 fields per data base and 2,048 active memory variables.

Clipper has the power to save and restore multiple screens to and from memory variables. You can also create overlays, call object modules compiled in other languages, and create function libraries to link with your applications. Power and flexibility make it the #1 dBASE compiler. List: **$695**, PC Brand: **Call.**

McMAX *NEW! From Nantucket*

Like dBASE for the Macintosh

McMax™ is like running dBASE on the Macintosh. It combines an easy-to-use menu-driven ASSIST mode using the Mac interface, an interactive command mode like dBASE at the dot prompt, and an application programming language fully compatible with dBase III. It gives you the power to create dBASE language applications on the Macintosh and transfer back and forth to the IBM® world. McMax accommodates up to 16 million records, 32,000 characters per record, 255 characters per field, and up to 32 files open concurrently. No copy protection. List: **$295**, PC Brand: **Call**

MICROSOFT C 4.0

A Great C Battle Rages and You're Winning

It bundles a source debugger and a "make", and sports a "huge" memory model permitting single data objects larger than 64k, but what's really impressive about Microsoft C are the benchmarks reported in Dr. Dobb's. Microsoft runs away from a field of 17 winning 11 of 27 benchmarks.

The CodeView™ debugger uses windows to show everything on one screen: source alongside disassembled object, variables, stack and registers. Drop down windows obviate learning of commands. "A source-level debugger that puts the rest to shame" said Dobb's.

Microsoft C has five memory models for code and data, plus non-library support for another thirteen, and boasts alternate math packages for speed versus accuracy, with or without 8087/80287 chips.

Both linker and library manager are part of the package, as is the "make", which knows how to rebuild any size project by compiling only elements which have changed.

It is reportedly used by Lotus, Ashton-Tate and, fittingly, Microsoft itself to develop Windows. Dobb's calls it "the best MS-DOS C development environment value today [for] virtually any kind of program conceivable." 320k suggested.

Ask for:	List:	PC Brand:
G0500	**$450**	**$295**

HALO GRAPHICS SYSTEM *Multi-Board Graphics Library*

The premier graphics library that got the ball rolling for PC-based graphics and has grown so omnipotent that it supports over 25 graphics boards — including IBM's EGA and Nr. 9 Revolution's hi-res series — and has a multitude of mouse and printer drivers. All that in each box. Separate C versions for Lattice, M'soft, Aztez, CI86. What does Multi-Halo do? A down to the last pixel graphics library plus functions to reset drivers so distributed program can run on anything. Wonderful value for single license. Costly royalties though for redistribution. Specify: S0315 & Language. List: **$300.** We: **$219.** With Dr. Halo II, a free-standing "paint": List: **$440,** Us: **$299.**

C-TREE & R-TREE *B-Tree File Manager Now Has Report Generator*

c-tree: Seasoned to perfection, c-tree™ is the only major b-tree file manager with network support in the standard low-cost version. It allows multiple users to access an index file simultaneously even during updating. Record-locking routines are provided for DOS 3.x, UNIX and XENIX.

C-tree even comes in C source code, yet there are no royalties. Source sticks to K&R, so C-tree is portable. Tests in many environments prove it.

C-tree permits any number of keys for a data file—alpha, numeric, even floating point. It handles files with varied record lengths and keeps multiple keys in one index file. Has both high level ISAM routines to handle details with minimum coding, and decomposed step-by-step functions you can access directly. In short, you get the works.

r-tree: thousands of c-tree users (and you) now have a suddenly expanded ability to produce ad hoc reports from files maintained by c-tree (v. 4.1 and up). Just link a file description to the r-tree library, and all you need is an ordinary text editor to write any number of report scripts with no further C coding. Reports can access data in several files, select on criteria, join the findings into new logical records, sort them, calculate new fields and columns, tabulate by any number of control breaks. The script files show a visual representation of the report image for easy creation and maintenance of even elaborate layouts. r-tree™ comes in source, boasts the same portability as c-tree, and fits any compiler.

	List:	PC Brand:
c-tree: F0660	**$395**	**$329**
r-tree: F0665	**$295**	**$245**
Combined:	**$650**	**$541**

dBC *Lattice Library Maintains dBASE Compatible Files With the Power and Speed of C*

dBC™ links C to dBASE. It creates and maintains files and their indexes which exactly replicate dBASE file design. So dBASE can read and update them. And the reverse. dBC can use any files created by dBASE. Now C and dBASE can operate on the same data bases interchangeably.

That opens up the widespread culture of dBASE installations to exploitation by C programmers. Tap that market, avoid the resident dBASE language, and gain the advantages of C with this single product.

dBC's functions parallel all dBASE's file handling commands, many decomposed to give closer control. Each backed by demo source files on disk.

Use dBC for custom work for clients, or on its own. It's a complete ISAM file manager for C whether or not dBASE will be used in tandem, supports all four memory models, and can have sixteen index and data files open. Big discount to buyers of both dBASE II and III versions. Specify Lattice, Microsoft 3.x, or DeSmet.

Versions:		List:	PC Brand:
L00II	For dBASE II	**$250**	**$195**
LCCII	With Source	**$500**	**$390**
L0III	For dBASE III	**$250**	**$195**
LCIII	With Source	**$500**	**$390**

POLYTRON VERSION CONTROL

Source Code Control for Any Language

PVCS allows programmers, project managers, librarians and system administrators to control the proliferation of revisions and versions of source code in software systems. Independent programmers, the leading software publishers and LAN companies, and hundreds of Fortune 1000 companies rely on PVCS to store and retrieve multiple revisions of text. It maintains a complete history of revisions as an "audit trail", generates status reports, and uses intelligent "difference detection" to minimize disk space for each new version.

On Corporate and Network PVCS simultaneous changes to a module are merged into a single new version. If changes conflict, the user is notified. The "Logfiles" used to track changes are interchangeable between any PVCS product.

Corporate PVCS is for multiple programmers. It includes "branching" to maintain code when programs evolve on multiple paths. Personal PVCS offers most of the power and flexibility of corporate PVCS, but excludes multiple programmer features. Network PVCS is the Corporate version for LANs. File locking and security levels can be tailored to each project.

PolyMake Still using a prehistoric Make? Step up to PolyMake, the most popular and powerful Make utility. Most flexible macros of any Make. Now integrated with PVCS and PolyLibrarian for faster performance and precise configuration management.

Ask for:	List	PC Brand:
Personal PVCS	**$149**	**$109**
Corporate PVCS	**$395**	**$309**
Network PVCS	**Call**	**Call**
PolyMake	**$149**	**$109**

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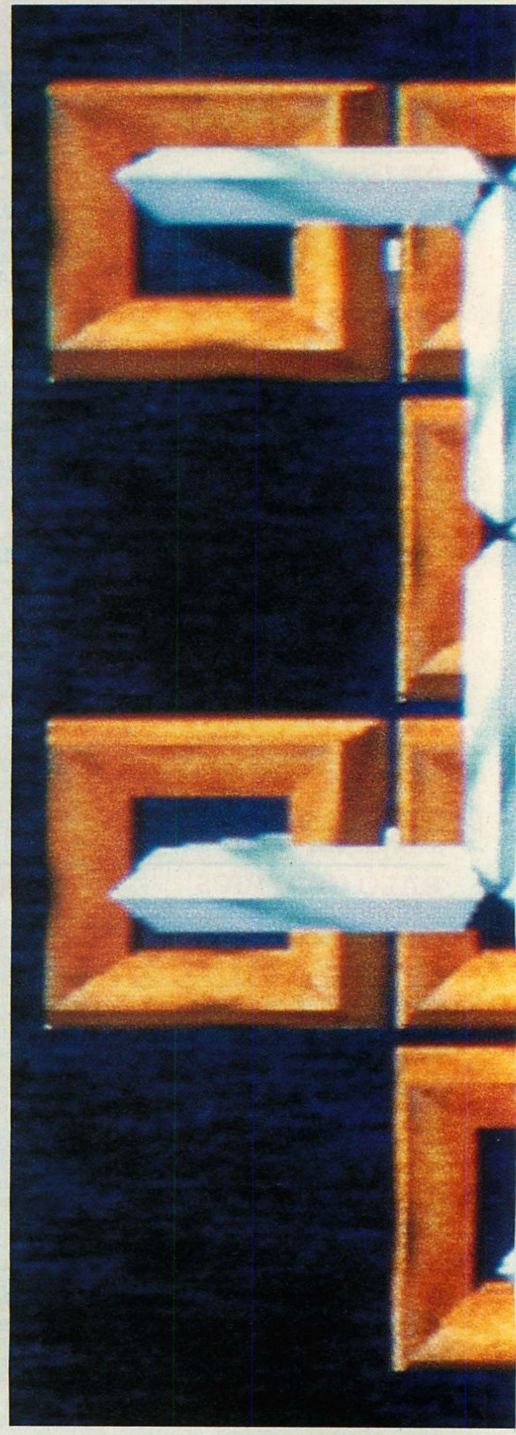
Database Design Techniques

Practical, real-world database applications can be made more efficient and effective through an understanding of pure, relational database design.

DAVE BROWNING

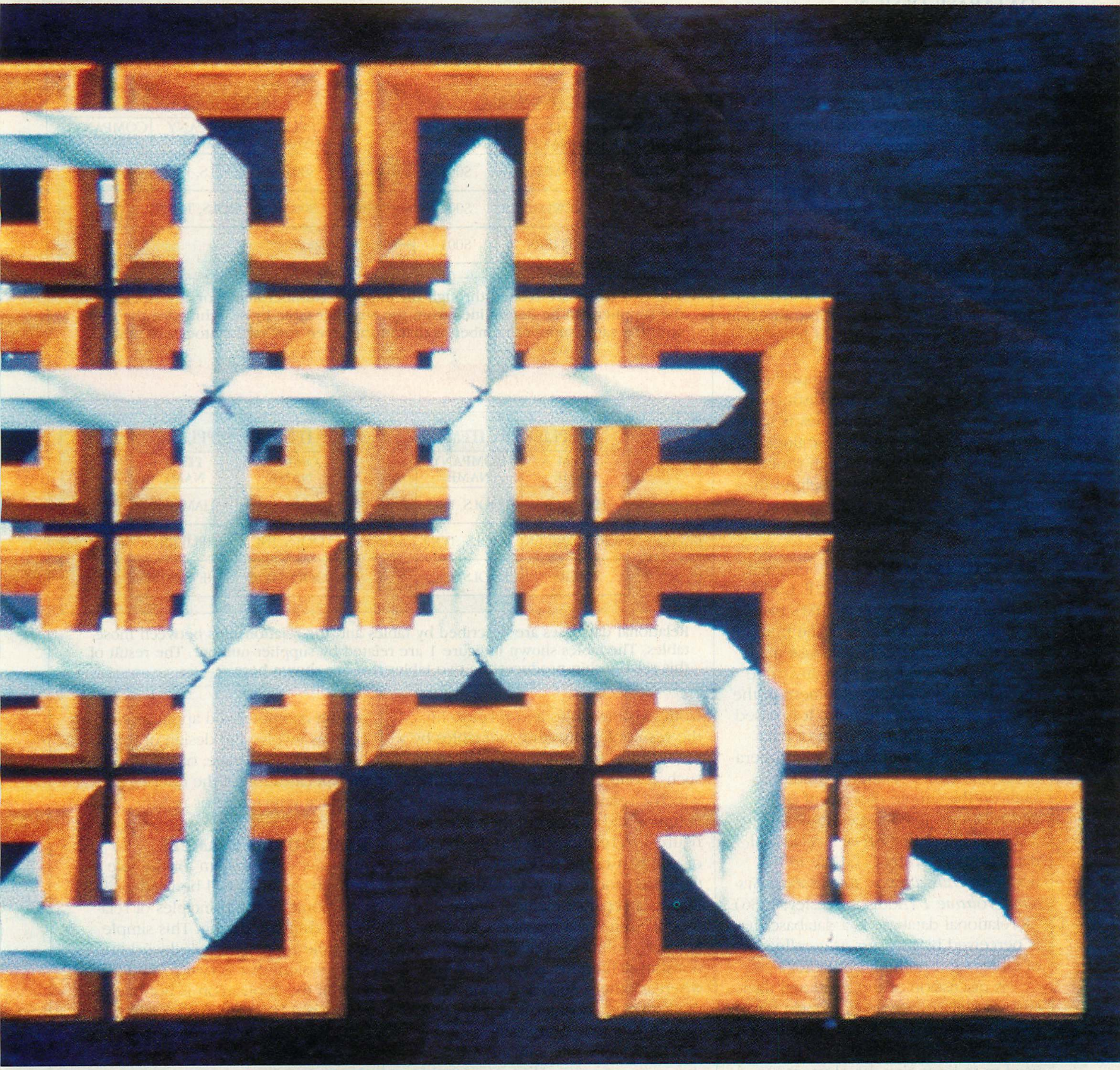


Much of the acceptance and popularity of spreadsheets and word processors is due to the similarity they have with their real-world counterparts of columnar pads and typewriters. Data managers, on the other hand, do not model real-world data management quite as closely. Real-world data storage must be represented within the database model that is chosen; and the programs and processes needed to manipulate the data in the database must be developed using whatever tools are provided by the particular data manager program that is selected.

When data managers are used in the development of real-world applications, the systems designer needs to apply principles of database structure as well as techniques of conventional systems analysis to the design process. Knowledge of the basic principles of database design will help the user to create more efficient and effective database applications. Many basic principles of database design are applicable across a wide variety of data managers.

Data managers maintain data in structures defined by the application designer. These structures are based on one of several data models. The dominant trend today is toward the relational model, which has eclipsed the older hierarchical and network data models.

In the relational model, data are organized in tables of rows and columns; the data manager manipulates and connects the tables to produce new tables representing the results of user-generated queries and data update processes. Table definitions and relationships between tables are defined in a structure that resembles the data storage and manipulation processes in the real-world application being automated.



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FUNCTIONAL ROLES

Database systems consist of two parts: the database structure and the applications that process data in the structure. System design is the process of developing the database structure and the applications that manipulate the data in the database. Several applications can process data in the same database; for example, payroll, accounts receivable, general ledger, and inventory management applications all can reference portions of the same corporate database even though each application is independent of the others.

With the relational model, the design of the database structure can be developed separately from the design of the processes that manipulate the data. The decision to use the relational model for data storage predetermines many attributes of the database structure; thus, the designer can theoretically devise a working representation of the database without any knowledge of the applications that will use the data. However, such knowledge can influence decisions in the database design process that will affect performance in the completed system, and practical, real-world processing considerations can lead to design choices that deviate from theoretically pure database structures.

Several key roles are involved in the design and implementation of a database system. The system designer provides a description of the entire system and chooses which database model and which data manager should be used. The application designer provides designs for applications that use data stored in the database structure. In most microcomputer applications the database and application designs are performed by the same person. Programmers often support the application developer in large implementations.

The database administrator maintains the security and integrity of the database, installs new database applications, makes changes to the database structure, and adds new user accounts. In addition, this person is often responsible for backing up and restoring the database when it becomes corrupted due to equipment failure, power loss, or program errors. This role may not require full-time attention in microcomputer database systems, but the function is just as important as it is in large mainframe database systems.

When one person accomplishes all of the above functions, the distinction between these functional roles is sometimes overlooked. Clear basic understanding of the system design process and the functional roles is helpful in avoiding confusion and developing effective, efficient systems.

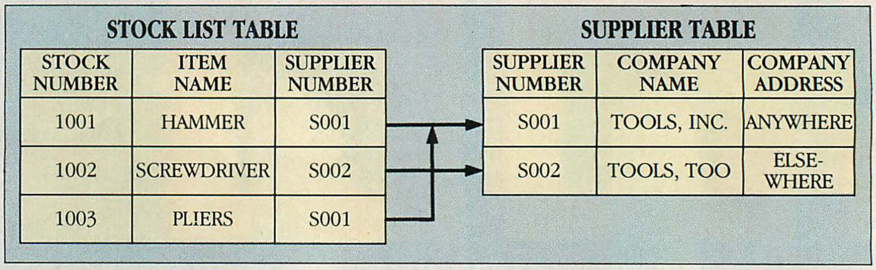
RELATIONAL MODEL

Developed in 1970 by Dr. E. F. Codd, a mathematician working at IBM's San Jose Research Laboratory at the time, the relational model of database management is considered by many to be the most important development in the history of the database field. It is based on a mathematical definition of data structures and data manipulation operations. The entire relational model is built on the simple concept of tables and relationships between tables. In fact, a useful definition of a relational database is given by C. J. Date in his book, *An Introduction to Database Systems, Volume 1* (Addison-Wesley, 1986): "A relational database is a database that is perceived by its users as a collection of tables (and nothing but tables)."

A discussion of the relational database model encompasses its own terminology. A *relation* is simply a table of rows and columns of data; the term is used to indicate that the elements in the table are related in some manner because they appear in the same table. The term *relationship*, on the other hand, generally refers to the logical connection between tables. An *n-tuple* is a row in a table, and an *attribute* is a column in a table. *Join*, *intersect*, and *union* refer to formal data manipulation commands where tables of data are combined to produce new tables. In many microcomputer data managers, tables are called *files*, rows are *records*, and columns are *fields*.

Figure 1 shows two sample tables (relations) and a logical relationship between them. New tables are constructed from existing tables and relationships; the result of connecting two tables by a relationship is really just a third table, such as one of those shown in figure 2, which display useful combinations of columns and rows from the tables in figure 1. A relationship can be thought of as a part of the process of combining tables to produce new tables rather than as a separate element of the model. Some data managers, such as Software Solutions' DataEase, store relationship definitions as specific items, whereas others, such as Ashton-Tate's dBASE III PLUS, consider a relationship to be part of a temporary state, as in the SET RELATION... command. In many data managers, a combination of tables and relationships between them defines a logical picture of the data, formally called a *view*, and facilities are provided to save and recall view definitions.

FIGURE 1: *Relationship between Tables*



STOCK LIST TABLE

STOCK NUMBER	ITEM NAME	SUPPLIER NUMBER
1001	HAMMER	S001
1002	SCREWDRIVER	S002
1003	PLIERS	S001

SUPPLIER TABLE

SUPPLIER NUMBER	COMPANY NAME	COMPANY ADDRESS
S001	TOOLS, INC.	ANYWHERE
S002	TOOLS, TOO	ELSE-WHERE

The two tables are related through the Supplier Number field. For any stock item, the supplier can be determined from the Supplier table by searching for the row with the same supplier number as that in the given row of the Stock List table.

FIGURE 2: *Result of Relationship between Tables*

SUPPLIERS BY ITEM

ITEM NAME	COMPANY NAME
HAMMER	TOOLS, INC.
SCREWDRIVER	TOOLS, TOO
PLIERS	TOOLS, INC.

ITEMS BY SUPPLIER

COMPANY NAME	ITEM NAME
TOOLS, INC.	HAMMER
TOOLS, INC.	PLIERS
TOOLS, TOO	SCREWDRIVER

Relational databases are described by tables and the relationships between those tables. The tables shown in figure 1 are related by supplier number. The result of this relationship produces the two tables that are shown here.

The relational model of database management is quite suitable for a great many real-world applications, but some knowledge of the model and how it operates is necessary for effective application design. Real-world data are rarely organized according to the relational model, and careful consideration needs to be given to alternatives in balancing theoretical aspects of the relational model with real-world processing requirements and performance of the resulting computerized application. Many choices involve the design of the tables used for data storage; others involve the specification of the queries that produce new tables or reports.

REAL-WORLD EXAMPLE

An order-entry system for the sale of items from stock will be used to illustrate some of the principles of relational database design. This simple example represents a real-world order-entry system that is easy to understand, even if the application is not one encountered by everyone.

The basic order-entry process consists of taking orders for items to be shipped to the purchaser. The list of items available for purchase is the *stock list* and is presented to purchasers in the form of a catalog. Customers having established accounts are kept in a file.

One of the principles of relational database management is that data elements should not be duplicated except as required for establishing relationships between tables. In the sample tables that are shown in figure 1, only the Supplier Number field appears in both tables. If only one table were used for all data, the supplier' name, address, telephone number, point of contact, etc. would have to be repeated in each row where one of that supplier's tools was

FIGURE 3: *Pure Order-entry Database Design*

CUSTOMER TABLE

ACCT #	NAME	STREET ADDRESS	CITY	ST	ZIP
C1001	BILL SMITH	101 FIRST ST.	NEW YORK	NY	12345
C1002	FRED BROWN	123 MAPLE AVE.	SAN DIEGO	CA	23456
C1003	GREG WHITE	456 OAK PLACE	OAKTON	CA	34567
C1004	BILL SMITH	202 SECOND ST.	CHICAGO	IL	45678

STOCK LIST TABLE

STK #	ITEM NAME	PRICE
S1001	HAMMER	7.95
S1002	SCREWDRIVER	1.59
S1003	PLIERS	2.95
S1004	WRENCH	4.49

ORDER HEADER TABLE

ORD #	ACCT #	ORD DATE
O1001	C1002	03/25/87
O1002	C1004	03/26/87
O1003	C1004	03/26/87

ORDER DETAIL TABLE

ORD #	LINE #	STK #	QTY
O1001	01	S1002	10
O1001	02	S1003	20
O1001	03	S1004	10
O1002	01	S1001	5
O1002	02	S1003	5
O1003	01	S1001	15
O1003	02	S1002	20
O1003	03	S1003	10
O1003	04	S1004	10

Each table is characterized by having a key field and one or more additional fields, each with only one value. The Customer and Stock List tables are intuitive; the Header and Detail tables allow an unlimited number of items for each order.

listed, thus wasting a significant amount of storage space.

Besides the storage consideration, the single-table scheme would require substantial processing to change a supplier's address or phone number. The change would have to be applied to each occurrence of the supplier's address or phone number. The dual-table approach allows each supplier's address to be stored only once; however, it does necessitate the presence of a key field to relate the two tables, in this case the Supplier Number field.

Many microcomputer data managers require or accept the designation of a field in each file as a key field. The field contents are used as names or labels for the records or rows in the table. Many data managers permit more than one field or combination of fields in a single table to be designated as keys. The proper selection of key fields is important in microcomputer database systems; too few or inappropriately chosen keys can have a significant performance impact in data retrieval operations, whereas too many key fields would adversely affect performance in data entry and update processes.

In many data managers, data in key fields must have unique values for each record. For example, the Acct #, Stk #, and Order # fields provide unique keys for the Customer, Stock, and Order Header tables in the data tables of figure 3; in each of these tables no two records can have the same account number, stock number, or order number. In the Order Detail table the Order # field is not unique, but the combination of Order # and Line # is unique for any row in the table.

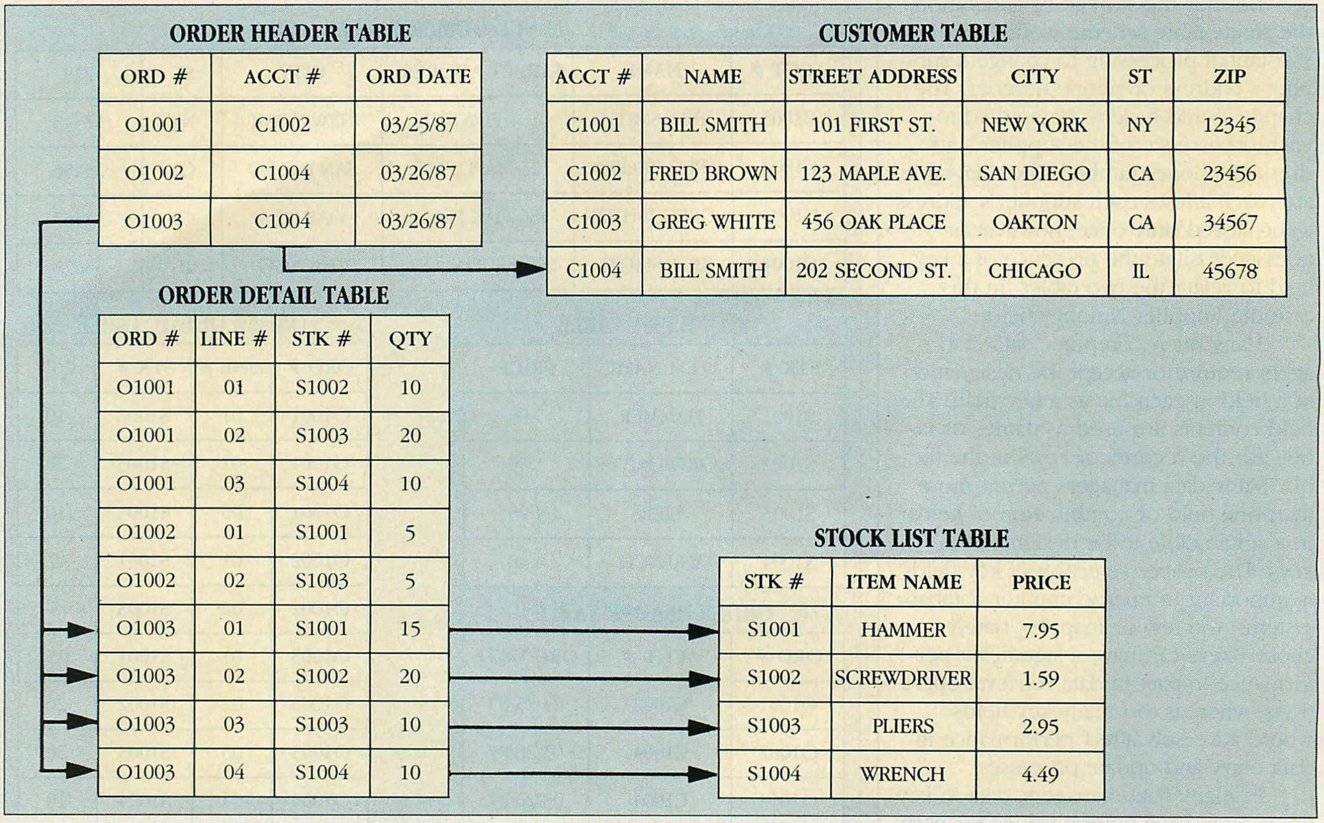
Often, the design of a database to model real-world applications requires introducing artificial numbers as keys to make the resulting application more efficient. While the user may want to replace the Supplier Number field with the Company Name field as the key, this approach has three problems. First, the Company Name field would have to be larger than the Supplier Number field and would take up additional space in the Stock List table. Second, as users type in company names they may make inconsistent choices in capitalization or abbreviation; a data manager is not likely to recognize ACME BOOTS, INC. to be the same company as Acme Boots, Incorporated. Third and most important, two suppliers may have the same company name but different addresses (divisions of the same company or separate companies incorporated in different states), so there would be no way to identify which company supplied a particular item. In relational database design, each table should have a field where the value is unique for each record or where some combination of fields uniquely identifies each record.

Theoretically, numbers used for keys should be pure—that is, they should not contain any specific information through coding techniques. When key numbers contain data such as stock groupings, changes to these groupings have a significant impact on the database, and substantial processing is required to reflect changes throughout the database. No matter what the coding technique, unanticipated changes are unavoidable. The U.S. telephone number assignment scheme is an example of this. The area code identifies a geographical section of the country, and the remaining digits identify the local exchange and individual subscriber's number. An area code that "runs out" of telephone numbers has to be split into two area codes, thus affecting large numbers of subscribers. This does not mean that information-containing numbering systems are necessarily bad; in fact, in many real-world applications the benefits may outweigh the problems.

In relational database terminology, *normalization* is the process of assigning data fields to tables such that data are not duplicated. Not only should duplication of fields in various tables except for assigned keys be avoided, but also the tables should be structured as illustrated in figure 1 so that rows are not required to contain repeated data.

Normalization is based on the concepts of normal forms and functional dependence. Essentially, each of the several defined normal forms simply specifies a set of constraints to be placed on a relation—for example, the constraint that each row and column position in a table have just one value. Functional dependence further specifies that for a given field in a record, there is only one corresponding value for each additional field in that record. For example, for a given customer in the Customer table there is only one street, one state, etc. Thus, normalization and functional dependence address the usually intuitive process of defining tables and assigning fields to tables.

FIGURE 4: *Relational Linkages*



ORDER HEADER TABLE

ORD #	ACCT #	ORD DATE
O1001	C1002	03/25/87
O1002	C1004	03/26/87
O1003	C1004	03/26/87

CUSTOMER TABLE

ACCT #	NAME	STREET ADDRESS	CITY	ST	ZIP
C1001	BILL SMITH	101 FIRST ST.	NEW YORK	NY	12345
C1002	FRED BROWN	123 MAPLE AVE.	SAN DIEGO	CA	23456
C1003	GREG WHITE	456 OAK PLACE	OAKTON	CA	34567
C1004	BILL SMITH	202 SECOND ST.	CHICAGO	IL	45678

ORDER DETAIL TABLE

ORD #	LINE #	STK #	QTY
O1001	01	S1002	10
O1001	02	S1003	20
O1001	03	S1004	10
O1002	01	S1001	5
O1002	02	S1003	5
O1003	01	S1001	15
O1003	02	S1002	20
O1003	03	S1003	10
O1003	04	S1004	10

STOCK LIST TABLE

STK #	ITEM NAME	PRICE
S1001	HAMMER	7.95
S1002	SCREWDRIVER	1.59
S1003	PLIERS	2.95
S1004	WRENCH	4.49

The figure 3 tables are used to extract data for order O1003. The order header record points to the Customer and Order Detail records with the same number. The stock number in the Order Detail table is used to identify all items in the Stock List table.

In practice, fields tend to fall into intuitive, logical groupings that can be used for table definitions, and precise formulas are not needed for the assignment process. The Customer table would naturally have fields containing data about each customer, such as account number, name, and address. Fields that need to contain more than one value for an individual customer, such as several shipping addresses for customers that place orders for shipment to multiple locations, should be assigned to separate tables.

Some database designs should not be normalized. However, an initial design of normalized tables is an excellent starting point for any application. Data duplication can then be applied to the design to accommodate real-world considerations. For example, in the sample order-entry database, the Customer table and the Stock List table have to be related via two other tables. A daily report that lists customer name and item ordered might save retrieval time if the item name were included in the Customer table. Thus, once a database structure of tables has been designed, it can be modified to accommodate real-world considerations.

PURE ORDER ENTRY

A simple order-entry system contains information about customers, stock, and orders. The design needs to allow for the possibility that a customer might purchase several items on one order. A database model of four tables can be used for this sample application. Figure 3 shows the structure of these four normalized tables. The Customer and Stock List tables are set up as would be expected, but orders are split between the Order Header and Order Detail tables; this allows for an unlimited number of items to be applied on each order. The terms *header* and *detail* are commonly used in data processing where an entity, such as an order, is split into two tables to allow for an unlimited number of items for one entity.

Key fields have been established with no information coded into the key-field numbering system other than a leading letter (*C*, *S*, or *O*) to identify whether the number refers to a customer, stock item, or order. This leading letter is a minor code that helps reduce possible conflicts between similar numbers used in different tables. Data management programs know that customer number 1001 is different from stock number 1001, but a leading letter helps the designer and user keep track with much less confusion.

An order can be displayed by extracting data elements from each of the four tables in figure 3. For example, to display order number O1003, the Order Header table row with the Order # field element equal to O1003 provides the date (03/26/87) and pointers into the Customer and Order Detail tables. Because the value of the Customer # field in the Order Header table matches Bill Smith's customer number in the Customer table, Bill Smith's name and address are extracted from the Customer table. The order number (O1003) from the Order Header table matches four occurrences of the Order # field in the Order Detail table, thus pointing to the four items purchased on this order. The Line # field in the Order Detail table serves to keep the order detail lines in sequence, and the combination of the Order # and Line # fields in the Order Detail table provides a unique key for access to the records for modification or query. The Stk # field in the Order Detail table uniquely identifies records in the Stock List table so that each line item of the printed or-

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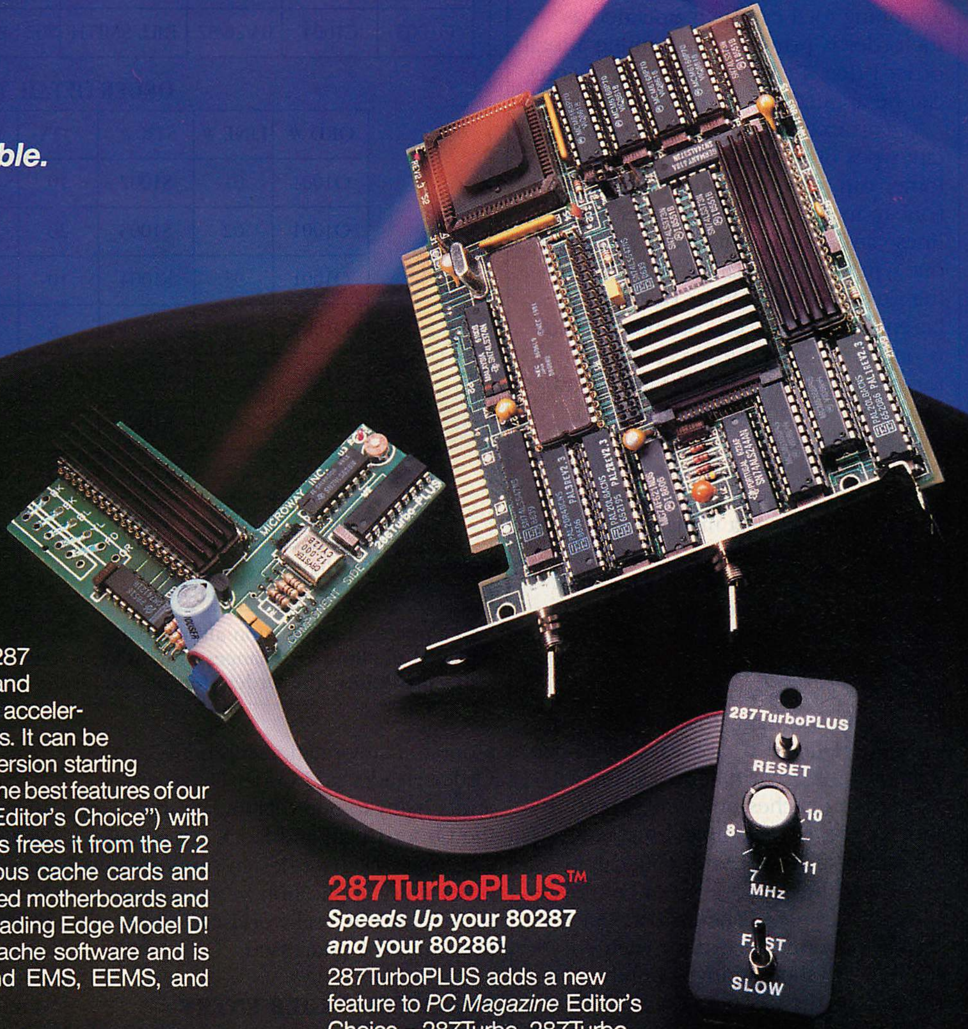

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der can list the stock item name (Item Name field from the Stock List table) and the unit price.

Figure 4 illustrates the relationship linkages between the tables for order number O1003. The Qty field from the Order Detail table and the Price field from the Stock List table can be multiplied to provide an extended price, and a running total can be maintained as the order is printed to determine a total order price. Taxes and shipping charges can be applied through program logic.

This example illustrates two important types of relationships: one customer can place more than one order (one-to-many), and many order detail lines can occur in one order (many-to-one). In fact, the relationship between the Customer and Order Header tables based on equality of Customer # fields is one-to-many in the direction from Customer to Order Header table, and many-to-one from Order Header to Customer table. This distinction is important in the design of queries and reports based on the available choice of operators in the data manager. Another many-to-one relationship occurs between the Order Detail and Stock List tables, where many records in the Order Detail table relate to a single record in the Stock List table.

Two other types of relationships, one-to-one and many-to-many, are possible in relational databases. One-to-one relationships occur when each record in one file matches only one record in another file. For example, employee information such as payroll data can be stored in a file separate from employee address and miscellaneous data. Each file has only one record for each employee, with the employee number being used as the key field for both. The relationship between these two files is one-to-one in both directions.

Many-to-many relationships are a little more difficult to handle. In the order-entry example, many orders could refer to many stock items, and a relationship between the Order Header table and the Stock List table would be many-to-many. Clearly, many stock items can be listed on one order, and many orders can list any one stock item for purchase. This relationship cannot be established directly between the two tables because any linkage field would have to contain multiple values in one or both of the tables.

The many-to-many relationship is created indirectly, using an intermediate connection—the Order Detail table in this case. The Order Detail table reduces the many-to-many relationship to a one-to-many relationship between the Order Header and Order Detail tables and a many-to-one relationship between the Order Detail and Stock List tables. This pure database design supports the order-entry application in theory, but some practical, real-world considerations must be addressed.

PRACTICAL ORDER ENTRY

Regardless of limitations of specific data manager relationship operators, the above database design provides a relatively pure solution to the order-entry application. However, this design is not suited to real-world conditions; customer information, stock prices, and stock numbers can change. Orders extracted from the pure database reflect the latest value of the data elements, which may not be the desired value.

In the pure database design, the data manager looks up stock prices for each line item of each order as it is printed. Thus, any changes to stock item prices or stock numbers are immediately reflected in all outstanding orders. In most real-world businesses, item prices are fixed at the time of order placement and are not subject to change between the time the order is placed and the time it is filled. To accommodate the real-world probability that prices will change, and that some order will have been placed at one price and will not yet have been filled before the price change, the Price field is duplicated in the Order Detail table, as shown in figure 5. The price in effect at the time of order placement (the time the order and order detail records are created) is copied into the order detail record. Subsequent changes to the price value in the Stock List table need not affect orders already placed.

Similarly, if the business frequently changes stock numbers and reuses previously active stock numbers to refer to new items, then the information in the Stock List table should be copied into corresponding fields set up in the Order Detail table records to preserve the information that is current at the time the order is placed.

In some cases, it is desirable to capture the entire order at the time it is placed. An order can be printed at any time and always produces the same output regardless of changes in any of the other files. Figure 5 shows the structures for the Order Header and Order Detail tables for this design. The choice

FIGURE 5: *Practical Order-entry Database Design*

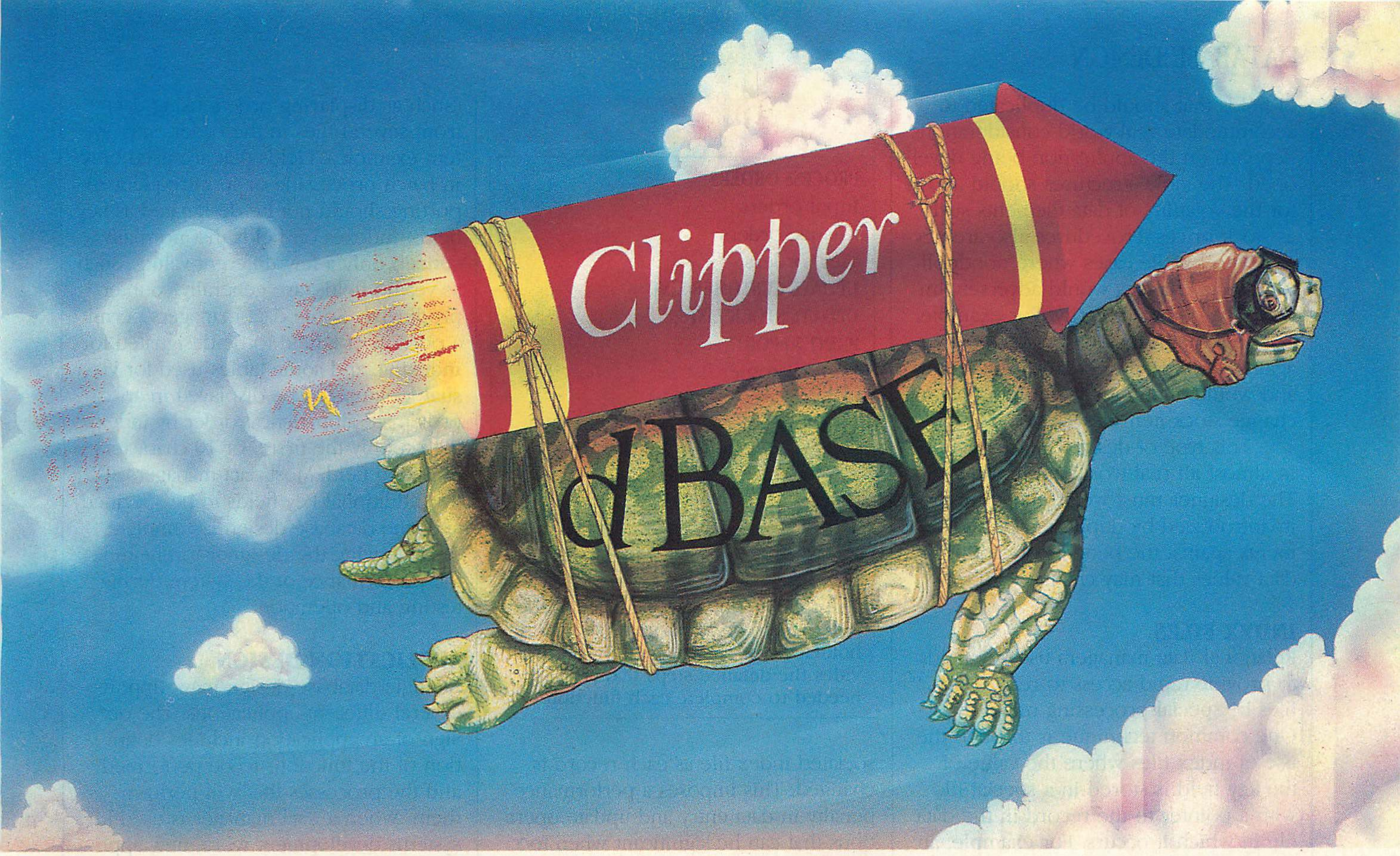
ORDER HEADER TABLE

ORD #	ACCT #	ORD DATE	NAME	STREET ADDRESS	CITY	ST	ZIP
O1001	C1002	03/25/87	FRED BROWN	123 MAPLE AVE.	SAN DIEGO	CA	23456
O1002	C1004	03/26/87	BILL SMITH	202 SECOND ST.	CHICAGO	IL	45678
O1003	C1004	03/26/87	BILL SMITH	202 SECOND ST.	CHICAGO	IL	45678

ORDER DETAIL TABLE

ORD #	LINE #	STK #	QTY	ITEM NAME	PRICE
O1001	01	S1002	10	SCREWDRIVER	1.59
O1001	02	S1003	20	PLIERS	2.95
O1001	03	S1004	10	WRENCH	4.49
O1002	01	S1001	5	HAMMER	7.95
O1002	02	S1003	5	PLIERS	2.95
O1003	01	S1001	15	HAMMER	7.95
O1003	02	S1002	20	SCREWDRIVER	1.59
O1003	03	S1003	10	PLIERS	2.95
O1003	04	S1004	10	WRENCH	4.49

In a practical application all order data must be captured at the time the order is placed to allow for changes in item price, customer address, etc. To accommodate this possibility, the Order Header and Order Detail tables are expanded.



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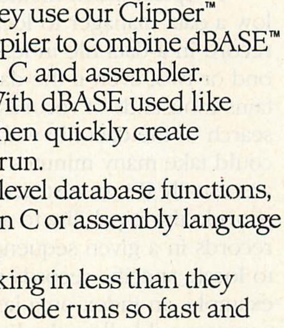

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of fields that should be duplicated to accommodate real-world considerations depends on the application being developed. The table structures should allow for the volatility of data elements such as stock prices. Procedures also are necessary to handle cases where nonduplicated data changes would adversely impact data output integrity. For example, a system might include protection against modification of stock numbers and would allow only certain people to change stock item descriptions.

This type of design choice occurs in almost all real-world applications. The designer must weigh the complexity introduced by duplicated data elements against the benefits of capturing data values that may change with time.

INDEX FILES

Relational data managers use key fields to provide rapid access to records in files by special processing methods. One common technique is through the use of index files where the value of the key field is stored in a special file with a pointer to the record in the data file in which it occurs. For example, an index file of account numbers for a customer data table allows the data manager to locate the customer record for a given account number using only a few operations on the index file, as opposed to searching the customer file from top to bottom for the record.

A typical index method would allow a data manager to locate a specific record in a data file in less than a second or two, even if the data file contains thousands of records; a sequential search of the data file without the index could take many minutes. Index files are usually B+ tree structures, which provide the capability to access data records in a given sequence as well as to locate specific records rapidly; for example, an index on a key field of last names would allow the listing of the file in alphabetical order as well as the rapid location of a record containing a specific name. B+ tree indexing is the technique most often used in popular microcomputer data managers.

Each designated key or index field requires storage for the index cross-reference information. B+ tree indexes are usually kept separately from data files; often, an individual file is used for each index. The size of an index file may exceed that of the data file when lengthy fields are specified as keys and the number of records is large. When records are modified with new data that affect the contents of a key field, the data manager must also update the associated index file as each record is changed. This imposes a performance penalty in data entry and update operations that can be significant when too many fields are designated as keys.

TABLE 1: *Top-down Design*

PROCESS ORDERS
Input orders
Change orders
View orders
UPDATE CUSTOMER LIST
UPDATE STOCK LIST
PRINT REPORTS
Print customer list
Print orders
Print stock list
Print orders by customer
Print orders by stock item
UTILITIES
Backup data files
Restore data files from backup

The top level of design is a list of the functions to be performed (shown in boldface type). The second level provides the detailed steps that are needed to complete each function.

Key fields also provide rapid access to tables combined in relationships. For example, the relationships illustrated in figure 4 would be implemented using indexes on the key fields in the various tables. The index on the Order # field in the Order Header table could be used to print orders in sequence, while the indexes on the other tables permit the related data to be extracted quickly from them as each record in the Order Header file is processed. Without indexes the performance for producing queries from multiple related tables might well be unacceptable.

When index files have not been defined as part of the database design, the data manager can create temporary index files in response to query and report requirements. Sorting and sort pointer techniques, such as inverted list files, also can be used during query and reporting data retrieval operations. The performance cost of the time for a data manager to create ad hoc indexes and to sort files is often acceptable for reports that are executed infrequently or are left to run unattended; this cost can be offset by the reduction in processing time that is needed to maintain indexes on fewer key fields during data entry and update operations.

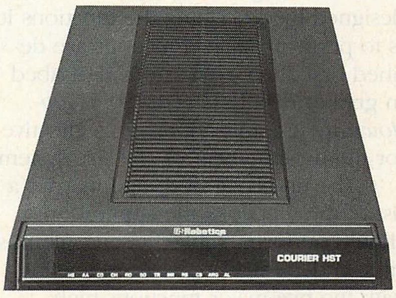
Key fields should be selected with a view toward providing good performance for on-line operations (such as data entry) and common ad hoc queries (such as displaying orders using data from several files in the order-entry system example). Fields that are used only in batch processing or in infrequent reporting should not be designated as key fields; indexes on fields that normally contain only a few different values, such as yes/no fields, are generally counterproductive. Some data managers permit a portion of a field to be designated for indexing, and some tables used for visual look-up can be displayed in approximate alphabetical order by indexing on only the first 8 or 10 characters of a long field. Most data managers allow additional key fields to be specified after the database design is complete, thus allowing the designer to fine-tune the performance of the system during testing and operation.

APPLICATION DESIGN

A single database design may support several different applications. The design of an application includes definition of the functions to be performed and the processes that will perform them. When a data manager is used for systems development work, new applications can be developed that use existing database structures, and additions to existing database structures often can be made without affecting the completed applications.

As an example, the order-entry application can be extended for added functionality. Users can create fields for the Customer table to hold additional data for point of contact, telephone numbers, billing address, credit status, and shipping location code. For customers with multiple shipping addresses, another table can be created using the same customer number key, location code, and shipping address. A table or fields in the Customer table can keep running totals of outstanding orders and year-to-date or month-to-date orders, allowing current credit balance or authorized discount rates to be listed. Users can collect statistical data for analysis of sales by customer. A Supplier table can be created and referenced from the Stock List table. Users can add fields for quantity on hand, reorder point quantities, economic order quantities, and purchase lead times to manage inventory functions.

In developing an application the designer must consider the following elements: functional design, transaction processing, data entry, data update, queries, reporting, security, utilities, and backup. Even small applications require that each of these points be addressed in some fashion.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Functional design. An application can be designed by describing the functions it is to perform. Major functions are defined first, then each one is described in greater detail. Referred to as *top-down design*, this approach is effective for the development of any size system.

The first level of design may be a list of the functions the application should perform. Table 1 lists some possible order-entry application functions, with the five major functions highlighted. Some of the major functions are further refined into a second level of functional detail, including order processing, a number of predefined reports, and two common utilities.

The data entry function (Input Orders) is separated from the function of changing existing orders (Change Orders) to permit more control over the integrity of the existing order data; in many order-entry applications, data entry personnel are not permitted to change existing orders; that function is reserved for supervisors. The View Orders function is also separate because it may be used by people not involved in the actual order-entry process. The separate View Orders function can simplify the user interface (by requiring the user to enter only the desired order number) and prevent inappropriate personnel from making changes to data.

The Update Customer List and the Update Stock List functions are not further refined because the purpose of this particular application is to process orders. The customer and stock lists are not subject to the volume of new data added to the Order Header and Order Detail files, so in this case the data entry and change functions are combined into a single update function, providing a feature to view the records in the Customer or Stock List tables.

For a simple order-entry system, this breakdown does not need to be further refined, but additional functional levels might be required for a complex order management system with multiuser and remote access features. This type of functional breakdown often leads to a logical menu structure for the application's user interface; the functional breakdown shown in table 1 would be easily implemented in a two-tier menu structure.

Transaction processing. In database management systems, a logical unit of work is referred to as a *transaction*. The process of entering a complete order into the sample order-entry system would be a transaction. A modification to a single record in the Customer table to update a telephone number also would be a transaction. Large data managers for minicomputers and mainframes include functions to manage transaction processing, but few current microcomputer data managers have this feature. Transaction processing is important to the maintenance of data integrity in databases, and knowledge of the concept is valuable even when using data managers that lack transaction capabilities.

Each transaction must be applied completely to maintain consistency of data in the database. For example, an order consists of an order header record and one or more order detail lines. If the detail lines of an order were entered into the system but the order header record were not, the system could not retrieve the order information from the data files. In a data manager that supports transaction processing, the developer could specify that a single order-entry transaction include the addition of a record to the Order Header file and the addition of all order detail line records to the Order Detail file. If the order-entry transaction does not complete properly—for example, if a customer wants to cancel an order because all parts of it cannot be filled—then the data manager "backs out" the completed parts of the transaction, thus preventing corruption of the database consistency. In a data manager that lacks transaction processing features, an equivalent function often can be programmed in it.

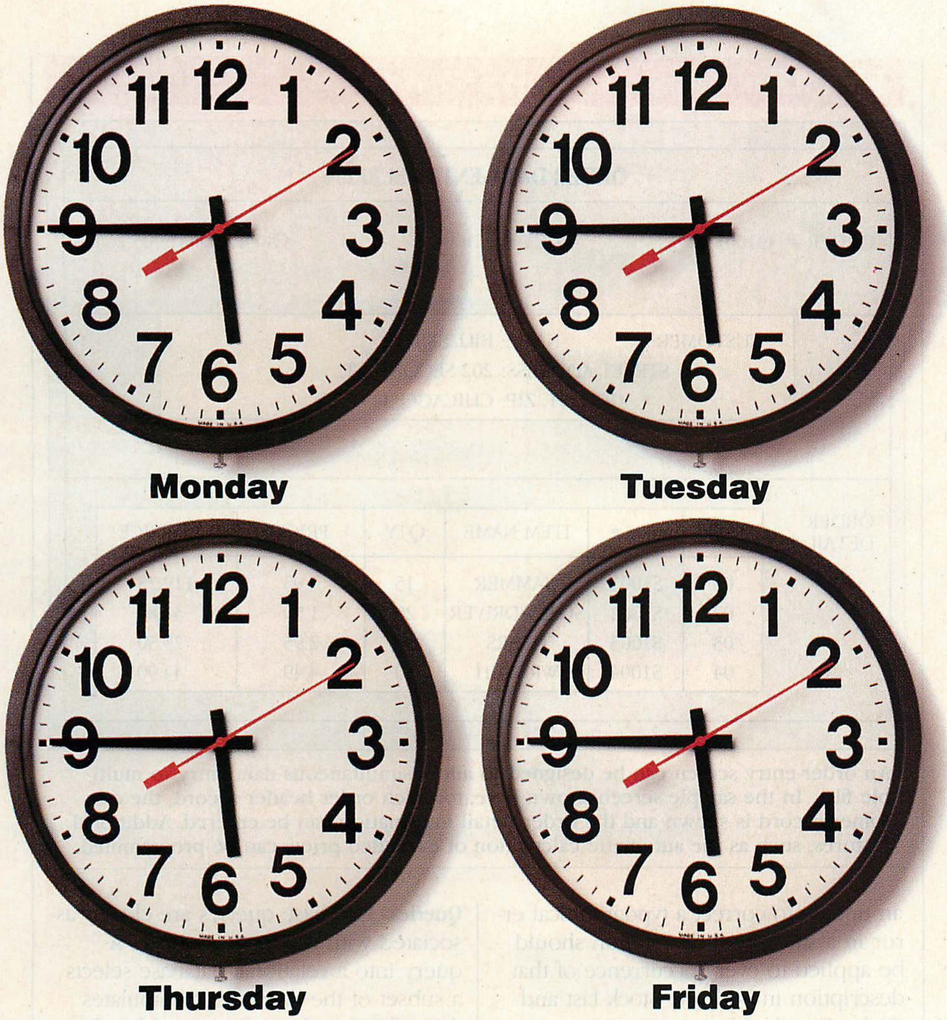
Transaction processing is important to the maintenance of data integrity in databases, and knowledge of this concept is valuable.

Data entry. The purpose of data entry is to get valid data into the database. Sometimes a data-entry process includes limited update capabilities as well, and sometimes the data-entry and update functions are combined into one operation. Validation of data is performed during the data-entry operation, and invalid data should be rejected at that time. Data validation should be combined with the principles of transaction processing so that transactions containing invalid data are completely rejected and not partially applied. Data entry also should follow the principles of transaction processing to prevent corruption of database consistency due to partially entered transactions.

Data validation techniques include type checking, range checking, and table look-up. Type checking verifies that the data being entered are the expected type (numeric, text, date); range checking limits data to specified ranges (such as dates within the current fiscal year); and table look-up validates input data against tables in the database. Table look-up is especially valuable because the data being entered are expected to be consistent with other data elements in the database. For example, when an order is entered in the example system, order numbers can be validated to prevent duplicate orders with the same number, account numbers can be looked up in the customer table, and stock numbers can be checked against the Stock List table.

In addition to data validation, transaction processing is very important to the data-entry process. A data-entry transaction in the example order-entry system consists of the complete order information, including one record to be added to the Order Header file and one or more records to the Order Detail file. Data can be entered directly into the database in an on-line mode, or they can be stored in a temporary file and posted to the database later. In either case data validation and transaction processing techniques should be used to prevent invalid data or partial transactions from affecting the integrity and consistency of the database.

To ensure concurrent update of multiple files, some microcomputer data managers support simultaneous entry of data into multiple files; for example, in Microrim's R:base System V program, the developer defines a *region* on the screen where data for the Order Detail file are to be entered. The data manager allows scrolling of the Order Detail file within the region as new records are added, while the remainder of the screen accepts data for the Order Header file. In many microcomputer data managers, the ability to manage multiple files on a single data-entry screen is not available, and in others this process can be implemented only with substantial programming. A sample screen for the entry of order header and detail data is provided in figure 6. The order-entry program has to manage the scrolling of the detail line input area when more lines are entered than there is room to put them. The program also can calculate the extended price, and could be programmed to



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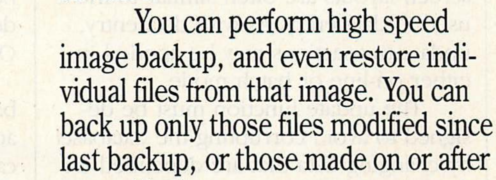

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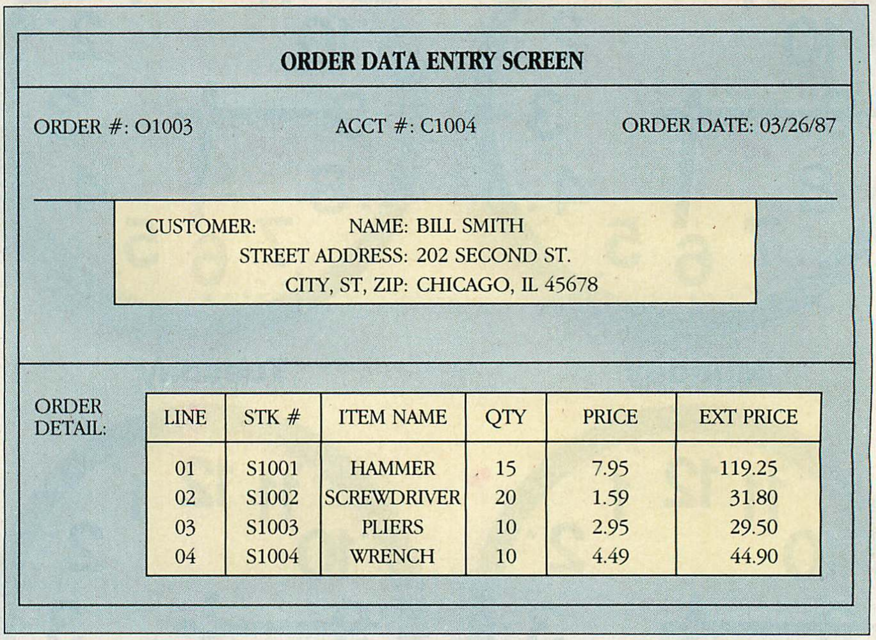
FIGURE 6: *Sample Order-entry Screen*



ORDER DATA ENTRY SCREEN

ORDER #: O1003 ACCT #: C1004 ORDER DATE: 03/26/87

CUSTOMER: NAME: BILL SMITH
STREET ADDRESS: 202 SECOND ST.
CITY, ST, ZIP: CHICAGO, IL 45678

ORDER DETAIL:

LINE	STK #	ITEM NAME	QTY	PRICE	EXT PRICE
01	S1001	HAMMER	15	7.95	119.25
02	S1002	SCREWDRIVER	20	1.59	31.80
03	S1003	PLIERS	10	2.95	29.50
04	S1004	WRENCH	10	4.49	44.90

An order-entry screen can be designed to allow simultaneous data entry to multiple files. In the sample screen shown here, for each order header record, the customer record is shown and the order detail information can be entered. Additional features, such as the automatic calculation of extended price, can be programmed.

show the total order value in the upper order header area.

The difficulty often encountered in developing multifile data-entry screens concerns the management of the key fields that are used to establish the relationship linking the related files. In the order-entry example, the process of entering an order consists of first entering the order header information, then the detail lines. The data-entry program either accepts the order number from the user and validates it against the order header file to prevent duplication or generates the order number and does not allow the user to modify it. (The method selected is a system design consideration.) This order number must then be entered into each record added to the Order Detail file for the specific record being entered. If the data-entry person were required to reenter the order number for each order detail line, then the data-entry program would have to manage this process to avoid typographical errors.

Data update. The purpose of the update function is to change existing data in the database. Data entered to replace or modify existing database information must be validated just as if it were entered as new data, and data update screen layouts are often similar to those used in data entry. As with data entry, update transactions may be applied in either on-line or batch mode.

The update function must be designed to avoid corrupting the database by changing data that are depended on by other data elements. For example, in the pure order-entry system shown in figure 3, any changes to the Stock List table would immediately be reflected in any orders printed after the change; this is because the Order Detail table records point to the stock data values in the Stock List table and always look up the most current value. To preserve the stock prices in effect at the time that an order was placed, the prices in the Stock List table cannot be changed until all orders that reference the effected item are completed and then purged from the order-entry system.

Modifying data elements duplicated in more than one table requires care. Sometimes only one occurrence of the data should be changed, but at other times all copies of the data element should reflect the change. In the modified database design in figure 5, data were extracted from the Stock List table and duplicated in the Order Detail table so that certain elements, such as stock price, could be updated without affecting existing orders. On the other hand, an update to correct a typographical error in a stock item description should be applied to every occurrence of that description in both the Stock List and Order Detail tables.

Deletion of records from the database is a unique type of update transaction that requires special attention; care must be taken to avoid deleting records that other records depend on for reference. In the order-entry system, deletion of an order header record could leave one or more records stranded in the Order Detail table.

A transaction that deletes all related records automatically along with the specified record is called a *cascading delete* and must be used with caution; the inadvertent deletion of a single record in a department file could eliminate the records of several hundred employees. The alternative choice is to prevent a record from being removed while subordinate records exist; deletions must be made from the bottom up. Each technique is appropriate in certain cases; in the example order-entry system, the user might want to delete the order detail records automatically when an order header record is removed, thus deleting the entire order. In the case of a personnel database, however, the department records should probably not be deleted unless all subordinate employee records have first been individually removed.

Queries. Database queries are closely associated with report production. A query into a relational database selects a subset of the database, manipulates this subset, and produces a table of rows and columns that represents the result of the manipulations that were defined by the query; the presentation of this table of results in a desired format is the reporting function. Some data manager designs address queries and reports as two parts of a general data-retrieval process, whereas others treat them as separate procedures.

Queries and reports are closely associated for two reasons. First, reports are often used to produce repeatable output such as a weekly report of outstanding orders by customer; the query that retrieves the desired data from the database is always run with the report. Second, many data managers use temporary index and sort pointer files to select the desired data defined by the query from the database and present the resulting information as a virtual table rather than creating a real table to contain the retrieved data. In this case, the data manager combines the query and report processes so that each row of the virtual table is submitted to the report program for processing as it is determined by the query procedure. This technique is used in many data managers to improve performance and minimize storage requirements.

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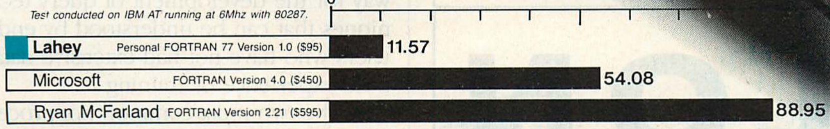

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Data can be retrieved from relational databases using either procedural or nonprocedural methods. All relational data managers use one or both of these techniques. In procedural data retrieval the query developer specifies the process and sequence of instructions that will be used to select and manipulate the database to produce the desired result. The procedural query function can be a programming language specific to the data manager program, as in the case of dBASE III PLUS (see review, "A Data Manager with an Evolving Standard," Dave Browning, May 1986, p. 166), or it may be an interface to a general-purpose programming language such as BASIC, C, or Pascal. The use of procedural query techniques requires the query developer to know the many intricacies of the database design, including the availability of index files, designation of key fields, and allocation of fields to files. The query developer uses the given programming language to define the sequence of steps that the data manager must perform in order to produce the desired output.

Nonprocedural query techniques specify the desired output to the data manager without stipulating the procedure the data manager must use to retrieve the data. The use of nonprocedural query methods requires the query developer to know less about the specifics of database design and opens the way for the development of query techniques that can be understood by end users who have not had extensive database experience or training.

The two most common nonprocedural query methods are Structured Query Language (SQL) and Query By Example (QBE). Some minicomputer data managers, such as Oracle from Oracle Corporation, that have been implemented on microcomputers provide SQL capabilities. Ansa Software's Paradox data manager uses QBE for nonprocedural query processing (see "A Data Manager with Visual Queries," Will Fastie, April 1986, p. 154). DataEase, from Software Solutions, provides its own DataEase Query Language (DQL) with procedural and nonprocedural components (see "A Data Manager for End-user Development," Dave Browning, September 1986, p. 146).

In a procedural query language, the programmer provides the processing sequence using the syntax of the given language. Structured and procedural statement types such as DO WHILE . . . ENDDO, IF . . . THEN . . . ELSE, DO CASE . . . ENDCASE, and GO TO are used to direct the operation of the data

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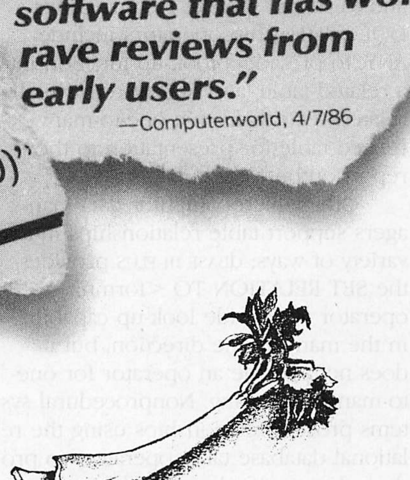

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manager. In a nonprocedural language such as SQL, statements such as SELECT<field list>FROM<table list>, WHERE <table1.field> EQUALS <table2.field>, and ORDER BY <sequence definition> are used to specify the desired table that defines the result of the query. The data manager is left to its own internal devices to establish and optimize a procedure that implements the query definition. QBE specifies nonprocedural statements to the data manager using visual representations of tables and fields.

In both procedural and nonprocedural query methods, queries use existing relationships between tables to retrieve data. Depending upon the tables involved, relationships can be one-to-one, one-to-many, or many-to-one. In the example order-entry system, the relationship between the Order Header and Order Detail tables is one-to-many. Thus, for each order number, many order detail records can be retrieved.

Some procedural and nonprocedural query languages provide relationship operators to reduce the amount of programming necessary to implement queries. For example, DataEase's DQL provides several relationship operators, such as SUM OF, COUNT OF, and HIGHEST OF, to manipulate a table other than the one being processed in accordance with a specified relationship and to return specific results. Other DQL relationship operators include ANY, to provide a look-up function into a related table, and ALL, to retrieve all related records from a one-to-many related table for presentation to the report output program.

Other microcomputer data managers support table relationships in a variety of ways; dBASE III PLUS provides the SET RELATION TO <formula> operator to provide look-up capability in the many-to-one direction, but it does not provide an operator for one-to-many processing. Nonprocedural systems process relationships using the relational database table operators to produce the specified result table.

Procedural methods resemble traditional programming languages and are therefore easier to learn by programmers. Nonprocedural query methods require the developer to learn a new way of viewing the database and query, thinking in terms of database subsets and virtual tables created by operations that manipulate entire tables rather than records and fields. Procedural query definitions are more detailed than nonprocedural ones, but are much easier to understand by individuals without nonprocedural expertise. Nonprocedural query definitions are smaller and can be created easily by developers with some knowledge of nonprocedural techniques.

Procedural query definitions allow the developer to take advantage of knowledge of the database structure to maximize performance, a significant advantage when developing extensive applications on microcomputer systems. Nonprocedural query techniques depend on the data manager to optimize query performance, but require the query developer to know less detail about the internal organization of the database. The selection of a query methodology depends on the choice of data manager and should match the requirements for the database application being developed. This choice is an important part of the design process.

Database structure design, key field selection, index specification, and query techniques all influence overall system performance and require developers to pay attention to such design details. Common queries and reports should be developed and optimized for performance by the developer and provided to the end user as a set of standard reports, usually on a menu. Many other common queries can be reduced to a small set of parameters, such as date ranges, geographic regions, or department numbers, that can be requested from the end user by a developer's predefined query program.

Security techniques involve preventing physical system access, limiting program access, and restricting access to certain tables or fields.

One goal of the development effort in nonprocedural database query technology is to provide query capability directly to end users. Projects in artificial intelligence and natural language programming are aimed at allowing database users to communicate data retrieval queries to the data manager without having to learn database technology, programming languages, or artificial nonprocedural query techniques. However, data managers for today's microcomputer users still require the query developer to have fairly detailed knowledge of retrieval techniques and database technology and design.

Reporting. The report process takes the result of a query and presents it in a format specified by the user. Standard reports should be defined early in the system design process so that data elements required for expected reports are accounted for in the database design. Application processing procedures should be established so that data entry and update are completed before any scheduled reports are run.

Data managers invoke a variety of techniques for the formatting of report output. Many data manager report writers permit the report designer to "paint" the report specifications on the screen, locating data elements where desired, adding text and page headers and footers, and establishing group breaks and subtotals. The report processor usually provides functions to calculate totals and subtotals for numeric fields, and many permit other calculations as well. In the example order-entry system, the report writer computes the extended price by multiplying the quantity and price fields from the order detail records as they are printed. Most report writers provide totaling of the virtual extended price field, and some also support calculation of taxes and shipping charges for each order.

Most microcomputer data manager report writers process report specifications at the time that the report is executed. A few actually generate source code from the report specifications; Reports+, the report writer for IBM's Data Edition, generates BASIC source code and merges user source code modifications into the final report program during the report design process (see "A Data Manager for Custom Reports," Dave Browning, January 1987, p. 150).

A flexible, full-feature report design and production capability is a valuable asset to have in a data manager. Often, the data manager's language can be used to write programs to produce unique reports not defined in the report writer, but such programs tend to be complicated because of the need to code page headers and footers, line counters, group headers and footers, and break level subtotals.

Security. A data manager must be able to safeguard sensitive data from access by unauthorized personnel. Various security techniques involve preventing physical access to the computer system, limiting access to the application programs, and restricting access to certain data tables or fields in the database. Different techniques are needed to protect data from determined intruders as opposed to casual snoopers.

Restricting physical access to the computer is the most reliable way to thwart determined intruders and is an easily implemented technique for most businesses and organizations. Encryption of data files so that unauthorized physical access to those files yields only unintelligible gibberish is another source of protection, but this technique extracts a penalty in system performance because data files must be decrypted and encrypted again each time they are used. Further, the encryption programs themselves are vulnerable to unauthorized access.

Many data managers allow users to establish log-on sequences with password schemes. Individual users and groups of users are defined and granted a variety of rights and privileges that specify access to data. Some data managers provide security access definition at the field level; this allows, for example, junior data-entry operators to accomplish routine maintenance of data in personnel files, but prevents them from viewing or changing sensitive information, such as salaries.

Utilities. Each database system design should include a set of utility functions to help the database administrator maintain the integrity and consistency of the database and the applications using the database. Data managers often provide some utility functions, but the need usually develops for additional utilities that are designed for the specific database or application.

When a data manager uses separate index files, a utility is needed to recreate all index files. If the data manager does not provide data dictionary management features, then a utility to list all data field descriptions and data file structures is helpful. Programs to verify the integrity and consistency of database values may be needed.

Backup. In large mainframe databases, physical backup of storage devices is combined with transaction logging and audit trail processing to support restoration of a damaged database. Physical backup of microcomputer storage using DOS backup or tape backup subsystems should be provided as a part of the overall system design. Transaction logging and audit trail techniques also should be considered.

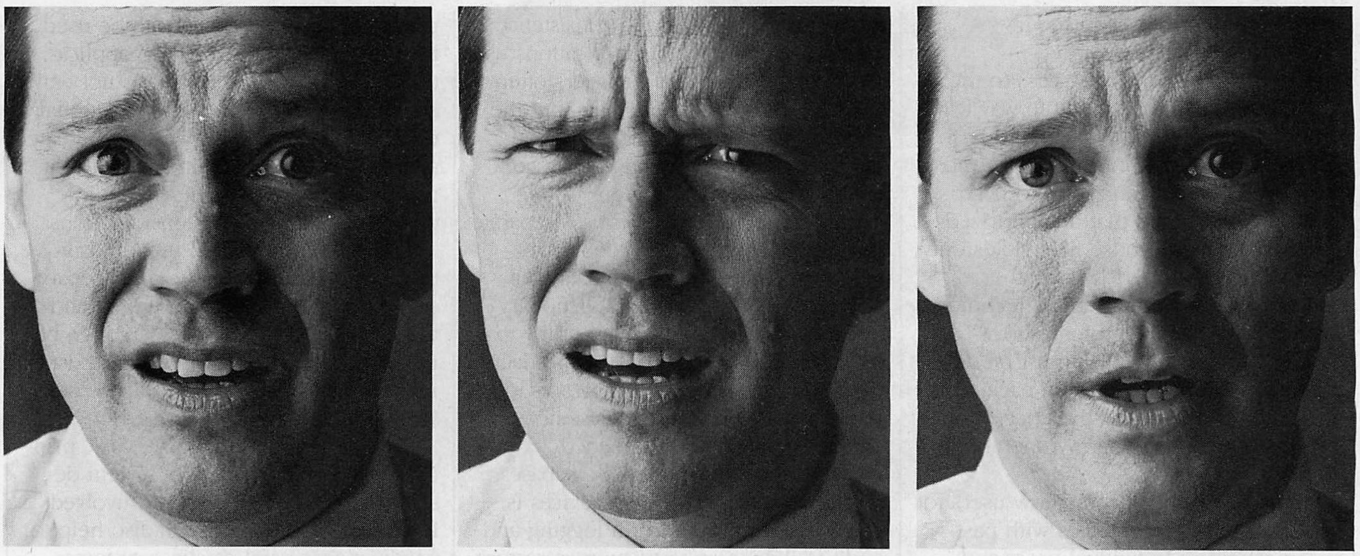
REAL-WORLD DATA MANAGERS

Understanding the basic principles of database system design can help both developers and users create more effective and efficient database systems. The relational database model can be used to represent many real-world applications, but the representation is not exact. A basic understanding of relational database technology is needed to create systems that deviate from theoretically pure designs where necessary to accommodate real-world considerations.

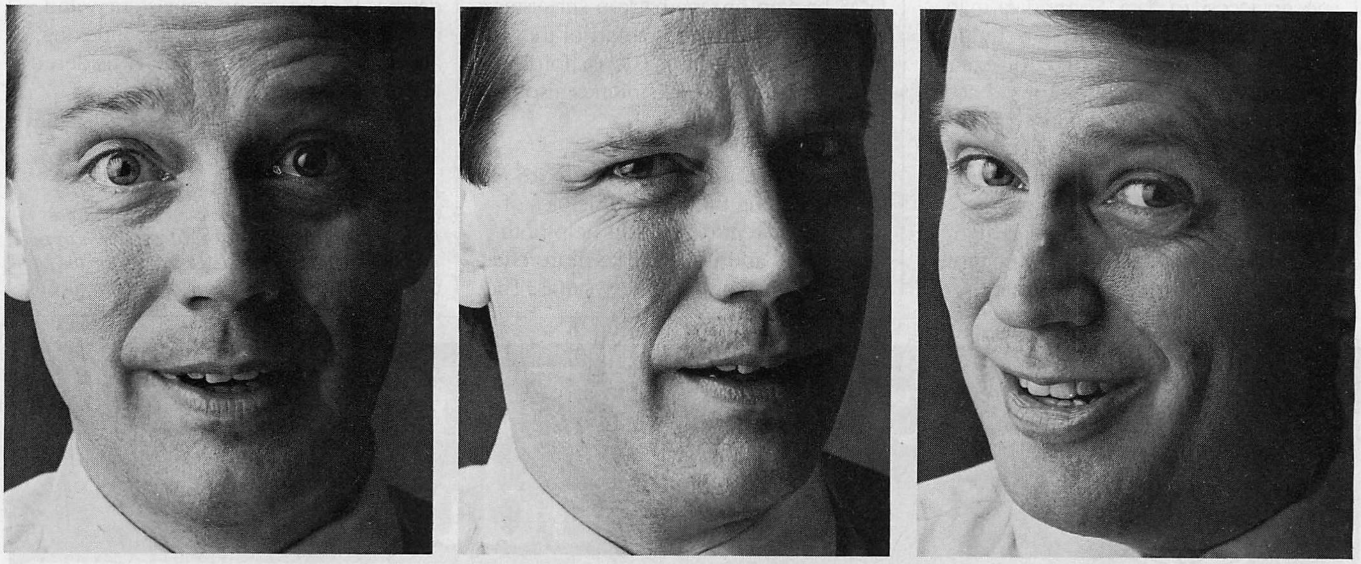
Using the relational model, database structures can be designed separately from application programs, and modifications to databases can often be implemented without disrupting existing applications. A single database design can support many applications.

An understanding of the basic principles of general top-down system design and the functional roles involved in system development can also help to produce successful database systems. The concept of transaction processing should be applied to help preserve database integrity and consistency, and techniques such as key fields, indexing, and query methods must be considered in addressing the important issue of system performance.

Dave Browning is vice president and co-owner of WBS and Associates, Inc., a database consulting firm. He is also chairman of the database special interest group for the Capital PC User Group in Washington, D.C.



1:24: *"They want the report in the morning. I'll be here all night."*



3:47: *"This is going too fast. I must be forgetting something."*

5:05: *"Having saved the day again, our hero rides off into the sunset."*

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Keying on a Standard

The 101-key enhanced keyboard, declared the standard for IBM's entire line of PCs, introduces a fundamental difference in the hardware and software interface to the system.

BOB SMITH

Staying power has never been the strongest attribute of IBM's keyboards. With the introduction of almost every model in the PC line has come a new version of the "standard" keyboard—that's three keyboards in five years. Worse, the differences between keyboards have been more than cosmetic, involving some fundamental software incompatibilities; every new keyboard model required that not only users, but also the software be retrained.

At last, IBM seems ready to end the frustration. The company has stated that all of its personal computers and terminals will use one model: the 101-key Enhanced Keyboard, introduced with the IBM RT PC in January 1986. The enhanced keyboard was subsequently made available with the 8-MHz model of the PC/AT, the XT-286, and the PC/XT models manufactured since April 1986. For reasons explained later, this keyboard cannot be retrofitted to systems not designed to support it.

Keyboard standardization received a boost with the introduction of the IBM Personal System/2 (PS/2) line; all models come with the enhanced keyboard. In fact, IBM has strengthened its commitment to the enhanced keyboard by making it the only model available for the PS/2 machines. (For the AT, the older 84-key model is available on special order as a no-cost option.)

The most obvious differences in the enhanced keyboard from previous models are the set of additional dedicated cursor control keys between the original numeric/cursor control keypad and the typewriter section, the line of function keys (12 instead of 10) across the top, and the shift state indicator lights. Photo 1 shows the layout of the enhanced keyboard. Actually, the enhanced keyboard comes in two versions: a 101-key and a 102-key layout. The latter, available only outside of the U.S., is referred to in IBM documentation as the WT, or World Trade keyboard. It has an additional alphabetical key nestled in the crook of the Enter Key, which is a larger, hook-shaped key on the WT; the backslash is located between the *Z* and the left shift key (as on the original PC keyboard). To support a variety of national languages, the WT keyboard is available with several different layouts of the alphabetic keys.

According to IBM documentation, the U.S. and WT versions of the enhanced keyboard are identical at the software level. The set-up program for the PS/2 models cannot distinguish between them; instead, it asks the user to identify the keyboard by indicating the shape of the Enter key.

SYSTEM INTERFACE

An overview of the enhanced keyboard interface, and its differences from previous models, can best be presented in terms of the incremental changes introduced to that interface with each keyboard model since the original PC.

Figure 1 shows the steps involved in processing keyboard input on a standard PC or XT. Each keystroke sends to the keyboard controller a one-byte scan code, which is a number uniquely identifying the key. The controller places the scan code unchanged in its output buffer, and generates a hardware interrupt that causes the processor to exe-

PHOTOGRAPH • JOHN LEI

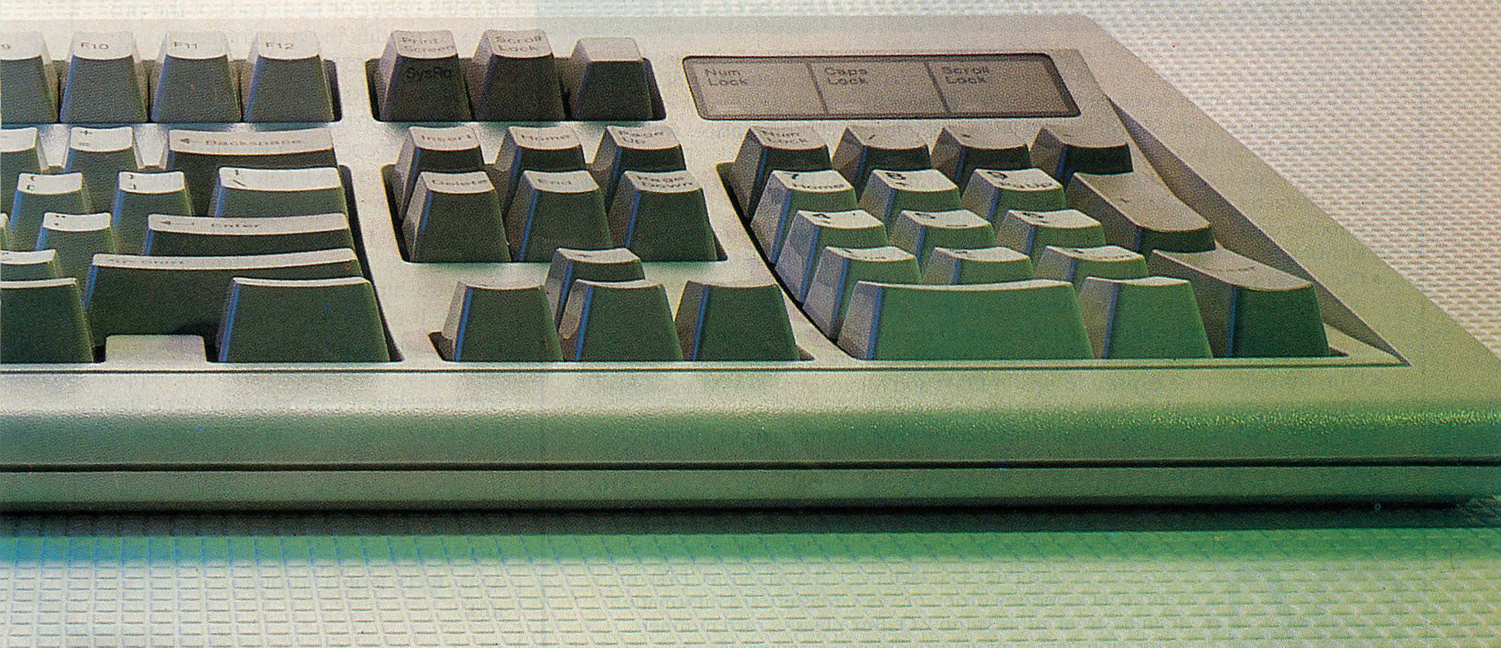

PHOTO 1: *The 101-key Enhanced Keyboard*

The enhanced keyboard has a dedicated cursor keypad and twelve function keys.

cute an interrupt 09H. The interrupt service routine (the default interrupt 09H handler is in the ROM BIOS) looks up the scan code in its internal tables and translates it into a two-byte code. In most cases, one of these bytes is the original scan code and, if the key represents an ASCII character, the other is the ASCII code. For non-ASCII characters, the second byte is usually zero. This two-byte code is placed into the next available location in the circular keyboard buffer, where it waits to be read by an input request from a program. Keyboard read requests are processed by the interrupt 16H handler, which reads the two-byte key codes from the buffer and passes them unmodified to the requesting program.

The 84-key keyboard introduced with the first model of the AT has a different key layout and produces scan codes distinct from those of the original 83-key PC keyboard. The scan-code sets on the two keyboards are different because, for reasons of physical circuit design, it is most efficient to assign scan codes by key location. To maintain compatibility at the software level, IBM introduced a preliminary scan-code translation at the controller level, shown in figure 2. After translation, the controller's output for a given key is the same as that key's output from a PC keyboard controller, thus the interrupt 09H handler and all subsequent software see the same set of key codes as on the original PC.

The 101-key enhanced keyboard introduced yet another key layout. Instead of merely coming up with a new set of scan codes for the new layout, IBM came up with three. By default, the scan-code set made active at boot-up is, for the most part, the same as produced by the 84-key model and is translated by the controller in much the same fashion. Differences arise because the enhanced keyboard produces output for the additional keys not present on the previous models. As shown in figure 3, these differences are handled by an additional translation step at the other end of the process, within the interrupt 16H handler that passes the two-byte codes out of the keyboard buffer to the requesting program.

The enhanced keyboard adds flexibility at two levels. First, the basic scan codes it produces at the keyboard end of the process are not fixed, but can be chosen from three sets. Second, the output at the other end of the process is filtered through an additional layer of translation. Customized programs can modify either or both ends of the process to modify the transformation of keystrokes into program input.

The differences between the enhanced keyboard and previous models go much deeper than layout and key count. One immediately noticeable difference is that, at boot-up, the enhanced keyboard is put in the NumLock state. This change from past behavior adds to the hardship of transition to the new layout. It is a minor symptom of the many changes made to the keyboard itself and to its interface with the support software, but it can be easily remedied. The following program turns off the NumLock bit in the shift status byte that the BIOS uses when reading keystrokes.

```
MOV  AX,40H
MOV  DS,AX
AND  BYTE PTR [17],0DFH
RET
```

It can be assembled into a .COM file (a debugger is more practical than an assembler) and then invoked from the AUTOEXEC.BAT file.

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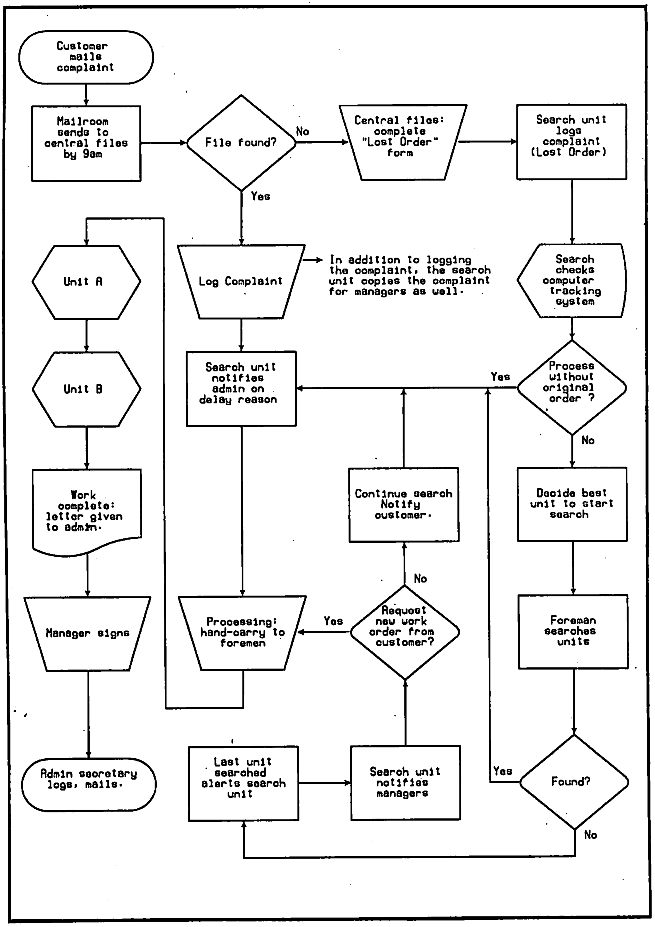

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CIRCLE NO. 113 ON READER SERVICE CARD

BIOS INTERFACE

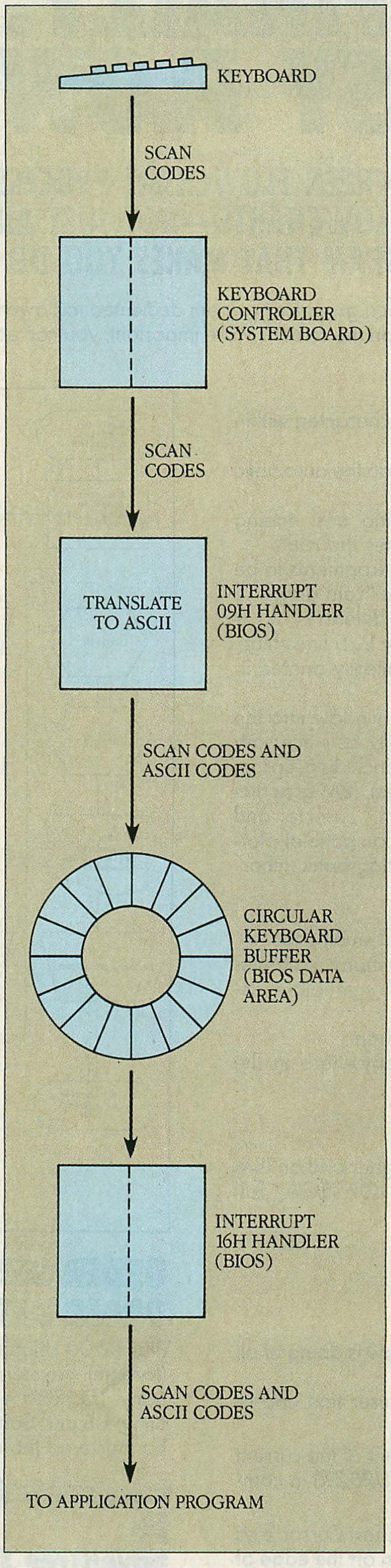
The enhanced keyboard can be used only with systems that support it with an enhanced interrupt 16H handler in the BIOS. According to IBM documentation, this includes the following models: the AT with the BIOS dated 11/15/86 and later; the XT with the BIOS dated 1/10/86 and later; the XT-286; and all of the PS/2 models. The enhanced BIOS routines support 70 new ASCII/scan-code pairs as listed in table 1. Some of these codes are the result of the new keys that are present on the enhanced keyboard (F11, F12, and the additional cursor control keys), while others add support for combinations of keys that were present but not recognized on previous keyboards (for example, Ctrl-up arrow, Ctrl-down arrow, and *5* on the numeric keypad).

In describing the keys on the right-hand side of the various keyboards, the following terminology will be used. Cursor control keys on the original numeric keypad will be named without prefix, such as Home or Del. Other keys around the keypad will be prefixed with *Pad-*, as in Pad-Enter or Pad-asterisk. Finally, the dedicated cursor control keys between the keypad and the typewriter section will be prefixed with *X*, as in X-up arrow and X-End.

The functions provided by the enhanced interrupt 16H handler are summarized in table 2. Two functions are used for reading characters from the keyboard buffer (AH = 00H and AH = 10H) and two are used for determining the presence of characters in the buffer (AH = 01H and AH = 11H). For keys that are common to both the 84-key and 101-key keyboards, each pair of functions operates identically. But their action is different for keys that are present only on the enhanced keyboard. The handling of the new keys by the standard and enhanced functions is listed in table 1. This information is not formally documented; it was determined by reading the BIOS listings and verifying it with test programs.

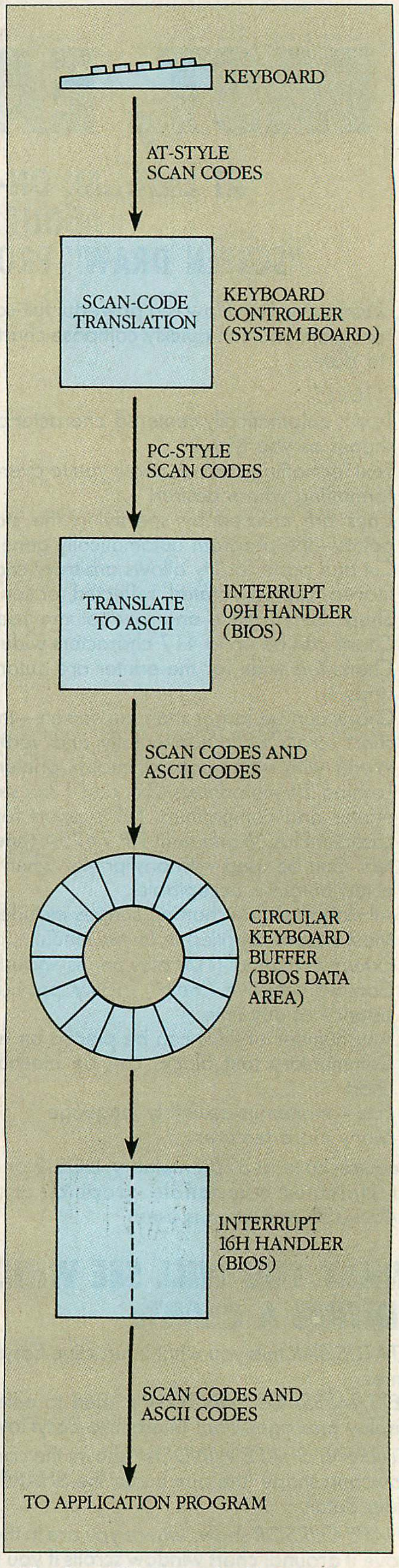
When a standard function encounters an enhanced key code, the code is either discarded or, if it duplicates one of the standard keys, is translated to a standard key code. Thus, the codes for pad-Enter and pad-slash are translated to the codes for Enter and slash in the standard set of keys. If, for example, F11 is the only key in the buffer and an AH = 01H call requests buffer status, the response is that no keys are present in the buffer. Unfortunately, that response turns out to be true because, after the call, there are in fact no keys in

FIGURE 1: *PC Processing*



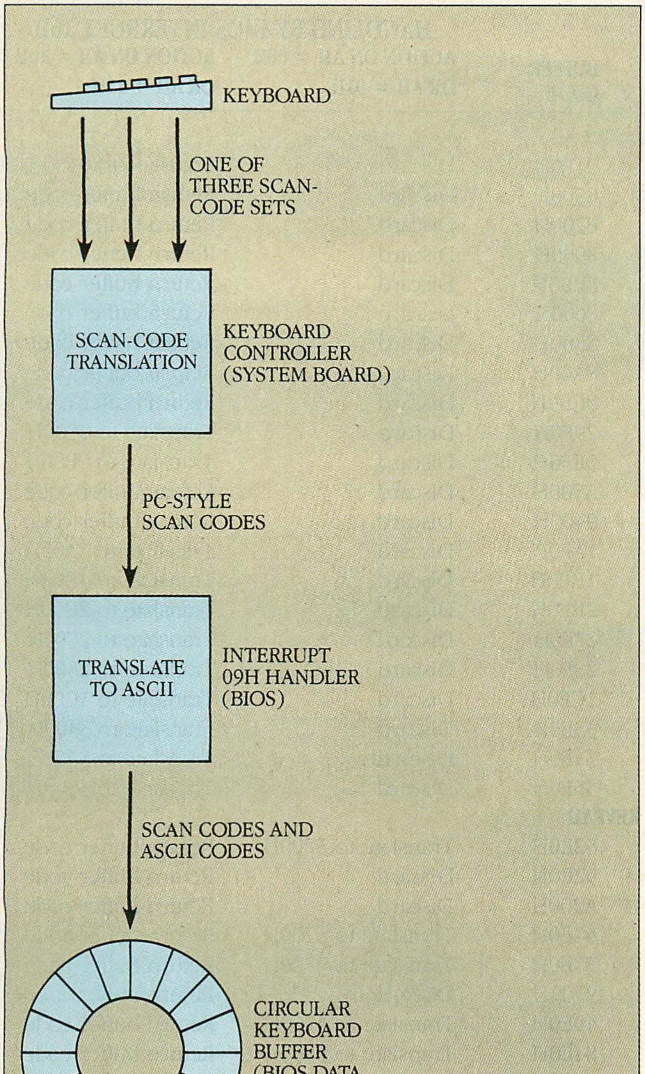
The PC introduced the concept of translating keystroke data into character codes and extended key codes. It applied one level of translation.

FIGURE 2: *84-key Processing*

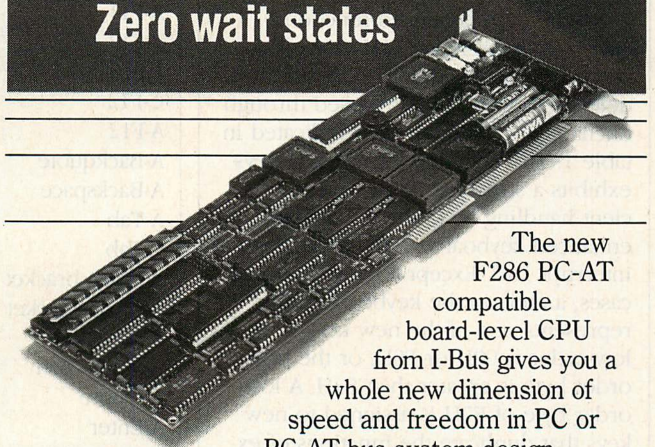


The first AT keyboard added another layer of translation at the level of the keyboard controller. Above that, the data are the same as in the PC.

FIGURE 3: *101-key Processing*



The enhanced keyboard added the capability of switching scan-code sets. Recognizing the new keys requires enhanced support to be present in the keyboard routines of the BIOS.




the buffer—the F11 key gets deleted by the status call. The effect is that programs not written for the enhanced keyboard see nothing different when keys specific to the enhanced keyboard are pressed. That approach is overly conservative because all programs should be written to handle unknown keystrokes. Furthermore, this unconditional deletion of keys can create problems even for programs that use only the enhanced BIOS functions.

When the enhanced functions (AH = 10H and AH = 11H) are used, however, enhanced key codes are never deleted; they are either passed through unchanged or translated as indicated in table 1. The encoding of the new keys exhibits a structure designed for efficient handling by both the standard and enhanced keyboard reading functions of interrupt 16H. Except for a few special cases, a code in the keyboard buffer represents one of the new keys if its low-order is 00H or F0H, or the high-order byte is greater than 84H. A low-order byte of E0H is assigned to new keys that duplicate the functions of existing keys, such as those on the dedicated cursor control keypad. A low-order byte of F0H is assigned to keys that exist on the 84-key keyboard but are ignored by earlier versions of the BIOS, such as Pad-5 and Ctrl-up arrow. A high-order byte greater than 84H is used for totally new keys, such as F11 and F12.

The translation rules for new keys, when read with functions AH = 00H and AH = 01H, are as follows:

- If high byte > 84H, discard the entry;
- If low byte = F0H, discard the entry;
- If low byte = E0H, set low byte to 0 and return that entry.

The exceptions are E00DH (Pad-Enter), which is translated to 1C0DH (Enter); E00AH (Ctrl-Pad-Enter), which is translated to 1C0AH (Ctrl-Enter or LF); E02FH (Pad-slash), which is translated to 352FH (slash); and 00E0H (Alt-Pad 224, Greek alpha) and 00F0H (Alt-Pad 240, triple horizontal line), which are returned unchanged.

For functions AH = 10H and AH = 11H, the rules are simpler. If the low-order byte is F0H, it is changed to 00H and returned; all other key codes are returned unchanged. These codes represent keys present on the standard keyboard, but recognized only by the enhanced BIOS functions.

To take advantage of these new ASCII/scan-code pairs, programs must use the extended interrupt 16H BIOS functions, AH = 10H and AH = 11H. Requesting input through DOS will not work because DOS is not sensitive to the enhanced keyboard—it uses the standard low-numbered calls only. Surprisingly, this is true even for version 3.3 (specifically written to support the PS/2 series, which requires the enhanced keyboard). However, using the BIOS instead of DOS calls for keyboard I/O means that the input redirection facilities of DOS are not available.

DOS calls to the keyboard routine cannot always be prevented; the resulting behavior can be quite hard to diagnose. Suppose that a program consistently uses the enhanced interrupt 16H functions so it can accept the extended keystrokes. However, if the user presses any enhanced key while the system is displaying characters on the screen, that keystroke is lost. Where did it go? When running with BREAK ON, DOS checks for Ctrl-Break and Ctrl-C each time it outputs a character to the display. It does so by requesting keyboard status with interrupt 16H function AH = 01H, thus deleting all leading extended keystrokes from the buffer. One solution to this problem is to install a customized interrupt 16H handler that converts all AH = 00H and AH = 01H calls to AH = 10H and AH = 11H respectively. Listing 1 shows such a program. With the customized handler installed, it becomes possible to use DOS calls in programs that need to receive the enhanced keys, thus restoring the input redirection capability.

The enhanced interrupt 16H handler also has two functions that return

TABLE 1: *Handling of New Keys by BIOS Interrupt 16H*

		HANDLING BY BIOS INTERRUPT 16H	
KEYNAME	BUFFER CODE	ACTION ON AH = 00H OR AH = 01H	ACTION ON AH = 10H OR AH = 11H
TYPEWRITER KEYS			
A-Esc	01F0H	Discard	Translate to 0100H
F11	8500H	Discard	Return buffer code
S-F11	8700H	Discard	Return buffer code
C-F11	8900H	Discard	Return buffer code
A-F11	8B00H	Discard	Return buffer code
F12	8600H	Discard	Return buffer code
S-F12	8800H	Discard	Return buffer code
C-F12	8A00H	Discard	Return buffer code
A-F12	8C00H	Discard	Return buffer code
A-Backquote	29F0H	Discard	Translate to 2900H
A-Backspace	0EF0H	Discard	Translate to 0E00H
A-Tab	A500H	Discard	Return buffer code
C-Tab	9400H	Discard	Return buffer code
A-Open bracket	1AF0H	Discard	Translate to 1A00H
A-Close bracket	1BF0H	Discard	Translate to 1B00H
A-Backslash	2BF0H	Discard	Translate to 2B00H
A-Semicolon	27F0H	Discard	Translate to 2700H
A-Quote	28F0H	Discard	Translate to 2800H
A-Enter	1CF0H	Discard	Translate to 1C00H
A-Comma	33F0H	Discard	Translate to 3300H
A-Period	34F0H	Discard	Translate to 3400H
A-Slash	35F0H	Discard	Translate to 3500H
DEDICATED CURSOR KEYPAD			
Insert	52E0H	Translate to 5200H	Return buffer code
C-Insert	92E0H	Discard	Return buffer code
A-Insert	A200H	Discard	Return buffer code
Home	47E0H	Translate to 4700H	Return buffer code
C-Home	77E0H	Translate to 7700H	Return buffer code
A-Home	9700H	Discard	Return buffer code
PageUp	49E0H	Translate to 4900H	Return buffer code
C-PageUp	84E0H	Translate to 8400H	Return buffer code
A-PageUp	9900H	Discard	Return buffer code
Delete	53E0H	Translate to 5300H	Return buffer code
C-Delete	93E0H	Discard	Return buffer code
A-Delete	A300H	Discard	Return buffer code
End	4FE0H	Translate to 4F00H	Return buffer code

KEYNAME	BUFFER CODE	HANDLING BY BIOS INTERRUPT 16H ACTION ON AH = 00H OR AH = 01H	ACTION ON AH = 10H OR AH = 11H
C-End	75E0H	Translate to 7500H	Return buffer code
A-End	9F00H	Discard	Return buffer code
PageDown	51E0H	Translate to 5100H	Return buffer code
C-PageDown	76E0H	Translate to 7600H	Return buffer code
A-PageDown	A100H	Discard	Return buffer code
Up arrow	48E0H	Translate to 4800H	Return buffer code
C-Up arrow	8DE0H	Discard	Return buffer code
A-Up arrow	9800H	Discard	Return buffer code
Left arrow	4BE0H	Translate to 4B00H	Return buffer code
C-Left arrow	73E0H	Translate to 7300H	Return buffer code
A-Left arrow	9B00H	Discard	Return buffer code
Down arrow	50E0H	Translate to 5000H	Return buffer code
C-Down arrow	91E0H	Discard	Return buffer code
A-Down arrow	A000H	Discard	Return buffer code
Right arrow	4DE0H	Translate to 4D00H	Return buffer code
C-Right arrow	74E0H	Translate to 7400H	Return buffer code
A-Right arrow	9D00H	Discard	Return buffer code
NUMERIC KEYPAD			
Slash	E02FH	Translate to 352FH	Return buffer code
C-Slash	9500H	Discard	Return buffer code
A-Slash	A400H	Discard	Return buffer code
C-Asterisk	9600H	Discard	Return buffer code
A-Asterisk	37F0H	Discard	Return buffer code
C-Minus	8E00H	Discard	Return buffer code
A-Minus	4AF0H	Discard	Return buffer code
C-Up arrow	8D00H	Discard	Return buffer code
C-Plus	9000H	Discard	Return buffer code
A-Plus	4EF0H	Discard	Return buffer code
5	4CF0H	Discard	Return buffer code
C-5	8F00H	Discard	Return buffer code
C-Down arrow	9100H	Discard	Return buffer code
C-Ins	9200H	Discard	Return buffer code
C-Del	9300H	Discard	Return buffer code
Enter	E00DH	Translate to 1C0DH	Return buffer code
C-Enter	E00AH	Translate to 1C0AH	Return buffer code
A-Enter	A600H	Discard	Return buffer code

S- = With Shift key C- = With Ctrl key A- = With Alt key

For compatibility with programs that cannot handle the enhanced keys, the BIOS translates or discards key codes unless requested through an enhanced function.

TABLE 2: *BIOS Interrupt 16H Functions*

FUNCTION NUMBER	FUNCTION NAME
AH = 00H	Read keyboard buffer
AH = 01H	Get keystroke status
AH = 02H	Get shift status
AH = 03H	Set typematic delay and repeat rate
AH = 04H	Reserved for PC*jr*
AH = 05H	Write to keyboard buffer
AH = 06H to 0FH	Reserved
AH = 10H	Extended keyboard read
AH = 11H	Get extended keystroke status
AH = 13H	Get extended shift state

The enhanced interrupt 16H handler recognizes eight functions; the last three deal specifically with the keys unique to the enhanced keyboard.

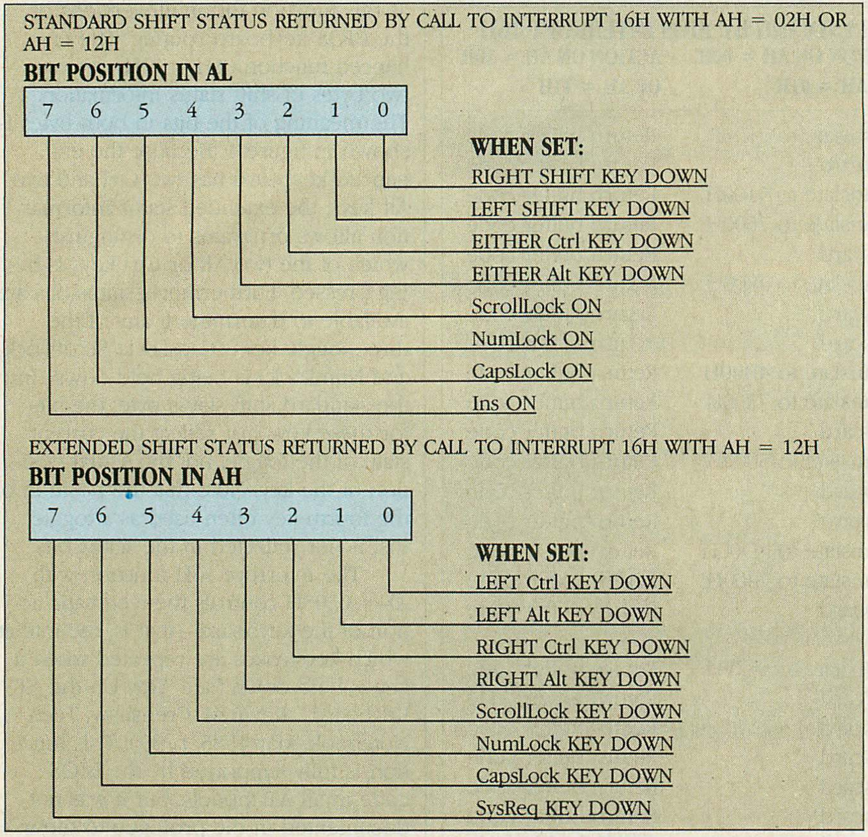
the Shift-key status. Function 2 returns the standard status byte, the same one as this function did in all versions of the BIOS keyboard routine. The enhanced function (AH = 12H) returns two bytes of shift status information. The meaning of the bits in both bytes is shown in figure 4. Because the enhanced keyboard has two Ctrl and two Alt keys, the extended status information allows programs to distinguish which of the two Alt or Ctrl keys is being pressed. Furthermore, status bits are available to determine if any of the three toggle keys (CapsLock, ScrollLock, and NumLock) is being held down. In the standard shift status byte, the bits for these keys just reflect the current state of the toggle, not the actual position of the key. Note that the position of the fourth key often used as a toggle, Ins, is not reflected in the status bits.

The interrupt 16H function with AX = 0305H controls the typematic action of the keyboard—that is, the rate at which keystrokes are repeated when a key is held down (see "Rev Up the AT Keyboard," Kevin M. Crenshaw, Tech Notebook, May 1985, p. 39). This function is fully supported by the BIOS code in all AT models, but it was not documented in the prologue to the interrupt 16H listing in IBM's *Technical Reference Manual*. The latest version of the BIOS documentation (which covers the entire IBM PC line, from the original PC through all the PS/2 models) now supplies this documentation. Two parameters are controlled by the interrupt 16H function: the delay before the repeating action begins, and the rate of repetition once it does begin. Both settings must be specified even though only one is to be changed.

The typematic delay (after which typematic action begins) is changed by setting register BH to a value between 00H and 03H (range-checked by the BIOS). The values BH = 00H, 01H, 02H, and 03H correspond to delays of 250 milliseconds (ms), 500 ms, 750 ms, and 1000 ms respectively. The typematic rate is set by the value in BL; it is also range-checked and must be between 00H and 1FH. Setting BL = 00H corresponds to 30 characters per second (cps); BL = 0BH restores the default rate of 10.9 cps; and BL = 1FH slows the keyboard down to 2 cps. Many fine gradations are possible, but the repeating action cannot be turned off.

This function requires AL = 05H. Support to control the typematic rate was introduced in the PC*jr* BIOS, which defines subfunctions AL = 00H through 04H. The enhanced keyboard's type-

FIGURE 4: *Keyboard Shift Status Bytes*



The BIOS maintains an accurate record of the position of certain keys in these two bytes. They are returned in AX from interrupt 16H function AH = 02H.

matic feature is unlike any of the PC*jr*'s, so a new subfunction was defined. None of the PC*jr* subfunctions is supported by the AT BIOS. The typematic feature, while supported in most AT compatibles and 80386-based machines, should be treated carefully. For example, the Phoenix 80386 ROM BIOS (version 3.03 and earlier) decrements AX and then jumps to code that checks for AL = 05H. Consequently, AX = 0306H is required to set the typematic parameters in that BIOS. This bug has been fixed in versions 3.04 and later.

The final enhanced function of the interrupt 16H handler is AH = 05H, the insert key code, which inserts the ASCII/scan-code pair from CX into the keyboard buffer as if it had just been typed at the keyboard (that is, at the end of the first-in, first-out buffer). The BIOS does absolutely no checking of the value. The CH register contains the scan code; CL contains the ASCII character (or extended ASCII code). Carefully follow the translation rules that were outlined above when placing codes into the buffer. For the new keys, codes retrieved from the buffer are not necessarily the same as the codes placed into it; when using functions 00H and 01H, some codes are never retrieved.

Function 05H can be used to seed the keyboard buffer with a program's input prior to invoking that program, although the default buffer size of 15 keys may be too limiting. This is different from redirecting standard input because, after all the key codes have been read from the buffer, the program waits for further input from the keyboard. With redirection, the program hangs at the end of the input file.

A feature in the BIOS interface can be used to identify the keyboard as either the 84-key or 101-key model. The byte at address 40:96H of the BIOS data area will have bit 4 set to 1, if the enhanced keyboard was detected on bootup, or 0, if otherwise. This feature is documented in the latest BIOS reference manual, so it should be supported by compatibles. It is implemented in Compaq models and in the Phoenix BIOS versions 3.02 and later for 80286- and 80386-based machines.

Testing this bit is the easiest way of determining the keyboard type, but the result reflects the keyboard present when the system was last booted. Because it is possible to switch keyboards without resetting the system, a different keyboard may be present at the time of the test. A method for determining the type of keyboard currently attached is described in a later section.

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HummingBoard-16Mhz	2,777	6,718	8.5
HummingBoard-20Mhz	3,571	8,470	10.7
Vax 8600 (Unix 4.3 BSD,cc)		6,423	8.1
Sun 3/160 (Sun 4.2 3.0A,cc)		3,246	4.1

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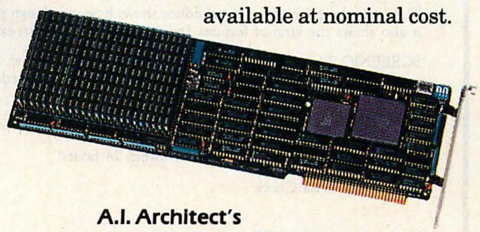

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CIRCLE NO. 253 ON READER SERVICE CARD

THE KEYBOARD CONTROLLER
Normally, communications between programs and the keyboard takes place by way of the BIOS calls explained above. The BIOS routines perform the actual I/O to the keyboard controller. Occasionally, programs might need to talk directly to the hardware in order to perform functions not supported by the BIOS. One example is in determining the type of keyboard attached.

The keyboard system consists of a Motorola 6805 microprocessor within the keyboard and an Intel 8042 controller on the motherboard. Programs can communicate with either chip. The only information on this subject is scattered over several sections of the *Technical Reference Manual*; it is cryptic and occasionally misleading. For example, the manual does not distinguish between the keyboard and the controller, using the term ***keyboard*** to refer to either or both the 6805 and 8042.

The 8042 keyboard controller on the motherboard directs communications traffic between the system and the keyboard. The controller is implemented identically in all models of the AT, regardless of the keyboard support present in the BIOS. In the PS/2 models, the functions of the 8042 are a superset of those in the AT. This article considers only the AT implementation.

The controller communicates with the keyboard via a serial link that supports either an 11-bit protocol with parity checking or a 9-bit protocol without it. The former is the format used by the AT keyboard, the latter by the original PC keyboard. At boot-up, the keyboard is in the 11-bit mode, which supports either the standard or enhanced AT keyboard. The controller can be switched into 9-bit mode to support the original 83-key PC keyboard.

By default, the 8042 translates the scan codes it receives from the 6805 to those recognized by the BIOS. The translation table is kept in ROM on the 8042 chip and is not accessible to programs; it is published in the *Technical Reference Manual*. As each scan code is received, the 8042 interrupts the processor. Both the translation and the generation of the interrupt can be disabled by reprogramming the controller.

The system and 8042 communicate with each other via a status register, an input buffer, and an output buffer. The 8042 also has a program-accessible command byte that controls its actions. All are accessed via I/O ports. The *Technical Reference Manual* also refers to additional components of the 8042: an input port, an output port, and a test input port. However, they are neither directly accessible as I/O ports nor involved in the keyboard interface. The input port contains the value of switch settings and jumpers on the system board (such as the keyboard-lock and display-adapter switches). The output port (which, despite its name, can be read from as well as written to) is used only during system start-up and shutdown, while the test input port is used only for hardware checkout.

The 8042 status register is a read-only port located at I/O address 64H. Its contents may be read at any time; the bit definitions are summarized in figure 5. Its most important function is to synchronize data flow between the controller and the system.

The output buffer (from the 8042 to the system) is a read-only port located at I/O address 60H. From it, the system can read the scan codes received from the 6805 (after translation, if that feature is enabled) and responses to 8042 commands. An instruction to read this port should be executed only when the status register indicates that

FIGURE 5: *8042 Status Register*

BIT POSITION IN AL

BIT	WHEN SET	WHEN CLEAR
0	OUTPUT BUFFER FULL, RESPONSE FROM 8042 READY	OUTPUT BUFFER EMPTY, NO RESPONSE READY
1	INPUT BUFFER FULL, DO NOT SEND COMMAND	INPUT BUFFER EMPTY, OK TO SEND COMMAND
2	IF DURING STARTUP, RETURNING FROM SHUTDOWN	IF DURING STARTUP, NORMAL POST
3	LAST INPUT WAS A COMMAND	LAST INPUT WAS DATA
4	KEYBOARD LOCKED (VIA KEY)	KEYBOARD UNLOCKED
5	8042 TO 6805 TRANSMIT TIMEOUT	NO TIMEOUT
6	6805 TO 8042 TRANSMIT TIMEOUT	NO TIMEOUT
7	PARITY ERROR FROM 6805	NO PARITY ERROR

A program can be used to determine the status of the keyboard controller at any time by reading this byte from an I/O port.

FIGURE 6: *8042 Command Byte*

BIT POSITION

BIT	WHEN SET	WHEN CLEAR
0	ENABLE KEYBOARD INTERRUPT	DISABLE KEYBOARD INTERRUPT
1		RESERVED (SET TO 0)
2	IF DURING STARTUP, RETURNING FROM SHUTDOWN	IF DURING STARTUP, NORMAL POST
3	DISABLE KEYLOCK	ENABLE KEYLOCK
4	DISABLE KEYBOARD	ENABLE KEYBOARD
5	IBM PC KEYBOARD MODE	IBM AT-KEYBOARD MODE
6	TRANSLATE SCAN CODES	DOES NOT TRANSLATE
7		RESERVED (SET TO 0)

The value that is sent to the keyboard controller in this byte can fundamentally alter the standard operation of the keyboard.

the output buffer is full; at other times the result is undefined. There is no clear indication as to how long the 8042 might take to respond to a command to fill its output buffer. An 8-MHz AT waits for about 1,200 ms for this condition, using a programmed delay loop. When the system reads the output buffer, bit 0 of the status register (output buffer full) is automatically cleared.

The input buffer (from the system to 8042) is a one-byte write-only port that can be addressed as either I/O port 60H or 64H. Commands to the 8042 are written to port 64H; data for the 8042 and for the 6805 are sent to port 60H. Nothing should be sent to the input buffer unless the status register indicates that it is empty. As with the output buffer, there is no clear indication as to how long a program should wait for the 8042 to read its input buffer, but the BIOS code for an 8-MHz AT uses a programmed delay loop of approximately 200 ms. The OUT instruction to either port address automatically sets bit 1 (input buffer full flag) of the status register. The 8042 resets the bit when it reads the input byte.

The commands to the 8042 are listed in table 3; they are sent to I/O port 64H. Commands 60H and D1H require that a subsequent byte of data be sent to I/O address 60H. The commands numbered C0H and higher manipulate the ports containing system initialization and test settings; they are not part of the keyboard interface.

Commands 20H and 60H read and write, respectively, the 8042 command byte. The bit definitions within this byte are shown in figure 6. The effect of setting or clearing each bit is only vaguely documented in the *Technical Reference Manual*, and much of it needs to be developed by hands-on testing.

When turned on, bit 0 causes the 8042 to interrupt the processor on IRQ1 when the controller's output buffer is full. Turning this bit off effectively disables the keyboard, just as resetting bit 4 does. The quickest way of disabling and enabling the keyboard, however, is by sending commands ADH and AEH to I/O port 64H. These commands directly control bit 4 of the command byte with only one OUT instruction.

Bit 6 of the command byte controls what the *Technical Reference Manual* calls *personal computer compatibility mode*, or the translation of scan codes by the controller. When this bit is set to a 1, scan codes are translated from those generated by an AT keyboard to those generated by the same keys on a PC keyboard. The BIOS, even on an AT, recognizes only the PC set of scan codes, and the keyboard generates garbage if the translation is turned off.

The *Technical Reference Manual* is vague about how bit 5, the *personal computer mode* bit, differs from bit 6. (It allows the use of the original PC keyboard on an AT.) When the bit is set, the 8042 is placed into a 9-bit serial

TABLE 3: *8042 Commands*

HEXADECIMAL COMMAND	MEANING
20	Place current 8042 command byte into output buffer
60	Read next byte as 8042 command byte (see table 4)
AA	Self-test: if OK, put 55H into output buffer
AB	Interface test: zero output if 6805 interface lines OK
AC	Diagnostic dump: return 20 bytes of information
AD	Disable 6805 interface—no data are processed, commands only
AE	Enable 6805 interface
C0	Place input port value into output buffer
D0	Place output port value into output buffer
D1	Replace output port value with next byte sent to port 60H
E0	Place test input values into output buffer
F0–FF	Pulse low-order three bits of output port (FE is used for system shutdown)

The BIOS and other programs can communicate with the keyboard by sending the commands summarized here to the 8042 controller on the system board.

protocol with no parity checking—the protocol used by the PC keyboard. Because this mode is intended for use with a keyboard that generates the scan codes expected by the BIOS, scan-code translation is turned off.

However, this support of the original PC keyboard is only half-heartedly implemented. At boot-up, the 8042 in the AT is initialized to communicate with an AT-style keyboard; if the older model is connected, the boot process stops on a keyboard error. The screen displays the message "Press F1 to resume," but the system cannot recognize any data from the keyboard, including Ctrl-Alt-Del. The machine must be turned off in order to reboot.

The PC keyboard can be used with the AT by following this sequence: boot up the system with an AT keyboard (either model); run a program to switch the 8042 into PC mode; after the program runs, do not press any key on the AT keyboard or the system will crash; unplug the AT keyboard and plug in a PC keyboard. The system beeps a few times, but then functions properly.

The most surprising aspect of the keyboard controller is its ability to be programmed to ignore the keyboard-lock switch on the front panel. If bit 3 of the command byte is turned on, the keyboard is active no matter what the position of the lock.

At boot-up, the BIOS initializes the 8042 command byte to 45H, which enables the following features: scan-code translation, AT-keyboard mode, data transfer to and from the 6805, the keyboard lock, and the generation of interrupts at each keystroke.

THE HARDWARE INTERFACE

The Motorola 6805 microprocessor resides in the keyboard. It scans the data lines from the keys and sends to the 8042 the scan code of each key as it is pressed and released. The microprocessor is present in the standard and enhanced AT keyboards, but the command set incorporated in each is different. The differences can be used by a program to determine which keyboard is attached to the system.

The system and the 6805 communicate with each other via I/O port 60H. Commands from the system to the 6805 are sent via OUT 60H,AL. Because that port is also the input buffer of the 8042 controller, these writes are intercepted by the 8042. The determination of whether the data byte is intended for the 8042 or for the 6805 is made by the state of the command/data bit (bit 3) of the 8042 status register (see figure 5). The state of this bit is maintained automatically by the 8042 as it receives commands via port 64H. If the previous write to port 64H was a controller command requiring a subsequent data byte, the byte written to port 60H is kept by the 8042; otherwise, the data are passed through to the 6805. The commands from the system to the 6805 are summarized in table 4. Those marked with an asterisk are supported only by the enhanced keyboard and are treated as no-operations by the 84-key model.

The 6805 responds to all transmissions by sending one or more bytes to the output buffer of the 8042. The system can read each of these bytes by executing an IN AL,60H. As with all

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communication involving the I/O buffers, a program must determine that the input buffer is empty before sending a command to it and that the output buffer is full before reading from it. Generally, the 6805 responds to a command within 20 ms. To the 8042, all data coming from the 6805 (whether scan codes or command responses) are equivalent. If scan-code translation is enabled, any incoming data with a value that matches a scan code are translated by the 8042. Therefore, in order to get correct command responses from the 6805, a program should disable translation for the duration of the communication.

TABLE 4: *Commands from the System to the 6805*

HEXADECIMAL COMMAND BYTE 1	BYTE 2	MEANING
ED	xx	Set/reset LED status indicators
EE		Echo (response is ECHO)
EF*		Invalid command (response is RESEND)
F0*	00	Inquire as to current scan-code set
F0*	xx	Select alternate scan-code set xx (1, 2, or 3)
F1*		Invalid command (response is RESEND)
F2*		Read keyboard ID (responses listed in table 5)
F3	xx	Set typematic rate and delay
F4		Enable keyboard
F5		Set default state and stop scanning
F6		Set default state and start scanning
F7*		Set all keys in scan-code set 3 to typematic
F8*		Set all keys in scan-code set 3 to make/break
F9*		Set all keys in scan-code set 3 to make only
FA*		Set all keys in scan-code set 3 to typematic/make/break
FB*	xx	Set a key in scan-code set 3 to typematic
FC*	xx	Set a key in scan-code set 3 to make/break
FD*	xx	Set a key in scan-code set 3 to make only
FE		Resend last output
FF		Reset 6805, self-test

* *Supported only by the enhanced keyboard; treated as no-operations by the 84-key model.*

At the lowest level accessible with programming, these commands control the operation of the keyboard microprocessor. They are sent via OUT 60H,AL.

TABLE 5: *Responses from the 6805 to the System*

HEXADECIMAL RESPONSE BYTE 1	BYTE 2	MEANING
00		Key detection error or overrun for scan code sets 2 and 3
01		Scan-code set 1 is currently selected
02		Scan-code set 2 is currently selected
03		Scan-code set 3 is currently selected
AA		Basic assurance test (BAT) completion code
AB	83	Keyboard ID
EE		Echo
FA		Acknowledge (used for all but ECHO and RESEND)
FC		Basic assurance test (BAT) failure code
FE		Resend last command
FF		Key detection error or overrun for scan code set 1
FF		Reset 6805, self-test

Besides sending the scan codes that corresponds to a user's keystrokes, the keyboard also sends the responses to system level commands (via OUT 60H,AL).

Responses from the 6805 are summarized in table 5. Most often, the response is ACK (acknowledge, FAH). For the two-byte commands, the 6805 responds to the initial byte with an ACK, stops scanning for keystrokes, and waits for the second byte (the option byte). To the two invalid commands, the 6805 responds with Resend (FEH); to the Resend command it responds with the previous output. Two commands (Read ID and Select Scan Code Set) produce responses of multiple bytes.

The BIOS uses the Set/reset LED Status command whenever it detects a change in the NumLock, CapsLock, or ScrollLock status. The low-order three bits of the option byte control the status of the ScrollLock, NumLock, and CapsLock indicators (bits 0, 1, and 2 respectively). Setting the bit turns the corresponding indicator light on; clearing it turns the light off. There is no means to read the current state to enable a program to set or clear just one light without affecting the others.

The Set Typematic Delay command is used by the BIOS interrupt 16H function AX = 0305H. The two parameters from registers BH and BL must be combined into one byte by placing the repeat rate value into bits 0 through 4, and by placing the initial delay value into bits 5 and 6. Bit 7 must be zero. The current setting of the typematic parameters cannot be interrogated.

The Echo command can be used to determine whether or not an AT-compatible keyboard is attached to the system. If, in reasonable time, the keyboard responds with Echo (EEH), the AT-style keyboard is determined to be present. Note that this response does not indicate whether or not an enhanced keyboard is present, only that it is AT compatible. In practice, setting the typematic rate and delay should work.

Only the enhanced keyboard supports the Read ID command; this command can be used to distinguish between 84-key and 101-key models. Both keyboards respond to this command with ACK, but the enhanced keyboard then follows this response with two more bytes: ABH and 83H. A program that tests the keyboard type should be written to time out if no further response is received within 500 ms of the initial response. A valid response to this command indicates that the enhanced keyboard is present, and that all of the commands in table 6 are valid.

This is the test used by the boot-up routine when setting the keyboard ID bit in location 40:96H of the BIOS data area. The boot-up routine indicates an enhanced keyboard if the second ID byte is either 83H or 85H. All of the keyboards tested (from IBM, including the PS/2 models and several AT compatibles) returned an ID of 83H.

Another feature present only in the enhanced keyboard is support for three scan-code sets. The Select Scan Code

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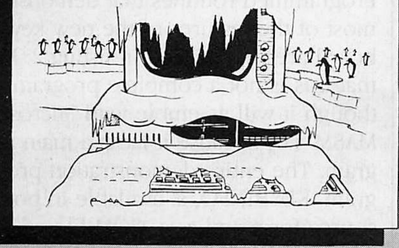

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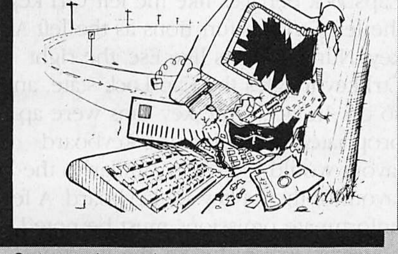

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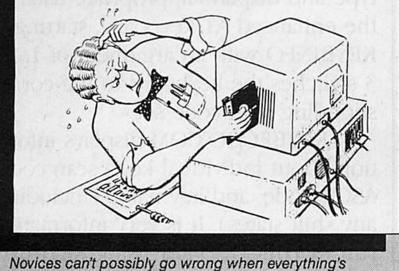

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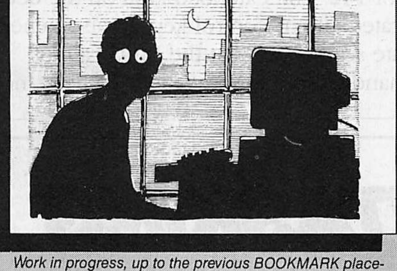

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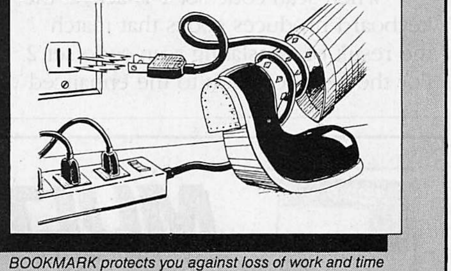

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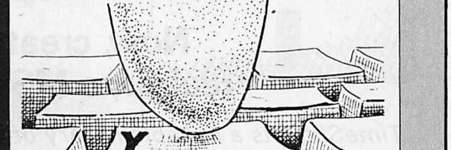

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command (followed by an option byte of 1, 2, or 3) activates the scan-code set of that number. An option byte of zero causes the keyboard to respond with the number of the currently active scan-code set. The code sets differ in the values generated for the press and release of each key. (The *Technical Reference Manual* uses the terms *make* and *break* for *press* and *release*.)

At boot-up, scan-code set 2 is activated by default. For most keys, it sends a single-byte press code and a two-byte release code consisting of F0H followed by the press code. These codes need to be translated to the ones expected by the BIOS interrupt 09H routine. For example, the *B* key sends scan code 32H, which, if passed to the BIOS, would be interpreted as *M*. With code translation enabled, however, the 8042 keyboard controller translates the scan code to 30H (the same as sent by the *B* key of the PC keyboard), which is properly interpreted by the BIOS. The translation process also converts each two-byte release code to a one-byte code that is the same as the press code with the high bit turned on.

When scan-code set 1 is active, the keyboard produces codes that match the result of translating scan-code set 2. For the keys common to the enhanced and original PC keyboards, this code set produces the same press and release codes as the original keyboard. In effect, this code set moves the translation down a level from the 8042 to the 6805, therefore, scan-code translation at the 8042 level must be disabled.

Scan-code set 3 is similar to the default scan code in that it produces the same scan codes for the majority of the ASCII keys and uses the same press/release coding convention. The scan-code translation on the 8042 should be enabled in order to use scan-code set 3. Some keys, though, are curiously reassigned. For example, with scan-code set 3 activated and translation enabled, CapsLock behaves like the left Ctrl key, the left Ctrl key functions as the left Alt key, NumLock acts like Esc, the right Ctrl-key toggles the CapsLock state, and so on. In fact, if the key caps were appropriately relabeled, the keyboard layout would look very similar to the layout of the 84-key AT keyboard. A few unfortunate omissions must be noted, however. Except for F1, the functions keys generate scan codes unknown to the BIOS; F1 generates the scan code for F12. The extended keys on the dedicated cursor control keypad also generate scan codes that the BIOS cannot handle (so it ignores them). Finally, no key generates the scan code for a backslash, and the NumLock, CapsLock, and ScrollLock states cannot be turned off.

Scan-code set 3 has the rather unusual characteristic of allowing the programming of keys to send scan codes only on press, only on release, or both, and enabling or disabling the typematic repeating action. These characteristics may be set for all keys at once, or for individual keys identified by scan code. The support for this scan set is far from complete, therefore, using its features would first require significant and time-consuming programming effort.

SAMPLE PROGRAMS

Programmed routines that demonstrate most of the features of the new keyboard are reproduced in listing 2. Note that this is not a complete program (although it will assemble with Microsoft MASM 4.0) because it lacks a main program. The entire demonstration program, KEYBINFO, is available in both source form and as a .COM file on PCTECHline. This program can be run on any of the three IBM keyboards. It automatically determines the keyboard type and displays appropriate data. On the enhanced AT keyboard, starting KEYBINFO with an argument of 1, 2, or 3 switches the keyboard to the corresponding scan code set.

KEYBECHO.COM displays information about individual keys: scan code, ASCII code, and key name (including any shift states). It is very informative to run KEYBECHO after using KEYBINFO to change the scan-code set. The source for KEYBECHO is in KEYBECHO.C and KEYBMISC.ASM; the object files from compiling the first and assembling the second are to be linked together. This source code is too large to be reproduced here. To ensure downloading of all the necessary components, all source and executable modules have been archived and placed on PCTECHline in the file named ATKEY.ARC.

The enhanced keyboard has many useful features, but its support at both the BIOS level (scan-code set 3) and the operating system level (discarding extended scan codes) is less than complete. Programming for it is tricky because of incomplete documentation. Because IBM finally seems to have settled on this keyboard model, however, it is worthwhile to search for solutions to some of the problems.

Bob Smith is president of Qualitas, Inc., a software development firm in Bethesda, Maryland. He is a member of the Capital PC User Group, Inc. in Washington, DC.

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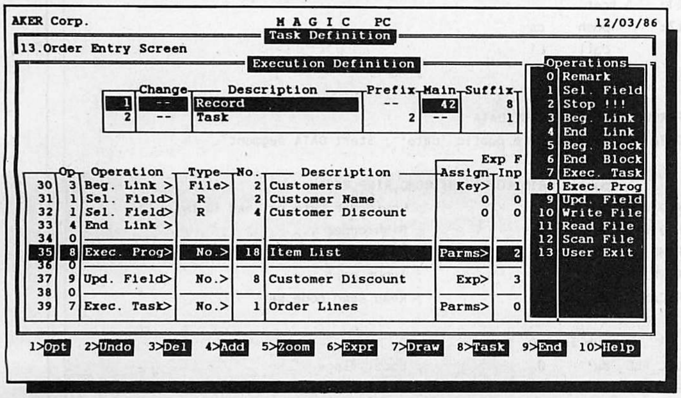
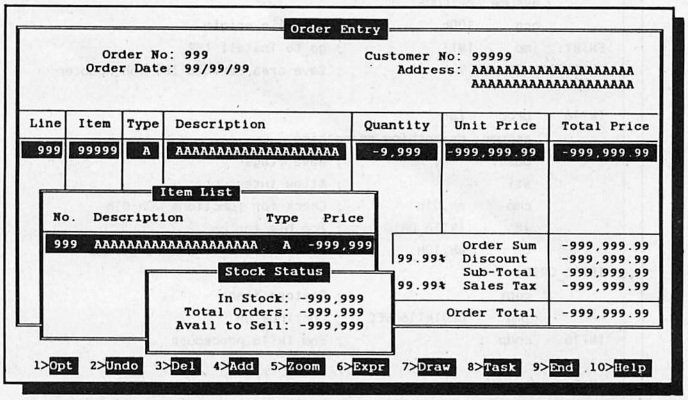


```
AKER Corp.                  M A G I C   PC                  12/03/86
                            Task Definition
13.Order Entry Screen
                         Execution Definition                Operations
                                                              0 Remark
           Change  Description          Prefix Main Suffix    1 Sel. Field
        1    --    Record                 --    42     8      2 Stop !!!
        2    --    Task                    2    --     1      3 Beg. Link
                                                              4 End  Link
                                                              5 Beg. Block
                                                Exp F         6 End  Block
     Op  Operation    Type  No.  Description   Assign Inp     7 Exec. Task
  30  3 Beg. Link >  File>   2 Customers         Key>  1      8 Exec. Prog
  31  1 Sel. Field>   R      2 Customer Name       0   0      9 Upd. Field
  32  1 Sel. Field>   R      4 Customer Discount   0   0     10 Write File
  33  4 End  Link >                                          11 Read File
  34  0                                                      12 Scan File
  35  8 Exec. Prog>   No.>  18 Item List        Parms> 2     13 User Exit
  36  0
  37  9 Upd. Field>   No.>   8 Customer Discount  Exp> 3
  38  0
  39  7 Exec. Task>   No.>   1 Order Lines      Parms> 0
```



```
                              Order Entry
      Order No: 999                    Customer No: 99999
    Order Date: 99/99/99                   Address: AAAAAAAAAAAAAAAAAAAA
                                                    AAAAAAAAAAAAAAAAAAAA

 Line  Item   Type  Description            Quantity   Unit Price   Total Price
  999  99999   A    AAAAAAAAAAAAAAAAAAAA    -9,999   -999,999.99   -999,999.99

            Item List
   No.  Description             Type   Price
   999  AAAAAAAAAAAAAAAAAAAA      A  -999,999
                                                       Order Sum   -999,999.99
                                              99.99%   Discount    -999,999.99
                   Stock Status                        Sub-Total   -999,999.99
              In Stock: -999,999              99.99%   Sales Tax   -999,999.99
          Total Orders: -999,999
         Avail to Sell: -999,999                       Order Total -999,999.99
```

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LISTING 1: ENHANKB.ASM

```
CODE    segment
        assume  cs:CODE
        org     100h            ; COM file origin
ENTRY:  jmp     INIT            ; go to install TSR
OLDINT16_VEC dd ?               ; Save area for old INT 16h handler

INT16     proc    far
          assume  ds:nothing,es:nothing
          pushf                 ; Save flags
          sti                   ; Allow interrupts
          cmp     ah,01h        ; Check for functions 00h-01h
          ja      INT16_ORIG    ; Too big for us
          or      ah,10h        ; Convert to extended functions
INT16_ORIG:
          popf                  ; Restore flags
          jmp     OLDINT16_VEC  ; Continue on
INT16     endp                  ; End INT16 procedure

INIT    proc
        assume  ds:CODE
        mov     ax,3516h        ;get int 16h vector
        int     21h
        mov     word ptr OLDINT16_VEC,bx        ;save it
        mov     word ptr OLDINT16_VEC+2,es
        mov     ax,2516h        ;repoint it
        mov     dx,offset INT16
        int     21h
        mov     dx,offset INIT  ;point to end of code
        int     27h             ;bye now
INIT    endp
CODE    ends
        end     ENTRY
```

LISTING 2: ATKEY.ASM

```
COMMENT|                NOT EXECUTABLE!   EXAMPLE ONLY

                Module Specifications
Environment:  IBM PC/AT, tested under DOS 3.20.

Segments, groups, and classes:
  Group PGROUP:
    Program segment CODE,  byte-aligned, public, class 'prog'
    Data    segment DATA,  byte-aligned, public, class 'data'

Original code by:  Bob Smith, Qualitas, Inc., 8314 Thoreau Dr.,
March 1987         Bethesda, MD  20817-3164, 301-468-8848
|

@8255_A      equ  60h           ; Read-only in PC, Read/write in AT
@8042_ST     equ  64h           ; Status port
@CMD_CPAT    equ  40h           ; IBM PC Compatibility Mode switch
@OUTFULL     equ  01b           ; Output buffer full
@INPFULL     equ  10b           ; Input  buffer full
@S2C_RCMD    equ  020h          ; Read controller's command byte
@S2C_WCMD    equ  060h          ; Write controller's command byte
@S2C_DIS     equ  0ADh          ; Keyboard disable
@S2C_ENA     equ  0AEh          ; Keyboard enable
@S2C_RINP    equ  0C0h          ; Read  input  port
@S2K_ECHO    equ  0EEh          ; Echo
@S2K_SCAN    equ  0F0h          ; Select alternate scan codes
@S2K_RID     equ  0F2h          ; Read ID (two bytes returned)
@K2S_ECHO    equ  0EEh          ; Echo response
@K2S_ACK     equ  0FAh          ; Last command acknowledged
@K2S_RESEND  equ  0FEh          ; Resend last command

REGSAVE  macro   LIST           ; Register save macro
         irp     XX,<LIST>
         push    XX
         endm
         endm                   ; REGSAVE

REGREST  macro   LIST           ; Register restore macro
         irp     XX,<LIST>
         pop     XX
         endm
         endm                   ; REGREST

POPFF    macro
         local   L1,L2
         jmp     short L2
L1:     iret
L2:      push    cs
         call    L1
         endm                   ; POPFF

PGROUP   group   CODE,DATA
DATA     segment byte public 'data' ; Start DATA segment

         public  RID_LO,RID_HI,RCMD,RINP,RSCAN
RID_LO   db      ?              ; Low-order byte of Read ID byte
RID_HI   db      ?              ; High-order ...
RCMD     db      ?              ; Command byte
RINP     db      ?              ; Input port
RSCAN    db      ?              ; Read scan code set

         public  LCL_FLG
LCL_FLG  dw      0              ; Local flags
@LCL_RID_LO equ  8000h          ; Low-order Read ID byte
@LCL_RID_HI equ  4000h          ; High-order Read ID byte
@LCL_RCMD equ    2000h          ; Command byte
@LCL_RINP equ    0800h          ; Input port
@LCL_RSCAN equ   0020h          ; Read scan code set

DATA     ends                   ; End DATA segment

CODE     segment byte public 'prog' ; Start CODE segment
         assume  cs:PGROUP

GETRCMD  proc    near           ; Get Command Byte
         assume  ds:PGROUP,es:PGROUP

; Read the command byte

         REGSAVE <ax>           ; Save register
         cli                    ; Nobody move
         call    CLEAROBUF      ; Wait for the output buffer to clear
         mov     al,@S2C_RCMD   ; Read the controller's command byte
         call    SEND8042       ; Send to keyboard controller
         jc      ERR_RCMD       ; Something went wrong
         call    WAITRESP       ; Wait for a response, returned in AL
         jc      ERR_RCMD       ; Something went wrong
         mov     RCMD,al        ; Save response
         or      LCL_FLG,@LCL_RCMD ; Mark as present
ERR_RCMD:
         REGREST <ax>           ; Restore
         ret                    ; Return to caller
         assume  ds:nothing,es:nothing
GETRCMD  endp                   ; End GETRCMD procedure

GETRID   proc    near           ; Read Keyboard ID
         assume  ds:PGROUP,es:PGROUP

; Read keyboard ID.
; This value is returned in scan code format.  Thus to obtain the
; actual value we need to turn off the controller's scan code
;translation.

         REGSAVE <ax>           ; Save registers
         cli                    ; Nobody move
         call    TRANSOFF       ; Turn off scan code translation
         jc      ERR_RID2       ; Something went wrong
         mov     al,@S2K_RID    ; Function code to read ID
         call    SEND6805       ; Send to keyboard, response in AL
         jc      ERR_RID1       ; Jump if controller not responding
         cmp     al,@K2S_ACK    ; Izit an ACK?
         jne     ERR_RID1       ; Something went wrong
         call    WAITRESP       ; Wait for a response, returned in AL
         jc      ERR_RID1       ; Something went wrong
         mov     RID_LO,al      ; Save response
         or      LCL_FLG,@LCL_RID_LO ; Indicate we read it
         call    WAITRESP       ; Wait for a response, returned in AL
         jc      ERR_RID1       ; Something went wrong
         mov     RID_HI,al      ; Save response
         or      LCL_FLG,@LCL_RID_HI ; Mark as present
ERR_RID1:
         call    RESTCMD        ; Restore original command byte
```

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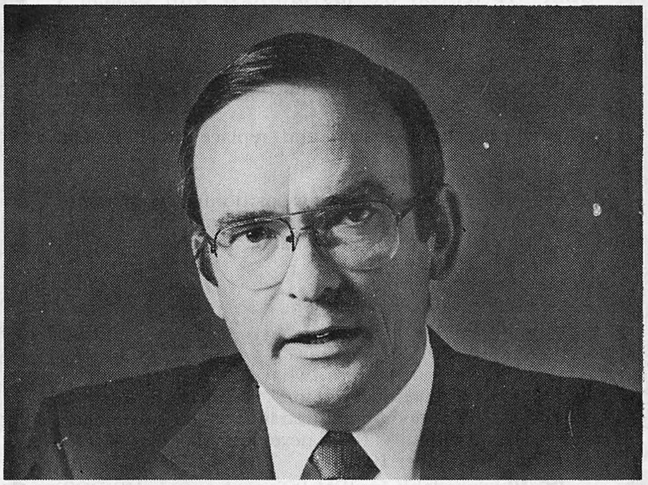

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```
ERR_RID2:
         REGREST <ax>           ; Restore
         ret                    ; Return to caller
         assume  ds:nothing,es:nothing

GETRID   endp                   ; End GETRID procedure

GETRINP  proc    near           ; Read Input Port
         assume  ds:PGROUP,es:PGROUP

;Read controller's input port.

         REGSAVE <ax>           ; Save registers
         cli                    ; Nobody move
         call    CLEAROBUF      ; Wait for the output buffer to clear
         mov     al,@S2C_RINP   ; Read controller's input port
         call    SEND8042       ; Send to keyboard controller
         jc      ERR_RINP       ; Something went wrong
         call    WAITRESP       ; Wait for a response, returned in AL
         jc      ERR_RINP       ; Something went wrong
         mov     RINP,al        ; Save response
         or      LCL_FLG,@LCL_RINP ; Mark as present
ERR_RINP:
         REGREST <ax>           ; Restore
         ret                    ; Return to caller
         assume  ds:nothing,es:nothing

GETRINP  endp                   ; End GETRINP procedure

GETRSCAN proc    near           ; Read Current Scan Code Set
         assume  ds:PGROUP,es:PGROUP

; Read current scan code set.
; This value is returned in scan code format.  Thus to obtain the
; actual value we need to turn off the controller's scan code
; translation.

         REGSAVE <ax>           ; Save registers
         cli                    ; Nobody move
         call    TRANSOFF       ; Turn off scan code translation
         jc      ERR_RSCAN2     ; Something went wrong
         mov     al,@S2K_SCAN   ; Select scan code set
         call    SEND6805       ; Send to keyboard, response in AL
         jc      ERR_RSCAN1     ; Jump if controller not responding
         cmp     al,@K2S_ACK    ; Izit an ACK?
         jne     ERR_RSCAN1     ; Something went wrong
         mov     al,0           ; Send it a request for current set
         call    SEND6805       ; Send to keyboard, response in AL
         jc      ERR_RSCAN1     ; Jump if controller not responding
         cmp     al,@K2S_ACK    ; Izit an ACK?
         jne     ERR_RSCAN1     ; Something went wrong
         call    WAITRESP       ; Wait for a response, returned in AL
         jc      ERR_RSCAN1     ; Something went wrong
         mov     RSCAN,al       ; Save response
         or      LCL_FLG,@LCL_RSCAN ; Indicate we read it
ERR_RSCAN1:
         call    RESTCMD        ; Restore original command byte
ERR_RSCAN2:
         REGREST <ax>           ; Restore
         ret                    ; Return to caller
         assume  ds:nothing,es:nothing

GETRSCAN endp                   ; End GETRSCAN procedure

TRANSOFF proc    near           ; Turn Off Scan Code Translation
         assume  ds:PGROUP,es:PGROUP
COMMENT|
Turn off scan code translation.
On exit:
CF       =       0 if all went well
         =       1 otherwise
|
         REGSAVE <ax>           ; Save register
         test    LCL_FLG,@LCL_RCMD ; Is RCMD valid?
         stc                    ; Assume not
         jz      TRANSOFF_EXIT  ; No
         mov     al,@S2C_WCMD   ; Write command byte
         call    SEND8042       ; Send to keyboard controller
         jc      TRANSOFF_EXIT  ; Something went wrong
         call    CLEARIBUF      ; Wait for input buffer to clear
         jc      TRANSOFF_EXIT  ; Error, controller not reading data
```

```
; Turn off scan code translation

        mov     al,RCMD         ; Get the original command byte
        and     al,not @CMD_CPAT ; Turn off compatibility mode
        out     @8255_A,al      ; Issue the command
TRANSOFF_EXIT:
        REGREST <ax>            ; Restore
        ret                     ; Return to caller
        assume  ds:nothing,es:nothing

TRANSOFF endp                   ; End TRANSOFF procedure

RESTCMD  proc   near            ; Restore Command Byte
        assume  ds:PGROUP,es:PGROUP
COMMENT|
Restore command byte from RCMD.
On exit:
CF      =       0 if all went well
        =       1 otherwise
|
        REGSAVE <ax>            ; Save registers
        mov     al,@S2C_WCMD    ; Write command byte
        call    SEND8042        ; Send to keyboard controller
        jc      RESTCMD_EXIT    ; Something went wrong
        call    CLEARIBUF       ; Wait for input buffer to clear
        jc      RESTCMD_EXIT    ; Error, controller not reading data
        mov     al,RCMD         ; Get the original command byte
        out     @8255_A,al      ; Issue the command
RESTCMD_EXIT:
        REGREST <ax>            ; Restore
        ret                     ; Return to caller
        assume  ds:nothing,es:nothing

RESTCMD  endp                   ; End RESTCMD procedure

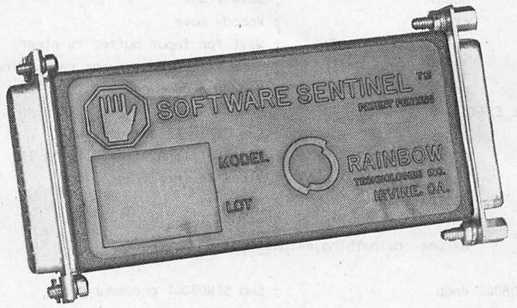
WAITRESP proc   near            ; Wait For A Response
        assume  ds:PGROUP,es:PGROUP
COMMENT|
Wait a response from the keyboard or its controller.
On exit:
CF      =       1 if no response
        =       0 otherwise
AL      =       response if CF=0
AH      =       clobbered
|
        REGSAVE <bx,cx>         ; Save registers
        clc                     ; Assume all goes well
        lahf                    ; Load AH with flags
        pushf                   ; Save flags
        cli                     ; Nobody move

; Wait for a response

        mov     bl,12           ; Outer loop counter
        xor     cx,cx           ; Inner loop counter
RESP1:
        in      al,@8042_ST     ; Get status from keyboard
        and     al,@OUTFULL     ; Check Output Buffer Full flag
        loopz   RESP1           ; Jump if no response as yet
        jz      RESP2           ; Still no response
        jmp     $+2             ; Take into account I/O delay
        in      al,@8255_A      ; Read in the code
        jmp     short RESP_EXIT ; Join common exit code
RESP2:
        dec     bl              ; Try again
        jnz     RESP1           ; Jump if more tries available
        inc     ah              ; Set CF in AH
RESP_EXIT:
        POPFF                   ; Restore flags with caller's IF
        sahf                    ; Store AH into flags
        REGREST <cx,bx>         ; Restore
        ret                     ; Return to caller
        assume  ds:nothing,es:nothing

WAITRESP endp                   ; End WAITRESP procedure

SEND8042 proc   near            ; Send Command To Keyboard Controller
        assume  ds:PGROUP,es:PGROUP
COMMENT|
Send the command in AL to the keyboard controller port 64h.
```



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CIRCLE NO. 157 ON READER SERVICE CARD

```
There is no acknowledgement of this command.
On exit:
CF        =         1 if keyboard controller not responding
          =         0 otherwise
|
          REGSAVE <ax>              ; Save for a moment
          clc                       ; Assume all goes well
          lahf                      ; Load AH with flags
          pushf                     ; Save flags
          cli                       ; Nobody move
          call    CLEARIBUF         ; Wait for input buffer to clear
          jc      CTRL_EXIT         ; Jump if controller not responding
          out     @8042_ST,al       ; Send the command
CTRL_EXIT:
          adc     ah,0              ; Set CF in AH as necessary
          POPFF                     ; Restore flags with caller's IF
          sahf                      ; Store AH into flags
          REGREST <ax>              ; Restore
          ret                       ; Return to caller
          assume  ds:nothing,es:nothing

SEND8042 endp                       ; End SEND8042 procedure

SEND6805 proc      near             ; Send Data in AL to Keyboard
          assume  ds:PGROUP,es:PGROUP
COMMENT|
Send AL to keyboard.
On exit:
CF        =         1 if timeout
          =         0 otherwise
AL        =         keyboard response if CF=0
AH is clobbered.
|
          REGSAVE <cx>              ; Save for a moment
          mov     cx,6              ; # retries of resend
          clc                       ; Assume all goes well
          lahf                      ; Load AH with flags
          pushf                     ; Save flags
```

```
          cli                       ; Nobody move
SEND0:
          REGSAVE <ax>              ; Save for a moment
          call    CLEARIBUF         ; Wait for input buffer to clear
          jc      SEND1             ; Error, controller not reading data
          out     @8255_A,al        ; Issue the command
          call    WAITRESP          ; Wait for a response, returned in AL
          jc      SEND1             ; Something went wrong
          cmp     al,@K2S_RESEND    ; Izit a resend?
          clc                       ; In case it isn't
          jne     SEND1             ; No
          REGREST <ax>              ; Restore
          loop    SEND0             ; Jump if more retries
          stc                       ; Indicate something went wrong
          push    ax                ; Save for a moment
SEND1:
          inc     sp                ; Restore stack pointer
          inc     sp                ; ...without changing CF
          adc     ah,0              ; Set CF in AH as necessary
          POPFF                     ; Restore flags with caller's IF
          sahf                      ; Store AH into flags
          REGREST <cx>              ; Restore
          ret                       ; Return to caller
          assume  ds:nothing,es:nothing

SEND6805 endp                       ; End SEND6805 procedure

CLEARIBUF proc    near              ; Wait For The Input Buffer To Clear
          assume  ds:PGROUP,es:PGROUP
COMMENT|
Wait for the one-byte input buffer to clear.
On exit:
CF        =         0 if buffer empty
          =         1 otherwise
|
          REGSAVE <ax,cx>           ; Save registers
          clc                       ; Assume all goes well
          lahf                      ; Load AH with flags
          pushf                     ; Save flags
          cli                       ; Nobody move
          xor     cx,cx             ; Loop counter
CLEARIBUF1:
          in      al,@8042_ST       ; Get status from keyboard
          and     al,@INPFULL       ; Check Input Buffer Full flag
          loopnz  CLEARIBUF1        ; Last char not read as yet
          jz      CLEARIBUF_EXIT    ; Jump if buffer clear before then
          stc                       ; Mark as in error
CLEARIBUF_EXIT:

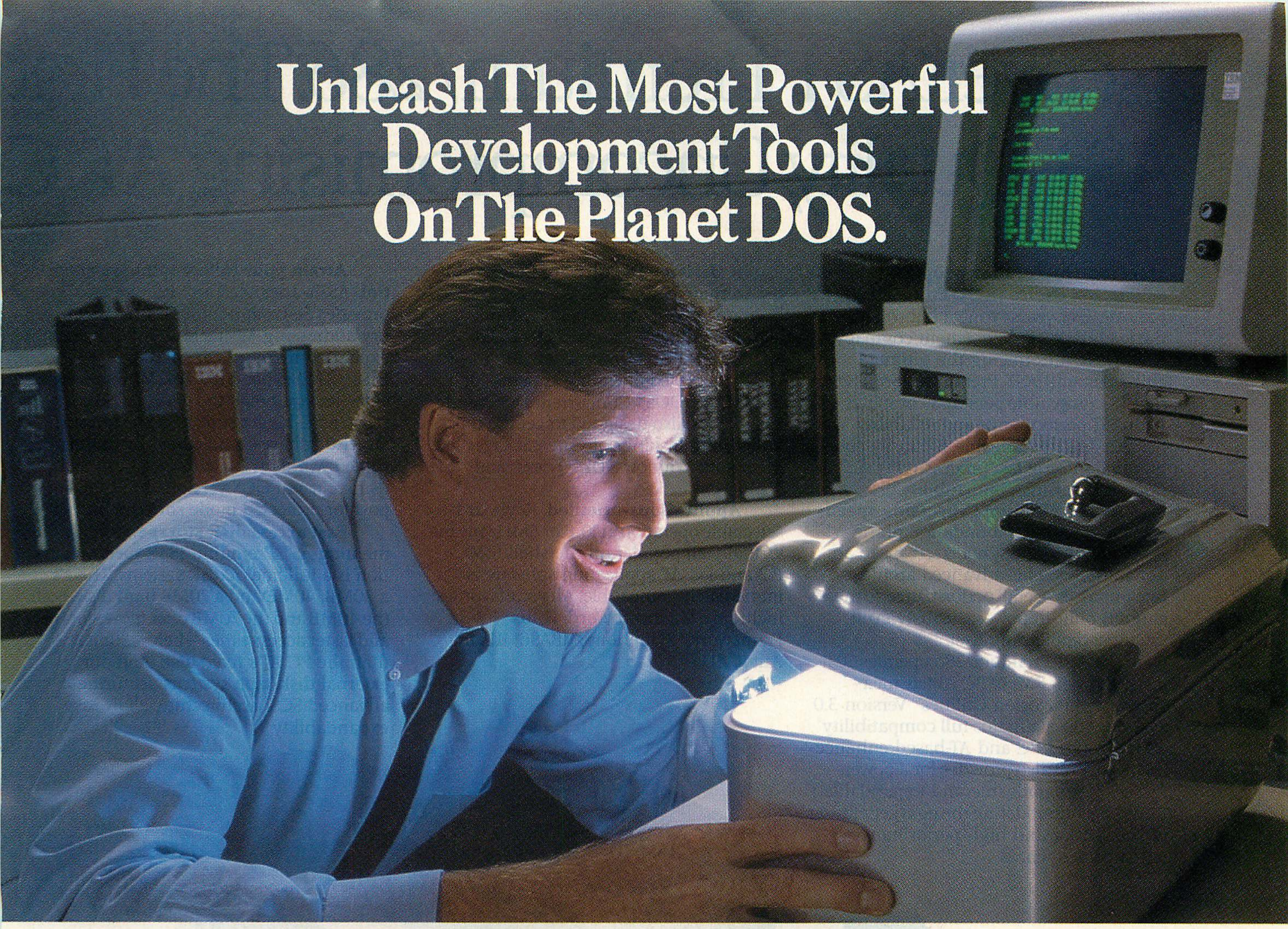
          adc     ah,0              ; Set CF in AH as necessary
          POPFF                     ; Restore flags with caller's IF
          sahf                      ; Store AH into flags
          REGREST <cx,ax>           ; Restore
          ret                       ; Return to caller
          assume  ds:nothing,es:nothing

CLEARIBUF endp                      ; End CLEARIBUF procedure

CLEAROBUF proc    near              ; Wait For The Output Buffer To Clear
          assume  ds:PGROUP,es:PGROUP

; Wait for the one-byte input buffer to clear.
          REGSAVE <ax>              ; Save register
          cli                       ; Nobody move
CLEAROBUF1:
          in      al,@8042_ST       ; Get status from keyboard
          and     al,@OUTFULL       ; Check Output Buffer Full flag
          jz      CLEAROBUF_EXIT    ; Jump if buffer clear before
          jmp     $+2               ; I/O delay
          in      al,@8255_A        ; Purge the character
          jmp     CLEAROBUF1        ; Continue on
CLEAROBUF_EXIT:
          REGREST <ax>              ; Restore
          ret                       ; Return to caller
          assume  ds:nothing,es:nothing

CLEAROBUF endp                      ; End CLEAROBUF procedure
CODE      ends                      ; End CODE segment
          end                       ; End LIST1 module
```



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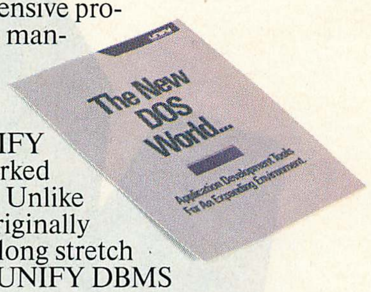

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Irvine, CA 92714-4992 Attn: M.C. PCTJ 7/87
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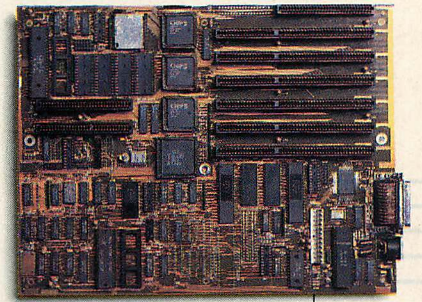
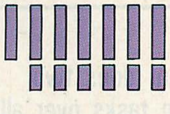
AST RESEARCH INC.

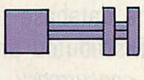


Seven industry-standard expansion slots; 1 PC-compatible slot, 6 PC AT-compatible slots, including two AST FASTslots. FASTslots provide no wait state operation with a high-speed direct interface to the 10MHz 80286 processor. Advanced architecture accommodates the next generation of accelerator and high-performance enhancement cards. It's also an open architecture for easy development and system integration.

Based on industry-standard native 80286 technology, complemented by AST advanced architecture.

Coprocessor socket accepts 8MHz 80287 devices to execute math- and floating point-intensive programs faster.

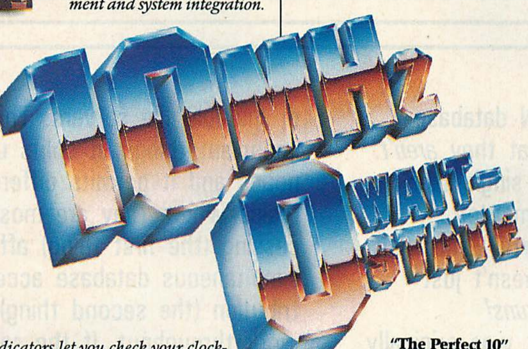




Two AT-compatible expansion slots with a plus: a third bus connector featuring lightning-quick CPU access time, for use with specially-designed cards like the AST FASTRAM Enhanced memory card. Expandable to 2MB in single slot, FASTRAM supports a variety of addressing capabilities—Enhanced EMS, EMS, extended (protected mode) and conventional memory addressing.

Enhanced, low-profile 101/102-key keyboard with separate numeric keypad, dedicated cursor control and extra function keys. International versions available.

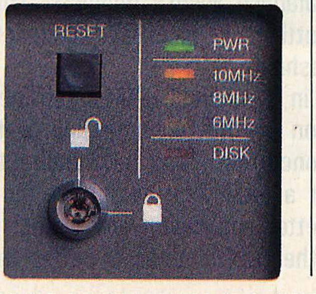
AST Premium/286 is shipped with MS-DOS and GW BASIC,® and it's fully compatible with a wide variety of operating systems, operating environment and utility packages, and application software.

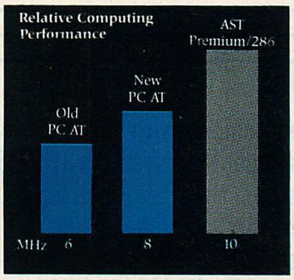


"The Perfect 10"

10MHz, 0 wait-state operation, faster than the 8MHz PC AT, with IBM PC AT hardware and software compatibility.

Indicators let you check your clock-speed—user-selectable at 10, 8 or 6MHz. Reset button allows easy cold-booting. Security lock prevents unauthorized keyboard access.





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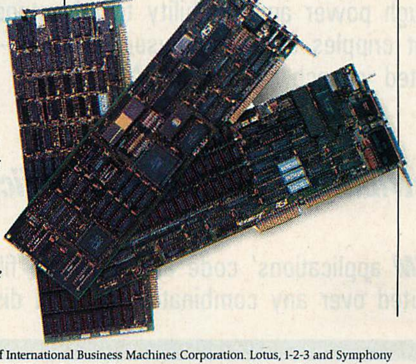
Supports standard PC, PC AT and AST FASTslot cards. With AST, you start with a lot, like our included FASTRAM Enhanced memory card and multimode Enhanced Graphics Adapter, but you've also got a lot of options. We offer the widest range of compatible enhancement products and peripherals to suit your needs—a true one-stop solution allowing you to expand and upgrade your system with the assurance of future service and support.



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ZIM

BORN TO RUN (ON NOVELL NETWORKS)

The problem with most multi-user LAN database management systems (DBMSes) is that they *aren't*. Rather, they are lame adaptations of single-user versions or sluggish ports of mini-computer DBMSes. ***ZIM***®, the *natural* multi-user Fourth Generation Language (4GL)/DBMS, is different; ***ZIM*** doesn't just more-or-less *work* on Novell networks, it *runs!*

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ZIM's "Four Ps"

On a global product level, ***ZIM***'s strengths may be encapsulated by "the four Ps": productivity, portability, power and performance.

1 ***Productivity*** ***ZIM*** incorporates the Entity-Relationship model of database design, a graphically-oriented data model that eclipses traditional Relational models because it recognizes relationships *between* tables of data as well as those within. ***ZIM***'s user-defined relationships permit the implementation of many-to-many relationships, outer joins and relationship consistency with an ease not found in any other product.

ZIM is also a true 4GL that integrates all necessary facilities (forms, data dictionary, update, query, report writer, debugging) into one package using common concepts. ***ZIM***'s code efficiency, combined with its 4GL conciseness, make it a system that will not only significantly reduce your development time, but maintenance programming as well.

ZIM/DA™, the ***ZIM*** Development Assistant, permits remarkably fast transition from prototype to finished product; ***ZIM/DA*** comprises an application generator, menu generator, interactive data dictionary, context-sensitive help and an on-line training module.

2 ***Portability*** Tools and applications written in any version of ***ZIM*** are uniquely 100 percent portable to and from any other supported environment (single- and multi-user MS-DOS®, Novell networks, QNX®, XENIX®, UNIX™, VMS®, VM/CMS®).

3 ***Power*** ***ZIM*** is a language rich in powerful features and functions:

- AI-based access strategy analyzer
- Unsurpassed computational abilities, including case expression, which handles with ease the "step" function found in real-world business applications
- Complete code-data independence
- Active data dictionary
- Exceptional text-handling capabilities
- Unlimited forms manipulation and report-writing capabilities
- Multi-lingual applications (French, German, etc.)

4 ***Performance*** ***ZIM*** was designed to be an optimally-performing development platform in each supported environment. As a result, it is an exceptionally speedy, compact system, even on a large network. In comparison to other 4GLs, the fact that ***ZIM***'s memory use is *less than* half by comparison permits faster performance and up to *three times as many users* on the same system.

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There is also a fifth "P", price. ***ZIM*** delivers exceptional value on Novell networks, starting at $1495 (U.S.) for a 1-4 node version and up to $4995 for 17-32 nodes.

ZIM™

CIRCLE NO. 236 ON READER SERVICE CARD

Patterning CD-ROM

CD-ROM technology signals a quantum leap in information dispersement: a new publishing medium has been born. Key to its widespread use is a workable standard, now close to approval.

PETER JANSSON

PHOTOGRAPH • WALTER LARRIMORE/BLAKESLEE-LANE

A sophisticated technology first made popular in the audio world promises to revolutionize the manner in which information is dispersed. Just as personal computers brought the power of computing to virtually every desktop, the tremendous capacity of CD-ROM (compact-disk read-only memory) cannot help but impact the PC world. A single CD-ROM disk will hold the contents of an entire bookshelf—more than half a gigabyte of data (500MB)—or the equivalent of about 1,500 5¼-inch diskettes.

The key to success for CD-ROM is widespread use. Producing disks and read-out devices for this technology is as yet an expensive proposition. It has become economically viable for the microcomputer market only because it can share technology with the broad-based consumer audio CD. Even so, producing data on CD-ROM entails an expensive mastering step that limits it to applications with broad appeal.

CD-ROM is not just another storage device: it is a full-fledged publishing medium that cannot succeed if it is limited to a few classes of hardware. A universal standard is needed to make the information on a CD-ROM as recognizable to a computer as the printed word is to a human reader. It must be readable to anyone with a CD-ROM drive and a computer, regardless of the brand of equipment or software.

Such a standard for data recording must be applied on three levels. The physical level defines the medium's dimensions and properties, the characteristics of recording and playback equipment, and the methods to encode and record data. The logical-format level specifies the organization of data into structures such as volumes, directories, and files. The applications level defines and interprets recorded data.

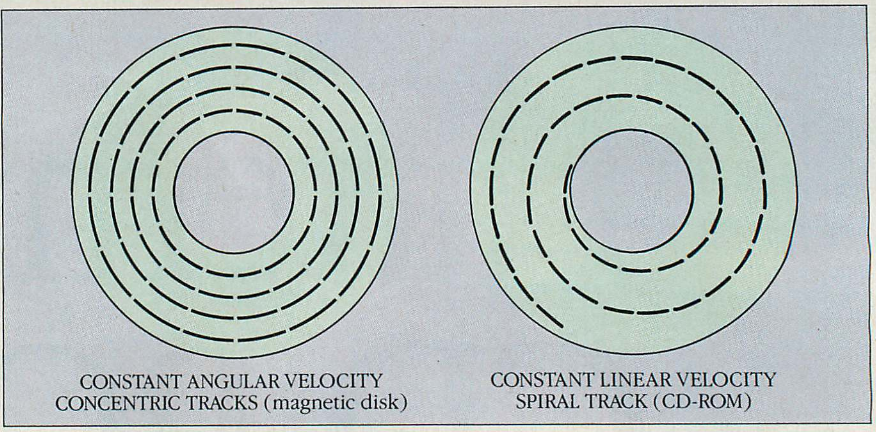
The physical level has been addressed by the owners of the technology, Phillips of the Netherlands and Sony of Japan. These companies defined the specifications for optically recording digital audio in a document popularly known as the *Red Book*. Using the same technology, the two firms extended the specifications to CD-ROM data recording in the *Yellow Book*.

Taking the idea one step further in recognizing that this purely physical standard is insufficient for publishing optically recorded information, the following group of companies has proposed a standard for the logical organization of data on a CD-ROM: Apple Computer, Inc., Digital Equipment Corporation, Hitachi, Microware Systems Corporation, Microsoft Corporation, Phillips, Reference Technology, Sony, 3M, TMS, Videotools, Xebec, and Yelick, Inc. Meeting in Lake Tahoe in May 1985, the group developed a file structure that has become known as the High Sierra Group (HSG) proposal; its formal title is the "Working Paper for Information Processing: Volume and File Structure of Compact Read-Only Optical Disks for Information Interchange."

The physical standards for the CD-ROM are controlled by patents held by Phillips and Sony; thus, the HSG has no power to enforce its proposal. However, attempts are currently under way to have the proposal approved as a voluntary standard through the International Standards Organization (ISO). The proposal has been submitted to the ISO by several national groups, including the European Computer Manufacturer's Association (ECMA) and the National Information Standards Organization (NISO) of the National Bureau of Standards. The document's approval as an international standard is expected to be complete by the end of 1987.

Left unaddressed at this point is the applications level of standardization. The HSG proposal specifies only how data are organized into files, not what files contain. For example, HSG specifies ASCII for encoding file names within directories, but does not specify how to encode data within those files.

FIGURE 1: *CLV Spiral versus CAV Concentric Organization*



At constant angular velocity (CAV), all sectors on a disk subtend the same angle, while at constant linear velocity (CLV), all sectors are the same length.

PHYSICAL DISK ORGANIZATION

The *Yellow Book* specifies that data on a CD-ROM be divided into physical sectors of 2,352 bytes each: 304 bytes for drive-mechanism synchronization, sector addressing, and error correction and detection, and the remaining 2,048 bytes for user data.

The physical layout of information on a CD-ROM is fundamentally different from the corresponding layout of a magnetic disk. In CD-ROM, sectors are arranged in one continuous spiral similar to the grooves of a phonograph record; in magnetic disks, they are arranged in concentric circular tracks. In CD-ROM, data are read at constant-linear velocity (CLV), in magnetic disks at constant-angular velocity (CAV). With CLV, each sector of data at any point on a disk has the same length; with CAV, each sector subtends the same angle (see figure 1). The rotation speed of a CLV disk varies in inverse proportion to the radius at which data are being read, whereas with CAV, the disk spins at a constant rate of speed.

Although variable speed requires a more complex drive mechanism, CLV provides for a maximum information-carrying capacity at every point on the recording surface. The simpler, constant-rotation speed of CAV allows maximum recording density only on the inner tracks; outer tracks typically use only about half the capacity.

CD-ROM's use of CLV and its spiral organization are separate design decisions—neither implies the other: a phonograph record spinning at a constant rate uses spiral organization with CAV, but a variable-speed magnetic-disk drive uses concentric organization with CLV. The combination of CLV and spiral organization was chosen for CD-ROM because it is optimal for CD audio, and by using CD audio components, CD-ROM can take advantage of mass-production economics.

Although spiral organization is ideal for CD audio because it is the most efficient method for reading sequential data in realtime, it is not the best arrangement for random-access retrieval. Finding a particular sector on one long track is more difficult than finding a concentric track at a fixed radius and searching through a small number of sectors on that track.

To search for data on a CD-ROM, the head moves to the general area of the sector being sought, then synchronizes with the spiral and follows the spiral until it reaches the correct sector. To maintain the constant velocity of sectors past the head, the drive's rotation must speed up or slow down as the head moves radially across the disk. This results in a slower access time: access to CD-ROM data takes between one-half and one full second. By comparison, access to data on a PC/AT hard disk takes less than 1/25th of a second (40 milliseconds).

As with the audio CD, sectors on a CD-ROM are identified by playing time (minute and second) and by sector number. Sectors are read at the rate of 75 per second, which results in an effective transfer rate of 150KB per second. With a nominal "playing time" of one hour, a CD-ROM contains 60 * 60 * 75, or 270,000 sectors. Thus, at 2KB per sector, total capacity equals 540MB. According to the *Yellow Book*, 00:02:00 is the first sector that can contain user data.

LOGICAL FORMAT

Although the logical format proposed by HSG is (necessarily) based on the underlying physical organization of CD-ROM, it does not depend on the size or spatial layout of physical sectors. Its aims are to optimize file formats on a medium where data layout is predetermined and invariant; to compensate for the slow seek times of the physical device; and, to facilitate CD-ROM's implementation on a variety of popular operating systems, specifically MS/PC-DOS, UNIX, VMS, and Apple DOS.

Space on a CD-ROM is mapped in units called *logical sectors*—the length of each is identical to the length of user data recorded on each physical sector. A logical sector is divided into *logical* *blocks*. Block length varies with the application, but it must be a power of two and at least 512 bytes.

Logical blocks are numbered consecutively on the disk, beginning with zero for the first block in the first sector. To avoid dependence on the physical specification, the HSG proposal avoids references to physical-sector numbering or to the number of sectors reserved before the data area. As the specification now stands, the mapping between a logical block number (LBN) and a physical sector is as follows:

$$\mathbf{LBN = (minute * 60 * 75 + second * 75 + sector - 150) * blocks\ per\ sector}$$

All data locations are specified in terms of LBNs, which are recorded as 32-bit integers, permitting a maximum 4.3 billion blocks. With the current sector size, the data capacity is almost 9 terabytes (9 trillion bytes) per disk.

The HSG proposal organizes these numbered logical blocks into named files. To this end, it defines two kinds of structures. One describes the volume—the data space of the entire disk (or set of disks); the other describes and locates files within that space. The HSG proposal also specifies how to encode the information that describes these structures. The proposed character set is a subset of ASCII. Because the HSG proposal defines a standard at the logical, not the applications, level, it specifies only the characters to be used for recording the volume and file structures; that is, the characters in the headers and directories. It places no restrictions on the characters that are used to record data within the files. It also specifies that directories and other organizational information can be recorded in alternate character sets in order to support specific applications or languages other than English.

Numeric quantities in the directories are recorded as binary integers of various lengths. In most computers, quantities occupying more than one byte can be recorded in order of least significant byte (LSB) or most significant byte (MSB). For example, the number 1234H (4,660 decimal) can be recorded as either 12H 34H or 34H 12H. Most microprocessors, including the Intel line, use MSB ordering; most mainframes use LSB. Instead of choosing between the two, the HSG proposal specifies that all multibyte quantities be recorded in both orders: LSB, then MSB. Thus, 1234H would be recorded in four bytes: 34H 12H 12H 34H.

Under this encoding scheme, a processor is not forced to switch bytes in order to convert numbers into its native format. Although the processing time is saved at the expense of storage space, this is a decidedly good trade-off considering the aforementioned capacity of a CD-ROM. In some systems, multibyte quantities must be located on certain boundaries; or at least, they are more efficiently retrieved from certain memory locations than others. The HSG proposal ensures that all word and double-word numbers are properly aligned by specifying zero-filled padding bytes as it becomes necessary.

VOLUME STRUCTURE

The portion of a CD-ROM that is available for recording data is its *volume space*, which is divided into a *system area*, in the first 16 sectors, and a *data area* in all remaining sectors. The HSG proposal does not specify the structure and use of the system area. Although the HSG format is intended for a variety of operating systems, it provides for only one system area. However, unstructured partitions in the data area can be used to provide information for more than one operating system.

TABLE 1: *File Structure Volume Descriptor*

BYTE POSITION	BYTE LENGTH	FORMAT	FIELD CONTENTS IN STANDARD AND CODED CHARACTER SET DESCRIPTORS
1	8	N	Volume descriptor logical block number (LBN)
9	1	N	Volume descriptor type
10	5	C	Volume structure standard identifier ("CDROM")
15	1	N	Volume structure standard version
16	1	N	Reserved/Volume flags
17	32	C	System identifier
49	32	C	Volume identifier
81	8	0	Reserved (used in unspecified structure descriptor)
89	8	N	Volume space size (logical blocks)
97	32	N	Reserved/Coded character set ID
129	4	N	Number of volumes in volume set
133	4	N	Sequence number within volume set
137	4	N	Logical block size (bytes)
141	8	N	Path table size (bytes)
149	4	N	Pointer to path table in LSB order
153	12	N	Three pointers to optional occurrences of path table
165	4	N	Pointer to path table in MSB order
169	12	N	Three pointers to optional occurrences of path table
181	34	*	Directory record for root directory
215	128	C	Volume set identifier
343	128	C	Publisher identifier
471	128	C	Data preparer identifier
599	128	C	Application identifier
727	32	C	Copyright file name
759	32	C	Abstract file name
791	16	D	Volume creation date and time
807	16	D	Volume modification date and time
823	16	D	Volume expiration date and time
839	16	D	Volume effective date and time
855	1	N	File structure standard version
856	1	0	Reserved (pad to word boundary)
857	512	U	Reserved for application use
1,369	680	0	Reserved for future standardization
Total	2,048		

N = Binary integer
0 = Binary zero
C = Character
D = Digit character 0–9
U = Unspecified
** = See table 3*

A CD-ROM must have one volume descriptor to define a standard file structure; it may have any number defining other structures coded in alternate character sets.

At the beginning of the data area is a sequence of fixed-length records called *volume descriptors* that describe the general layout of volume space. They comprise the only data structure in the HSG proposal with fixed-length records and an assigned location. The five types of volume descriptor include a standard-files-structure volume descriptor (SFSVD type 1), which describes volume space and points to the head of the standard-file structure; a coded-character-set-file-structure volume descriptor (type 2), which defines a standard-file structure for directories in an alternate character set; an unspecified-structure volume descriptor (type 3), which defines a partition having a format that does not conform to the HSG proposal; a boot record (type 0), which provides unstructured data within the descriptor itself; and, a volume-descriptor sequence terminator (type 255), which indicates the end of the sequence of volume descriptors.

Every set of volume descriptors must include one SFSVD type 1, and only one is allowed per CD-ROM. Although several duplicate descriptors may be present to ensure the integrity of directory data, they all must define the identical file structure. The last descriptor must be a sequence terminator; otherwise, any number of volume descriptors can occur in any order.

Boot records and type 3 unspecified-structure descriptors can be used to provide system-dependent information to more than one operating system. They can, for example, be used to supplement the system area at the start of the CD-ROM. The System ID field in these descriptors identifies the system that interprets the data. Unstructured partitions also can be used to record other file structures—for example, an image of a DOS disk.

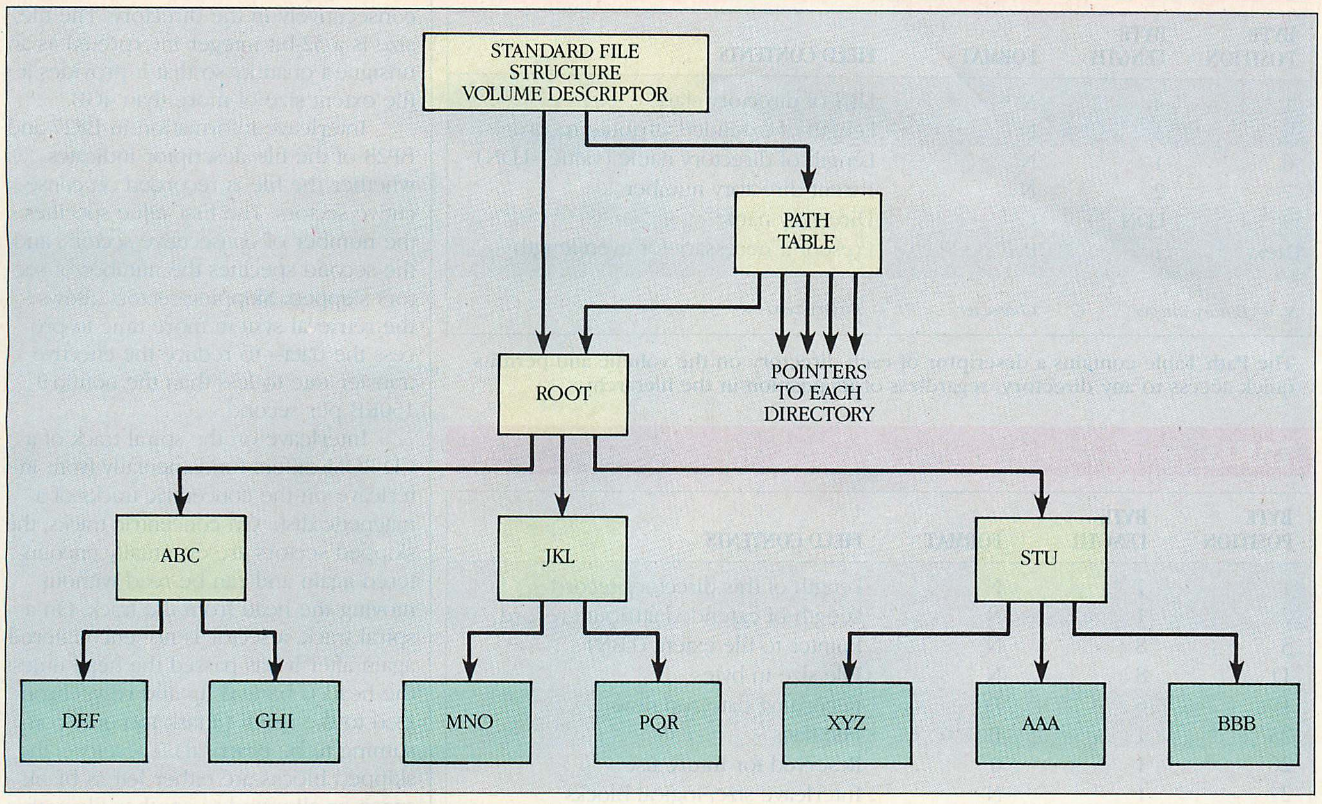
Each volume descriptor is 2,048 bytes long. HSG specifies the length in absolute terms, not in relation to logical-sector size. The information in the first 15 bytes is the same in all volume descriptors. See table 1 for layouts of the two most important descriptors, SFSVD type 1 and type 2, which define the variations of standard-file structure.

The volume descriptor's LBN (byte position 1) is the logical block number where the descriptor starts. It is a 32-bit number, recorded in both LSB and MSB order, that identifies the particular copy of the descriptor. If a descriptor is replicated for purposes of data integrity, the LBN is the only field that varies from copy to copy. The volume-descriptor type (BP 9) identifies the descriptor, such as type 1 or type 2. The Standard Identifier (BP 10) contains the characters CDROM to identify the standard to which the CD conforms, and the Standard Version (BP 15) identifies the particular version of the standard. Currently, all CD-ROMs conforming to the HSG proposal have the value 1 in the Standard Version field.

The remaining contents of a descriptor depend upon its type. SFSVD types 1 and 2 contain the following fields: Volume Flags (BP 16) and Coded Character Set ID (BP 97) identify the nonstandard character set used in a type 2 descriptor. In a type 1 descriptor, these fields are set to zero. System Identifier (BP 17) identifies the system using the system area.

Volume ID (BP 49) is informational. Its function is analogous to the DOS Volume ID. A retrieval system would use this field to ensure that the proper disk is mounted. Volume Space Size (BP 89) lists the total number of logical blocks in the volume space, including the system area and any unstructured data areas defined by type 3 descriptors. Volume Count and Volume Sequence (BP 129 and BP 133) define multivol-

FIGURE 2: *High Sierra Group CD-ROM Directory Structure*



This directory is similar to MS-DOS's, but the added Path Table allows locating any directory without traversing the entire path.

ume sets. Logical Block Size (BP 137) defines the length of the CD-ROM's basic allocation unit on the disk—currently 512, 1,024, or 2,048 bytes.

Several fields beginning at BP 141 describe the root directory and the Path Table; they point to the head of the standard-file structure. The fields at BP 343, 471, and 599 (128 bytes each) identify the publisher, data preparer, and application. File Structure Standard Version (BP 855), and the fields at BP 10 and 15, identify the standard to which the CD-ROM conforms; all of these fields are informational.

The fields at BP 727 and 759 identify files that contain copyright notices and abstracts of the information contained on the volume. These files, if present, reside in the CD-ROM's root directory. Four time stamps beginning at BP 791, encoded in ASCII, give the creation, modification, expiration, and effective date/times. Expiration and effective dates can be used to control time-sensitive information.

The ability to define directories in alternate-character sets supports files that are named in languages other than English. Type 2 file structures specify characters only for directories, not for encoding data in files. Although alternate and standard structures use different directories, the directories need not point to totally disconnected files. For example, each structure may point to its own text files recorded in a different language, but to a common set of files containing numeric data.

FILE STRUCTURE

The file structure defined by the HSG proposal is a tree-shaped, multilevel directory structure similar to DOS and UNIX except that it allows only eight levels of directories. Further, it does not fix the location of the root directory; instead, the SFSVD points to it.

The slow CD-ROM seek time makes a deeply nested tree structure inefficient. Opening a file listed in a subdirectory three levels below the root might require three or four separate seeks just to obtain the file's location, plus another to open the file. To speed access, the HSG file structure defines a Path Table that lists the locations of all directories on the disk, at all levels. Each directory (including the root directory) can be accessed through either of two paths: one directly through the Path Table, another along the pointers from the root through the branches of the tree (see figure 2).

The Path Table contains a directory descriptor for each directory on the disk (see table 2). A directory name can have up to 31 characters, including uppercase letters, digits, and underscores. No punctuation characters are allowed because various operating systems assign different meanings to them.

Directories are assigned numbers by their position in the Path Table, and are ordered in the table by directory level (root first), by parent directory number, and alphabetically within the parent directory. In the sample structure shown in figure 2, the order of entries in the Path Table is as follows:

1 Root Level 0
2 ABC Level 1
3 JKL
4 STU
5 DEF Level 2
6 GHI
7 MNO
8 PQR
9 AAA
10 BBB
11 XYZ

Because of this hierarchical ordering and the variable length of the entries, the Path Table can be searched only sequentially. Efficient look-up algorithms, such as binary search, cannot be used.

Each CD-ROM must have at least two copies of the Path Table. One copy

TABLE 2: *Directory Descriptor (Path Table Record)*

BYTE POSITION	BYTE LENGTH	FORMAT	FIELD CONTENTS
1	4	N	LBN of directory start
5	1	N	Length of extended attribute record
6	1	N	Length of directory name (value=LDN)
7	2	N	Parent directory number
9	LDN	C	Directory name
Next	1	0	Present if necessary for even length

N = Binary integer *C = Character* *0 = Binary zero*

The Path Table contains a descriptor of each directory on the volume and permits quick access to any directory, regardless of its position in the hierarchy.

TABLE 3: *File Descriptor (Directory Record)*

BYTE POSITION	BYTE LENGTH	FORMAT	FIELD CONTENTS
1	1	N	Length of this directory record
2	1	N	Length of extended attribute record
3	8	N	Pointer to file extent (LBN)
11	8	N	File size in bytes
19	6	D	Recording date and time
25	1	B	File flags
26	1	0	Reserved for future use
27	1	N	Interleave size, logical blocks
28	1	N	Interleave skip factor, logical blocks
29	4	N	Volume set sequence number
33	1	N	Length of file name (value = LFN)
34	LFN	C	File identifier
34+LFN	1	0	Reserved (present only if LFN is odd)
Next	Rest	U	Reserved for system use (optional)

N = Binary integer
0 = Binary zero
C = Character
D = Digit characters 0–9
B = Bit flags
U = Unspecified

Similar to MS-DOS, a directory may contain entries identifying both files and other directories, but unlike MS-DOS, the entries are variable-length.

has multibyte numeric values (LBN of the directory, number of its parent) recorded in LSB order, the other in MSB order. The entire table—not just each numeric value—is repeated to save space when the table is read into memory. The Path Table is meant to reside in memory so that directories can be found quickly with minimum accesses to the CD-ROM. Recording the number twice would add six bytes to each entry; instead, extra space for the table is allocated on CD-ROM, where high capacity produces a low per-byte cost.

Each mandatory copy of the Path Table can be replicated three times for data integrity. All copies must define the identical directory structure, but need not point to the same directory files.

The directories contain records called *file descriptors* that point to file locations in the data space (see table 3). Within a directory, each file descriptor is arranged alphabetically by a *file identifier* that contains up to three components: a file name, followed by a period; a file extension, followed by a semicolon; and a file version number. The name and extension can contain uppercase letters, digits, and underscores; the optional version number is made up of digit characters representing a number between 1 and 32,767. Either the name or extension (but not both) may be omitted. If the name is omitted, the identifier begins with a period. The file-identifier string is also limited to 31 characters.

Files with multiple extents (for spanning more than one disk volume) have one directory entry for each file extent. Because all of the entries for a multiextent file contain the same file identifier, these entries are grouped consecutively in the directory. The file size is a 32-bit integer interpreted as an unsigned quantity so that it provides a file extent size of more than 4GB.

Interleave information in BP27 and BP28 of the file descriptor indicates whether the file is recorded on consecutive sectors. The first value specifies the number of consecutive sectors, and the second specifies the number of sectors skipped. Skipping sectors allows the retrieval system more time to process the data—to reduce the effective transfer rate to less than the nominal 150KB per second.

Interleave on the spiral track of a CD-ROM differs fundamentally from interleave on the concentric tracks of a magnetic disk. On concentric tracks, the skipped sectors are eventually encountered again and can be read without moving the head from the track. On a spiral track, a sector is not encountered again after it has passed the head unless the head is backed up and resynchronized to the spiral (a task too time-consuming to be practical). Therefore, the skipped blocks are either left as blank space or allocated to another file with a complementary interleave.

As in DOS, the first two entries in every subdirectory point to the directory itself and to its parent, but instead of using periods to identify them, the HSG proposal specifies 00H for the current-directory descriptor and 01H for the parent-directory descriptor. Unlike DOS, the root directory also includes these two pointers: because the root has no parent directory, its parent pointer points to itself.

The attribute byte proposed by HSG is also similar to DOS (see table 4). The *existence* attribute is analogous to the hidden attribute of DOS, and the *associated* attribute allows two different files to have the same name. The file with the associated attribute turned on is, in effect, a hidden file. The use of two files having the same name is system-dependent: for example, the main file could contain encrypted data and the associated file, the decryption keys.

The attribute byte has eight bits, many of which act as switches to enable other attributes to be specified in an extended-attribute record (EAR), see table 2. An EAR, if present, begins in the location specified by a file's LBN; the actual data begins immediately after the EAR. Existence of an EAR is indicated by a nonzero length value in the EAR field at BP 2 of the file descriptor. Directories can also have extended attributes.

TABLE 4: *File Attribute Byte*

BIT POSITION	NAME	MEANING IF SET
0	Existence	Existence of file need not be revealed upon user query
1	Directory	This directory record identifies a subdirectory, not a file
2	Associated	The file is associated in a system-dependent manner with another file of the same name
3	Record	The record structure specified in the extended attribute record for this file does apply
4	Protection	The protection modes specified in the extended attribute record are enabled
5–6	Reserved	Must be zero
7	Multiextent	This is not the final (or only) extent for this file

Bit 0 = Least significant bit

The function of the CD-ROM file attribute byte is similar to that in MS-DOS. To allow specifying more attributes than can fit in one byte, some of the flags enable extended attributes to be recorded elsewhere on the volume.

TABLE 5: *Extended Attribute Record*

BYTE POSITION	BYTE LENGTH	FORMAT	FIELD CONTENTS
1	4	N	Owner identification code
5	4	N	Group identification code
9	2	B	Permissions (see table 6)
11	16	D	File creation date and time
27	16	D	File modification date and time
43	16	D	File expiration date and time
59	16	D	File effective date and time
75	1	N	Record format
76	1	N	Record attributes
77	4	N	Record length
81	32	C	System identifier
113	64	U	Reserved for system use
177	1	N	Standard version
178	64	0	Reserved for future standardization
243	4	N	Parent directory number
247	4	N	Length of applications area (value=LAA)
251	LDR	*	Directory record for this file
Next	LAA	U	Applications area

LDR = Length of directory record, in first byte of directory record
N = Binary integer
0 = Binary zero
B = Bit flags
C = Character
D = Digit characters 0–9
U = Unspecified
** = See table 3*

This optional area precedes the data space of a file. It records the additional file attributes that are enabled by flags set in the file attribute byte.

One purpose of an EAR is to specify who may access the file. As in UNIX, permissions are specified for four classes of users: the system, the owner, members of the owner's group, and all other users, sometimes called "the world." (See table 6 for a list of permission flags.) The permissions specified in the HSG proposal are highly system-dependent—a CD-ROM is protected by permission flags only if the operating system or the application offer such protection. MS-DOS does not; under MS-DOS, a disk can be protected only by its applications software.

The EAR also can specify the record format of a file as fixed length, variable length, or unstructured. BP 77 of the EAR specifies the length for fixed-length records and the maximum length for variable-length records. A variable-length record is preceded by a 16-bit integer that specifies its length; the EAR's Record Format field (BP 75)

TABLE 6: *File Permission Flags*

BIT POSITION	WHEN CLEAR	WHEN SET
0 (LSB)	System may read	System may not read
1		Reserved: must be set
2	System may execute	System may not execute
3		Reserved: must be set
4	Owner may read	Owner may not read
5		Reserved: must be set
6	Owner may execute	Owner may not execute
7		Reserved: must be set
8	Group member may read	Owning group member may read
9		Reserved: must be set
10	Group member may execute	Owning group member may execute
11		Reserved: must be set
12	Any user may read	Group member may read
13		Reserved: must be set
14	Any user may execute	Group member may execute
15		Reserved: must be set

The four levels of file protection offered (system, owner, group, and world) are similar to those available in UNIX, except that write protection is obviously not needed. This feature is available only if the operating system supports it.

TABLE 7: *Record Format and Record Attributes*

RECORD FORMAT ID	RECORD FORMAT
0	Does not conform to HSG format
1	Fixed-length records
2	Variable-length records, each preceded by a 16-bit integer length in LSB format
3	Variable-length records, length values in MSB format

RECORD ATTRIBUTE	FORMATTING CONTROL
0	Precede with LF, follow with CR
1	Formatting specified in first byte of each record, per ISO/FORTRAN conventions
2	Formatting specified within the record, to be interpreted by application

If specified in the extended attribute area, these characteristics define the structure of data records and how to display records on screen or on paper.

indicates whether this integer is written in LSB or MSB order (see table 7).

A copy of the entire file descriptor (directory entry) for the file is incorporated in the EAR. The EAR therefore provides in one place all the information about the file, including the attribute byte, pointer to its location on disk, file size, and pointer to the parent-directory entry in the Path Table.

MULTIVOLUME SETS

Multiple sets of CD-ROMs are used when the information to be recorded exceeds the capacity of one disk and when supplementing or replacing information on the original disk. Information defining a multivolume set is located in three fields of the SFSVD type 1 (see table 1): the volume-set identification (BP 215), the number of volumes in the set (BP 129), and the sequence number of each disk within the set (BP 133).

If all the volumes of a set are released together, the directory information on each volume describes the entire file structure on all disks of the set. Thus, the location of any file on any disk can be determined regardless of the identity of the disk mounted. The directory entry for a file contains both its disk number and a pointer to the file's starting location. The user may have to change disks before the file can be read, but no more than one disk change is ever necessary.

TABLE 8: *Example of Multivolume Set*

	VOLUME ID	VOLUME SET ID	VOLUME SET SIZE	VOLUME SET SEQUENCE
INITIAL SET				
Disk 1	DISK_A	MY_SET	2	1
Disk 2	DISK_B	MY_SET	2	2
UPDATE				
Disk 3	DISK_C	MY_SET	3	3

The determination of which disk in a set actually contains the valid directory is made by comparing the volume set size to the volume set sequence number.

Although the information on a CD-ROM cannot be altered, a multivolume set can be updated by releasing a new disk with a different directory structure. This updated disk then contains the only valid directory for the entire set: any files on earlier disks that do not appear in the updated directory cannot be accessed and are, in effect, deleted. If the updated directory contains pointers to new copies of files, these files appear to replace the previous files.

When using an updated set on a single-drive system, it might be necessary to change disks several times to read one file. In the example in table 8, the disk set called MY_SET initially consisted of two volumes, each containing a directory structure so that any file listing could be located using either disk. When a third disk is issued to update the set, only that disk contains a correct directory for the three-disk set. The directories on disks 1 and 2 are rendered obsolete and the system must be started with disk 3 mounted. When disk 3 is read, the system records that it is part of a three-volume set.

If a file is needed from disk 1 or 2, the system prompts the user to mount the appropriate disk. When the disk is read, the system records the fact that its directory is obsolete because its volume count is less than the current set size. When the user is finished with the file on disk 2 and wants to access another, the system must prompt for disk 3 so as to access the current version of the directory. Once it has located the next file, it may need to prompt for disk 1 or 2 again. The developer of a CD-ROM application that may be updated should try to minimize this disk swapping by a careful lay-out of files and by maintaining appropriate portions of the directory structure in memory.

LEVELS OF INTERCHANGE

The HSG proposal defines three possible levels of implementation or *levels of interchange* of the disk format. The purpose is to accommodate the widest variety of operating systems. Not all of them can support all features described in the proposal, but instead of allowing each implementing party to choose which features to support, the proposal defines several acceptable subsets.

In level 1, directory and file names are limited to eight characters and file extensions are limited to three. Level 1 does not support file-version numbers, multiextent files, multivolume sets, hidden and associated files, interleaving, or protection. Level 2 supports interleaving, and file and directory identifiers up to 31 characters long, but still does not allow file-version numbers. Level 3 is the full implementation.

A system can read equal or lower-level CD-ROMs, but may produce errors when reading disks prepared to a higher level. In the HSG proposal, a retrieval system cannot determine the interchange level of a particular disk. The proposal also does not specify how a system implemented at one level should react to information recorded at a higher level. These issues are being addressed by the standards committees currently studying the proposal.

MS-DOS EXTENSIONS

One of the first implementations of the HSG proposal on a popular operating system is Microsoft's CD-ROM extensions for MS-DOS. These extensions, available only to OEM CD-ROM drive manufacturers, consist of two components: first, specifications for a device driver that controls the physical device, and, second, a terminate-and-stay-resident (TSR) program called MSCDEX that interfaces between MS-DOS and the device driver. The end user obtains the device driver and the program from the CD-ROM drive manufacturer.

To incorporate a CD-ROM drive into a PC configuration, the user must add a DEVICE statement to CONFIG.SYS specifying the CD-ROM device driver file and the number of physical drives it supports. He then must run MSCDEX from the DOS prompt or a batch file.

The device driver is defined as a character, not a block, device; because DOS block devices are restricted to file sizes of 32MB—far from adequate considering the capacity of a CD-ROM. Therefore, the CD-ROM drive cannot be treated as an ordinary disk drive accessed by a block-device driver.

When the MSCDEX program is installed, it assigns the next available drive letter to the CD-ROM using the DOS Redirection facility available in MS-DOS versions 3.1 and later. The LASTDRIVE parameter might need to be set in CONFIG.SYS to assure that sufficient drive letters are available.

An installation option specifies the number of sector buffers allocated by MSCDEX: the more buffers, the less frequently the CD-ROM must be accessed. This parameter is analogous to the BUFFERS command in CONFIG.SYS. Sector buffers also can be allocated in expanded memory (EMS), if available.

The interface between MSCDEX and EMS memory has two problems. First, if the read of the CD-ROM drive fails (because of an open drive door, for example) and the user answers "Abort" to the DOS error message, the EMS memory becomes unusable and the CD-ROM interface is inoperative until the system is rebooted. Second, on the next warm reboot after a successful read of the CD-ROM, the expanded-memory manager (EMM) does not recognize the presence of EMS memory until the reboot is repeated. (Microsoft is working to correct both problems.)

After MSCDEX is installed, the CD-ROM drive can be treated like a DOS disk drive: it can be made the current drive, its directories can be listed, and files can be read from it. However, because DOS treats it like a network drive, CHKDSK, SUBST, JOIN, and ASSIGN, along with a few other commands are not allowed. At the end of a directory list, the space remaining on the drive is listed as zero, which is technically correct—because the drive does not allow writing, no additional space can be allocated.

Because the CD-ROM device driver is a character device, DOS cannot call it directly to read blocks from CD-ROM. All calls to the device driver come from MSCDEX. DOS and MSCDEX communicate by means of undocumented interrupt 2FH (multiplex interrupt) calls: DOS issues several interrupt 2FH calls at every disk I/O request. During installation, MSCDEX hooks itself to interrupt 2FH and then intercepts all calls from DOS for disk I/O, processing those that refer to the CD-ROM drive.

Microsoft specifies that a device driver for use with MS-DOS/CD-ROM extensions must support the following commands: INIT, IOCTL INPUT, INPUT FLUSH, IOCTL OUTPUT, DEVICE OPEN, DEVICE CLOSE, READ LONG, READ LONG PREFETCH, SEEK, PLAY, and STOP PLAY. These commands are implemented by the device-driver manufacturer, not the developer of the retrieval software. INIT, OPEN, CLOSE, and FLUSH perform standard functions essentially as documented for any device driver in the DOS *Technical Reference Manual.* IOCL INPUT allows MSCDEX to request status information from the device driver, including the address of the device header, location of the read head, whether the disk was changed, and the presence of audio tracks. IOCTL OUTPUT allows the drive door to be locked and unlocked, the disk to be ejected, and the drive to be reset (if the drive supports these functions under software control).

READ LONG, which requests the transfer of data from the CD-ROM to the system, is the crux of the MSCDEX program: it provides a way to specify a 32-bit sector number to an otherwise straightforward block-device driver. READ LONG operates in several modes. *Raw data mode* returns all 2,352 bytes of the physical sector, including the 2,048 data bytes of the logical sector and the error-detection codes (EDC) and error-correction codes (ECC). *Cooked mode* returns only the user data, leaving the EDC/ECC for the drive controller to handle. Two options are available for specifying the address of data to be read: In *HSG addressing mode*, the sector number is specified as a 32-bit logical sector number; in *Red Book addressing mode*, sector addresses are specified in physical format, as minute:second:sector.

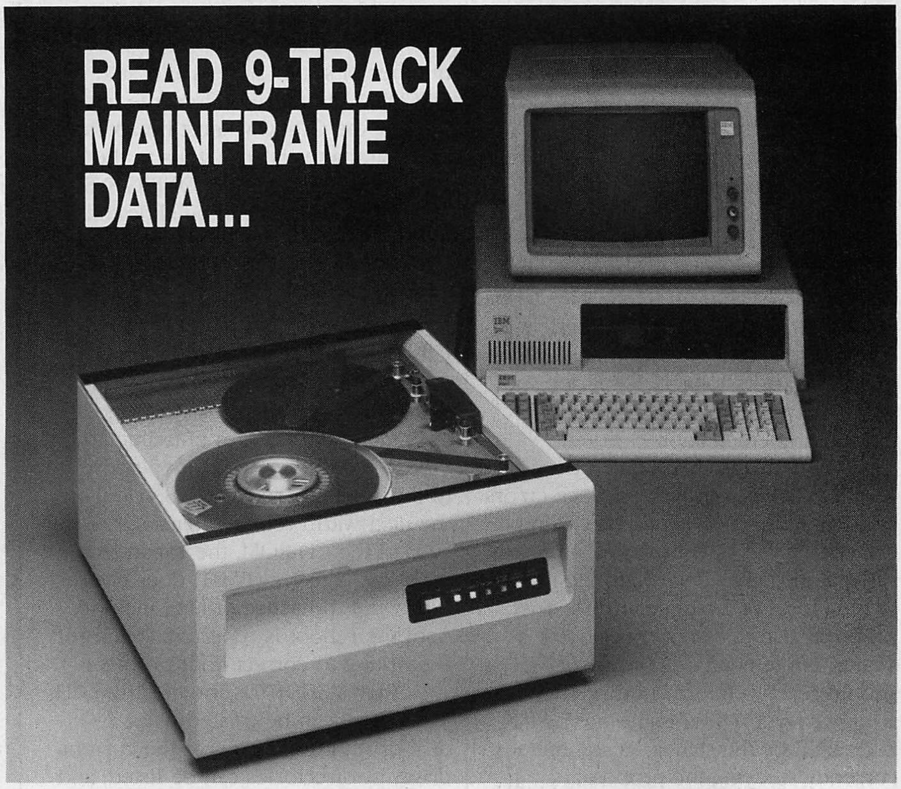
The READ LONG PREFETCH command helps compensate for the device driver's slow average access time. It initiates a low-priority seek operation and returns immediately. If a subsequent command is received by the drive before the seek is completed, the seek is canceled and the next command is performed. An option controls whether the requested sectors are actually read-in if the seek is successful. According to the documentation, this command is used for "advisory seek" operations to improve drive performance.

The SEEK command performs an explicit seek. Although the call also returns immediately, any subsequent disk operation waits until the SEEK operation is completed. Like the advisory seek, this command also can be used to improve performance by sending the head to the next data area while the previous input is being processed.

PLAY and STOP PLAY need to be supported only by an "extended" device driver. The PLAY command begins reading audio information at a specified sector number and sending it to the drive's audio output. Control returns immediately to the caller, but playback continues until a specified sector count is satisfied or a STOP PLAY command is issued. The calling program can monitor the busy bit in the device driver's status word to determine when playback has been completed.

The above commands are issued to the device driver by MSCDEX. Commands to MSCDEX, in turn, usually come from DOS through interrupt 21H. However, Microsoft also provides a way for applications to communicate directly with MSCDEX, allowing them to obtain information not available through DOS.

The programming interface with MSCDEX is implemented through the multiplex interrupt 2FH with AH =



15H. Available functions are shown in table 9. To invoke a function, the application loads 15H into the AH register, the function number into the AL register, and other information into other registers as required, and executes an interrupt 2FH. Function 0 returns the number of DOS drive letters assigned to CD-ROM drives and the starting drive letter. Function 1 returns, for each DOS volume, a pointer to the device header for the CD-ROM drive and a subunit number of the drive within the driver. For example, if one device driver were supporting three CD-ROM drives, this function would fill an array with three subunit numbers 0 through 2 and three far pointers all set to the same value.

Functions 2, 3, and 4 return the names of the indicated files from the type 1 volume descriptor. The copyright- and abstract-file names are defined in the HSG proposal, and the bibliographic document file is expected to appear in the ISO standard. Read VTOC (function 5) displays the Volume Table of Contents, Microsoft's name for the sequence of volume descriptors at the front of the data area. Each call to this command reads the next descriptor in sequence. Function 9 is analogous to DOS interrupt 25H: it is directly converted into a READ LONG call to the device driver that reads in sectors identified by logical sector number.

TABLE 9: *MSCDEX Interface*

AL	FUNCTION
0	Get CDROM drive info
1	Get CDROM drive list
2	Get copyright file name
3	Get abstract file name
4	Get bibliographic documentation file name
5	Read VTOC
8	Absolute disk read
9	Absolute disk write

These MSCDEX interface functions are implemented through the multiplex interrupt 2FH with AH = 15H.

Although formal CD-ROM standards do not as yet exist, the process of standardizing CD-ROM has been quite successful. Because the HSG proposal is already widely accepted, submissions to various standard-setting groups are proceeding at a fast pace. Almost certainly, the final standard will be modified from the original. The appearance of CD-ROM retrieval tools, such as the Microsoft DOS extensions, indicates that applications conforming to a base level can begin to reach the market.

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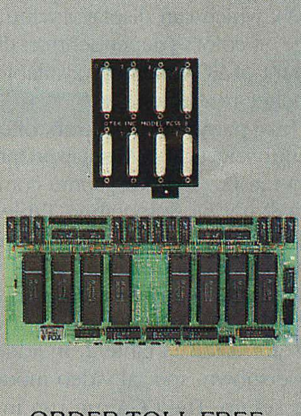
Peter Jansson, an internal consultant for LifeCard International, has worked for the last three years on development of the firm's optical memory card technology. LifeCard International is based in Towson, Maryland.



Detecting Display Systems

The variety of display adapters and monitors for the PC means that software developers must take steps to detect and select the most suitable combination.

AUGIE HANSEN

The ability to choose among a dozen PC display modes (15 counting the PC*jr* modes) is a mixed blessing. With so many modes, at least one is bound to suit the needs of a program; however, determining the type of hardware installed in a PC can be difficult.

PCs endowed with multiple display systems provide versatility for the user, but pose additional problems for program developers. Automatic display system selection, although desirable, is often inappropriate; often, the user must be involved in the selection process.

Detecting the presence of various types of display system hardware, obtaining the current video mode, and switching between display modes and adapters all can be achieved with the proper programming tools. This article presents two such demonstration programs. The source code is for Microsoft C 4.0. If the source code files are to be compiled using other C compilers, minor modifications may be needed.

Many display adapters and video monitors are available. Ignoring the IBM Professional Graphics Controller, 3270 PC, and other specialty display systems, the bulk of the display systems installed in PCs includes the following:

- IBM monochrome display adapter, which displays text and contains a parallel port adapter
- IBM Color Graphics Adapter (CGA), which has RGB (red-green-blue) and composite video outputs
- Hercules Graphics Card, which allows graphics to be displayed on a monochrome monitor
- IBM Enhanced Graphics Adapter (EGA), which can display a wide range of colors (dependent on the amount of EGA memory available) at higher resolution

Third-party manufacturers offer a bountiful selection of display adapters and monitors. However, some combinations will not work together. Table 1 summarizes the adapter-display combinations that are acceptable.

Access to display systems is handled by the PC's BIOS. Supported video modes are listed in table 2. In addition to those shown, special video modes can be set up. The CGA can run in low resolution, displaying 160-by-100 pixels per screen. This is actually a text mode, although it gives the appearance of being a graphics mode with fat pixels. Low-resolution mode is not supported by BIOS routines. A mode that displays 43 lines of 80 characters each can be programmed into the EGA by loading an 8-by-8-pixel character set and selecting a print-screen routine.

TAKING INVENTORY

The BIOS data area contains two bytes that reflect the state of the machine when it was booted. The bits indicate how many diskette drives, parallel ports, and serial ports are installed, what the initial video mode is, how much memory is on the system board, and whether a game I/O board is present. This information can be obtained by a call to software interrupt 11H. The information is not sufficient to discern how many video adapters are installed, so another method is needed.

Figure 1 identifies the primary display adapter memory allocations. Examining display memory directly provides

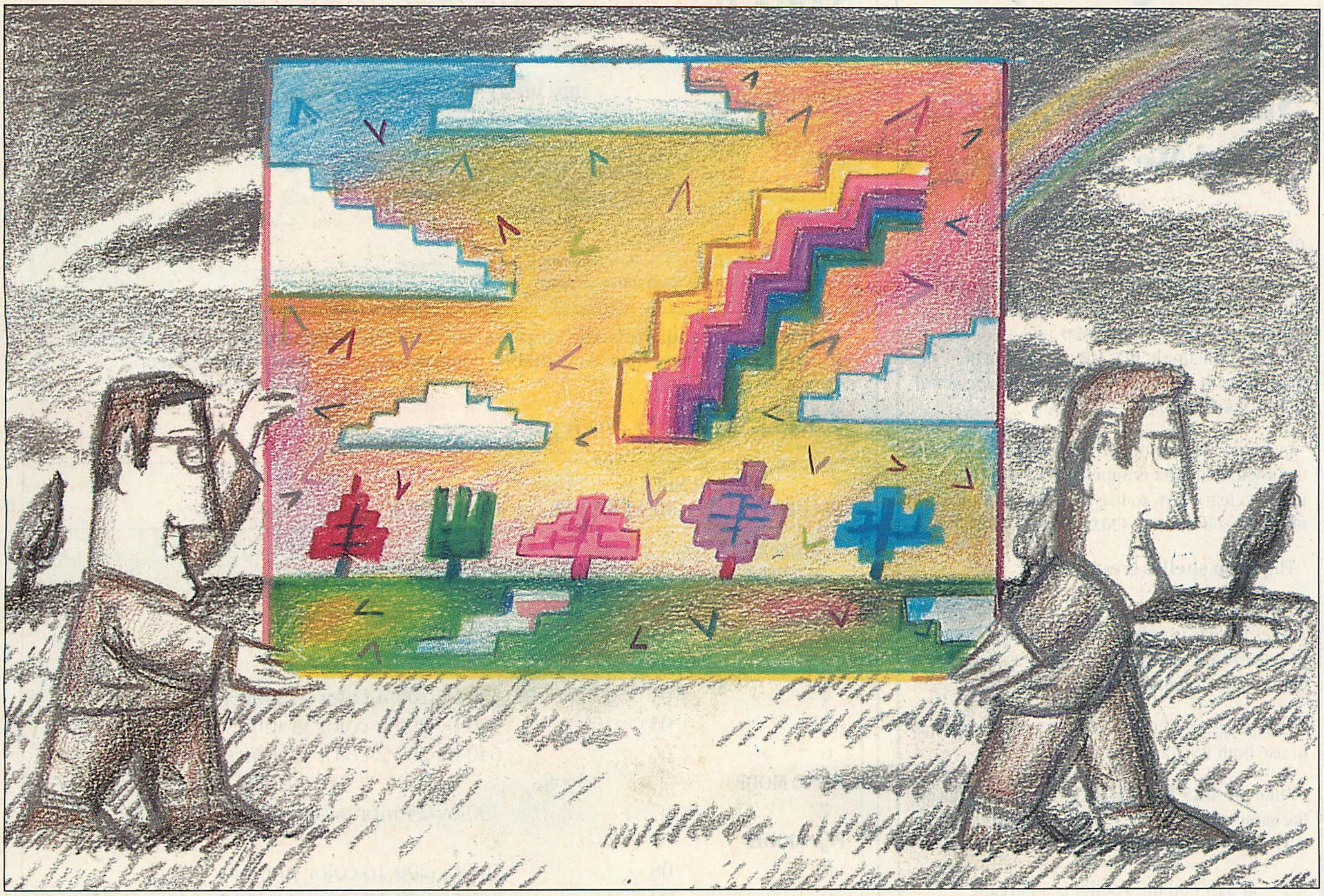


ILLUSTRATION • MACIEK ALBRECHT

a means of checking for the presence of adapters other than the default indicated by BIOS. The tool that checks for memory is an elaboration of BASIC's PEEK function. Listing 1 is the source code for MEMCHK.C, which uses the **movedata** runtime library routine to copy data between segments. The **memchk** function checks for active memory at the specified segment and offset by writing a value into the location, reading it back, and, finally, comparing the before and after values. It preserves the original value at the tested location, thus protecting the operating system and program code or screen characters and attributes.

The memory test works fine for monochrome and CGA hardware, but it does not work with the EGA. It is detected by using an EGA BIOS routine, ALTERNATE FUNCTION (service number 12H under the BIOS video interrupt). One service of this function is to return EGA information (BL = 10H).

The function EGA_INFO.C (listing 2) returns a 1 if an EGA is installed and a 0 if not. The four variables, the addresses of which are passed as parameters to the function call, are filled in with the memory size, current mode (monochrome or color), feature-bit settings, and EGA switch settings. The variables contain useful data only if the **ega_info** function returns a 1.

The BIOS data area is updated when the display mode is altered. The BIOS video interrupt service 0FH is used to obtain the current video state. GETSTATE.C (listing 3) uses video service 0FH to determine which display adapter is currently active by checking the video mode.

The program DSPYINFO examines memory and retrieves data from BIOS and displays a summary of the display adapters it finds and the current video state. The source code for DSPYINFO is contained in DSPYINFO.C (listing 4). The Microsoft MAKE command will use the makefile DSPYINFO.MK as well as TOOLS.INI (listings 5 and 6) to compile and link the program automatically.

When determining what display adapters are installed, the DSPYINFO first tests for an EGA. If one is found, the program looks for a secondary adapter. If the EGA is in color mode, the program tests for a monochrome adapter; if in monochrome mode, it tests for a CGA. Figure 2 shows the output from DSPYINFO when it is run on a system equipped with both a Quadram EGA+ and an IBM monochrome adapter.

DISPLAY/MODE SWITCHING

When a PC has more than one display system, the default may not be the one needed by a program to run successfully. The program must intelligently determine a course of action that will either make a smooth transition to the needed display or tell the user to switch displays and then exit. The danger of automatically switching to the needed display is that it may not be turned on. It is safer to have the user manually select the needed display.

Manual selection can be achieved easily at the DOS level by using the MODE command of DOS before running a program that needs to be on a particular display (or that would at least benefit from being on a color monitor

TABLE 1: *Acceptable Adapter-Display Combinations*

	DISPLAY TYPE			
ADAPTER TYPE	**IBM MONO**	**RGB**	**COMPOSITE**	**ENHANCED**
IBM Monochrome	●	○	○	○
CGA	○	●	●	○
Hercules	●	○	○	○
EGA	●	●	—[a]	●

● = *Supported* ○ = *Not supported*
[a] *Supported by most third-party adapters*

Although many adapters and displays are available, some combinations were not meant to work together. Acceptable combinations are summarized here.

TABLE 2: *Video Modes*

MODE NUMBER		
DECIMAL	**HEXADECIMAL**	**DESCRIPTION**
CGA MODES		
0	00	40-by-25 monochrome text
1	01	40-by-25 color text
2	02	80-by-25 monochrome text
3	03	80-by-25 color text
4	04	320-by-200 4-color graphics
5	05	320-by-200 4-color graphics (color burst off)
6	06	640-by-200 2-color graphics
MONO MODE		
7	07	80-by-25 monochrome text
PC*jr* MODES		
8	08	160-by-200 16-color graphics
9	09	320-by-200 16-color graphics
10	0A	640-by-200 4-color graphics
RESERVED		
11	0B	N/A
12	0C	N/A
EGA MODES		
13	0D	320-by-200 16-color graphics
14	0E	640-by-200 16-color graphics
15	0F	640-by-350 monochrome graphics
16	10	640-by-350 4- or 16-color graphics[a]

N/A = Not applicable
[a] *Number of colors depends on amount of EGA memory*

The PC's BIOS supports several video modes. The programs presented here detect the current mode and allow switching between display modes and adapters.

rather than a monochrome display, for example). The command

```
MODE CO80
```

switches to a CGA- or EGA-driven display from a monochrome display system, and the command

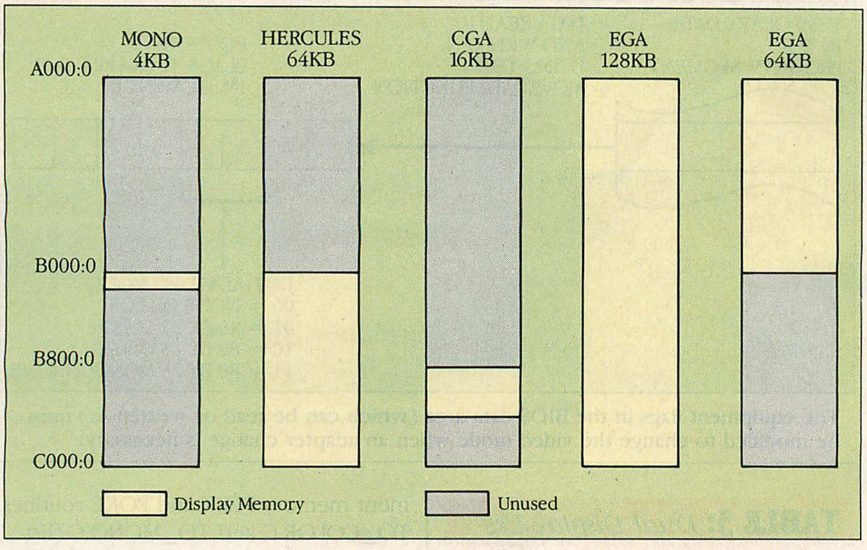
```
MODE MONO
```

does the opposite. A viable alternative is to display a menu on the default display that permits choosing the display from within the running program.

Automatic mode selection has its place as long as simple courtesy is observed. If, for example, a program must run on a graphics display, but the default is the monochrome mode on a dual-display system, the program can switch unilaterally to the graphics screen, provided that it returns to the monochrome display default when it terminates. This gives users the opportunity to exit if they choose not to turn on the graphics display.

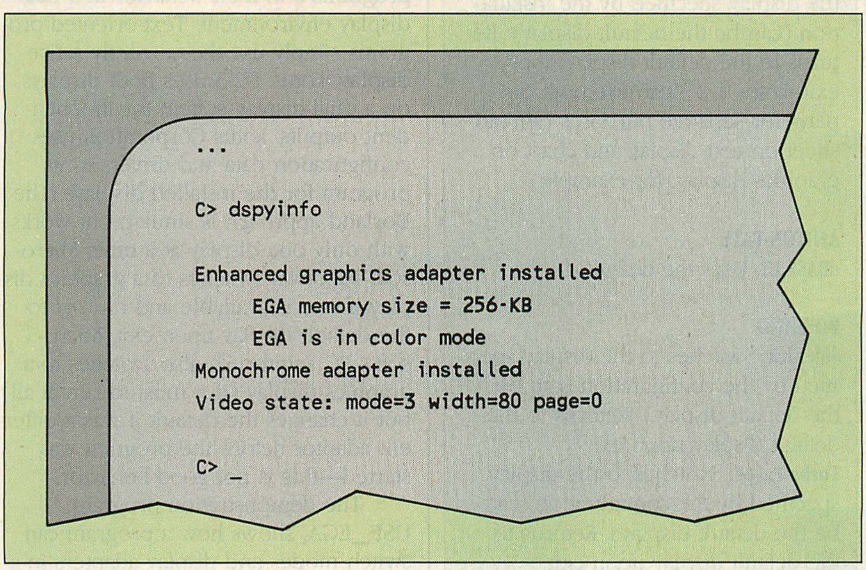
Even on a single-display system, an application often must change the video mode before it can proceed. DOS runs only in text modes, so a program that produces graphics will have to switch to a graphics mode. Methods for switching modes, whether from assembly, C, or

FIGURE 1: *Display Adapter Memory Allocations*



The primary memory allocation for four adapters is shown. Checking display memory directly can indicate the presence of an adapter other than the default.

FIGURE 2: *Sample DSPYINFO Output*



```
...

C> dspyinfo

Enhanced graphics adapter installed
    EGA memory size = 256-KB
    EGA is in color mode
Monochrome adapter installed
Video state: mode=3 width=80 page=0

C> _
```

DSPYINFO.C displays the adapters found and the video state. This is the screen shown when both an EGA and monochrome display adapter are installed.

another high-level language, are all based on the video interrupt, service 00H. A C-language equivalent to the mode-switching function of BASIC's SCREEN command is handled by the **setvmode** function of SETVMODE.C (listing 7). This function first sets the specified video mode and then updates the video parameters by calling the **getstate** function.

Attempting to change the video mode by using **setvmode** when it is necessary to switch to a different display adapter (mode 7 to mode 3, for example) requires additional work. The equipment flags in the BIOS data area also must be modified. Figure 3 depicts a program reading and writing the equipment flags at absolute address 0:0410H. Bits 4 and 5 indicate the initial display adapter that is specified by the switches on the system board at boot time. To indicate the current default display, a program must alter the monitor bits in the equipment flags while not disturbing any of the other bits.

Both the **to_color** and **to_mono** functions must be used in conjunction with the **setvmode** function when the mode switch implies an adapter switch. These two functions use the **movedata** intersegment copy function to imple-

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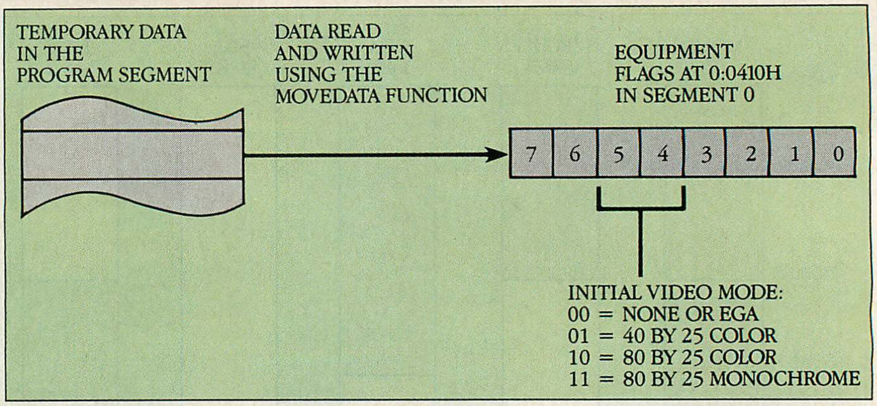
FIGURE 3: *Using the BIOS Equipment Flags*



The equipment flags in the BIOS data area (which can be read or written to) must be modified to change the video mode when an adapter change is necessary.

TABLE 3: *Dual Display Use*

LOTUS

Lotus 1-2-3. Lotus Access runs on the default display. Lotus 1-2-3 runs on the display specified by the installation (can be the default display). Returns to the default display upon exit. Lotus 1-2-3 can use both displays for separate purposes (spreadsheet on text display and chart on graphics display, for example).

ASHTON-TATE

dBASE III. Uses the default display.

BORLAND

SideKick. Switches to the display specified by the configuration (can be the default display). Returns to the default display upon exit.

Turbo Pascal. Switches to the display specified by the configuration (can be the default display). Returns to the default display upon exit.

MICROSOFT

PC Paintbrush. Switches to the graphics display if necessary. Makes the graphics display the new default.

QuickBASIC. Uses the default display.

Windows. Switches to the graphics display if necessary. Returns to the default display upon exit.

Word. Uses the default display.

WORDPERFECT CORP.

WordPerfect. Uses the default display.

Programs behave differently in the presence of two display systems. In the ideal situation, the program should return the system to the default display upon exiting.

ment memory PEEK and POKE routines. TO_COLOR.C and TO_MONO.C (listings 8 and 9) give the source code.

Major PC applications handle the display selection task in a variety of ways. Table 3 is a summary of selected programs and their behavior in a dual-display environment. Text-oriented programs simply use the currently active display. Lotus 1-2-3 uses both displays on a dual-display system for independent outputs. Lotus Corporation uses configuration data and drivers in its program for the installed displays. The Borland approach is similar, but works with only one display at a time. Microsoft Windows switches to a graphics display if one is available and returns to the default display upon exit. Microsoft's PC Paintbrush also switches to a graphics display (if it must to run at all) but it changes the default if was a different adapter before the program was started—this is not good behavior.

The demonstration program, USE_EGA, shows how a program can switch modes and display adapters in a controlled and predictable manner. USE_EGA.C (listing 10) is the source code for USE_EGA, and its makefile, USE_EGA.MK, is contained in listing 11. The program switches from the default video mode (usually 3 or 7) to mode 13, displays a simple message, and waits for the user to press the Enter key. Upon exit, the program restores the user's previous video mode. Note the use of **to_color** and **to_mono** if an adapter switch is required. If no EGA adapter is installed, the program displays an error message and exits.

Augie Hansen owns Omniware, a Denver-based computer consulting firm. This article is based on portions of his latest book, Proficient C, *published by Microsoft Press (1987).*

LISTING 1: MEMCHK.C

```
/*
 *      memchk -- look for random-access memory at
 *      a specified location; return non-zero if found
 */

#include <dos.h>
#include <memory.h>

int
memchk(seg, os)
unsigned int seg;
unsigned int os;
{
        unsigned char tstval, oldval, newval;
        unsigned int ds;
        struct SREGS segregs;

        /* get value of current data segment */
        segread(&segregs);
        ds = segregs.ds;
        /* save current contents of test location */
        movedata(seg, os, ds, (unsigned)&oldval, 1);
        /* copy a known value into test location */
        tstval = 0xFC;
        movedata(ds, (unsigned)&tstval, seg, os, 1);
        /* read test value back and comapre to value written */
        movedata(seg, os, ds, (unsigned)&newval, 1);
        if (newval != tstval)
                return (0);

        /* restore original contents of test location */
        movedata(ds, (unsigned)&oldval, seg, os, 1);

        return (1);
}
```

LISTING 2: EGA_INFO.C

```
/*
 *      ega_info -- gather information about an EGA;
 *      return a non-zero value if one is found
 */

#include <dos.h>

#define ALT_FUNCTION    0x12
#define EGA_INFO        0x10
#define NMODES          2
#define NMEMSIZ         4
#define VIDEO_IO        0x10

int
ega_info(memsize, mode, features, switches)
int *memsize;           /* EGA memory size indicator: 0 = 64K */
                        /* 1 = 128K; 2 = 192K; 3 = 256K */
int *mode;              /* 0 = color mode; 1 = mono mode */
                        /* use getstate function to find out which mode */
unsigned int
        *features,      /* feature bit settings */
        *switches;      /* EGA switch settings */
{
        int result = 0;
        union REGS inregs, outregs;

        /* request EGA information */
        inregs.h.ah = ALT_FUNCTION;
        inregs.h.bl = EGA_INFO;
        int86(VIDEO_IO, &inregs, &outregs);

        *memsize = outregs.h.bl;
        *mode = outregs.h.bh;
        *features = outregs.h.ch;
        *switches = outregs.h.cl;

        /* return non-zero if EGA installed */
        if (*memsize >= 0 && *memsize < NMEMSIZ &&
                *mode >= 0 && *mode < NMODES)
                result = 1;
        return (result);
}
```

LISTING 3: GETSTATE.C

```
/*
 *      getstate -- update video state variables
 */

#include <dos.h>

#define GET_STATE       0xF
#define VIDEO_IO        0x10

/* current video state/mode information */
short Vmode;
short Vwidth;
short Vpage;

int
getstate()
{
        union REGS inregs, outregs;
        inregs.h.ah = GET_STATE;
        int86(VIDEO_IO, &inregs, &outregs);
        Vmode = outregs.h.al;
        Vwidth = outregs.h.ah;
        Vpage = outregs.h.bh;
        return (outregs.x.cflag);
}
```

LISTING 4: DSPYINFO.C

```
/*
 *      dspyinfo -- display information about installed adapters
 */

#include <stdio.h>
#include <dos.h>
#define MDA_SEG 0xB000
#define CGA_SEG 0xB800

main()
{
        int mdaflag, egaflag, cgaflag;
        int ega_mem, ega_mode;
        unsigned int features, switches;
        static int memtab[] = {
                64, 128, 192, 256
        };

        extern int getstate();
        /* current video mode information (declared in getstate) */
        extern short Vmode, Vwidth, Vpage;
        extern int ega_info(int *, int *, unsigned *, unsigned *);
        extern int memchk(unsigned int, unsigned int);

        mdaflag = egaflag = cgaflag = 0;

        /* look for display adapters */
        if (ega_info(&ega_mem, &ega_mode, &features, &switches))
                ++egaflag;
        if (egaflag) {
                puts("Enhanced graphics adapter installed");
                printf("\tEGA memory size = %d-KB\n",
                        memtab[ega_mem]);
                printf("\tEGA is in %s mode\n",
                        ega_mode ? "monochrome" : "color");
        }

        if (egaflag && ega_mode == 0) {
                /* look for IBM monochrome memory */
                if (memchk(MDA_SEG, 0))
                        ++mdaflag;
        }
        else {
                /* look for color/graphics memory */
                if (memchk(CGA_SEG, 0))
                        ++cgaflag;
```

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```
        }
        if (mdaflag)
                puts("Monochrome adapter installed");
        if (cgaflag)
                puts("Color/graphics adapter installed");
        /* report video settings */
        getstate();
        printf("Video state: mode=%d width=%d page=%d\n",
                Vmode, Vwidth, Vpage);

        exit(0);
}
```

LISTING 5: DSPYINFO.MK

```
# makefile for the DSPYINFO program

# --- symbolic names ---
MODEL = S       # used by tools.ini
OBJS = ega_info.obj getstate.obj memchk.obj

# --- the DSPYINFO program ---
dspyinfo.exe:   dspyinfo.obj $(OBJS)
        link $* $(OBJS), $*, nul;

# --- linkable objects ---
ega_info.obj:   ega_info.c

getstate.obj:   getstate.c

memchk.obj:     memchk.c

dspyinfo.obj:   dspyinfo.c
```

LISTING 6: TOOLS.INI

```
[make]

.c.obj:
        cl -c -A$(MODEL) -DLINT_ARGS $*.c
```

LISTING 7: SETVMODE.C

```
/*
 *   setvmode -- set the video mode
 *   (color/graphics systems only)
 */

#include <dos.h>

#define VIDEO_IO    0x10
#define SET_MODE    0

int
setvmode(vmode)
unsigned int vmode; /* user-specified mode number */
{
        union REGS inregs, outregs;
        extern int getstate();

        inregs.h.ah = SET_MODE;
        inregs.h.al = vmode;     /* value not checked */
        int86(VIDEO_IO, &inregs, &outregs);

        /* update video data */
        getstate();

        return (outregs.x.cflag);
}
```

LISTING 8: TO_COLOR.C

```
/*
 *      to_color -- switch from MDA to CGA
 */

#include <dos.h>
#include <memory.h>
```

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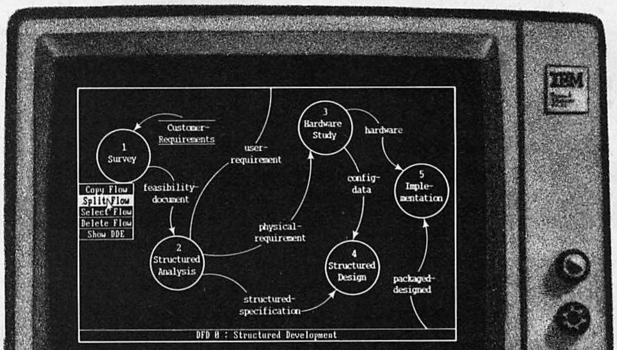

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```
#define EQ_FLAGS        0x410
#define VMASK           0xCF    /* mask video bits off */
#define CGA_MODE        0x10

void
to_color()
{
        unsigned int ds;
        unsigned char tmp;
        struct SREGS segregs;
        segread(&segregs);
        ds = segregs.ds;
        movedata(0, EQ_FLAGS, ds, (unsigned)&tmp, 1);
        tmp &= VMASK;
        tmp |= CGA_MODE;
        movedata(ds, (unsigned)&tmp, 0, EQ_FLAGS, 1);
}
```

LISTING 9: TO_MONO.C

```
/*
 *      to_mono -- switch from CGA to MDA
 */

#include <dos.h>
#include <memory.h>

#define EQ_FLAGS        0x410
#define MDA_MODE        0x30

void
to_mono()
{
        unsigned int ds;
        unsigned char tmp;
        struct SREGS segregs;
        segread(&segregs);
        ds = segregs.ds;
        movedata(0, EQ_FLAGS, ds, (unsigned)&tmp, 1);
        tmp |= MDA_MODE;
        movedata(ds, (unsigned)&tmp, 0, EQ_FLAGS, 1);
}
```

LISTING 10: USE_EGA.C

```
/*
 *      use_ega -- Attempt to switch to an EGA graphics mode.  Return
 *      to the default display and mode upon exit.
 */

#include <stdio.h>
#include <dos.h>

/* --- video modes --- */
/* CGA modes */
#define CGA_M40         0
#define CGA_C40         1
#define CGA_M80         2
#define CGA_C80         3
#define CGA_CMRES       4
#define CGA_MMRES       5
#define CGA_MHRES       6
/* MDA mode */
#define MDA_M80         7
/* PCjr modes */
#define PCJR_CLRES      8
#define PCJR_CMRES      9
#define PCJR_CHRES      10
/* modes 11 and 12 are not currently used */
/* EGA modes */
#define EGA_CMRES       13
#define EGA_CHRES       14
#define EGA_MHRES       15
#define EGA_EHRES       16

/* current video state/mode information (declared in getstate) */
extern short Vmode;
extern short Vwidth;
extern short Vpage;

main()
{
        int egaflag, oldmode;
        int ega_mem, ega_mode;
        unsigned int features, switches;
        static int memtab[] = {
                64, 128, 192, 256
        };

        extern int getstate();
        extern int ega_info(int *, int *, unsigned *, unsigned *);
        extern int setvmode(int);
        extern void to_color();
        extern void to_mono();

        egaflag = 0;

        /* get video state data */
        getstate();
        oldmode = Vmode;

        /* look for an EGA */
        if (ega_info(&ega_mem, &ega_mode, &features, &switches))
                ++egaflag;

        /*
         * if EGA found, switch video mode, display something, and
         * then return to the display mode found upon entry
         */
        if (egaflag) {
                if (oldmode == MDA_M80)
                        to_color();
                setvmode(EGA_CMRES);
                printf("\nTESTING EGA IN GRAPHICS MODE\n");
                getstate();
                printf("Current video state:\n\tmode=%d width=%d page=%d\n",
                        Vmode, Vwidth, Vpage);
                printf("\nPress ENTER to return to DOS:");
                /* pause */
                while (getchar() != '\n')
                        ;
                if (oldmode == MDA_M80)
                        to_mono();
                setvmode(oldmode);
                getstate();
                printf("Current video state:\n\tmode=%d width=%d page=%d\n",
                        Vmode, Vwidth, Vpage);
        }
        else {
                /* write to the default display */
                puts("No EGA adapter installed");
                exit(1);
        }

        exit(0);
}
```

LISTING 11: USE_EGA.MK

```
# makefile for the USE_EGA program

# --- symbolic names ---
MODEL = S
OBJS = ega_info.obj getstate.obj setvmode.obj to_color.obj to_mono.obj

# --- the USE_EGA program ---
use_ega.exe:    use_ega.obj $(OBJS)
        link $* $(OBJS), $*, nul;

# --- objects ---
ega_info.obj:   ega_info.c

getstate.obj:   getstate.c

setvmode.obj:   setvmode.c

to_color.obj:   to_color.c

to_mono.obj:    to_mono.c

use_ega.obj:    use_ega.c
```

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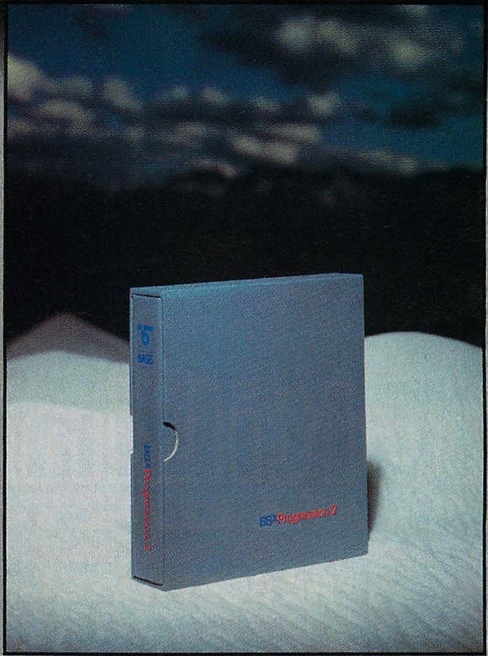

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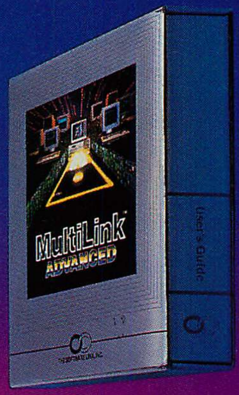

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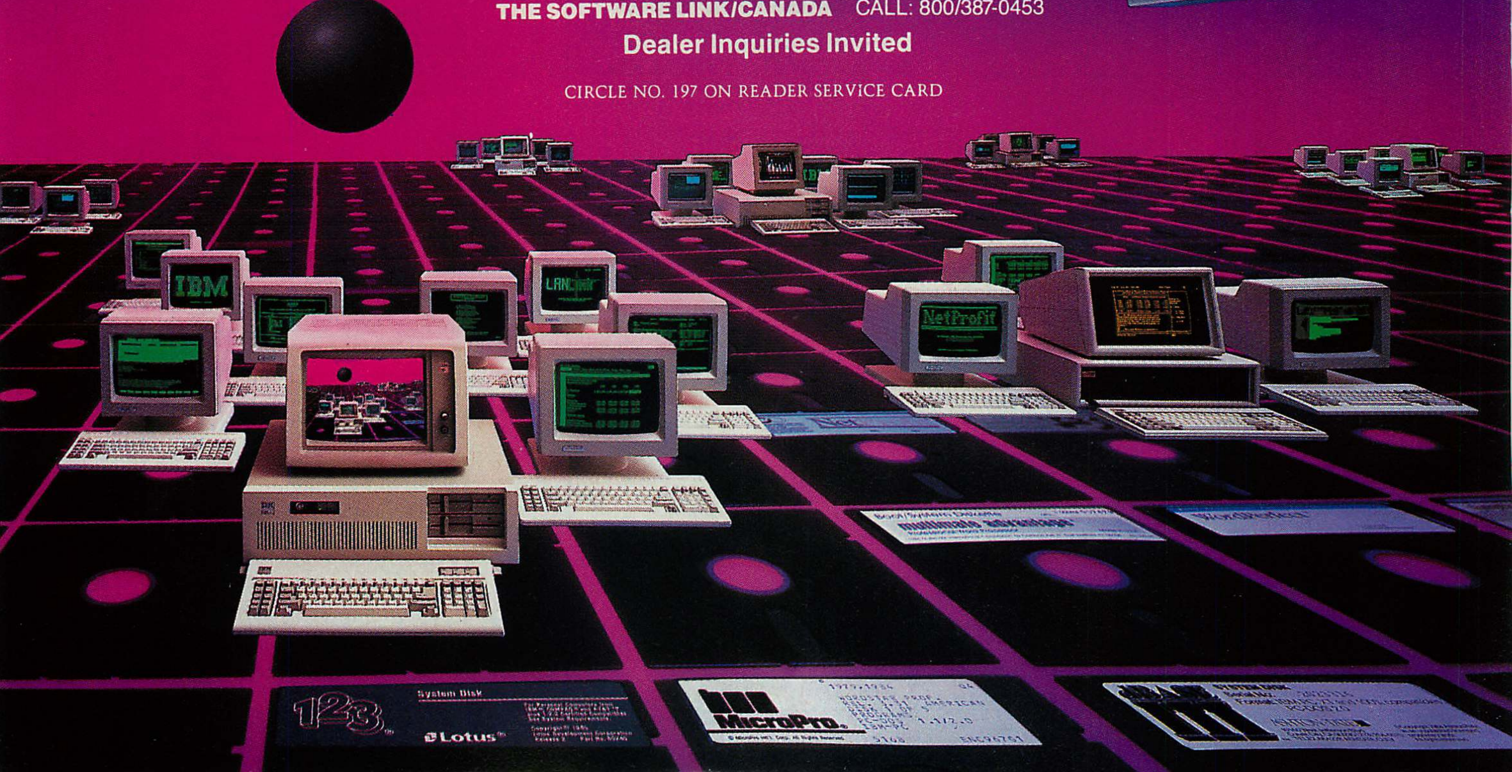

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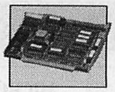
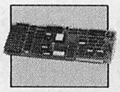


286 SPEEDCARD
Micro 1



MOTHERCARD 5.0
SOTA Technologies, Inc.

HDTEST
Proto PC, Inc.

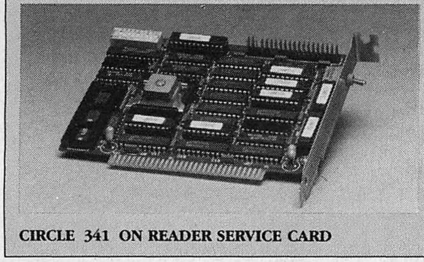
PRINTQ 3.06
Software Directions, Inc.

BOOSTERS 2.0
George F. Smith & Company

286 SPEEDCARD

Micro 1
557 Howard Street
San Francisco, CA 94105
415/974-5439

PRICE: $495

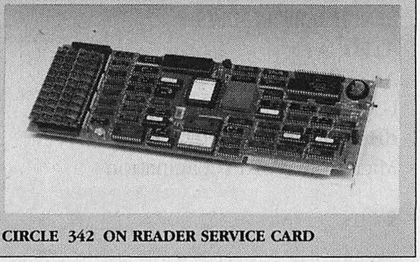


CIRCLE 341 ON READER SERVICE CARD

MOTHERCARD 5.0

SOTA Technologies, Inc.
657 N. Pastoria Avenue
Sunnyvale, CA 94086
408/245-3366

PRICE: $1,295



CIRCLE 342 ON READER SERVICE CARD

Three types of accelerators exist for speeding up an IBM PC: the first speeds up the original PC hardware with faster clock rates; the second replaces the original 8088 microprocessor with an 8086, which is not only faster, but also a greater workhorse; the third replaces the 8088 with an even more capable processor—the 80286. This third type of accelerator presents two different approaches in using the 80286. At one end are caching boards that provide a limited amount of high-speed 16-bit memory to augment the slower memory on the 8-bit bus. At the other end are boards that provide a full complement of memory either by replacing the original memory or by adding a separate address space. The two products reviewed here are examples of each. Micro 1's 286 SpeedCard is a caching board running at 7.2 MHz, and the MotherCard 5.0 from SOTA (State of the Art) Technologies, Inc., is a full-complement coprocessor running at 12.5 MHz—the fastest speed available on an add-in board. (Eleven other 80286 accelerator boards were reviewed in "Speed Infusion, Part 3", Ted Mirecki, June 1987, p. 118. For a review of five 8086 accelerators, see "Speed Infusion, Part 2," Ted Mirecki, April 1987, p. 66. For a review of six boards that increase the frequency of the 8088 on the PC, see "Speed Infusion, Part 1," Ted Mirecki, February 1987, p. 126.)

The Micro 1 286 SpeedCard is identical to the PC Technologies, Inc. (PCT) 286 Express accelerator board reviewed in last month's article. It provides 8KB of cache memory and obtains its synchronous 7.2-MHz clock signal by halving the frequency of the oscillator signal from the motherboard. It accepts an 80287 numeric coprocessor and runs it either at 4.77 MHz (the speed of the 8088 clock on the motherboard) or at the same speed as the 80286.

Before installation, eight DIP switches need to be set for selecting the 80287's operating speed, the total system memory, and the purpose of the toggle switch on the rear bracket. This last setting determines whether the switch selects between operation on the 80286 and 8088, or enables and disables the memory caching.

Installation into a PC follows a procedure that is standard for most accelerator boards. The 8088 and 8087, if present, are removed from the motherboard. The SpeedCard is inserted into an expansion slot and connected to the 8088 socket with a ribbon cable; the 8088 is then plugged into a socket on the end of the cable. A noise suppressor module is inserted into the vacated 8087 socket. This process is adequately described in the manual, and the ribbon cable connector is appropriately keyed to prevent inserting it backwards.

The documentation consists of a 12-page booklet with adequate installation instructions, but no information on the board's design and very little on its operation. No clue is given, for example, as to why one function of the toggle switch might be more desirable than the other. In this respect, PCT provides much better documentation for its version of this product.

Switching between processors, if the board is so configured, causes a reboot, but does not require powering down, as on some other accelerators. Caching may be turned on and off at any time. Micro 1 provides a resident program to control caching with hot keys, therefore, it is more useful to configure the board to have the toggle switch select the processor.

The 286 SpeedCard's performance is shown in the accompanying table. The tests used were described at length in February. They exercise the boards in several ways, including measuring the bus bandwidth, testing the 80287, and timing application programs.

The results for the 286 SpeedCard are identical to those obtained with its twin, the PCT 286 Express, and very similar to the other four synchronous caching boards. Because the measured performance of boards of this type is virtually indistinguishable, the choice can be made on price, quality of documentation, and vendor support.

The SOTA MotherCard 5.0, by contrast, is an advanced full-complement coprocessor unlike most other boards of this type. Because it is available in several configurations, there is a good chance that one MotherCard is unlike another of the same brand.

The first choice in configuring this accelerator is the amount of on-board memory—either 1MB using 256Kbit chips, or 4MB populated with 1Mbit chips. An optional daughterboard can raise the on-board memory to a maximum of 16MB, but its presence will allow only short boards in the adjacent expansion slot. The second option is the clock speed—a choice of 8, 10, or 12.5 MHz. Both options must be chosen when the board is purchased.

A third option, the speed of the 80287 numeric coprocessor, can be set by the user at installation either to 5 MHz or to the same speed as the 80286. Intel does not make a model of the 80287 guaranteed to run at more than 10 MHz (even though selected samples may run at over 12 MHz). Thus, it is advisable to purchase the high-speed MotherCard with an 80287 tested by SOTA. The model tested for this review had 1MB of memory, a 12.5-MHz clock, and an 80287 selected by SOTA for operation at that high speed.

With the 1MB model, the memory above the 640KB used by DOS is automatically configured as expanded memory according to the Lotus/Intel/Microsoft expanded memory specification (LIM EMS). Models with more than 1MB can split it between EMS and extended memory for protected mode use.

Installation involves removing the 8088 from the system board and plugging it into a socket on the MotherCard. The accelerator card itself is then plugged into an expansion slot on the system board and connected with a ribbon cable to the original 8088 socket. The 8087 need not be removed.

The MotherCard contains a BIOS that gains control during boot-up and prompts the user to choose (by pressing function keys) between booting up on the 8088 or on the 80286. Once running on either processor, the user may switch to the other one by executing a program from the DOS prompt. Going from one processor to the other, in either direction, reboots the system. Therefore, although the MotherCard is a true coprocessor with two distinct address spaces, it is not possible to leave data in one address space while executing in the other.

In operation, the MotherCard provides a very noticeable increase in speed. Screen updating, even on a CGA (Color Graphics Adapter), is very rapid yet remains smooth and free of video interference. The subjective impression, especially without heavy disk I/O, is that the MotherCard is faster than a PC/AT.

TABLE: *Accelerator Features and Performance*

	MICRO 1	**SOTA TECHNOLOGIES**
MODEL[a]	286 Speedcard	MotherCard 5.0
PRICE	$495	$1,295
SIZE OF BOARD	Half	Full
MEMORY TYPE	Cache, synchronous	Full complement, coprocessor
ON-BOARD MEMORY	8KB	1MB
SWITCH BETWEEN 8088/80286		
Toggle switch	●	○
Software	○	●
Hot key	○	○
Switch without reset	○	○
Switch without power down	●	●
MEASURED CLOCK RATES (MHz)		
80286 clock	7.2	12.5
80287 clock	7.2	12.5
MEMORY ACCESS		
Wait states	4	1
Bus bandwidth[b]	1	6.70
BENCHMARK RESULTS[b,c]		
ATFLOAT	2.25	3.90
Assembly of IBM VDISK	2.07	5.50
Lotus 1-2-3 recalculation	1.40	3.65
dBASE (Ashton-Tate) sort	1.17	1.25
Microsoft Word repagination	2.38	4.25

●=*Yes* ○=*No*

[a] *Features may be compared with other 80286 accelerators in table 1 of "Speed Infusion, Part 3," Ted Mirecki, June 1987, p. 120.*

[b] *Numbers represent the ratio to the speed of a standard IBM PC at 4.77 MHz.*

[c] *Performance may be compared with other 80286 accelerators in table 2 of "Speed Infusion, Part 3," Ted Mirecki, June 1987, p. 134.*

Two types of 80286 accelerators—a synchronous caching board and a full-complement coprocessor–show the trade-offs of cost, complexity, and performance.

The number in the product's name, 5.0, refers to the expected version number of the future protected-mode DOS —the name of which has since been announced as Operating System/2 (OS/2). SOTA, by designing its accelerator with protected-mode operation in mind, has tried to build-in insurance for future compatibility with OS/2. The on-board BIOS is not permanently burned into ROM, but resides instead in battery-backed static RAM (SRAM). Any updates made necessary by the production version of OS/2, or any interim bug fixes, can be distributed on disk much more economically than on ROM chips. In current models of the board, the battery is soldered in; when it runs down, the board must be returned to SOTA for replacement of the battery and reloading of the SRAM. The expected battery life is three to five years.

Although it is an actual production model, some elements of the MotherCard package make it resemble a prototype. The software is marked "preliminary," and the documentation—stapled pages from a laser printer—looks like a final draft, not a finished manual. The contents, however, are quite good—especially the installation instructions. A section on the theory of operation is not as useful as it might be; instead of describing the operation of this particular accelerator, it explains the general differences between the 8088 and 80286. Given the unusual design of this board, even a moderately experienced user would appreciate a more technical explanation of its operation.

The preliminary nature of the software is underlined by a bug in the EMM (Expanded Memory Manager) device driver. If the 8088 is activated after the EMM is installed, returning to the 80286 becomes impossible. SOTA is working to fix this bug.

In light of the promising technical specifications, the measured results for the SOTA MotherCard 5.0 are somewhat

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CIRCLE NO. 195 ON READER SERVICE CARD

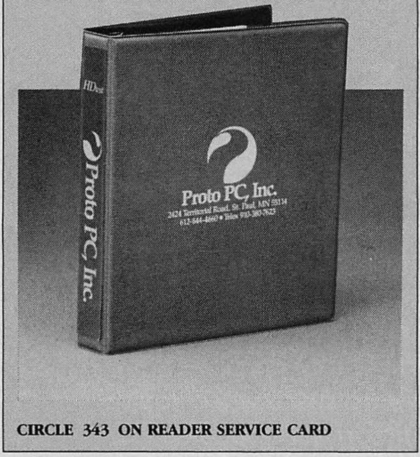
disappointing. Except for floating-point operations (which it runs at a higher clock speed than any other board tested in the accelerator series), the MotherCard does not stand out in comparison with the other full-complement accelerators reviewed last month. The attraction of this product, however, is not raw speed, but its promise of flexibility in adapting to the needs of future protected-mode operation under OS/2.

—TED MIRECKI

HDTEST

Proto PC, Inc.
2424 Territorial Road
St. Paul, MN 55114
612/644-4660

PRICE: $99



CIRCLE 343 ON READER SERVICE CARD

HDtest, a utility program that performs testing and low-level formatting of hard-disk drives, is a product mainly intended for use when a hard disk is first installed. It offers both *destructive* (that is, altering the contents of a disk) and *nondestructive* disk-testing options. HDtest's read-only test is its only nondestructive option. Destructive tests include both read and write operations; these options can detect hard-disk problems that the read-only test would miss. The nondestructive test logs bad track numbers, but the destructive test actually reformats bad tracks, marking each of them as "bad."

HDtest's low-level formatting capabilities give the user the ability to modify many drive and format parameters. When a hard disk is manufactured, its magnetic surfaces are completely blank. The first step in preparing a disk for use is low-level formatting, which maps out the disk's surface according to parameters that are set by the formatting program and disk-controller card. Concentric tracks are electronically marked on the disk's surface; each track is divided into a number of segments that will eventually hold data. Certain information (such as head number, cylinder number, logical sector number, and error-correction information) is encoded on the disk before and after each data segment. This information and the corresponding data segment combine together to make up each sector.

After low-level formatting, the disk then must be partitioned and high-level formatted. These functions are performed by two DOS programs FDISK (for partitioning) and FORMAT.

Most hard disks are sold with low-level formatting already performed. Those that are not preformatted usually come with the necessary software to handle this task. Therefore, the extensive formatting capabilities of HDtest are of no use to most end users. The program is intended more for those who need to prepare large numbers of hard-disk drives, such as manufacturers, VARs, dealers, and managers of large MIS departments. HDtest's ability to work with a wide variety of controller/disk combinations makes it particularly useful for those managers who are trying to stretch their equipment budgets by purchasing drives and controllers from various sources.

HDtest permits drives to be automatically configured (autoconfigured). During normal disk operations, certain information about the hard disk must be available—for example, the number of cylinders and heads, the starting cylinder number, and error-correction parameters. On hard disks that are not autoconfigured, this information is stored in ROM on the controller card (in the PC/AT, the active parameter table is stored in the battery-backed CMOS RAM parameter area). Each controller card's ROM contains a number of configuration tables, each of which contains a different set of parameters. The appropriate table is selected, by means of jumpers or switches on the controller, to match the characteristics of the disk that is attached to the controller. Without autoconfiguration, the disks that can be used with a particular drive controller are limited by the configuration tables of the controller.

An autoconfigured drive has the configuration information stored on the disk itself, written on track 0, and the information is read from there rather than from the ROM table on the controller card. The configuration information written on track 0 actually may be identical to that stored in one of the controller ROM tables, in which case autoconfiguration offers no advantage. However, autoconfiguration becomes useful when the configuration information written on the disk is different from that available in one of the controller's ROM tables. In certain situations, autoconfiguration can enable a controller to work with a disk that is not supported by its ROM tables. If HDtest is used to enter the autoconfiguration information onto the disk from the keyboard, it is possible to use some disk/controller combinations that, otherwise, would be incompatible.

HDtest also permits a disk to be virtually configured, which means dividing one physical disk into two DOS volumes. For example, a 40MB hard-disk drive could be virtually configured as a 30MB C: drive and a 10MB D: drive.

Not all hard-disk drive controllers support autoconfiguration and virtual configuration. The HDtest documentation provides detailed information on which controllers support which options. Many PC/XT-compatible controllers support autoconfiguration and virtual configuration; at present, AT-compatible controllers do not.

HDtest can be operated in either menu or command-line mode. In menu mode, the menu and data-entry screens are straightforward and well planned, allowing the user to move easily between various parts of the program, but, fortunately, with little chance of accidentally starting a formatting process. On-line help also is available.

The command-line mode allows essentially all program parameters to be controlled by entries on the command line when the program is started. Through this procedure, HDtest can be run from a batch file, which would be useful when the same operations need to be performed on a large number of drives or when extended tests need to be run, during which the computer may be left unattended for several hours.

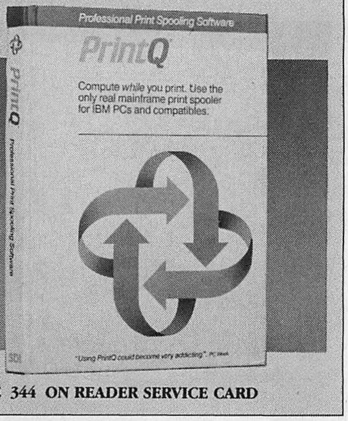
Two versions of the program are supplied: HT.EXE for the XT and compatibles, and HTA.EXE for the AT and compatibles. A head-parking program also is provided, as well as a patch to the DOS 2.1 FORMAT command that allows proper handling of bad tracks above 16MB. The manual is very good, providing clear explanations of program operation plus examples of how to proceed in common situations. HDtest will be welcome by those who need its high-volume hard-disk formatting and testing capabilities.

—PETER G. AITKEN

PRINTQ 3.06

Software Directions, Inc.
1572 Sussex Turnpike
Randolph, NJ 07689
201/584-8466

PRICE: $89



CIRCLE 344 ON READER SERVICE CARD

Printed output is the result of most computing activity, such as spreadsheets, reports, and so on. Advances in computer and printer performance notwithstanding, dealing with printers and printing is still one of the most time-consuming and user-*un*friendly aspects of personal computing.

The crux of the problem is that, compared to the other parts of a computer system, printers are extremely slow. For example, a spreadsheet that is calculated in a few seconds can take several minutes to print.

Hardware print buffers and memory-resident print spoolers can help by quickly swallowing data destined for the printer and allowing the application to proceed. This works well enough until the buffer fills up, whereupon things slow down to printer speeds again. Worse, if the power fails in mid-printing, all of the data in the buffer must be regenerated, possibly from multiple applications. In addition, other costs (in money and in time) are incurred: large external print buffers can cost more than the printers they feed, and internal memory has other more valuable uses.

PrintQ implements a spooling strategy more like that used on multiuser mainframe and minicomputer systems. In those environments, each user's printer output is diverted to a disk file. When an application program generates a print file, that print file is placed in a queue to be printed in turn.

PrintQ functions as a print buffer, capturing data sent to the printer via BIOS interrupt 17H and diverting it to a disk queue file. Queued data is printed in the background, allowing applications to run in the foreground.

The size of the queue file can be set from 1,014 to 65,000 blocks (1 block = 1,024 characters). The queue file will never grow beyond the specified size; if the queue fills up, programs that print will wait for space to be freed as the printer empties the queue.

Unlike more simple-minded buffers and spoolers, PrintQ stores each report or document as a separate logical entity, called a *printfile*. PrintQ's distinguishing strength is its ability to control each printfile separately.

PrintQ deduces printfile boundaries by watching for certain events:

- Program termination
- Time out (no data sent to printer within a specified time)
- Closing of the DOS PRN: device
- Explicit closing of the current print file by a user command

Each printfile in the queue is identified by the name of the program that generated the output (or a user-specified identification string) and a sequence number. In addition, each printfile has an associated priority, form type, page length, and other attributes that affect when and how it is printed.

Individual printfiles can be printed multiple times, held for later printing, viewed without printing, and written to DOS text files. Printfiles are grouped by the type of form required, and those that have a high priority are printed first. PrintQ also has options for pagination and forms alignment. The current printfile can be restarted from any page, which is a big help when the paper jams or runs out.

A single installation program, INSTALL, copies the necessary files to the specified target disk. PrintQ is not copy protected and can be installed on either diskettes or hard disks.

The installed PrintQ package consists of four programs: PRINTQ.EXE, PQSD.COM, PRTF.COM, and LIST.EXE. PrintQ places these executable files in the root directory of the target disk. Hard-disk users will probably want to place the programs in a subdirectory. The queue files are always created in a subdirectory called \PRINTQ.

PRINTQ.EXE is the actual spooler program, which captures and prints all the data. It is a terminate-and-stay-resident (TSR) program and includes a status/control display that can be activated by pressing Ctrl-Alt-P. PQSD.COM invokes the status/control display just as if Ctrl-Alt-P were struck. This program is intended for use in batch files to automatically invoke this display. PRTF.COM allows the printfile options to be set from the keyboard or from batch files. LIST.EXE copies DOS files into individual printfiles in the current queue file. Files are not identified by name, and wild-card templates are not supported.

The PRINT command of DOS, which does allow wild-card file names, can be used with PrintQ. The user should be sure to start PrintQ *before* trying to print any files with DOS PRINT; if PRINT runs first, it becomes the resident print multiplexer and PrintQ will refuse to run. If PrintQ is loaded first, PRINT will queue files correctly to the resident PrintQ multiplexer. Rebooting is the only way to remove the resident portion of PRINT.

The queue portion of the PrintQ status/control display shows the name of the current queue file, its current and maximum size in 1KB blocks, and the current queue and printer status. The printfile status portion of the display lists the printfiles in the current queue in the order in which they will be printed. For each entry in the queue, the display shows detailed information about the printfile. Commands are provided in an easy-to-use, full-screen interactive display. The commands control the settings of the various options and defaults for selecting and controlling queues and printfiles.

Despite its sophistication and power, PrintQ does have a few quirks and deficiencies worth noting. The pop-up status/control display switches to text mode and is supposed to restore the previous application screen before exiting. If the application was in an EGA (Enhanced Graphics Adapter) high-resolution graphics mode, the mode is restored but the screen image is not—a blank screen appears.

The status display does not change automatically to reflect any changes in printer status or page counts; to see changes, the F5 function key must be pressed to redisplay the status screen.

Deleting a printfile from the queue is not possible unless the status of the individual printfile is Hld (hold)—a minor annoyance. Trying to delete ready files while the entire queue is held from printing does not work; the status of the actual file to be deleted needs to be changed from ready to hold before deletion can take place.

PrintQ does not interpret the data in printfiles, except to count lines and pages for reporting and restarting purposes. This behavior allows PrintQ to work with virtually any printer. Because PrintQ has no idea what a printfile is supposed to have in it, the page counts for printfiles that contain graphics output or downloaded fonts are generally meaningless. For similar reasons, the option to view a printfile is not useful for graphics printfiles.

PrintQ could be even more useful if it added an option to print a text file paginated with top and bottom margins (perforation skipping), page title and subtitle, page numbers, line wrap, and so forth. This added feature would be especially useful for program listings and unformatted reports.

The PrintQ manual is superb. It is well organized, well written, complete, easy to use, professionally typeset, and includes a comprehensive index. Documentation of this quality is rare.

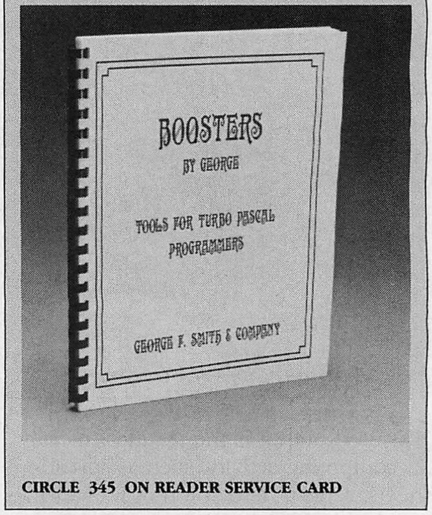
PrintQ is considerably less expensive and more intelligent than hardware buffers or simple memory-based FIFO (first-in, first-out) spoolers. The safety of spooling to nonvolatile disk storage; the ability to recover and restart after paper jams, power failures, or worse; and the rather complete control over individual printfiles make PrintQ an attractive productivity tool for the PC.

—THOMAS V. HOFFMANN

BOOSTERS 2.0

George F. Smith & Company
609 Candlewick Lane
Lilburn, GA 30247
(404) 923-6879

PRICE: $40



CIRCLE 345 ON READER SERVICE CARD

Speed is the name of the game in the ability to write attractive screen output, and Boosters, from George F. Smith & Company, will improve the screen-writing speed of any Turbo Pascal program. This collection of software tools for Turbo programmers, originally a user-supported package, comprises 78 video, heap, string, DOS, and special routines; demonstration and tutorial programs; a screen generator; a user's manual; and source code.

Boosters accommodates either a monochrome adapter or a CGA (Color Graphics Adapter) operating in the 80-column-by-25-line text modes. It does not support any of the higher-resolution graphics modes, however, leaving these tasks to packages such as Borland's own Turbo Grafix Toolbox.

The Boosters files come on three diskettes, which are not copy protected. The spiral-bound user's manual is clear and concise, including a summary of the Boosters routines, installation instructions, and detailed descriptions of each routine (with examples).

The Microsoft MASM-compatible assembly language source files in Boosters are used to create routines for in-line code in Turbo Pascal programs. These routines are incorporated using the {**$I**} compiler directive. The actual include files containing INLINE statements also are provided. Unfortunately, if changes need to be made to a source file, the file must be reassembled and new INLINE statements created manually from the assembly language listing. A program to perform this tedious task would be a greatly appreciated addition to this package.

Boosters achieves its speed by directly accessing the display memory and some BIOS memory. This reduces the portability of the Turbo programs, but with some changes, these routines can be adapted to other memory-mapped machines. The program's designers have included the source code so the problem is made relatively painless for the experienced programmer.

The Boosters screen-display routines are based on a page-data structure stored on Turbo Pascal's heap. Pages are read or built onto the heap and may be displayed quickly using video routines. This allows any time-consuming operations to be performed off-screen without affecting the display.

The Boosters video utilities address either monochrome or CGA memory automatically by examining the BIOS data stored in low RAM. When writing into display memory, the routines take care to ensure that a retrace is in effect. When moving large blocks of video data, the 6845 video controller's signal is disabled altogether. This is fine when an entire screen is being written, but it results in a choppy, flashing display when the tile effect is used.

In addition to the screen-drawing routines, many string utilities are provided for speeding up such string operations as centering, copying, pattern searching, replacement, and type conversion. Various DOS utilities allow manipulation of files and directory management. The Exec utility allows another program to be executed from within a Turbo Pascal .COM file. Other routines display pop-up calendars, date, and time; control the cursor; and provide filtered input.

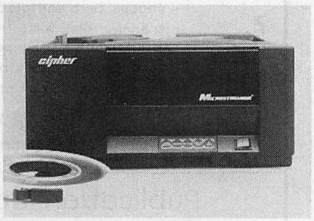
One of Booster's most interesting features is the screen generator—a program that allows users to design screens interactively. Once constructed, these screens can be saved to disk files to be loaded and displayed by the heap and video utilities. The screen generator, written in Turbo Pascal (with help from Boosters), can be run from the Turbo environment or as a .COM file. The user's manual contains an instructive tutorial, and the program also provides an on-line help facility, making screen generation effortless.

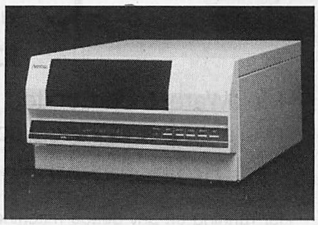
Most commands are entered using Alt-key combinations. It is worth noting that the Turbo Pascal editor uses the Ctrl key for commands, which makes using the Alt key for commands awkward. Worse, the screen generator program does not use Turbo Pascal's {$C-} directive to turn off Ctrl-key checking, so the program "breaks" when Ctrl-C is pressed. (Alt-C is the copy command.) Fortunately, the source code for the screen generator can be used to create a simple two-line fix to disable Ctrl-C.

Several tutorial programs are included with Boosters, along with associated source code. Also included is a job-estimation worksheet program that illustrates the use of many of the routines. In addition, a report on a bug in the Input procedure was included in the review package. The bug report contained instructions for a simple fix and expressed a commitment to support registered users in fixing bugs.

George Smith & Company has put together a winning package. This inexpensive product fills a niche in the Turbo Pascal world, allowing users to write aesthetically pleasing, professional programs easily. The authors are to be commended for including the source code as well—an invaluable aid in designing quality software.

—DOUG ORTEGA





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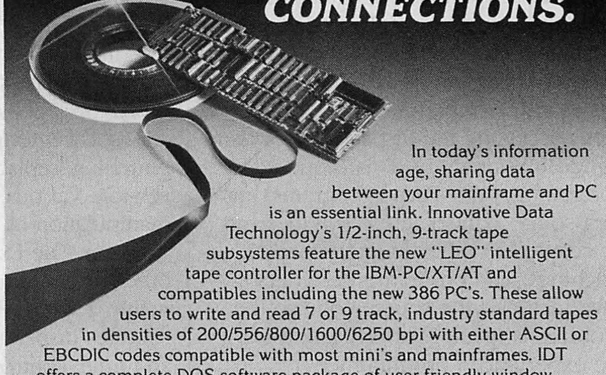

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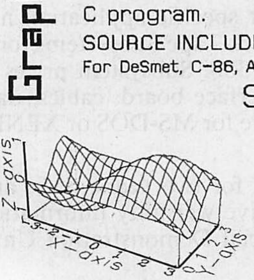

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An Outstanding Example

The computerized 1984 Olympic Message System employed human factors to the fullest extent possible.

After dialing a telephone number, you hear the following message:

WELCOME TO ELECTRONIC MAIL
PLEASE PRESS
1 For new mail
2 To reply to your mail
3 To send mail
4 To continue
5 To clean up files
6 For help
7 Replay this message

The above is an audio prompt with seven choices. After hearing the message (that is, hearing all the choices) you must recall the number that corresponds to your choice. Suppose there were fifteen choices. Suppose there were only three. This is the question with audio messages: *how many choices can a user handle effectively?*

The answer may or may not be obvious, but the question is an important one as computers with telephone access enter the home. Developers may disagree strongly about the answer, but the process can be put to actual empirical tests. This kind of testing does produce an answer (given later).

The subject of this month's column on human factors is a paper entitled, "The 1984 Olympic Message System—A Test of Behavioral Principles of System Design." Written by John Gould, Stephen Boies, Stephen Levy, John Richards, and Jim Schoonard, it is scheduled to be published in an upcoming issue of the *Communications of the ACM*. My hope is to encourage you to read this excellent paper.

I hold that the promulgation of human engineering is advanced as much by example as by research. But do not draw the wrong conclusion. The work discussed here was performed by a team, some of the members of which are recognized scholars in the field. Years of research are part of the authors qualifications. It is the final work, not the research, that is of interest here.

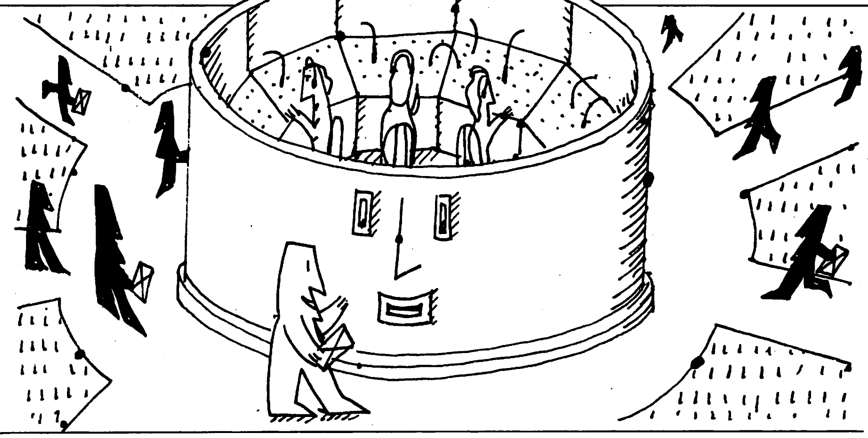


ILLUSTRATION • MACIEK ALBRECHT

The 1984 Olympic Message System (OMS) was a small but significant system. Basically, it was a limited electronic mail system operated over telephone lines by voice (see photo). It was used by people throughout the world and operated in 12 languages.

From a usability standpoint, the system was most interesting: It required public access and handled sensitive information. If it did not work correctly, people surely would know it. If it were too complicated to use, people would ignore it because substitute ways of sending messages were available.

The system was also interesting from a software engineering viewpoint. Developed by a team of five professional programmers and implemented on a network of more than 35 computers, the OEM certainly had a fixed deadline for being ready: the Olympics could not be postponed for late software. The system was designed, developed, and tested in less than a year.

A typical session with the OMS is shown in the accompanying figure. Although it may have cost a few million dollars, the system is beautiful in its simplicity. This work is significant for the following reasons

- The authors measured the progress on their project empirically.
- The work showed a sense of humor.
- The work revealed the power of an iterative design approach.
- The work demonstrated that larger is not necessarily better.
- The attention to detail was intense.
- The authors treated human engineering as seriously as functionality.
- The authors wrote the user manual before they did anything else.
- The system did not drown in a sea of cost overruns.
- The authors used prototypes of the system to great advantage.
- They had win-a-teddy-bear contests.
- They had try-to-crash-it tests.
- OMS was a success.

A great deal could be written on each of these points, a few of which will be reviewed here briefly.

One of the first things that the authors do in their paper is treat, head-on, the misconceptions that (1) human factors are obvious—everyone does those things, and (2) in real life, it is too expensive—there is not enough time. These perspectives cannot be dismissed; they are commonplace and represent the norm. While everyone preaches good human engineering, issues such as those listed above separate the faithful from those of little faith.

What have the authors actually demonstrated by their work on OMS? First, the principles listed above are not generally followed. They are not obvious and take definite discipline. Human factors are not a matter of fine tuning. The authors went on numerous field trips, studied and practiced with users, listened and learned, and listened and learned again. Second, and more significant, the schedule was met.

As far as expense is concerned, the authors continually point out that resolving design choices early provides for a greater savings later on. The result is a product more likely to be used or bought. Even the avoidance of just one or two false paths can mean great savings for the project overall, certainly enough to offset additional initial costs to support human factors.

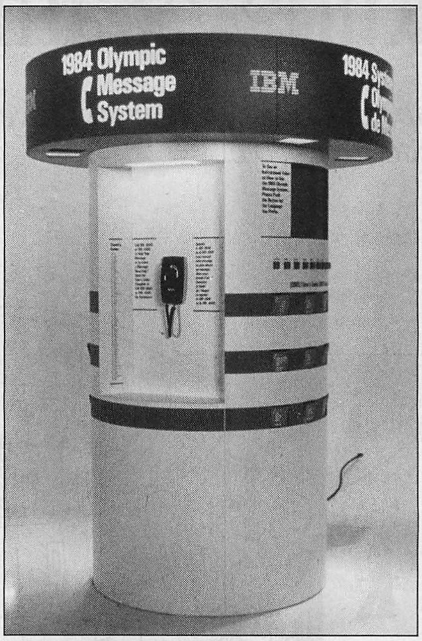
This did not mean that putting human engineering first was easy. The authors submit that it often was hard to break away from the computer terminal. Inevitable conflicts arose about spending time on interviews and travel when a piece of unfinished software was needed by a colleague. Conflicts also arose between time spent programming the real system versus time spent on a simulator.

The design was highly driven by empirical methods. For some, this conjures up the idea of special laboratories, statistical work, identification of sample sizes, and so on. But as a design strategy, one need not be so formal. Performing interviews, watching typical users try out the system, and setting up benchmark tasks can go a long way toward giving reliable feedback.

Some human factor specialists have argued that the user manual should be written first. In OMS, this principle was very successful. At the outset, the designers prepared printed scenarios describing how the user interface would work. These scenarios epitomized the system by forcing out a type of syntax, some functionality, and specific methods of navigating through the system. The designers forced themselves to examine and state what they were thinking by casting their thoughts in scenario sessions with the system.

The scenarios thus forced the system out into the open where outsiders and users could criticize, question, and evaluate its use. It made people consider whether they could use what was being offered—a critical question for the system at hand. Moreover, changes to the scenarios could be made easily. Such changes, before writing any code, paid for themselves by simply preventing code from being written when it was, in fact, not needed.

PHOTO: *An OMS Kiosk*



These kiosks had a display of the names of Olympians with messages, a push-button telephone, and instructions in 12 languages.

FIGURE: *An OMS Session*

```
USER:  Dial 740-4560.
OMS:   Olympic Message System.
       Please keypress your 3-letter Olympic
       country code.

USER:  U S A
OMS:   United States.  Etats-Unis.
       Please keypress your last name.

USER:  S M I T
OMS:   Alexis Smith.
       Please keypress your password.

USER:  4 0 5
OMS:   New messages sent by Message Center.
       "Alexi, all the best.  Your family."
       End of message.
       Press 1 Listen again, 2 Leave a Message,
       3 Hang up.

USER:  3
OMS:   Bye.
```

Maximum functionality is achieved on the OMS with a simple user interface.

Along this line of thought, the authors prepared two actual user guides. One was a guide for family and friends, and the other was for Olympians. Again, changes here were easy to make because the guide could be altered without writing code. Also, outsiders could readily respond and influence the design of the system. One consequence of having the guides early was that they served in the role of a functional specification. The guides became the defining documents for the system rather than letting the guides trail the actual implementation of the system.

Because of the user guides, the scenarios, the emphasis on earlier empirical testing, the simulation of the system with actual users, and the repeated testing to check the functionality, late changes to the product were reduced to a bare minimum. Certainly, people would have additional ideas later on, but, as often as not, a late change request had been considered at an earlier date and some rationale (possibly empirical data) had suggested that it was ill advised. It is easy to argue principles, but difficult to argue with data.

The authors also deal with the "help" myth. How often has someone muttered something about a feature being complex or suggesting that the system as a whole might be overwhelming only to hear, "Don't worry, we have a good help system." This is a throwaway line, a lame excuse. This group of authors did not rely on help to explain or justify any complexity. The goal was always the same—simplicity wherever possible. They made some tough choices, often in favor of simplicity, at the expense of functionality.

This brings up a novel point with respect to OMS. It is one of those rare times where there was pressure to *reduce* functionality rather than expand it. Time after time the authors found complexity trying to creep in. Consider the simple feature to review a message before sending it. Consider also the feature to send the same message to multiple users. These seem "trivial" to implement. Well, perhaps, but they did not make it to the final system.

The lengths to which the authors went to promote true human engineering did not go unrewarded. By most objective measures, the system was an unqualified success: A full 40 percent of the Olympians used the system at least once. It was in operation 24 hours a day and was used an average of one or two times each minute. The authors have been informally asked to make systems for similar events, which include future Olympic games, national meets, and international events.

I heartily recommend this paper. And what about the answer to my opening question? Three.

Henry F. Ledgard, Ph.D., is a consultant, specializing in software engineering audits, education, and human factors. He has written several books on programming style.

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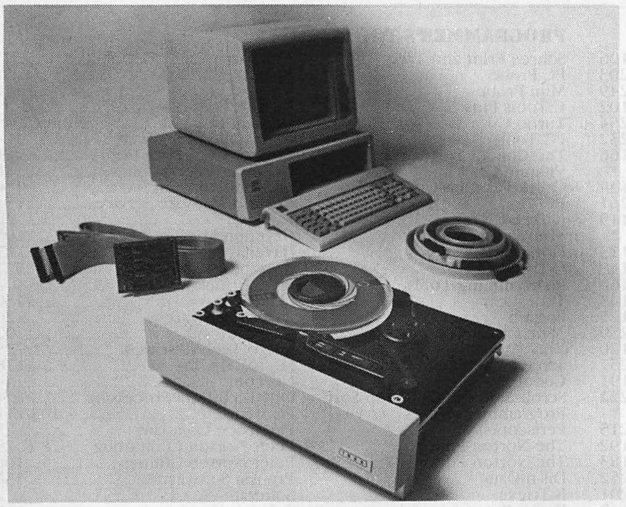

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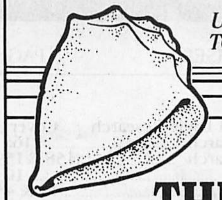

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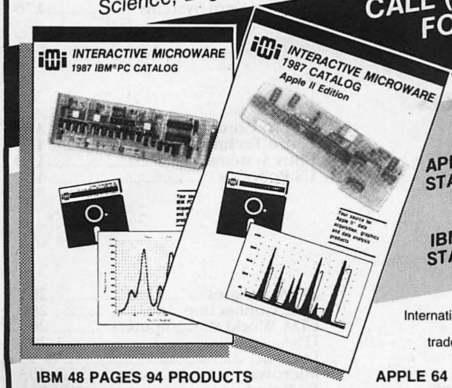

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INDEX TO PRODUCTS

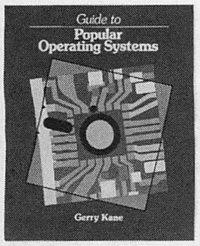
RS#	PRODUCT	ADVERTISER	PAGE
	IBM AND COMPATIBLE PC'S		
116	386 Network Tower	Advanced Logic Research	Cover 3
*	AST Product Line	AST Research	16a-f
*	AST Premium/286	AST Research	158 &159
230	386 System/286 12 Mhz	Atronics	103
*	Personal System/2	IBM	44 & 45
	MULTIFUNCTION/MEMORY CARDS		
*	AST Product Line	AST Research	16a-f
230	Multi-function Card	Atronics	103
187	Above Board	Intel Corporation	107
248	Fast Cache-286/287 Turbo	Microway	117
159	RamQuest	Orchid Technology	37
202	Fastcard	Peripheral Marketing	156
	GRAPHICS CARDS		
206	EGA Wonder	ATI Technologies	72
230	PIB & 12 MHZ	Atronics	103
178	Artist 10/16	Control Systems/Artist	147
242	Hercules Incolor Card	Hercules Computer Tech.	6 & 7
108	LEO	Innovative Data Technology	192
146	Genesis 1024	National Design	52
223	Graphics HPG	Quadram Inc.	60
	MASS STORAGE HARDWARE		
111	9 Track Tape System	Catamount Corporation	192
123	9 Track Tape	Digi Data	172
149	9 Track Tape System	Ibex Computer Systems	195
122	IDEATape	IDEAssociates	123
250	9 Track Tape System	M4 Data	195
185	Nine Track Micro	Overland Data, Inc.	191
170	PCTerminal	Santa Clara Systems	84
219	Data Manager	Seagate Technology	100 & 101
227	Laser View Display	Sigma Designs	54
	PRINTERS-PLOTTERS		
194	J Laser Plus	Tall Tree Systems	35
	MODEMS		
237	208AB Modem/Barr Hasp	Barr Systems	105
238	Smart Modem 9600	Hayes Microcomputer	91-93
	DATA COMMUNICATIONS		
251	PCSS 8	G-Tek	173
	DATA ACQUISITION		
209	Catalogue	Interactive Microware	195
	MONITORS		
138	MJ503	Teknica	64
	MICRO-MINI MAINFRAME COMMUNICATIONS		
239	KB 3270	Keytronics Intl.	96
195	Access 36	Mux Lab	187
	LOCAL AREA NETWORKS		
165	3-N-1	Attachmate Corporation	169
172	Easy Queue	Giltronix	82
103	Link Up-LAN Gateway	Information Technology	153
109	Lan Report	Novell	23
	OTHER COMMUNICATION HARDWARE		
110	Digiboard Com/XI	Digiboard Inc.	179
177	Stargate OC8000	Stargate Technologies	146
	OTHER COMMUNICATION SOFTWARE		
167	Crosstalk	Crosstalk Comm.	Back Cover
245	ASYST	MacMillan Software	50
196	Multi Link Advanced	Software Link	66
	SCIENTIFIC/ENGINEERING SOFTWARE		
254	Eureka	Borland Intl.	Front Cover
112	Generic Cadd/Iges	Generic Software	98
218	EE Designer	Visionics Corp.	165
	LANGUAGES		
136	Prolog Compiler	Arity, Inc.	24
105	Clarion	Barrington Systems	62
133	BBX (Business Basic Extend)	Basis	183
254	Basic, Prolog, Pascal	Borland Intl.	Front Cover
131	C Products	Ecosoft Inc.	129
*	Weiner Shell	Gryphon Microproducts	195
128	F77L Lahey Fortran	Lahey Computer Systems	105
263	Personal Rexx	Mansfield Software	142
*	Language Newsletter	Microsoft Corporation	33
130	Brief	Solution Systems	14

RS#	PRODUCT	ADVERTISER	PAGE
	PROGRAMMER'S TOOLS		
106	Source Print and Tree	Aldebaran	17
203	PC Probe	Atron	8
249	Mini Probe	Atron	16
102	C Tools Plus	Blaise Computing	19
254	Turbo C	Borland Intl.	Front Cover
232	PC Tools	Central Point Software	104
166	The Condor Editor	Condor Computer Corp.	20
*	Vitamin C	Creative Programming	18
144	Quick Pak/Qbase	Crescent Software	180
261	PC/VI	Custom Software Services	154
119	R-Tree/C-Tree	FairCom	22
*	The Weiner Shell	Gryphon Microproducts	195
113	Flowchart	HavenTree Software	137
148	C-Tree Query	Kurtzberg Computer System	177
160	Programming Tools	Lattice, Inc.	102
143	Timeslicer	Lifeboat Associates	150
125	Epsilon	Lugaru Software	126
259	386c Pascal Computers	Metaware	192
120	Xray	Micro Tech Research	25
257	Screen Machine/Mach 2	MicroHelp, Inc.	178
191	Cobol	Norcom	144
222	Scroll & Recall/Opt-Tech Sort	Opt-Tech Data Processing	4
*	Programmer's Tools	PC Brand	108-111
215	Periscope	Periscope Company	5
192	The Norton Editor	Peter Norton Computing	28 & 29
183	The Norton Editor	Peter Norton Utilities	106
252	Dis-n-Data	Pro-Am Software	136
201	B-Trieve	Softcraft	2
142	Demo Program	Software Garden	127
115	Windows for Data	Vermont Creative	21
132	UI Programmer	Wallsoft Systems Inc.	170
	SOFTWARE UTILITIES		
114	Bookmark	Intellisoft Intl.	149
191	Cobol	Norcom	144
157	Software Sentinel	Rainbow Technologies	155
176	Speedstar	Storage Dimensions	126
	GRAPHIC SOFTWARE		
107	Graph C	Scientific Endeavors	192
	ALTERNATE INPUT/OUTPUT DEVICES		
229	Logitech Mouse	Logitech, Inc.	39
	DATA BASE MANAGEMENT SOFTWARE		
153	Magic PC	Aker Corporation	151
*	Paradox 2	Ansa Software	26 & 27
118	DataFlex	Data Access	86
135	DataEase	Data Ease	130 & 131
211	MDBS III	Micro Data Base Systems	88
224	Clipper	Nantucket Corporation	119
*	Db Vista	Raima Corporation	11
156	Unify	Unify Corporation	157
236	ZIM	Zanthe	160 & 161
	OPERATING SYSTEMS		
253	OS/286 and OS/386	AI Architects	143
174	MKS Tool Kit	Mortice Kern Systems	176
	OTHER SERVICES		
*	Little Board/PC	Ampro Computers Inc.	189
124	Teamwork/PCSA	Cadre Technologies Inc.	181
210	PC-AT Board Level	I-Bus Systems	139
226	Career HST	US Robotics	121
	MAIL ORDER		
*	Mail Order	BC Associates	204
147	Mail Order	Byte Connection, Inc.	200
117	Mail Order	CDA World of Computers	200
134	Mail Order	ITS	202
179	Mail Order	Logisoft	12 & 13
*	Mail Order	Microway	203
*	Programmer's Tools	Pc Brand	108-111
175	Mail Order	Programmer's Connection	75-77
173	Mail Order	Programmer's Paradise	201
220	Mail Order	Programmer's Shop	42
162	Mail Order	Programmer's Shop	132 & 133
240	Mail Order	Scantel Systems Ltd.	204
127	Mail Order	Scottsdale Systems	204

Systematic Operation

Although repetitious in its approach, the first book to compare popular operating systems aids the user in moving between microcomputer environments.

Guide to Popular Operating Systems
Gerry Kane (Scott, Foresman and Company, 1986) 200 pages, paper, $19.95



Putting microcomputers to work today requires an understanding of computer software as well as hardware. A firm foundation for understanding software begins with an understanding of computer operating systems: what they are, why they are needed, how they work, and how to work with them. Thus, a book that summarizes, compares, and contrasts the major operating systems would be useful in gaining this understanding.

The appropriately titled *Guide to Popular Operating Systems* by Gerry Kane is such a book. It summarizes operating systems in terms that will be useful to the first-time buyer, the manager who is evaluating different systems, the systems consultant, and even the experienced user who needs to move between computer environments.

The author discusses seven operating systems: Apple-DOS, Apple ProDOS, CP/M, MS-DOS, PC-DOS, the p-System, and UNIX. The book's stated purpose is to shorten the learning curve on a new computer system. Operating systems are discussed from the perspective of the average applications user, not that of the system programmer.

Before inexpensive diskette drives became abundant, there was no need for sophisticated operating systems. It was not until Digital Research's founder, Gary Kildall, released CP/M in 1976 specifically to support IBM's 8-inch diskette drive that an operating system became widespread on the microcomputer. Because most of an end user's interaction with the operating system will involve manipulating diskette or hard-disk files, it is extremely beneficial to understand how an operating system structures and manages its file system.

Basic features of the file system are covered in chapter 2. In it, Mr. Kane discusses file naming; wild-card naming conventions; single, multiple, and hierarchical file directory systems; volumes; and physical devices. The book clearly explains files and directories using a file-cabinet/file-folder analogy, and gives an exhaustive example of file naming conventions. The trade-off between using long file names (harder to manipulate, but more accurate) and short file names (harder to remember, but easier to control) is examined.

The author continues by describing the types of commands that an operating system should provide and develops a theoretical system with "generic" versions of each command. These generic versions consist of a list of desired features or capabilities, which the author has pulled together from the desirable features of all operating systems covered. No single operating system supports all of these features.

The generic commands that are discussed show the directory (or catalog); change devices and directories; and copy, erase (or delete), rename, move, lock, and unlock files. The book describes only those commands that can be issued from the command line. It does not go into system calls issued from within an executing program.

Following chapters on file systems and generic commands are chapters on specific operating systems. Each chapter introduces the particular operating system and the file system it supports, then goes on to compare that system's basic commands with the generic commands developed earlier. Most chapters contain a section that describes the commands unique to that system.

The book makes extensive use of bar charts to compare the "relative power" of different operating system commands. By relative power, Mr. Kane means how many of the desirable generic features he mentioned earlier are included in that particular operating system command. This, admittedly, is a crude method of measuring power within the context of a given operating system. The bar charts are simply not effective: they look almost identical, are repeated to excess, and do not convey information that is essential.

It is also somewhat surprising to see CP/M come out ahead in so many of the comparisons. While CP/M embodies simplicity and usefulness (along with a touch of nostalgia), there can be little doubt that MS-DOS is at least slightly more powerful, and UNIX is undoubtedly the real powerhouse.

The book has a large set of appendixes, including a cross-referenced command summary table (perhaps worth the cost of the book alone), a list of command syntaxes (a rehash of information already contained in the book), a list of common file extension types, and separate appendixes for the error messages most likely to be encountered with each operating system.

The operating system is the single most important element to learn in working with a specific computer. *Guide to Popular Operating Systems* does not try to cover the kind of specific, technical information needed by the programmer, and at times it is repetitious in its comparisons. It is the first book, however, to tackle the task of comparing the important microcomputer operating systems. For the user already familiar with an operating system, but who needs to come up to speed quickly on one of the operating systems covered, or for the user who needs to compare the features of different operating systems, or for the user who wants a useful introduction on how operating systems work and what they do, this book can help.

—DARROW KIRKPATRICK

INDEX TO ADVERTISERS

READER SERVICE NUMBER	ADVERTISER	PAGE
116	Advanced Logic Research	Cover 3
253	A.I. Architects	143
153	Aker	151
106	Aldebaran	17
*	Ampro Computers	189
*	Ansa Software	26 & 27
136	Arity Corporation	24
*	AST Research, Inc.	158 & 159
206	ATI	72
203	Atron	8
249	Atron	16
230	Atronics	103
165	Attachmate	169
237	Barr Systems	105
105	Barrington Systems	62
133	Basis	183
*	BC Associates	204
102	Blaise Computing	19
*	Borland Int'l.	Front Gatefold Cover
254	Borland Int'l.	1
147	Byte Connection	200
124	Cadre Technologies	181
111	Catamount Corp.	192
117	CDA Computer Sales	200
232	Central Point	104
166	Condor Computer Corp.	20
178	Control Systems	147
*	Creative Programming Consultants	18
144	Crescent Software	180
167	Crosstalk Comm.	Back Cover
261	Custom Software Systems	154
118	Data Access Corp.	86
135	Data Ease	130 & 131
110	Digiboard	179
123	Digi Data	172
131	Ecosoft	129
119	FairCom	22
112	Generic Software	98
172	Giltronix	82
*	Gryphon Micro	195
251	G-Tek	173
113	Haven Tree Software Limited	137
238	Hayes Microcomputer	91-93
242	Hercules Computer	6 & 7
149	Ibex	195
*	IBM	44 & 45
210	I-Bus Systems	139
122	IDEassociates	123
103	Information Tech	153
108	Innovative Data Tech	192
187	Intel Corp.	107
114	Intellisoft	149
209	Interactive Microware	195
134	ITS	202
239	Keytronics	96
148	Kurtzberg Computer Systems	177
128	Lahey Computer Systems, Inc.	105
160	Lattice, Inc.	102
143	Lifeboat Assoc.	150
179	Logicsoft	12 & 13
229	LOGITECH Inc.	39
125	Lugaru	126
245	Macmillan Software	50
263	Mansfield Software	142
259	MetaWare, Inc.	192
250	M4 Data	195
211	Micro Data Base Systems	88
257	MicroHelp, Inc.	178
*	Microsoft Corp.	33
120	MicroTec	25
*	MicroWay	203
248	MicroWay	117
174	Mortice Kern	176
195	Mux Lab	187
224	Nantucket Corp.	119
146	National Design	52
191	Norcom	144
109	Novell Data	23
222	Opt-Tech Data Processing	4
159	Orchid Technology	37
185	Overland Data	191
*	PC Brand	108-111
202	Peripheral Marketing	156
215	Perisope Company	5
183	Peter Norton	106
192	Peter Norton	28 & 29
252	Pro/Am	136
175	Programmer's Connection	75-77
173	Programmer's Paradise	201
220	Programmer's Shop	42
162	Programmer's Shop	132 & 133
223	Quadram	60
*	Raima Corp.	11
157	Rainbow Technology	155
170	Santa Clara	84
240	Scantel Systems Ltd.	204
107	Scientific Endeavors	192
127	Scottsdale Systems	204
219	Seagate Tech	100 & 101
227	Sigma Designs	54
201	SoftCraft Inc.	2
142	Software Garden	127
196	Software Link	66
130	Solution Systems	14
177	Stargate Technologies	146
176	Storage Dimensions	126
194	Tall Tree Systems	35
138	Teknika	64
156	Unify Corp.	157
226	U.S. Robotics	121
115	Vermont Creative Software	21
218	Visionics	165
132	Wall Soft	170
236	Zanthe	160 & 161

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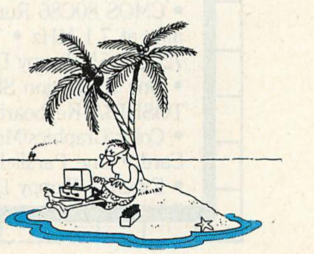

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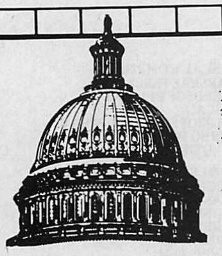

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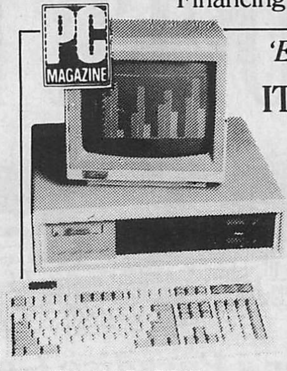

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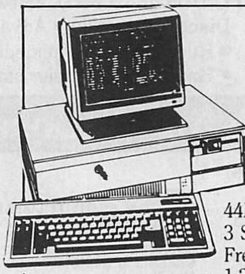

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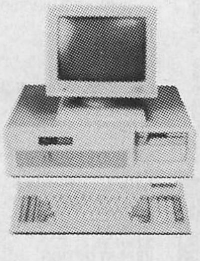

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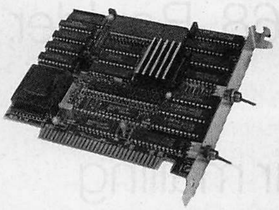

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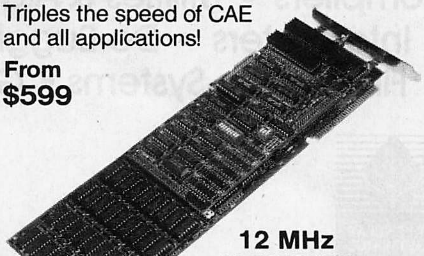

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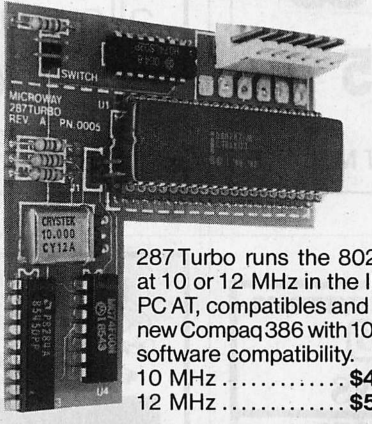

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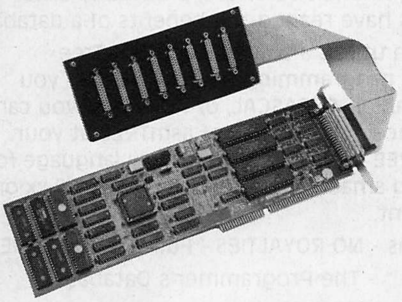

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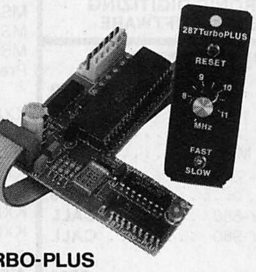

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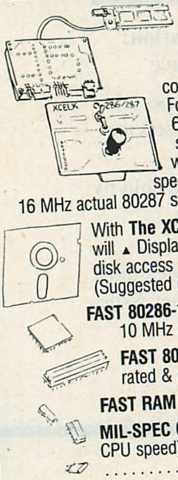

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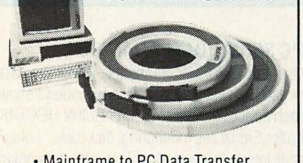

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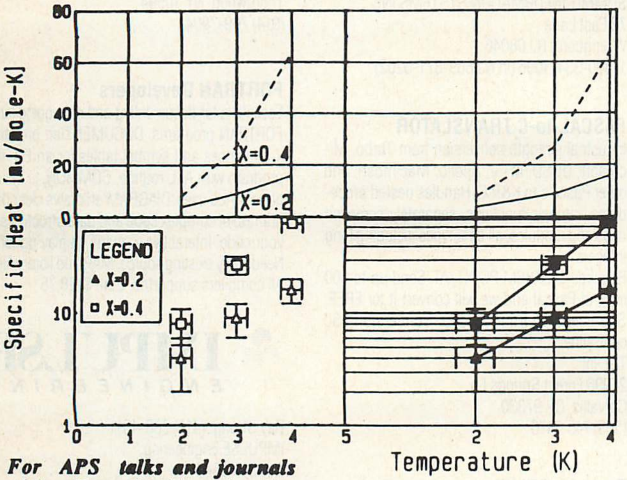

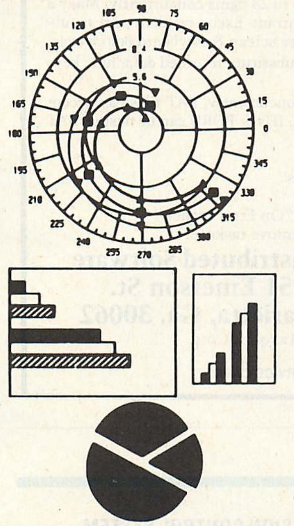

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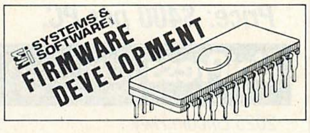

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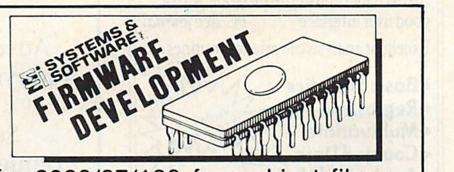

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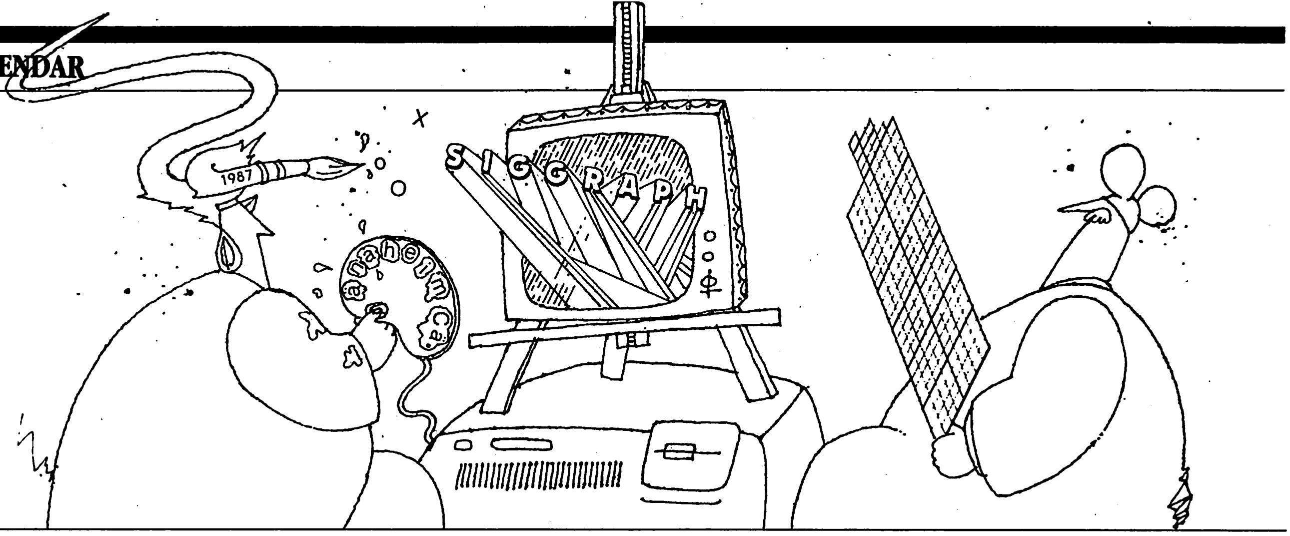

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JULY

July 21–23
Optical Drive and Media Manufacturing Conference
San Francisco, CA (Rothchild Consultants) *Contact:* Judith Hanson, Conference Coordinator, Rothchild Consultants, 256 Laguna Honda Blvd., San Francisco, CA 94116-1496; 415/681-3700

July 27–31
SIGGRAPH '87
Anaheim, CA (ACM SIGGRAPH) *Contact:* SIGGRAPH '87 Conference Management, Smith, Bucklin, and Associates, 111 E. Wacker Dr., Suite 600, Chicago, IL 60601; 312/644-6610

July 29–31
AI and Knowledge-based Systems: Realizing the Potential
San Francisco, CA (Decision Support Technology) *Contact:* Decision Support Technology, Conference Registration Office, 51 Church St., Boston, MA 02116; 800/843-3263; in Massachusetts, 617/482-3596

AUGUST

August 6–7
Microcomputer Security
San Francisco, CA (MIS Training Institute) *Contact:* Michael I. Sobol, MIS Training Institute, 4 Brewster Road, Framingham, MA 01701; 617/879-7999

August 17–20
CAD/CAM '87
Boston, MA (National Computer Graphics Association) *Contact:* National Computer Graphics Association, 2722 Merrilee Drive, Suite 200, Fairfax, VA 22031; 800/225-6242; in Virginia, 703/698-9600

August 19–21
COMDEX/Australia
Sydney, Australia (Interface Group) *Contact:* The Interface Group, Inc., 300 First Ave., Needham, MA 02194; 617/449-6600

August 23–28
IJCAI '87
Milan, Italy (International Joint Conferences on Artificial Intelligence) *Contact:* John McDermott, CS Dept., Carnegie-Mellon University, Pittsburgh, PA 15213; 415/328-3123

August 24–28
AAAI '87
Seattle, WA (American Association for Artificial Intelligence) *Contact:* Lorraine Cooper, AAAI, 445 Burgess, Menlo Park, CA 94025; 415/328-3123

SEPTEMBER

September 1–3
PC EXPO
New York, NY (PC EXPO) *Contact:* Jim Mion, PC EXPO, 333 Sylvan Ave., Englewood Cliffs, NJ 07632; 800/922-0324; in New Jersey, 201/569-8542

September 15–16
Systems Network Architecture
New York, NY (New York University) *Contact:* NYU, School of Continuing Education, Seminar Center, 575 Madison Ave., New York, Ny 10022; 212/580-5200

September 21–23
Software Maintenance
Austin, TX (National Bureau of Standards, DPMA, and IEEE-CS) *Contact:* Roger Martin, National Bureau of Standards, Building 225, Room B266, Gaithersburg, MD 20899; 301/921-3545

September 23–25
***PC Tech Journal* Systems Forum**
San Diego, CA (*PC Tech Journal*) *Contact:* Marti Cunha, *PC Tech Journal*, Suite 800, Little Patuxent Parkway, Columbia, MD 21044; 301/740-8300

September 28–October 1
Conference on Electronic/Desktop Publishing
San Francisco, CA (National Computer Graphics Association) *Contact:* National Computer Graphics Association, 2722 Merrilee Dr., Suite 200, Fairfax, VA 22031; 800/225-6242; in Virginia, 703/698-9600

OCTOBER

October 4–8
OOPSLA '87
Kissimmee, FL (ACM SIGPLAN) *Contact:* Object Oriented Programming: Systems, Languages, and Applications Conference; ACM, 11 W. 42nd St., New York, NY 10036; 212/869-7440

October 5–8
ASPLOS-II
Palo Alto, CA (ACM SIGPLAN) *Contact:* Architectural Support for Programming Languages and Operating Systems Conference, ACM, 11 W. 42nd St., New York, NY 10036; 212/869-7440

October 13–15
PC EXPO/Chicago
Chicago, IL (PC EXPO) *Contact:* Jim Mion, PC EXPO, 333 Sylvan Ave., Englewood Cliffs, NJ 07632; 800/922-0324; in New Jersey, 201/569-8542

October 15–17
Northeast Computer Faire
Boston, MA (Interface Group) *Contact:* The Interface Group, Inc., 300 First Ave., Needham, MA 02194; 617/449-6600

October 20–22
NetWorld '87
Dallas, TX (PC EXPO) *Contact:* Annie Zdinak, PC EXPO, 333 Sylvan Ave., Englewood Cliffs, NJ 07632; 800/526-3247; in New Jersey, 201/569-6409

October 27–29
UNIX EXPO
New York, NY (National Expositions Co.) *Contact:* National Expositions Co., Inc., 49 W. 38th St., Suite 12A, New York, NY 10018; 212/391-9111

October 28–30
AI/East '87
Atlantic City, NJ (Tower Conference Management) *Contact:* Tower Conference Management, 331 W. Wesley St., Wheaton, IL 60187; 312/668-8100

NOVEMBER

November 3–5
COMDEX/Fall
Las Vegas, NV (Interface Group) *Contact:* The Interface Group, Inc., 300 First Ave., Needham, MA 02194; 617/449-6600

November 9–11
Symposium on Operating System Principles
Austin, TX (ACM SIGOPS) *Contact:* Les Belady, MCC, 9430 Research Blvd., Echelon 1, Suite 200, Austin, TX 78759; 512/834-3330

November 9–12
ICCAD-87
Santa Clara, CA (IEEE-CS) *Contact:* International Conference on Computer-aided Design, IEEE-CS, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903; 202/371-0101

DECEMBER

December 1–3
Optical Information Systems '87
New York, NY (Conference Management Corporation) *Contact:* Meckler Publishing, 11 Ferry Lane W, Westport, CT 06880; 203/226-6967

December 6–9
International Conference on Information Systems
Pittsburgh, PA (Society for Information Management) *Contact:* William D. King, Graduate School of Business, University of Pittsburgh, Pittsburgh, PA 15260; 412/648-1587

December 16–18
Microcomputer Graphics '87
New York, NY (Expoconsul International) *Contact:* Expoconsul International, Inc., 3 Independence Way, Princeton, NJ 08540; 609/987-9400

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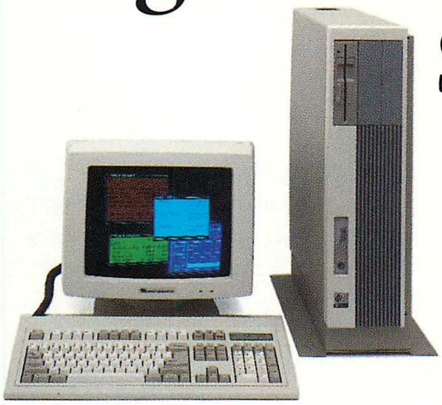

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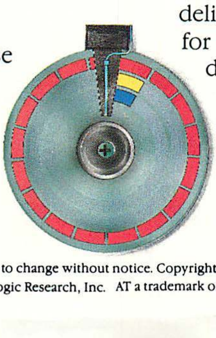

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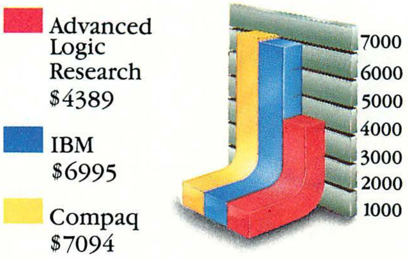

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