CHIPS 82C574
MICROCHANNEL INTERFACE CHIP

- **Compatible with IBM Microchannel specifications**
- **Provides highly integrated Microchannel interface solution**
- **Flexible Card ID assignment**
- **Supports POS registers**
- **Resource relocation capability to avoid address conflict**
- **Flexible Interrupt level selection**
- **Sophisticated Card Channel Ready signal generator.**
- **Two modes of operation:**
  Mode 1 for general purpose 8 bit slave I/O peripherals
  Mode 0 for 82C570 CHIPSLINK application
- **Low power CMOS technology**
- **68 pins PLCC package**

The 82C574 is a highly integrated Microchannel interface chip for IBM PS/2 personal computer application. It can be configured to operate in either of two modes; "**mode 0**" for 82C570 CHIPSLINK 3270 coaxial protocol controller or "**mode 1**" for the 8 bit general purpose IO slave peripherals.

When **mode 0** is selected, the chip decodes the IO address of 02DXH and 022XH for IBM & IRMA registers and generates the $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$ signals for 82C570. It also decodes the memory space of 0CE000 to 0CFFFF for the display buffer and external micro code access by activating the $\overline{\text{MEMRD}}$, $\overline{\text{MEMWR}}$ signals.

In **mode 1** operation, the 82C574 supports the microchannel bus interface to most 8 bit IO slave devices. The adapter IO address can be programmable during the setup procedure. This resource relocation capability avoids conflicts with the adapter's address. The interrupt level can also be selected via software. The 82C574 greatly simplifies the circuitry to interface to the microchannel bus.

The 82C574 is fabricated using advanced CMOS technology and is packaged in a 68 pin PLCC.

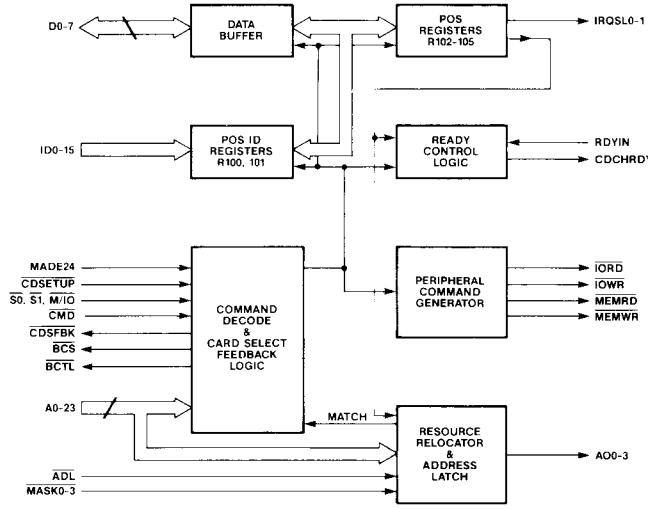
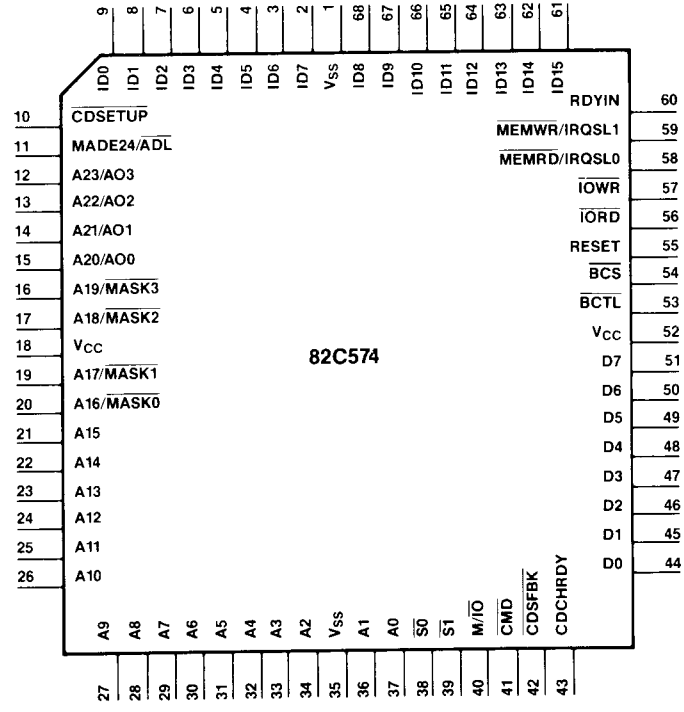


Figure 1. 82C574 Functional Block Diagram


82C574
9 ID0
8 ID1
7 ID2
6 ID3
5 ID4
4 ID5
3 ID6
2 ID7
1 VSS
68 ID8
67 ID9
66 ID10
65 ID11
64 ID12
63 ID13
62 ID14
61 ID15
10 CDSETUP
11 MADE24/ADL
12 A23/AO3
13 A22/AO2
14 A21/AO1
15 A20/AO0
16 A19/MASK3
17 A18/MASK2
18 VCC
19 A17/MASK1
20 A16/MASK0
21 A15
22 A14
23 A13
24 A12
25 A11
26 A10
RDYIN 60
MEMWR/IRQSL1 59
MEMRD/IRQSL0 58
IOWR 57
IORD 56
RESET 55
BCS 54
BCTL 53
VCC 52
D7 51
D6 50
D5 49
D4 48
D3 47
D2 46
D1 45
D0 44
27 A9
28 A8
29 A7
30 A6
31 A5
32 A4
33 A3
34 A2
35 VSS
36 A1
37 A0
38 S0
39 S1
40 M/IO
41 CMD
42 CDSFBK
43 CDCHRDY

82C574 Pin Description

Pin No.	Pin Type	Symbol	Description
61-68 2-9	I I	ID15-8 ID7-0	Adapter Identification bits 15 to 0. ID15 is the most significant bit (MSB) and ID0 is the least significant bit (LSB). The user can select each bit to be 0 or 1 by tying the pin to VCC or VSS. The value of these pins are returned by executing READ ID command during adapter setup operation.
12-15	B	A23-20 /AO3-0	**Mode 0:** A23-20 Address Input. These bits are used for the address decoding of the memory slave device. **Mode 1:** AO3-0 Latched Address Output. These bits are latched by ADL and are used by the peripheral device to address the registers.
16-17 19-20	I I	A19-18 /MASK3-2 A17-16 /MASK1-0	**Mode 0:** A19-16 Address Input. They are used for the address decoding of the memory slave device. **Mode 1:** MASK3-0. Active low mask bits for the comparator of the resource relocator. When the mask bit is on (low), the comparison of the corresponding address input (A3-0) with the card address bits (ADR3-0) is bypassed.
21-34 36-37	I I	A15-2 A1-0	System Address bits 15 to 0. These bits are used for the address decoding of the slave IO or memory device. They are also used to address the POS registers.
38 39	I I	S0 S1	Status bits 0 and 1. These signals indicate the start and the type of channel cycle. It is used with M/IO to generate the memory or IO read and write commands.
40	I	M/IO	Memory/Input Output. When M/IO is high, it indicates a memory cycle. If it is low, it indicates an IO cycle.
41	I	CMD	Active low Command signal to define when data is valid on the data bus. It is used to generate the IO/memory read and write commands and is also used to latch the status signals.

M/IO	S0	S1	Function
0	0	0	Reserved
0	0	1	IO Write
0	1	0	IO Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

82C574 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
10	I	$\overline{\text{CDSETUP}}$	Active low Card Setup enable signal. During configuration and error recovery procedures, $\overline{\text{CDSETUP}}$ becomes active along with IO Read/Write commands to access the POS registers.
11	I	MADE24 /$\overline{\text{ADL}}$	**Mode 0:** MADE24. Active low Memory Address Enable 24. It goes active when a memory cycle is in progress with the memory address less than 16 M. It is used in the memory address decoding. **Mode 1:** $\overline{\text{ADL}}$. Active low Address Decode Latch. It is used to latch the A0-3 address lines.
42	O	$\overline{\text{CDSFBK}}$	Active low Card Select Feedback. This signal goes active when a memory or IO slave device is addressed by the host. It stays inactive during setup cycle.
43	O	CDCHRDY	Card Channel Ready. This signal is used by the slow IO or memory slave device to extend the channel cycle. During setup operation, CDCHRDY always stays active and no bus cycle is extended. The maximum time CDCHRDY can stay inactive is 3 μs.
60	I	RDYIN	Active high Ready Input from IO or memory slave device. For asynchronous extended channel cycle operation, CDCHRDY goes inactive at the beginning of the cycle and stays inactive until a low to high transition is detected on RDYIN pin.
44-51	B	D0-7	System data bit 0 to 7. These bits are used to transfer the data to and from the CPU data bus during the configuration cycle. They are 3 state bidirectional lines.
53	O	$\overline{\text{BCTL}}$	Active low external 74LS245 buffer transfer direction control signal. It becomes active during IO/memory READ operation if POS registers or external IO/memory slave device is addressed.
54	O	$\overline{\text{BCS}}$	Active low 74LS245 buffer chip enable. It goes active if internal POS registers or external IO/memory slave device is addressed. (Either read or write operation.)
55	I	RESET	Active high hardware reset signal to initialize the chip. It should stay high for a minimum period of 500 ns.
56	O	$\overline{\text{IORD}}$	Active low IO read strobe. It is the decoded command from CPU to read the device registers. It goes active only when the external IO slave is addressed.

82C574 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
57	O	$\overline{\text{IOWR}}$	Active low IO write strobe. It is the decoded command from CPU to load the information into the registers of the external addressed IO slave device.
59	O	$\overline{\text{MEMWR}}$ /IRQSL1	**Mode 0:** $\overline{\text{MEMWR}}$. Active low memory write strobe. When active, the 82C570 display buffer is written or the external microcode is downloaded. **Mode 1:** IRQSL1. It is the content of bit 2 of POS register 102H and is used to select the interrupt level.
58	O	$\overline{\text{MEMRD}}$ /IRZSL0	**Mode 0:** $\overline{\text{MEMRD}}$. Active low memory read strobe. When active, the 82C570 display buffer is read. **Mode 1:** IRQSL0. This pin is the content of bit 1 of POS register 102H and is used with IRQSL1 for the interrupt level selection.
18, 52	I	VCC	5V Power supply.
1, 35	I	VSS	Power Supply Ground.

Note:
I = Input
O = Output
B = Bidirectional

82C574 Functional Description

The 82C574 block diagram is illustrated in Fig 1. The chip consists of the following functional blocks:

- POS Registers
- Peripheral Commands and Card Select Feedback Generator
- Resource Relocation Logic
- Card Channel Ready Signal Generator

POS REGISTERS

A total of 6 POS registers are supported by 82C574. These registers can be accessed only during configuration cycle by activating CDSETUP, M/IO to low. The description of each register are as follows:

1.100H: Low Byte ID Register.

Bit	7	6	5	4	3	2	1	0
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

This register is read only. The reading of this register returns the content of pins ID7-ID0.

2.101H: High Byte ID Register.

Bit	7	6	5	4	3	2	1	0
	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Read only register. The content of pins ID15-ID8 is returned when reading this register.

3.102H: Miscellaneous Register.

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	RDYCTL	IRQSL1	IRQSL0	CDEN

Bits 7-4 are unused. The reading of these bits are "1". Bit 3 RDYCTL is used in **mode 1** to control the CDCHRDY signal generation. A "0" selects the synchronous extended channel cycle. A "1" selects the asynchronous extended cycle.

Bit 2-1 IRQSL1 and IRQSL0. They are used in **mode 1** with the external 72LS156 demultiplexer to select the interrupt level.

Bit 0 Card Enable control bit. When this bit is "0", the adapter is disabled. 82C574 responds only to setup IO read and write operations. It does not respond to the access of peripheral IO registers or memory.

Register 102H is readable and writable. All the bits are reset to "0" by RESET signal.

4.103H: Low Byte Card Address Register.

Bit	7	6	5	4	3	2	1	0
	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

5.104H: High Byte Card Address Register.

Bit	7	6	5	4
	ADR15	ADR14	ADR13	ADR12

Bit	3	2	1	0
	ADR11	ADR10	ADR9	ADR8

The Card Address registers are read/write registers. They are used for resource relocation to avoid the adapter conflict. In case of the same adapter address, the host can reassign the board address. These two registers are used in **mode 1** operation. To generate the IO read/write commands for the peripheral or to activate the CDSFBK or inactivate the CDCHRDY signals, the address from host A15 to A4 have to match ADR15 to ADR4, A3 to A0 may bypass the comparison with ADR3 to ADR0 if the individual mask bit is activated by forcing MASK3-0 pins to VSS. ADR15 is the most significant bit (MSB) and ADR0 is the least significant bit (LSB).

6.105H: Mode Select Register.

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	MODSL3	MODSL2	MODSL1	MODSL0

Bits 4-7 are unused. The reading of these bits are "1". Bits 3-0 are used to select operation modes. Pattern 1010 is for **mode 1**: General Purpose 8 Bit I/O Slave Peripheral application. All other combinations of bit pattern are for **mode 0** operation: 82C570 CHIPSLINK application. RESET signal resets all the bits to "0" which is **mode 0** operation.

Register 105H is a read/write register.

PERIPHERAL COMMANDS AND CARD SELECT FEEDBACK GENERATOR

The peripheral read/write command is generated by decoding the IO or memory address, M/IO, S0, S1 status and gating with CMD signal.

Mode 0:

In this mode, both IO and memory operations are supported. For IO operation, the decoding of IO address 02DXH or 022XH will activate the IORD if S0 = 1 and S1 = 0 or IOWR if S0 = 0 and S1 = 1. For memory operation, the decoding of memory space of 0CE000 to 0CFFFF will generate MEMRD or MEMWR commands.

Mode 1:

The IO operation is supported in this mode. To generate the IO read/write commands, the address from host needs to match the relocation card address programmed in POS registers. (A0-A3 comparison can be bypassed by activating MASK3 to MASK0 individually.)

The Card Select Feedback (CDSFBK) is used to inform the host that the adapter is selected. It stays inactive during setup cycle. It is generated by decoding the IO address space and S0, S1 status. It should go active within 50 ns after Address, M/IO, MADE24 become valid and within 25 ns from the time status becomes active.

RESOURCE RELOCATION LOGIC

The resource relocation capability is supported in **mode 1**. The operation of this block was described in the POS REGISTERS section.

CARD CHANNEL READY GENERATOR

The basic channel cycle time in IBM PS/2 system is 200 ns. It can be extended by using CDCHRDY signal. There are two ways to extend the cycle: Synchronously or Asynchronously.

Mode 0:

When the host addresses the IO space of 02DXH or 022XH, the CDCHRDY will go low within 55 ns from the time M/IO, Address become valid (25 ns from the time status S0, S1 becomes valid) and then return to high within 25 ns after CMD becomes active. The bus cycle is extended from 200 ns to 300 ns, this is called synchronously extended.

If the host accesses the memory space of 0CE000 to 0CFFFF, CDCHRDY will go inactive just like IO access but it will stay low until a low to high transition on pin RDYIN is detected. This is called asynchronously extended bus cycle.

Mode 1:

The bus extention can be done in either way by programming the RDYCTL bit in POS register. If this bit is "0", the bus cycle is extended synchronously to 300 ns. A "1" in this bit will extend the cycle asynchronously.

APPLICATION

Figure 2 shows the application diagram for 82C570 CHIPSLINK 3270 protocol controller. The Card ID is selected by tying ID0 to ID15 pins to VCC or VSS. This provides a flexible choice. RDYIN from 82C570 is used to control the bus cycle for dual port RAM access. D0-7 are used during setup cycle. The 82C574 also provides the 74LS245 buffer chip select and direction control signals. Due to the high integration of both 82C574 and 82C570, only a few components are required to implement the solution for micro to mainframe communication in microchannel environment.

Figure 3 shows the application diagram for the 8 bit IO slave peripherals. In this mode, the resource relocation capability is provided. The interrupt level can be selected by software during setup cycle. The address 0 to 3 are also latched by the 82C574 for the peripherals.

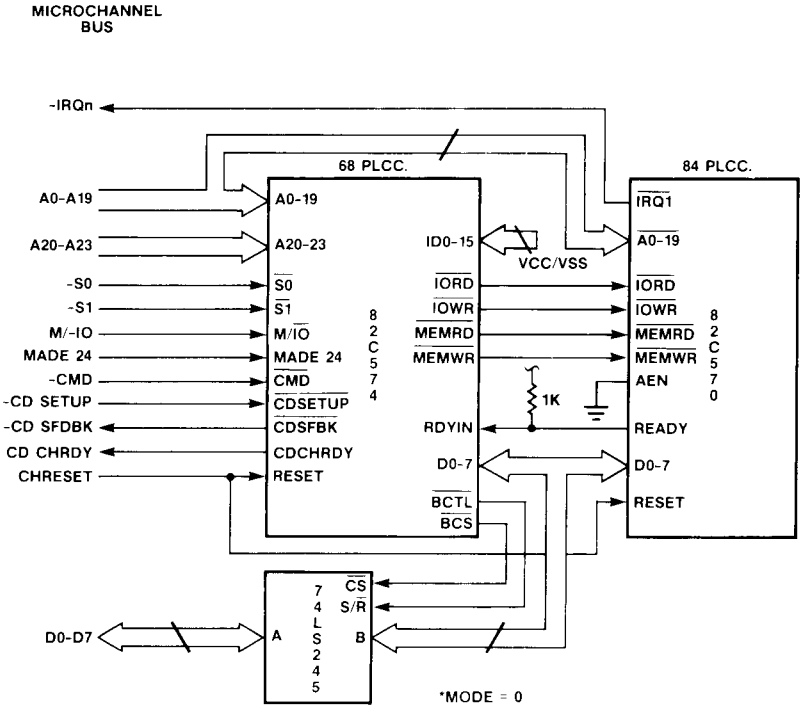


Figure 2. 82C574 Application Diagram for 82C570 CHIPSLink

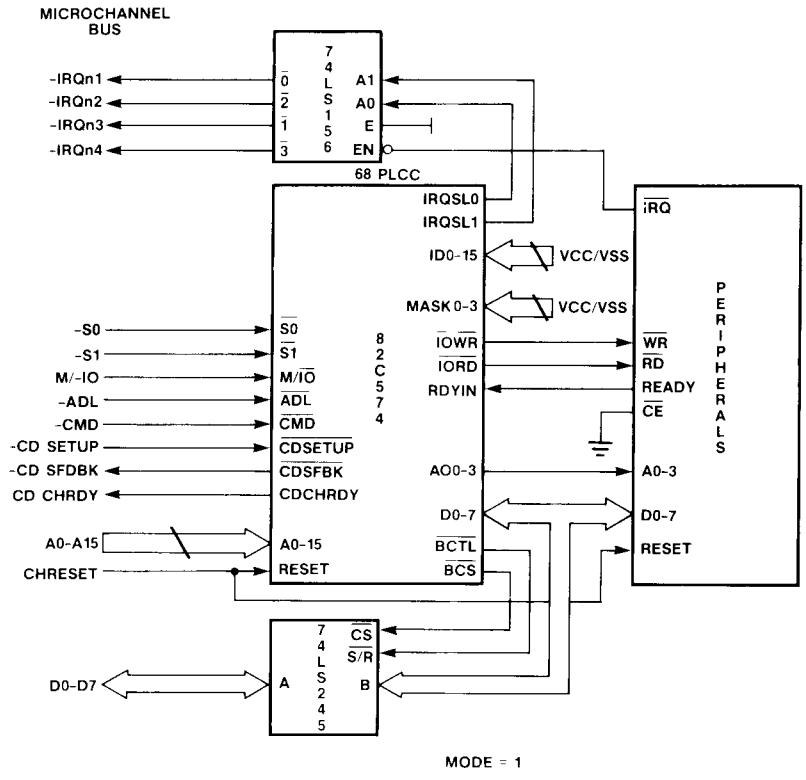


Figure 3. 82C574 Application Diagram for 8 Bit I/O Slave Peripherals

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	—	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-40	125	°C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

82C574 Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C574 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Power Supply Current	I_{CC}	—	30	mA
Input Low Voltage	V_{IL}	-0.5	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC}+0.5	V
Output Low Voltage (Note 1)	V_{OL}	—	0.4	V
Output High Voltage (Note 1)	V_{OH}	2.4	—	V
Input Leakage Current For V_{IN} = 0 to V_{CC}	I_{IL}	-10	10	μA
Output Tri-State Leakage Current For V_O = 0 to V_{CC}	I_{IL}	-10	10	μA

Note 1: I_{OL} = 6 mA I_{OH} = -2 mA for pins CDCHRDY, $\overline{\text{CDSFBK}}$.
I_{OL} = 2.4 mA I_{OH} = -400 μA for all other pins.

Capacitance (T_A = 25°C, V_{CC} = 0)

Parameter	Symbol	Min.	Max.	Units
Input Capacitance For F_C = 1 MHz	C_{IN}	—	10	pF
Output Capacitance	C_{OUT}	—	20	pF
I/O Capacitance	$C_{I/O}$	—	20	pF

82C574 AC Characteristics

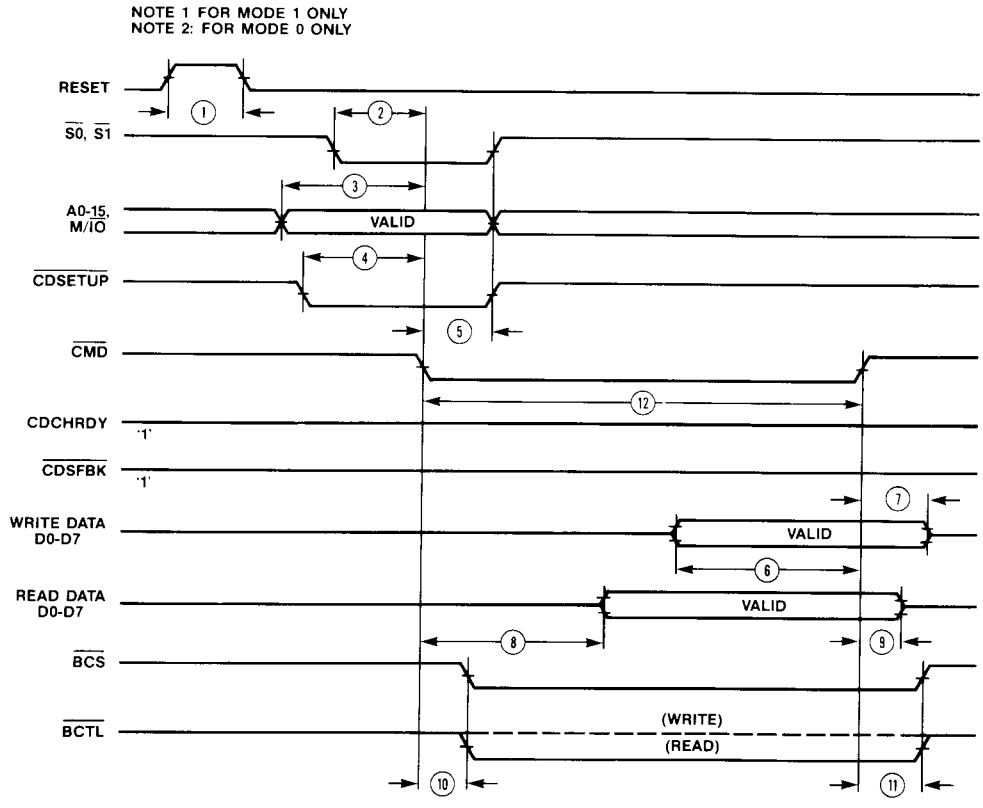
(T_A = 0°C to 70°C, V_{CC} = 5V ±5%, CL = 60 pF for all the output pins)

Sym	Description	Min.	Typ.	Max.	Units
t1	RESET Active Pulse Width	500			ns
t2	$\overline{S0}$, $\overline{S1}$, Set-up to $\overline{CMD}$ Active	50			ns
t3	A0-23, M/$\overline{IO}$, MADE24 Set-up to $\overline{CMD}$ Active	80			ns
t4	$\overline{CDSETUP}$ Set-up to $\overline{CMD}$ Active	50			ns
t5	$\overline{S0}$, $\overline{S1}$, A0-23, M/$\overline{IO}$, $\overline{CDSETUP}$, MADE24 Hold time from $\overline{CMD}$ Active	25			ns
t6	Write Data Set-up to $\overline{CMD}$ Inactive	30			ns
t7	Write Data Hold time from $\overline{CMD}$ Inactive	15			ns
t8	Read Data Delay from $\overline{CMD}$ Inactive			40	ns
t9	Read Data Hold time from $\overline{CMD}$ Inactive	5			ns
t10	$\overline{BCS}$, $\overline{BCTL}$ Assert Delay from $\overline{CMD}$ Active			28	ns
t11	$\overline{BCS}$, $\overline{BCTL}$ Deassert Delay from $\overline{CMD}$ Inactive	5		36	ns
t12	$\overline{CMD}$ Active Pulse Width in SETUP Cycle	90			ns
t21	$\overline{ADL}$ Active to $\overline{CMD}$ Active	40			ns
t22	AO0-3 Delay from $\overline{ADL}$ Active	0		30	ns
t23	$\overline{CDSFBK}$ Active Delay from Address, M/$\overline{IO}$, MADE24 Valid			50	ns
t24	$\overline{CDSFBK}$ Active Delay from Status Active			25	ns
t25	CDCHRDY Inactive Delay from Status Active			25	ns
t26	CDCHRDY Inactive Delay from Address, M/$\overline{IO}$, MADE24 Valid			55	ns
t27	CDCHRDY Release Delay from $\overline{CMD}$ Active in Synchronous Extended Cycle			25	ns

82C574 AC Characteristics (Continued)
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, CL = 60 pF for all the output pins)

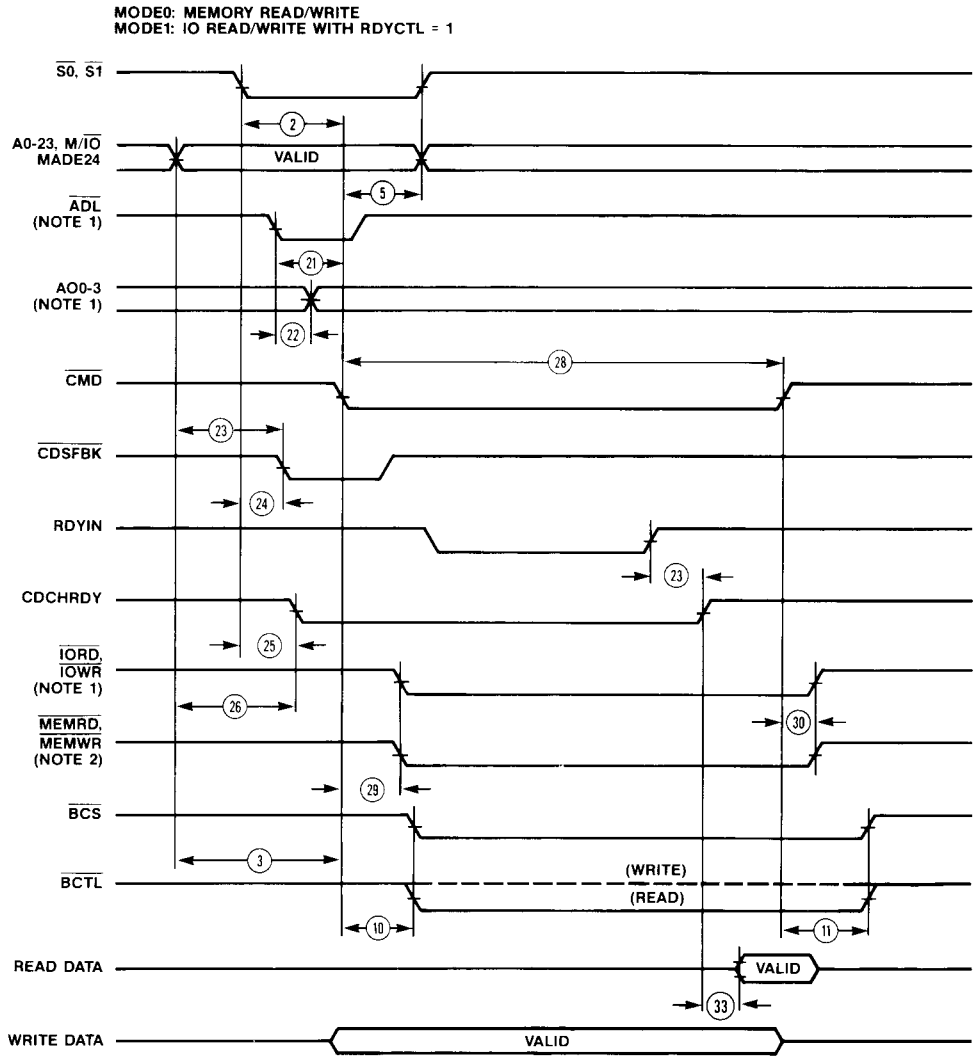
Sym	Description	Min.	Typ.	Max.	Units
t28	$\overline{CMD}$ Active Pulse Width in both Sync and Asyn Extended Cycles	190			ns
t29	$\overline{IORD}$, $\overline{IOWR}$, $\overline{MEMRD}$, $\overline{MEMWR}$ Active Delay from $\overline{CMD}$ Active			18	ns
t30	$\overline{IORD}$, $\overline{IOWR}$, $\overline{MEMRD}$, $\overline{MEMWR}$ Inactive Delay from $\overline{CMD}$ Inactive			18	ns
t31	READ DATA Valid from $\overline{CMD}$ Active in Sync Extended Cycle			140	ns
t32	CDCHRDY Release Delay from RDYIN Active			25	ns
t33	READ DATA Valid from CDCHRDY Active in Asyn Extended Cycle			40	ns

82C574 Timing Diagram



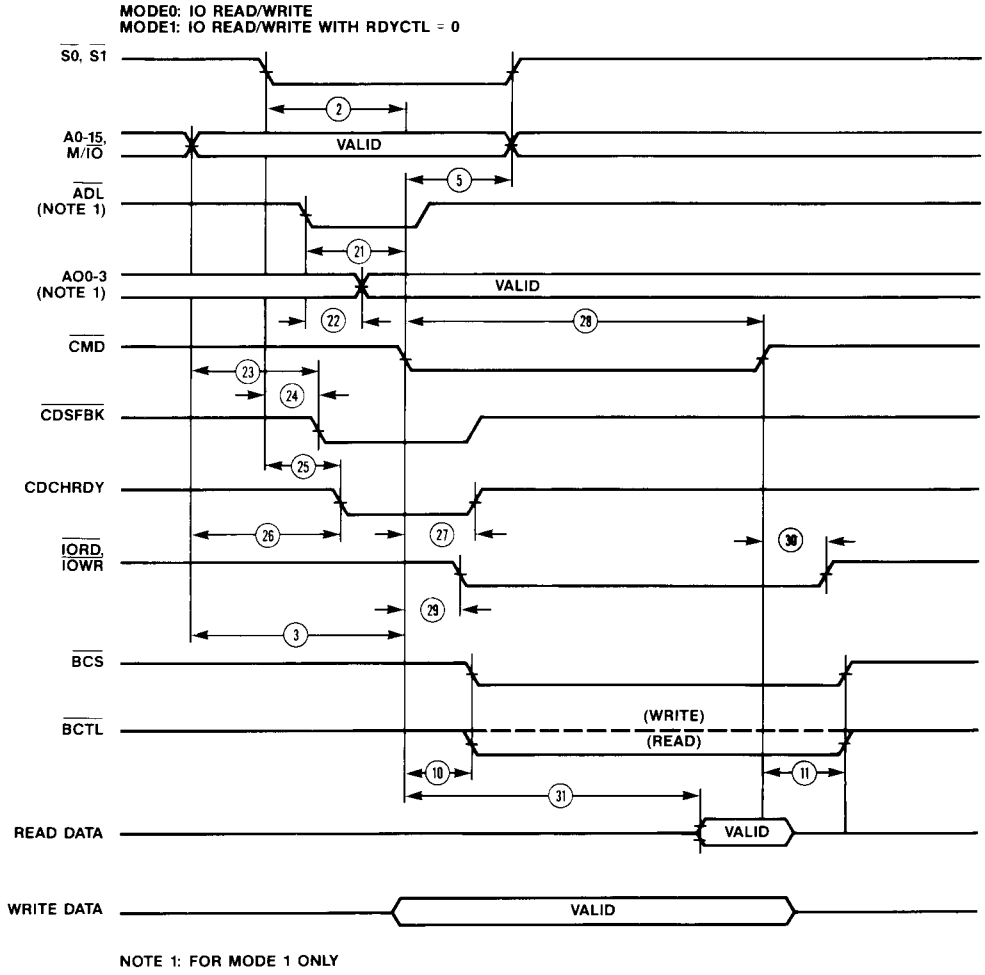
POS Register Setup Cycle Timing

82C574 Timing Diagram (Continued)



Asynchronous Extended Cycle Timing

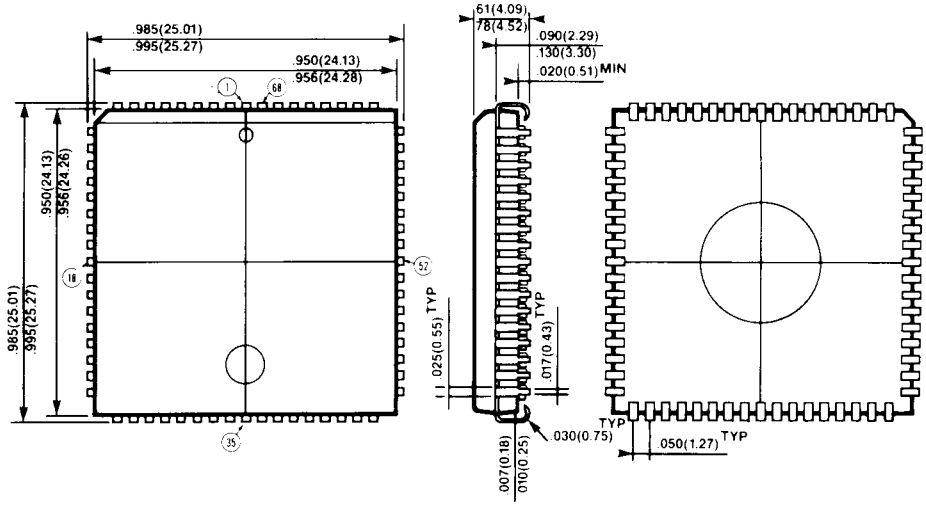
82C574 Timing Diagram (Continued)



NOTE 1: FOR MODE 1 ONLY

Synchronous Extended Cycle Timing

68-PIN PLASTIC LEADED CHIP CARRIER



Ordering Information

Order Number	Package Type
P82C574	PLCC-68

Note:
1. PLCC = Plastic Leaded Chip Carrier