# HM511665 Series — Preliminary

**65,536-Word x 16-Bit Dynamic Random Access Memory**

## ■ DESCRIPTION

The Hitachi HM511665 are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511665 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511665 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511665 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

## ■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....TBD
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- Write per Bit Capability
- 256 Refresh Cycles .....(4 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

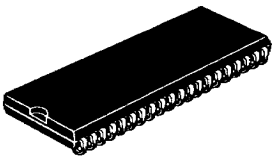
## ■ ORDERING INFORMATION

| Part No. | Access Time | Package |
|---|---|---|
| HM511665JP-8<br>HM511665JP-10 | 80 ns<br>100 ns | 400 mil 40-pin<br>Plastic SOJ<br>(CP-40D) |
| HM511665ZP-8<br>HM511665ZP-10 | 80 ns<br>100 ns | 475 mil 40-pin<br>Plastic ZIP<br>(ZP-40) |

## ■ PIN DESCRIPTION

| Pin Name | Function |
|---|---|
| $A_0$–$A_7$ | Address Input<br>Refresh Address Input |
| $W1/I/O_1$–$W16/I/O_{16}$ | Write Select/Data-in/Data-out |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WB}/\overline{WE}$ | Write per Bit/Read/Write Enable |
| $\overline{WB}/\overline{WE}$ | Write per Bit/Read/Write Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| NC | No Connection |

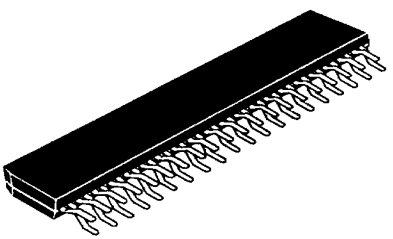
HM511665JP Series



3DCP40D

(CP-40D)

HM511665ZP Series

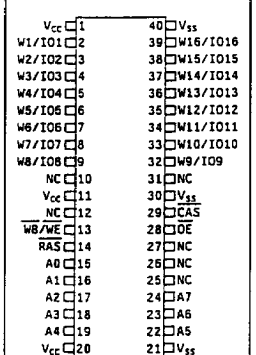


3DZP40

(ZP-40)

## ■ PIN OUT

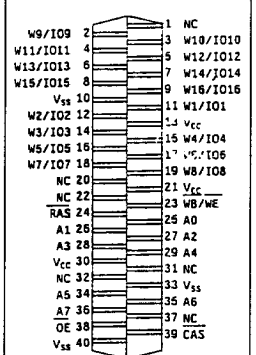
HM511665JP Series




0075-1

(Top View)

HM511665ZP Series




0075-2

(Bottom View)

## ■ TRUTH TABLE

| Inputs | | | | I/O | Operation |
|---|---|---|---|---|---|
| $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WB}/\overline{WE}$ | $\overline{OE}$ | $W1/I/O_1$–$W16/I/O_{16}$ | |
| H | H | H | H | High-Z | Standby |
| L | H | H | H | High-Z | Refresh |
| L | L | H | L | $D_{out}$ | Read |
| L | L | L | H | $D_{in}$ | Write |
| L | L | H | H | High-Z | |

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$ | −1.0 to +7.0 | V |
| Supply Voltage Relative to $V_{SS}$ | $V_{CC}$ | −1.0 to +7.0 | V |
| Short Circuit Output Current | $I_{out}$ | 50 | mA |
| Power Dissipation | $P_T$ | 0.8 | W |
| Operating Temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C |

## ■ ELECTRICAL CHARACTERISTICS

### • Recommended DC Operating Conditions ($T_A$ = 0 to +70°C)

| Parameter | | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{SS}$ | 0 | 0 | 0 | V | |
| | | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| Input High Voltage | | $V_{IH}$ | 2.4 | — | 6.5 | V | 1 |
| Input Low Voltage | (Wi/I/Oi Pin) | $V_{IL}$ | −0.5 | — | 0.8 | V | 1, 2 |
| | (Others) | $V_{IL}$ | −1.0 | — | 0.8 | V | 1, 2 |

Notes: 1. All voltage referenced to $V_{SS}$.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

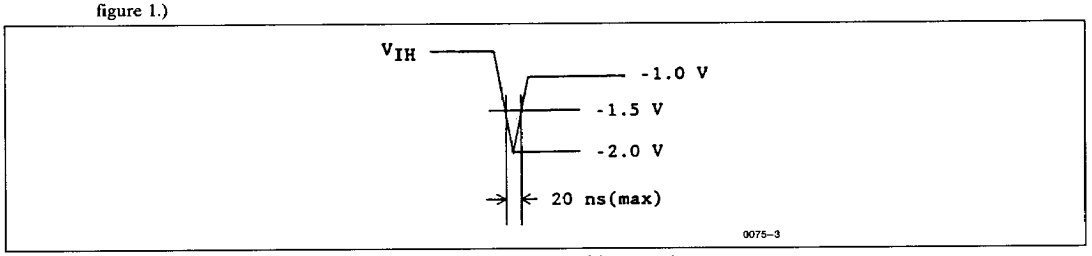



Figure 1. Undershoot of input voltage

## • DC Electrical Characteristics ($T_A$ = 0 to +70°C, $V_{CC}$ = 5V ±10%, $V_{SS}$ = 0V)

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | | |
| Operating Current | $I_{CC1}$ | TBD | | | | mA | $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}$ = Min | 1, 2 |
| Standby Current | $I_{CC2}$ | 2 | | | | mA | TTL Interface $\overline{RAS}$, $\overline{CAS}$ = $V_{IH}$, $D_{out}$ = High-Z | |
| | | 1 | | | | mA | CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ $V_{CC}$ − 0.2V, $D_{out}$ = High-Z | |
| $\overline{RAS}$ Only Refresh Current | $I_{CC3}$ | TBD | | | | mA | $t_{RC}$ = Min | 2 |
| Standby Current | $I_{CC5}$ | TBD | | | | mA | $\overline{RAS}$ = $V_{IH}$, $\overline{CAS}$ = $V_{IL}$, $D_{out}$ = Enable | 1 |
| $\overline{CAS}$ Before $\overline{RAS}$ Refresh Current | $I_{CC6}$ | TBD | | | | mA | $t_{RC}$ = Min | |
| Fast Page Mode Current | $I_{CC7}$ | TBD | | | | mA | $t_{PC}$ = Min | 1, 3 |
| Input Leakage Current | $I_{LI}$ | − 10 | 10 | − 10 | 10 | µA | 0V ≤ $V_{in}$ ≤ 6.5V | |
| Output Leakage Current | $I_{LO}$ | − 10 | 10 | − 10 | 10 | µA | 0V ≤ $V_{out}$ ≤ 5.5V, $D_{out}$ = Disable | |
| Output High Voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High $I_{out}$ = − 2.5 mA | |
| Output Low Voltage | $V_{OL}$ | 0 | 0.4 | 0 | 0.4 | V | Low $I_{out}$ = 2.1 mA | |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected, $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less while $\overline{CAS}$ = $V_{IH}$.

## • Capacitance ($T_A$ = 25°C, $V_{CC}$ = 5V ±10%)

| Parameter | Symbol | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Capacitance (Address) | $C_{I1}$ | — | 5 | pF | 1 |
| Input Capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output Capacitance (Data-in, Data-out) | $C_{I/O}$ | — | 7 | pF | 1, 2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable $D_{out}$.

## • AC Characteristics ($T_A$ = 0 to +70°C, $V_{CC}$ = 5V ±10%, $V_{SS}$ = 0V)[1, 14, 15]

### Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 135 | — | 170 | — | ns | |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 45 | — | 60 | — | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 80 | 10000 | 100 | 10000 | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 30 | 10000 | 40 | 10000 | ns | |
| Row Address Setup Time | $t_{ASR}$ | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RAH}$ | 10 | — | 10 | — | ns | |
| Column Address Setup Time | $t_{ASC}$ | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CAH}$ | 15 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 50 | 20 | 60 | ns | 8 |
| $\overline{RAS}$ to Column Address Delay Time | $t_{RAD}$ | 15 | 35 | 15 | 45 | ns | 9 |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 30 | — | 40 | — | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 80 | — | 100 | — | ns | |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | 10 | — | 10 | — | ns | |
| $\overline{OE}$ to $D_{in}$ Delay Time | $t_{ODD}$ | 15 | — | 15 | — | ns | |
| $\overline{OE}$ Delay Time from $D_{in}$ | $t_{DZO}$ | 0 | — | 0 | — | ns | |
| $\overline{CAS}$ Setup Time from $D_{in}$ | $t_{DZC}$ | 0 | — | 0 | — | ns | |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 50 | 3 | 50 | ns | 7 |
| Refresh Period | $t_{REF}$ | — | 4 | — | 4 | ms | |

### Read Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | — | 80 | — | 100 | ns | 2, 3 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | — | 30 | — | 40 | ns | 3, 4, 13 |
| Access Time from Address | $t_{AA}$ | — | 45 | — | 55 | ns | 3, 5, 13 |
| Access Time from $\overline{OE}$ | $t_{OAC}$ | — | 30 | — | 40 | ns | |
| Read Command Setup Time | $t_{RCS}$ | 0 | — | 0 | — | ns | |
| Read Command Hold Time to $\overline{CAS}$ | $t_{RCH}$ | 0 | — | 0 | — | ns | |
| Read Command Hold Time to $\overline{RAS}$ | $t_{RRH}$ | 0 | — | 0 | — | ns | |
| Column Address to $\overline{RAS}$ Lead Time | $t_{RAL}$ | 45 | — | 55 | — | ns | |
| Output Buffer Turn-off Time | $t_{OFF1}$ | 0 | 20 | 0 | 20 | ns | 6 |
| Output Buffer Turn-off to $\overline{OE}$ | $t_{OFF2}$ | 0 | 15 | 0 | 15 | ns | 6 |
| $\overline{CAS}$ to $D_{in}$ Delay Time | $t_{CDD}$ | 20 | — | 20 | — | ns | |
| $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | $t_{ROH}$ | 10 | — | 10 | — | ns | |

### Write Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Write Command Setup Time | $t_{WCS}$ | 0 | — | 0 | — | ns | 10 |
| Write Command Hold Time | $t_{WCH}$ | 15 | — | 15 | — | ns | |
| Write Command Pulse Width | $t_{WP}$ | 15 | — | 15 | — | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 20 | — | 20 | — | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 20 | — | 20 | — | ns | |
| Data-in Setup Time | $t_{DS}$ | 0 | — | 0 | — | ns | 11 |
| Data-in Hold Time | $t_{DH}$ | 15 | — | 15 | — | ns | 11 |

### Read-Modify-Write Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Read-Modify-Write Cycle Time | $t_{RWC}$ | 185 | — | 220 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ Delay Time | $t_{RWD}$ | 105 | — | 125 | — | ns | 10 |
| $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{CWD}$ | 55 | — | 65 | — | ns | 10 |
| Column Address to $\overline{WE}$ Delay Time | $t_{AWD}$ | 70 | — | 80 | — | ns | 10, 13 |
| $\overline{OE}$ Hold Time from $\overline{WE}$ | $t_{OEH}$ | 15 | — | 15 | — | ns | |

### Refresh Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle) | $t_{CSR}$ | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle) | $t_{CHR}$ | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time | $t_{RPC}$ | 10 | — | 10 | — | ns | |
| $\overline{CAS}$ Precharge Time in Normal Mode | $t_{CPN}$ | 10 | — | 10 | — | ns | |

### Fast Page Mode Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Fast Page Mode Cycle Time | $t_{PC}$ | 55 | — | 65 | — | ns | |
| Fast Page Mode $\overline{CAS}$ Precharge Time | $t_{CP}$ | 10 | — | 10 | — | ns | |
| Fast Page Mode $\overline{RAS}$ Pulse Width | $t_{RASC}$ | 80 | 100000 | 100 | 100000 | ns | 12 |
| Access Time from $\overline{CAS}$ Precharge | $t_{ACP}$ | — | 45 | — | 55 | ns | 3, 13 |
| $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | $t_{RHCP}$ | 45 | — | 55 | — | ns | |
| Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | $t_{CPW}$ | 70 | — | 80 | — | ns | |
| Fast Page Mode Read-Modify-Write Cycle Time | $t_{PCM}$ | 100 | — | 110 | — | ns | |

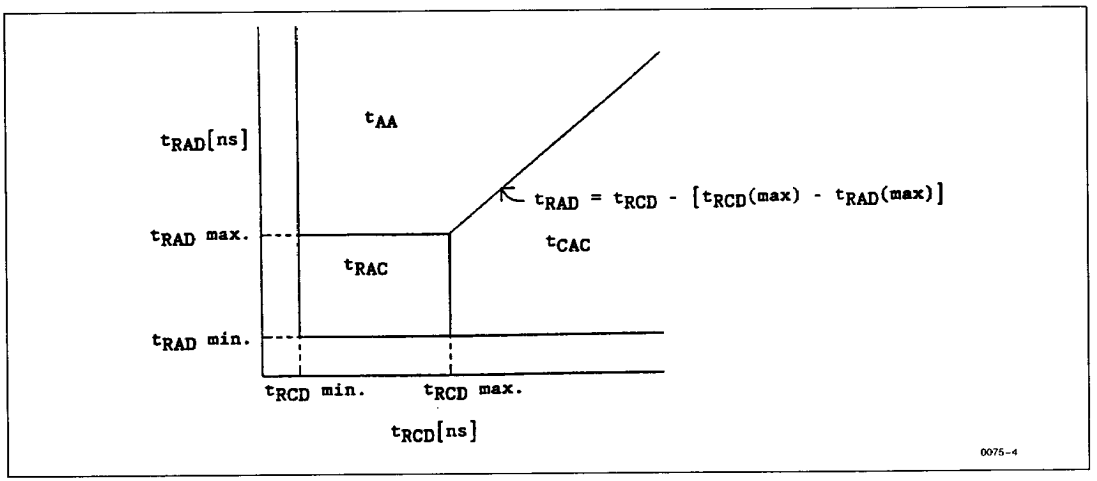
### Counter Test Cycle

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $\overline{CAS}$ Precharge Time in Counter Test Cycle | $t_{CPT}$ | 40 | — | 40 | — | ns | |

### Write per Bit Cycle[16, 17]

| Parameter | Symbol | HM511665-8 | | HM511665-10 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Write per Bit Setup Time | $t_{WBS}$ | 0 | — | 0 | — | ns | |
| Write per Bit Hold Time | $t_{WBH}$ | 10 | — | 10 | — | ns | |
| Write per Bit Selection Setup Time | $t_{WDS}$ | 0 | — | 0 | — | ns | |
| Write per Bit Selection Hold Time | $t_{WDH}$ | 10 | — | 10 | — | ns | |

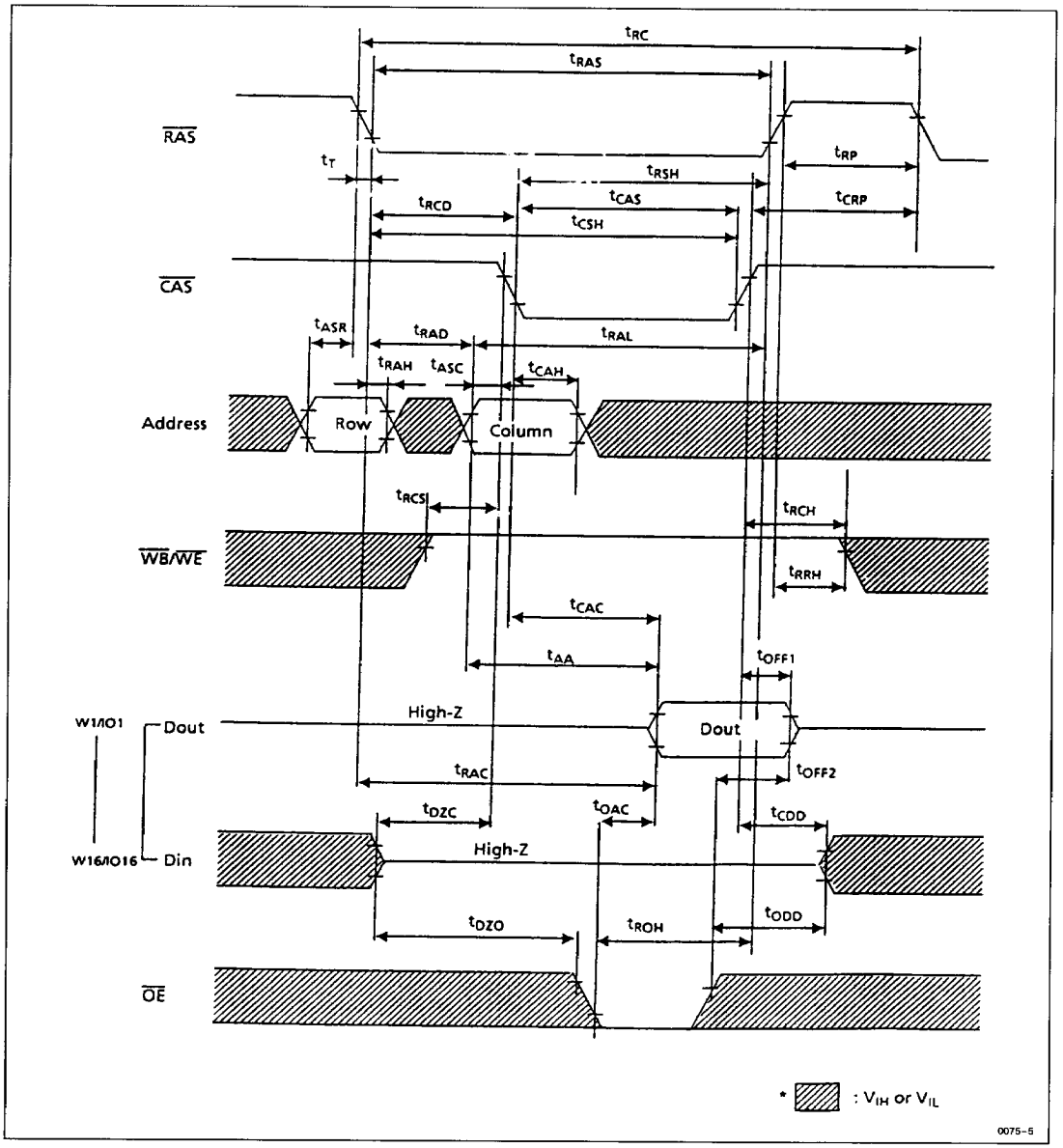
Notes: 1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. $t_{RAC}$, $t_{CAC}$, and $t_{AA}$ are determined as follows.




6. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
8. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only, if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
9. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only, if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
10. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$ and $t_{AWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to CAS leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. $t_{RASC}$ defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of $t_{AA}$ or $t_{CAC}$ or $t_{ACP}$.
14. An initial pause of 100 $\mu$s is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
17. The data bits to which the write operation is applied can be specified by keeping Wi/I/Oi high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

## ■ TIMING WAVEFORMS

• Read Cycle



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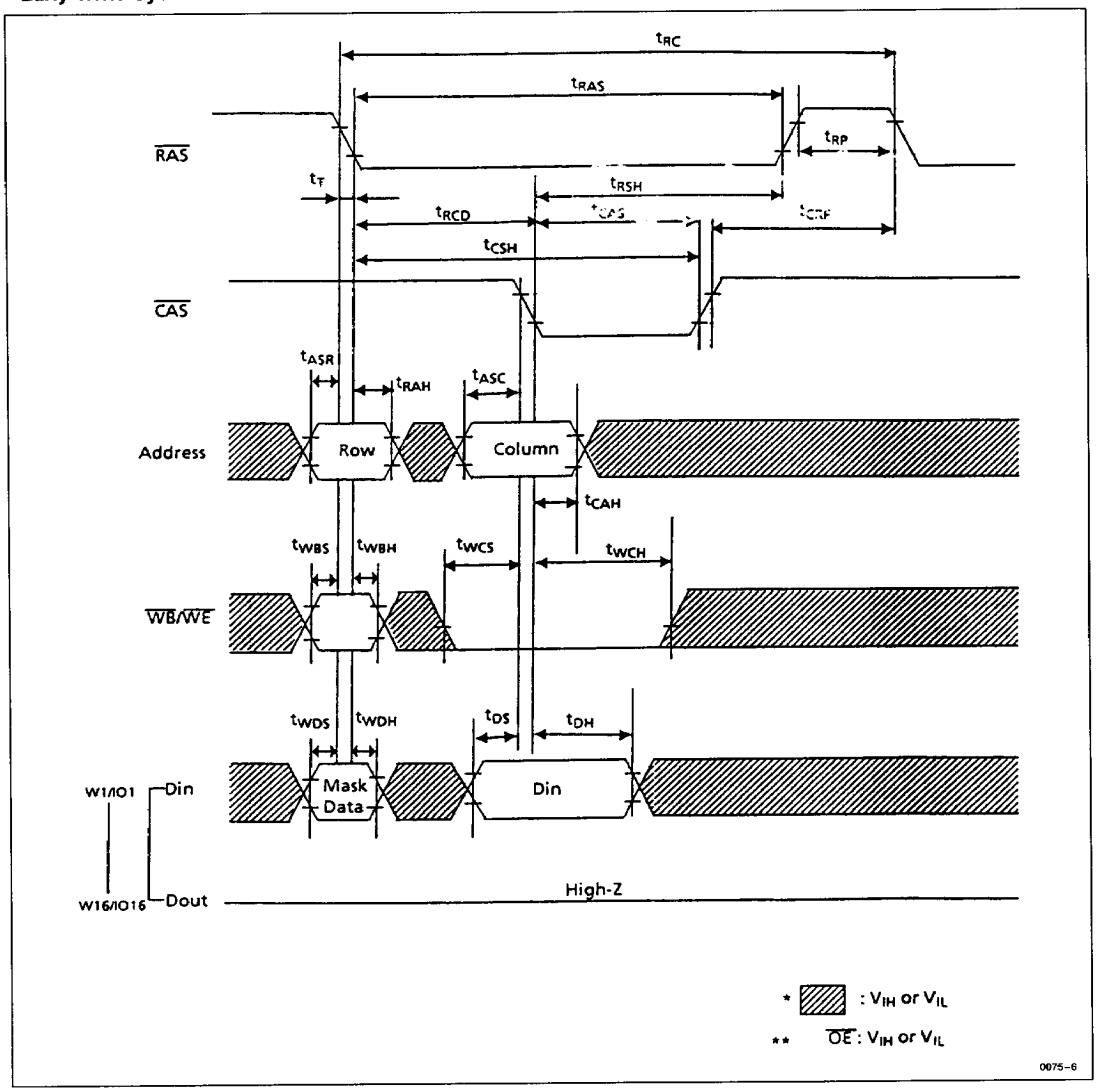
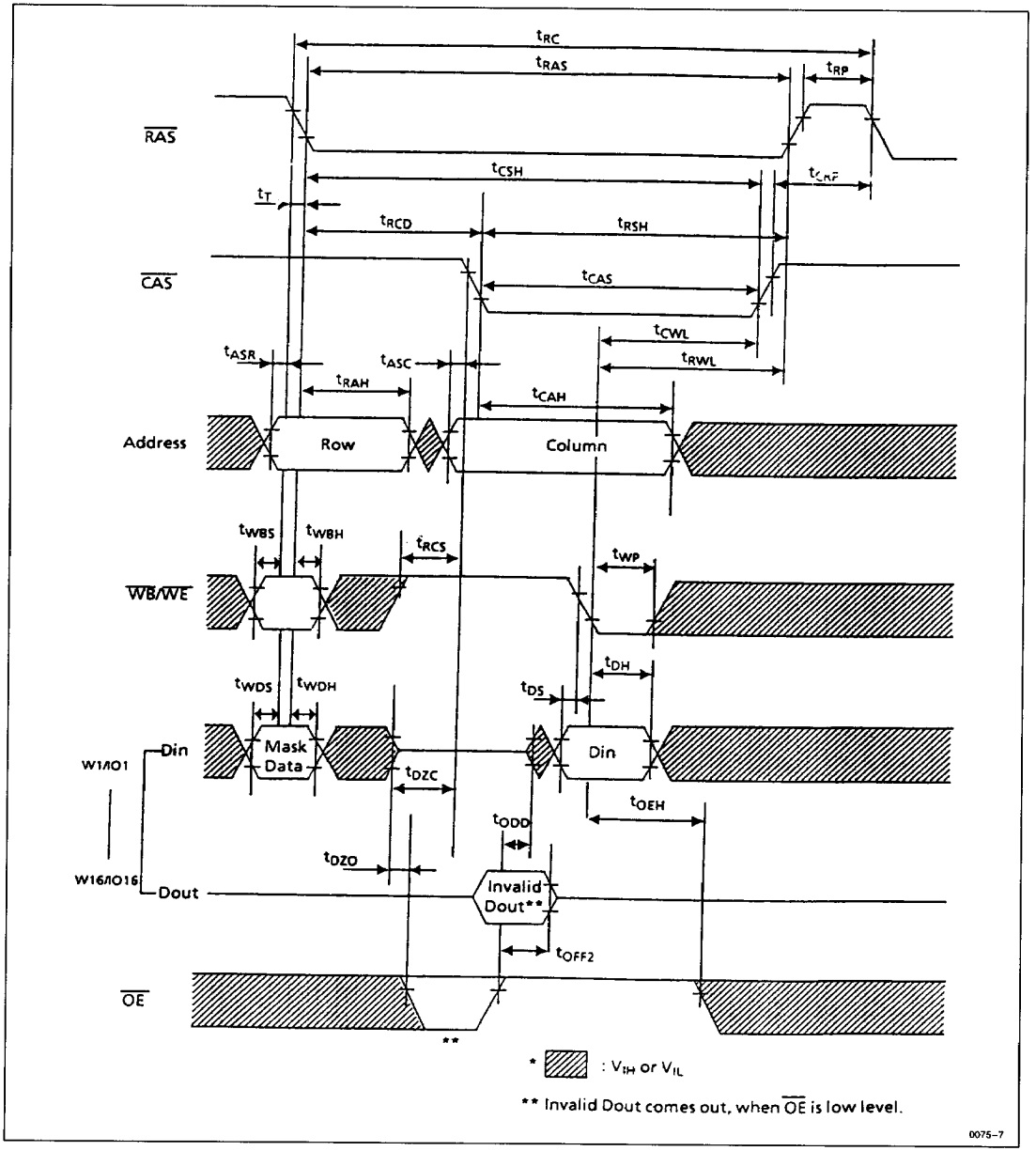
• **Early Write Cycle**



• **Delayed Write Cycle**



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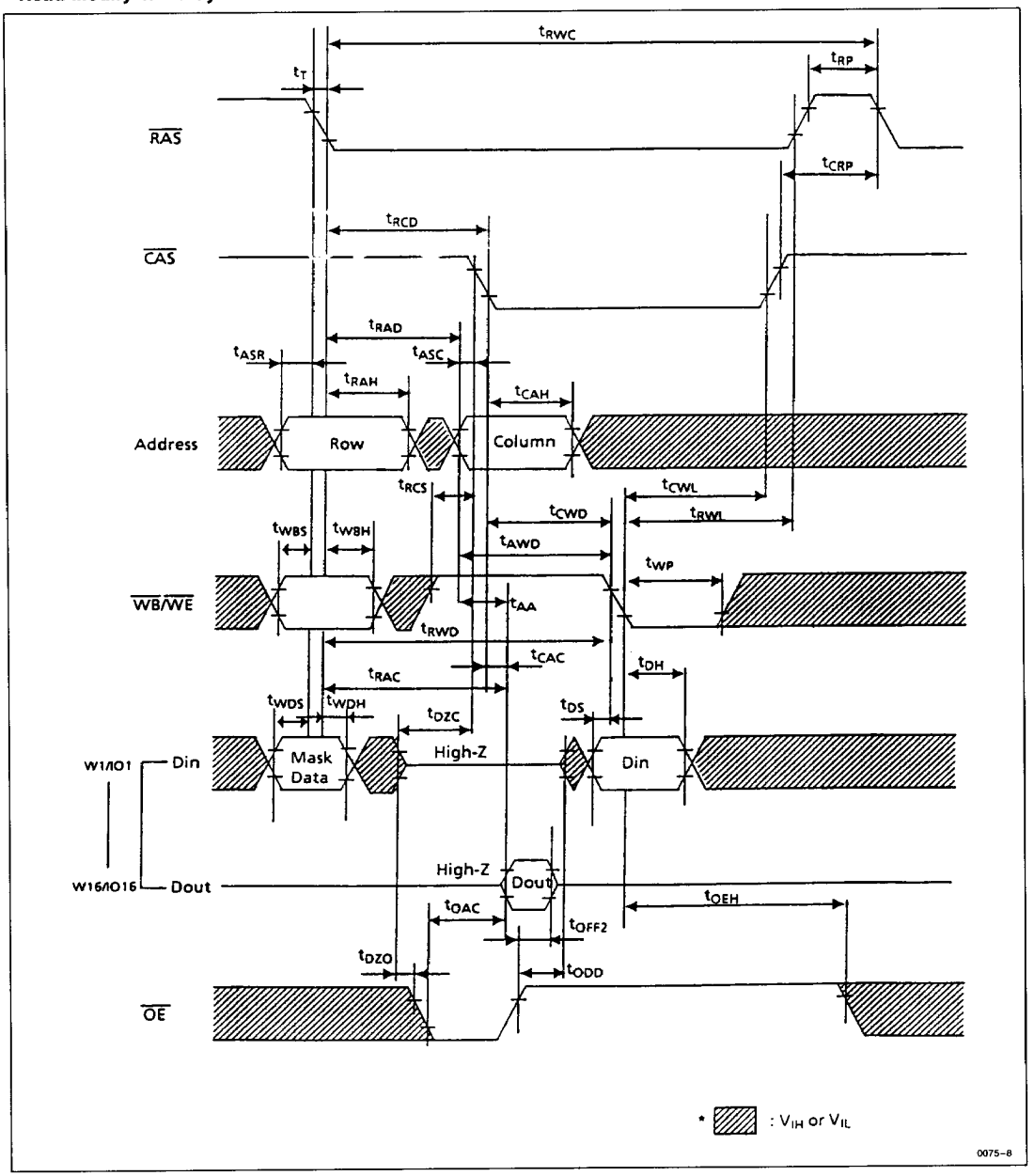
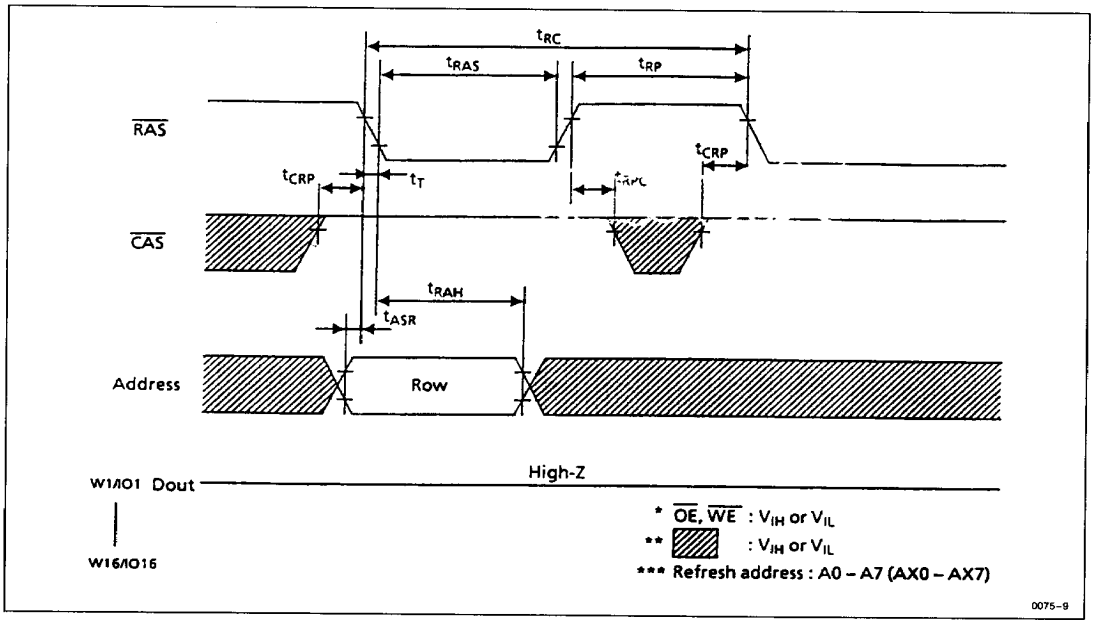
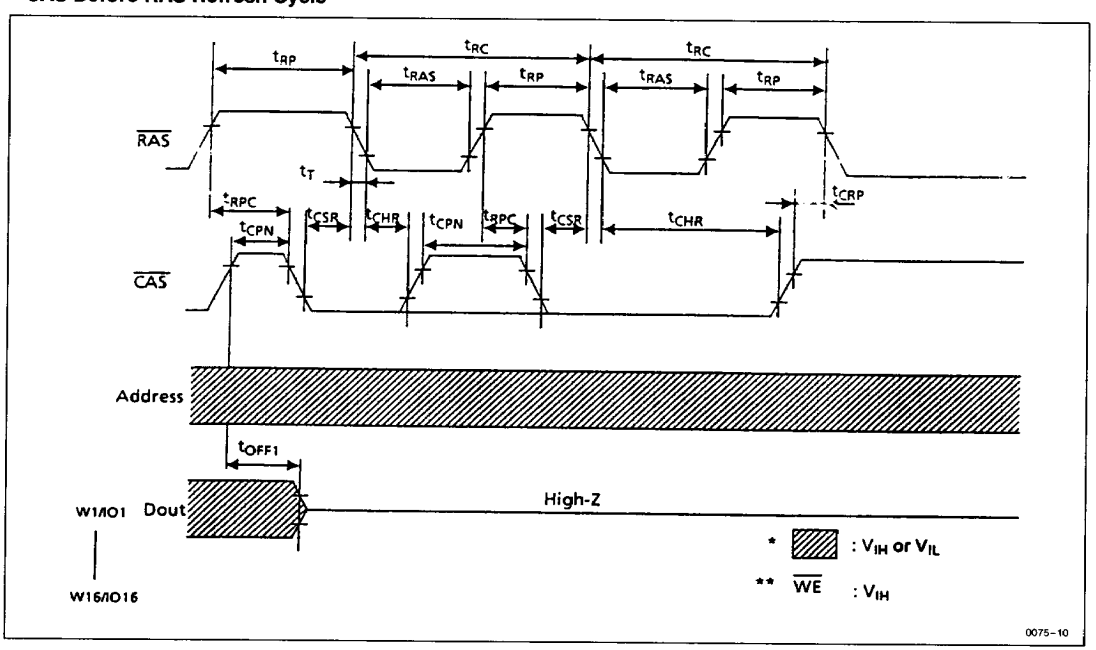
• **Read-Modify-Write Cycle**



• $\overline{RAS}$ Only Refresh Cycle




• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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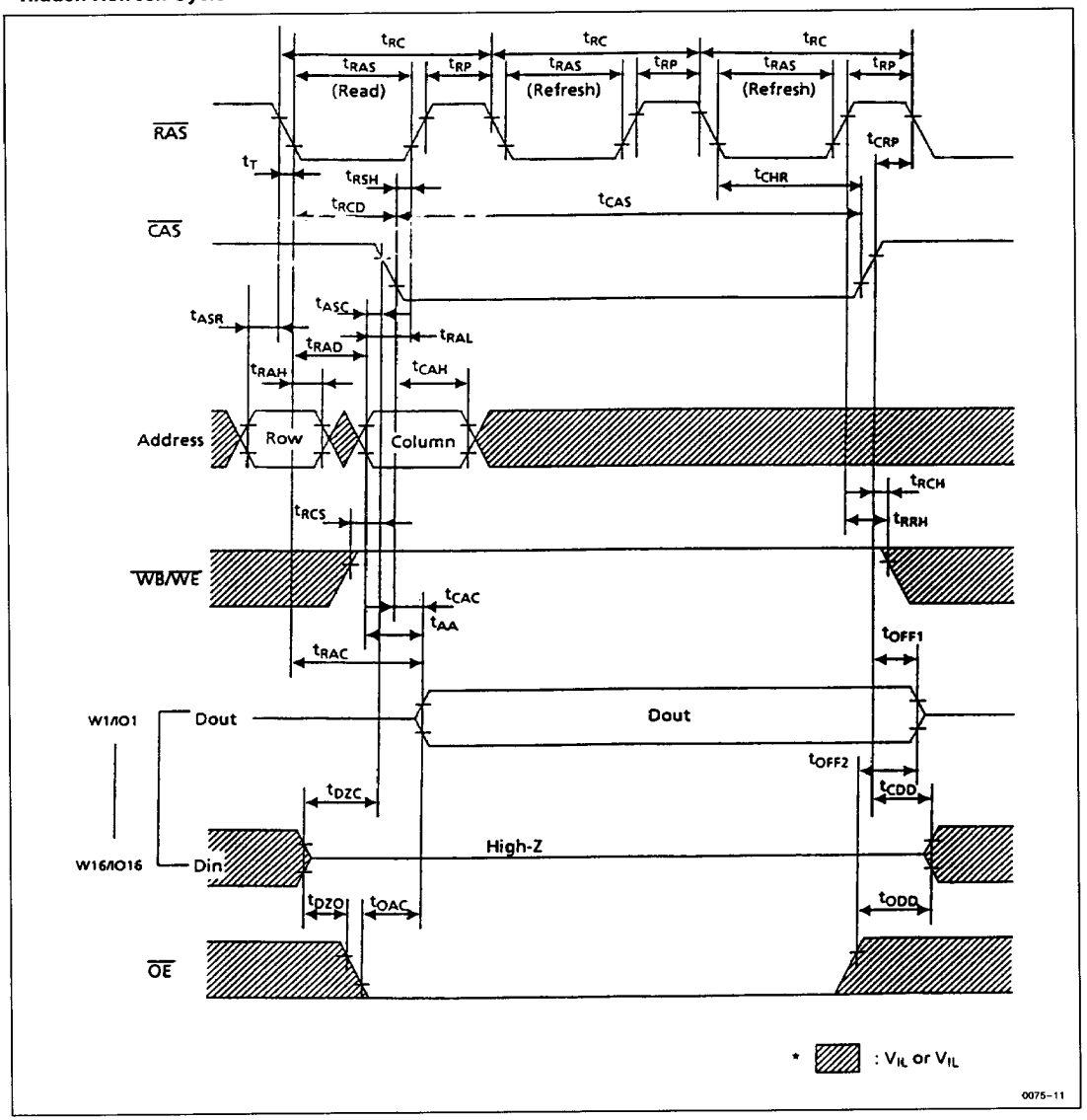
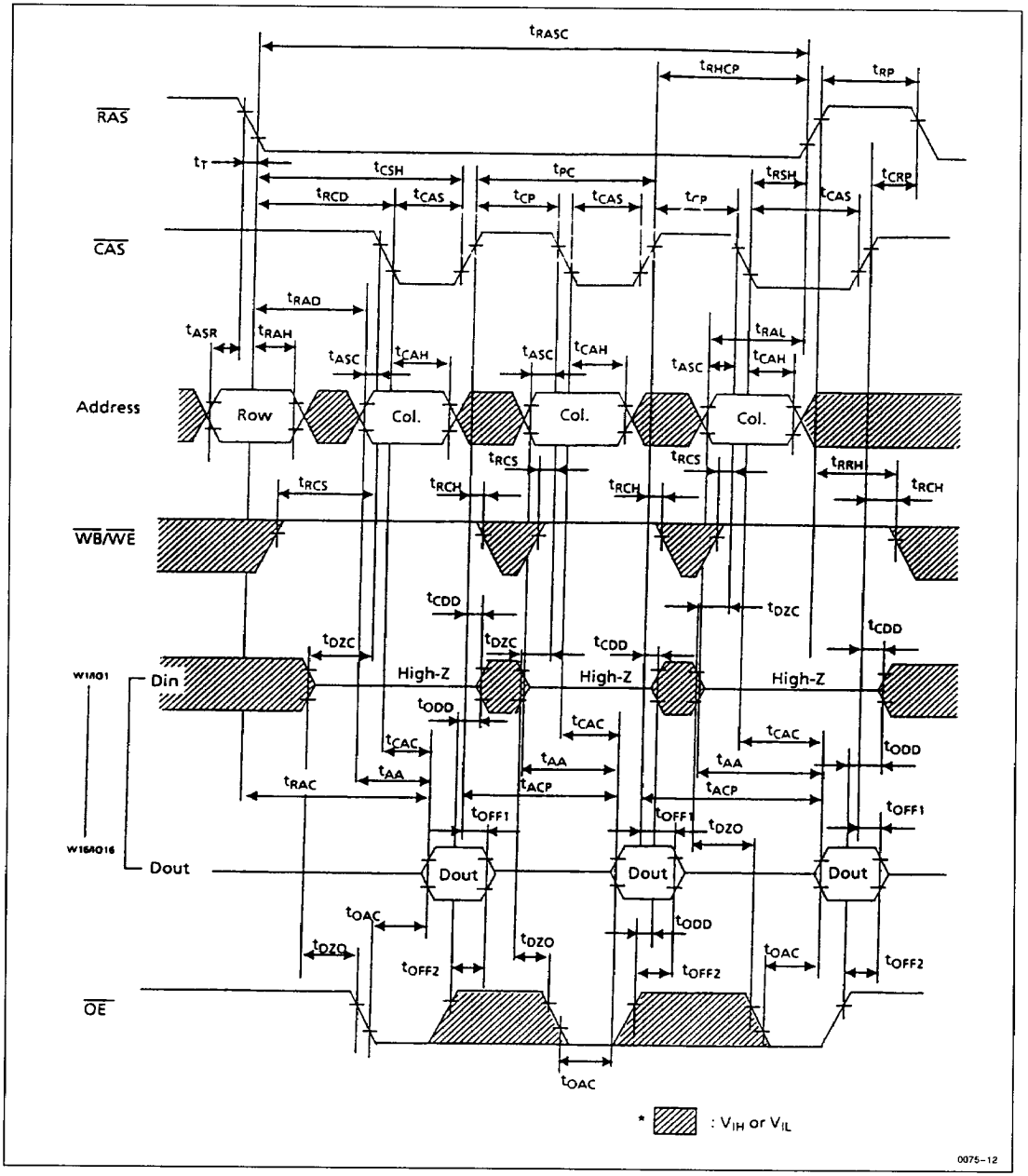
• **Hidden Refresh Cycle**



• **Fast Page Mode Read Cycle**



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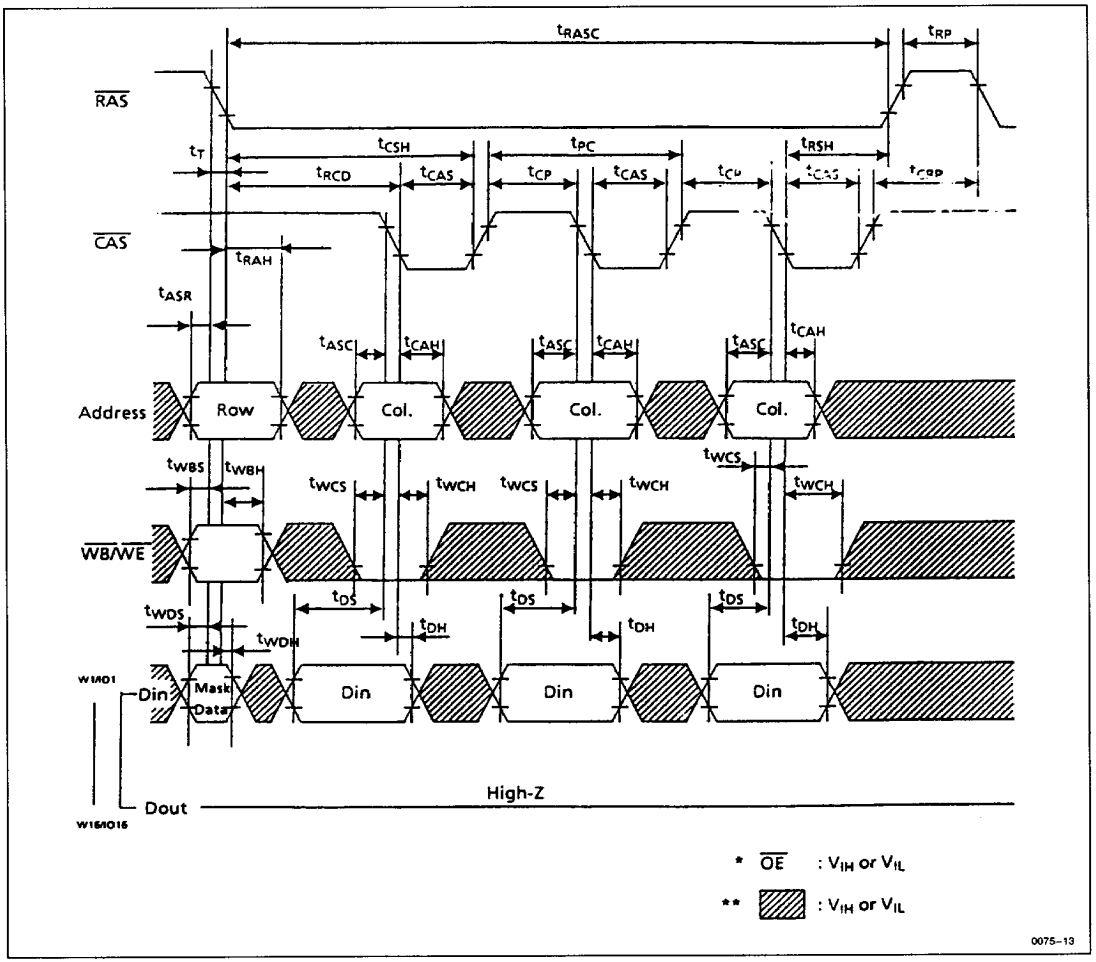
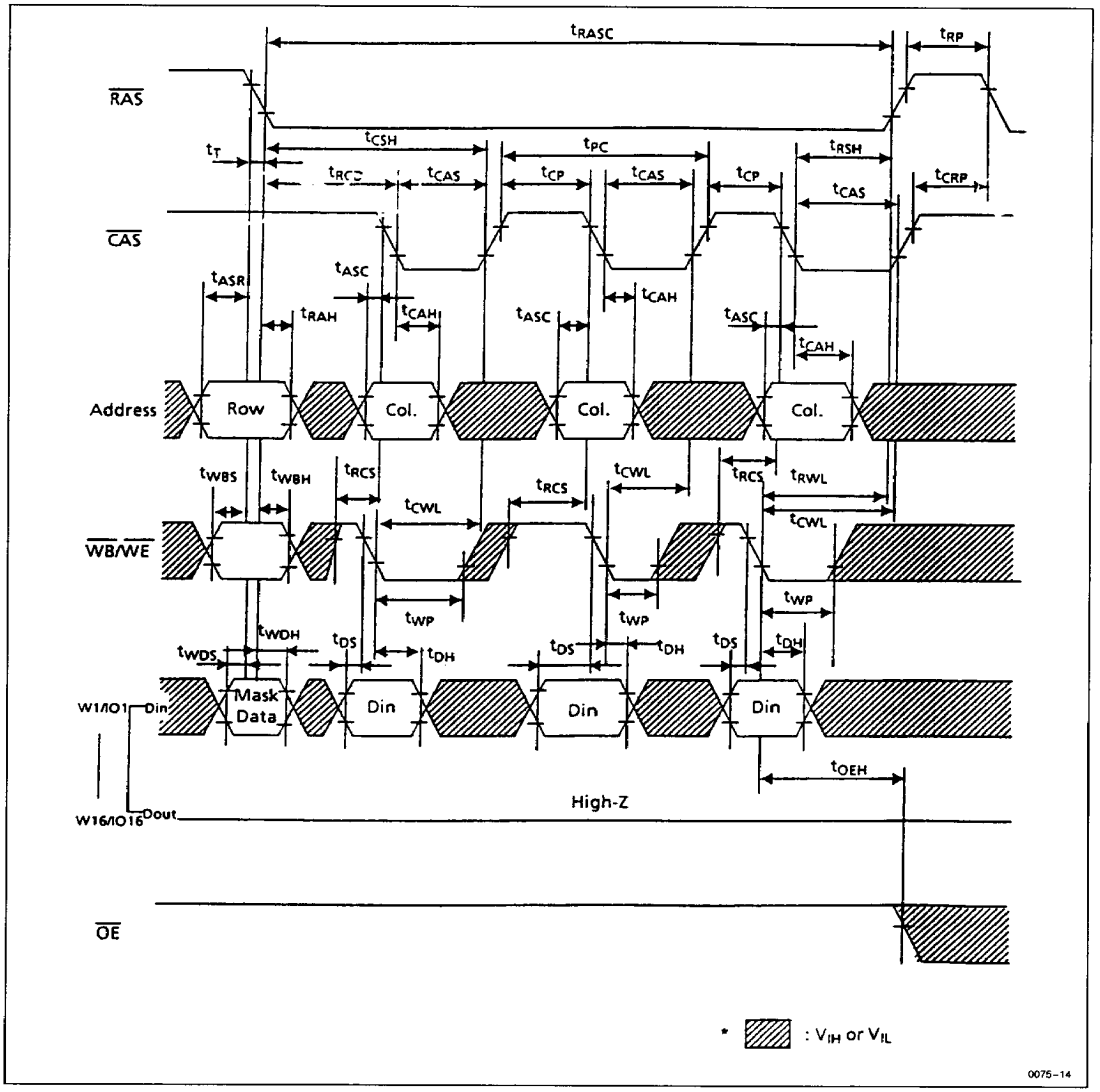
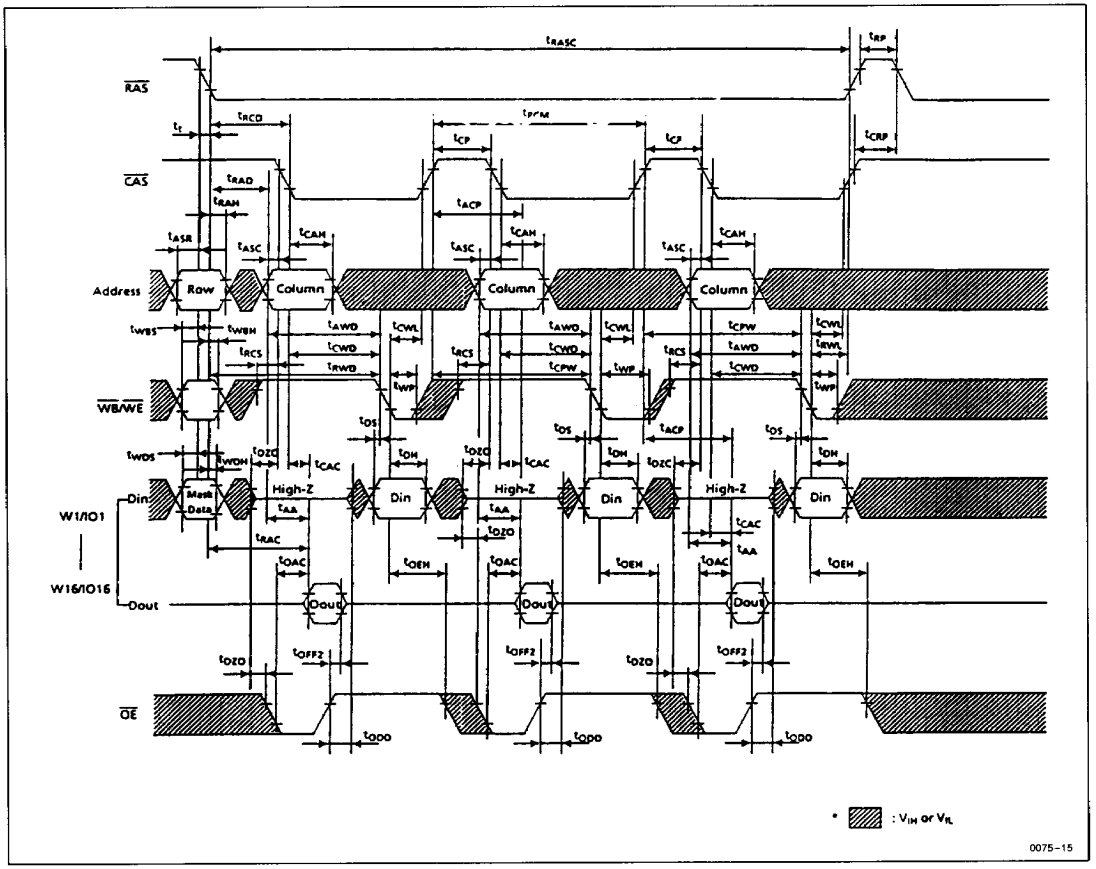
• **Fast Page Mode Early Write Cycle**



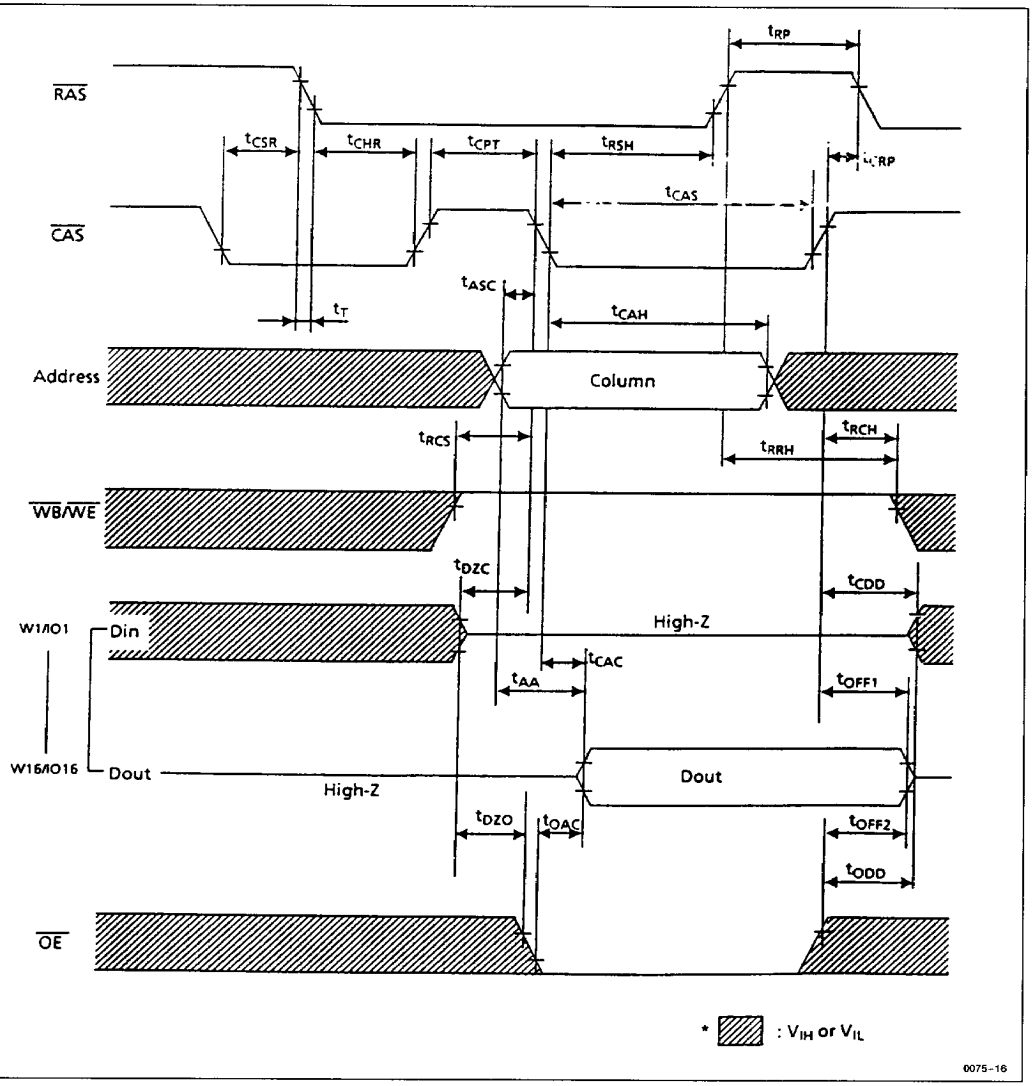
• **Fast Page Mode Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Check Cycle (Write)