OKI Semiconductor

MSM514260/SL

262,144-Words x 16-Bits Dynamic RAM: Fast Page Mode Type

DESCRIPTION

The MSM514260/SL is a new generation dynamic RAM organized as 262,144 words by 16 bits. The technology used to fabricate the MSM514260/SL is OKI's CMOS silicon gate process technology. The device operates on a single +5 V power supply. Its I/O pins are TTL compatible.

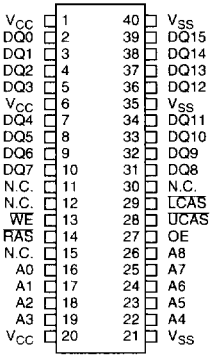
FEATURES

- Silicon gate quadruple polysilicon CMOS, 1-transistor memory cell using advanced OKI process technology for high quality and reliability
- 262,144 words by 16 bits organization - Word size ideally suited for graphic applications. The wide bit organization allows higher data throughput and wider- bandwidth performance allowing better screen colors.
- Single +5 V supply, ±10% tolerance - Industry standard one power supply.
- Input: TTL compatible
- Output: TTL compatible, three-state, non-latch
- Refresh: 512 cycles/8 ms, 512 cycles/128ms (SL version) - has an extremely low standby power specification a 5:1 ratio, it is lower in current consumption than the standard versions.
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$ only refresh capability
- $\overline{CAS}$ before $\overline{RAS}$ self - refresh capability (SL version)

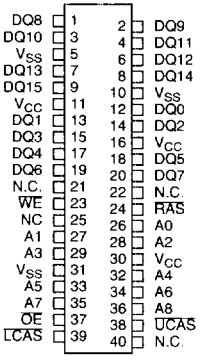
MSM514260/SL FAMILY

Part Number	Access Time (Max)			Cycle Time (Min)	Power Dissipation (Max)	
	t_{RAC}	t_{AA}	t_{CAC}		Operating	Standby
MSM514260/SL-70	70 ns	35 ns	20 ns	130 ns	880 mW	5.5 mW / 1.1 mW (SL version)
MSM514260/SL-80	80 ns	40 ns	20 ns	150 ns	770 mW	
MSM514260/SL-10	100 ns	50 ns	25 ns	180 ns	660 mW	

PIN CONFIGURATION



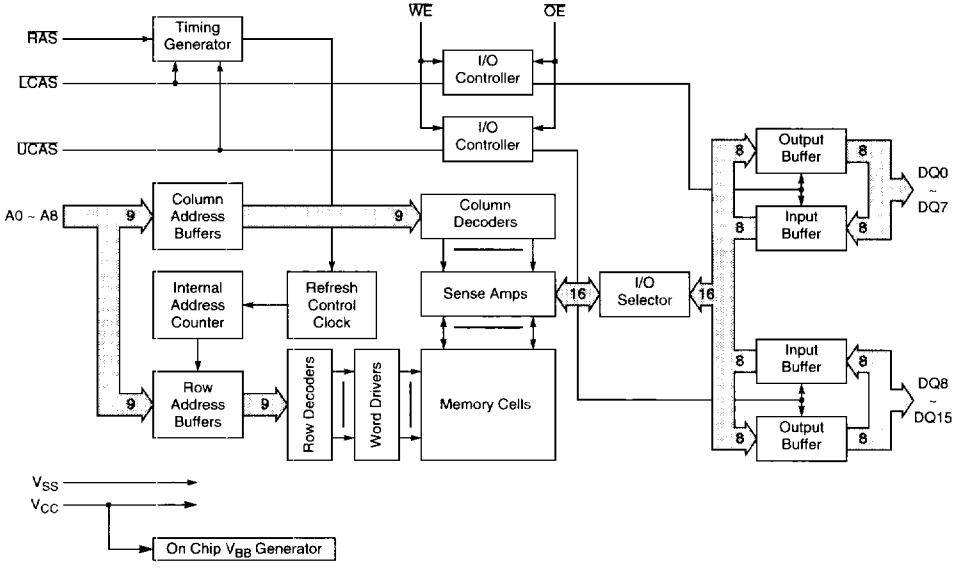
MSM514260/SL
40 Pin 400 mil SOJ



MSM514260/SL
40 Pin 475 mil ZIP

Pin Name	Function
A0 ~ A8	Address Input
$\overline{RAS}$	Row Address Strode
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
DQ0 ~ DQ15	Data-In / Data-Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE

Input Pin					DQ Pin		
RAS	LCAS	UCAS	WE	OE	DQ0~DQ7	DQ8~DQ15	Functional Mode
H	—	—	—	—	High-Z	High-Z	Standby
L	H	H	—	—	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	T_a = 25°C	-1.0 ~ +7.0	V
Short circuit output current	I_{OS}	T_a = 25°C	50	mA
Power dissipation	P_D	T_a = 25°C	1	W
Operating temperature	T_{OPR}	—	0 ~ +70	°C
Storage temperature	T_{STG}	—	-55 ~ +150	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	
Input high voltage	V_{IH}	—	2.4	—	6.5	V
Input low voltage	V_{IL}	—	-1.0	—	0.8	V

Capacitance (T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Typ	Max	Unit
Input capacitance (A0 ~ A8)	C_{IN1}	—	–	7	pF
Input capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	–	7	pF
Output capacitance (DQ0 ~ DQ15)	$C_{I/O}$	—	–	10	pF

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C)

Parameter	Symbol	Condition		MSM514260 / SL-70		MSM514260 / SL-80		MSM514260 / SL-10		Unit	Note
				Min	Max	Min	Max	Min	Max		
Output high voltage	V_{OH}	I_{OH} = -5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V		-10	10	-10	10	-10	10	µA	
Output leakage current	I_{LO}	D_{OUT} disable 0 V ≤ V_O ≤ 5.5 V		-10	10	-10	10	-10	10	µA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min		–	160	–	140	–	120	mA	[1] [2]
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z	TTL	–	2	–	2	–	2	mA	
			MOS	–	1	–	1	–	1		
				–	200	–	200	–	200	µA	[4]

DC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) (Continued)

Parameter	Symbol	Condition	MSM514260 / SL-70		MSM514260 / SL-80		MSM514260 / SL-10		Unit	Note
			Min	Max	Min	Max	Min	Max		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	–	160	–	140	–	120	mA	[1] [2]
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable	–	5	–	5	–	5	mA	[1]
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	160	–	140	–	120	mA	[1] [2]
Average power supply current (Fast page mode)	I_{CC7}	RAS = V_{IL}, CAS cycling t_{PC} = min	–	130	–	120	–	110	mA	[1] [3]
Average power supply current (Battery Backup)	I_{CC10}	t_{RC} = 128 µs, $\overline{CAS}$ before $\overline{RAS}$, t_{RAS} ≤ 1 µs, $\overline{CAS}$ = V_{IL}	–	300	–	300	–	300	µA	[4]
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ self - refresh)	I_{CC5}	$\overline{RAS}$ ≤ 0.2 V, $\overline{CAS}$ ≤ 0.2 V, D_{OUT} = High-Z	–	200	–	200	–	200	µA	[4]

1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Only SL version.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] [4]

Parameter	Symbol	MSM514260 / SL-70		MSM514260 / SL-80		MSM514260 / SL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	–	150	–	180	–	ns	
Read or write cycle time	t_{RWC}	180	–	200	–	240	–	ns	
Fast page mode cycle time	t_{PC}	45	–	50	–	60	–	ns	
Fast page mode read or write cycle time	t_{PRWC}	95	–	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	[5] [6] [7]
Access time for $\overline{CAS}$	t_{CAC}	–	20	–	20	–	25	ns	[5] [6]
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	[5] [7]
Access time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	25	ns	[5]
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	40	–	45	–	55	ns	[5] [13]
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	15	0	15	0	20	ns	[8]
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	0	15	0	15	0	20	ns	[8]
Transition time	t_T	3	50	3	50	3	50	ns	
Refresh period	t_{REF}	–	8	–	8	–	8	ms	

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] [4] (Continued)

Parameter	Symbol	MSM514260 / SL-70		MSM514260 / SL-80		MSM514260 / SL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Refresh period	t_{REF}	–	128	–	128	–	128	ms	[16]
$\overline{RAS}$ precharge time	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10k	80	10k	100	10k	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100k	80	100k	100	100k	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	–	10	–	10	–	ns	[15]
$\overline{CAS}$ pulse width	t_{CAS}	20	10k	20	10k	25	10k	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	[13]
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	[6]
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	[7]
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	[12]
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	[12]
Column address hold time from $\overline{RAS}$	t_{AR}	55	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	[12]
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	[9] [12]
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	[9]
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	[10] [12]
Write command hold time	t_{WCH}	15	–	15	–	20	–	ns	[12]
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	55	–	60	–	75	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	25	–	ns	[14]
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	[11] [12]
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	[11] [12]
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	15	–	15	–	20	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	–	45	–	55	–	ns	[10]
Column address to $\overline{WE}$ delay time	t_{AWD}	60	–	65	–	80	–	ns	[10]
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	–	105	–	130	–	ns	[10]
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	[12]
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	[12]

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0°C ~ +70°C) [1] [2] [3] [4] (Continued)

Parameter	Symbol	MSM514260 / SL-70		MSM514260 / SL-80		MSM514260 / SL-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	15	–	15	–	20	–	ns	[13]
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	[15]
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns	[15]
$\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{RASS}	100	–	100	–	100	–	ns	[16]
$\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{RPS}	130	–	150	–	180	–	ns	[16]
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self-refresh)	t_{CHS}	-50	–	-60	–	-70	–	ns	[16]

1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only refresh) before proper device operation is achieved.
2. Same V_{CC}-voltage level must be applied to all V_{CC}-pins. And same V_{SS}-voltage level must be applied to all V_{SS}-pins.
3. The AC characteristics assume at t_T = 5 ns.
4. V_{IH} (Min) and V_{IL} (Max) are reference levels for measuring of input signals. Also, transition times (t_T) are measured between V_{IH} and V_{IL}.
5. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
6. Operation within the t_{RCD} (Max) limit insures that t_{RAC} (Max) can be met, t_{RCD} (Max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max) limit, then access time is controlled exclusively be t_{CAC}.
7. Operation within the t_{RAD} (Max) limit insures that t_{RAC} (Max) can be met, t_{RAD} (Max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (Max) limit, than access time is controlled exclusively be t_{AA}.
8. t_{OFF} (Max) and t_{OEZ} (Max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (Min) the cycle is an early write cycle and the data out will remain open circuit (High impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (Min), $t_{RWD} \geq t_{RWD}$ (Min) and $t_{AWD} \geq t_{AWD}$ (Min) the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read-modify-write cycle.
12. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{DS}, t_{DH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ and $\overline{LCAS}$.
13. t_{CRP}, t_{CHR} and t_{CPA} are determined by the later rising edge of $\overline{UCAS}$ and $\overline{LCAS}$.
14. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
15. t_{CPN}, t_{CP} and t_{CPT} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
16. Only SL version.

AC Timing Charts

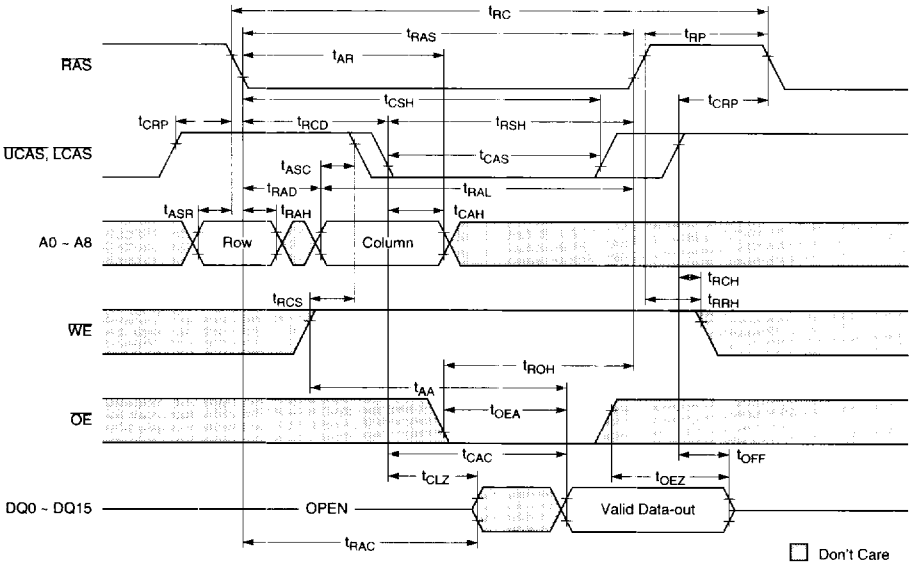


Figure 1. Read Cycle

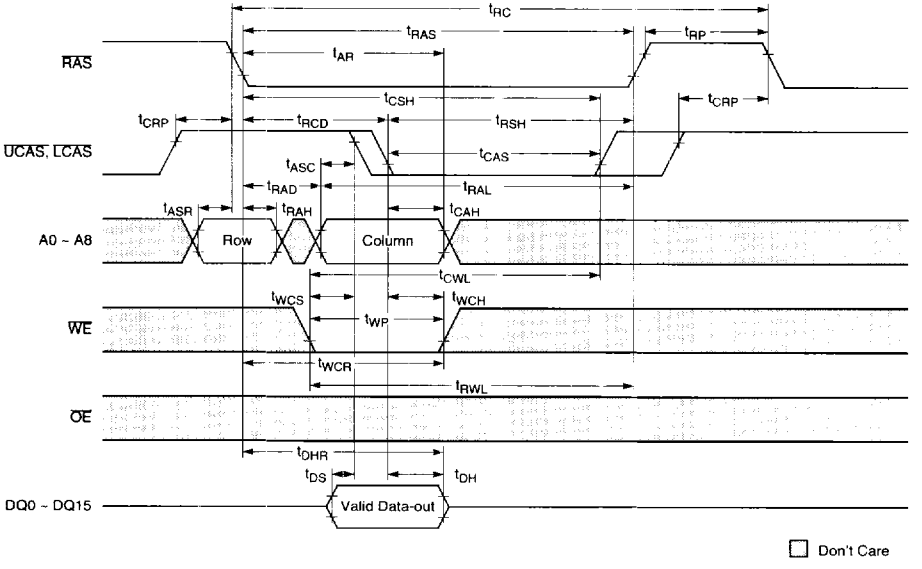


Figure 2. Write Cycle (Early Write)

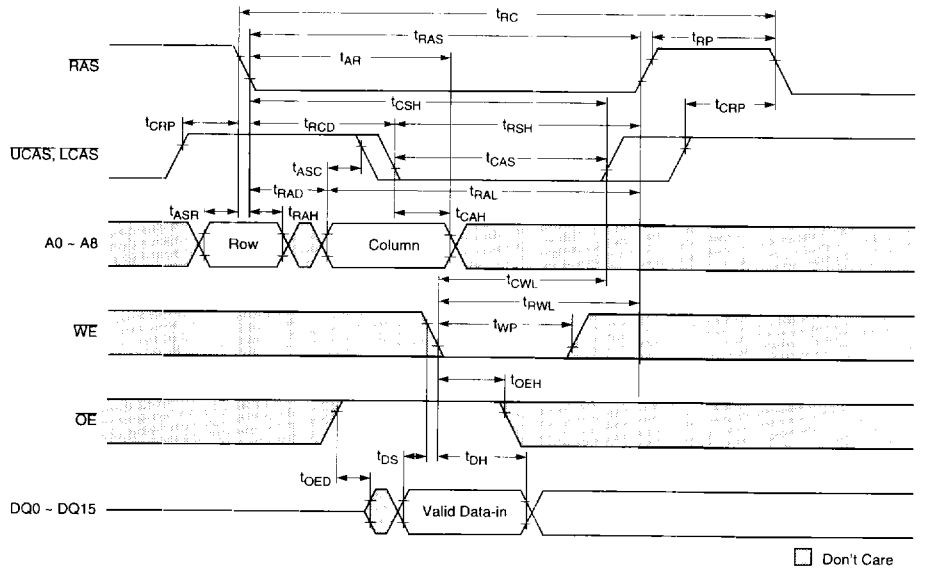


Figure 3. Write Cycle (OE Control Write)

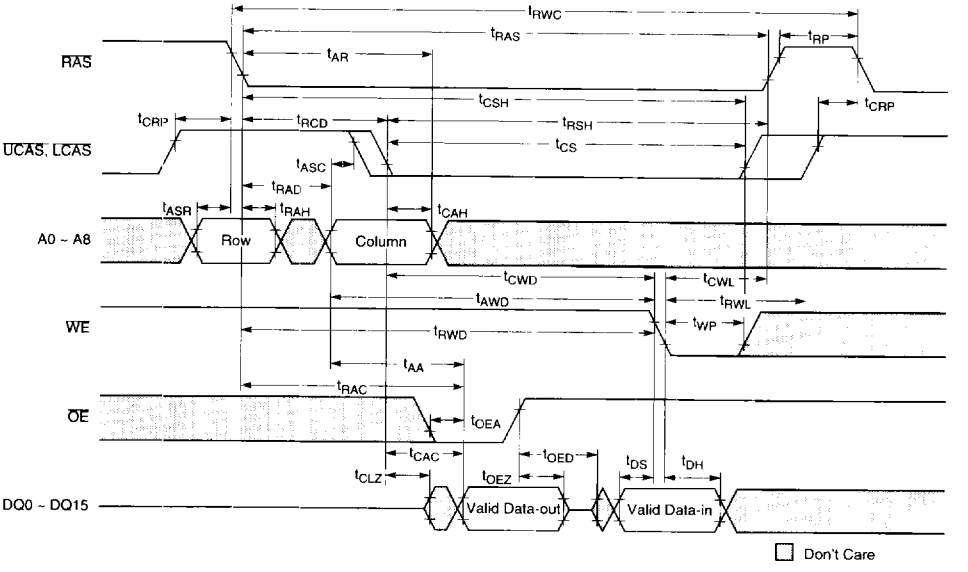


Figure 4. Read/Write Cycle

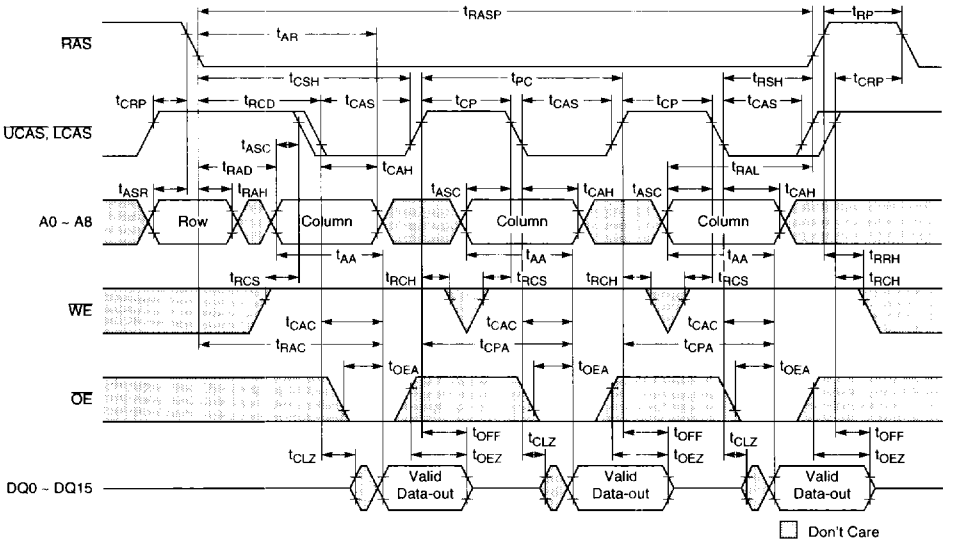


Figure 5. Fast Page Mode Read Cycle

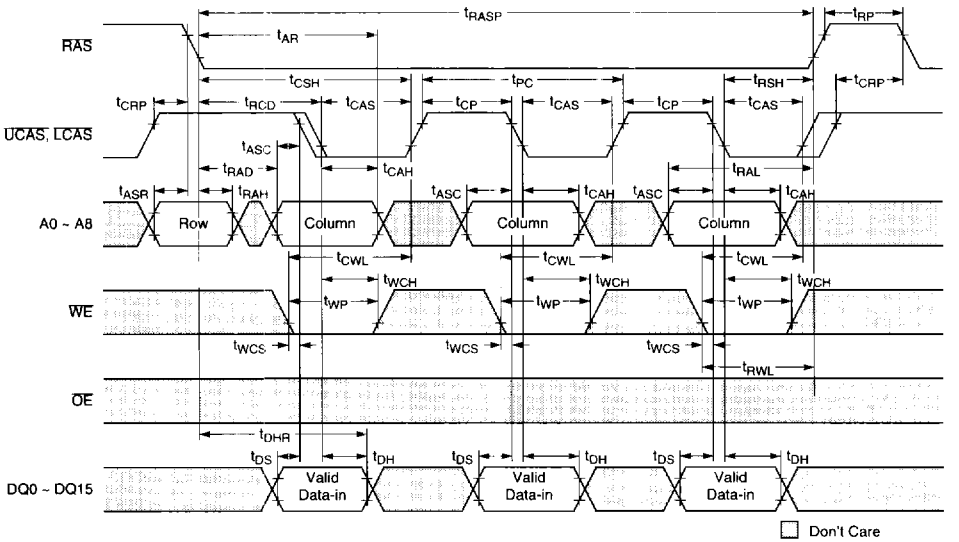


Figure 6. Fast Page Mode Write Cycle (Early Write)

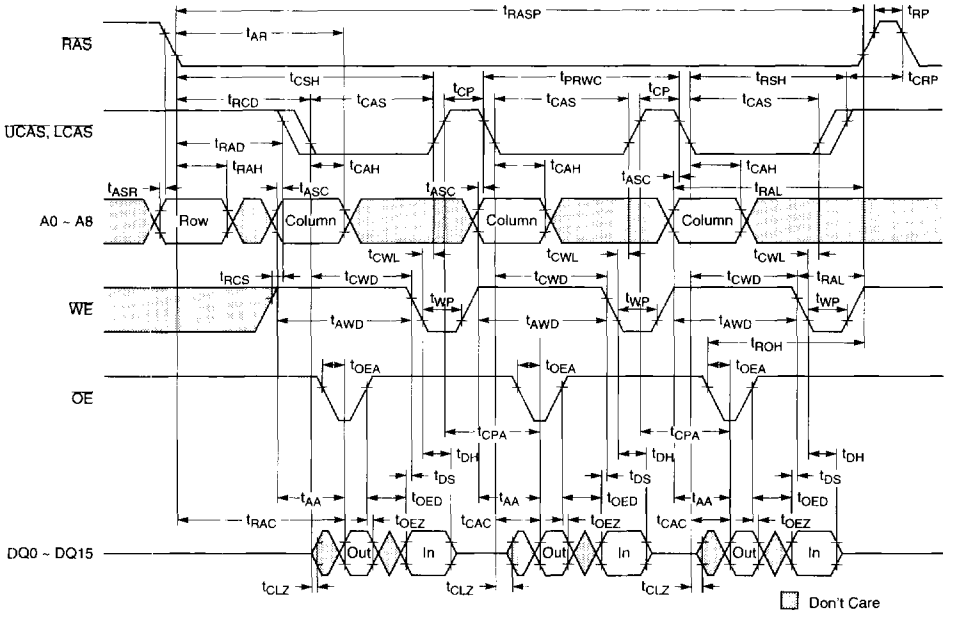


Figure 7. Fast Page Mode Read/Write Cycle

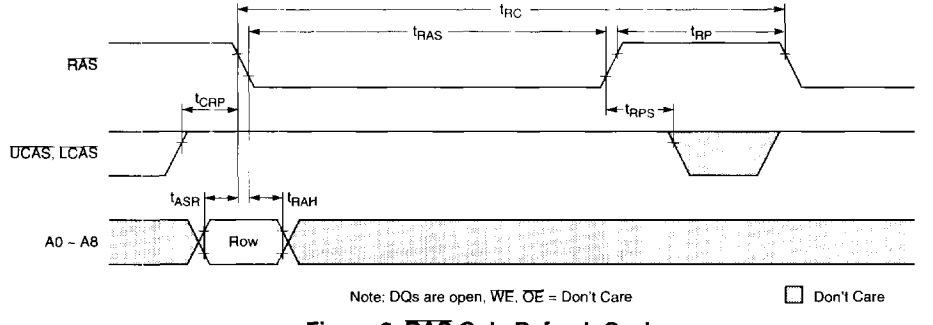


Figure 8. RAS Only Refresh Cycle

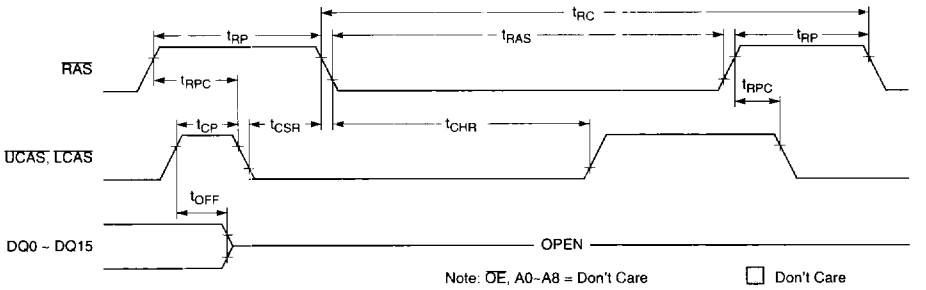


Figure 9. $\overline{CAS}$ Before $\overline{RAS}$ Auto Refresh Cycle

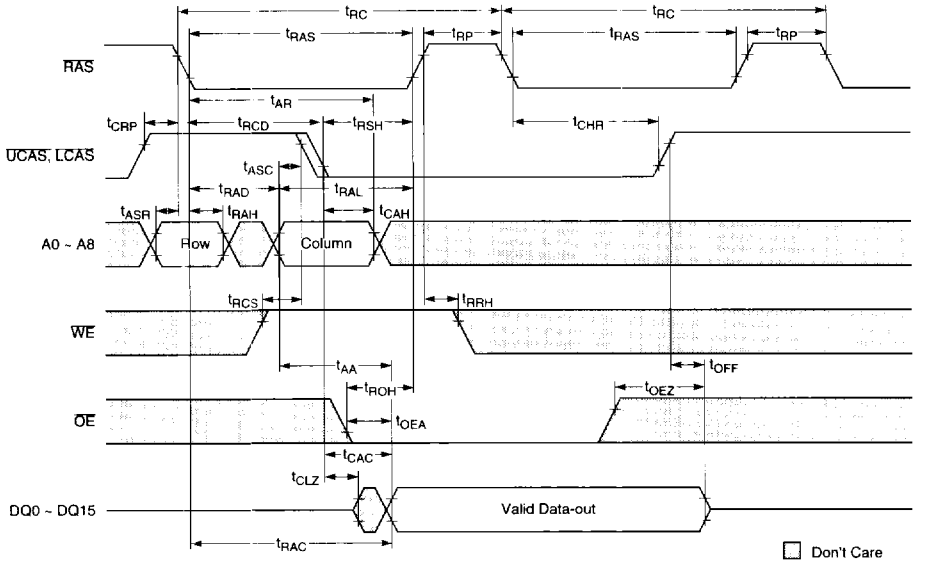


Figure 10. Hidden Refresh Read Cycle

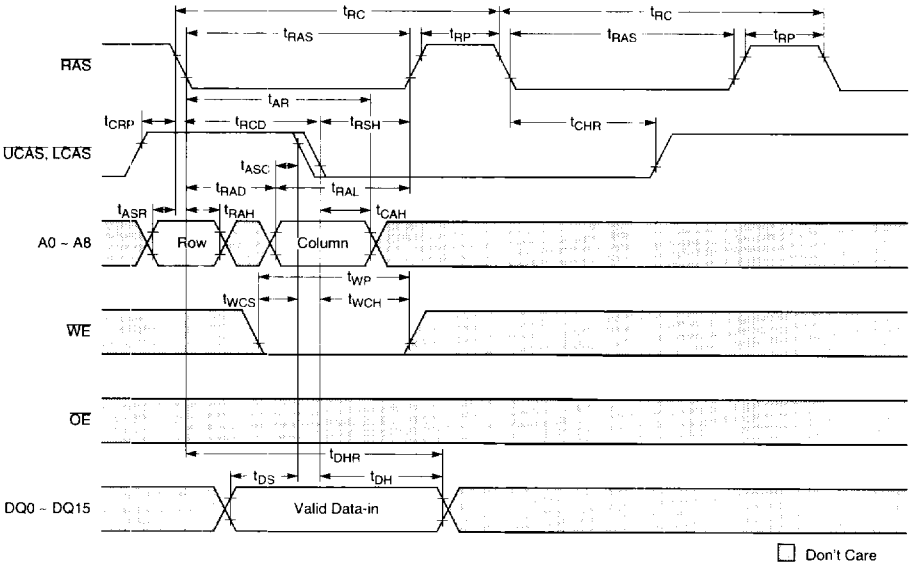


Figure 11. Hidden Refresh Write Cycle

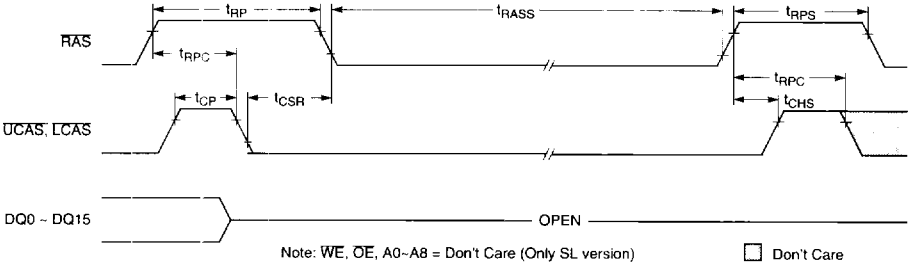


Figure 12. $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle

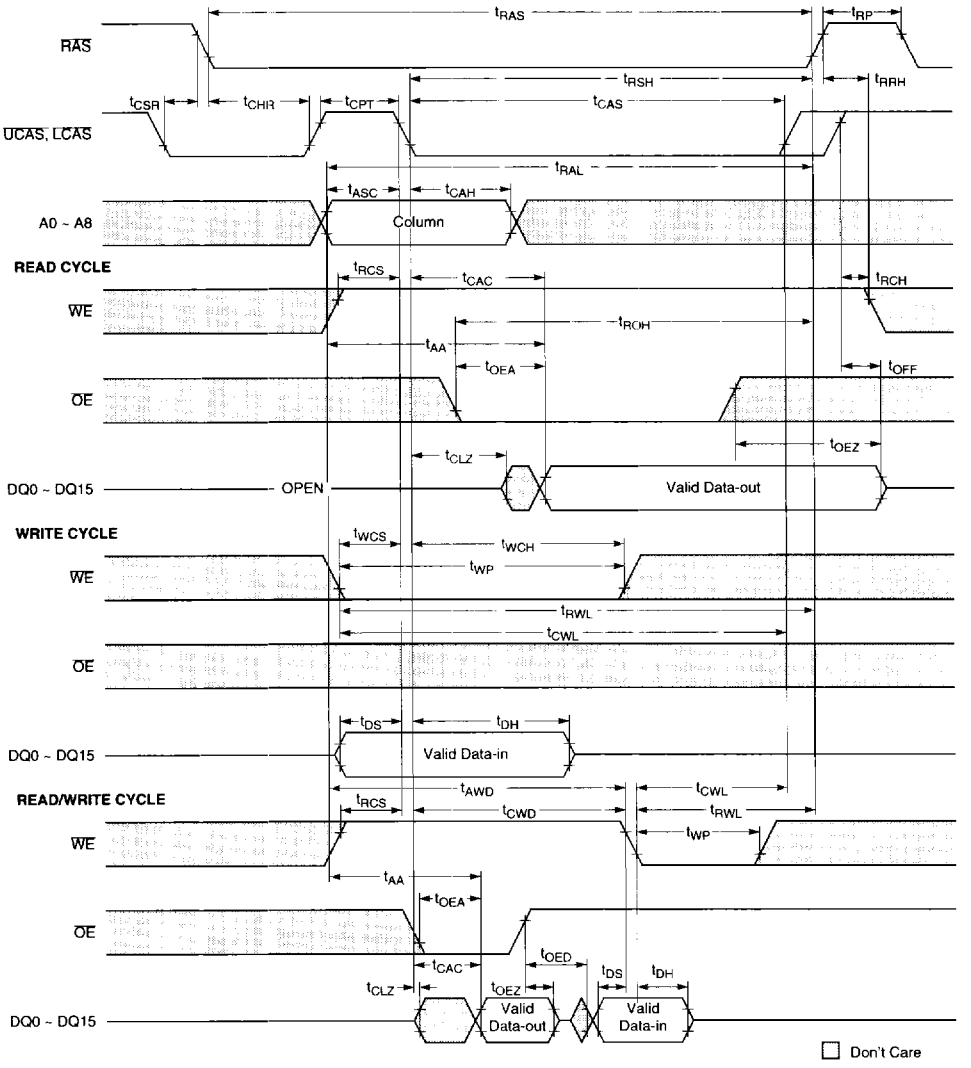


Figure 13. $\overline{CS}$ Before $\overline{RAS}$ Refresh Counter Test

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