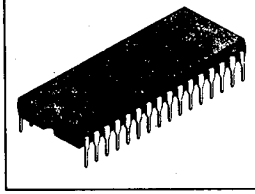
131,072-word × 8-bit High Speed CMOS Static RAM

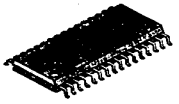
Description

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAMs organized as 131,072 words by 8-bit and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

CXK581001P
32 pin DIP (Plastic)



CXK581001M
32 pin SOP (Plastic)



Features

- Fast access time: (Access time)
  CXK581001P/M-70L/70LL 70ns (Max.)
  CXK581001P/M-85L/85LL 85ns (Max.)
- Low power operation :
  CXK581001P/M Standby/Operation
  –70L/85L : 10μW (Typ.)/237.5mW (Typ., Cycle=Min.)
  –70LL/85LL : 3.5μW (Typ.)/237.5mW (Typ., Cycle=Min.)
- Single + 5V supply : +5V ± 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600mil 32 pin DIP package
- CXK581001M 525mil 32 pin SOP package

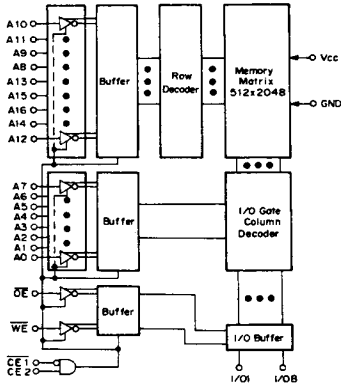
Function

131,072-word × 8-bit static RAM

Structure

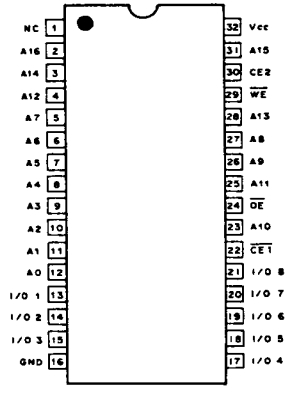
Silicon gate CMOS IC

Block diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A_0 to A_{16}	Address input
I/O1 to I/O8	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	+5V power supply
GND	Ground
NC	No connection

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E89Y03B08 – ST

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	Vcc		− 0.5 to +7.0	V
Input voltage	V_{IN}		− 0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$		− 0.5 * to Vcc +0.5	V
Allowable power dissipation	P_D	CXK581001P	1.0	W
		CXK581001M	0.7	
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		− 55 to +150	℃
Soldering temperature • time	Tsolder		260 • 10	℃ • sec

* V_{IN}, $V_{I/O}$= − 3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	Icc
L	H	L	H	Read	Data out	Icc
L	H	×	L	Write	Data in	Icc

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	Vcc+0.3	V
Input low voltage	V_{IL}	− 0.3 *	——	0.8	V

* V_{IL}= − 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70℃)

Item	Symbol	Test conditions		− 70L/85L			− 70LL/85LL			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc		− 1	—	1	− 1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=GND to Vcc		− 1	—	1	− 1	—	1	μA
Average operating current	Icc	Cycle=Min, Duty=100% I_{OUT}=0mA		—	47.5	80	—	47.5	80	mA
Standby current	I_{SB1}	CE2 ≦ 0.2V or $\overline{CE1}$ ≧ Vcc − 0.2V CE2 ≧ Vcc − 0.2V	0 to 70℃	—	—	100	—	—	20	μA
			0 to 40℃	—	—	20	—	—	4	
			+25℃	—	2	8	—	0.7	2	
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	1.2	3	—	1.2	3	mA
Output high voltage	V_{OH}	I_{OH}= − 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	—	—	0.4	V

* Vcc=5V, Ta=25℃

I/O capacitance

(Ta=25℃, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

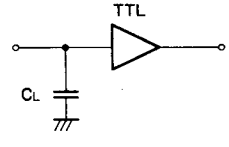
AC characteristics

• AC test conditions

(Vcc=5V ± 10%, Ta=0 to +70℃)

Item	Conditions
Input pulse high level	V_{IH}=2.2V
Input pulse low level	V_{IL}=0.8V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	C_L*=100pF, 1TTL

* C_L includes scope and jig capacitances.



• **Read cycle** ($\overline{WE}$="H")

Item	Symbol	− 70L/70LL		− 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	70	—	85	—	ns
Address access time	t_{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t_{CO2}	—	70	—	85	ns
Output enable to output valid	t_{OE}	—	40	—	45	ns
Output hold from address change	t_{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2} *	—	25	—	25	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	—	25	—	25	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

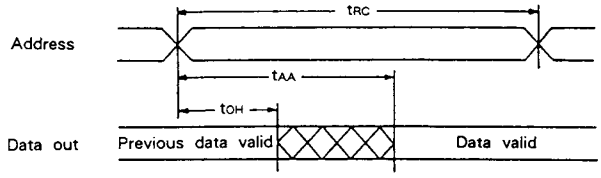
• **Write cycle**

Item	Symbol	− 70L/70LL		− 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	70	—	85	—	ns
Address valid to end of write	t_{AW}	60	—	75	—	ns
Chip enable to end of write	t_{CW}	60	—	75	—	ns
Data to write time overlap	t_{DW}	25	—	30	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	50	—	60	—	ns
Address set up time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$, $\overline{CE1}$)	t_{WR}	5	—	5	—	ns
Write recovery time (CE2)	t_{WR1}	10	—	10	—	ns
Output active from end of write	t_{OW}	5	—	5	—	ns
Write to output in high Z	t_{WHZ} *	—	25	—	30	ns

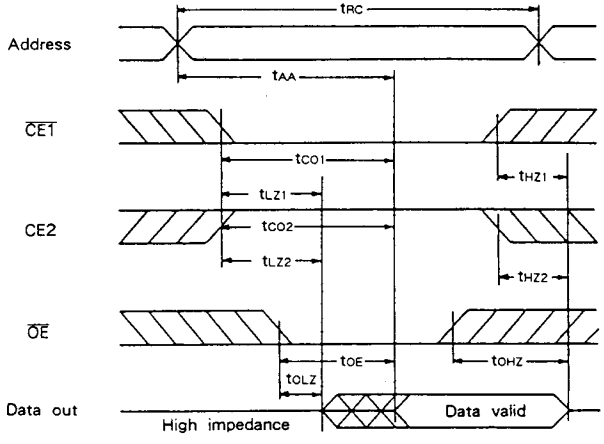
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

Timing Waveform

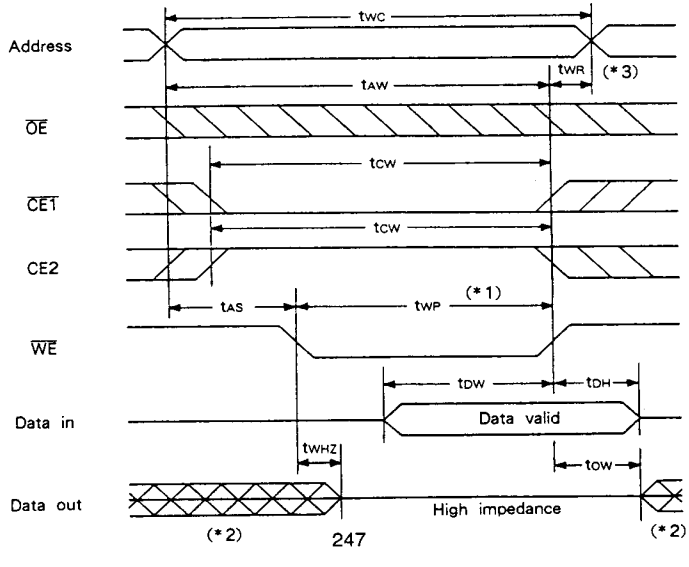
• Read cycle (1): $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



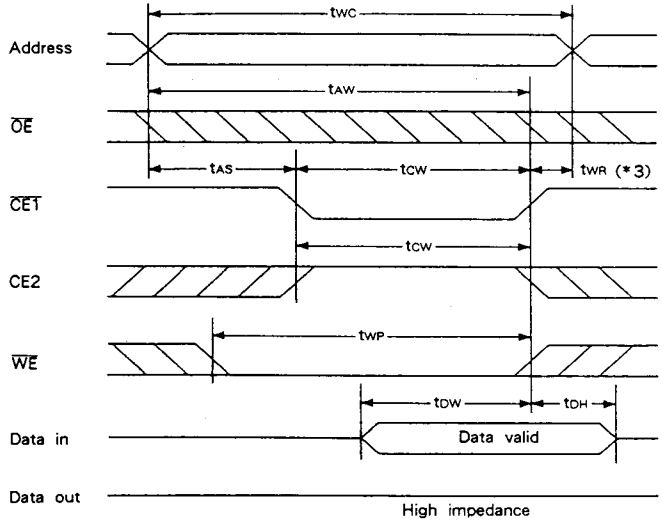
• Read cycle (2): $\overline{WE}$=V_{IH}



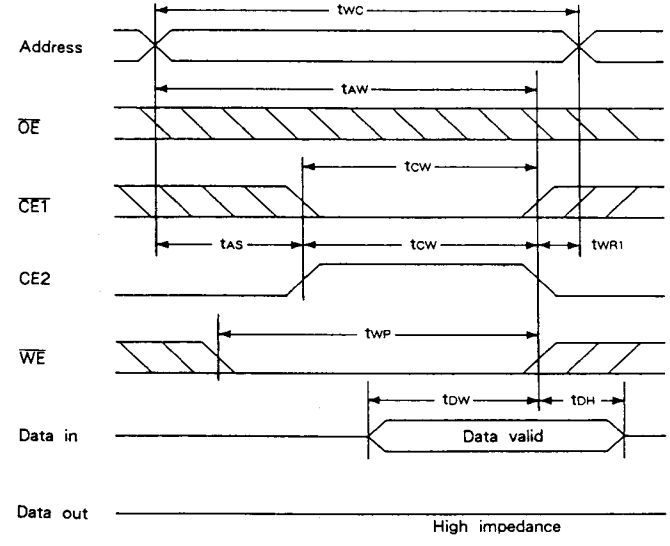
• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): CE2 control



*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
*2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
*3. twr is tested from the rising edge of $\overline{WE}$ or $\overline{CE1}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

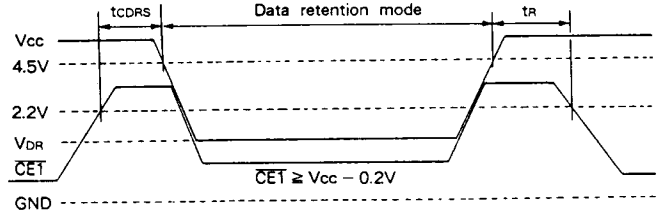
Item	Symbol	Test conditions		− 70L/85L			− 70LL/85LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=0.3V *1	0 to 70 °C	—	—	50	—	—	12	µA
			0 to 40 °C	—	—	10	—	—	2.4	
			+25 °C	—	1	4	—	0.4	1.2	
	I_{CCDR2}	Vcc=2.0 to 5.5V *1		—	2	100	—	0.7	20	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t_R			t_{RC} *2	—	—	t_{RC} *2	—	—	ns

*1. $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)

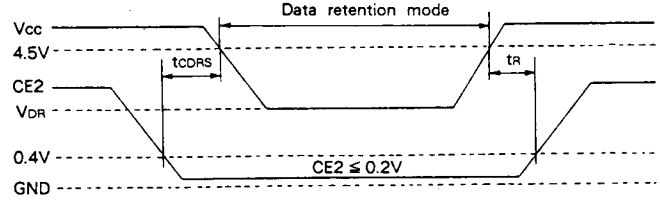
*2. t_{RC} : Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



- Low supply voltage data retention waveform (2) (CE2 control)



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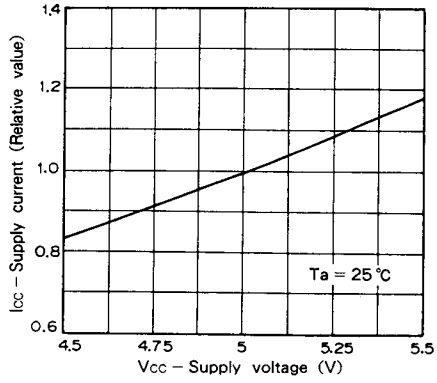
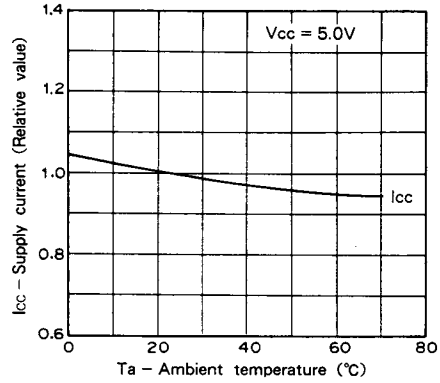
Example of Representative Characteristics

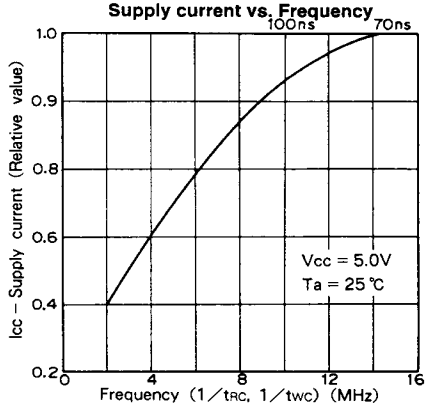
Supply current vs. Supply voltage



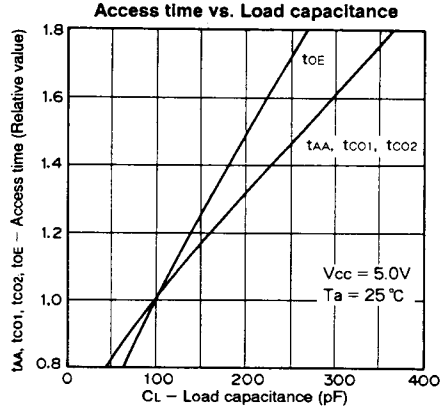
Supply current vs. Ambient temperature



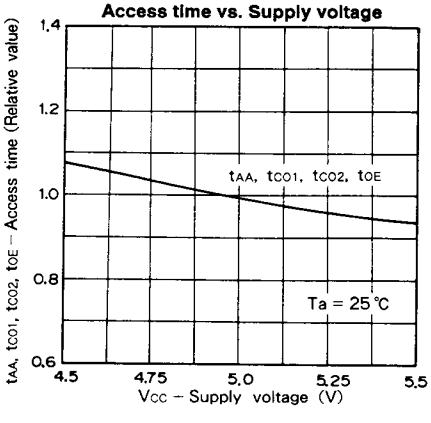
Supply current vs. Frequency



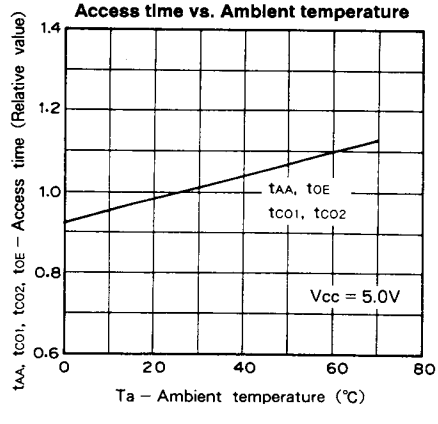
Access time vs. Load capacitance



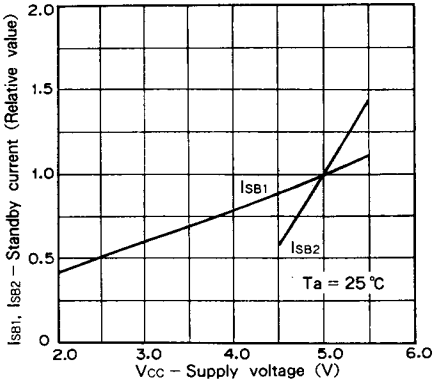
Access time vs. Supply voltage



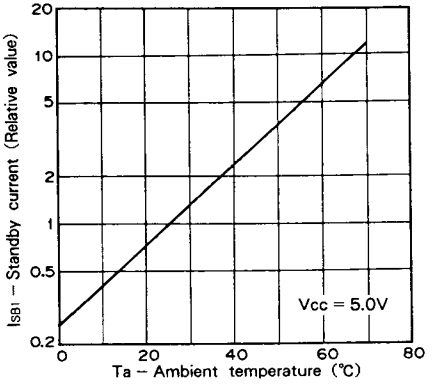
Access time vs. Ambient temperature



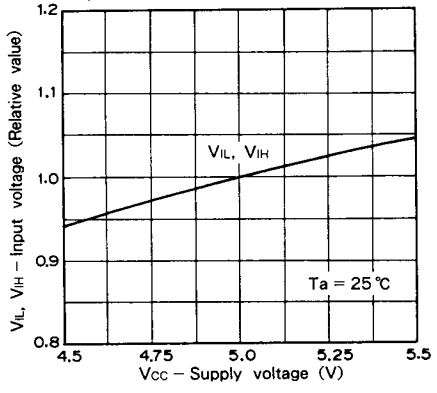
Standby current vs. Supply voltage



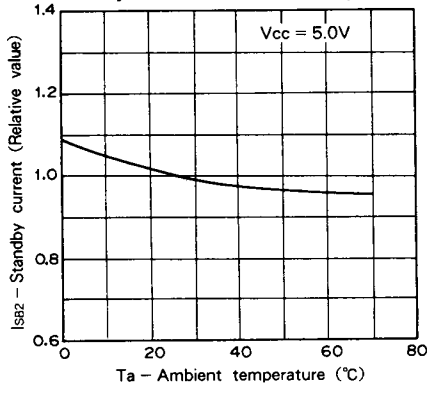
Standby current vs. Ambient temperature



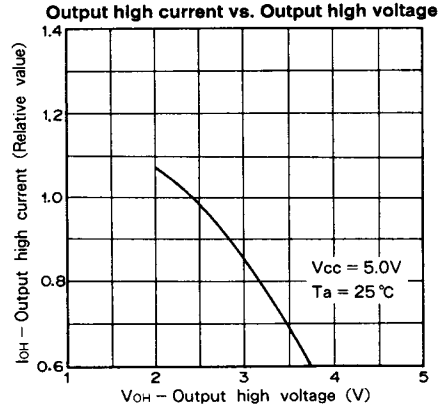
Input voltage level vs. Supply voltage



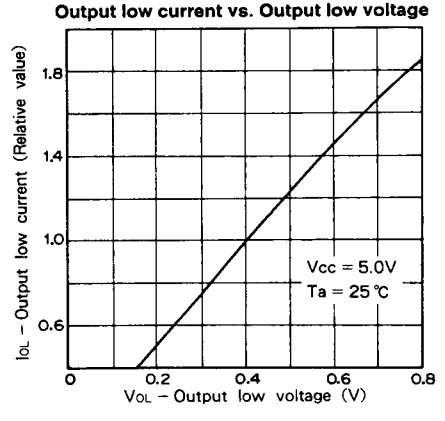
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



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