



OpenSPARC Program

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Agenda

- What is OpenSPARC?
- OpenSPARC University Program
- OpenSPARC Resources


OpenSPARC™

The open-source versions of Sun's UltraSPARC T1 & T2 multithreaded multicore processor designs, including accessible software and hardware stacks.

World's First 64-bit Open Source Microprocessor



Governed by GPLv2



Complete Processor Architecture

- Freely downloadable now:
- OpenSPARC® T1 RTL (Verilog)
- OpenSPARC® T2 RTL (Verilog)
- OpenSPARC T2 developer resources
 - > Documentation
 - > Simulation tools
 - > Verification Package
- Plus other essential CMT developer tools
- And links to partner sites



All available on opensparc.net

OpenSPARC™ Is Building Momentum



“Innovation Happens Everywhere”
~11,000 downloads

OpenSPARC Update

- **New Releases**
 - > T2 Version 1.2 – March 2009
 - > T1 Version 1.7 – April 2009
- **188 teaching & researching CMT technology**
 - > That we *know by name* – many others likely
 - > In 36 countries, the expected ones plus:
 - > Jordan
 - > South Korea
 - > New Zealand
 - > Singapore
 - > Ukraine
 - > Kazakhstan
 - > Tunisia
 - > Latvia
 - > Columbia
 - > Trinidad
 - > Argentina
 - > Peru
 - > Montenegro
 - > Mexico
 - > Egypt

OpenSPARC University Program

University Programs for OpenSPARC

- Sun supports academic use of OpenSPARC
 - > Collaborations
 - > Centers of Excellence (CoE)
 - > For university:
 - > access to real, modern industrial microprocessor designs and full verification test suites!
 - > publicity and prestige that aids in obtaining grants
 - > Sharing of course material on OpenSPARC website
 - > Hosting of projects on OpenSPARC website
 - > Go to <http://www.opensparc.net> to see more

University Uses for OpenSPARC

- Starting point for lab courses
 - > a working design that can be modified for lab projects in computer architecture or VLSI design courses
- Real-world input to test robustness of CAD tools and simulators developed at Univ.
 - > major industry CAD tool vendors already doing this!
- Burn derivative processors into FPGAs
 - > quick design iterations
 - > high-speed emulation
- Trigger spin-off/start-up ventures?

University Uses for OpenSPARC (cont.)

- Experimental processor designs
 - > highly threaded, high-bandwidth network processor
 - > add FPUs, for highly threaded processing node
 - > add co-processors for specialized functions
 - > research into optimizing power efficiency
 - > computer architecture research
 - > add/remove instructions
 - > new operating modes

OpenSPARC Curriculum

Hardware

Computer Architecture
 Micro-Architecture
 VLSI Design
 (frontend & backend)
 FPGA implementation
 I/O, memory interface
 Networking
 Security

Hardware/Software

FPGA
 Hypervisor
 Operating System Port
 HW/SW Co-Design
 Performance Studies

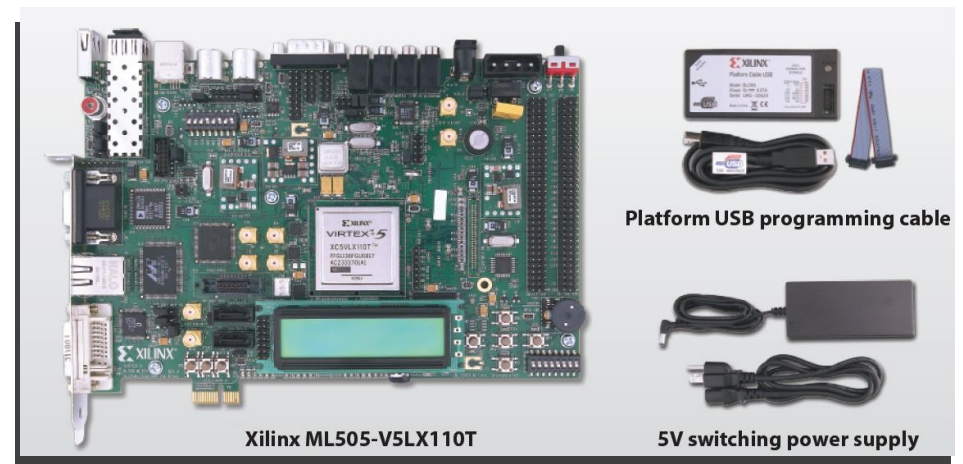
Software

CMT programming
 Developer Tools
 Application Tuning
 Compilers
 Optimization Tools
 Cool Tools
 Algorithm development
 Virtualization

~~~~~*Blend of Teaching, Lab and Research work*~~~~~

# Programs to Support OpenSPARC Teaching and Research

- Server Grants
  - > T2000 or T5120 configurations
  - > Sun internal sponsors submit requests
- FPGA Grants: ~180 requests received since Sept 8!
  - > Xilinx OpenSPARC FPGA Evaluation Platform
  - > Professors submit request at:  
<http://www.opensparc.net/edu/>



# Ten OpenSPARC Centers of Excellence



Carnegie Mellon



ILLINOIS



# China Universities Go Open



- Developing 10 courses using OpenSPARC
- Translating OpenSPARC books to Chinese
- Training workshop for professors Oct. 29, 08

# Taiwan Universities Join OpenSPARC



- Sun Microsystems, Inc., with the support of the Embedded Software Consortium under the Ministry of Education announced today the partnership with National Taiwan University, National Tsing Hua University (NTHU), and National Chiao Tung University to promote OpenSPARC technology development.
- In an announcement held on July 7th, in Taipei, Sridhar Vajapey, Sun Microsystems, gave the opening and talked about OpenSPARC program followed by Dr. Shyu, Dean of EECS of NTHU, representing MOE's SoC program, and Dr. Lee, Professor of NTHU and Director for MOE's ESW program.

# New Center of Excellence: University of Sao Paulo, Brazil



- Courses and Research in OpenSPARC
- 2 day IEEE Workshop on OpenSPARC Architecture
- Ph.D. student presented on current work
  - > Random regression test for OpenSPARC T1
  - > Communication structure performance analysis based on transaction level modeling for OpenSPARC processors

# University Work Highlights:

- **Australia:** High Performance Scientific Computation Courses
- **Canada:** Modeling Throughput of Fine-grained Multi-threaded Architectures & Multi-processor Scheduling
- **India:** Architecture, CMT & VLSI CAD courses
- **Israel:** Concurrent algorithms & Compilation, Multiprocessor programming
- **Mexico:** Coursework in concurrent computing
- **Spain:** Paper on “Improving Search Engines Performance on Multi-threading Processors” accepted at VECPAR 2008; Computer architecture masters courses

# University Highlights, Cont.

- **Sweden:** CMT courses & research
- **Switzerland:** SW Transactional memory
- **UK:** Multiprocessing & concurrent programming courses, FPGA
- **USA:** VLSI design, Coverage-directed test generation, NSF network test bed, Reliability Aware Computer Architecture course, thread scheduling and power, memory models, concurrent data structures, work on findbugs (for heavily threaded programs)

# OpenSPARC Resources

- Downloads
- Books
- Online training
- FPGA
- Curricula

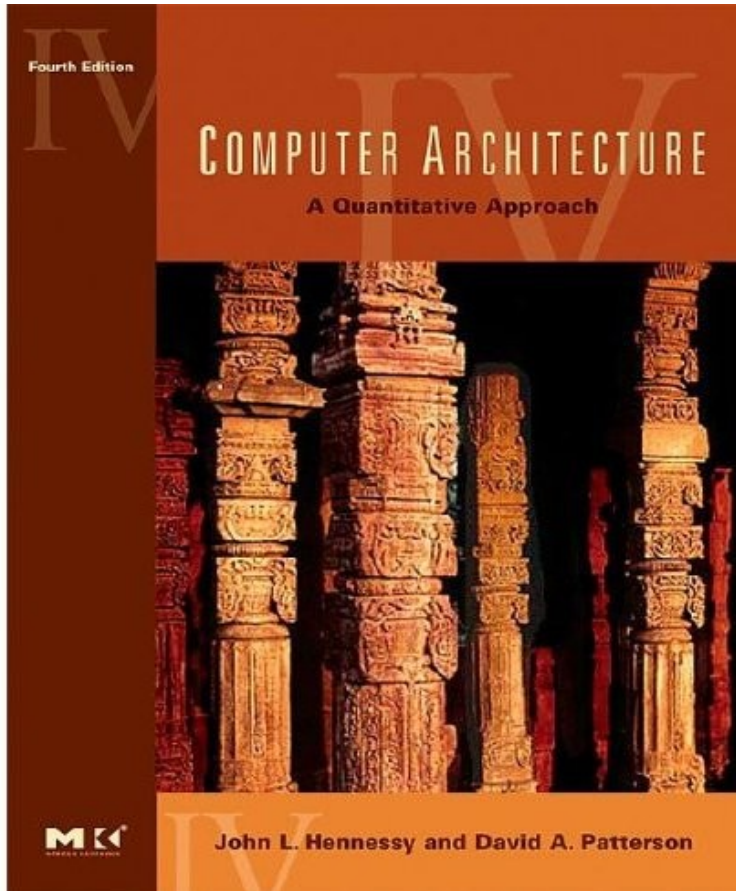
# T1: What's Available- for HW Engineering

- RTL (Verilog) of OpenSPARC T1 design (8 cores, 32 threads – 14 million lines of code!)
- RTL for reduced OpenSPARC, for FPGA
- Synthesis scripts for RTL
- Verification test suites
- UltraSPARC Architecture 2005 spec
- UltraSPARC T1 implementation spec
- Full OpenSPARC simulation environment
- “CoolTools” - including Sun Studio software, SPARC-optimized GCC compiler, development tools, ATS, etc

# T1: What's Available - for SW Engineering

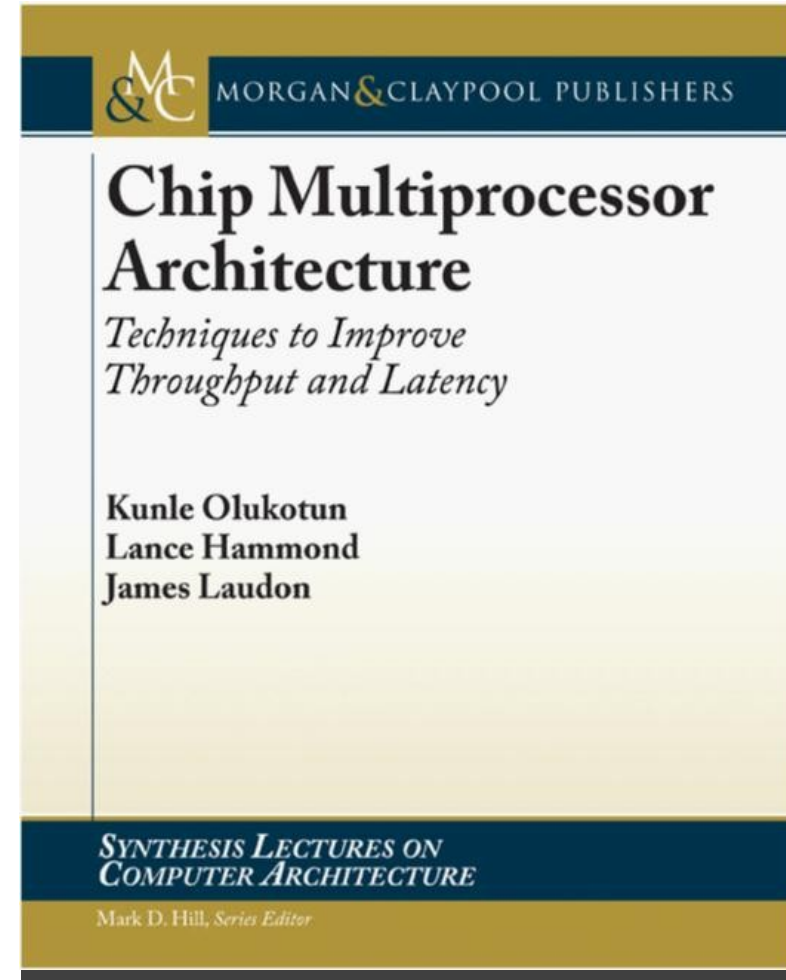
- Architecture and Performance Modeling Package, including:
  - > SAS – Instruction-accurate SPARC Architecture Simulator (includes source code)
  - > SAM – SPARC instruction-accurate full-system simulator (includes source code)
  - > Solaris Images for simulation: Solaris 10, Hypervisor, OBP
  - > Legion – SPARC full-system simulation model for Software Developers (includes source code)
  - > Hypervisor source code
  - > Documentation

# OpenSPARC/Niagara in textbooks



Computer Architecture:  
A Quantitative Approach, 4<sup>th</sup> edition  
by John Hennessy and David Patterson  
Oct. 2006

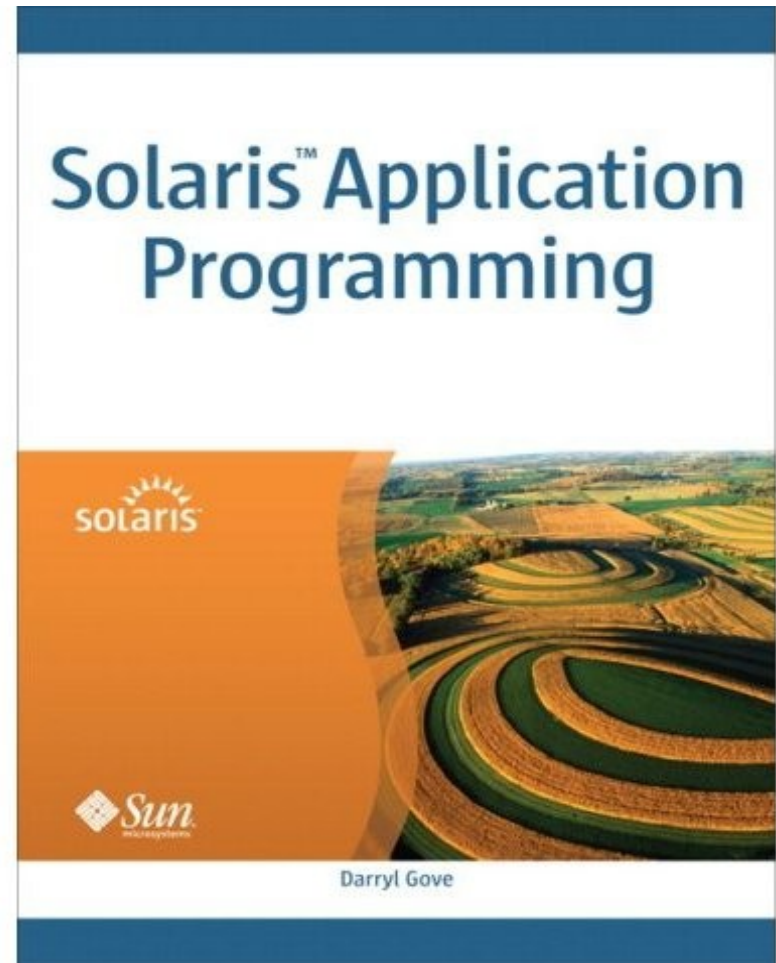
[www.OpenSPARC.net](http://www.OpenSPARC.net)



Published Nov. 2007

# Solaris Application Programming

- Author:
  - Darryl Gove  
Performance Analyst  
Sun Microsystems
    - Published January 2008
  - "Solaris Application Programming ... gives you the background information, tips, and techniques for developing, optimizing, and debugging applications on Solaris."

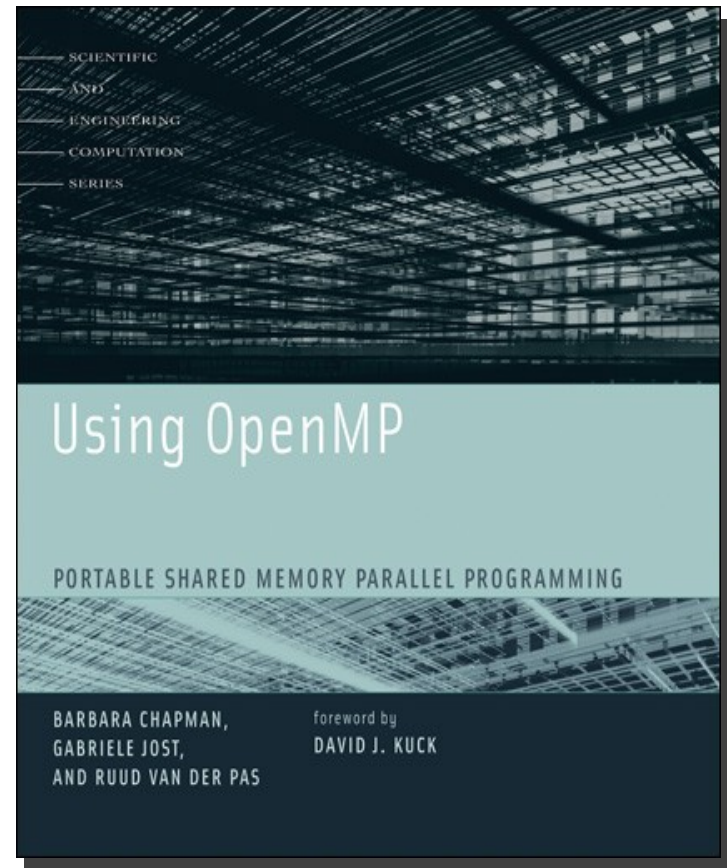


[http://www.sun.com/books/catalog/solaris\\_app\\_programming.xml](http://www.sun.com/books/catalog/solaris_app_programming.xml)

# Using OpenMP

## *Portable Shared Memory Parallel Programming*

- Published October 2007
- Authors:
  - Barbara Chapman  
Professor of Computer Science  
University of Houston
  - Gabriele Jost  
Principal Member of Technical Staff  
Application Server Performance Eng.  
Oracle, Inc.
  - Ruud van der Pas  
Senior Staff Engineer  
Sun Microsystems



# The Book

- Published Nov. 2008
- Written by a team of OpenSPARC designers, developers and programmers
- A “how to” book to guide users as they develop their own OpenSPARC designs.
- Buy on Amazon.com, Lulu.com or download free PDF at [www.OpenSPARC.net](http://www.OpenSPARC.net)
- Over 4300 PDF downloads since Nov. 2008



# New Online Training Available

**Slide-Cast  
Presentations  
by Sun Engineers**

1. OpenSPARC Program
2. Chip Multi-Threading
3. Architecture
4. T1 Overview
5. T2 Overview
6. What's available
7. FPGA
8. Simulators
9. Hypervisor & Virtualisation
10. Compiler
11. OpenSolaris
12. Community Participation

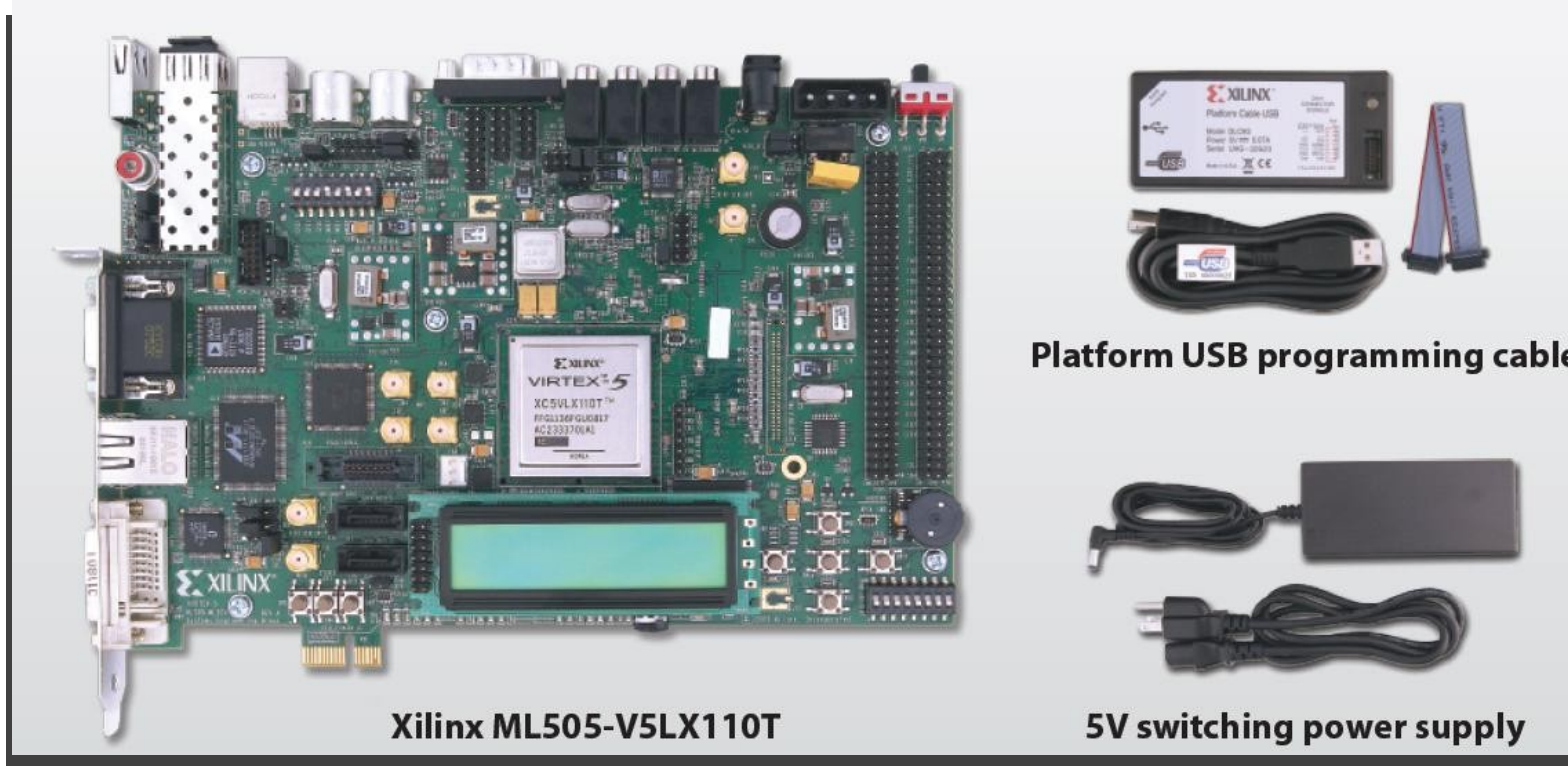
# Partners

- **Europractice**
  - > Over 500 European university members
  - > Using OpenSPARC as reference design
- **Synopsys**
  - > OpenSPARC used in curricula
  - > 90nm library available
- **Nangate**
  - > 45nm Open Cell Library
- **Xilinx**
  - > OpenSPARC Evaluation FPGA kit
    - > More simple to teach and research
  - > Many universities buying kits
- **BeeCube**
  - > FPGA supports 4 cores, 16 threads

# Xilinx OpenSPARC Evaluation Kit

- ML505 board with XC5VLX110T FPGA upgrade
- Includes USB interface for FPGA programming
- Tested with OpenSPARC T1 release 1.6 design
- Ships with:
  - > FPGA Board, with power supply & 256 MB DRAM
  - > Platform USB download cable
  - > Host to host SATA crossover cable
  - > Compact flash card with OpenSPARC T1 1.6 ace files

# Kit Contents



# Curricula: Use Others', Share Yours

- Growing community of faculty using and sharing their OpenSPARC curriculum

## Wayne State University

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- [ECE 4680: Computer Organization and Design](#)
  - Winter 2008: Taught by [Nabil J. Sarhan](#)

-- [NabilSarhan](#) - 04 Apr 2008

## Lamar University

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- Point of contact: [Jane Liu](#)
- Class Information
  - [COSC 4310: Introduction to Computer Architecture](#)
    - Spring 2008: Taught by [Jane Liu](#)
- Material to offer for sharing
- Material adopted from elsewhere

## The Australian National University

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- \* Point of contact: [Peter Strazdins](#)
- Class Information
  - [COMP2300/COMP6300: Introduction to Computer Systems](#)
    - Semester 1 2008: Taught by [Peter Strazdins](#)
    - [Semester 1 2007](#): Taught by [Peter Strazdins](#)

# More Curricula Available

## Community Members

### Brown

- [CS176: The Art of Multiprocessor Programming](#)
  - Fall 2007: Taught by [Maurice Herlihy](#)

### Dresden University of Technology

- [Foundations of Concurrent and Distributed Systems](#)
  - Summer 2007: Taught by [Christof Fetzer](#)

### Harvard

- [CS165 Introduction to Information Management](#)
  - Spring 2008: Taught by [Margo Seltzer](#)
  - [Fall 2006 web page](#)

### MIT

- [6.170: Laboratory in Software Engineering](#)
  - Fall 2007: Taught by [Martin Rinard](#) & Sivan Toledo

### Purdue University

- Point of contact: [Tony Hosking](#)
- [CS 490M: Multicore Architecture](#)
  - Spring 2008: Taught by [Zhiyuan Li](#)
- [CS 390C - Principles of Concurrency and Parallelism](#)

## Rice University

- [COMP 422: Introduction to Parallel Computing](#)
  - Spring 2008: Taught by Vivek Sarkar & [Bill Scherer](#)
  - Previous version: Spring 2007: <http://www.owl.net.rice.edu/~comp422/>

## Simon Fraser University

- [Multicore bibliography portal](#)
- [CMPT 886: Special Topics in Operating Systems and Computer Architecture](#)
  - Spring 2007: Taught by [Sasha Fedorova](#)
- [CMPT 886: Special Topics in Operating Systems and Computer Architecture](#)
  - Spring 2008: Taught by [Sasha Fedorova](#)
  - This web site has a homework assignment that teaches students how to use teaching students how to use Simics, and a good collection of papers on mu

## SUNY Oswego

- [CS375: Concurrent Programming](#)
  - Fall: Taught by [Doug Lea](#)
- [CS445: Computer Networks](#)
  - Spring: Taught by [Doug Lea](#)

## Technion

- [Assaf Schuster](#) will be teaching ...

## Tel Aviv University

- [0368-3469: The Art of Multiprocessor Programming](#)
  - Spring 2007: Taught by [Nir Shavit](#)

# Why OpenSPARC?

- View Excerpts from Education and Research Conference 2008, Carnegie Mellon University Professor Dr. James Hoe's highlights from the Panel Discussion at the ERC. (7:27) at

<http://www.opensparc.net/publications/videos/erc-highlights-dr.-james-hoe.html>

The screenshot shows the OpenSPARC website homepage. The header features the OpenSPARC logo in orange and blue, with the tagline "World's First Free 64-bit CMT Microprocessors" in yellow. Below the header is a navigation bar with five orange buttons: "Home", "Get The Source", "Get Informed" (which is highlighted with a dark blue background), "Get Connected", and "Get Cool Tools". Underneath the navigation bar is a green section with "Get Involved" and "Site" links. A breadcrumb trail shows "Home" with a star icon, followed by "Get Informed" with a star icon, "Publications" with a star icon, "Videos" with a star icon, and "ERC Highlights - Dr. James Hoe". To the right of the breadcrumb trail are "Search" (with a magnifying glass icon), "Contact Us" (with an envelope icon), and "About" (with a gear icon). At the bottom, a blue banner contains a white paper thumbnail and the text: "This white paper highlights the technical benefits Sun's chip multithreading (CMT) ...".

# open

64 bit, 64 threads, and free

<http://OpenSPARC.net>

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# OpenSPARC Program

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