LESSON 17:
TIME DIVISION SWITCHING

Objective
To provide a detailed understanding of the concepts, principles of time division switching.

Introduction
We already studied that in single-stage space division switching networks, a crosspoint switching element is used to establish a specific connection between two subscribers. A conversation in multistage space division switching networks could be established via anyone of the many alternative paths. In other words we can say that across point is usable for establishing more than one connection. It means that a crosspoint is sharable among many subscribers.

The number of switching elements in multistage space division switching networks is reduced due to sharing of a crosspoint among many subscribers. A switching element, once allotted, remains dedicated to a connection for its entire duration. As a result, saving of a crosspoint occurs from one connection to the next. At a time, a crosspoint element is dedicated to one active speech circuit. Continuous analog speech waveform is passed through the switch in pace division switching. Such type of waveform needs dedicated crosspoint element.

In digital transmission, sampled values of speech are sent as pulse amplitude modulated (PAM) values or pulse code modulated (PCM) binary words. A sample occurs every 125 msecond for a sampling rate of 8kHz. In the digital domain, a sample value can be passed from an inlet to an outlet in a few microseconds or less, through a switching element. As a result, during 125 msecond sampling interval, a dedicated switching element remains unused for most of the time, say for over 120 ms. If we can establish a dynamic control mechanism whereby a switching element can be assigned to a number of inlet- outlet pairs for a few microseconds each, a single switching element can be used to transmit speech samples from a number of inlets to the corresponding outlets. In other words a switching element can be shared by a number of simultaneously active speech circuit.

This is the principle of time division in switching. By using this principle of time division switching, the switching elements are shared in time division switching. Therefore, much greater savings can be achieved in the number of switching elements when compared to multistage space division switching.

Basic Time Division Space Switching (Tdss)
A simple N x N Time Division Space Switch is shown in Fig.17.1 (a). The equivalent form of N x N time division space switch for two stage network with N x 1 and 1 x N switching matrices for the first and the second stages, respectively, are shown in Fig.17.1(b). This two-stage network has one link interconnecting the two stages. Each inlet/outlet is a single speech circuit corresponding to a subscriber line. The speech is carried as PAM analog samples or PCM digital samples. These samples are occur at 125 ms intervals.

Analog Time Division Switching
When PAM samples are switched in time-division manner, then such type of switching is called Analog Time Division Switching.

Digital Time Division Switching
When PCM digital (binary) samples are switched in time division manner, then the switching is known as Digital Time Division Switching.

Interconnecting link in Fig.17.1 (a) is shown as bus to which a chosen inlet-outlet pair can be connected by a suitable control mechanism and the speech sample transferred from the inlet to the outlet.

If the PAM samples are switched, the bus is analog in nature. If the PCM samples are switched the bus is digital in nature.

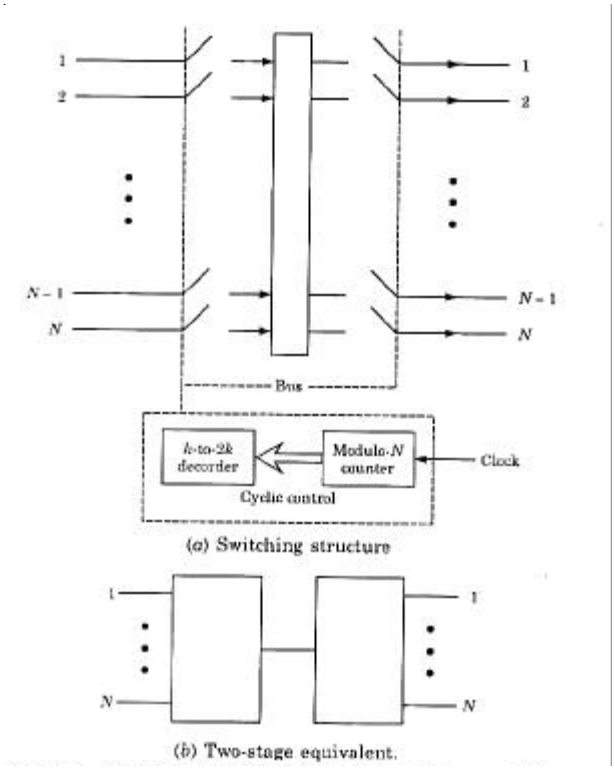

Fig. 17.1 Illustration of simple PAM time division switching.

The number of simultaneous conversations that can be supported on a network is called switching capacity (SC). The switching capacity (SC) of a network of this kind is inversely proportional to the time required to select and connect an inlet-

outlet pair and transfer the speech sample from the inlet to the outlet.

$$SC = \frac{125}{t_s} \text{.....Eq.1}$$

where,

t_s = Time required to setup a connection and transfer the sample value in microseconds.

The selection of inlet /outlet is controlled dynamically. The simplest form of control is to select the inlets and outlets in a cyclic manner in synchronism. In cyclic manner (in synchronism) there is a fixed one-to-one correspondence between the inlets and the outlets. We suppose a cycle starts at inlet/outlet 1 and proceeds as 2, 3, 4, ..., N, and so on, then we can say that inlet i is always connected to outlet i. In effect, there is no switching in the true sense except that a single switching element is being shared by all the connections. The cyclic control is organised using a modulo-N counter and k-to-2^k decoder. It is shown in Fig. 17.1 (a). N and k are related by the equation,

$$k = \lceil \log_2 N \rceil \quad \text{.....Eq.2}$$

where the symbol [ ] is a ceiling function. It gives the lowest integer equal to or higher than the quantity inside the symbol.

Since all the inlets and outlets are scanned within 125 ms, the switching capacity (SC) of the network is the same as the number of inlets or outlets in the system and the switch is nonblocking. It cannot provide full availability, as it is not possible to connect any inlet to any outlet.

Input Controlled Time Division Space Switch

If we make one of the controls such as on the output side, where memory is based then full availability can be obtained. Such a scheme is shown in Fig.17.2. The input side is cyclically switched. There is a control memory on the output side, which contains the addresses of the outlets stored in contiguous locations in the order in which they are to be connected to the inlets. For example; an address sequence 4-7-1-5 stored in locations 1,2,3 and 4 of the control memory implies that inlet 1 is connected to outlet 4, inlet 2 to outlet 7, inlet 3 to outlet 1 and inlet 4 to outlet 5. This switch is called Input Controlled (or Input driven). Here outlet is chosen on the basis of inlet that is being scanned at any instant of time.

The modulo-N counter of the cyclic control also acts as Memory Address Register (MAR) of the control memory. The control memory has N words corresponding to inlets. The width of this control memory is élog$_2$ Nù bits which are used to address the N outlets. Cyclic control at input means that all the subscriber lines are scanned irrespective of whether they are active or not. For an active inlet i, the corresponding outlet address is contained in the i^{th} location of the control memory. The outlet address is read out and passed to the address decoder. This decoder also acts as the memory data register (MDR) of the control memory. The decoder output enables the proper outlet to be connected to the bus. The speech sample value is then transferred from the inlet to the outlet.

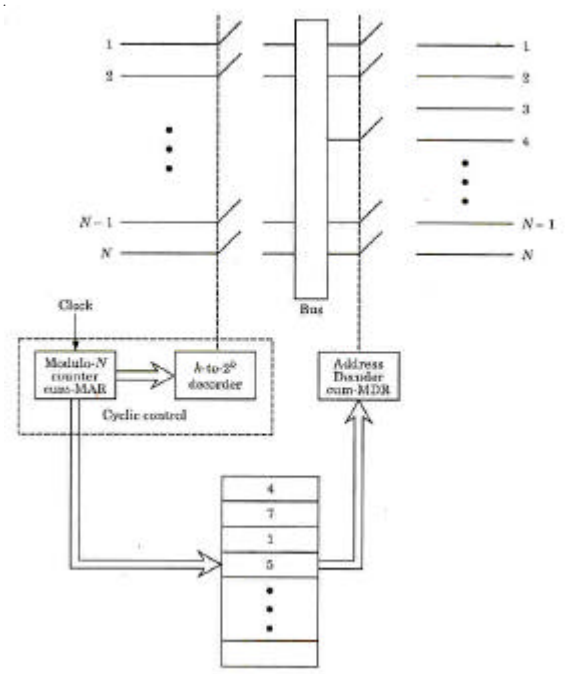

Fig.17.2 Input-controlled time division space switch.

Thus, any inlet i can be connected to any outlet k, which ensures full availability. If any inlet is not active then the corresponding location in the control memory contains a null value. This null value forbids the address decoder from enabling any of the output lines. Since a single switching element is being time-shared by N connections all of which are active simultaneously. Therefore, a physical connection is established between the inlet and the outlet for the duration of the sample transfer. This switching technique is called **Time Division Space Switching (TDSS).**

Output-controlled time division space switch

We can also organise a fully available time division space switch with cyclic control for the outlets and control memory based selection for the inlets. It is shown in Fig.17.3. In such a case, the switch is called output controlled because each location of the control memory is rigidly associated with a given outlet. For both input and output controlled time division space switch, the number of inlets or outlets N are equal to switching capacity (SC).

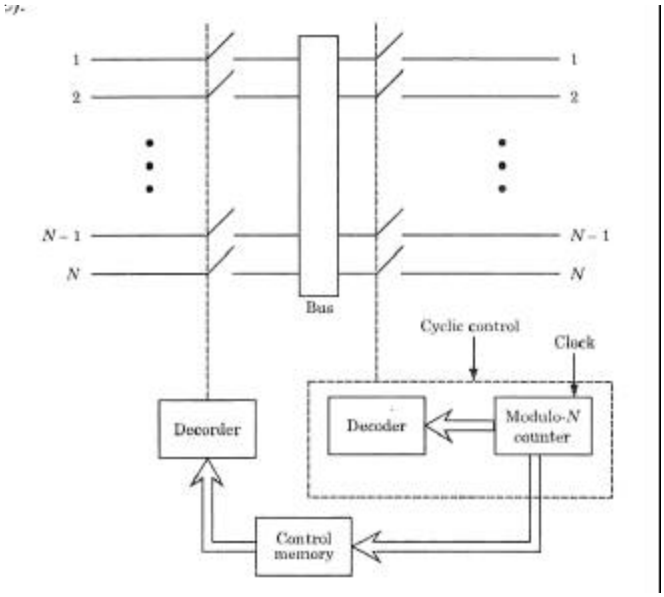

Fig.17.3 Output-controlled time division space switch.

It is given by,

$$N = SC = \frac{125}{t_i + t_m + t_d + t_t} \quad \ldots\ldots\ldots\ldots \text{Eq.3}$$

where,

t_i = Time to increment the modulo N counter

t_m = Time to read the control memory

t_d = Time to decode address and select the inlet or outlet as the case may be

t_t = Time to transfer the sample value from inlet to outlet.

All time values are expressed in microseconds. Eqs.1 and 3 are valid for an 8-kHz sampling rate and a non-folded network. The clock input to the modulo-N counter has a rate such that N- sample transfers are organised in 125 ms.

$$\text{Clock Rate} = 8\ N \text{ kHz} \quad \ldots\ldots\ldots \text{Eq.4}$$

The output-controlled Time-Division Space Switches are capable of supporting broadcast connections. But the input-controlled Time- Division Space Switches cannot be used for broadcast connections. Broadcast takes place when all the control memory locations contain the same inlet address, in which case, the data from the specified inlet is transferred to all the outlets.

Upto now we have assumed that speech samples are transferred m inlet to outlet. In practical telephone conversations, speech samples have to be exchanged both ways. For this purpose, two independent buses may be used. In these buses, data transfers take place simultaneously in opposite directions. Alternatively, a single bus may be used to organise the two-way data transfer first in one direction and then in the other. Digital buses usually support parallel data transfer. If the incoming data is in serial form it is passed through a serial-to-parallel converter before being fed to the bus. Similarly, a parallel-to-serial converter is required on the output side.

The input or output-controlled time-division space switch configurations can be used to support folded network connections. These configurations (with single bus) support two-way transfers for folded networks.

We can illustrate this by considering a connection between subscriber 4 and subscriber 27 in an input-controlled switch. The control memory location 4 contains the value 27 and the location 27 contains the value 4. When the subscriber line 4 is scanned by cyclic control, the input sample from the up (transmit) line of the subscriber 4 is transferred to the ring (receive) line of the subscriber 27.

When the subscriber line 27 is scanned, the input from the line 27 is transferred to the ring line of the subscriber 4.

Thus, data samples are exchanged both ways in one 125-ms cycle: When the switches are operated in this fashion, the Eqs.1, 3 and 4 are applied to folded networks as well.

We know that only N /2 simultaneous conversations are possible in a folded network. Therefore, this network can be used to arrive at another switch configuration with only N/2 control memory locations. In this case, no cyclic control is possible and both the input and output are memory controlled.

First we discuss design parameters of a time-division space switch and compare the same with that of a space division switch. Then we discuss configuration of such type of switch.

Let us assume same unit cost for each switching element and for each word of the control memory. The stored program control (SPC) may be ignored, as it is of the same order irrespective of whether the switching network uses space-division or time-division techniques.

For non-folded networks, we have

Number of switching elements on the input side = N

Number of switching elements on the output side = N

Total Number of switching elements = 2N

Switching capacity, SC = N

Traffic handling capability, TC = 1

Cost of the switching network

= Cost of the switching elements + cost of the control memory

= 2N + N = 3N

$$\text{Cost Capacity index, ICC} = \frac{N}{3N / N} = \frac{N}{3}$$

Obviously, time division networks are more cost effective than space division networks. That is why most of the present day switching systems uses time-division techniques.

Memory-Controlled Time Division Space Switch

The use of cyclic control in input or output controlled switches restricts the number of subscribers on the system rather than the switching capacity. This is because cyclic control demands that all the subscriber lines be scanned irrespective of whether they are active or not. In practice, the number of active subscrib-

ers is only 20% of the total subscribers. A switch configuration based on the use of control memory for controlling inlets and outlets would permit a much larger number of subscribers than the switching capacity (SC) of the network.

A switch configuration based on the use of control memory can be made to function either as a folded or a nonfolded network. Such type of switch configuration is called memory controlled time division space switch. It is shown in Fig. 17.4.

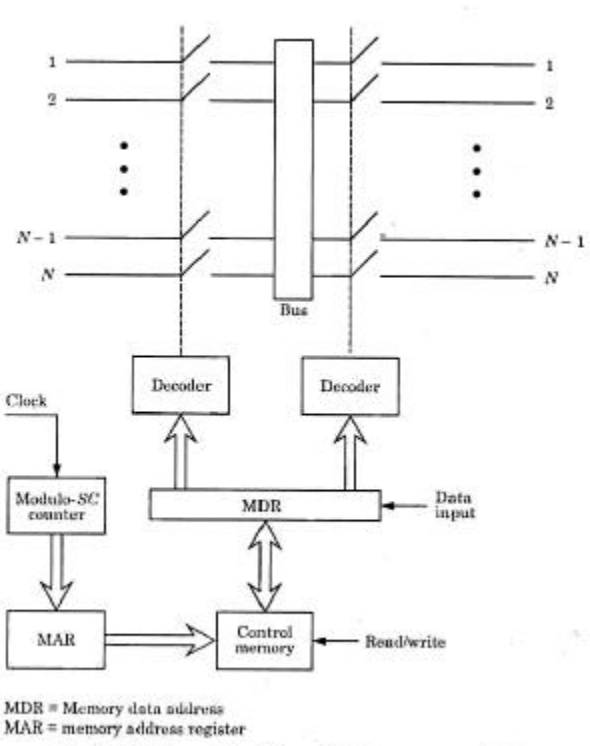

Fig. 17.4 Generalised time division space switch.

The memory-controlled time division space switch is more general and versatile than the input or output controlled structures. In memory controlled structure, each word of the control memory has two addresses:

1. An inlet address
2. An outlet address

The control memory width is $2\lceil \log_2 N \rceil$

The operation of memory-controlled switch:

The modulo – SC counter is updated at the clock rate. The control memory words are read out one after another. The inlet address is used to connect the corresponding inlet to the bus. Similarly, outlet address is used to connect the corresponding outlet to the bus. Next, the clock updates the counter and the cycle of the operations is repeated.

When a connection is to be set up between inlet k and outlet j, the two addresses are entered into one of the free locations of the control memory via the data input facility and the location is marked busy.

When the conversation finishes, the two addresses are replaced by null values and the location is marked free. The information regarding a location (either busy or free) may be maintained in a bit vector. In bit vector, one bit corresponds to one location in the control memory. If a bit is set, the corresponding location is busy, otherwise, it is free. The busy/free vector and the data input are managed by the SPC processor. There is no reservation of the control memory location for particular inlets and outlets or inlet- outlet pairs unlike in case of input or output controlled network configurations.

The number of words in the control memory and the size of the modulo counter are equal to the switching capacity (SC) of the network and have no relation to the number of subscribers connected to the network.

The switching capacity (SC) is given by

$$SC = \frac{125}{t_s} \quad \text{.....Eq.5}$$

and clock rate is given by clock rate = 8 x SC, kHz Eq.6

where,

$$t_s = t_i + t_m + t_d + t_t$$

If the time to read the memory, t_m of t_s, is the dominating factor in eqn.5, it means that the control memory is busy throughout the sampling interval of 125 ms. Some write cycles are required to input data into the memory whenever a new connection is established or an existing connection is terminated.

We made a provision for this. Such a provision is dependent on the number of new connections or terminations that may occur during each sampling interval. However, t_m is a very small number (fraction of a call). It is adequate if one write cycle is reserved for the input purpose in every sampling interval.

If t_m is not the dominant factor, changes to the contents of the control memory may be done while other operations are being performed. But usually, t_m is the dominant factor.