LESSON 18:
BASIC TIME DIVISION TIME SWITCHING

Objective

To provide a detailed understanding of the concepts basic time division time switching

Introduction

Basic Time Division Time Switching (Tdts)

Another way of organising time division switching is use a memory block in place of the bus. Here sampled speech values are provided as PCM samples and not. PAM samples. The functional blocks of a memory based time division switch is shown in Fig. 18.1 (a). Its equivalent circuit is shown in Fig. 18.1 (b). In this organisation, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and outgoing data usually is in the serial form. But the data are written into or read out of the memory in parallel form. So, it is necessary to perform serial-to-parallel conversion and parallel-to-serial conversion at the inlets and outlets respectively. For convenience, the data-in and data-out parts of the MDR are shown separately for the data memory in Fig. 18.2. Although in reality, MDR is a single register. Since there is only one MDR, a gating mechanism is necessary to connect the required inlet/outlet to MDR.

This gating mechanism is done by the in-gate and out-gate units. There is no physical connection, even momentarily, between inlets and outlets in the case of data memory based operation. But we already know that there is physical connection between inlets and outlets in case of time division space switches. Further, the information in memory based operation is not transferred in real time. It is first stored in the memory and later transferred to the outlet. There is a time delay between the acquisition of sample from an inlet and its delivery to the corresponding outlet. The data memory-based scheme is also called Time Division Time Switching (TDTS).

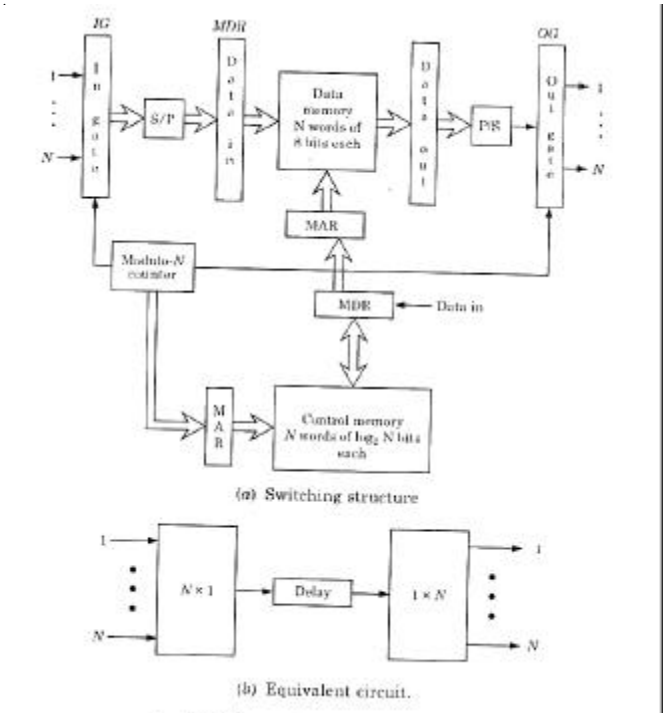

Fig. 18.1 Illustration of basic time division

We have already studied about input controlled, output controlled or memory controlled time division space switches in some of the previous sections. In similar-fashion, a time-division time switch may be controlled in any of the following three ways:

1. Sequential Write/Random Read
2. Random Write/Sequential Read
3. Random Input/Random Output

In the first two methods of control, the Sequential/Random, Read / Write operations refer to the Read/Write operations associated with the data memory. In both these cases, the inlets and outlets are scanned sequentially.

In third method, the inlets and outlets are scanned randomly and the data memory is accessed sequentially.

Following two modes are used to operate Time Division Time-Switch under any of three forms.

1. Phased operation
2. Slotted operation.

Phase Operation

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This operation of Time Division Time Switches proceeds in two phases.

When the method of control is sequential Write/Random Read, the inlets are scanned in the first phase one after another and the data is stored in the data memory sequentially. There is a one-to-one correspondence between the inlets and the locations of the data memory. In other words, the data memory location corresponds to inlet. The control memory locations, 1, 2, 3, ..., N, contain the addresses of the inlets corresponding to the outlet 1, 2, 3, ..., N.

The inlet addresses are read out from the control memory in the second phase. The corresponding locations in the data memory are accessed and the data transferred to the outlets in sequence. Since any inlet may be connected to any of the outlets because the inlet addresses are randomly distributed in the control memory.

Consequently, the read access to the data memory is random. Since the write access to the data memory in the first phase proceeds, sequentially and the read access in the second phase randomly. A nomenclature Sequential writes/random read to describe this form of control. So, we can, note here that the inlets, outlets and the ~ control memory are accessed sequentially.

In the first phase, one memory write is involved per inlet. But in the second phase two memory reads (one at the control memory and the other at the data memory) are involved per outlet. The time taken for the two-phase operation is given by

$t_s = Nt_d + N(t_d + t_c)$ ……Eq.1

where,

t_d = read/write time for the data memory

t_c = read/write time for the control memory

If $t_d = t_c = t_m$, we have

$T_s = 3Nt_m$

Since the entire operation is to be completed within 125 ms, we have the expression for the number of subscribers as,

$$N = \frac{t_s}{3t_m}$$

$$N = \frac{125}{3t_m}, \text{ since } t_s = 125 \text{ ms} \quad \ldots\ldots\ldots\ldots\text{Eq.2}$$

Where t_m is expressed in microseconds.

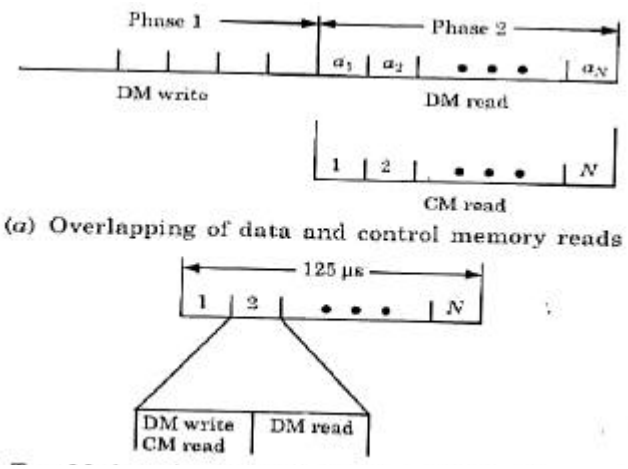

Fig. 18.2 Two-Modes of operations of time division time switches.

The number of subscribers can be increased by overlapping the read cycles of the data memory and the control memory in the second phase of operation as shown in fig.19.2 (a). During the last cycle of the phase 1, the first location of the control memory which contains an inlet address, say a_1, is read. During the first cycle of the second phase, the location a_1 of the data memory and the second location of the control memory are read out simultaneously. Thus equation may be modified for overlapped operation as

$$N = \frac{125}{2t_m} \quad \ldots\ldots\ldots\ldots\text{Eq.3}$$

In the slotted operation the 125 ms period is divided into N subperiods of duration 125 / N. In each subperiod, the following operations are performed:

1. Read inlet i and store the data in data memory location i
2. Read the location i of the control memory which contains the value, sayj
3. Read the data memory location i and transfer the data to outlet i.

The first two operations are carried out simultaneously such that the eq.3 holds valid for this mode of operation which is depicted in fig.19.2 (b).

For example, in the phased mode of operation the modulo-N counter goes through two cycles for the operation as against only one cycle in the slotted mode. The data transfer from inlets to the data memory can be organised using Direct Memory Access (DMA) facility in the phased mode operation. But data transfer from inlets to the data memory in slotted mode of operation is not organised by DMA.

In the phased mode of operation, samples transferred to the outlets belong to the same 125 ms period in which they were acquired. But in slotted mode of operation, the sample values may belong to the previous 125 ms period, thus it introduces on sample delay between the inlet and the outlet.

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In random write/sequential read form of control, the control memory contains the addresses of outlets corresponding to the outlets. In the first phase, the control memory is read and inlet data is written into the data memory location specified by the contents of the control memory. The inlets are scanned sequentially but the data are written into the data memory randomly.

In the second phase of operation, the data memory is read out sequentially and the data sent to the outlets sequentially.

The inlets and the data memory locations have no correspondence in each other. But, there is one-to-one correspondence between the outlet and the data memory locations. Now we can note that there is one-to-one relationship between inlets and the control memory locations.

Both eqns. N = 125/3tm and N =125/2tm are applicable to random Write Sequential read form of control as well. The overlapped operation corresponding to Eqn. N =125/2tm implies that the first read cycle of the control memory will be overlapped with the last read cycle of the data memory in previous 125-ms cycle. In other words, we can say that the' writing into the data memory proceeds simultaneously with the reading of the control memory locations. While the contents of the I^{th} location of the control memory is being used as address for the data memory to write data into, the $(i + l)^{th}$ location of the control memory is read out.

It is shown in Fig. 3.34.

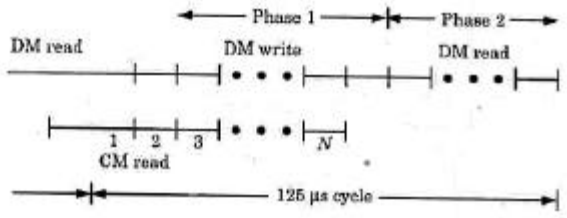

Fig. 18.3 Overlapping of data memory write and control memory read operations.

Both Sequential Write/Random Read and Random Write/ Sequential Read controls impose a serious restriction on the number of subscribers that can be connected to the system. Since all the inlets and the outlets are scanned irrespective of whether they are active or not. Therefore, the total number of subscribers is limited to the number of Read/Write operations that can be performed in a 125 μs interval.

In other words we can say that the number of subscribers is not more than the switching capacity (SC) of the system. Switches are obviously non-blocking. If we have a scheme whereby only the active subscribers are scanned, then the total number of subscribers connected to the system can be increased significantly.

Random Input/Random Output Time Switch

Random Input/Random Output form of control permits a larger number of subscribers than switching capacity SC of the system. The switch in this case is; however, blocking in nature. Fig. 18.4 shows the Random Input/Random Output Scheme.

Functionally, this scheme comprises of two control Memory modules, CMl and CM2. These modules (CM1 and CM2) hold the addresses of the active inlets and outlets, respectively. There is a one-to-one correspondence between the two locations of the two control memories. If the address of an active Inlet is placed in the location *x* of control memory module CM1 then the address of the outlet to which this inlet is connected, is placed in the location *x* of CM2. The phased operation of Random Input/Random output time switch also proceeds in two phases.

In the first phase, the addresses of the active inlets are read out of CM1 one by one and the data transferred from the respective inlets to the data memory starting from its first location.

In the second phase, the addresses of the outlets are read out of CM2 and the data from the data memory is transferred to the outlets specified by these addresses. In each phase, two memory read/write operations are involved. As a result, the Switching Capacity (SC) of the system range expressed as

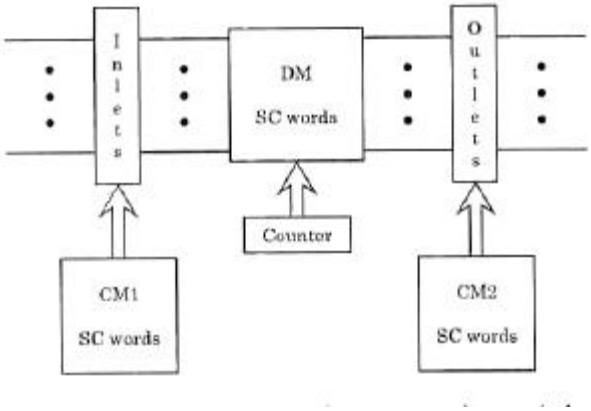

Fig. 18.4 Random input/ random output time switch.

By overlapping the control memory and the data memory operations the switching capacity will be doubled. In this case, SC can be expressed as

$$SC = \frac{125}{4\,t_m} \qquad \text{.....Eq.4}$$

By overlapping the control memory and the data memory operations the switching capacity will be doubled. In this case, SC can be expressed as,

$$SC = \frac{125}{2\,t_m} \qquad \text{.....Eq.5}$$

With the advent of integrated semiconductor memories, dual port memory chips, where two accesses can be made simultaneously, are commonly available. Input and output operations can be done simultaneously by using these memory chips. Therefore, these provide double switching capacity. However, one sample delay occurs in the process because the sample value is sent to the outlet, corresponding to the previous 125 μs cycle. In this case, the two control memories are read out simulta-

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neously. Alternatively, only one control memory may be used with each location containing both the inlet and the outlet addresses.

By using overlapped and deal port memories and overlapped, the *i* switching capacity can be given as,

$$SC = \frac{125}{t_m} \quad \text{……..Eq.6}$$

Entries in the control memory modules specify the active inlet/ outlet pairs. Whenever a call is established, the corresponding inlet and outlet addresses are entered in CM1 and CM2, respectively at the same location addresses. When a call is completed or terminated, the corresponding entries are set to null values. .

The entries in the control memory can be managed in any of the three ways. These are:

1. By maintaining a free list
2. By compacting the entries every time a call terminates.
3. By maintaining free and occupied lists.

The free list is a linked list which maintains information about the free locations in the control memory. This list is organised by using First-Come-First-Served (FCFS queue) or Last-Come-First-Served (LCFS stack) discipline. Wherever a call is to be set up, a free location is obtained from this list. Whenever a call is terminated, the free location is added to the list. The free locations are distributed throughout the control memory interspersed with the busy locations. When a free list alone is used for managing the entries in the control memories, all locations of these memories have to be scanned in the respective phases of operation. Whenever a free location is encountered with a null value, the data transfer between the inlet and the data memory or between the data memory and the outlet will not take place.

Thus, the time required to complete the two phases of operation is given by,

$T = 4 N_p t_m + 2 (SC - N_p) t_m$, μs Eq.7

where, N_p = Number of active subscriber pairs

Eqn.7 corresponds to the case where single port memory chips are used. There is no overlapped operation. The remaining time, i.e., (125 -T) μs in the 125 -μs cycle may be used for maintenance and diagnostic purposes.

According to all the locations of the control memory can be avoided by maintaining an occupied list in addition to the free list. In this case, only those locations in the occupied list are accessed and therefore Eqn.7 can be written as,

$T = 4 N_p t_m$ Eq.8

Maintenance of the lists can be done away with if compaction is resorted to every time a call terminates. Compaction means that all entries corresponding to active inlet/ outlet pairs are gathered at the beginning of the control memory. In this case, the control memory access is terminated as soon as a location with null value is encountered.

The time taken to complete the two phases of operation is given by,

$T = 4 N_p t_m + 2 t_m$ ……...Eq.9

The free list or occupied list is usually managed by using pointers. Every entry in the list now consists of two parts. These parts are: Data and a pointer to the next entry in the list.

For a free list, data value part has no significance. The beginning of the list is identified by a variable. This variable contains the address of the first free or occupied location which, in turn, points to the next free or occupied location.

Thus, a link is established to all the free or occupied locations. The last free or occupied location contains a null pointer. This shows in Fig. 18.5 (a). At the head of the free list is location 7. It is indicated by the free list pointer (FLP). The free list comprises of locations 7, 9, 3, 10, 5, 4 and 1. The first location of the occupied list is 2 it is indicated by the occupied list pointer (OLP). Thus, occupied list is 2-11-12-8-6.

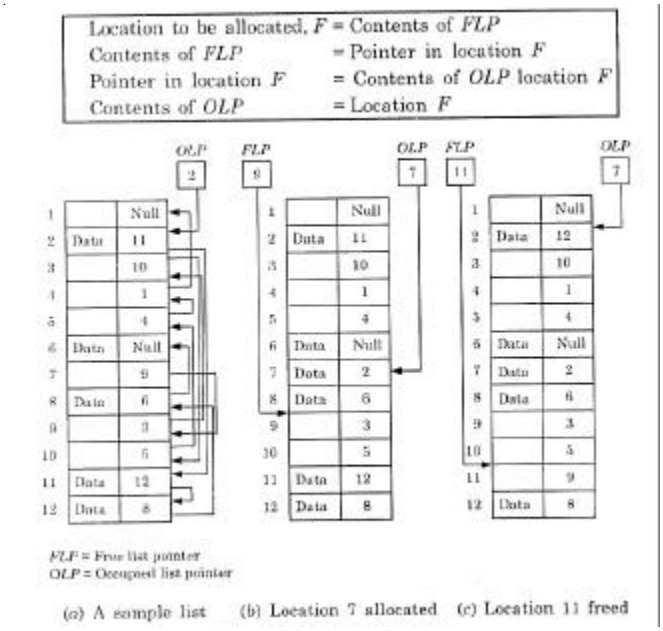

Fig.18.5 List of management

There are two fundamental list management operations for any list.These operations are:

1. Add an Item to the list
2. Remove an Item from the list

In the case of free and occupied lists (both lists have the same set of memory locations), a location is added to the free list when it is taken out of the occupied list and vice-versa.

The actions involved in these operations are:

1. Allocate a location from the 'free list to the occupied list

   Location to be allocated, F = Contents of FLP

   Contents of FLP = Pointer in location F

   L Pointer in location F = Contents of OLP location F

   Contents of OLP = Location F

Status of the lists after the first location in the free list is moved to the occupied list is shown in Fig 18.5 (b).

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The free list now is 9-3-10-5-4-1 and the occupied list is 7-2-11-12- 8-6.

2. Free the location X from the occupied list and add to the free list

Pointer in the predecessor of X	=	Pointer is X
Pointer in X	=	Contents of FLP
Contents of FLP	=	X

List status after location 11 is freed from the occupied list and added to the free list.

The new free list is 11-9-3-10-5-4-1 and the new occupied list is 7- 2-12-8-6.

Notes

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