LESSON 19:
TIME-MULTIPLEXED SPACE SWITCHING (TMSS) AND TIME MULTIPLEXED TIME SWITCHING (TMTS)

Objective

To provide a detailed understanding of the concepts Time multiplexed space switching and time multiplexed time switching

Introduction

Time-multiplexed Space Switching (Tmss)

We have already studied about time-division space switch and time division time switch in previous sections. In these switches an inlet or an outlet corresponding to a single subscriber line with one speech sample appearing every 125 ms on the line is used. Such switches are used in local telephone exchanges.

Now, we discuss here switches that are required in transit telephone exchanges were, the inlets and outlets are trunks which carry time division multiplexed data streams. These switches are called Time-multiplexed switches. Time multi-plexed switches are of two types:

1. Time Multiplexed space switches

2. Time Multiplexed time switches.

In this section, we discuss time-multiplexed time switches.

A time multiplexed time-division space switch is shown in Fig. 19.1

There are N incoming trunks and N outgoing trunks. Each trunk carries a time-division multiplexed stream of M samples per frame. Each frame is of 125mS time duration. In one frame time, a total of MN speech samples have to be switched. One sample duration is usually called a time slot. In one time slot, N speech samples are switched. An output-controlled switch is shown in Fig. 19.1. The outlet is cyclically scanned. There is a 1-to-M relationship between the outlets and the control memory locations. In other words, there are M locations in the control memory corresponding to each outlet.

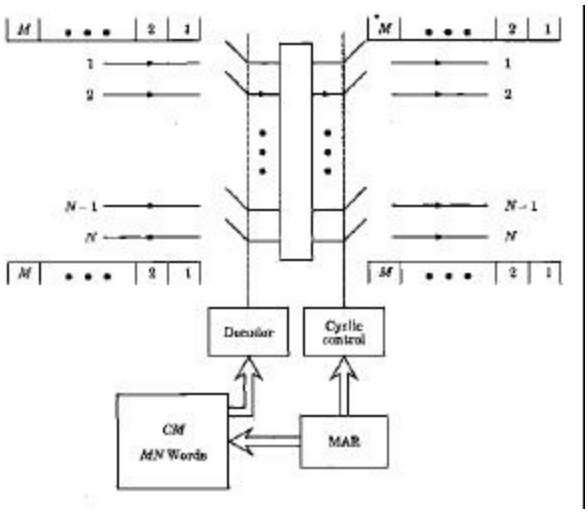


Fig. 19.1 Time multiplexed space switch.

The control memory has MN words. If we view the control memory as M blocks of N words each then a location address may be specified in two-dimensional form. It is given as L (i, j), where *i* is the block address and j is the word within the block.

We have

$$1 \leq j \leq M \text{ and}$$

$$1 \leq j \leq N$$

The block address i corresponds to the time slot i and the address j to the outlet j. The first N locations of the control correspond to the first time slot, the next N locations (i.e. N) when addressed in a two dimensional from N + 1 to 2N) when addressed linearly, or locations (2, 1) correspond to time slot 2 and so on. Therefore, if the location, L (i, j) contains inlet address K, it implies that K is connected to the outlet j the time slot i.The number of trunks that can be supported on this switch is given by

$$N = \frac{125}{M t_s} \qquad \text{……..Eq.1}$$

where t_s = Switching time including memory access time per inlet-outlet pair

The cost of the switch can be estimated as

C = No. of switches + No. of Memory words

$$= 2N + MN$$

$$= N(2 + M) \qquad \text{……..Eq.2}$$

The cost of an equivalent single-stage space division network

$$= (MN)^2$$

The number of trunks supported on this switch can be increased considerably by splitting the control memory into N independent modules of M words each and lettering each module service one input or output line. If the control memory modules are arranged such that each one services one input line and switches the input data to the appropriate output during every time slot, the switch is input-controlled.

If the control memory modules serve the output lines by switching the appropriate inputs, the switch is output-controlled. Fig. 19.2 shows an output-controlled configuration. It uses one control memory module for each output line. The control memory modules contain the addresses of inlets that should be switched to the respective outputs in each of the time slots.

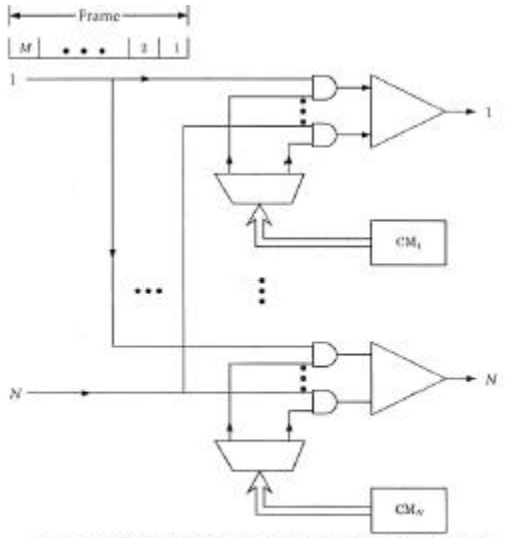


Fig. 3.38 Time multiplexed space switch with N control memory module.

.19.2

Time multiplexed space switch with N control memory module

Location of every module corresponds to timeslot 1; location 2 of every module corresponds to time slot 2, and so on. All locations corresponding to a particular time slot are read out in parallel. Consequently, there is no constraint due to time on the number of trunks that can be supported by the switch.

There is only one time constraint that needs to be satisfied is

$$M = \frac{125}{t_m} \quad \text{.....Eq.3}$$

where t_m = Control memory access time in ms.

In eqn.3, we have assumed that the time required for decoding addresses from the control memory and switching the gates are negligible 1 when compared to memory access time.

We now estimate the cost of the switch. The switch has N switching matrices of Size N x 1 each at the Inputs. There are NM memory j words. Therefore, the cost is given by,

$C = N (N \times 1) + NM$

$= N^2 + NM$ Eq.4

The cost of the switch is lower than that of the equivalent single stage space division switch but is more expensive than that of the one shown in Fig. 19.1. In this case, we observed that there is no cost increase on account of the memory words. The cost has gone up due to the number of space division matrices used for gating the inlets.

It can be noted here that output-controlled configurations permit broad-cast or one-to-many connections. Any particular input can be enabled during a given time slot by more than one control memory module. This control memory module leads to a one-to-many connection. Such a connection is not possible in an input-controlled switch. That is why, output-controlled configurations are preferred to the input- controlled configurations. Here, the width of the control memory is $\log_2 N$.

These switches (time multiplexed space switches) do not provide full availability. Each incoming trunk carries multiplexed samples from M different voice sources each stream on the outgoing trunk is de multiplexed to M different destinations. It is depicted in Fig. 19.3.

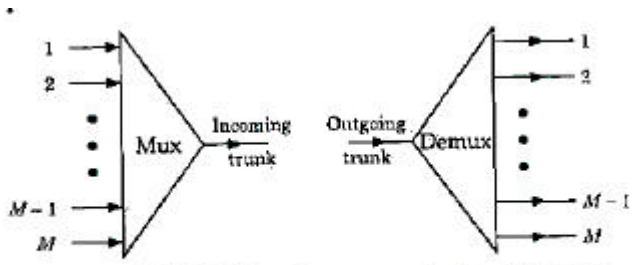


Fig. 3.39 Multiplexing of sources and demultiplexing of destination.

Fig.19.3 Multiplexing of sources and demultiplexing of destination.

Sources, trunks and destinations have one-to-one time relationship as follows:

1. Sources and incoming trunks time slots
2. Outgoing trunks time slots and the destinations
3. Time slot of incoming and outgoing trunks.

The sample of the source i is always carried in time slot i of the inlet similarly, the time slot j of the outlet is always de multiplexed to destination j. The time slot K of any incoming trunk is transferred to the time slot K of any outgoing trunk. It is not possible that transfer of a voice sample from time slot i of any inlet to time slot K of any outlet when i ¹ K. A voice sample from input time slot i can only be transferred to destination i of one or more outlets. In other words, interchange of samples among different time slots is not possible. So, we can conclude that this switch does not support full availability.

For every input, there are N (M -1) outputs that cannot be reached.

After development of large scale integration (LSI) in semiconductor technology, integrated circuit space arrays that are suitable for digital space switching are becoming available. A digital space array of size N x N is similar to a N x N crossbar switching matrix, except that bulky, expensive and power consuming electromagnets are replaced by digital gates.

A time-multiplexed time-division space switch can be configured around a space array. It is shown in Fig. 19.4.

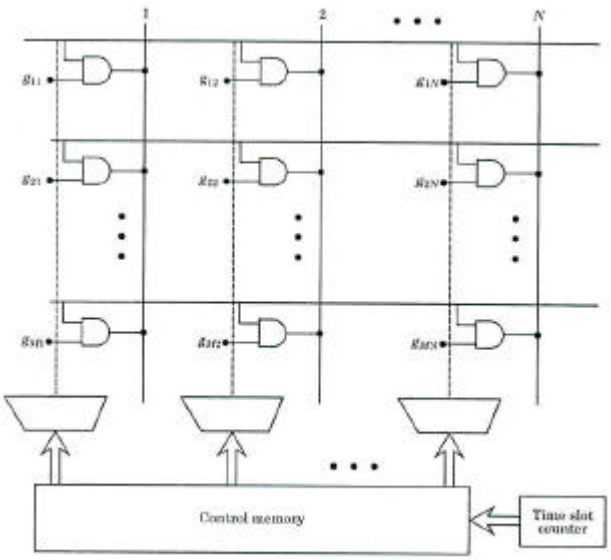


Fig. 3.40 Time-division space switch using space array.

Fig. 19.4 Time-division space switch using space array.

The space array consists of M input horizontals and N output verticals.

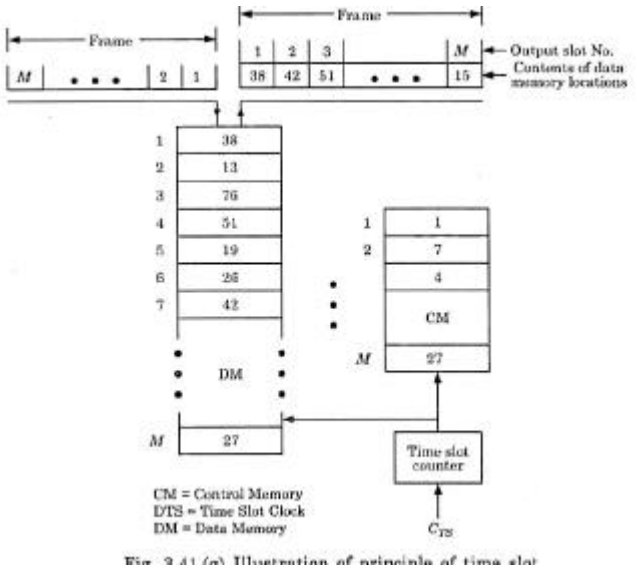
1. If M = N, the switch is non blocking
2. If M > N, the switch is concentrating
3. If M < N, the switch is expanding.

In every time slot, one logic gate per vertical if M < N, or one logic gate per horizontal if M < N is enabled for one-to-one connections.

We can observe that the space array is capable of establishing one-to-many and broadcast connections. In anytime slot, only one gate for vertical and up to N gates per horizontal can be enabled for these connections. An enabled logic gate panes the input digital sample to the corresponding output vertical.

In every time slot, up to Nor M samples are switched simultaneously. The control store has N addresses corresponding to N vertical outputs with each address selecting one gate in each vertical output.

The size of the control memory is N and its width [$\log_2$ M]. Because of the parallel transfer of N or M data samples in each time slot, a large number of channels can be multiplexed per input line. The performance of time multiplexed time switching is similar to that of Time multiplexing of Time multiplexed space switching with N control memory modules.



Time Multiplexed Time Switching (Tmts)

We know that time Multiplexed space switches cannot permit time slot interchange (TSI) of samples values. But Time multiplexed Time switches permit TSI of sample values. In TSI, a speech sample input during one time slot may be sent to the output during a different time slot. Such an operation necessarily imposes a delay between the reception and the transmission of a sample.

The principle of Time Slot Interchange (TSI) can be illustrated by considering a time switch which has one incoming trunk and one outgoing trunk. It is shown in Fig. 19.5 (a). Here M number of channels are multiplexed on each trunk. This switch is organised in the, Sequential Write/Random Read fashion.

(a) Illustration of principle of time slot interchange (TSI) switch

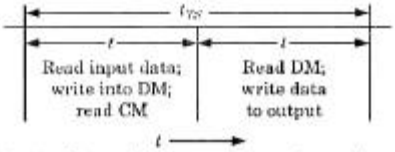


Fig. 3.41 (*b*) various operations in a time slot.

(c) Time relationship between inlet and outlet streams

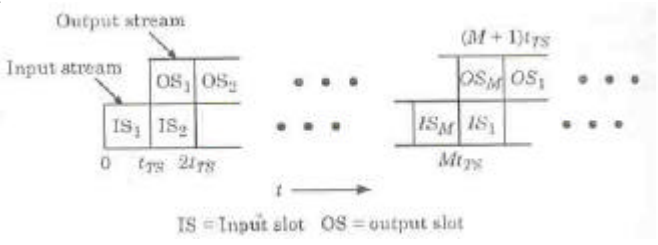


Fig.19.5 Illustration of time slot interchange (TSI) switch

Here, the time slot duration is given by

$$t_{TS} = \frac{125}{M} \quad \text{.....Eq.5}$$

The time slot clock runs at time slot rate. But the time slot rate is the one pulse every 125 / M microseconds. The time slot (TS) counter is incremented by one at the end of each time slot. The contents of TS counter provides location addresses for the data memory and control memory. Accessing of data memory and control memory takes place simultaneously in the beginning of the time slot. After then, the contents of the control memory are used as the address of the data memory and the data read out to the output trunk.

The various operations carried out in one ti me slot are shown in Fig. 19.5 (b). The input sample is available for reading in at the beginning of the time slot and the sample is ready to be clocked in on the output stream at the end of the time slot.

Even if there is no time slot interchange (TSI), a sample is delayed by a minimum of one time slot. This delay time is taken in passing the sample from the input stream to the output stream because of storage action. . In other words, a time slot switch may be considered to have an inherent time delay of one time slot.

The time relationship between inlet and outlet stream are shown in Fig. 19.5 (c). In other words, the output stream is delayed by one slot time, i.e., t_{TS} microseconds when compared to incoming data stream. Depending on the output time slot to which an input time slot contents are switched, the sample experiences a delay in the range of t_{TS} to M t_{TS} microseconds, The entries shown in control memory of Fig. 19.5 (a), the first location contains the value 1. This implies that the contents of the input time slot 1 are switched to output time slot 1. In this case, sample experiences a delay of t_{TS} microseconds. The second location of the control memory contains the value 7. Therefore, input time slot 7 is switched to output time slot 2. This sample experiences a delay of [(M -7) + 2 + 1] t_{TS} or (M – 4) t_{TS} microseconds.

Output time slot 3 carries the contents of input time slot 4. Therefore, the delay experienced by the sample is given by

[M - (4 - 3) + 1] t_{TS} or M t_{TS} i.e. 125 s. There are two sequential memory accesses per time slot. Hence the time constraint can be stated as

$$t_{TS} = 2\, t_m$$
$$125 = 2\, M\, t_m \quad \text{.....Eq.6}$$

Here t_m = Access time of the memory modules in .

When there is a two way traffic and the network is non folded then mother set of data and control memories is used. In the second control memory, the location 1, 7 and 4 contain the value 1, 2 and 3, respectively, corresponding to the sample entries shown in Fig. 19.5 (a).

When the cycle of time 125 s is complete, the values in the input time slots 1, 7, and 4 are interchanged with output time slots 1, 2, and 3, respectively.

When the switching network is folded, there is only one set of data and control memories even for two-way traffic. From Fig. 19.5 (a), we know that control memory locations of 7 and 4 contain the values 2 and 3, respectively when the cycle of time 125s is complete, the values in the time slots 7 and 2 and time slots 3 and 4 are interchanged.

For a folded network, transferring the data between the same input and output time slots is not relevant. For example, transfer of data from input time slot 1 to output time slot 1 is not relevant.

Since there are no switching elements in this configuration, the cost of the switch is equal to the number of memory locations. There are allocations each in the control and in the data memory.

Cost of the switch = Cost of the switching elements + Cost of memory locations ;

$$C = 0 + 2M, \text{ units}$$
$$\text{or } C = 2M \quad \text{.....Eq.7}$$

A Time Slot Interchange (TSI) switch may be designed to be expanding or concentrating. In these switches, number of time slots (samples) per frame in the input stream and in the output stream are different.

If we represent these numbers of time slots as M_1 and M_2, respectively, then the switch is expanding when $M_2 > M_1$. The bit rates of the input and the output streams are also different. For expanding switch, the output bit rate is higher than the input bit rate.

If $M_1 > M_2$, then this switch is termed as concentrating switch. In this stream input stream bit rate is higher than the output stream bit rate.

An expanding or concentrating time switch can be realized by delinking the read and write operations of the data memory. They are carried out independently and in a synchronous fashion. Asynchronous Read/Write operations for an expanding switch are illustrated in Fig. 19.6.

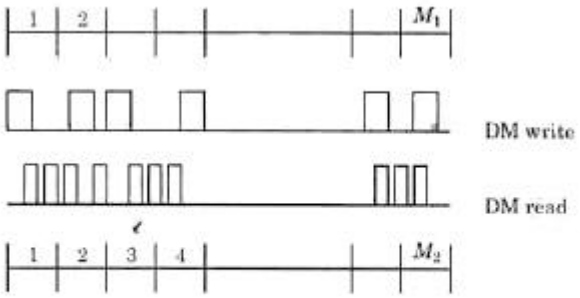


Fig. 3.42 Illustration of Read/Write operation for an expanding switch.

Fig. 19.6 Illustration of Read/Write operation for an expanding switch.

The time constraint for this switch can be stated as in an expanding TSI switch,

$$125 = (M_1 + M_2)\, t_m \quad \text{.....Eq.9}$$

Buffering may be required at the input and output of the data memory to ensure uniform data rates on the lines. The

expanding and concentrating time switches has application in combination switching. The control memory read is assumed to be overlapped with the data memory read. There are M_1 data memory write Operations and M_2 data memory read operations in every 125 s interval.

Up to now we have discussed the principle of operation of TSI switch. Now we consider practical configurations of Time multiplexed time switches. In these switches, there are N time multiplexed input streams each multiplexing M subscribers and, there are N time multiplexed output stream each carrying M subscribers.

The problem is to handle NM subscribers in the time duration of 125 s.

Such problem can be handled in four different ways:

1. Serial-In Serial-Out (SISO) Configuration
2. Parallel In Serial-Out (PISO) Configuration
3. Serial-In Parallel out (SlPO) Configuration
4. Parallel In Parallel Out (PIPO) Configuration.

Now we discuss each way of handling above problem one-by-one is subsequent subsections.

Serial-In Serial-Out (SISO) Configuration

Such type of configuration is abbreviated as SISO Configuration and shown in Fig.19.5 (a). The gating circuits are required to route data from the inlets to the data memory and from the data memory to outlets. They are equivalent to N * I and I * N switching matrices.

The capacities of the data and the control memories are NM words each. The width of the data memory word is 8 bits and the width of the control memory word is [log2 (MN)]. The time slot (TS) counter width is also the same as the width of the control memory word. The TS counter functions as a Module-MN counter. Here we can note the following:

The samples of the first time slot are stored in the first N consecutive locations of the data memory, the samples of the second time slots are stored in, the locations N + 1 to 2N, and so on.

Similarly, the input sample addresses corresponding to the first output time slots are stored in locations 1 to N of the control memory, the sample addresses corresponding to output time slot 2 are stored in locations N + 1 to 2N; and so on.

In each time slot, N data words are to be input and N data words are to be output. During the first time slot, the first slot samples from all the input streams are read one after another and stored in the data memory.

Within the same time duration (i.e. time slot period), the data words corresponding to the first time slot of all the N output streams are read out of the data memory and sent to the respective output streams. The same operations are repeated for everyone of the M time slots. The data memory write and control memory read operations are caused out simultaneously followed by data memory read operation.

The time constraints can be stated as

$$t_{TS} = 2N\, t_m$$

$$125 = 2N\, M\, t_m \qquad \text{.....Eq.10}$$

Parallel-In/Serial-Out (PISO) Configuration

In this configuration, the data memory is organised as N modules of M words each. It is shown in Fig. 19.7 (a). Each module is associated with one input line. The time slot duration (t_{TS}) is divided into N +1 sub slots to, t_1, t_2, ...t_N. During the sub slot to data from all the input lines are read into the respective data memory modules simultaneously.

A two dimensional adding structure that comprises of module address and word address, is used to access the data memory words. The word address compounds to the time slot number and the module address to the inlet number. The word address,

Word 1 corresponds to time slot 1,

Word 2 corresponds to time slot 2,

Word 3 corresponds to time slot 3, and so on.

A special control signal is used to enable all the data memory modules for write access during the sub slot 't_0' .

During the subslots 't_1' to 't_N', the control memory locations are accessed one after the another, the contents of the location are used to address the data memory for read access. Therefore, data words read out are transferred to the corresponding output lines.

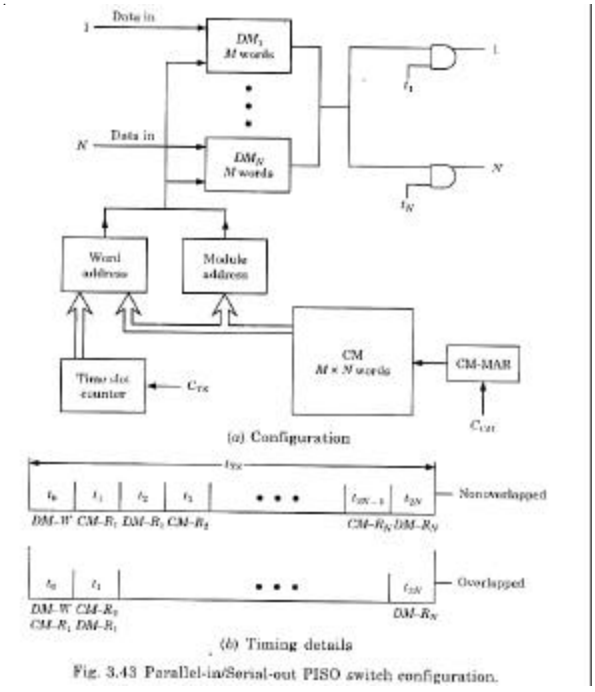


Fig. 3.43 Parallel-in/Serial-out PISO switch configuration.

Fi.19.7 Parallel-in / Serial-out PISO switch configuration.

During the subslots 't_1' of the time slot I, a data word read from the data memory is transferred to the outgoing trunk 1, for insertion in the time slot i of this stream. Similar transfers also take place during subslots 't_2' to 't_N' to outgoing trunks 2 to N.

The control memory locations contain the two-part address of the data memory. The first part of the address bits which are used to select the module.

The second part of the address has lower-order address bits which are used to represent word within a module. The width of the control memory word is élog$_2$ Nù + élog$_2$ Mù. The control memory 1m clock, C_m runs at the rate of one pulse per (t_{TS} / N+1) microseconds except that one pulse is inhibited during the sub slot 'to'.

The control memory read may be overlapped with data memory. It is indicated in Fig. 19.7 (b). In this case, C_m is inhibited during subslot 't_N'.

The time constraints can now be stated as:

1. For non overlapped operation:

$$t_{TS} = (2N + 1)\ tm$$

$$125 = M\ (2N + 1)\ tm$$

……...Eq.11

2. For overlapped operation:

$$t_{TS} = (N + 1)\ tm$$

$$125 = M\ (N + 1)\ tm \qquad \text{……Eq.12}$$

From above eqns.11 and 12, it can be observed that the maximum delay between the acquisition and transmission of a sample I varies between 'to' and (125 -t_N) microseconds. The PISO switch functions like an output -controlled switch, because each storage location of the control memory is rigidly associated with a given output time slot and a specific outlet.

Serial-in/Parallel-out (SIPO) Configuration

This switch is the dual of the parallel in/Serial-out (PISO) switch. Here, the data memory modules are associated with the output lines instead of input lines. The data input is serial and is carried out during the sub slots 't_1' to 't_N'. The sub slot 't_0' is used for parallel read-out from all the data memory modules to the corresponding output lines. With this arrangement, it appears as though the output precedes input. Since the entire operation is cyclic, it is immaterial whether the output operation is carried out in sub slot 'to' or 'tN'. The SIPO configuration is called input-controlled due to some reasons. Here we can note that it is easier to organise broadcast connections in a PISO switch rather than. SlPO switches.

Parallel-In/Paralle1-0ut (PI PO) Switch

It is the most complex of all the time multiplexed time switch configurations such as SISO, PISO and SIPO. It is also the configuration that can support the largest number of subscribers for a given technology option. Both the data memory and the control memory are organised as N independent modules of M words each, such type of configuration is shown in Fig. 19.8 (a). There is one-to-one correspondence between the data memory and control memory modules. Address outputs from the control memory module i are always used to access words in the data memory module i. The correspondence is limited to the module level. We cannot extend correspondence to word level.

Each location of the control memory module contains information about both input side and output side. It is illustrated in Fig. 19.8 (b).

The input side contains an inlet address part and a word address part.

The output side contains an outlet address and a word address part. Inlet/Outlet address selects one of the N inlet/outlet streams. Word address is used to access one of the M words in the data memory module corresponding to the control memory module from which the word address is read. There is one-to-one correspondence between the control memory words and time slots. The word i in each module contains information pertaining to time slot i. There is no such correspondence with data memory words.

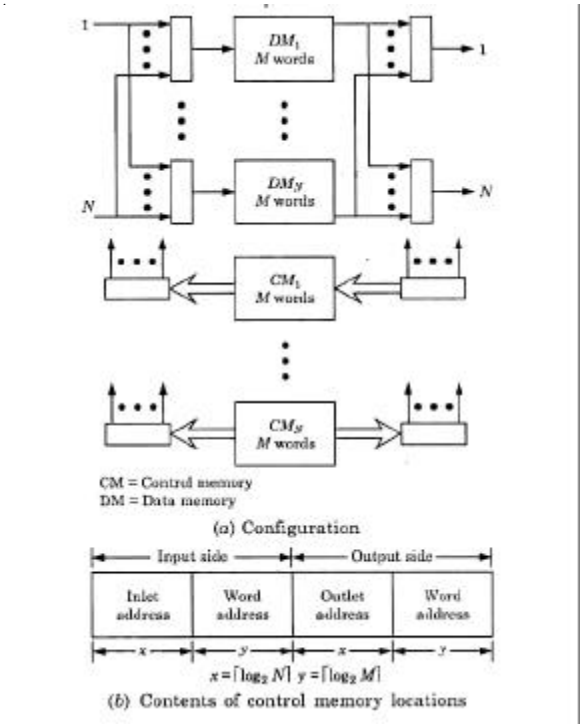


Fig.19.8 Illustration of contents of control memory locations

In each slot, the operation of the switch takes place in three phases:

1. Control Memory Read
2. Data Memory Write
3. Data Memory Read.

Now we consider the operation of the switch corresponding to time slot:

1. In the first phase, the first location of all the control memory modules are read. The inlet addresses are decoded. Therefore, the respective inlets are gated to the MDR other data memory modules. The word addresses of the input side are transferred to the respective MARs of the data memory modules.

2. In the second phase operations, a write operation is performed in all the data memory modules simultaneously. The data contained in the MDRs are transferred to the respective locations.
3. In the third phase of operation, the word addresses of the output side are transferred to respective MARs. A read operation is performed in all the data memory modules. The MDRs now contain the data to be transferred to the required outlets. The outlet addresses from the control memory word are decoded to select the respective outlets and the data from the MDRs transferred.

The time constraint may be expressed as

$t_{TS} = 3\ t_m$ ……....Eq.13

It can be noted here that this equation is independent of N and thus permitting any number of trunks to be supported theoretically. In practice, however, engineering considerations would limit the number of trunks.

It is possible to organise the control memory in two sets of modules. One set of module for the input side and other for the output side.

The output side set may be read out during second phase of operation of the data memory modules.

Example 19.1: Determine the number of trunks that can be supported on a time multiplexed space switch.

We have been given the following for this switch:

1. 32 channels are multiplexed in each stream
2. Control memory access time = 10 ms
3. Bus switching and transfer time is 100 ms per transfer.

Solution:

The number of trunks that can be supported on a time multiplexed space switch is determined by,

$N = 125 / (M * t_s)$ ……..Eq.1

But t_s = Switching time including memory access time per inlet-outlet pair

$= 100 + 100 = 200$ ms

Given M = Number of channels that are multiplexed in each stream

$= 32$

Substituting $t_s = 200$ ms and M = 32 in eq.1, we get

$N = 125 / (M * t_s)$

$= 125 / (32 * 200 * 10^{-3})$

$= 20$

Example 19.2: Find the maximum access time that can be permitted for the data and control memories in a TSI switch with a single input and single output trunk multiplexing 2500 channels. Also determine the cost of the switch and compare it with that of a single stage space division switch.

Solution:

Time slot duration is determined as,

$t_{TS} = 125 / M$

$= 125 / 2500$ …….eq.1

Also, we know that

$t_{TS} = 2\ t_m$

or $t_m = t_{TS} / 2$ ……eq.2

Substituting the value of t_{TS} from eq.1 in eq.2, we get

$t_m = 125 / (2 * 2500)$

$= 25$ ms

Cost of the switch, $C = 2\ M$

$= 2 * 2500$

$= 5000$

This switch is nonblocking and supports full availability.

An equivalent single-stage space division switch uses a matrix of N * N = 2500 * 2500. Hence, the cost of such switch is $6.25 * 10^6$ units.

Cost of single-stage space division switch

Cost advantage of the time switch =Cost of time-division switch

$$\text{Cost advantage of the time switch} = \frac{6.25 * 10^6}{5000}$$

$$= 1250$$

Maximum access time is 25ms & cost advantage of the time switch is 1250 units.

Example 19.3: Find the access time of the memory module in PISO time switch using 64 input and 64 output streams with each stream multiplexing 32 channels.

Solution:

Here, we assuming over-lapped operation, we have

$125 = M (N + 1)\ t_m$

$$\text{or} \quad t_m = \frac{125}{M (N + 1)} = \frac{125}{32 (64}$$

1. $t_m = 0.06$ microsec.

Number of trunks are 20

Maximum access time is 25ms & cost advantage of the time switch is 1250 units.