



Professional Radio GP Series

**Power Distribution and Controller
Service Information**

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THEORY OF OPERATION

This Chapter provides a detailed theory of operation for the power distribution and controller circuits in the radio. The components for these circuits are contained on the Main Board. Refer to the RF sections of this manual for the component location details and the parts lists for these circuits.

[illegible]

Figure 1-1 illustrates the DC distribution throughout the radio board. A 7.5V battery (BATT 7.5V) supplies power directly to the electronic on/off control as UNSWB+. When the radio is turned on, MECH_SWB+ (on/off/volume control) will trigger the electronic on/off control (momentary-on path), then SWB+ is distributed as shown in Figure1-1. Vdda from 3.3V Vdda regulator will then supply the microprocessor. Data is then sent to ASFIC_CMP to turn on GCB4(DAC). GCB4 will take over the momentary-on path within 12ms. SWB+ will continue to support the whole board until the radio is turned off.

1. MECH_SWB+ turned off
2. Low battery

When low battery level is detected by the microprocessor through both conditions above, it will store the radio personality data to EEPROM before turning off.

3.0 Controller Circuits

3.1 Controller Architecture

The controller board is the central interface between the various subsystems of the radio. It is separated into MCU digital and audio/signalling architectures as shown in Figure 1-2.

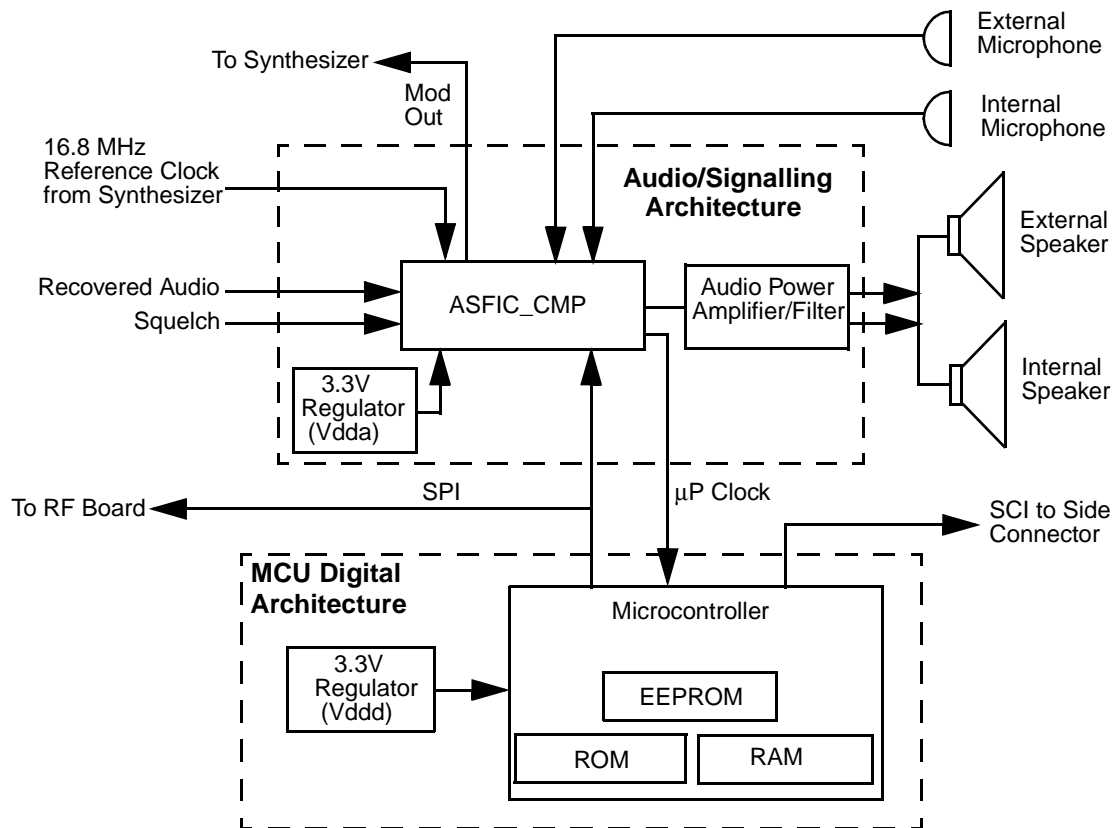


Figure 1-2 Controller Block Diagram

3.2 MCU Digital Architecture

(Refer to Figure 1-2, the Microprocessor and the Memory schematic diagrams)

The digital architecture portion consists of a microcontroller and associated EEPROM, RAM, and ROM memories. The architecture is commonly used for both low-tier and high-tier products and also includes conventional and trunking portables. Combinations of different size RAM and ROM are available to support various application software. RAM supports 8KB and 32KB sizes. ROM supports 128KB, 256KB, and 512KB sizes. Table 1-1 shows the ROM, RAM and EEPROM requirements for different applications.

Table 1-1 Radio Memory Requirements

RADIO		ROM (KB)	EXT RAM (KB)	EEPROM (KB)
Conventional MDC	GP140	128K	-	8K
Conventional 5 Tone	GP320	512K	16K	16K
	GP340	512K	16K	16K
Conventional 5 Tone	GP360	512K	16K	16K
	GP380	512K	16K	16K
MPT	GP640	512K	16K	16K
	GP680	512K	16K	16K
MPT	GP1280	512K	16K	16K

3.3 Real Time Clock

(Refer to Figure 1-3 and the Microprocessor schematic diagram)

Radios with displays support a Real Time Clock (RTC) module for purposes of message time stamping and time keeping. The RTC module resides in the microcontroller. The clock uses a back-up Lithium Ion battery for operating power when the primary battery is removed.

3.3.1 Circuit Description

The RTC module circuit, shown in Figure 1-3, is powered by the ModB/Vstby pin and PI6/PI7 from the crystal oscillator circuit. A clock frequency of 38.4kHz from a crystal oscillator provides the reference signal which is divided down to 1 Hz in the processor.

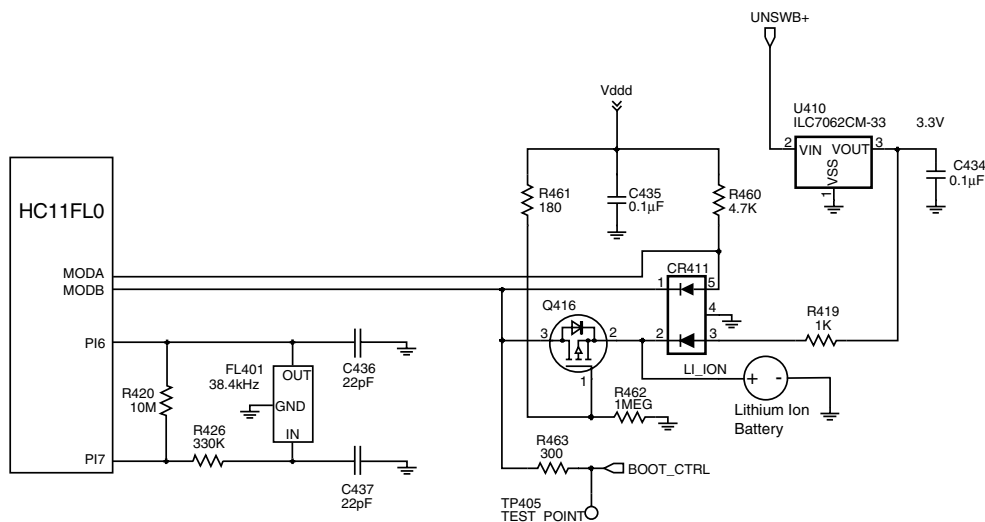


Figure 1-3 RTC Circuit

As the RTC module is powered separately from the processor Vdd, the RTC is kept active through the ModB / Vstby pin which provides the Lithium battery back-up power when the radio is switched off.

A MOSFET Q416 switches in the LiO supply when Vdd is removed. Q416 also provides isolation from BOOT_CTRL function in the event of radio program flashing. The 3.3V regulator charges the Lithium battery.

3.4 ModB/Vstby Supply

The supply to the ModB/Vstby pin varies depending on the conditions listed in Table 1-2.

Table 1-2 ModB/Vstby Supply Modes

Condition	Circuit Operation
Radio On	Vdd supply voltage via CR411
Radio Off	<ul style="list-style-type: none"> • Vdd turned off • Q416 gate pulled low by R462 • Q416 switched on • U410 supplies 3.2V to ModB/Vstby
Primary battery removed	<ul style="list-style-type: none"> • Vdd turned off • Q416 gate pulled low by R462 • Q416 switched on • Lithium battery provides 3.2V to ModB/Vstby
Flash Mode	<ul style="list-style-type: none"> • Boot_Ctrl line pulled low • ModA & ModB go low • Processor in boot-strap mode

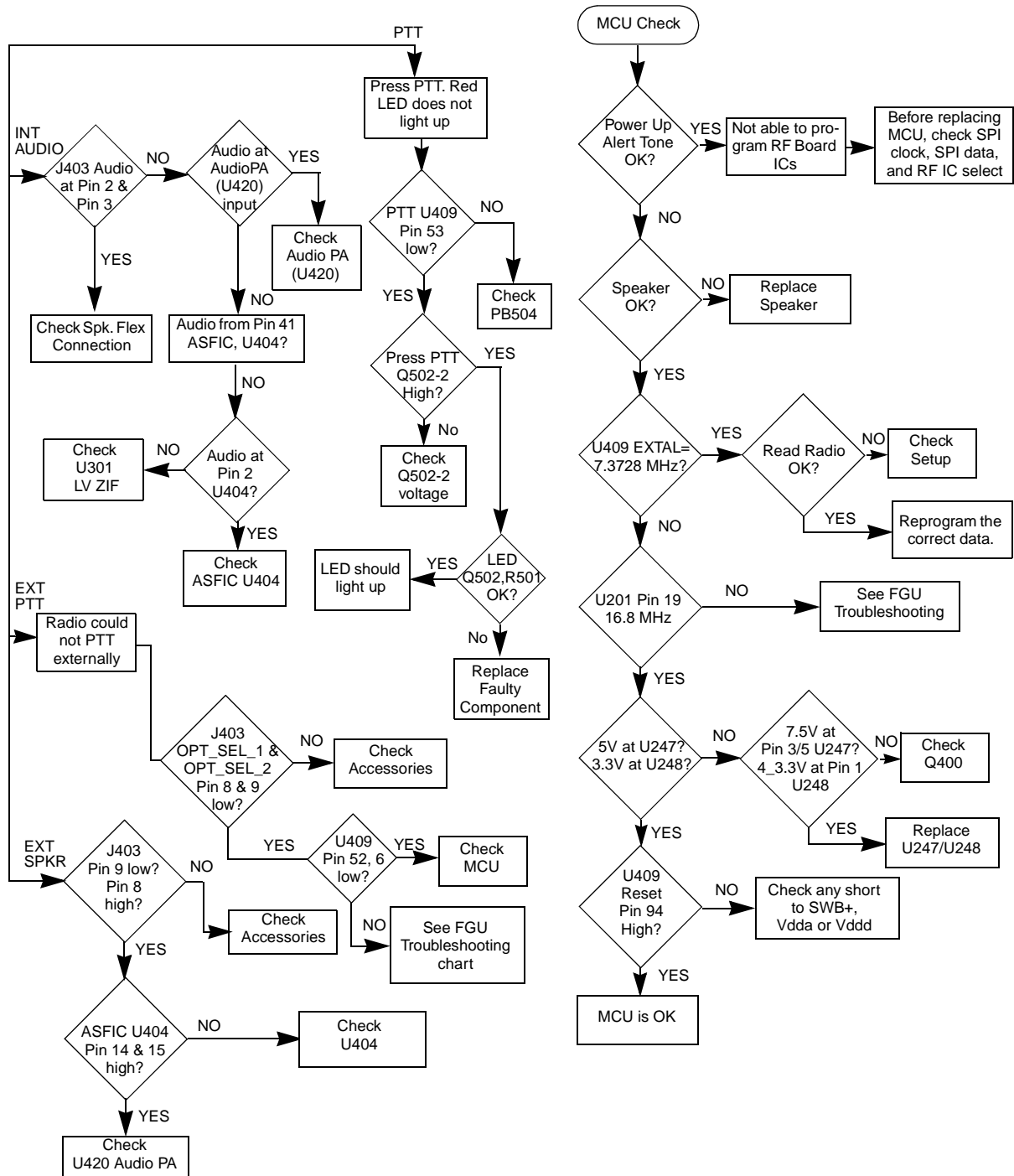
3.5 Audio/Signaling Architecture

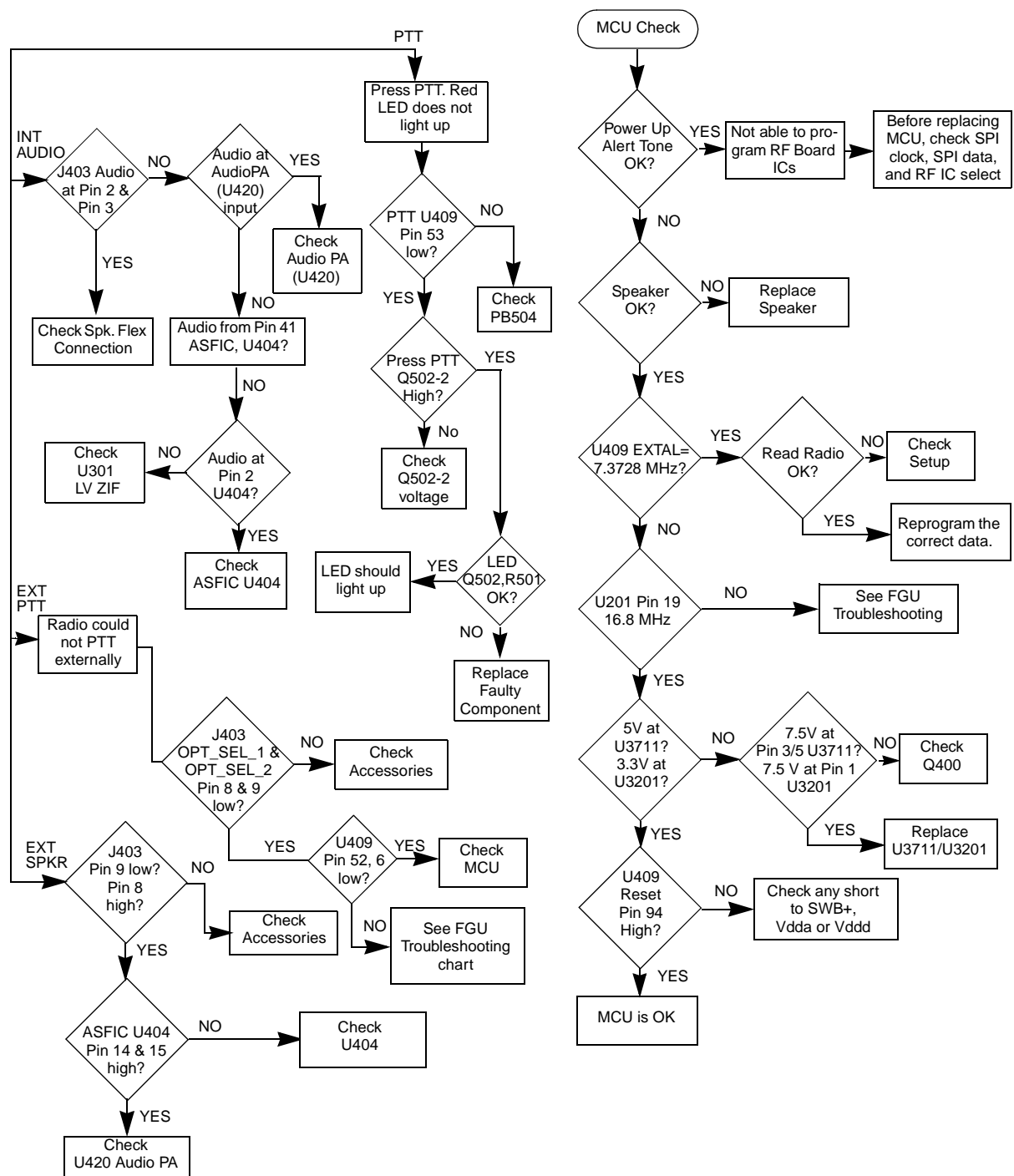
(Refer to Figure 1-2 and the ASFIC/ON_OFF and Audio Power Amplifier schematic diagrams)

The audio/signalling/filter/companing IC (ASFIC_CMP) and the audio power amplifier, shown in Figure 1-2, form the main components of the audio/signalling architecture section of the controller board. Inputs include a 16.8 MHz clock from the synthesizer, recovered audio and squelch, MCU control signals, and external or internal microphones. Outputs include a microprocessor clock (uP), modulator output to the synthesizer, and amplified audio signals to an internal or external speaker.

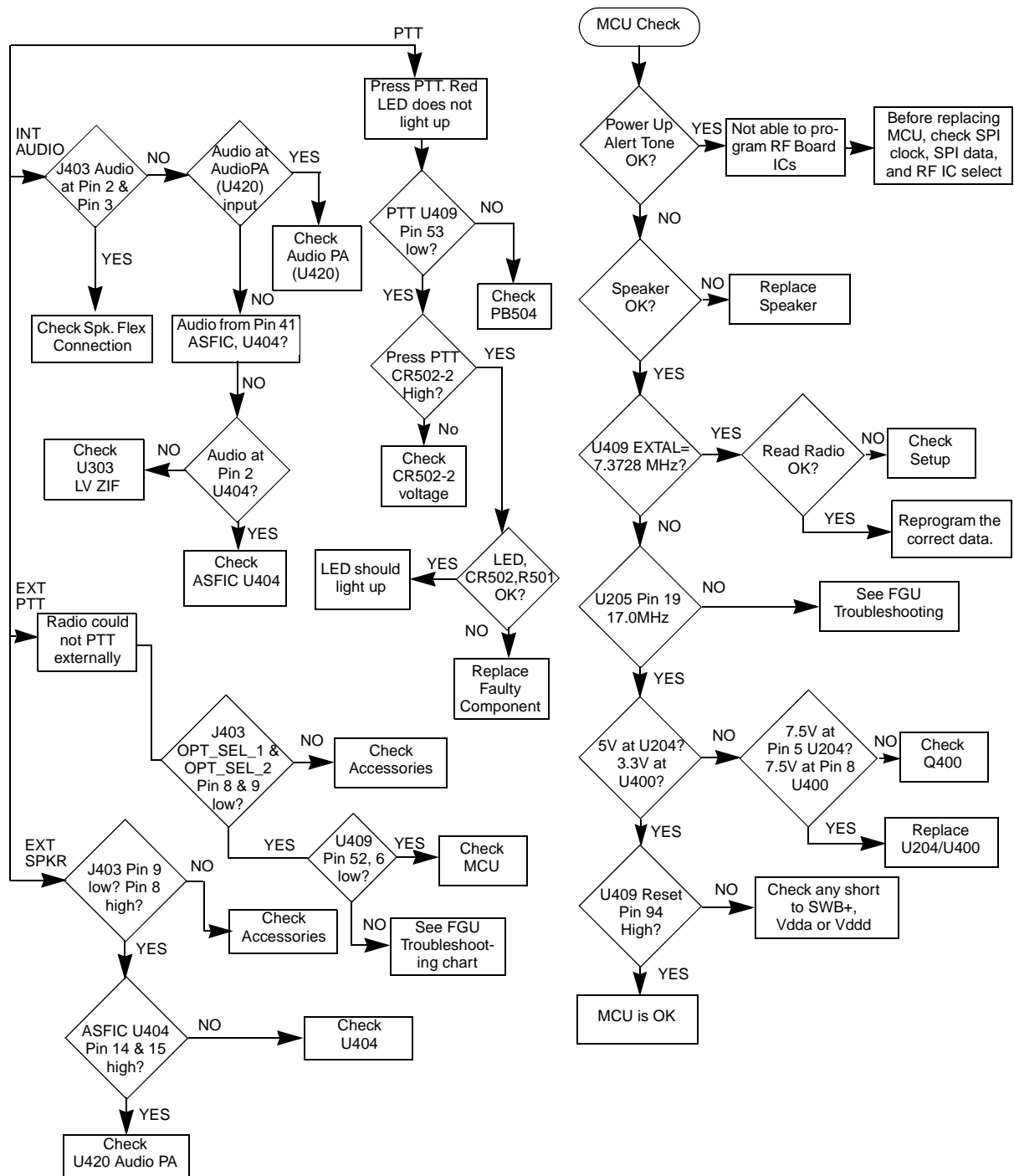
TROUBLESHOOTING CHARTS

1.0 UHF/ UHF2/ 300R1 Controller





3.0 Lowband Controller



CONTROLLER SCHEMATICS

1.0 Allocation of Schematics and Circuit Boards

The Controller circuits are contained on the printed circuit board (PCB) containing the RF circuits. This Chapter shows the schematics for the Controller circuits only, refer to the relevant RF section for details of the related RF circuits, the PCB component layouts and the Parts Lists. The Controller schematic diagrams and the related PCB and parts list are shown in the tables below:

Table 3-1 Schematics - Set 1

PCBs : 8480450Z03 8485641Z02 8480587Z01 8485677Z01 8486062B12/ B14 8485726Z01	UHF UHF2 UHF GP1280 UHF2 GP1280 VHF 300R1
SCHEMATICS Overall Controller Schematic ASFIC/ ON_OFF Microprocessor Interface Memory Audio Power Amplifier	Page 3-3 Page 3-4 Page 3-5 Page 3-6 Page 3-6 Page 3-7

Table 3-2 Schematics - Set 2

PCBs : 8486101B09/ B10	VHF GP1280
SCHEMATICS Overall Controller Schematic ASFIC ON_OFF Memory Microprocessor Interface Audio Power Amplifier	Page 3-9 Page 3-10 Page 3-10 Page 3-11 Page 3-12 Page 3-13

Table 3-3 Schematics - Set 3

PCBs : 8485658Z01	Lowband
SCHEMATICS Overall Controller Schematic ASFIC ON_OFF Microprocessor Interface Memory Audio Power Amplifier	Page 3-15 Page 3-16 Page 3-17 Page 3-18 Page 3-18 Page 3-19

Table 3-4 Schematics - Set 4

PCBs : 8486062B16	VHF
SCHEMATICS Overall Controller Schematic ASFIC ON_OFF Microprocessor Memory Interface Audio Power Amplifier	Page 3-21 Page 3-22 Page 3-23 Page 3-24 Page 3-24 Page 3-25

Table 3-5 Schematics - Set 5

PCBs : 8480450Z13	UHF
SCHEMATICS Overall Controller Schematic ASFIC ON_OFF Microprocessor Memory Interface Audio Power Amplifier	Page 3-27 Page 3-28 Page 3-29 Page 3-30 Page 3-30 Page 3-31