MOTOROLA

Professional Radio
GP Series

UHF2 (450 - 527MHz)

Service Information

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Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 GP640/GP680 Model Chart

Professional GP600 Series (UHF2)				
Model				Description
MDH25SDC9CK3_E				GP640 UHF2 450-527 MHz 4W
	MDH25SDH9CK6_E			GP680 UHF2 450-527 MHz 4W
			Item	Description
X			PMLE4122_	GP640 UHF2 Back Cover Kit
	X		PMLE4123_	GP680 UHF2 Back Cover Kit
X			6864110B14	GP640 Basic User Guide
	X		6864110B19	GP680 Basic User Guide
X	X		PMAE4008_	UHF 14cm (465-527 MHz) Antenna
X	X		HNN9008_	Battery, NiMH Standard

x = Indicates one of each is required.

2.0 GP1280 Model Chart

Professional GP1280 (UHF2)			
Model			Description
MDH25SDN9CK8_E			GP1280 UHF 450-527 MHz 4W
		Item	Description
X		PMLE4142_	GP1280 UHF2 Back Cover Kit
X		6864110B20	GP1280 Basic User Guide
X		PMAE4008_	UHF 14cm (465-527MHz) Antenna
X		HNN9008_	Battery, NiMH Standard

x = Indicates one of each is required.

3.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General Specifications		
Channel Capacity		
GP640	16 (Conventional)	
GP680	16 (Conventional)	
GP1280	16 (Conventional)	
Power Supply	Rechargeable battery 7.5v	
Dimensions: H x W x D (mm) Height excluding knobs	**GP640/680**	
With standard high capacity NiMH battery	137 x 57.5 x 37.5	
With ultra high capacity NiMH battery	137 x 57.5 x 40.0	
With NiCD battery	137 x 57.5 x 40.0	
With Lilon battery	137 x 57.5 x 33.0	
	GP1280	
With standard high capacity NiMH battery	152 x 57.5 x 37.5	
With ultra high capacity NiMH battery	152 x 57.5 x 37.5	
With NiCD battery	152 x 57.5 x 37.5	
With Lilon battery	152 x 57.5 x 37.5	
Weight: (gm)	**GP640**	**GP680**
With Standard high capacity NiMH battery	420	428
With Ultra high capacity NiMH battery	500	508
With NiCD battery	450	458
With Lilon battery	350	358
	GP1280	
With Standard high capacity NiMH battery	460	
With Ultra high capacity NiMH battery	535	
With NiCD battery	485	
With Lilon battery	390	
Average Battery Life @5/5/90 Cycle:	Low Power	High Power
With Standard high capacity NiMH battery	11 hours	8 hours
With Ultra high capacity NiMH battery	14 hours	11 hours
With NiCD battery	12 hours	9 hours
With Lilon battery	11 hours	8 hours
Sealing:	Withstands rain testing per MIL STD 810 C/D /E and IP54	
Shock and Vibration:	Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603	
Dust and Humidity:	Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603	

Transmitter	UHF2
*Frequencies - Full Bandsplit	450-527 MHz
Channel Spacing	12.5/20/25 kHz
Frequency Stability (-25°C to +55°C, +25° Ref.)	±2.5 ppm @ 12.5kHz ±5ppm @ 25 kHz
Power	450 - 527 MHz: 1-4W
Modulation Limiting	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz
FM Hum & Noise	-40 dB typical
Conducted/Radiated Emission	-36 dBm <1 GHz -30 dBm >1 GHz
Adjacent Channel Power	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB
Audio Distortion	<3% typical

Receiver	UHF2
*Frequencies - Full Bandsplit	450-527 MHz
Channel Spacing	12.5/20/25 kHz
Sensitivity (12 dB SINAD) EIA Sensitivity (20 dB SINAD) ETS	0.25 μV typical 0.50 μV typical
Intermodulation EIA	65 dB
Adjacent Channel Selectivity	60 dB @ 12.5 kHz 70 dB @ 25 kHz
Spurious Rejection	>70 dB
Rated Audio	0.5W
Audio Distortion @ Rated Audio	<3% typical
Hum & Noise	-45 dB @ 12.5 kHz -50 dB @ 20/25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB
Conducted Spurious Emission	-57 dBm <1 GHz -47 dBm >1 GHz ETS 300 086

*Availability subject to the laws and regulations of individual countries.

Chapter 2

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the UHF2 circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

2.0 UHF2 Transmitter

(Refer to Figure 2-1 and the UHF Transmitter schematic diagram)

The UHF2 transmitter consists of the following basic circuits:

1. Power amplifier (PA).
2. Antenna switch/harmonic filter.
3. Antenna matching network.
4. Power Control Integrated Circuit (PCIC).

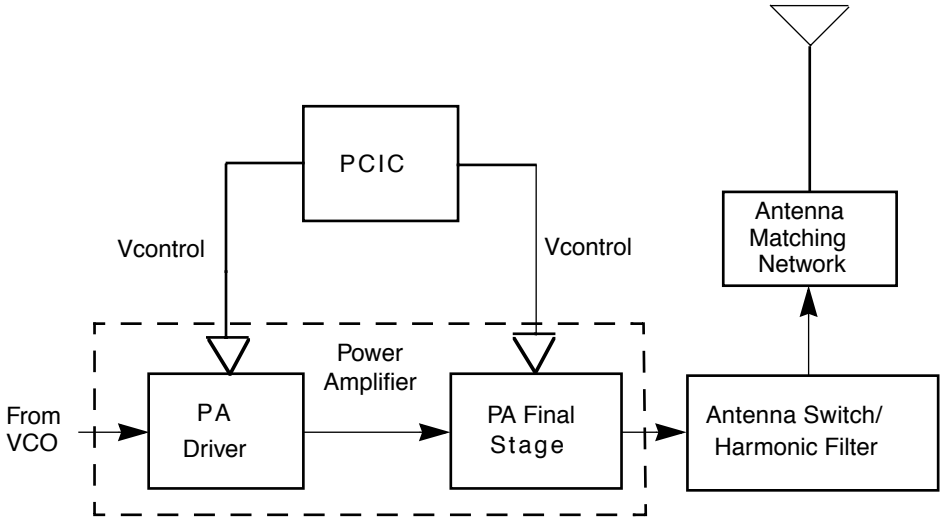


Figure 2-1 UHF2 Transmitter Block Diagram.

2.1 Power Amplifier

The power amplifier (PA) consists of two principle devices:

1. LDMOS PA driver IC, U101.
2. LDMOS PA final stage, Q110.

The LDMOS driver IC provides 2-stage amplification using a supply voltage of 7.3V. The amplifier is capable of supplying an output power of 0.3W (pins 6 and 7) with an input signal of 2mW at 3dBm (pin16). The current drain is typically 160mA while operating in the frequency range of 450-527MHz.

The LDMOS PA is capable of supplying an output power of 7W with an input signal of 0.3W. The current drain is typically 1300mA while operating in the frequency range of 450-527 MHz. The power output can be varied by changing the bias voltage.

2.2 Antenna Switch

The antenna switch circuit consists of two pin diodes (CR101 and CR102), a pi network (C107, L104 and C106), and two current limiting resistors (R101 and R170). In the transmit mode, B+ at PCIC (U102) pin 23 goes low turning on Q111 which applies a B+ bias to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port and the pi network. This operates as a quarter wave transmission line to transform the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, creating a low attenuation path between the antenna and receiver ports.

2.3 Harmonic Filter

The harmonic filter consists of components C104, L102, C103, L101 and C102. The harmonic filter for UHF is a modified Zolotarev design optimized for efficiency of the power module. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2dB.

2.4 Antenna Matching Network

The antenna matching network is made up of inductor L116. This component matches the antenna impedance to the harmonic filter to optimize the performance of the transmitter and receiver.

2.5 Power Control Integrated Circuit (PCIC)

The transmitter uses PCIC, U102, to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101 to provide a voltage proportional to the current drain. This voltage is then fedback to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC contains internal digital to analog converters (DACs) that provide a programmable control loop reference voltage through the SPI line of the PCIC.

The PCIC internal resistors, integrators, and external capacitors (C133, C134 and C135) control the transmitter rise and fall times to reduce the power splatter into adjacent channels.

Diode CR105 and its associated components are part of a temperature cut back circuit. This circuit senses the printed circuit board temperature around the transmitter circuits and outputs a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold of the PCIC, the transmitter output power decreases to reduce the transmitter temperature.

3.0 UHF2 Receiver

The UHF2 receiver consists of a front end, back end, and automatic gain control circuits. A block diagram of the receiver is shown in Figure 2-2. Detailed descriptions of these features are contained in the paragraphs that follow.

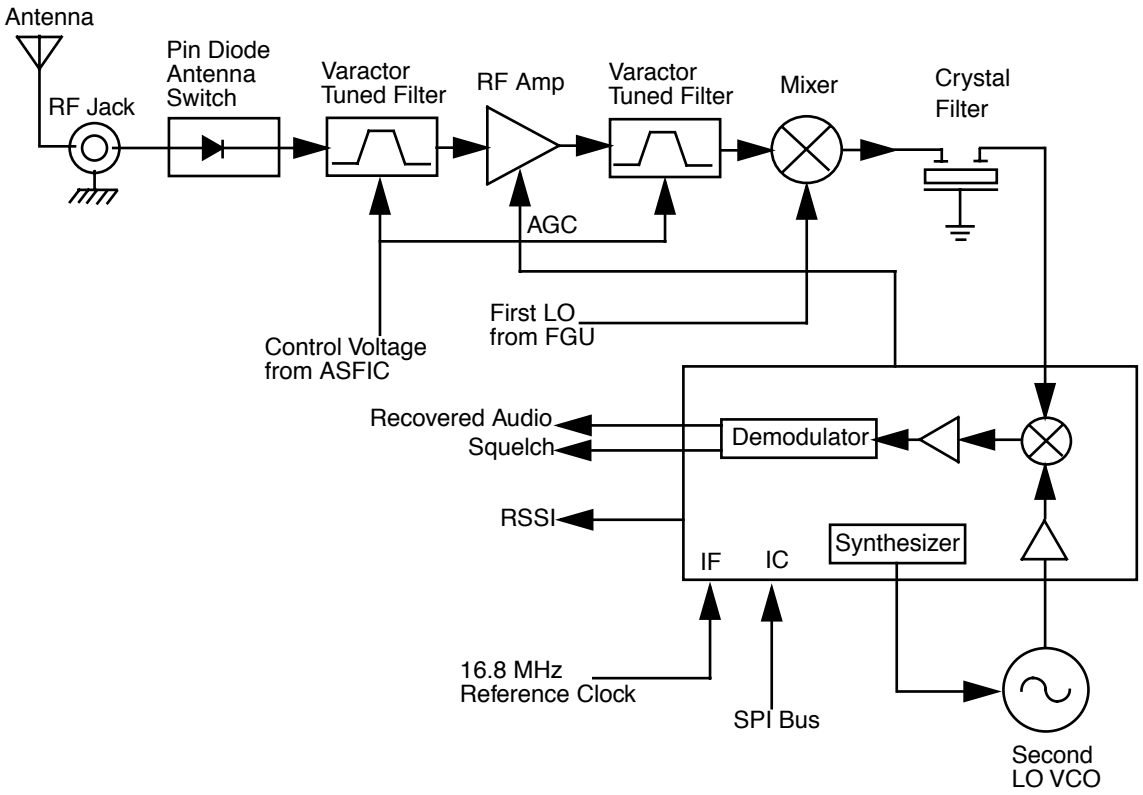


Figure 2-2 UHF2 Receiver Block Diagram.

3.1 Receiver Front-End

(Refer to Figure 2-2 and the UHF2 Receiver Front End schematic diagram)

The RF signal received by the antenna is applied to a low-pass filter. For UHF, the filter consists of components L101, L102, C102, C103, and C104. The filtered RF signal is passed through the antenna switch circuit consisting of two pin diodes (CR101 and CR102) and a pi network (C106, L104, and C107). The signal is then applied to a varactor tuned bandpass filter.

The UHF bandpass filter consists of components L301, L302, C302, C303, C304, CR301, and CR302. The filter is electronically tuned by DACRx from IC 404 which supplies a control voltage to the varactor diodes (CR301 and CR302) in the filter as determined by the microprocessor depending on the carrier frequency. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q301 via C307. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L306, L307, C313, C317, CR304 and CR305.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3 dB bandwidth of the filter is approximately 50 MHz. This enables the filters to be electronically controlled by using a single control voltage from DACRx.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer consisting of components T301, T302, and CR306. Matching of the filter to the mixer is provided by C381. After mixing with the first local oscillator (LO) signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to a 45.1 MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL301) through a resistor pad and a diplexer (C322 and L310). Matching to the input of the crystal filter is provided by C324 and L311. The crystal filter provides the necessary selectivity and intermodulation protection.

3.2 Receiver Back-End

(Refer to Figure 2-2 and the UHF2 Receiver Back End schematic diagram)

The output of crystal filter FL301 is matched to the input of IF amplifier transistor Q302 by components L322 and C325. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifier provides a gain of about 7dB. The amplified IF signal is then coupled into U301(pin 3) via C330, C338 and L330 which provides matching for the IF amplifier and U301.

The IF signal applied to pin 3 of U301 is amplified, down-converted, filtered, and demodulated, to produce recovered audio at pin 27 of U301. This IF IC is electronically programmable, and the amount of filtering, which is dependent on the radio channel spacing, is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in IF module U301.

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U301 so that it is very close to the first IF frequency. The IF IC (U301) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO searches for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO locks onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q320. The VCO has a varactor diode, CR310, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of components C362, C363, C364, R320 and R321.

The IF IC (U301) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the front-end.

The demodulated signal on pin 27 of U301 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

3.3 Automatic Gain Control (AGC)

(Refer to the UHF2 Receiver Front End and Receiver Back End schematic diagrams)

The front end automatic gain control circuit provides automatic reduction of gain, of the front end RF amplifier via feedback. This action is necessary to prevent overloading of backend circuits. This is achieved by drawing some of the output power from the RF amplifier output. At high radio frequencies, capacitor C331 provides a low impedance path to ground for this purpose. CR308 is a pin diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the pin diode on. Transistors Q315 and Q311 provide for this current. When Q315 is turned on, current flows via R323, collector and emitter of Q315, and R319 before going to ground. Q315 is an NPN transistor used for switching.

The Radio Signal Strength Indicator (RSS I) voltage signal is used to drive Q315 to saturation, i.e., turned on. RSSI is produced by U301 and is proportional to the gain of the RF amplifier and the input power to the radio.

Resistors R318 and R316 are voltage dividers designed to turn on Q315 at certain RSSI levels. To turn on Q315, the voltage across R318 must be greater or equal to the voltage across R319 + Vbe. Capacitor C397 dampens any instability while the AGC is turning on.

Diode D300 is to ensure that C397 only discharges towards the transistor and not back to U301. The current flowing into the base of Q311, a high current gain PNP transistor, is amplified and fed to the pin diode to turn it on. Maximum current flowing through the pin is limited by resistors R347 and R317. Feedback capacitor C333 provides some stability to this high gain stage. Q316, R325, R326, R327, R338, R339 and R341 make up the temperature compensation circuit for this AGC. RSSI generated by U301 is lower at cold compared to normal operation at room temperature. Q316 is designed to turn on only at cold temperature. When Q316 is turned on, current flows through the collector-emitter junction to ground. Current through R319 and hence voltage across it is reduced. The turn on voltage is lower and this accommodates for the reduction of the RSSI at cold temperature.

4.0 Frequency Generation Circuit

(Refer to Figure 2-3 and the UHF2 Frequency Synthesizer schematic diagram)

The frequency generation circuit, shown in Figure 2-3, is composed of Fractional-N synthesizer U201 and VCO/Buffer IC U241. Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the schematic for the reference designator.

The synthesizer is powered by regulated 5V and 3.3V which are provided by ICs U247 and U248 respectively. The 5V signal goes to pins 13 and 30 while the 3.3V signal goes to pins 5, 20, 34 and 36 of U201. The synthesizer in turn generates a superfiltered 5V which powers U241.

In addition to the VCO, the synthesizer also interfaces with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines (pins 7, 8 and 9) from the microprocessor, U409. A 3.3V dc signal from pin 4 indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out at pin 41 to the VCO.

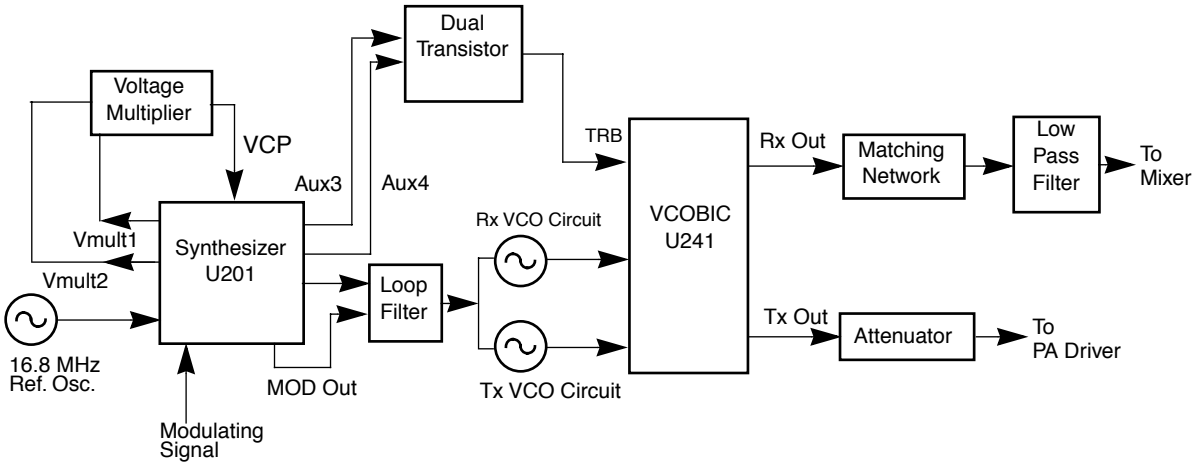


Figure 2-3 UHF2 Frequency Generation Unit Block Diagram

4.1 Synthesizer

(Refer to Figure 2-4 and the UHF2 Synthesizer schematic diagram)

The Fractional-N synthesizer, shown in Figure 2-4, uses a 16.8 MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1MHz, 2.225MHz, and 2.4MHz to be used as reference frequencies. Together with C206, C207, C208, R204 and CR203, they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8 MHz at pin 19 of U201 for use by the ASFIC and LVZIF.

The loop filter consists of components C231, C232, C233, R231, R232 and R233. This circuit provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

To achieve fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put the synthesizer within lock range. The required frequency is then locked by normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier made up of C258, C259, C228, triple diode CR201, and level shifters U210 and U211. Two 3.3V square waves, 180 degrees out of phase, are first shifted to 5V, then along with regulated 5V, put through arrays of diodes and capacitors to build up 13.3V at pin 47 of U201.

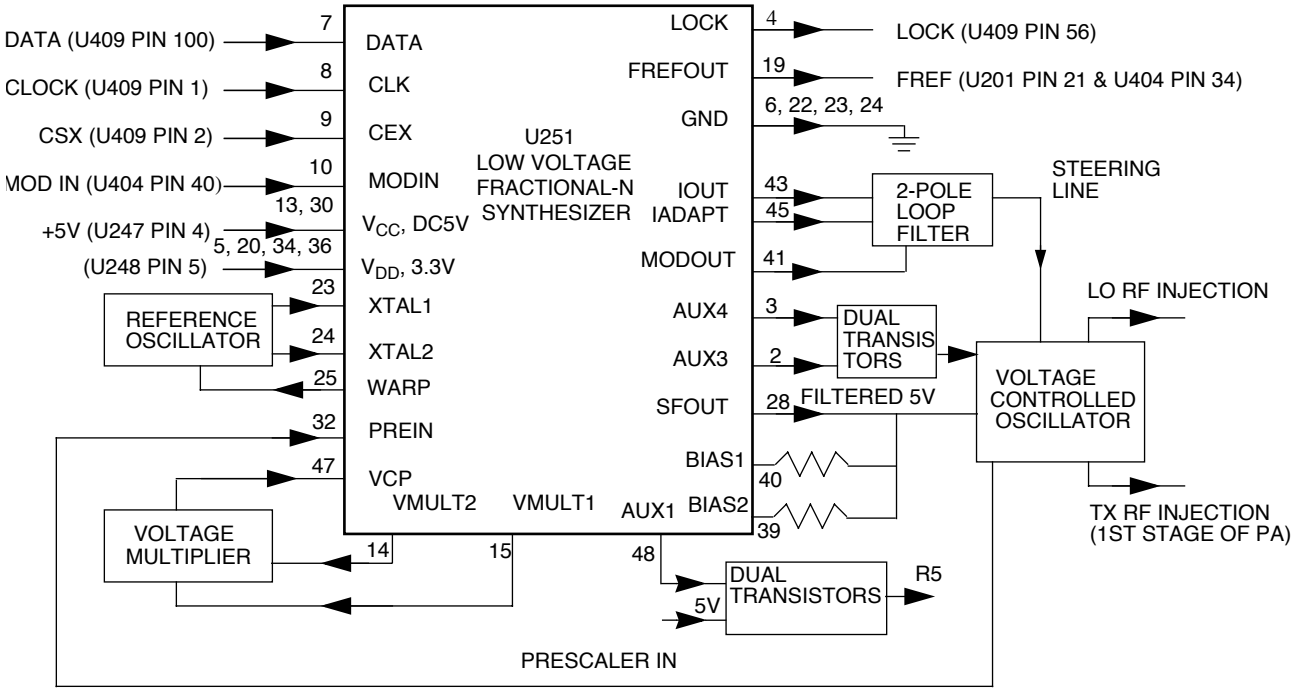


Figure 2-4 UHF2 Synthesizer Block Diagram

4.2 Voltage Control Oscillator (VCO)

(Refer to Figure 2-5 and the UHF2 Voltage Controlled Oscillator schematic diagram)

The VCOB IC (U241), shown in Figure 2-5, in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U241 pin 19) determines which oscillator and buffer are enabled. A sample of the RF signal from the enabled oscillator is routed from U241, pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 3.5V and 9.5V when the PLL is locked on frequency.

The VCOB IC is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3V. This difference in operating voltage requires a level shifter consisting of Q260 and Q261 on the TRB line. The operation logic is shown in Table 2-1.

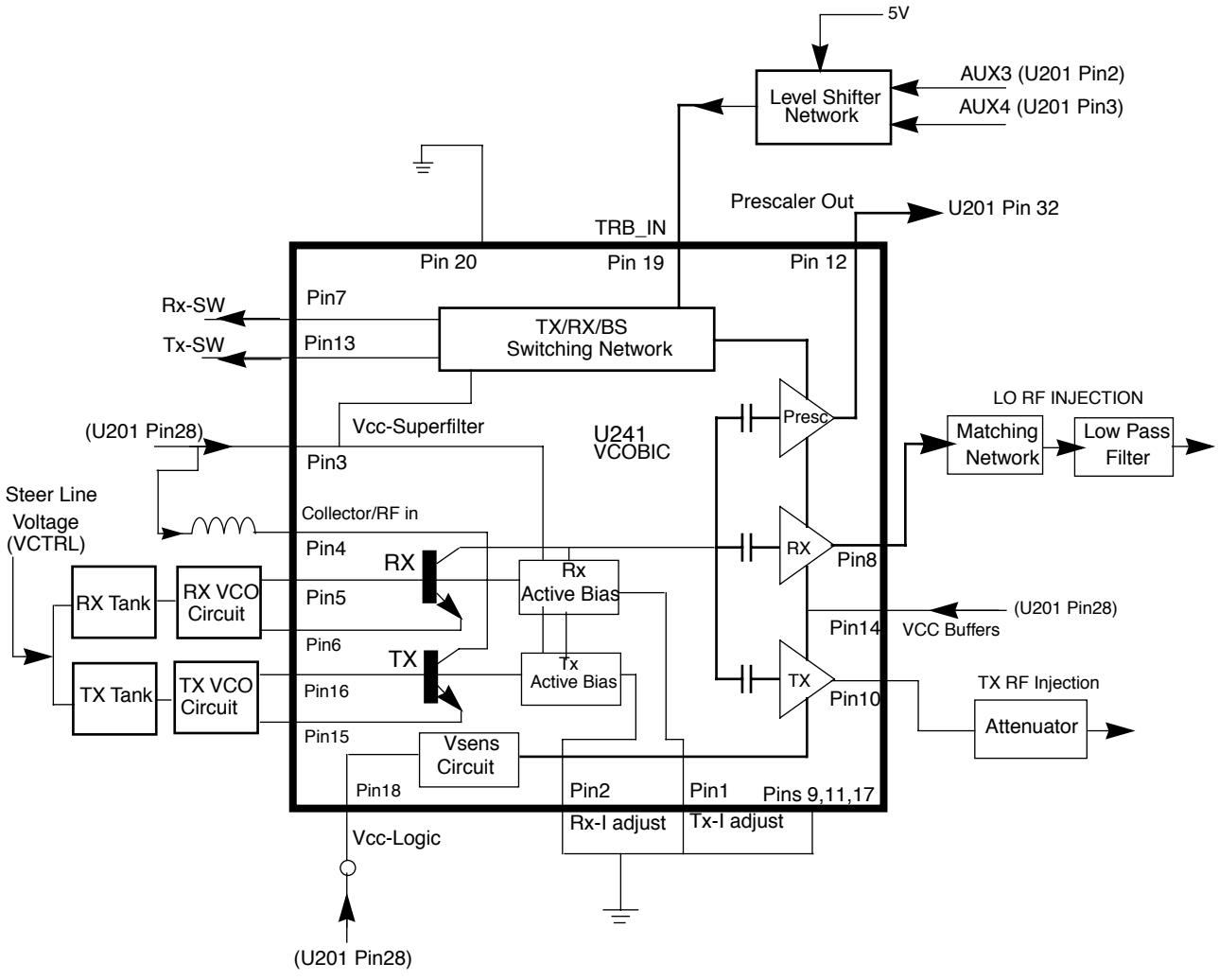


Figure 2-5 UHF2 VCO Block Diagram

Table 2-1 Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In the receive mode, U241 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U241. The RF signal at U241 pin 8 is run through a matching network. The resulting LO RF INJECTION signal is applied to the mixer at T302.

During the transmit condition, when PTT is pressed, five volts is applied to U241 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U241. The RF signal at U241 pin 10 is injected into the input of the PA module (U101 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through U201, pin 41.

When a high impedance is applied to U241 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

5.0 Voice Storage (GP1280 Only)

(Refer to Figure 2-6 and the UHF2 Voice Storage schematic diagram)

The Voice Storage feature is offered as standard in the GP1280 and as an Option board for GP340/GP360/GP380 and GP640/GP680 models.

The Voice Storage feature enables users to:

- ❑ Record and Playback Personal Memo (Reminders, Notes, etc.).
- ❑ Send over-the-air an “Out-Of-Office” message when an incoming call is received but is not available to take up call.
- ❑ Over-the-air recording of important voice message being received.

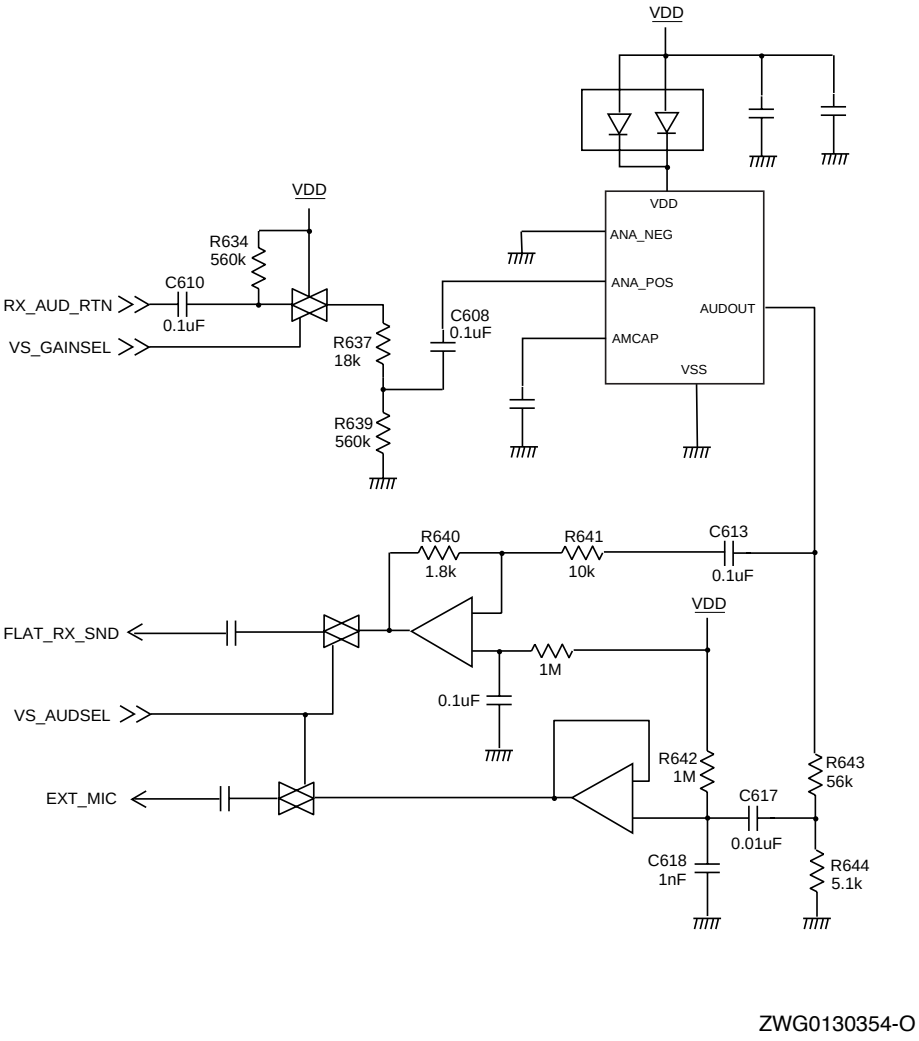


Figure 2-6 Audio path for voice storage connection to interface connector

Audio routing to the Voice Storage circuitry during receive message recording, message playback, personal memo recording and voice prompt transmit over the air are as follows:

Received Message Recording

The receive audio is tapped from the Rx_Aud_Rtn pin of the ASFIC_CMP during receive mode.

Message Playback

Message playback is via the FLAT_RX_SND pin of ASFIC_CMP. In the ASFIC_CMP, the signal is routed via the Side-Tone path to the Receive path where playback audio is routed to the speaker.

Personal Memo Recording

In this mode, voice is pick-up at the Mic. and via the Side-Tone path will be directed to the Rx_Aud_Rtn pin, which is then routed to the voice recording chip.

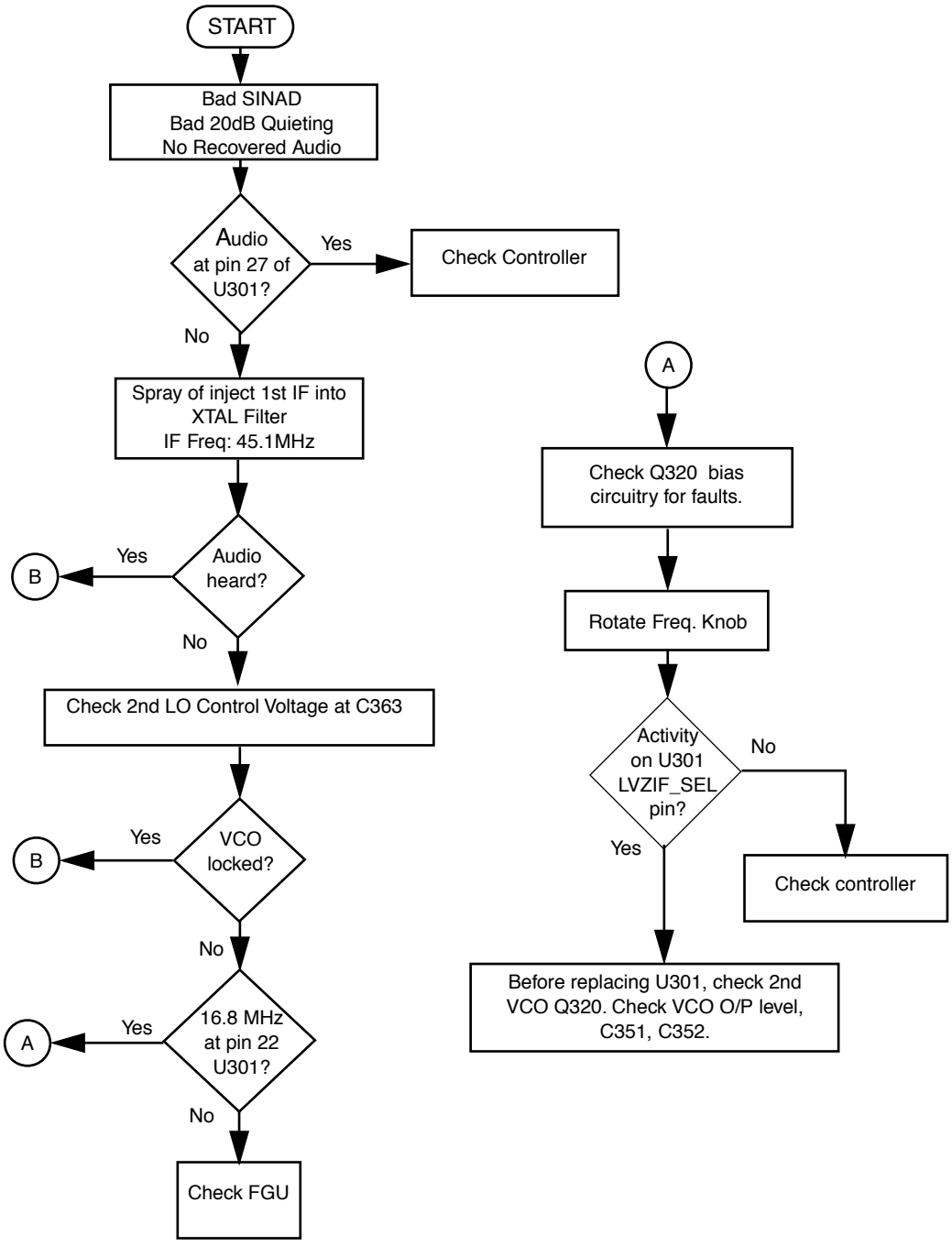
Voice Prompt transmit over the air

A personal voice prompt or Out-Of-Office Message which is stored in the IC can be transmitted over the air through mic path in the ASFIC_CMP to the calling party. This feature is similar to the Telephone Answering Machine feature when the person called is not available to attend the call.

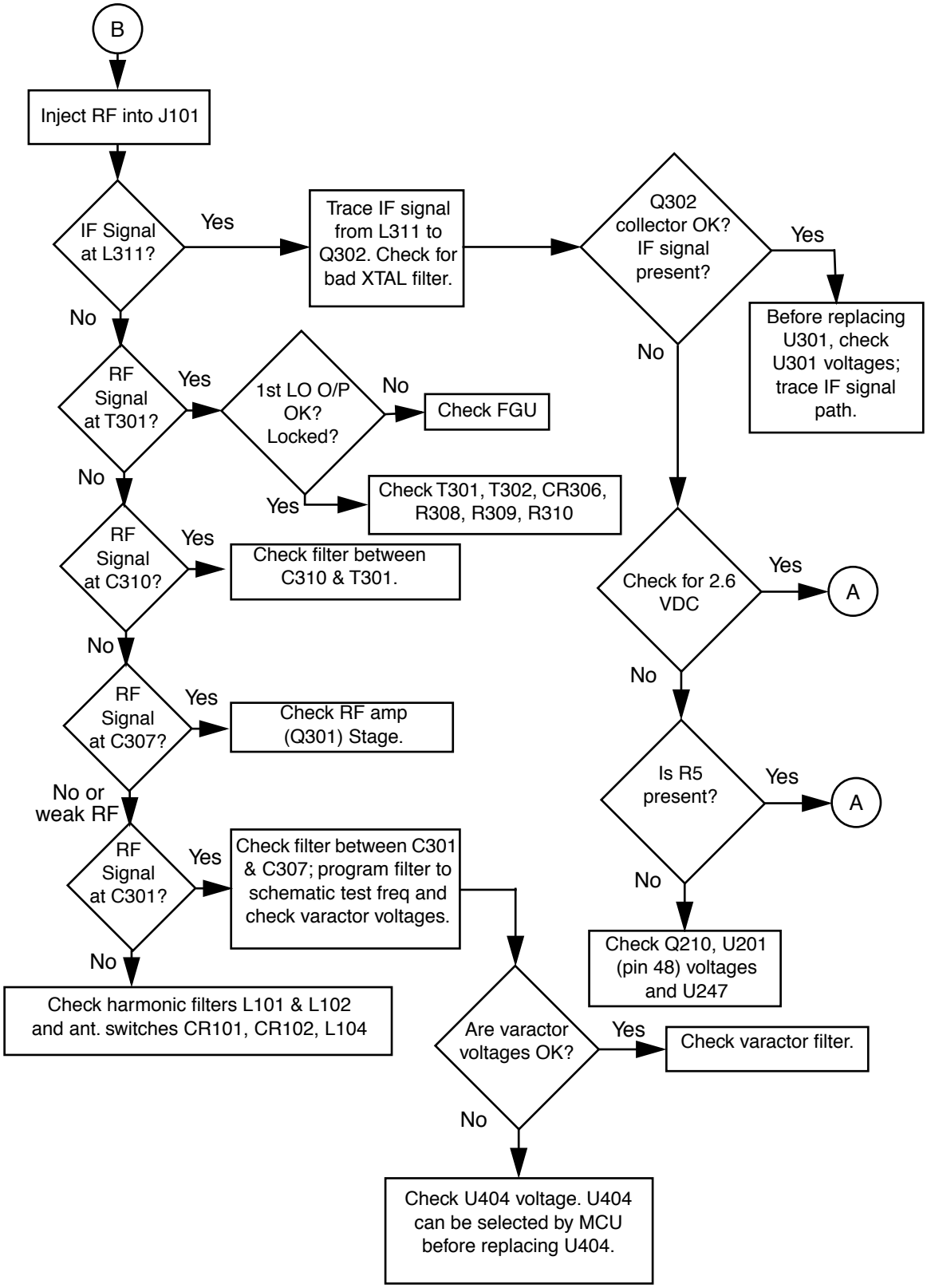
Chapter 3

TROUBLESHOOTING CHARTS

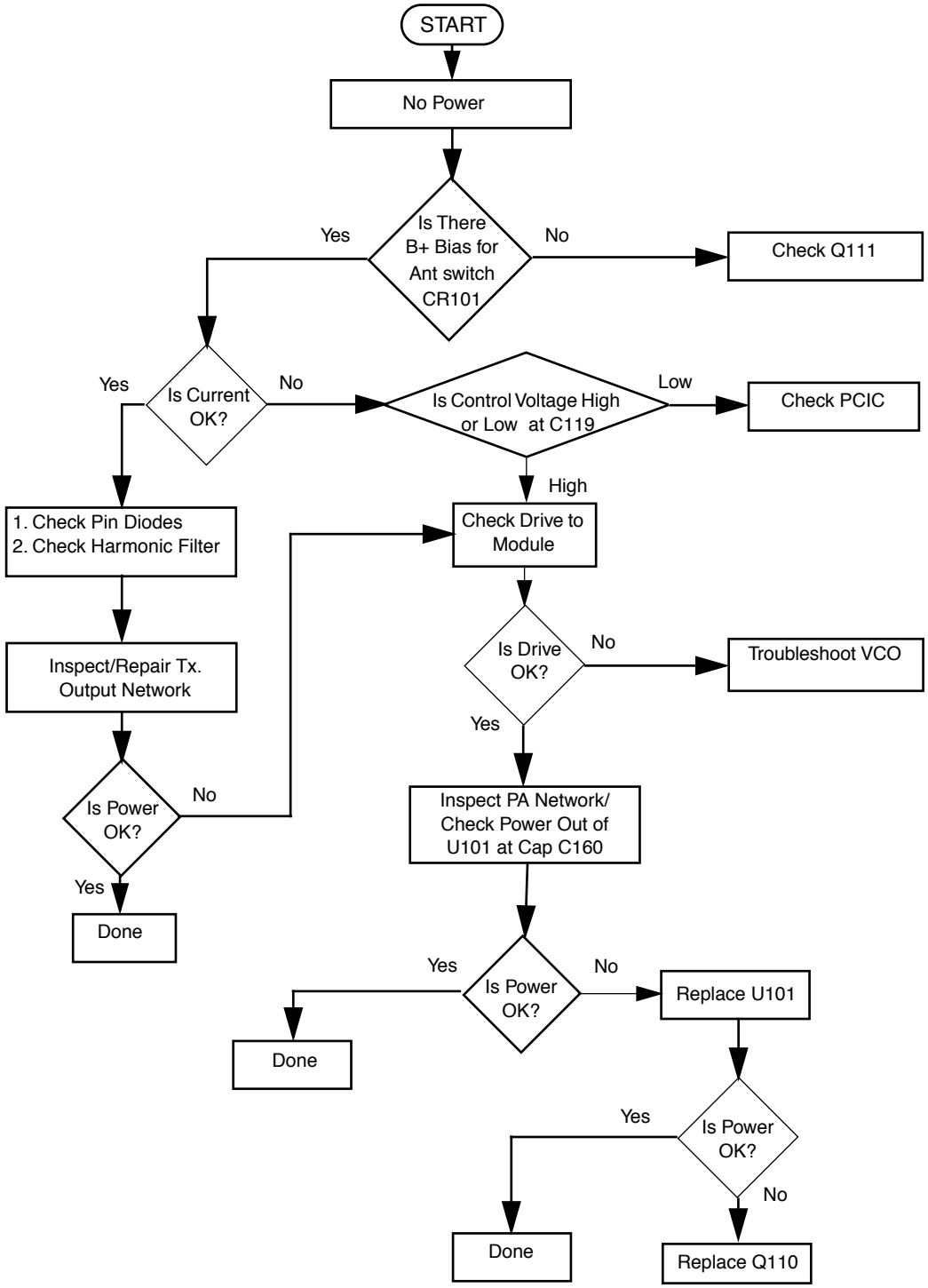
1.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



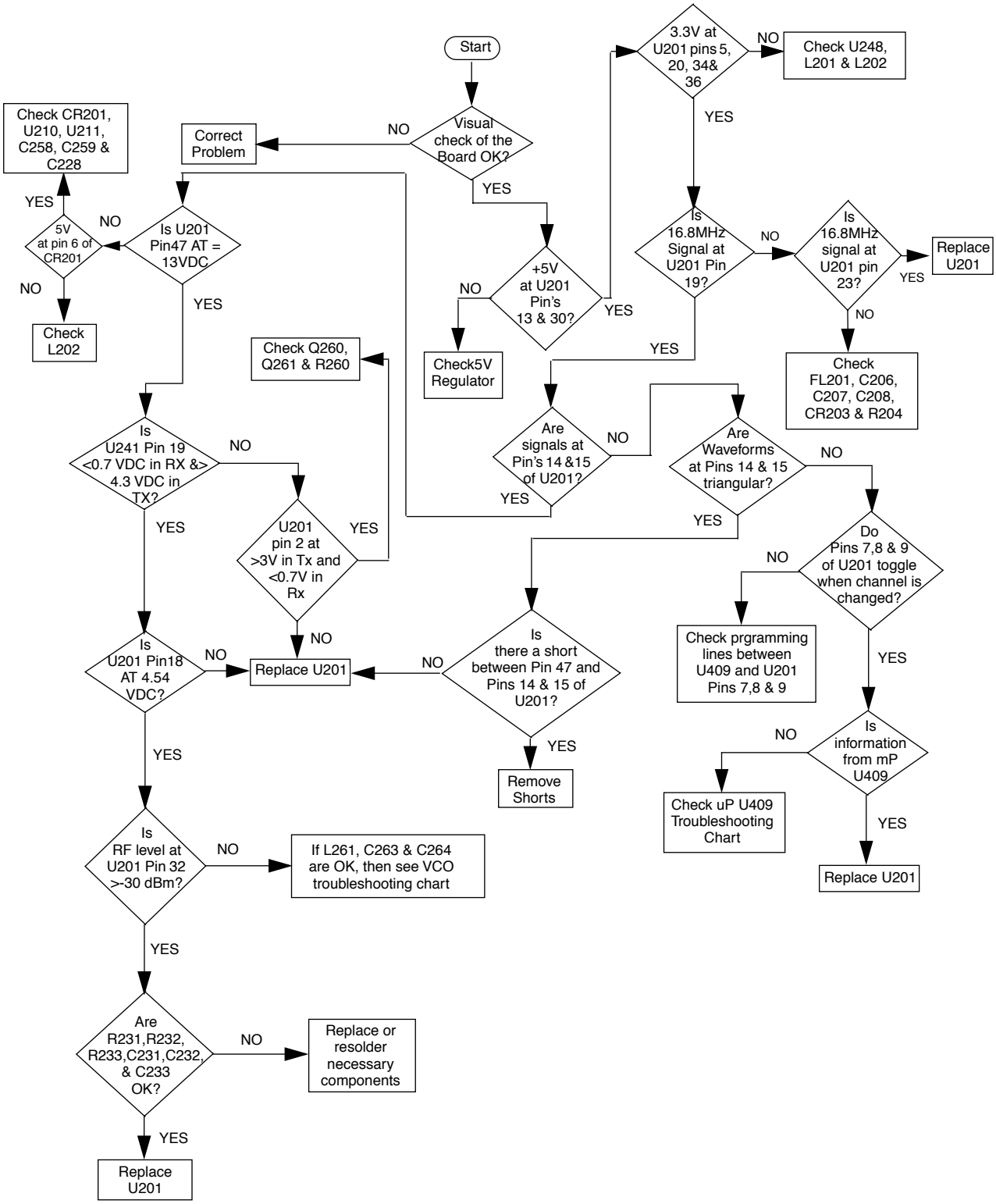
2.0 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



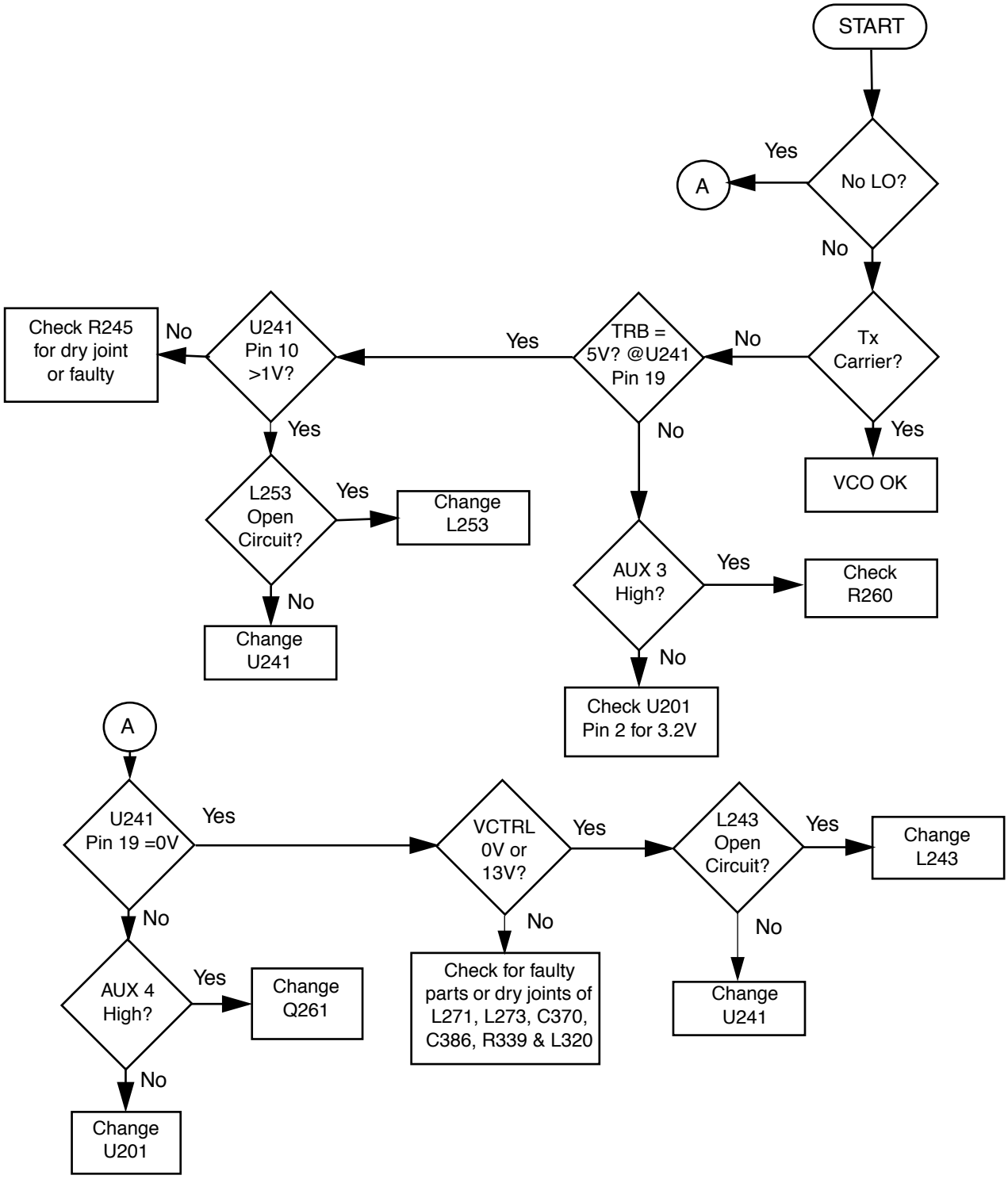
3.0 Troubleshooting Flow Chart for Transmitter



4.0 Troubleshooting Flow Chart for Synthesizer



5.0 Troubleshooting Flow Chart for VCO



Chapter 4

UHF2 PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

1.1 Controller Circuits

The UHF2 circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for the UHF2 circuits only, refer to the Controller section for details of the related Controller circuits.The PCB component layouts and the Parts Lists in this Chapter show both the Controller and UHF2 circuit components. The UHF2 schematics and the related PCB and parts list are shown in the tables below.

1.2 Voice Storage Facility

The Voice Storage facility is fitted to the GP1280 radio as standard and the schematics, component layout and parts list for these circuits are shown in this Chapter. The Voice Storage facility may be fitted to other radios in the GP Series as an option board; reference must be made to the Option Board manual in this case. The Voice Storage schematic and the related PCB is shown in Table 4-2 below.

Table 4-1 UHF2 Drawings and Parts Lists

Table 4-2 UHF2 GP1280 Drawings and Parts Lists