MOTOROLA

Professional Radio
GP Series

300R1 (300 - 350MHz)

Service Information

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Chapter 1

MODEL CHART AND TECHNICAL SPECIFICATIONS

1.0 GP340 Model Chart

Professional GP300 Series (300-350MHz)			
Model			Description
MDH25EDC9AN3_E			GP340 300R1 300-350 MHz 4W 16 CH
		Item	Description
X		PMLD4141_	GP340 Back Cover Kit
X		6864110B13_	GP340 Basic User Guide
X		PMAD4022_	9cm (300-344 MHz) Antenna
X		HNN9008_	Battery, NiMH Standard

x = Indicates one of each is required.

2.0 GP640 / GP680 Model Chart

Professional GP600 Series (300-350MHz)				
Model				Description
MDH25EDC9CK3_E				GP640 300R1 300-350 MHz 4W
	MDH25EDH9CK6_E			GP680 300R1 300-350 MHz 4W
			Item	Description
X			PMLD4125_	GP640 300R1 Back Cover Kit
	X		PMLD4126_	GP680 300R1 Back Cover Kit
X			6864110B14_	GP640 Basic User Guide
	X		6864110B19_	GP680 Basic User Guide
X	X		PMAD4022_	9cm (300-344 MHz) Antenna
X	X		HNN9008_	Battery, NiMH Standard

x = Indicates one of each is required.

3.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

General Specifications		
Channel Capacity		
GP340	16	
GP640	16 (Conventional)	
GP680	16 (Conventional)	
Power Supply	Rechargeable battery 7.5v	
Dimensions: H x W x D (mm) Height excluding knobs		
With standard high capacity NiMH battery	137 x 57.5 x 37.5	
With ultra high capacity NiMH battery	137 x 57.5 x 40.0	
With NiCD battery	137 x 57.5 x 40.0	
With Lilon battery	137 x 57.5 x 33.0	
Weight: (gm)		
	GP340/GP640	**GP680**
With Standard high capacity NiMH battery	420	428
With Ultra high capacity NiMH battery	500	508
With NiCD battery	450	458
With Lilon battery	350	358
Average Battery Life @5/5/90 Cycle:	Low Power	High Power
With Standard high capacity NiMH battery	11 hours	8 hours
With Ultra high capacity NiMH battery	14 hours	11 hours
With NiCD battery	12 hours	9 hours
With Lilon battery	11 hours	8 hours
Sealing:	Withstands rain testing per MIL STD 810 C/D /E and IP54	
Shock and Vibration:	Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603	
Dust and Humidity:	Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603	

Transmitter	300R1
*Frequencies - Full Bandsplit	300-350 MHz
Channel Spacing	12.5/20/25 kHz
Frequency Stability (-25°C to +55°C, +25° Ref.)	±2.5 ppm @ 12.5kHz ±5ppm @ 25 kHz
Power	1-4W
Modulation Limiting	±2.5 @ 12.5 kHz ±4.0 @ 20 kHz ±5.0 @ 25 kHz
FM Hum & Noise	-40 dB typical
Conducted/Radiated Emission	-36 dBm <1 GHz -30 dBm >1 GHz
Adjacent Channel Power	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB
Audio Distortion	<5% typical

Receiver	300R1
*Frequencies - Full Bandsplit	300-350 MHz
Channel Spacing	12.5/20/25 kHz
Sensitivity (12 dB SINAD) EIA Sensitivity (20 dB SINAD) ETS	0.35 µV typical 0.50 µV typical
Intermodulation ETS	-65 dB
Adjacent Channel Selectivity	-60 dB @ 12.5 kHz -70 dB @ 25 kHz
Spurious Rejection	-70 dB
Rated Audio	0.5W
Audio Distortion @ Rated Audio	<3% typical
Hum & Noise	-45 dB @ 12.5 kHz -50 dB @ 20/25 kHz
Audio Response (300 - 3000 Hz)	+1 to -3 dB
Conducted Spurious Emission	-57 dBm <1 GHz -47 dBm >1 GHz ETS 300 086

*Availability subject to the laws and regulations of individual countries.

Chapter 2

THEORY OF OPERATION

1.0 Introduction

This Chapter provides a detailed theory of operation for the 300-350MHz circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

2.0 Transmitter

(Refer to Figure 2-1 and the Transmitter schematic diagram)

The transmitter contains five basic circuits:

1. power amplifier,
2. antenna switch,
3. harmonic filter,
4. antenna matching network,
5. power control integrated circuit (PCIC).

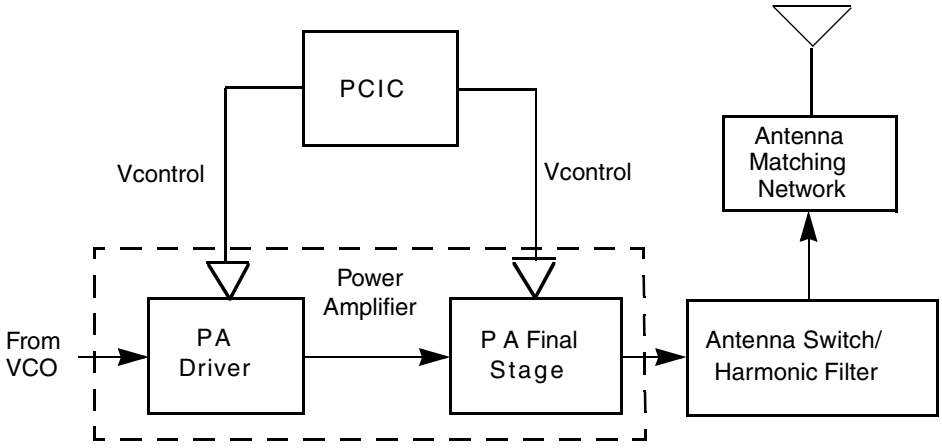


Figure 2-1 Transmitter Block Diagram.

2.1 Power Amplifier

The power amplifier consists of two devices:

1. 9Z67 LDMOS driver IC (U101) and
2. PRF1507 LDMOS PA (Q110).

The 9Z67 LDMOS driver IC contains 2 stages of amplification with a supply voltage of 7.3V.

This RF power amplifier is capable of supplying an output power of 0.3W (pin 6 and 7) with an input signal of 2mW (3dBm) (pin16). The current drain would typically be 160mA while operating in the frequency range of 300-350MHz.

The PRF1507 LDMOS PA is capable of supplying an output power of 7W with an input signal of 0.3W. The current drain would typically be 1300mA while operating in the frequency range of 300-350MHz. The power output can be varied by changing the biasing voltage.

2.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C107, L104 and C106), and two current limiting resistors (R101, R170). In the transmit mode, B+ at PCIC (U102) pin 23 will go low and turn on Q111 where a B+ bias is applied to the antenna switch circuit to bias the diodes "on". The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

2.3 Harmonic Filter

The harmonic filter consists of C104, L102, C103, L101 and C102. The design of the harmonic filter for VHF is that of a modified Zolotarev design. It has been optimized for efficiency of the power module. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2dB.

2.4 Antenna Matching Network

A matching network which is made up of L116 is used to match the antenna's impedance to the harmonic filter. This will optimize the performance of the transmitter and receiver into an antenna.

2.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R101, which provides a voltage proportional to the current drain. This voltage is then fedback to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C133, C134 and C135) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

CR105 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and output a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

3.0 Receiver

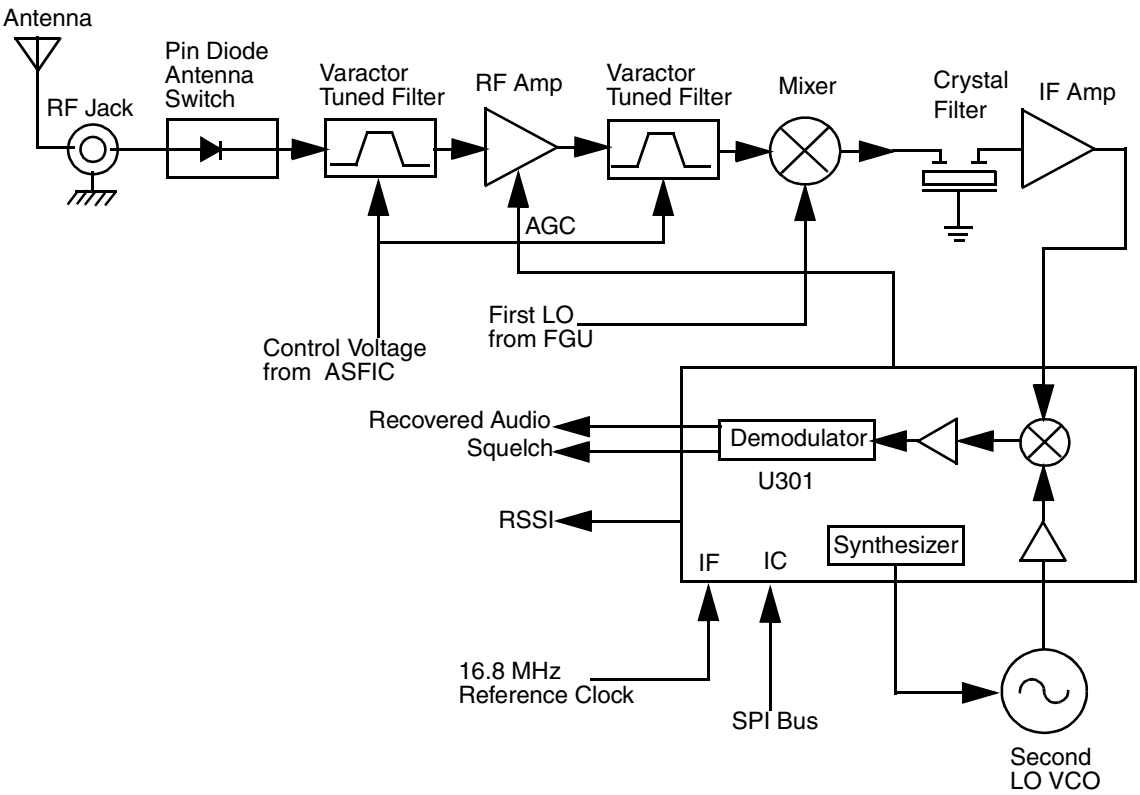


Figure 2-2 Receiver Block Diagram

3.1 Receiver Front-End

(Refer to Figure 2-2 and the Receiver Front End schematic diagram)

The RF signal is received by the antenna and applied to a low-pass filter. For 300R1, the filter consists of L101, L102, C102, C103, C104. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes (CR101 and CR102) and a pi network (C106, L104 and C107). The signal is then applied to a varactor tuned bandpass filter. The VHF bandpass filter comprises of L301, L302, C302, C303, C304, CR301 and CR302. The bandpass filter is tuned by applying a control voltage to the varactor diodes (CR301 and CR302) in the filter.

The bandpass filter is electronically tuned by the DACRx from U404 which is controlled by the microprocessor. Depending on the carrier frequency, the DACRx will supply the tuned voltage to the varactor diodes in the filter. Wideband operation of the filter is achieved by shifting the bandpass filter across the band.

The output of the bandpass filter is coupled to the RF amplifier transistor Q301 via C307. After being amplified by the RF amplifier, the RF signal is further filtered by a second varactor tuned bandpass filter, consisting of L306, L307, C313, C317, CR304 and CR305.

Both the pre and post-RF amplifier varactor tuned filters have similar responses. The 3dB bandwidth of the filter is about 50 MHz. This enables the filters to be electronically controlled by using a single control voltage which is DACRx .

The output of the post-RF amplifier filter which is connected to the passive double balanced mixer consists of T301, T302 and CR306. Matching of the filter to the mixer is provided by C381. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 45.1 MHz IF signal.

The IF signal coming out of the mixer is transfered to the crystal filter (FL301) through a resistor pad and a diplexer (C322 and L310). Matching to the input of the crystal filter is provided by C324 and L311. The crystal filter provides the necessary selectivity and intermodulation protection.

3.2 Receiver Back-End

(Refer to Figure 2-2 and the Receiver Back-End schematic diagram)

The output of crystal filter FL301 is matched to the input of IF amplifier transistor Q302 by components R352 and C325. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). The IF amplifer provides a gain of about 7dB. The amplified IF signal is then coupled into U301(pin 3) via C330, C338 and L330 which provides the matching for the IF amplifier and U301.

The IF signal applied to pin 3 of U301 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U301. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U301).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U301 so that it is very close to the first IF frequency. The IF IC (U301) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q320. The VCO has a varactor diode, CR310, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of C362, C363, C364, R320 and R321.

The IF IC (U301) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used as a peak indicator during the bench tuning of the receiver front-end varactor filter. The RSSI voltage is also used to control the automatic gain control (AGC) circuit at the front-end.

The demodulated signal on pin 27 of U301 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

3.3 Automatic Gain Control Circuit

(Refer to the Receiver Front End and Receiver Back End schematic diagrams)

The front end automatic gain control circuit is to provide automatic gain reduction of the front end RF amplifier via feedback. This action is necessary to prevent overloading of backend circuits. This is achieved by drawing some of the output power from the RF amplifier's output. At high radio frequencies, capacitor C331 provides the low impedance path to ground for this purpose. CR308 is a PIN diode used for switching the path on or off. A certain amount of forward biasing current is needed to turn the PIN diode on. Transistors Q315 provides this current where upon saturation, current will flow via R347, PIN diode, collector and emitter of Q315 and R319 before going to ground. Q315 is an NPN transistor used for switching here. Maximum current flowing through the PIN is mainly limited by the resistor R319.

Radio signal strength indicator, RSSI, a voltage signal, is used to drive Q315 to saturation hence turning it on. RSSI is produced by U301 and is proportional to the gain of the RF amplifier and the input RF signal power to the radio.

Resistor network at the input to the base of Q315 is scaled to turn on Q315, hence activating the AGC, at certain RSSI levels. In order to turn on Q315, the voltage across the transistor's base to ground must be greater or equal to the voltage across R319, plus the base-emitter voltage (Vbe) present at Q315. The resistor network with thermistor RT300 is capable of providing temperature compensation to the AGC circuit, as RSSI generated by U301 is lower at cold temperatures compared to normal operation at room temperature. Resistor R300 and capacitor C397 form an R-C network used to dampen any transient instability while the AGC is turning on.

4.0 Frequency Generation Circuitry

(Refer to Figure 2-3 and the Frequency Synthesizer schematic diagram)

The Frequency Generation Circuitry is composed of two main ICs, the Fractional-N synthesizer (U201), and the VCO/Buffer IC (U241). Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

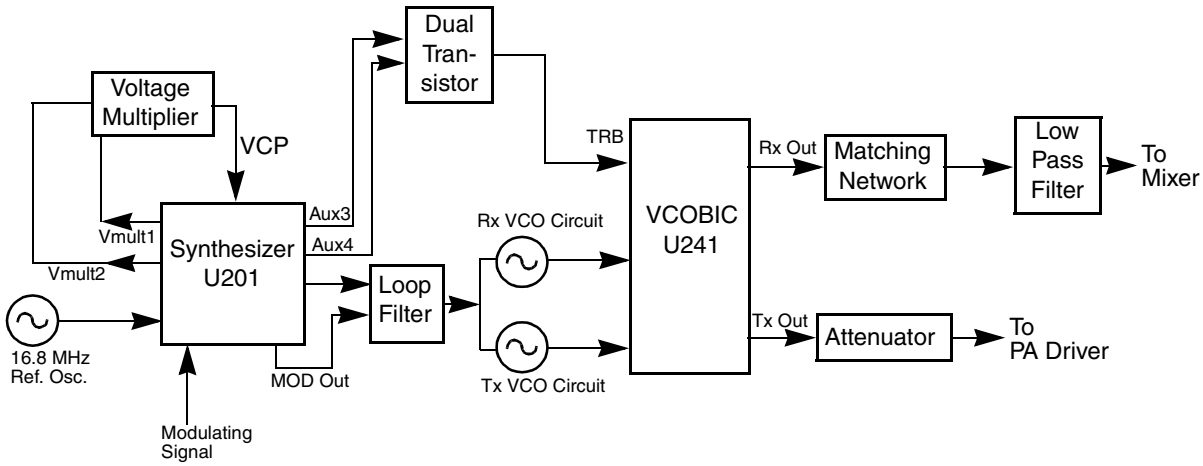


Figure 2-3 Frequency Generation Unit Block Diagram

The synthesizer is powered by regulated 5V and 3.3V which come from U247 and U248 respectively. The synthesizer in turn generates a superfiltered 4.5V which powers U241.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data , clock and chip select lines from the microprocessor. A 3.3V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

4.1 Synthesizer

(Refer to Figure 2-4 and the Synthesizer schematic diagram)

The Fractional-N Synthesizer uses a 16.8MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1MHz, 2.225MHz, and 2.4MHz as reference frequencies. Together with C206, C207, C208, R204 and CR203 , they build up the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8MHz at pin 19 of U201 to be used by ASFIC and LVZIF.

The loop filter which consist of C231, C232, C233, R231, R232 and R233 provides the necessary dc steering voltage for the VCO and determines the amount of noise and spur passing through.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put synthesizer within the lock range. The required frequency is then locked by normal mode charge pump at pin 43 .

Both the normal and adapt charge pumps get their supply from the capacitive voltage multiplier which is made up of C258, C259, C228, triple diode CR201 and level shifters U210 and U211. Two 3.3V square waves (180 deg out of phase) are first shifted to 5V, then along with regulated 5V , put through arrays of diodes and capacitors to build up 13.3V at pin 47 of U201.

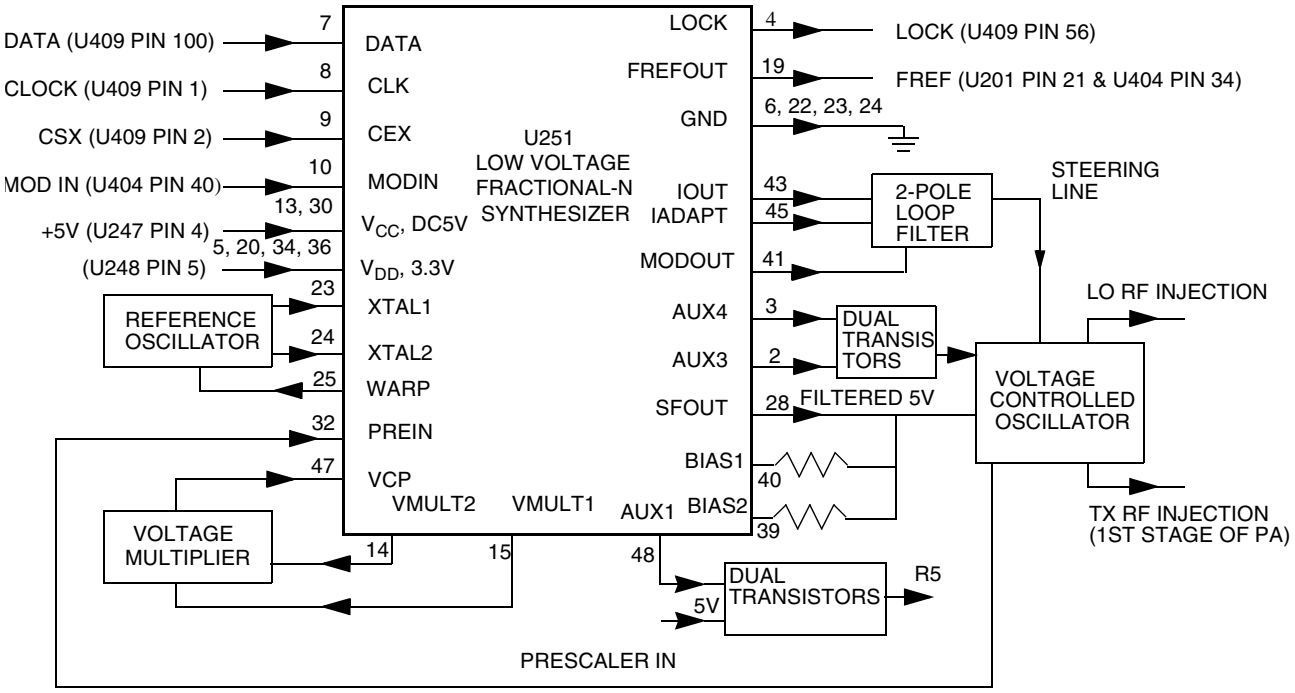


Figure 2-4 Synthesizer Block Diagram

4.2 Voltage Controlled Oscillator (VCO)

(Refer to Figure 2-5 and the Voltage Controlled Oscillator schematic diagram)

The VCOBIC (U241) in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U241 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U241 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 3.5V and 9.5V when the PLL is locked on frequency.

The VCOBIC(U241) is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3V. This difference in operating voltage requires a level shifter consisting of Q260 and Q261 on the TRB line.

The operation logic is shown in Table 2-1.

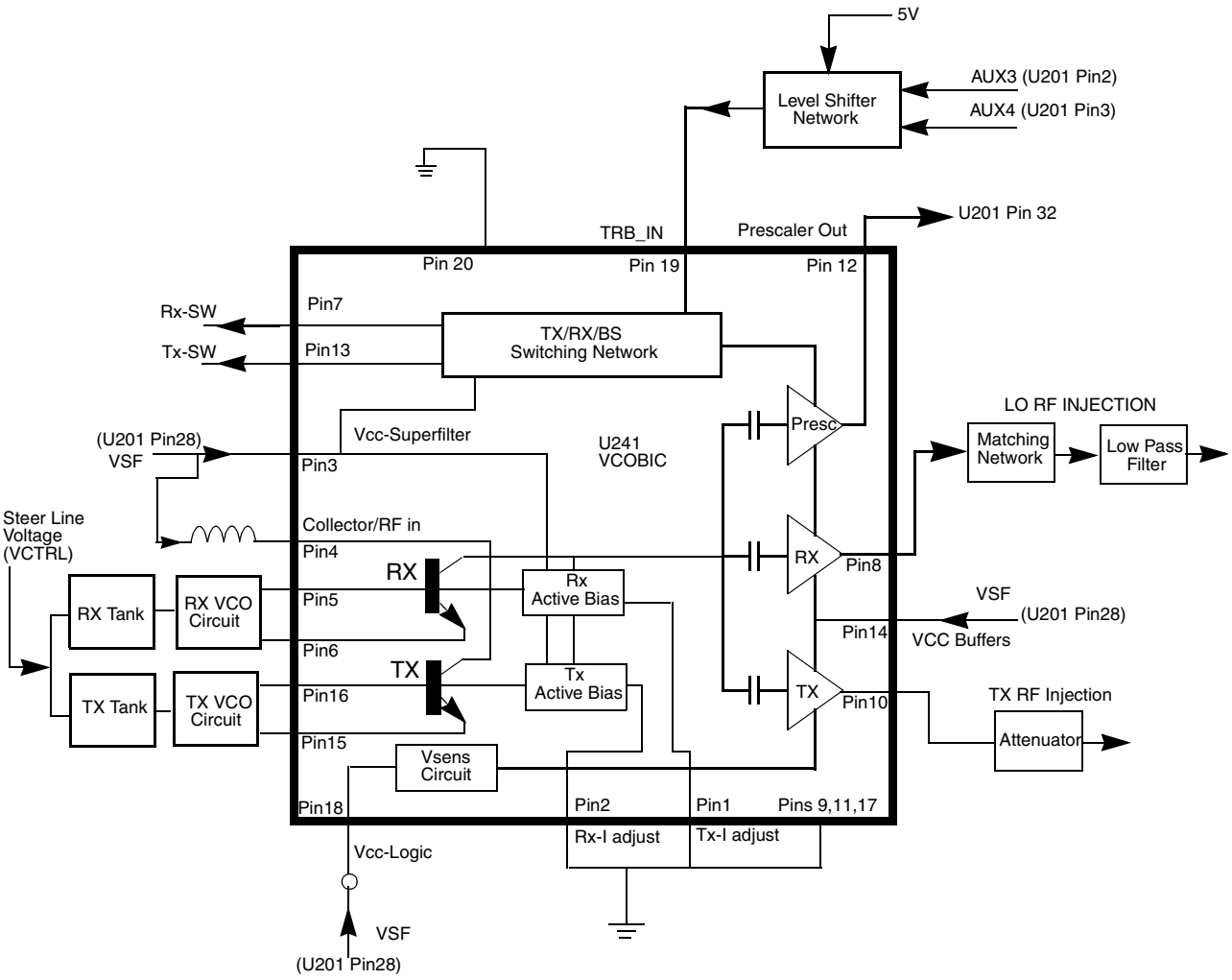


Figure 2-5 VCO Block Diagram

Table 2-1 Level Shifter Logic

Desired Mode	AUX 4	AUX 3	TRB
Tx	Low	High (@3.2V)	High (@4.8V)
Rx	High	Low	Low
Battery Saver	Low	Low	Hi-Z/Float (@2.5V)

In the receive mode, U241 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U241. The RF signal at U241 pin 8 is run through a matching network. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at T302.

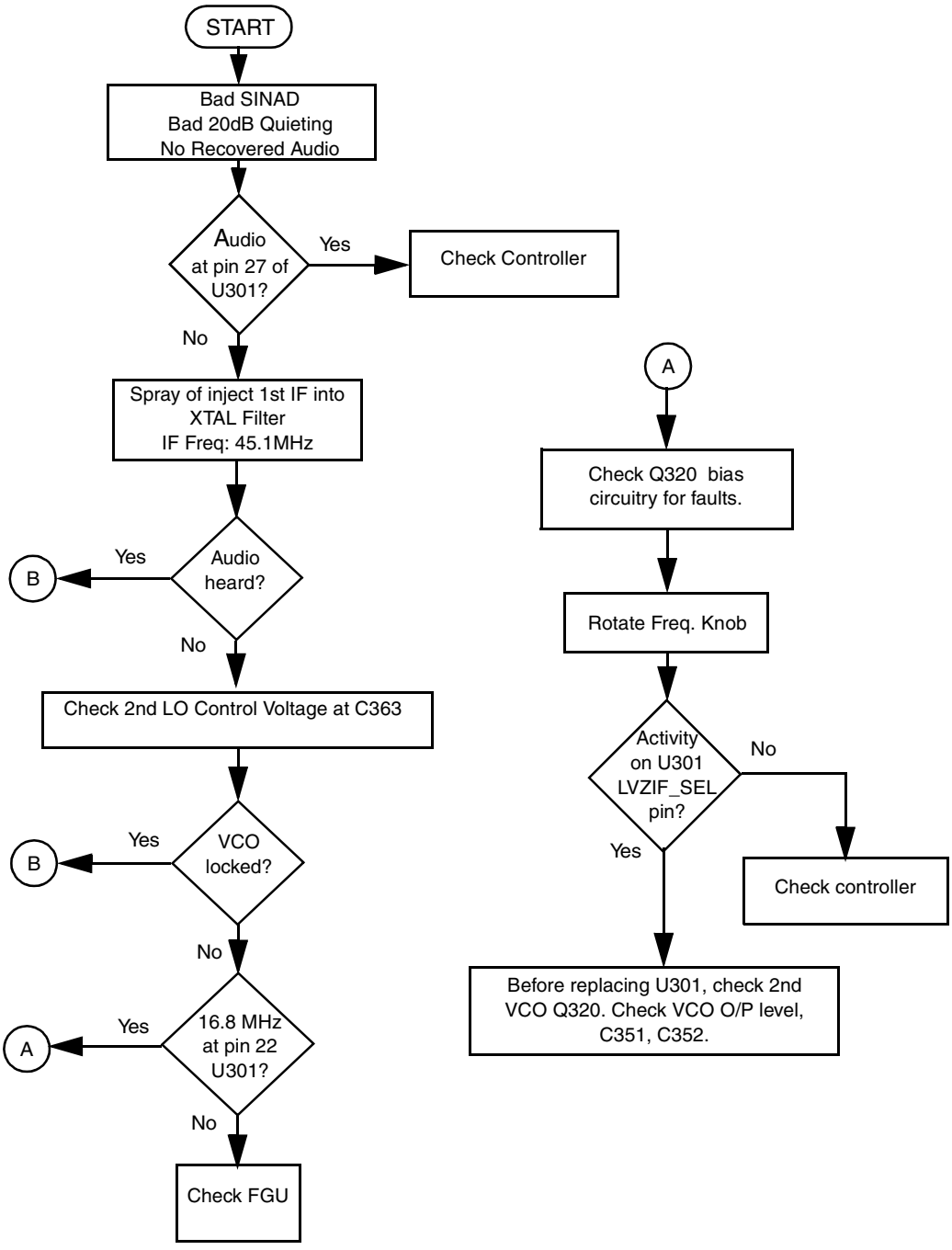
During the transmit condition, when PTT is depressed, five volts is applied to U241 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U241. The RF signal at U241 pin 10 is injected into the input of the PA module (U101 pin16). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U241 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

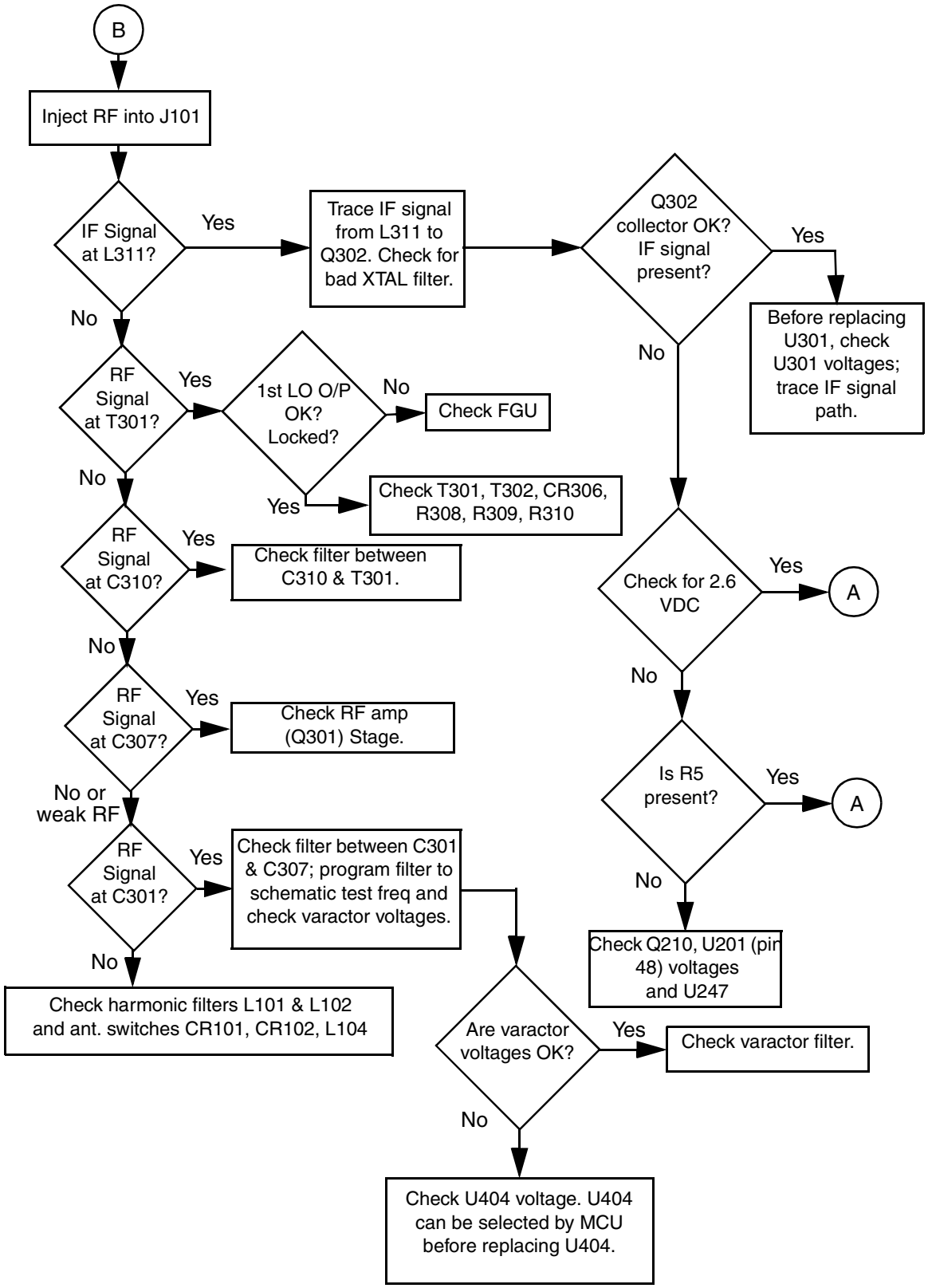
Chapter 3

TROUBLESHOOTING CHARTS

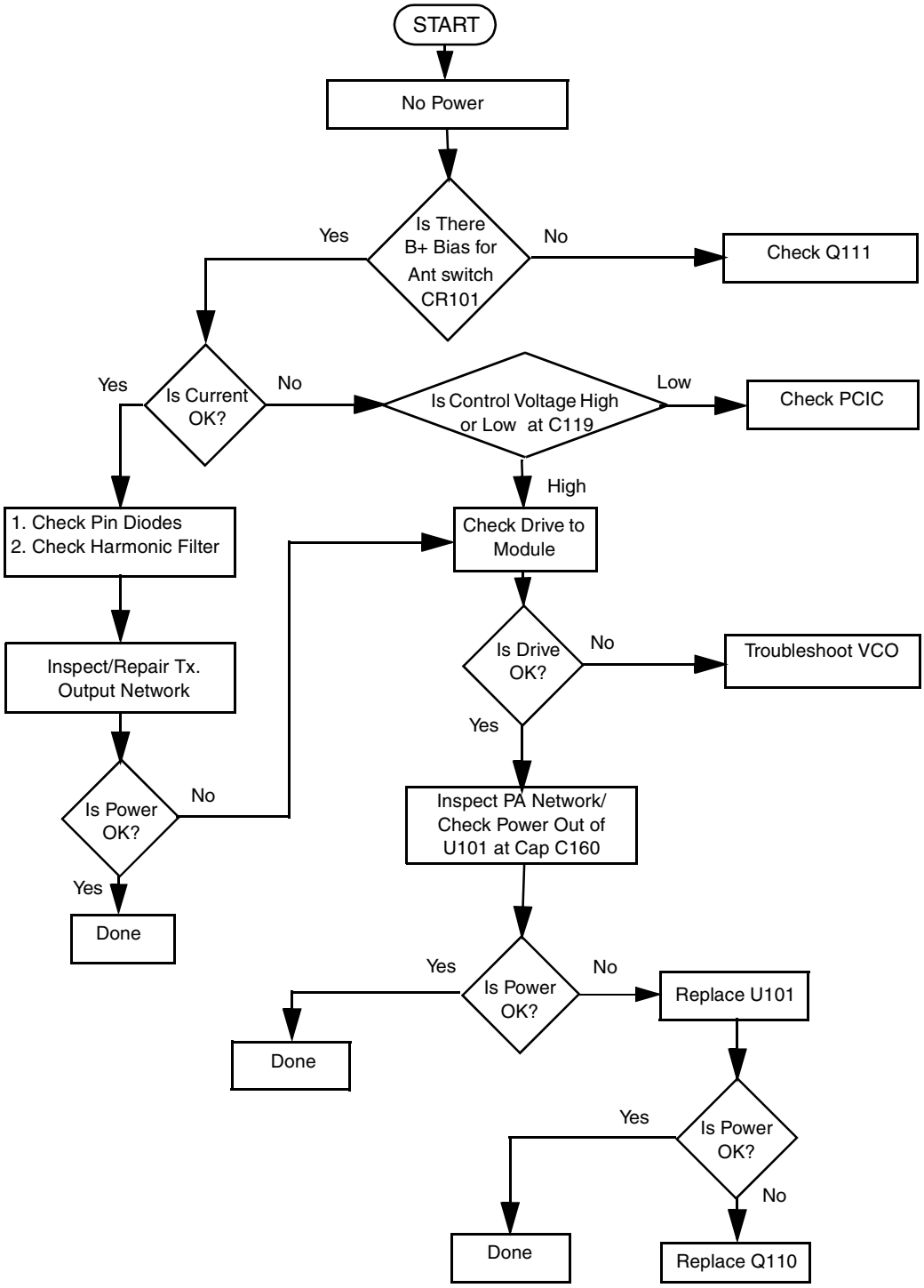
1.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



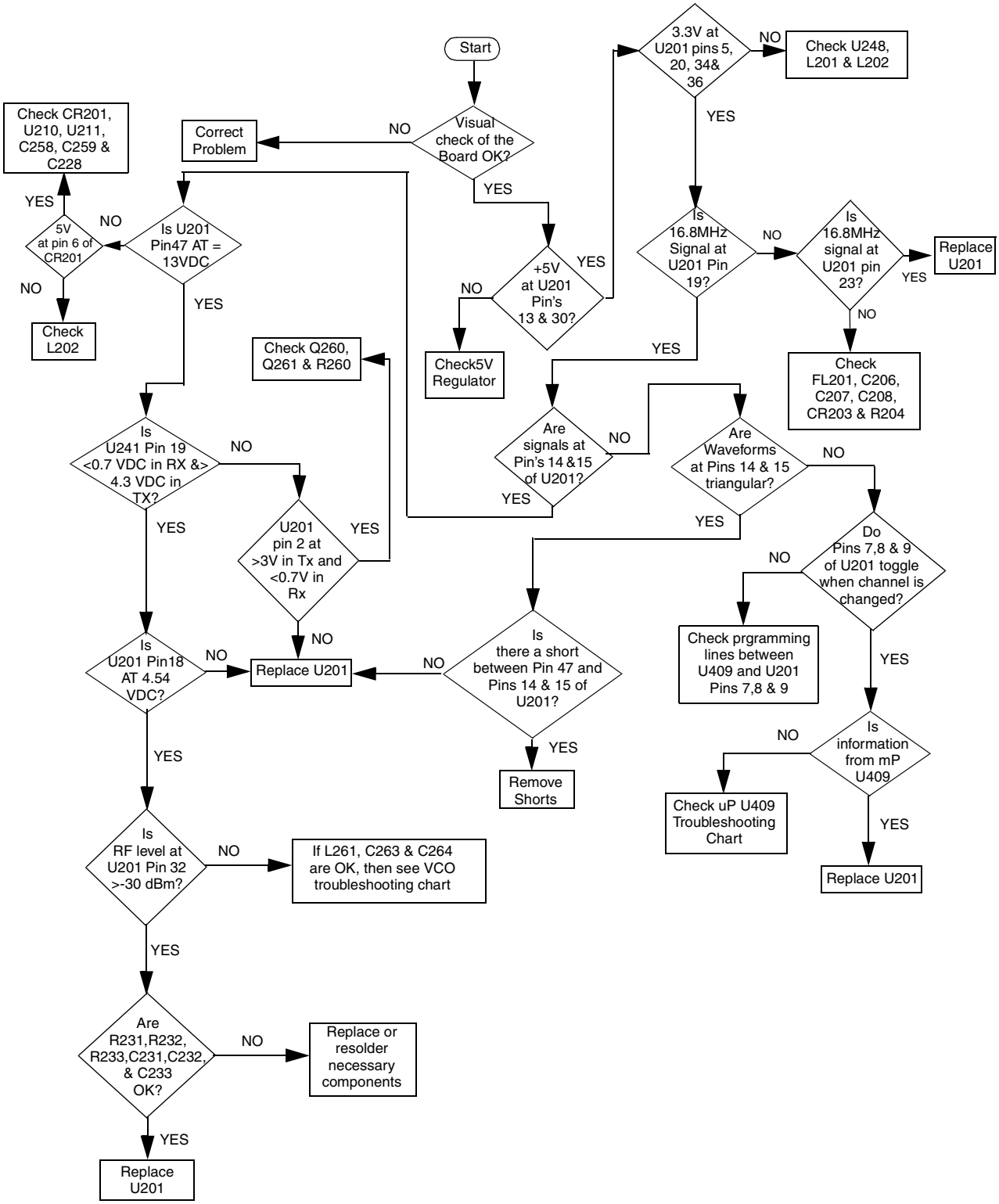
2.0 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



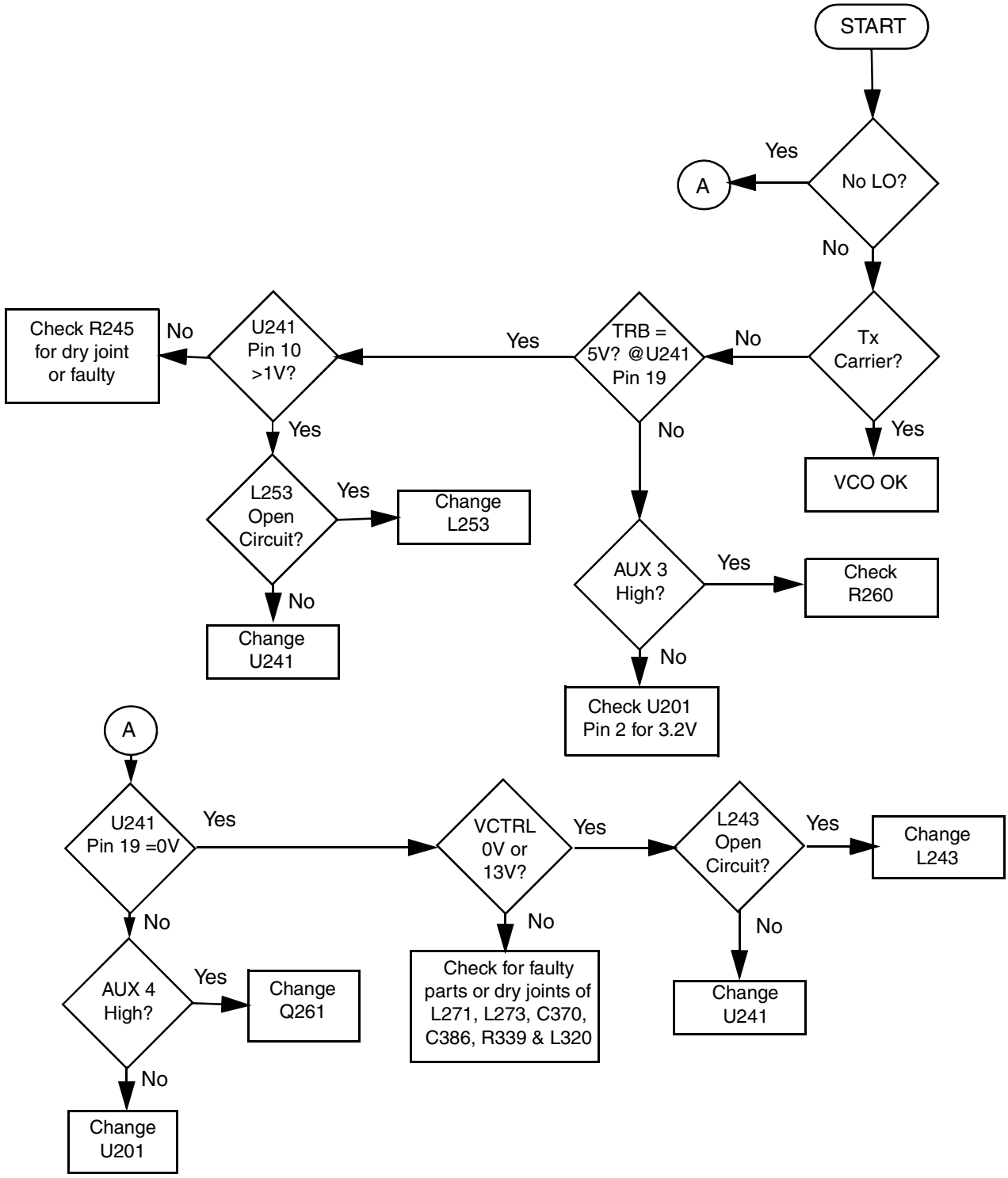
3.0 Troubleshooting Flow Chart for Transmitter



4.0 Troubleshooting Flow Chart for Synthesizer



5.0 Troubleshooting Flow Chart for VCO



Chapter 4

PCB/SCHEMATICS/PARTS LISTS

1.0 Allocation of Schematics and Circuit Boards

1.1 Controller Circuits

The 300-350MHz circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This Chapter shows the schematics for the 300R1 circuits only, refer to the Controller section for details of the related Controller circuits.The PCB component layouts and the Parts Lists in this Chapter show both the Controller and 300R1 circuit components. The 300R1 schematics and the related PCB and parts list are shown in the tables below.

Table 4-1 Diagrams and Parts Lists