MOTOROLA

# Professional Radio
# GP Series

800 MHz (806 - 870MHz)

Service Information

Issue: June 2002

# Computer Software Copyrights

# Table of Contents

## Chapter 1 MODEL CHART AND TECHNICAL SPECIFICATIONS



## Chapter 2 THEORY OF OPERATION



## Chapter 3 TROUBLESHOOTING CHARTS



## Chapter 4 800 MHz PCB/SCHEMATICS/PARTS LISTS

# Chapter 1

# MODEL CHART AND TECHNICAL SPECIFICATIONS

## 1.0 GP240/GP280/GP540/GP580 Model Chart

| Professional GP200/GP500 Series (800 MHz) | | | | | | |
|---|---|---|---|---|---|---|
| Model | | | | | | Description |
| MDH25UCC6FC3 | | | | | | GP540 800MHz 806-870MHz 2.5W |
| | MDH25UCH6FC6 | | | | | GP580 800MHz 806-870MHz 2.5W |
| | | MDH25UCC6FB3 | | | | GP240 800MHz 806-870MHz 2.5W |
| | | | MDH25UCH6FB6 | | | GP280 800MHz 806-870MHz 2.5W |
| | | | | | | |
| | | | | | Item | Description |
| X | | X | | | *PMLF4020_ | GP240/GP540 800MHz Back Cover Kit |
| | X | | X | | *PMLF4021_ | GP280/GP580 800MHz Back Cover Kit |
| X | | X | | | *PMLN4216_ | GP240/GP540 800MHz Front Housing Kit |
| | X | | X | | *PMLN4373_ | GP280/GP580 800MHz Front Housing Kit |
| X | X | X | X | | NAF5037_ | 800MHz Whip Antenna |
| | | X | X | | 6864120B15 | GP240/GP280 User Guide (English) |
| | | X | X | | 6864120B16 | GP240/GP280 User Guide (ENG, RUS, FR, TUR) |
| | | X | X | | 6864120B17 | GP240/GP280 User Guide (GER, SPA, POR, IT) |
| | | X | X | | 6864120B18 | GP240/GP280 User Guide (SWE,NL, DAN, FIN) |
| | | X | X | | 6864120B19 | GP240/GP280 User Guide (CZ, PL, HU, RO) |
| X | X | | | | 6864120B20 | GP540/GP580 User Guide (English) |
| X | X | | | | 6864120B21 | GP540/GP580 User Guide (ENG, RUS, FR, TUR) |
| X | X | | | | 6864120B22 | GP540/GP580 User Guide (GER, SPA, POR, IT) |
| X | X | | | | 6864120B23 | GP540/GP580 User Guide (SWE,NL, DAN, FIN) |
| X | X | | | | 6864120B24 | GP540/GP580 User Guide (CZ, PL, HU, RO) |
| X | X | X | X | | HNN9008_ | Battery, High Capacity NiMH, Standard |

One user guide is selectable via option.

x = Indicates one of each is required.

* = Service replacement boards.

## 2.0 Technical Specifications

Data is specified for +25°C unless otherwise stated.

| General Specifications | | |
|---|---|---|
| Channel Capacity<br>**GP240**<br>**GP280**<br>**GP540**<br>**GP580** | 128 in conv. Mode | |
| Power Supply | Rechargeable battery 7.5Volts ±20% | |
| Dimensions: H x W x D (mm) Height excluding knobs<br>With standard high capacity NiMH battery<br>With ultra high capacity NiMH battery<br>With NiCD battery<br>With Lilon battery | **GP240/280/540/580**<br>137 x 57.5 x 37.5<br>137 x 57.5 x 40.0<br>137 x 57.5 x 40.0<br>137 x 57.5 x 33.0 | |
| Weight: (gm) | **GP240/GP540** | **GP280/GP580** |
| With Standard high capacity NiMH battery | 420 | 428 |
| With Ultra high capacity NiMH battery | 500 | 508 |
| With NiCD battery | 450 | 458 |
| With Lilon battery | 350 | 358 |
| Average Battery Life @5/5/90 Cycle: | Low Power | High Power |
| With Standard high capacity NiMH battery | 11 hours | 8 hours |
| With Ultra high capacity NiMH battery | 14 hours | 11 hours |
| With NiCD battery | 12 hours | 9 hours |
| With Lilon battery | 11 hours | 8 hours |
| Sealing: | Withstands rain testing per MIL STD 810 C/D /E and IP54 | |
| Shock and Vibration: | Protection provided via impact resistant housing exceeding MIL STD 810-C/D /E and TIA/EIA 603 | |
| Dust and Humidity: | Protection provided via environment resistant housing exceeding MIL STD 810 C/D /E and TIA/EIA 603 | |

| Transmitter | 800 MHz |
|---|---|
| *Frequencies - Full Bandsplit | 806 - 825 MHz<br>851 - 870 MHz |
| Channel Spacing | 25 and 20 kHz |
| Frequency Stability<br>(-30°C to +60°C) | ±1.5PPM |
| RF Output NiMH @ 7.5V: | 806 - 825 MHz: 1-2.5W<br>851 - 870 MHz: 1-2.0W |
| Audio Distortion:<br>@ 1000Hz, 60% Rated Max. Dev. | <5% |
| FM Noise | -40 dB |
| Spurs/Harmonics:<br>(Conducted/Radiated Emission) | -36 dBm |
| Audio Response<br>(from 6dB/oct. Pre-Emphasis, 300 - 3000 Hz) | +1 to -3 dB |

| Receiver | 800 MHz |
|---|---|
| *Frequencies - Full Bandsplit | 851- 870 MHz |
| Channel Spacing | 25 and 20 kHz |
| Sensitivity (12 dB SINAD) EIA | 0.35 µV |
| Intermodulation | -65 dB |
| Adjacent Channel Selectivity | -70 dB |
| Spurious Rejection | -70 dB |
| Image Rejection | -70 dB |
| Audio Distortion @ Rated Audio | <3% typical |
| Frequency Stability<br>(-30°C to +60°C) | ±1.5PPM |
| Audio Output @ <5% Distortion | 500 mW |

*Availability subject to the laws and regulations of individual countries.

# Chapter 2

# THEORY OF OPERATION

## 1.0 Introduction

This Chapter provides a detailed theory of operation for the UHF circuits in the radio. For details of the theory of operation and trouble shooting for the the associated Controller circuits refer to the Controller Section of this manual.

## 2.0 800 MHz Transmitter

(*Refer to Figure 2-1 and the 800 MHz Transmitter schematic diagram*)

The 800 MHz transmitter consists of the following basic circuits:

1. Power amplifier (PA).
2. Antenna switch.
3. Harmonic filter.
4. Power Control Integrated Circuit (PCIC).

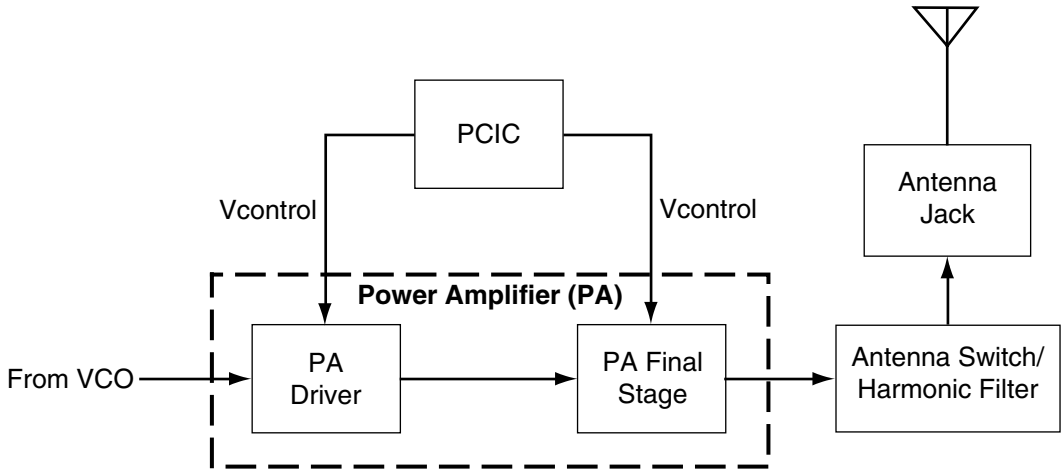



**Figure 2-1** 800 MHz Transmitter Block Diagram.

### 2.1 Power Amplifier

The power amplifier (PA) consists of two principle devices:

1. 63J66 driver IC (U101).
2. 85Y73 LDMOS PA (Q101).

The 63J66 driver IC contains a 2 stage amplification with a supply voltage of 7.5V.

This RF driver IC is capable of supplying an output power of 0.3W (pin 13 and 14) with an input signal of 2.5mW (4dBm) (pin16). The current drain would typically be 200mA while operating in the frequency range of 806-870MHz.

The 85Y73 LDMOS PA is capable of supplying an output power of 4.5W with an input signal of 0.3W. The current drain would typically be 1100mA while operating in the frequency range of 806-870MHz. The power out can be varied by changing the biasing voltage and the drive level from the driver IC.

## 2.2 Antenna Switch

The antenna switch circuit consists of two PIN diodes (CR101 and CR102), a pi network (C109, L103 and C110), and three current limiting resistors (R101, R102, R103). In the transmit mode, B+ at PCIC (U102) pin32 will go high, applying a B+ bias to the antenna switch circuit to bias the diodes “on”. The shunt diode (CR102) shorts out the receiver port, and the pi network, which operates as a quarter wave transmission line, transforms the low impedance of the shunt diode to a high impedance at the input of the harmonic filter. In the receive mode, the diodes are both off, and hence, there exists a low attenuation path between the antenna and receiver ports.

## 2.3 Harmonic Filter

The harmonic filter consists of C104, L102, C105, C106,C107, L101 and C109. It has been optimized for efficiency of the power amplifier. This type of filter has the advantage that it can give a greater attenuation in the stop-band for a given ripple level. The harmonic filter insertion loss is typically less than 1.2dB.

## 2.4 Antenna Matching Network

The antenna matching network is made up of inductor L116. This component matches the antenna impedance to the harmonic filter to optimize the performance of the transmitter and receiver.

## 2.5 Power Control Integrated Circuit (PCIC)

The transmitter uses the Power Control IC (PCIC), U102 to regulate the power output of the radio. The current to the final stage of the power module is supplied through R104, which provides a voltage proportional to the current drain. This voltage is then fed back to the Automatic Level Control (ALC) within the PCIC to regulate the output power of the transmitter.

The PCIC has internal digital to analog converters (DACs) which provide the reference voltage of the control loop. The reference voltage level is programmable through the SPI line of the PCIC.

There are resistors and integrators within the PCIC, and external capacitors (C126, C130 and C132) in controlling the transmitter rising and falling time. These are necessary in reducing the power splatter into adjacent channels.

U103 and its associated components are part of the temperature cut back circuitry. It senses the printed circuit board temperature around the transmitter circuits and provides a DC voltage to the PCIC. If the DC voltage produced exceeds the set threshold in the PCIC, the transmitter output power will be reduced so as to reduce the transmitter temperature.

# 3.0 800 MHz Receiver

The receiver functions are shown in Figure 2-20 and are described in the paragraphs that follow.

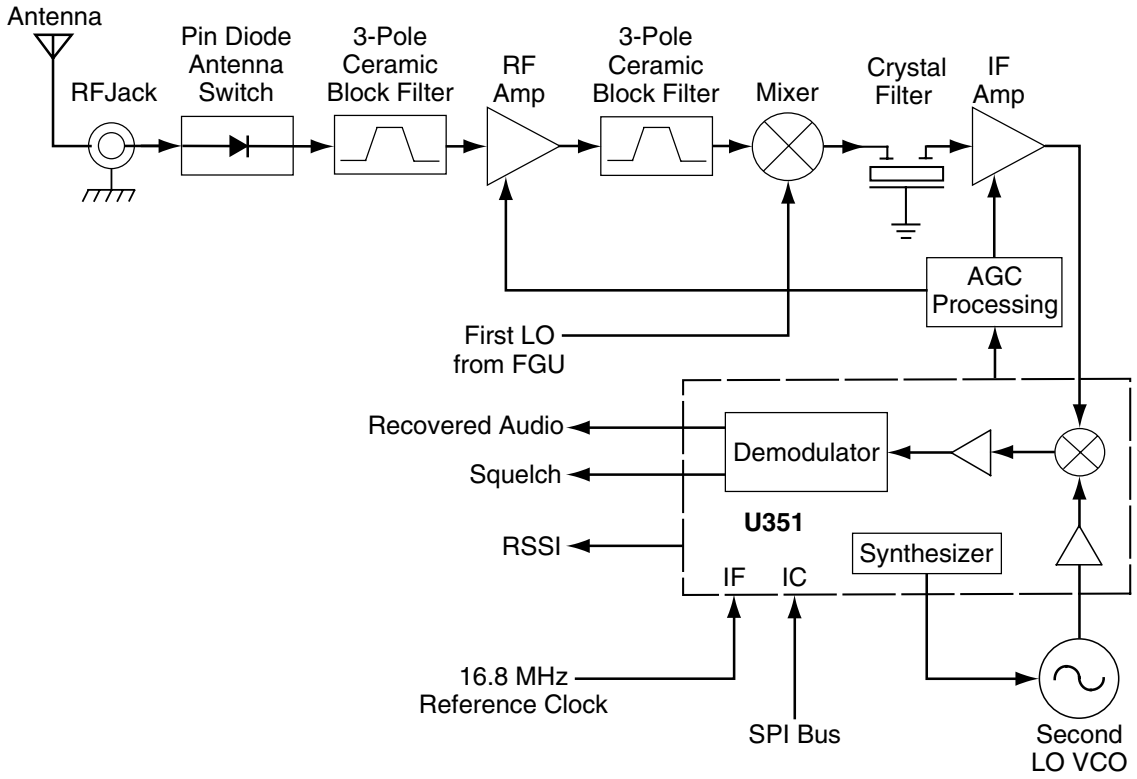



**Figure 2-2** 800 MHz Receiver Block Diagram.

## 3.1 Receiver Front-End

(*Refer to Figure 2-2 and the UHF Receiver Front End schematic diagram)*

The RF signal is received by the antenna and applied to a low-pass filter. For 800MHz, the filter consists of L101, L102, C104, C105, C106, C107, C109. The filtered RF signal is passed through the antenna switch. The antenna switch circuit consists of two PIN diodes(CR101 and CR102) and a pi network (C109, L103 and C110).The signal is then applied to a fixed tuned ceramic bandpass filter, FL300.

The output of the bandpass filter is coupled to the RF amplifier transistor Q302 via C300. The RF amplifier provides a gain of approximately 12 dB. After being amplified by the RF amplifier, the RF signal is further filtered by a second fixed tuned ceramic bandpass filter, FL301.

Both the pre and post-RF amplifier ceramic filters have similar responses. The insertion loss of each filter across the 851-870MHz band is typically 1.8dB.

The output of the post-RF amplifier filter is connected to the passive double balanced mixer, U301. After mixing with the first LO signal from the voltage controlled oscillator (VCO) using low side injection, the RF signal is down-converted to the 109.65MHz IF signal.

The IF signal coming out of the mixer is transferred to the crystal filter (FL350) through a resistive pad and a diplexer (C312 and L306). Matching to the input of the crystal filter is provided by L353,L354, C377, and C378. The crystal filter provides the necessary selectivity and intermodulation protection.

## 3.2 Receiver Back-End

(*Refer to Figure 2-2 and the 800 MHz Receiver Back End schematic diagram*)

The output of crystal filter FL350 is matched to the input of the dual gate MOSFET IF amplifier transistor U352 by components L355, R359 and C376. Voltage supply to the IF amplifier is taken from the receive 5 volts (R5). AGC voltage is applied to the second gate of U352. The IF amplifier provides a gain of about 11 dB. The amplified IF signal is then coupled into U351(pin 3) via L352, R356 and C365 which provides the matching for the IF amplifier and U351.

The IF signal applied to pin 3 of U351 is amplified, down-converted, filtered, and demodulated, to produce the recovered audio at pin 27 of U351. This IF IC is electronically programmable, and the amount of filtering (which is dependent on the radio channel spacing) is controlled by the microprocessor. Additional filtering, once externally provided by the conventional ceramic filters, is replaced by internal filters in the IF module (U351).

The IF IC uses a type of direct conversion process, whereby the externally generated second LO frequency is divided by two in U351 so that it is very close to the first IF frequency. The IF IC (U351) synthesizes the second LO and phase-locks the VCO to track the first IF frequency. The second LO is designed to oscillate at twice the first IF frequency because of the divide-by-two function in the IF IC.

In the absence of an IF signal, the VCO will “search” for a frequency, or its frequency will vary close to twice the IF frequency. When an IF signal is received, the VCO will lock onto the IF signal. The second LO/VCO is a Colpitts oscillator built around transistor Q350. The VCO has a varactor diode, CR350, to adjust the VCO frequency. The control signal for the varactor is derived from a loop filter consisting of R365, C391, and C392.

The IF IC (U351) also performs several other functions. It provides a received signal-strength indicator (RSSI) and a squelch output. The RSSI is a dc voltage monitored by the microprocessor, and used to control the automatic gain control (AGC) circuit in both the front-end and the IF.

The demodulated signal on pin 27 of U351 is also used for squelch control. The signal is routed to U404 (ASFIC) where squelch signal shaping and detection takes place. The demodulated audio signal is also routed to U404 for processing before going to the audio amplifier for amplification.

## 3.3 Automatic Gain Control (AGC)

(*Refer to the 800 MHz Receiver Front End and Receiver Back End schematic diagrams*)

The automatic gain control circuit provides automatic gain reduction of both the low noise amplifier in the receiver front end and the IF amplifier in the receiver backend. This action is necessary to prevent overloading of the backend IF IC.

The IF automatic gain control circuit provides approximately 50 dB of attenuation range. The signal strength indicator (RSSI) output of the IF IC produces a voltage that is proportional to the RF level at the IF input to the IF IC. This voltage is inverted by U350, R351, R353, R352, R354 and C355 and it determines the RF level at which the backend end AGC is activated as well as the slope of the voltage at the output of U350 vs. the strength of the incoming RF at the antenna. The inverted output of U350 is applied to the second gate of the IF amplifier U352 via R355. As the RF signal into the IF IC increases the following occurs:

- the RSSI voltage increases,
- the output of inverter U350 decreases, and
- the voltage applied to the second gate of the FET is reduced thus reducing the gain of the IF amplifier.

The output of inverter U350 is also used to control the receiver front end AGC.

The receiver front end automatic gain control circuit provides and additional 20 dB of gain reduction. The output of the receiver backend inverter U350 is fed into the receiver front end AGC inverter U302. The components R317, R314, and C318 determine:

- the RF level at which the front end AGC is activated, and
- the slope of the voltage at the output of U302 vs. the strength of the incoming RF at the antenna.

As the RF into the antenna increases the following occurs:

- The output voltage of the receiver backend inverter U350 decreases.
- The voltage at the output of the front end inverter U302 increases.
- The result is the forward biasing of pin diode CR301.

As the diode becomes more and more forward biased the following occurs:

- C310 loads the output of the low noise amplifier Q302 thus reducing the gain of the low noise amplifier.
- R315 and R318 provide a DC path for CR301 and also limit the current through CR301.

The blocking capacitor C317 prevents DC from the AGC stage from appearing at the input of the filter FL301.

# 4.0 Frequency Generation Circuit

(*Refer to Figure 2-3 and the 800 MHz Frequency Synthesizer schematic diagram*)

The frequency generation circuit is shown in Figure 2-21. The circuit is composed of the two main ICs:

- Fractional-N synthesizer, U201
- VCO/Buffer IC, U250

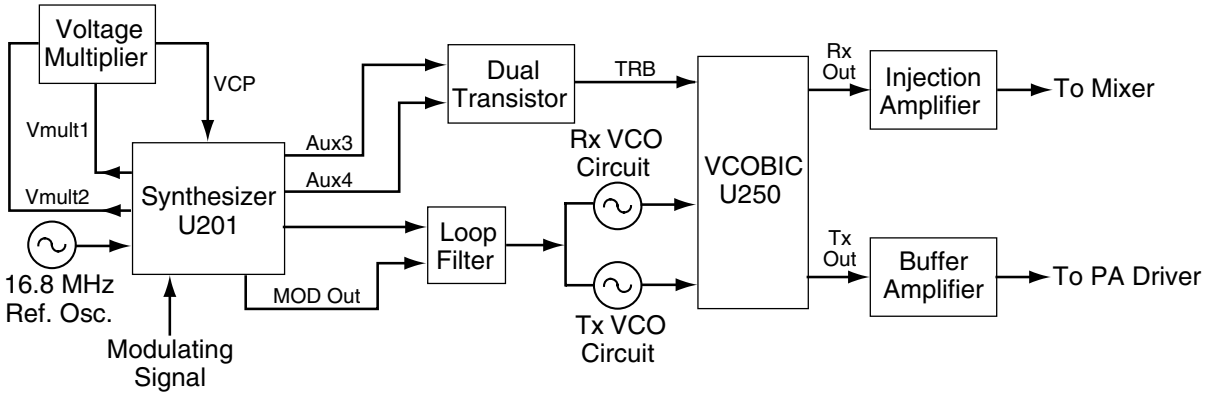



**Figure 2-3** 800 MHz Frequency Generation Unit Block Diagram

Designed in conjunction to maximize compatibility, the two ICs provide many of the functions that normally would require additional circuitry. The synthesizer block diagram illustrates the interconnect and support circuitry used in the region. Refer to the relevant schematics for the reference designators.

The synthesizer is powered by regulated 5V and 3.3V which come from U247 and U248 respectively. The synthesizer in turn generates a superfiltered 4.5V which powers U250.

In addition to the VCO, the synthesizer must interface with the logic and ASFIC circuitry. Programming for the synthesizer is accomplished through the data, clock and chip select lines from the microprocessor. A 3.3V dc signal from synthesizer lock detect line indicates to the microprocessor that the synthesizer is locked.

Transmit modulation from the ASFIC is supplied to pin10 of U201. Internally the audio is digitized by the Fractional-N and applied to the loop divider to provide the low-port modulation. The audio runs through an internal attenuator for modulation balancing purposes before going out to the VCO.

## 4.1 Synthesizer

(*Refer to Figure 2-4 and the 800 MHz Synthesizer schematic diagram)*

The Fractional-N Synthesizer uses a 16.8MHz crystal (FL201) to provide a reference for the system. The LVFractN IC (U201) further divides this to 2.1MHz, 2.225MHz, and 2.4MHz as reference frequencies. Together with C235, C236, C237, R211 and CR203, they comprise the reference oscillator which is capable of 2.5ppm stability over temperatures of -30 to 85°C. It also provides 16.8MHz at pin 19 of U201 to be used by ASFIC and LVZIF.

Some models are equipped with a packaged 1.5ppm reference oscillator, Y200. On these models components C235, C236, C237, CR203, FL201, and R211 are not placed. Components C238, C239, C241, R212, R213, R214 and Y200 are placed instead.

The loop filter which consists of C220, C225, C226, R204, R209 and R210 provides the necessary dc steering voltage for the VCO and provides filtering of noise and spurs from U201.

In achieving fast locking for the synthesizer, an internal adapt charge pump provides higher current at pin 45 of U201 to put the synthesizer within the lock range. The required frequency is then locked by the normal mode charge pump at pin 43.

Both the normal and adapt charge pumps get their supply from the capacitive multiplier which is made up of D201, D202, C244, C245, C246, C247, R200, R218, C208, C243, R219, and R220. Two 3.3 V square waves (180 degrees out of phase) are applied to R219 and R220. These square waves switch alternate sets of diodes from D201 and D202, which in turn charge C244, C245, C246, and C247 in a bucket brigade fashion. The resulting output voltage that is applied to pin 47 of U201 is typically 12.8V and allows the steering line voltage (VCO control voltage) to reach 11V.

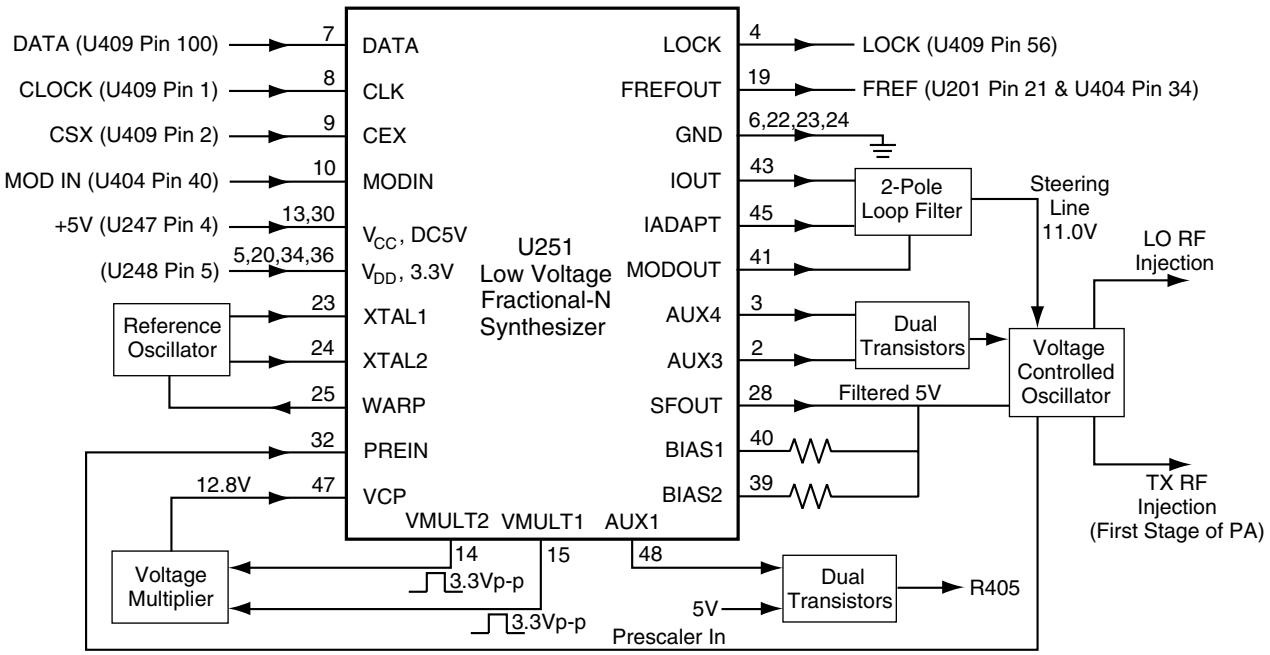



**Figure 2-4** 800 MHz Synthesizer Block Diagram

## 4.2 Voltage Controlled Oscillator (VCO)

(*Refer to Figure 2-5 and the 800 MHz Voltage Controlled Oscillator schematic diagram)*

The VCOBIC (U250) in conjunction with the Fractional-N synthesizer (U201) generates RF in both the receive and the transmit modes of operation. The TRB line (U250 pin 19) determines which oscillator and buffer will be enabled. A sample of the RF signal from the enabled oscillator is routed from U250 pin 12, through a low pass filter, to the prescaler input (U201 pin 32). After frequency comparison in the synthesizer, a resultant CONTROL VOLTAGE is received at the VCO. This voltage is a DC voltage between 2.0V (low frequency) and 11.0V (high frequency) when the PLL is locked on frequency.

The VCOBIC(U250) is operated at 4.54 V (VSF) and Fractional-N synthesizer (U201) at 3.3V. This difference in operating voltage requires a level shifter consisting of Q200 and Q252 on the TRB line.

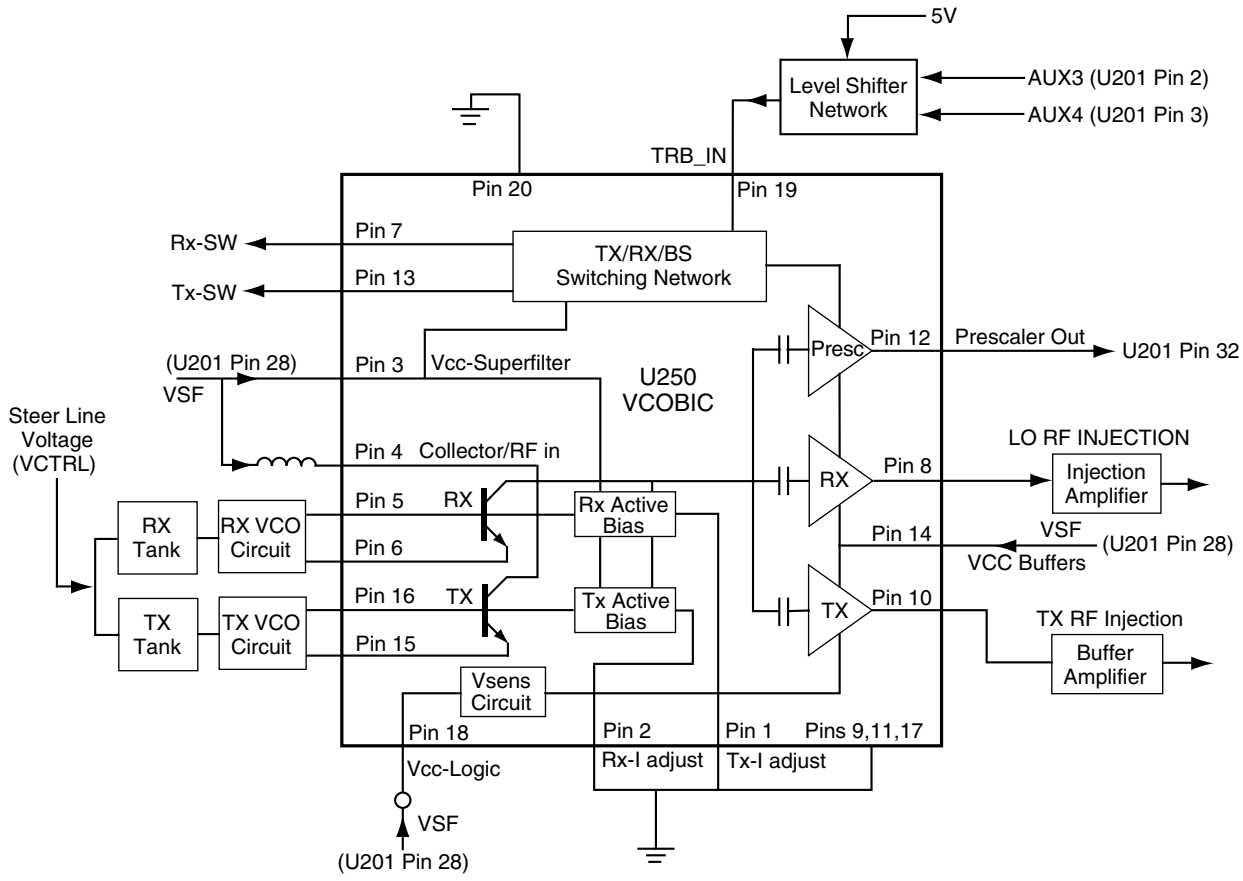



**Figure 2-5** UHF VCO Block Diagram

The operation logic is shown in Table 2-1.

| Desired Mode | AUX 4 | AUX 3 | TRB |
|---|---|---|---|
| Tx | Low | High (@3.2V) | High (@4.8V) |
| Rx | High | Low | Low |
| Battery Saver | Low | Low | Hi-Z/Float (@2.5V) |

*Table 2-1: Level Shifter Logic*

In the receive mode, U250 pin 19 is low or grounded. This activates the receive VCO by enabling the receive oscillator and the receive buffer of U250. The RF signal at U250 pin 8 is run through an injection amplifier, Q304. The resulting RF signal is the LO RF INJECTION and it is applied to the mixer at U301 (refer to Figure 4-88: 800MHz Receiver Front End Schematic Diagram).

During the transmit condition, when PTT is depressed, five volts is applied to U250 pin 19. This activates the transmit VCO by enabling the transmit oscillator and the transmit buffer of U250. The RF signal at U250 pin 10 is amplified by Q251 and injected into the input of the PA module (U101 pin1). This RF signal is the TX RF INJECTION. Also in transmit mode, the audio signal to be frequency modulated onto the carrier is received through the U201 pin 41.

When a high impedance is applied to U250 pin19, the VCO is operating in BATTERY SAVER mode. In this case, both the receive and transmit oscillators as well as the receive transmit and prescaler buffer are turned off.

## 4.3 Trunked Radio Systems

Trunked systems allow a large number of users to share a relatively small number of frequencies or repeaters without interfering with each other. The airtime of all the repeaters in a trunked system is pooled, which maximizes the amount of airtime available to any one radio and minimizes channel congestion. A benefit of trunking is that the user is not required to monitor the system before transmitting.

### 4.3.1 Privacy Plus Trunked Systems

Privacy Plus is a proprietary trunking protocol developed by Motorola which allows a large number of users to share small amounts of frequencies without interfering with each other. The Privacy Plus configuration consists of shared multiple channel repeaters. The Privacy Plus Trunked system includes a Central Controller, which directs the users to the open channels. This kind of Trunked system requires no monitoring of the channel as in conventional systems. The Central Controller places the user in a queue to wait for a free channel. The Central Controller does the monitoring and channels selection for the user.

### 4.3.2 LTR™ Trunked Systems

LTR is a transmission based trunking protocol developed by the E. F. Johnson Company for primarily single site trunking applications. In transmission trunking, a repeater is used for only the duration of a single transmission. Once a transmission is completed, that repeater becomes available to other users.

### 4.3.3 MPT Trunked Systems

MPT (Ministry of Post and Telecommunications) developed a signalling standard (MPT1327) for trunked private land mobile radio systems. This standard defines the protocol rules for communication between a trunking system controller (TSC) and user's radio units. The protocol offers a broad range of options which can be implemented in subsets according to user requirements. Also, there is scope for customization for special requirements, and provision made to further standardized features to be added to the protocol in the future. The standard defines only the over-air signalling and imposes only minimum constraints on system design.

### 4.3.4 PassPort™ Trunked Systems

PassPort is an enhanced trunking protocol developed by Trident Microsystems that supports wide area dispatch networking. A network is formed by linking several trunked sites together to form a single system. This offers users an extended communication coverage area. Additionally, users with PassPort can seamlessly roam among all sites within the network. Seamless roaming means that the radio user does not have to manually change the position on the radio when roaming from site-to-site.

For models which feature PassPort Trunking operation, the standard keypad board is replaced with the PassPort Trunking Controller Board (PTCB). This board also provides advanced voice storage features. Refer to Figure 2-2 for connector and signal routing from, to and through the Radio, PTCB and Liquid Crystal Display (LCD) sub-systems.

#### *Power Supplies*

The radio supplies regulated Vdd of 3.3 VDC. This is used to power the Low Speed Data Filter and Voice Storage circuits. The radio also supplies Switched Battery Voltage (SWB+). U612 regulates the SWB+ to 3.3V which is applied to the PTCB microcontroller U601. A filtered voltage (Vdda) of _ Vdd is developed by U603-4 and is used to supply a clean reference bias for the Low Speed Data filter and Voice Storage circuits. The circuit of Q607 which can limit the voltage applied to the Voice Storage chip is not used in portable applications and is disabled by 0 Ohm resistor R614.

#### *Microcontroller (MCU)*

PassPort Trunking operation is managed by the reprogrammable FLASH ROM based microcontroller (U601). The MCU clock oscillator uses 8MHz crystal Y601 as a stable resonator. The PTCB communicates with the main radio microcontroller by attaching to the same Serial Peripheral (SPI) bus that passes though the PTCB to the LCD on the CLK, DATA, RDY, and MISO lines. The OPT_EN line is strobed low only for communications with U601.

The MCU includes an on-chip Analog to Digital Converter (ADC). The received and filtered sub-audible low speed trunking data waveform is applied to one of the ADC inputs. The software in the MCU decodes and acts upon the trunking data.

The MCU includes a Digital to Analog Converter (DAC). As required, the MCU software generates appropriate PassPort Low Speed Trunking Data waveforms. These are applied to the Low Speed Data Filter and then to the radio transmitter modulation point. The amplitude of this waveform and the resulting transmitted deviation is controlled by software.

#### *Low Speed Data Filter*

This analog circuitry is a 4 pole, 150 Hz cutoff low pass filter comprised of U603-1, U603-2 and associated passive components. In receive mode, it removes noise and voice band signals leaving

only the low speed data waveform which is applied to the ADC input of the MCU. U608-4 isolates the receive signal from the filter in transmit mode. When the radio is transmitting PassPort data, the MCU DAC low speed data waveform is applied to the input of the filter which removes harmonics that would interfere with voice and applies the resulting sub-audible data to the radio transmitter modulation point.

### *Keyboard Circuit*

The keyboard consists of a matrix of key switches and resistors as described in section 2.3. U605-2 monitors the column voltage and applies an interrupt signal to the radio microcontroller when any key is pressed.

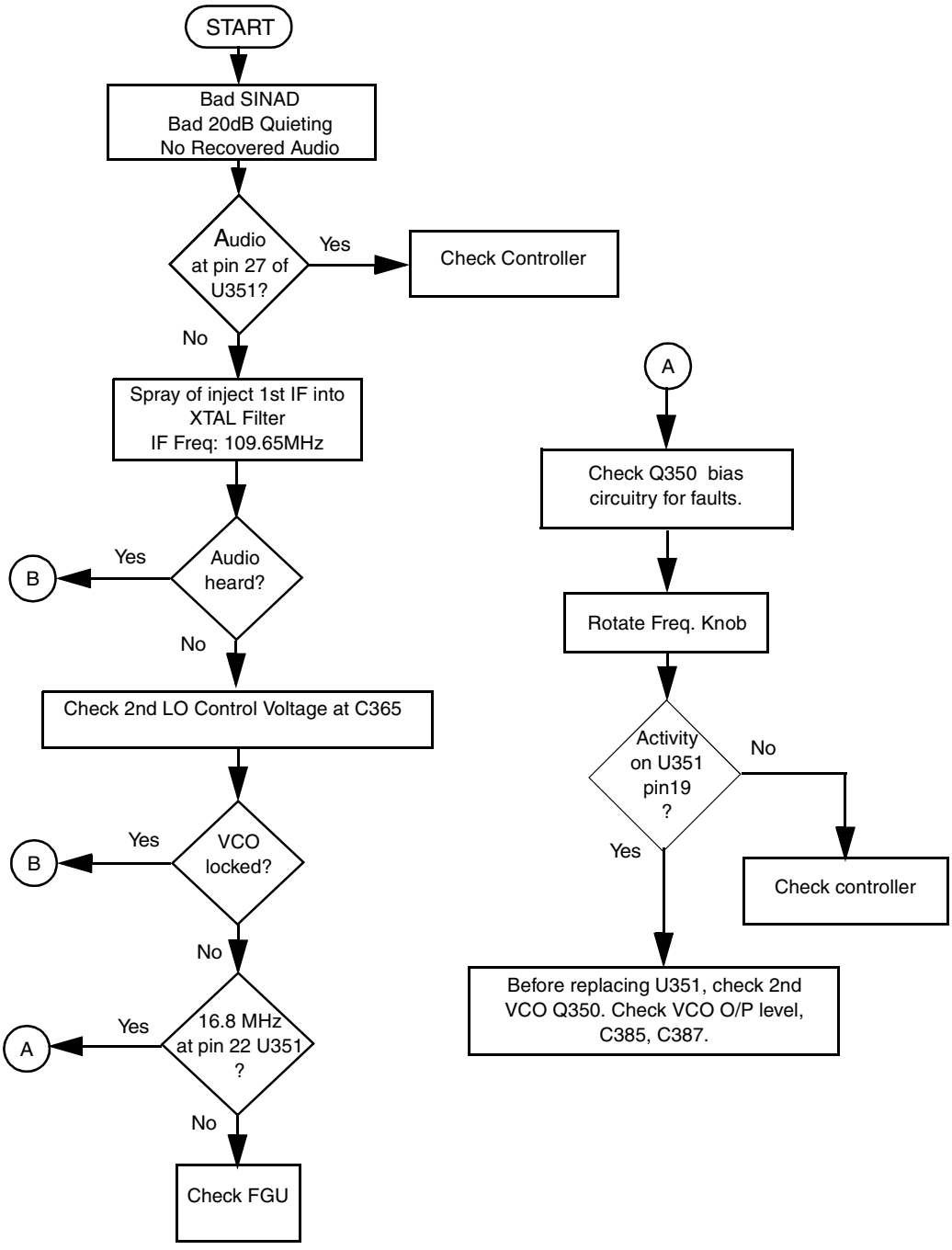
### *BackLight Driver and LED's*

The logic level signal from the radio microcontroller is translated via Q611 and applied to Q610 which uses Switched Battery Voltage (SWB+) to operate the keypad backlight LED’s.

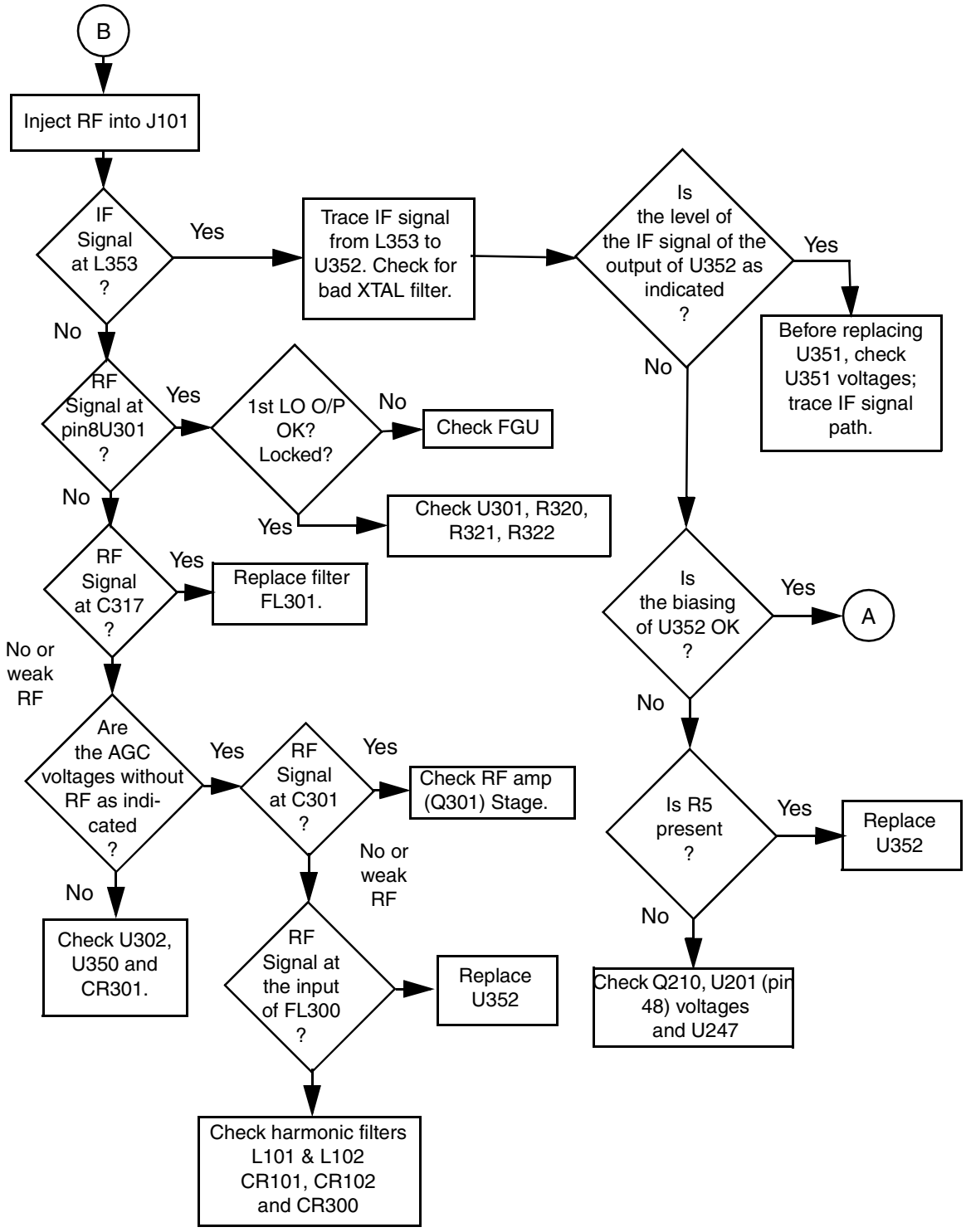
# Chapter 3

# TROUBLESHOOTING CHARTS

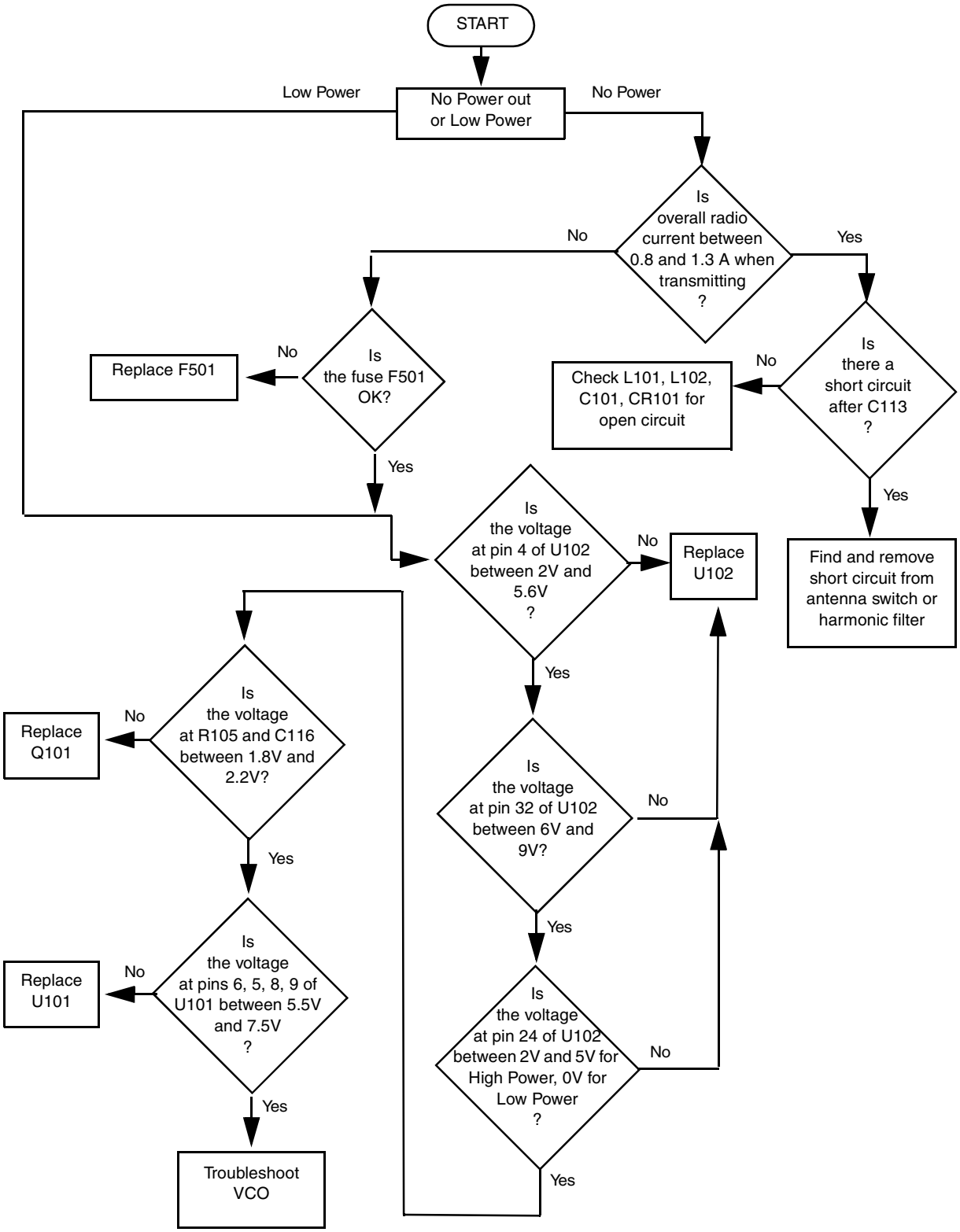
## 1.0 Troubleshooting Flow Chart for Receiver (Sheet 1 of 2)



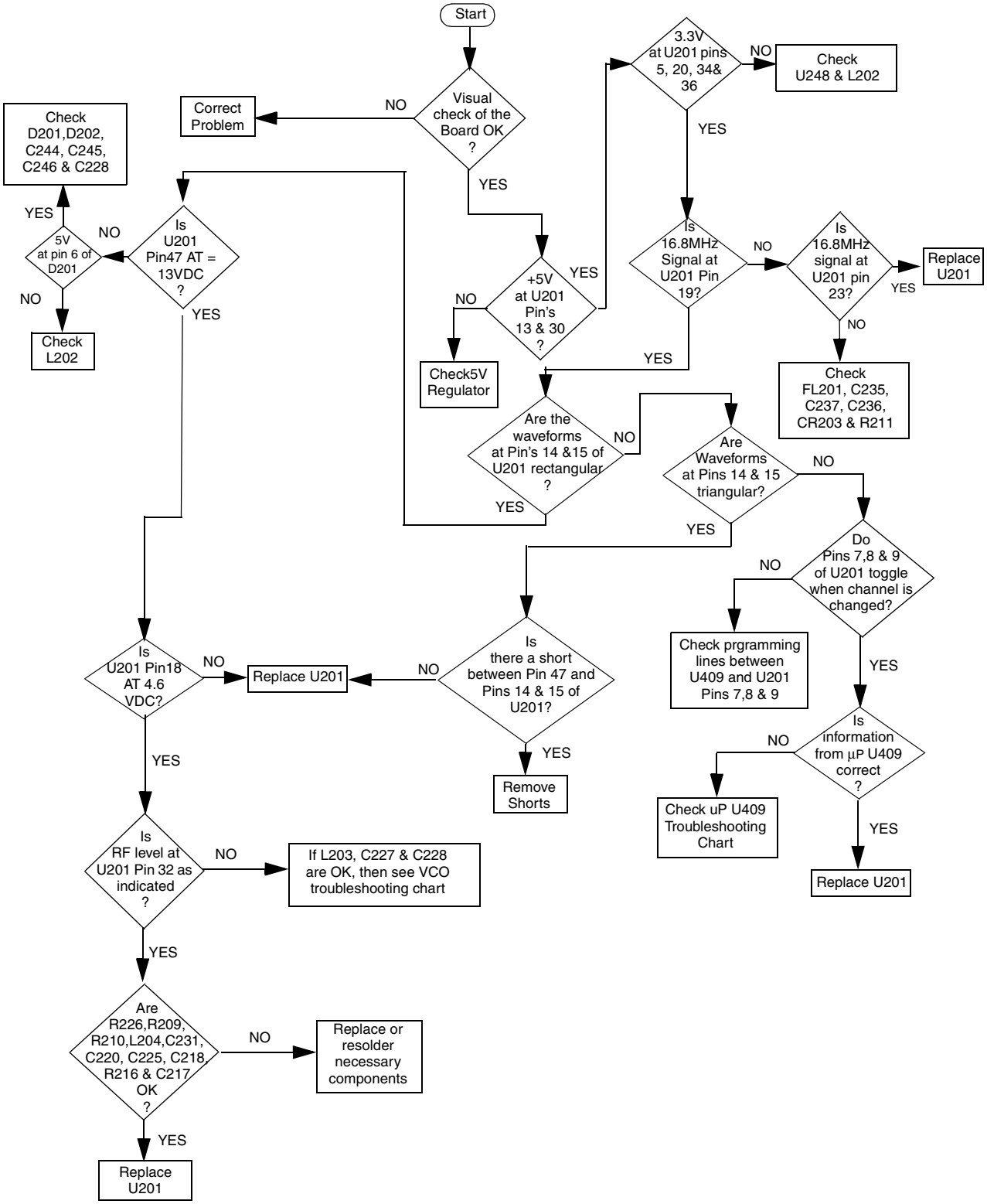
## 2.0 Troubleshooting Flow Chart for Receiver (Sheet 2 of 2)



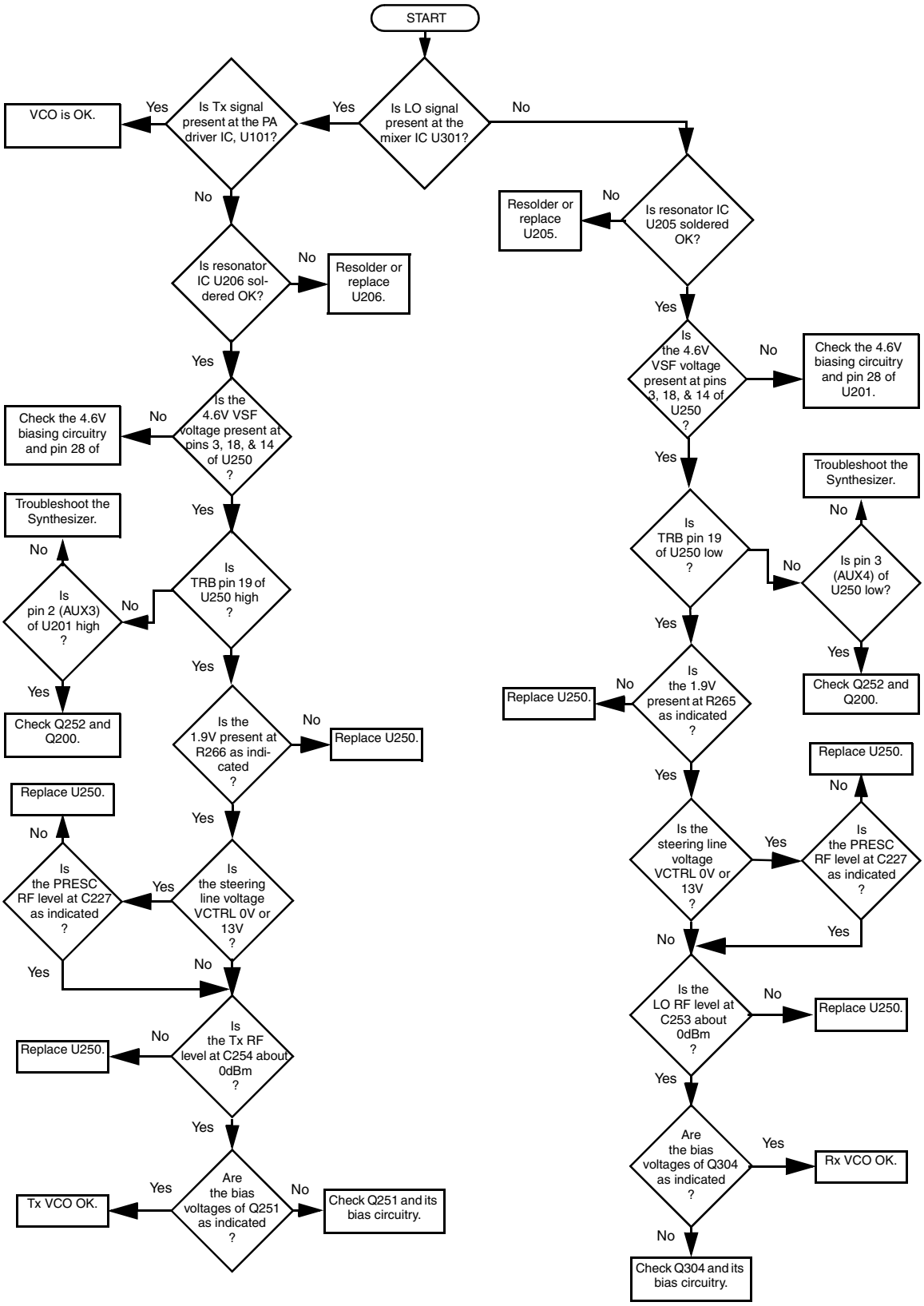
# 3.0 Troubleshooting Flow Chart for Transmitter



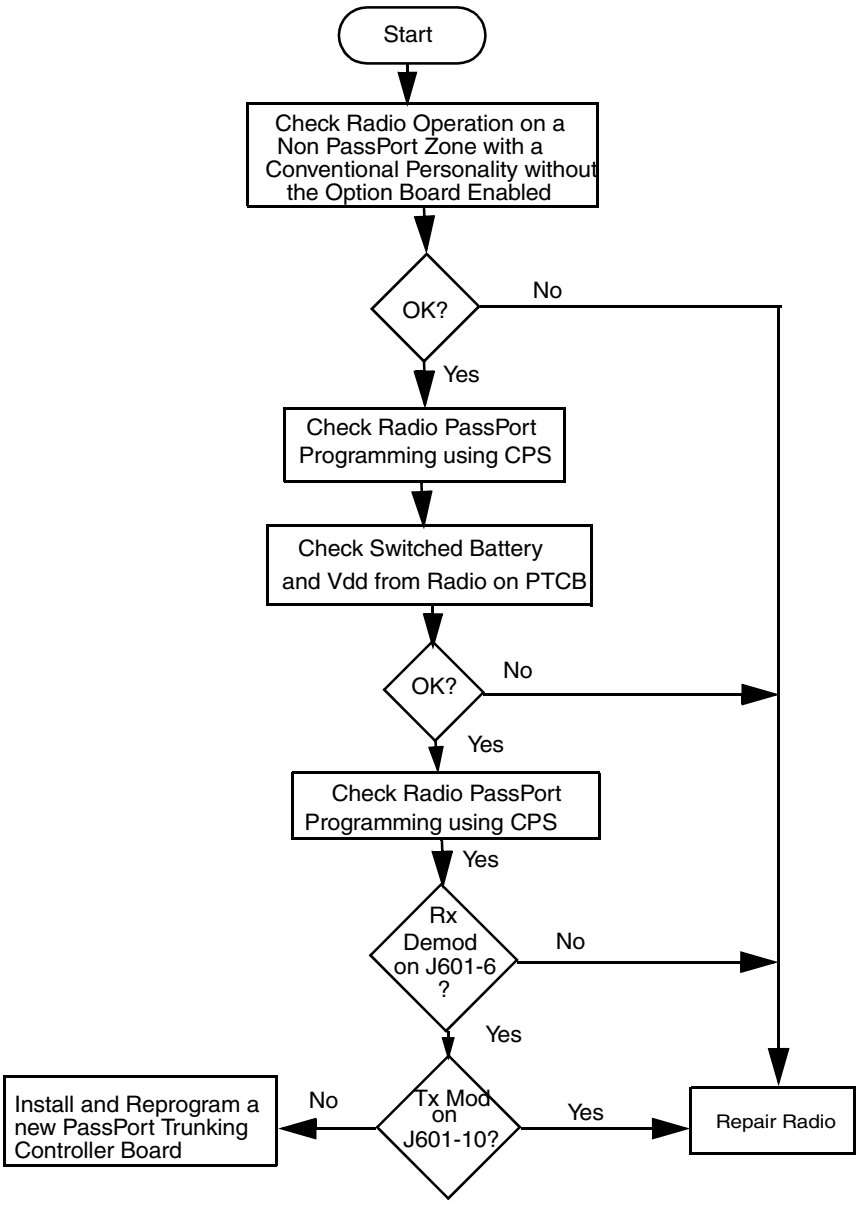
# 4.0 Troubleshooting Flow Chart for Synthesizer



# 5.0 Troubleshooting Flow Chart for VCO



# 6.0 Troubleshooting Flow Chart for PassPort Trunking



# Chapter 4

# 800 MHZ /PCB/SCHEMATICS/PARTS LIST

## 1.0 Allocation of Schematics and Circuit Boards

### 1.1 Controller Circuits

The 800 MHz circuits are contained on the printed circuit board (PCB) which also contains the Controller circuits. This chapter shows the schematics for the 800 MHz circuits only, refer to the Controller section for details of the related Controller circuits.The PCB component layouts and the Parts Lists in this Chapter show both the Controller and UHF circuit components. The 800 MHz schematics and the related PCB and parts list are shown in the tables below.

**Table 4-1** 800 MHz Diagrams and Parts Lists