Technical Manual

iDEN

Enhanced Base Tranceiver System (EBTS)

Volume 2 of 3
Base Radios

68P80801E35-C

09/23/02

MOTOROLA
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RF SUB-SYSTEM

REV 062802

Contact Information

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SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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Base Radios

About This Volume

Volume 2 of the Enhanced Base Transceiver System (EBTS) manual, *Base Radios*, provides the experienced service technician with an overview of the EBTS operation and functions, and contains information regarding the 800 MHz, 900 MHz, 1500 MHz Single Channel and 800 MHz and 900 MHz QUAD Channel Channel base radios.

The EBTS System has three major components:

❐ Generation 3 Site Controller (Gen 3 SC) or an integrated Site Controller (iSC)

❐ Base Radios (BRs)

❐ RF Distribution System (RFDS)

Installation and testing is described in Volume 1, *System Installation and Testing*, and RFDS are described in Volume 3, *RF Distribution Systems (RFDS)*. Detailed information about the Gen 3 SC is contained in the *Gen 3 SC Supplement Manual, 68P80801E30*. Detailed information about the iSC is contained in the *iSC Supplement Manual*, *68P81098E05*

The information in this manual is current as of the printing date. If changes to this manual occur after the printing date, they will be documented and issued as Schaumburg Manual Revisions (SMRs).

Target Audience

The target audience of this document includes field service technicians responsible for installing, maintaining, and troubleshooting the EBTS.

In keeping with Motorola's field replaceable unit (FRU) philosophy, this manual provides sufficient functional information to the FRU level. Please refer to the appropriate section of this manual for removal and replacement instructions.

Maintenance Philosophy

The EBTS has been designed using a Field Replaceable Unit (FRU) maintenance concept. To minimize system down time, faulty FRUs may be quickly and easily replaced with replacement FRUs. This helps to restore normal system operation quickly.

Due to the high percentage of surface mount components and multi-layer circuit boards, field repair is discouraged. Faulty or suspect FRUs should be returned to the Motorola Customer Support Center for further troubleshooting and repair.

Each FRU has a bar code label attached to its front panel. This label identifies a sequential serial number for the FRU. Log this number whenever contacting the Motorola Customer Support Center. For complete information on ordering replacement FRUs, or instructions on how to return faulty FRUs for repair, contact:

Nippon Motorola LTD.	**OR**	**Motorola Customer Support Center**
Tokyo Service Center		**1311 East Algonquin Road**
044-366-8860		**Schaumburg, Illinois 60196**
		(800) 448-3245 or (847) 576-7300

Technical Support Service

Motorola provides technical support services for installation, optimization, and maintenance of its fixed network equipment. Before calling the Motorola Customer Support Center, please note the following information:

- ❐ Where the system is located.
- ❐ The date the system was put into service.
- ❐ A brief description of problem.
- ❐ Any other unusual circumstances.

General Safety Information

The following general safety precautions must be observed during all phases of operation, service, and repair of the equipment described in this manual. The safety precautions listed below represent warnings of certain dangers of which we are aware. You should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Read and follow all warning notices and instructions marked on the product or included in this manual before installing, servicing or operating the equipment. Retain these safety instructions for future reference. Also, all applicable safety procedures, such as Occupational, Safety, and Health Administration (OSHA) requirements, National Electrical Code (NEC) requirements, local code requirements, safe working practices, and good judgement must be used by personnel.

Refer to appropriate section of the product service manual for additional pertinent safety information.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modifications of equipment.

Identify maintenance actions that require two people to perform the repair. Two people are required when:

- ✓A repair has the risk of injury that would require one person to perform first aid or call for emergency support. An example would be work around high voltage sources. A second person may be required to remove power and call for emergency aid if an accident occurs to the first person.
- ✓Use the National Institute of Occupational Safety and Health (NIOSH) listing equation to determine whether a one or two person lift is required when a system component must be removed and replaced in its rack.

If troubleshooting the equipment while power is applied, be aware of the live circuits.

DO NOT operate the transmitter of any radio unless all RF connectors are secure and all connectors are properly terminated.

All equipment must be properly grounded in accordance with *Motorola Standards and Guidelines for Communication Sites* "*R56*" (6881089E50) and specified installation instructions for safe operation.

Slots and openings in the cabinet are provided for ventilation. To ensure reliable operation of the product and protect it from overheating, these slots and openings must not be blocked or covered.

Only a qualified technician familiar with similar electronic equipment should service equipment.

Some equipment components can become extremely hot during operation. Turn off all power to the equipment and wait until sufficiently cool before touching.

Human Exposure Compliance

This equipment is designed to generate and radiate radio frequency (RF) energy by means of an external antenna. When terminated into a non-radiating RF load, the base station equipment is certified to comply with Federal Communications Commission (FCC) regulations pertaining to human exposure to RF radiation in accordance with the FCC Rules Part 1 section 1.1310 as published in title 47 code of federal regulations and procedures established in TIA/EIA TSB92, Report on EME Evaluation for RF Cabinet Emissions Under FCC MPE Guidelines, Compliance to FCC regulations of the final installation should be assessed and take into account site specific characteristics such as type and location of antennas, as well as site accessibility of occupational personnel (controlled environment) and the general public (uncontrolled environment). This equipment should only be installed and maintained by trained technicians. Licensees of the FCC using this equipment are responsible for insuring that its installation and operation comply with FCC regulations Part 1 section 1.1310 as published in title 47 code of federal regulations.

Whether a given installation meets FCC limits for human exposure to radio frequency radiation may depend not only on this equipment but also on whether the "environments" being assessed are being affected by radio frequency fields from other equipment, the effects of which may add to the level of exposure. Accordingly, the overall exposure may be affected by radio frequency generating facilities that exist at the time of the licensee's equipment is being installed or even by equipment installed later. Therefore, the effects of any such facilities must be considered in site selection and in determining whether a particular installation meets the FCC requirements.

FCC OET Bulletin 65 provides materials to assist in making determinations if a given facility is compliant with the human exposure to RF radiation limits. Determining the compliance of transmitter sites of various complexities may be accomplished by means of computational methods. For more complex sites direct measurement of power density may be more expedient. Additional information on the topic of electromagnetic exposure is contained in the *Motorola Standards and Guideline for Communications Sites* publication. Persons responsible for installation of this equipment are urged to consult the listed reference material to assist in determining whether a given installation complies with the applicable limits.

In general the following guidelines should be observed when working in or around radio transmitter sites:

- All personnel should have electromagnetic energy awareness training.
- All personnel entering the site must be authorized.
- Obey all posted signs
- Assume all antennas are active
- Before working on antennas, notify owners and disable appropriate transmitters.
- Maintain minimum 3 feet clearance from all antennas.
- Do not stop in front of antennas.
- Use personal RF monitors while working near antennas.
- Never operate transmitters without shields during normal operation.
- Do not operate base station antennas in equipment rooms

For installations outside of the U.S., consult with the applicable governing body and standards for RF energy human exposure requirements and take necessary steps for compliance with local regulations.

References:

TIA/EIA TSB92 “Report on EME Evaluation for RF Cabinet Emissions Under FCC MPE Guidelines”, Global Engineering Documents: http://globl.ihs.com/

FCC OET Bulletin 65 “Evaluating Compliance with FCC Guidelines for Human Exposure to Radiofrequency Electromagnetic Fields”; http://www.fcc.gov/oet/rfsaftey/.

Motorola Standards and Guideline for Communications Sites, Motorola manual 68P81089E50.

IEEE Recommended Practice for the Measure of Potentially Hazardous Electromagnetic Fields-- RF and Microwave, IEEE Std. C95.3-1991, Publication Sales, 445 Hoes Lane, P.O. Box 1331, Piscattaway, NJ 08855-1331

IEEE Standard for Safety Levels with Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz, IEEE C95.1-1991,

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Base Radio

Overview

This chapter provides an overview of the 800 MHz Legacy, 800 MHz Generation 2 Single Channel, 800 MHz and 900 MHz QUAD Channel Base Radios (BRs) along with technical information. The section topics are listed and described in Table 1.

FRU Number to Kit Number Cross Reference

Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
Single Channel 800 MHz BRC	TLN3334	CLN1469
Single Channel BRC (MCI)	TLN3425	CLN1472
Enhanced Base Radio Controller	DLN6446	CLN1653
900 MHz QUAD Channel BRC	DLN1203	CLF6242
800 MHz QUAD Channel BRC	CLN1497	CLF1560

NOTE

The Single Carrier Base Radio section covers the 800 MHz Legacy and 800 MHz Generation 2 versions of the Base Radio (BR). Information is presented generally for all models. Information that is model specific noted in the text.

NOTE

For Generation 2 BR, both the 800 MHz Exciter and the 800 MHz Low Noise Exciter modules are supported subject to Table 2 on page 4.

NOTE

For QUAD Channel 800 MHz BR use, all Single Carrier BR modules have undergone redesign. Therefore, Single Carrier BR modules are incompatible with the QUAD Channel 800 MHz BR. QUAD Channel 800 MHz BR modules are incompatible with the Single Carrier BR.

Do not attempt to insert QUAD Channel 800 MHz BR modules into a Single Carrier BR or Single Carrier BR modules into a QUAD Channel 800 MHz BR.

NOTE

For QUAD Channel 900 MHz BR use, all Single Carrier BR modules are incompatable with the 900 MHz QUAD Channel BR. 900 MHz QUAD Channel BR modules are incompatable with the Single Carrier BR.

Do not attempt to insert QUAD Channel 900 MHz BR modules into a Single Carrier BR or Single Carrier BR modules into a QUAD Channel 900 MHz BR.

Generation 2 Single Channel 800 MHz Base Radio Overview

The BR provides reliable digital RF communication capabilities in a compact software-controlled design. Increased channel capacity is provided through voice compression techniques and Time Division Multiplexing (TDM).

The BR contains the five FRUs listed below:

- ❐ Enhanced Base Radio Controller (EBRC)
- ❐ Exciter or Low Noise Exciter
- ❐ Power Amplifier
- ❐ Power Supply (DC)
- ❐ Receiver

The modular design of the BR also offers increased shielding and provides easy handling. All FRUs connect to the backplane through blindmate connectors. Figure 1 shows the front view of the BR.

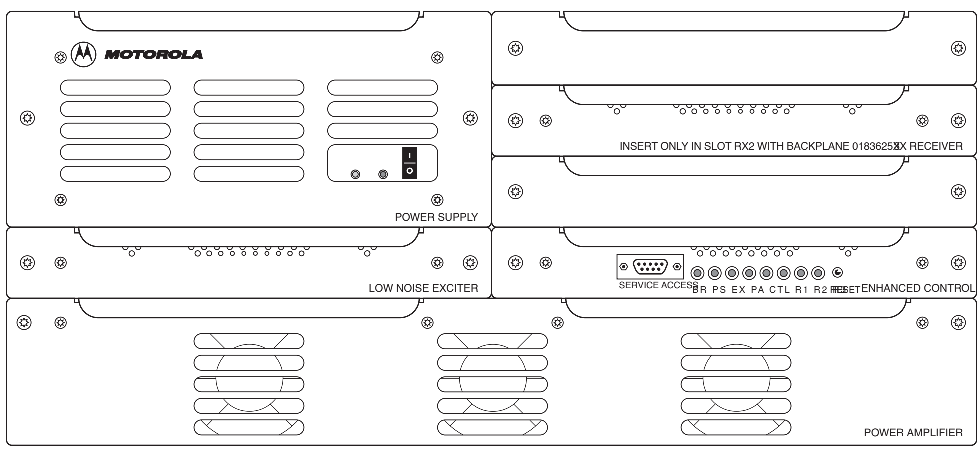


Figure 1 ***Generation 2 Base Radio (Typical)***

Generation 2 Single Channel Radio Controls and Indicators

The Power Supply and EBRC contain controls and indicators that provide a means for monitoring various status and operating conditions of the BR, and also aid in fault isolation. The controls and indicators for both modules are discussed in the Power Supply and EBRC sections of this chapter.

The Power Supply contains two front panel indicators; the EBRC contains eight front panel indicators. The Power Supply contains a power switch used to apply power to the BR. The EBRC contains a RESET switch used to reset the BR.

Generation 2/EBRC Compatibility

Table 2 ***EBRC Compatibility***

Module	Software Revision	System Release
Exciter	***R01.00.xx- R01.03.xx***	SR10.0 or Greater
Exciter	***R01.04.xx*** and higher	SR9.15 or Greater
Single Receiver	R01.00.xx - R01.02.xx	SR10.0 or Greater
Single Receiver	R01.03.xx and higher	SR9.15 or Greater
3X Receiver	all versions	SR9.15 or Greater
40W Power Amplifier	all versions	SR9.15 or Greater
70W Power Amplifier	all versions	SR9.15 or Greater

The Enhanced Base Radio Controller (EBRC) serves as the main controller for the Base Radio. The EBRC provides signal processing and operational control for other Base Radio modules. Figure 1 shows a top view of the EBRC module with the cover removed. The EBRC module consists of two printed circuit boards (EBRC board and LED display board), a slide-in housing, and associated hardware.

- ❐ The EBRC is only compatible with System Software Release SR 9.15 or later. Any system running a pre-SR 9.15 System Release must be updated to at least SR 9.15 prior to installation.
- ❐ The EBRC module is compatible with Legacy Base Radios that support multiple receiver module assemblies.
- ❐ The Generation 2 Base Radio is compatible with all versions of power supplies.

- ❒ The Generation 2 Base Radio is compatible with all 800 MHz 70W and 40W Power Amplifiers.
- ❒ The EBRC module is only compatible with Legacy Exciter (containing revision number R1.04.xx and higher) or the Low Noise Exciter.

Determining FRU and Kit Revisions

For Generation 2 BR/EBRC

These commands will return all available FRU and Kit Revision numbers. Use these to determine installation requirements:

1. Connect one end of the RS-232 cable to the service computer.
2. Connect the other end of the RS-232 cable to the Service Access port, located on the front panel of the EBRC module.
3. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the password **motorola**, log in to the BR.

```
:> login -ufield
password: motorola

field>
```

4. Collect revision numbers from the station by typing the following command:

```
field> fv -oplatform
field>
```

5. If all modules return revision numbers of the format “Rxx.xx.xx”, then all revision numbers are present. In that case, verification requires no further action. If revision numbers return as blank, or not in the format “Rxx.xx.xx”, contact your local Motorola representative or Technical Support.

For Legacy Single Channel BR/BRC

1. Connect one end of the RS-232 cable to the service computer.
2. Connect the other end of the RS-232 cable to the STATUS port, located on the front panel of the BRC.
3. Using the field password, login to the BR.
4. Collect revision numbers from the station by typing the following commands:

```
BRC>dekey
BRC>test_mode
BRC>get brc_rev_no
BRC>get rx1_rev_no
BRC>get rx2_rev_no
BRC>get rx3_rev_no                (if BR is 3 branch)
BRC>get pa_rev_no
BRC>get ex_rev_no

BRC>
```

5. If all modules return revision numbers of the format “Rxx.xx.xx”, then all revision numbers are present and no further action is required. Log out and repeat steps 1 through 4 for each additional BR.

   If revision numbers were returned as blank or not in the format “Rxx.xx.xx”, contact your local Motorola representative or Technical Support.

Generation 2 Single Channel BR General Specifications

General specifications for the Generation 2 BR are listed in Table 2.

Table 3 ***Generation 2 BR General Specifications***

Specification	Value or Range
Dimensions: Height Width Depth	 5 EIA Rack Units (RU) 19" (482.6 mm) 16.75" (425 mm)
Operating Temperature	32˚ to 104˚ F (0˚ to 40˚ C)
Storage Temperature	-22˚ to 140˚ F (-30˚ to 60˚ C)
Rx Frequency Range: 800 MHz iDEN	 806 - 825 MHz
Tx Frequency Range: 800 MHz iDEN	 851 - 870MHz
Tx – Rx Spacing: 800 MHz iDEN	 45 MHz
Channel Spacing	25 kHz
Frequency Generation	Synthesized
Digital Modulation	M-16QAM
Power Supply Inputs: VDC	 -48 VDC (-41 - 60 VDC)
Diversity Branches	Up to 3

Gen 2 Single Channel BR Transmit Specifications

The Generation 2 BR transmit specifications are listed in Table 4.

Table 4 ***Transmit Specifications***

Specification	Value or Range
Average Power Output: (800 MHz) 40 W PA (800 MHz) 70 W PA	 5 - 40 W 5- 70 W
Transmit Bit Error Rate (BER)	0.01%
Occupied Bandwidth	18.5 kHz
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 90): (800 MHz Legacy) 40 W PA (800 MHz Legacy) 70 W PA (800 MHz Low Noise Exciter) 40 W PA (800 MHz Low Noise Exciter) 70 W PA	 ABZ89FC5772 ABZ89FC5763 ABZ89FC5772-A ABZ89FC5763-A
* Stability without site reference connected to station.	

Gen 2 Single Channel BR Receive Specifications

The receive specifications are listed in Table 5.

Table 5 ***Receive Specifications***

Specification	Value or Range
Static Sensitivity †: 800 MHz BR	 -108 dBm (BER = 8%)
BER Floor (BER = 0.01%)	≥ -80 dBm
IF Frequencies 1st IF (All bands): 2nd IF: 800MHz	 73.35 MHz (1st IF) 450 kHz (2nd IF)
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 15): 800 MHz BR	 ABZ89FR5762
† Measurement referenced from single receiver input port of BR. * Stability without site reference connected to station.	

NOTE

FCC Compliance Notice: The Base Radio (BR) is FCC Compliant only when used in conjunction with Motorola supplied RF Distribution Systems. Motorola does not recommend that this BR be used without a Motorola approved RF Distribution System. It is the customer's responsibility to file for FCC approval if the BR is used with a non-Motorola supplied RF Distribution System.

Generation2 Single Channel BR Theory of Operation

The BR operates in conjunction with other site controllers and equipment that are properly terminated. The following description assumes such a configuration. Figures 5 shows an overall block diagram of the BR.

Power is applied to the DC Power input located on the BR backplane. The DC Power input is connected if -48 VDC or batteries are used in the site.

Power is applied to the BR by setting the Power Supply power switch to the ON position. Upon power-up, the BR performs self-diagnostic tests to ensure the integrity of the unit. These tests are primarily confined to the EBRC and include memory and Ethernet verification routines.

After the self-diagnostic tests are complete, the BR reports any alarm conditions present on any of its modules to the site controller via Ethernet. Alarm conditions may also be verified locally using service computer and the STATUS port located on the front of the EBRC.

The software resident in Flash Memory on the EBRC registers the BR with the site controller via Ethernet. Once registered, the BR software is downloaded via resident FLASH- or Ethernet and is executed from RAM. Operating parameters for the BR are included in this download. This software allows the BR to perform call processing functions.

The BR operates in a TDMA (Time Division Multiple Access) mode. This mode, combined with voice compression techniques, provides an increased channel capacity ratio of as much as 6 to 1. Both the receive and transmit signals of the BR are divided into 6 individual time slots. Each receive slot has a corresponding transmit slot; this pair of slots comprises a logical RF channel.

The BR uses diversity reception for increased coverage area and improved quality. The Receiver module within the BR contains up to three receivers. Two Receivers are used with two-branch diversity sites, and three Receivers are used with three-branch diversity sites.

All Receivers within a given BR are programmed to the same receive frequency. The signals from each receiver are fed to the EBRC where a diversity combining algorithm is performed on the signals. The resultant signal is processed for error correction and then sent to the site controller via Ethernet with the appropriate control information regarding its destination.

The transmit section of the BR is comprised of two separate FRUs, the Exciter and Power Amplifier (PA). Several PA FRUs are available, covering different applications and power levels; these are individually discussed as applicable in later subsections.

The Exciter processes the information to transmit from the EBRC in the proper modulation format. This low level signal is sent to the PA where it is amplified to the desired output power level. The PA is a continuous keyed linear amplifier. A power control routine monitors the output power of the BR and adjusts it as necessary to maintain the proper output level.

QUAD Channel 900 MHz Base Radio Overview

The QUAD Channel 900 MHz BR provides reliable, digital BR capabilities in a compact, software-controlled design. Voice compression techniques, time division multiplexing (TDM) and multi-carrier operation provide increased channel capacity.

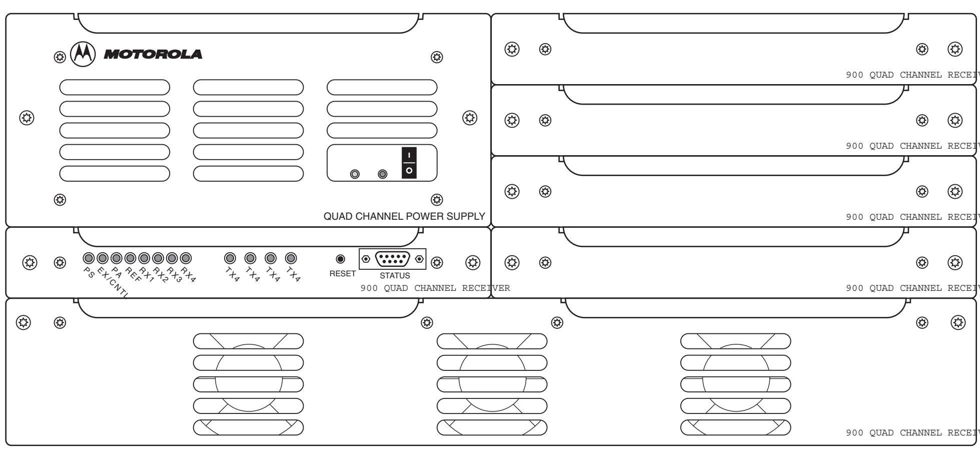
The QUAD Channel 900 MHz BR contains the four FRUs listed below:

- ❐ QUAD Channel 900 MHz EX /Cntl
- ❐ QUAD Channel 900 MHz Power Amplifier
- ❐ QUAD Channel 800 MHz and 900 MHz Power Supply (DC)
- ❐ QUAD Channel 900 MHz Receiver (qty. 4)

The modular design of the QUAD Channel 900 MHz BR also offers increased shielding and provides easy handling. All FRUs connect to the backplane through blindmate connectors.

NOTE
Both the 800 MHz QUAD and 900 MHz QUAD Base Radios use the same backplane and cardcage but call out different FCC ID numbers.

Figure 2 shows the front view of the BR.



EBTS282Q_900
112601JNM

Figure 2 ***QUAD Channel 900 MHz Base Radio (Typical)***

QUAD Channel 900 MHz Base Radio Controls and Indicators

Power Supply and EX / CNTL controls and indicators monitor BR status and operating conditions, and also aid in fault isolation. The Power Supply and EX / CNTL sections of this chapter discuss controls and indicators for both modules.

The Power Supply has two front panel indicators. The EX / CNTL has twelve front panel indicators. The Power Supply power switch applies power to the BR. The EX / CNTL RESET switch resets the BR.

QUAD Channel 900 MHz Base Radio Performance Specifications

QUAD Channel 900 MHz Base Radio General Specifications

Table 6 lists general specifications for the BR.

Table 6 ***QUAD Channel 900 MHz BR General Specifications***

Specification	Value or Range
Dimensions: Height Width Depth Weight	 5 EIA Rack Units (RU) 19" (482.6 mm) 16.75" (425 mm) 85 lbs. (38.6 kg)
Operating Temperature	32˚ to 104˚ F (0˚ to 40˚ C)
Storage Temperature	-22˚ to 140˚ F (-30˚ to 60˚ C)
Rx Frequency Range: 900 MHz iDEN	 896 - 901 MHz
Tx Frequency Range: 900 MHz iDEN	 935 - 940 MHz
Tx – Rx Spacing: 900 MHz iDEN	 39 MHz
Carrier Spacing	25 kHz
Carrier Capacity[a]	1, 2, 3 or 4
Frequency Generation	Synthesized
Digital Modulation	QPSK, M-16QAM, and M-64QAM
Power Supply Inputs: VDC	 -48 VDC (-41 to -60 VDC)
Diversity Branches	Up to 3

a. Multi-carrier operation must utilize adjacent, contiguous RF carriers.

QUAD Channel 900 MHz Base Radio Transmit Specifications

Table 7 lists the BR transmit specifications.

Table 7 ***QUAD Channel 900 MHz BR Transmit Specifications***

Specification	Value or Range	
Average Power Output:	Low average output power per carrier	High average output power per carrier
(900 MHZ) Single Carrier	5.0W	52.0W
(900 MHz) Dual Carrier	2.5W	26.0W
(900 MHz) Triple Carrier	1.7W	16.1W
(900 MHz) QUAD Channel	1.3W	10.5W
Transmit Bit Error Rate (BER)	0.01%	
Occupied Bandwidth	18.5 kHz	
Frequency Stability *	1.5 ppm	
RF Input Impedance	50 Ω (nom.)	
FCC Designation (FCC Rule Part 90): 900 MHz QUAD BR	ABZ89FC5798	

* Transmit frequency stability locks to an external site reference, which controls ultimate frequency stability to a level of 50 ppb.

QUAD Channel 900 MHz Base Radio Receive Specifications

Table 8 lists the receive specifications.

Table 8 ***QUAD Channel 900 MHz Receive Specifications***

Specification	Value or Range
Static Sensitivity †: 900 MHz BR	-108 dBm (BER = 8%)
BER Floor (BER = 0.01%)	≥ -80 dBm
IF Frequencies 1st IF (All bands): 2nd IF:	 73.35 MHz (1st IF) 450 kHz (2nd IF)
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 15): 900 MHz BR	ABZ89FR5799

† Measurement referenced from single receiver input port of BR.

* Stability without site reference connected to station. Receive frequency stability locks to an external site reference, which controls ultimate frequency stability to a level of 50 ppb.

NOTE

FCC Compliance Notice: The QUAD Channel 900 MHz Base Radio (BR) is FCC Compliant only when used with Motorola-supplied RF Distribution Systems. Motorola does not recommend using this BR without a Motorola- approved RF Distribution System. If customer uses the BR with a non-Motorola supplied RF Distribution System, the customer is responsible for filing for FCC approval.

QUAD Channel 900 MHz Base Radio Theory of Operation

The QUAD Channel 900 MHz BR operates with other site controllers and equipment and must be properly terminated. The following description assumes such a configuration. Figure 6 show an overall block diagram of the QUAD Channel 900 MHz BR.

Power is applied to the DC Power inputs located on the QUAD Channel 900 MHz BR backplane. The DC Power input is connected if -48 VDC or batteries are used in the site.

Power is applied to the BR by setting the Power Supply power switch to the ON position. Upon power-up, the QUAD Channel 900 MHz BR performs self-diagnostic tests to ensure the integrity of the unit. These tests, which include memory and Ethernet verification routines, primarily examine the EX / CNTL.

After completing self-diagnostic tests, the QUAD Channel 900 MHz BR reports alarm conditions on any of its modules to the site controller via Ethernet. Alarm conditions may also be verified locally. Local verification involves using the service computer and the STATUS port located on the front of the QUAD Channel 900 MHz EX / CNTL.

The software resident in FLASH on the EX / CNTL registers the BR with the site controller via Ethernet. After BR registration on initial power-up, the BR software downloads via resident FLASH or Ethernet and executes from RAM. The download includes operating parameters for the QUAD Channel 900 MHz BR. These parameters allow the QUAD Channel 900 MHz BR to perform call processing functions.

After software downloads to the BR via Ethernet, FLASH memory stores the software object. Upon future power-ups, the software object in FLASH loads into RAM for execution.

The BR operates in a TDMA (Time Division Multiple Access) mode. This mode, combined with voice compression techniques, increases channel capacity by a ratio of as much as six to one. TDMA divides both the receive and transmit signals of the BR into six individual time slots. Each receive slot has a corresponding transmit slot. This pair of slots comprises a logical RF channel.

The BR uses diversity reception for increased coverage area and improved quality. The Receiver modules within the QUAD Channel 900 MHz BR contain three receiver paths. Two-branch diversity sites use two Receiver paths, and three-branch diversity sites use three Receiver paths.

All Receiver paths within a given Receiver module are programmed to the same receive frequency. Signals from each receiver arrive at the EX / CNTL module. This module performs a diversity combining algorithm on the signals. The resultant signal undergoes an error-correction process. Then, via Ethernet, the site controller acquires the signal, along with control information about signal destination.

Two separate FRUs comprise the transmit section of the QUAD Channel 900 MHz BR. These are the Exciter portion of the EX / CNTL and the Power Amplifier (PA). The Exciter processes commands from the CNTL, assuring transmission in the proper modulation format. Then the low-level signal enters the PA. The PA amplifies this signal to the desired output power level. The PA is a continuously keyed linear amplifier. A power control routine monitors the output power of the BR. The routine adjusts the power as necessary to maintain the proper output level.

QUAD Channel 800 MHz Base Radio Overview

The QUAD Channel 800 MHz BR provides reliable, digital BR capabilities in a compact, software-controlled design. Voice compression techniques, time division multiplexing (TDM) and multi-carrier operation provide increased channel capacity.

The QUAD Channel 800 MHz BR contains the four FRUs listed below:

- ❒ QUAD Channel 800 MHz EX / Cntl
- ❒ QUAD Channel 800 MHz Power Amplifier
- ❒ QUAD Channel 800 MHz/900 MHz Power Supply (DC)
- ❒ QUAD Channel 800 MHz Receiver (qty. 4)

The modular design of the QUAD Channel 800 MHz BR also offers increased shielding and provides easy handling. All FRUs connect to the backplane through blindmate connectors.

NOTE

Both the 800 MHz QUAD and 900 MHz QUAD Base Radios use the same backplane and cardcage but call out different FCC ID numbers.

Figure 3 shows the front view of the BR.

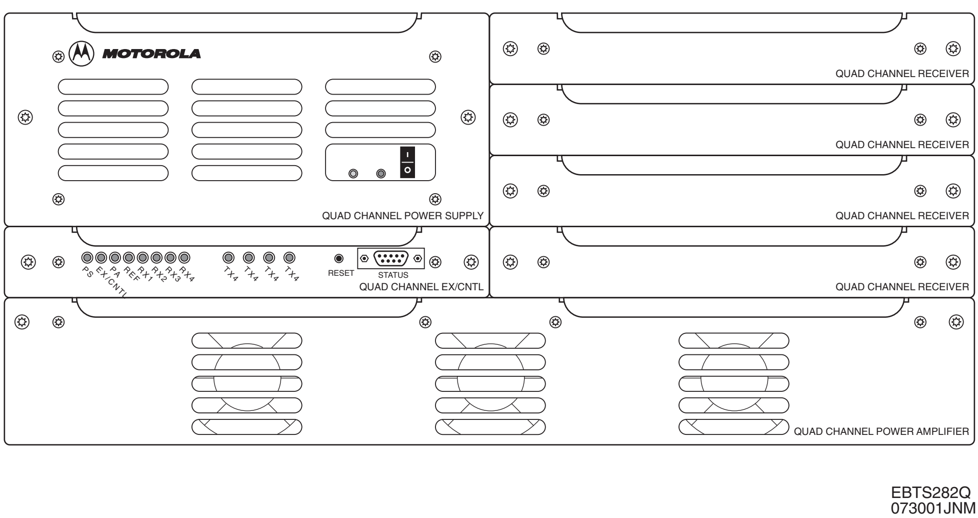


Figure 3 ***QUAD Channel 800 MHz Base Radio (Typical)***

QUAD Channel 800 MHz Base Radio Controls and Indicators

Power Supply and EX / CNTL controls and indicators monitor BR status and operating conditions, and also aid in fault isolation. The Power Supply and EX / CNTL sections of this chapter discuss controls and indicators for both modules.

The Power Supply has two front panel indicators. The EX / CNTL has twelve front panel indicators. The Power Supply power switch applies power to the BR. The EX / CNTL RESET switch resets the BR.

QUAD Channel 800 MHz Base Radio Performance Specifications

QUAD Channel 800 MHz Base Radio General Specifications

Table 9 lists general specifications for the BR.

Table 9 ***QUAD Channel 800 MHz BR General Specifications***

Specification	Value or Range
Dimensions: Height Width Depth Weight	 5 EIA Rack Units (RU) 19" (482.6 mm) 16.75" (425 mm) 91 lbs. (40 kg)
Operating Temperature	32˚ to 104˚ F (0˚ to 40˚ C)
Storage Temperature	-22˚ to 140˚ F (-30˚ to 60˚ C)
Rx Frequency Range: 800 MHz iDEN	 806 - 825 MHz
Tx Frequency Range: 800 MHz iDEN	 851 - 870 MHz
Tx – Rx Spacing: 800 MHz iDEN	 45 MHz
Carrier Spacing	25 kHz
Carrier Capacity[a]	1, 2, 3 or 4
Frequency Generation	Synthesized
Digital Modulation	QPSK, M-16QAM, and M-64QAM
Power Supply Inputs: VDC	 -48 VDC (-41 to - 60 VDC)
Diversity Branches	Up to 3

a. Multi-carrier operation must utilize adjacent, contiguous RF carriers.

QUAD Channel 800 MHz Base Radio Transmit Specifications

Table 10 lists the BR transmit specifications.

Table 10 ***QUAD Channel 800 MHz Transmit Specifications***

Specification	Value or Range	
Average Power Output:	Low average output power per carrier	High average output power per carrier
(800 MHZ) Single Carrier	5.0W	52.0W
(800 MHz) Dual Carrier	2.5W	26.0W
(800 MHz) Triple Carrier	1.7W	16.1W
(800 MHz) QUAD Channel	1.3W	10.5W
Transmit Bit Error Rate (BER)	0.01%	
Occupied Bandwidth	18.5 kHz	
Frequency Stability *	1.5 ppm	
RF Input Impedance	50 Ω (nom.)	
FCC Designation (FCC Rule Part 90): 800 MHz) QUAD BR	ABZ89FC5794	

* Transmit frequency stability locks to an external site reference, which controls ultimate frequency stability to a level of 50 ppb.

QUAD Channel 800 MHz Base Radio Receive Specifications

Table 11 lists the receive specifications.

Table 11 ***QUAD Channel 800 MHz Receive Specifications***

Specification	Value or Range
Static Sensitivity †: 800 MHz BR	-108 dBm (BER = 8%)
BER Floor (BER = 0.01%)	≥ -80 dBm
IF Frequencies 1st IF (All bands): 2nd IF:	 73.35 MHz (1st IF) 450 kHz (2nd IF)
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 15): 800 MHz QUAD BR	ABZ89FR5793

† Measurement referenced from single receiver input port of BR.

* Stability without site reference connected to station. Receive frequency stability locks to an external site reference, which controls ultimate frequency stability to a level of 50 ppb.

NOTE

FCC Compliance Notice: The QUAD Channel 800 MHz Base Radio (BR) is FCC Compliant only when used with Motorola-supplied RF Distribution Systems. Motorola does not recommend using this BR without a Motorola- approved RF Distribution System. If customer uses the BR with a non-Motorola supplied RF Distribution System, the customer is responsible for filing for FCC approval.

QUAD Channel 800 MHz Base Radio Theory of Operation

The QUAD Channel 800 MHz BR operates together with other site controllers and equipment that are properly terminated. The following description assumes such a configuration. Figure 6 show an overall block diagram of the QUAD Channel 800 MHz BR.

Power is applied to the DC Power inputs located on the QUAD Channel 800 MHz BR backplane. The DC Power input is connected if -48 VDC or batteries are used in the site.

Power is applied to the BR by setting the Power Supply power switch to the ON position. Upon power-up, the QUAD Channel 800 MHz BR performs self-diagnostic tests to ensure the integrity of the unit. These tests, which include memory and Ethernet verification routines, primarily examine the EX / CNTL.

After completing self-diagnostic tests, the QUAD Channel 800 MHz BR reports alarm conditions on any of its modules to the site controller via Ethernet. Alarm conditions may also be verified locally. Local verification involves using the service computer and the STATUS port located on the front of the QUAD 800 MHz EX / CNTL.

The software resident in FLASH on the EX / CNTL registers the BR with the site controller via Ethernet. After BR registration on initial power-up, the BR software downloads via Ethernet and executes from RAM. The download includes operating parameters for the QUAD Channel 800 MHz BR. These parameters allow the QUAD Channel 800 MHz BR to perform call processing functions.

After software downloads to the BR via Ethernet, FLASH memory stores the software object. Upon future power-ups, the software object in FLASH loads into RAM for execution.

The BR operates in a TDMA (Time Division Multiple Access) mode. This mode, combined with voice compression techniques, increases channel capacity by a ratio of as much as six to one. TDMA divides both the receive and transmit signals of the BR into six individual time slots. Each receive slot has a corresponding transmit slot. This pair of slots comprises a logical RF channel.

The BR uses diversity reception for increased coverage area and improved quality. The Receiver modules within the QUAD Channel 800 MHz BR contain three receiver paths. Two-branch diversity sites use two Receiver paths, and three-branch diversity sites use three Receiver paths.

All Receiver paths within a given Receiver module are programmed to the same receive frequency. Signals from each receiver arrive at the EX / CNTL module. This module performs a diversity combining algorithm on the signals. The resultant signal undergoes an error-correction process. Then, via Ethernet, the site controller acquires the signal, along with control information about signal destination.

Two separate FRUs comprise the transmit section of the QUAD Channel 800 MHz BR. These are the Exciter portion of the EX / CNTL and the Power Amplifier (PA). The Exciter processes commands from the CNTL, assuring transmission in the proper modulation format. Then the low-level signal enters the PA. The PA amplifies this signal to the desired output power level. The PA is a continuously keyed linear amplifier. A power control routine monitors the output power of the BR. The routine adjusts the power as necessary to maintain the proper output level.

Legacy Single Carrier 800 MHz Base Radio Overview

The BR provides reliable digital RF communications capabilities in a compact software-controlled design. Increased channel capacity is provided through voice compression techniques and Time Division Multiplexing (TDM).

The BR contains the five FRUs listed below:

- ❐ Base Radio Controller (BRC)
- ❐ Exciter
- ❐ Power Amplifier
- ❐ Power Supply (DC)
- ❐ Receiver

The modular design of the BR also offers increased shielding and provides easy handling. All FRUs connect to the backplane through blindmate connectors. Figure 1 shows the front view of the BR.

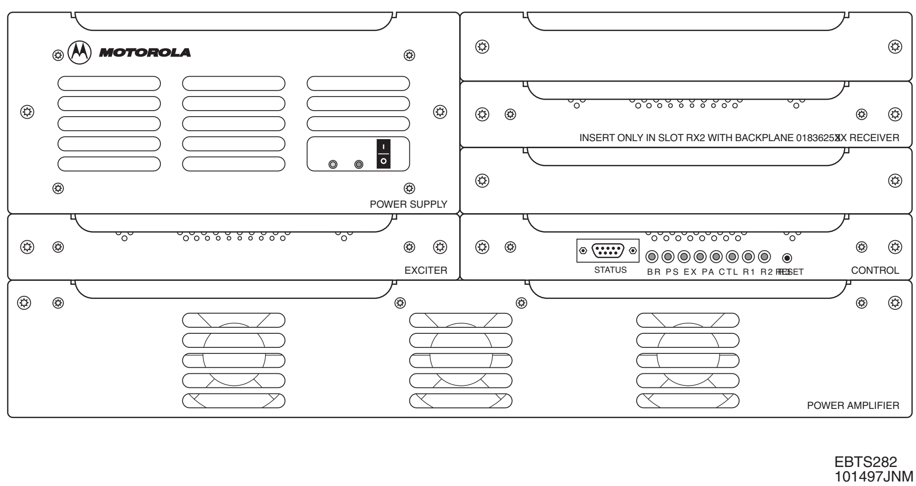


Figure 4 ***Legacy Base Radio (Typical)***

Legacy Single Carrier Base Radio Controls and Indicators

The Power Supply and BRC contain controls and indicators that provide a means for monitoring various status and operating conditions of the BR, and also aid in fault isolation. The controls and indicators for both modules are discussed in the Power Supply and BRC sections of this chapter.

The Power Supply contains two front panel indicators; the BRC contains eight front panel indicators. The Power Supply contains a power switch used to apply power to the BR. The BRC contains a RESET switch used to reset the BR.

Legacy Single Carrier Base Radio Performance Specifications

Legacy Single Channel BR General Specifications

General specifications for the BR are listed in Table 2.

Table 12 ***BR General Specifications***

Specification	Value or Range
Dimensions: Height Width Depth	 5 EIA Rack Units (RU) 19" (482.6 mm) 16.75" (425 mm)
Operating Temperature	32˚ to 104˚ F (0˚ to 40˚ C)
Storage Temperature	-22˚ to 140˚ F (-30˚ to 60˚ C)
Rx Frequency Range: 800 MHz iDEN	 806 - 821 MHz
Tx Frequency Range: 800 MHz iDEN	 851 - 866 MHz
Tx – Rx Spacing: 800 MHz iDEN	 45 MHz
Channel Spacing	25 kHz
Frequency Generation	Synthesized
Digital Modulation	M-16QAM
Power Supply Inputs: VDC	 -48 VDC (-41 - 60 VDC)
Diversity Branches	Up to 3

Legacy Single Channel BR Transmit Specifications

The BR transmit specifications are listed in Table 3.

Table 13 ***Transmit Specifications***

Specification	Value or Range
Average Power Output: (800 MHz) 40 W PA (800 MHz) 70 W PA	 5-40 W 5 - 70 W
Transmit Bit Error Rate (BER)	0.01%
Occupied Bandwidth	18.5 kHz
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 90): (800 MHz) 40 W PA (800 MHz) 70 W PA	 ABZ89FC5772 ABZ89FC5763
* Stability without site reference connected to station.	

Legacy Single Channel BR Receive Specifications

The receive specifications are listed in Table 4.

Table 14 ***Receive Specifications***

Specification	Value or Range
Static Sensitivity †: 800 MHz BR	 -108 dBm (BER = 8%)
BER Floor (BER = 0.01%)	≥ -80 dBm
IF Frequencies 1st IF (All bands): 2nd IF: 800 MHz	 73.35 MHz (1st IF) 450 kHz (2nd IF)
Frequency Stability *	1.5 ppm
RF Input Impedance	50 Ω (nom.)
FCC Designation (FCC Rule Part 15): 800 MHz BR	 ABZ89FR5762
† Measurement referenced from single receiver input port of BR. * Stability without site reference connected to station.	

NOTE

FCC Compliance Notice: The Base Radio (BR) is FCC Compliant only when used in conjunction with Motorola supplied RF Distribution Systems. Motorola does not recommend that this BR be used without a Motorola approved RF Distribution System. It is the customer's responsibility to file for FCC approval if the BR is used with a non-Motorola supplied RF Distribution System.

Legacy Single Channel BR Theory of Operation

The BR operates in conjunction with other site controllers and equipment that are properly terminated. The following description assumes such a configuration. Figures 7 show an overall block diagram of the BR.

Power is applied to the DC Power inputs located on the BR backplane. The DC Power input is connected if -48 VDC or batteries are used in the site.

Power is applied to the BR by setting the Power Supply power switch to the "ON" position. Upon power-up, the BR performs self-diagnostic tests to ensure the integrity of the unit. These tests are primarily confined to the BRC and include memory and Ethernet verification routines.

After the self-diagnostic tests are complete, the BR reports any alarm conditions present on any of its modules to the site controller via Ethernet. Alarm conditions may also be verified locally using service computer and the STATUS port located on the front of the BRC.

NOTE

Legacy Single Channel Base Radios configured with 3X Receiver modules and Exciter modules (Version R.01.04.xx or higher) can be upgraded to Generation 2 2 Base Radios by removing the BRC module and replacing it with the EBRC (Enhanced Base Radio Controller) module.

The software resident in EPROM on the BRC registers the BR with the site controller via Ethernet. Once registered, the BR software is downloaded via Ethernet and is executed from RAM. Operating parameters for the BR are included in this download. This software allows the BR to perform call processing functions.

The BR operates in a TDMA (Time Division Multiple Access) mode. This mode, combined with voice compression techniques, provides an increased channel capacity ratio of as much as 6 to 1. Both the receive and transmit signals of the BR are divided into 6 individual time slots. Each receive slot has a corresponding transmit slot; this pair of slots comprises a logical RF channel.

The BR uses diversity reception for increased coverage area and improved quality. The Receiver module within the BR contains up to three receivers. Two Receivers are used with two-branch diversity sites, and three Receivers are used with three-branch diversity sites.

All Receivers within a given BR are programmed to the same receive frequency. The signals from each receiver are fed to the BRC where a diversity combining algorithm is performed on the signals. The resultant signal is processed for error correction and then sent to the site controller via Ethernet with the appropriate control information regarding its destination.

The transmit section of the BR is comprised of two separate FRUs, the Exciter and Power Amplifier (PA). Several PA FRUs are available, covering different applications and power levels; these are individually discussed as applicable in later subsections.

The Exciter processes the information to transmit from the BRC in the proper modulation format. This low level signal is sent to the PA where it is amplified to the desired output power level. The PA is a continuous keyed linear amplifier. A power control routine monitors the output power of the BR and adjusts it as necessary to maintain the proper output level.

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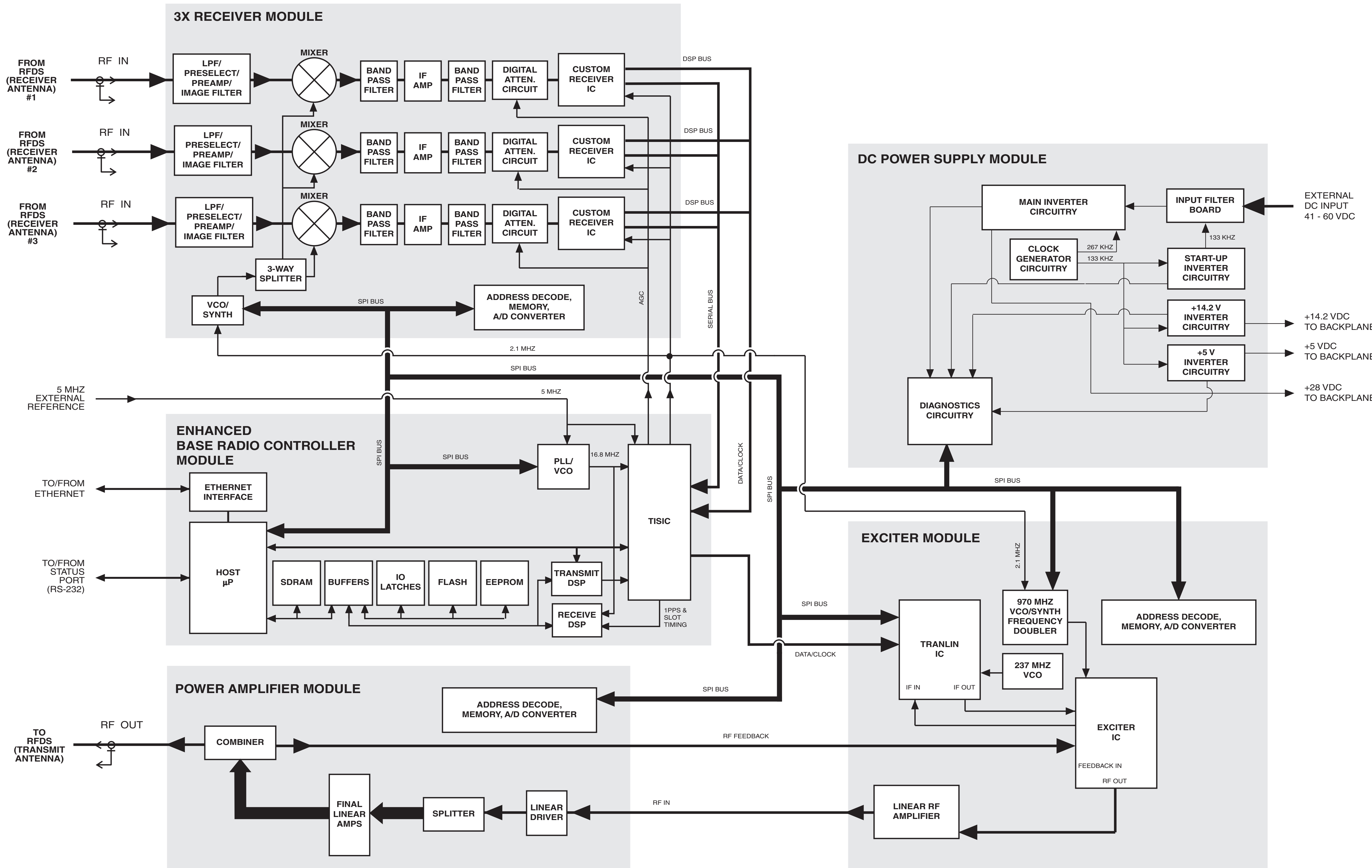


NOTES:
1. 2-Branch systems must have a 50Ω load (P/N 5882106P03) installed on Antenna Port #3.
2. Set the RX_FRU_CONFIG parameter as follows:
   2-Branch Systems: 12
   3-Branch Systems: 123

EBTS284
053001JNM

Figure 5 ***Generation 2***
Single Channel 800 MHz Base Radio Functional Block Diagram

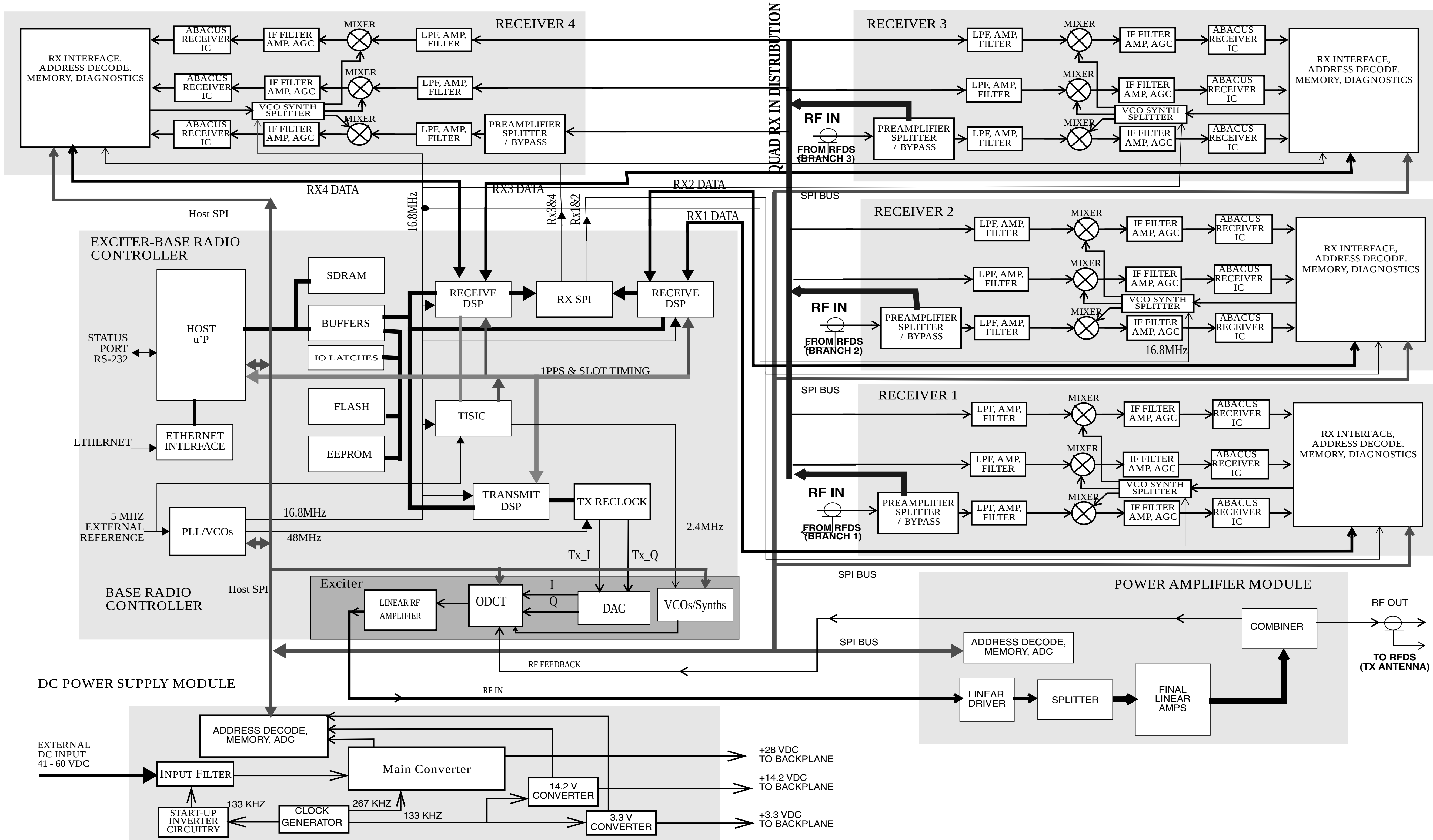
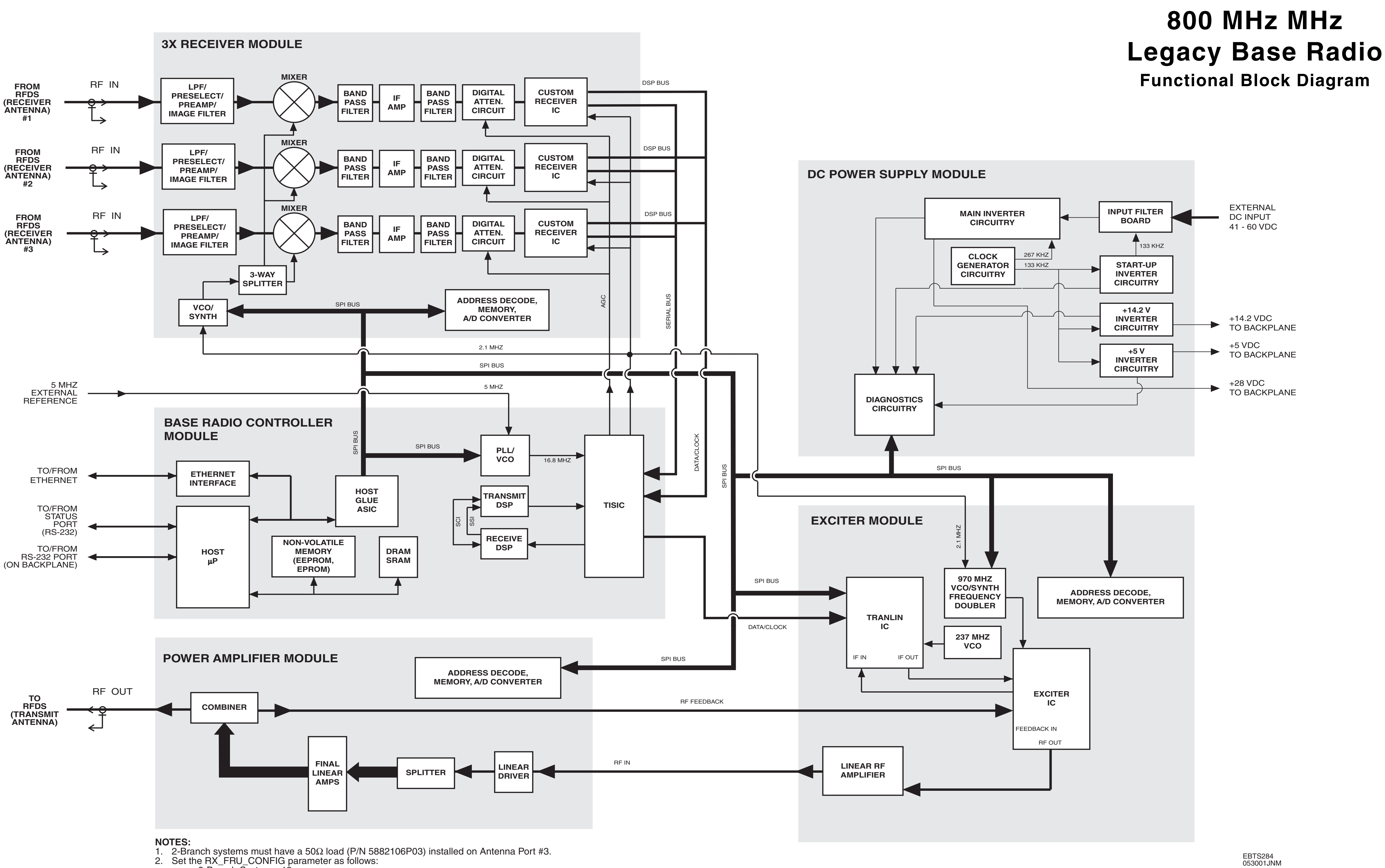


Figure 6 ***800 and 900 MHZ QUAD Channel Base Radio Functional Block Diagram***



NOTES:

1. 2-Branch systems must have a 50Ω load (P/N 5882106P03) installed on Antenna Port #3.
2. Set the RX_FRU_CONFIG parameter as follows:
   - 2-Branch Systems: 12
   - 3-Branch Systems: 123

Figure 7 ***800 MHz Legacy Base Radio Functional Block Diagram***

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MOTOROLA

Base Radio Controllers

Overview

This chapter provides information on Base Radio Controllers (BRCs):

FRU Number to Kit Number Cross Reference

Base Radio Controller (BRC) Field Replaceable Units (FRUs) are available for the iDEN EBTS. The FRU contains the BRC kit and required packaging. Table 1 provides a cross reference between BRC FRU numbers and kit numbers.

Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
Single Channel 800 MHz Base Radio Controller	TLN3334	CLN1469
Single Channel Base Radio Controller (1500 MHz MCI)	TLN3425	CLN1472
Enhanced Base Radio Controller	DLN6446	CLN1653
QUAD Channel 900 MHz Exciter/BR Controller	DLN1203	
QUAD Channel 800 MHz Exciter/BR Controller	CLN1497	CLF1560

Enhanced Base Radio Controller

Enhanced Base Radio Controller Overview

Generation 2 BR/EBRC Compatibility

Table 2 ***EBRC Compatibility***

Module	Software Revision	Compatible
Exciter	***R01.00.xx- R01.03.xx***	SR 10.0 or Greater
Exciter	***R01.04.xx*** and higher	SR 9.15 or Greater
Single Receiver	R01.00.xx - R01.02.xx	SR 10.0 or Greater
Single Receiver	R01.03.xx and higher	SR 9.15 or Greater
3X Receiver	all versions	SR 9.15 or Greater
40W Power Amplifier	all versions	SR 9.15 or Greater
70W Power Amplifier	all versions	SR 9.15 or Greater

The Enhanced Base Radio Controller (EBRC) serves as the main controller for the Base Radio. The EBRC provides signal processing and operational control for other Base Radio modules. Figure 1 shows a top view of the EBRC with the cover removed. The EBRC module consists of two printed circuit boards (EBRC board and LED display board), a slide-in housing, and associated hardware.

❐ The EBRC is only compatible with System Software Release SR 9.15 or newer. Any system running a pre-SR 9.15 System Release must be updated to at least SR 9.15 prior to installation.

❐ The EBRC is compatible with Legacy Base Radios that support multiple receiver module assemblies.

❐ The Generation 2 Base Radio is compatible with all versions of power supplies.

Determining FRU and Kit Revisions

For Generation 2 BR/EBRC

These commands will return all available FRU and Kit Revision numbers. Use these to determine installation requirements:

1. Connect one end of the RS-232 cable to the service computer.
2. Connect the other end of the RS-232 cable to the Service Access port, located on the front panel of the EBRC module.
3. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the password **motorola**, log in to the BR.

```
:> login -ufield
password: motorola

field>
```

4. Collect revision numbers from the station by typing the following command:

```
field> fv -oplatform
field>
```

5. If all modules return revision numbers of the format "Rxx.xx.xx", then all revision numbers are present. In that case, verification requires no further action. If revision numbers return as blank, or not in the format "Rxx.xx.xx", contact your local Motorola representative or Technical Support.

For Legacy Single Channel BR/BRC

1. Connect one end of the RS-232 cable to the service computer.
2. Connect the other end of the RS-232 cable to the STATUS port, located on the front panel of the BRC.
3. Using the field password, login to the BR.

4. Collect revision numbers from the station by typing the following commands:

```
BRC>dekey
BRC>test_mode
BRC>get brc_rev_no
BRC>get rx1_rev_no
BRC>get rx2_rev_no
BRC>get rx3_rev_no                    (if BR is 3 branch)
BRC>get pa_rev_no
BRC>get ex_rev_no

BRC>
```

5. If all modules return revision numbers of the format “Rxx.xx.xx”, then all revision numbers are present and no further action is required. Log out and repeat steps 1 through 4 for each additional BR.

   If revision numbers were returned as blank or not in the format “Rxx.xx.xx”, contact your local Motorola representative or Technical Support.

EBRC Description

The EBRC memory contains the operating software and codeplug. The software defines BR operating parameters, such as output power and operating frequency.

The EBRC connects to the Base Radio backplane with one 96-pin Euro connector and one blindmate RF connector. Two Torx screws secure the EBRC in the Base Radio chassis.

Figure 1 shows a top view of the EBRC (model CLN1653) with the cover removed. The EBRC module contains the main board, CLN7428 and LED board, CLN7208.

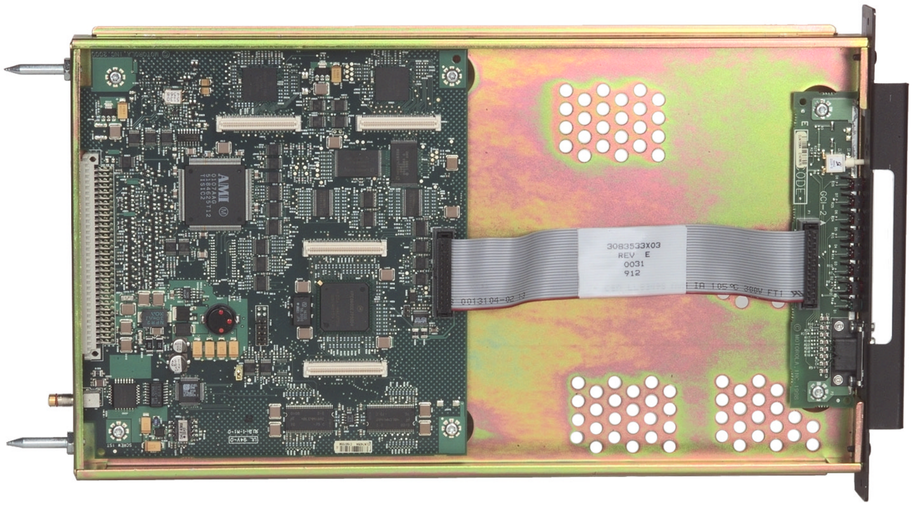


Figure 1 ***Enhanced Base Radio Controller, version CLN1653 (with cover removed)***

Enhanced Base Radio Controller Controls and Indicators

The EBRC monitors the functions of other Base Radio modules. The LEDs on the front panel indicate the status of EBRC-monitored modules. The CTL LED on the front panel light momentarily on initial BR power-up and on BR resets. Figure 2 shows the front panel of the EBRC.

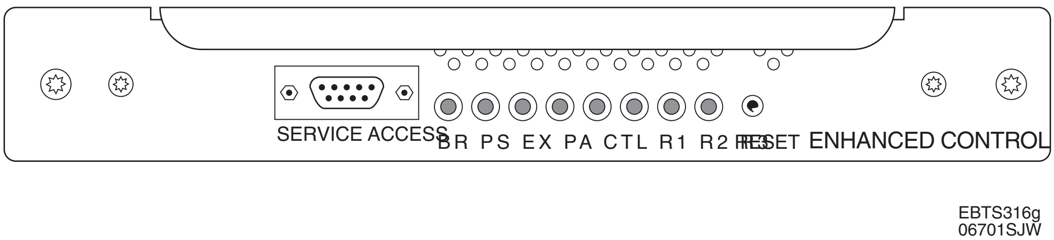


Figure 2 ***EBRC (Front View)***

Indicators

Table 3 lists and describes the EBRC LEDs.

Table 3 ***EBRC Indicators***

LED	Color	Module Monitored	Condition	Indications
BR	Green	BR	Solid (on)	Station is keyed
			Flashing (on)	Station is not keyed
			Off	Station is out of service or power is removed
PS	Red	Power Supply	Solid (on)	FRU failure indication - Power Supply has a major alarm and is out of service
			Flashing (on)	Power Supply has a minor alarm and may be operating at reduced performance
			Off	Power Supply under normal operation (no alarms)
EX	Red	Exciter	Solid (on)	FRU failure indication - Exciter has a major alarm and is out of service
			Flashing (on)	Exciter has a minor alarm and may be operating at reduced performance
			Off	Exciter under normal operation (no alarms)
PA	Red	Power Amplifier	Solid (on)	FRU failure indication - PA has a major alarm and is out of service
			Flashing (on)	PA has a minor alarm and may be operating at reduced performance
			Off	PA under normal operation (no alarms)

Table 3 ***EBRC Indicators (Continued)***

LED	Color	Module Monitored	Condition	Indications
CTL	Red	Controller	Solid (on)	FRU failure indication - BRC has a major alarm and is out of service. **NOTE:**
			Flashing (on)	BRC has a minor alarm and may be operating at reduced performance
			Off	BRC under normal operation (no alarms)
R1 R2 R3	Red	Receiver #1, #2, or #3	Solid (on)	FRU failure indication - Receiver (#1, #2, or #3) has a major alarm and is out of service
			Flashing (on)	Receiver (#1, #2, or #3) has a minor alarm and may be operating at reduced performance
			Off	Receiver (#1, #2, or #3) under normal operation (no alarms)

Controls

Table 4 lists the controls and descriptions.

Table 4 ***EBRC Controls***

Control	Description
RESET Switch	A push-button switch used to manually reset the BR.
STATUS connector	A 9-pin connector used for connection of a service computer, providing a convenient means for testing and configuring.

STATUS Connector

Table 5 the pin-outs for the STATUS connector.

Table 5 ***Pin-outs for the STATUS Connector***

Pin-out	Signal
1	not used
2	TXD
3	RXD
4	not used
5	GND
6	not used
7	not used
8	not used
9	not used

Enhanced Base Radio Controllers Theory of Operation

Table 6 briefly describes the EBRC circuitry. Figure 15 is a functional block diagram of the EBRC.

Table 6 ***EBRC Circuitry***

Circuit	Description
Host Microprocessor	Contains integrated circuits that comprise the central controller of the EBRC and station
Non-Volatile Memory	Consists of: • FLASH containing the station operating software • EEPROM containing the station codeplug data
Volatile Memory	Contains SDRAM to store station software used to execute commands.
Ethernet Interface	Provides the EBRC with a 10Base2 Ethernet communication port to network both control and compressed voice data
RS-232 Interface	Provides the EBRC with an RS-232 serial interface
Digital Signal Processors	Performs high-speed modulation/demodulation of compressed audio and signaling data
TISIC	Contains integrated circuits that provide timing reference signals for the station
TX Reclock	Contains integrated circuits that provide highly stable, reclocked transmit signals and peripheral transmit logic
Station Reference Circuitry	Generates the 16.8 MHz and 48 MHz reference signals used throughout the station
Input Ports	Contains 16 signal input ports that receive miscellaneous inputs from the BR
Output Ports	Contains 40 signal output ports, providing a path for sending miscellaneous control signals to circuits throughout the BR
Remote Station Shutdown	Provides software control to cycle power on the BR

MPC860 Host Microprocessor

The MPC860 host microprocessor is the main controller for the BR. The processor operates at a 50-MHz clock speed. The processor controls Base Radio operation according to station software in memory. Station software resides in FLASH memory. For normal operation, the system transfers this software to non-volatile memory. An EEPROM contains the station codeplug.

NOTE

At BR power-up, the EBRC LED indicates a major alarm. This indication continues until BR software achieves a predetermined state of operation. Afterward, the software turns off the EXBRC LED.

Serial Communication Buses

The microprocessor provides a general-purpose SMC serial management controller bus.

The SMC serial communications bus is an asynchronous RS-232 interface with no hardware handshake capability. The BRC front panel includes a nine-pin, D-type connector. This connector provides a port where service personnel may connect a service computer. Service personnel can perform programming and maintenance tasks via Man-Machine Interface (MMI) commands. The interface between the SMC port and the front- panel STATUS connector is via EIA-232 Bus Receivers and Drivers.

Host Processor

The microprocessor incorporates 4k bytes of instruction cache and 4k bytes of data cache that significantly enhance processor performance.

The microprocessor has a 32-line address bus. The processor uses this bus to access non-volatile memory and SDRAM memory. Via memory mapping, the processor also uses this bus to control other BRC circuitry.

The microprocessor uses its Chip Select capability to decode addresses and assert an output signal. The eight chip-select signals select non-volatile memory, SDRAM memory, input ports, output ports, and DSPs.

The Host processor...

- ❒ Provides serial communications between the Host Microprocessor and other Base Radio modules.
- ❒ Provides condition signals necessary to access SDRAM.
- ❒ Accepts interrupt signals from EBRC circuits (such as DSPs).
- ❒ Organizes the interrupts, based on hardware-defined priority ranking.
- ❒ The Host supports several internal interrupts from its Communications Processor Module. These interrupts allow efficient use of peripheral interfaces.
- ❒ The Host supports 10 Mbps Ethernet/IEEE 802.3.
- ❒ Provides a 32-line data bus transfers data to and from EBRC SDRAM and other BRC circuitry. Buffers on this data bus allow transfers to and from non-volatile memory, general input and output ports and DSPs.

Non-Volatile Memory

Base Radio software resides in 2M x 32 bits of FLASH memory. The Host Microprocessor addresses the FLASH memory with 20 of the host address bus' 32 lines. The host accesses FLASH data over the 32-line host data bus. A host-operated chip-select line provides control signals for these transactions.

The FLASH contains the operating system and application code. The system stores application code in FLASH for fast recovery from reset conditions. Application code transfers from network or site controllers may occur in a background mode. Background mode transfers allow the station to remain operational during new code upgrades.

The data that determines the station personality resides in a 32K x eight bit codeplug EEPROM. The microprocessor addresses the EEPROM with 15 of the host address bus’ 32 lines. The host accesses EEPROM data with eight of the data bus’ 32 lines. A host-operated chip-select line provides control signals for these transactions.

During the manufacturing process, the factory programs the codeplug’s default data. The BRC must download field programming data from network and site controllers. This data includes operating frequencies and output power level. The station permits adjustment of many station parameters, but the station does not store these adjustments. Refer to the Software Commands chapter for additional information.

Volatile Memory

Each BRC contains 8MB x 32 bits of SDRAM. The BRC downloads station software code into SDRAM for station use. SDRAM also provides short-term storage for data generated and required during normal operation. SDRAM is volatile memory. A loss of power or system reset destroys SDRAM data.

The system performs read and write operations over the Host Address and Data buses. These operations involve column and row select lines under control of the Host processor’s DRAM controller. The Host address bus and column row signals sequentially refresh SDRAM memory locations.

Ethernet Interface

The Host processor’s Communications Processor Module (CPM) provides the Local Area Network (LAN) Controller for the Ethernet Interface. The LAN function implements the CSMA/CD access method, which supports the IEEE 802.3 10Base2 standard.

The LAN coprocessor supports all IEEE 802.3 Medium Access Control, including the following:

- framing
- preamble generation
- stripping
- source address generation
- destination address checking

The PCM LAN receives commands from the CPU.

The Ethernet Serial Interface works directly with the CPM LAN to perform the following major functions:

- 10 MHz transmit clock generation (obtained by dividing the 20 MHz signal provided by on-board crystal)
- Manchester encoding/decoding of frames

- electrical interface to the Ethernet transceiver

An isolation transformer provides high-voltage protection. The transformer also isolates the Ethernet Serial Interface (ESI) and the transceiver. The pulse transformer has the following characteristics:

- Minimum inductance of 75 µH
- 2000 V isolation between primary and secondary windings
- 1:1 Pulse Transformer

The Coaxial Transceiver Interface (CTI) is a coaxial cable line driver and receiver for the Ethernet. CTI provides a 10Base2 connection via a coaxial connector on the board. This device minimizes the number of external components necessary for Ethernet operations.

A DC/DC converter provides a constant voltage of -9 Vdc for the CTI from a 3.3 Vdc source.

The CTI performs the following functions:

- Receives and transmits data to the Ethernet coaxial connection
- Reports any collision that it detects on the coaxial connection
- Disables the transmitter when packets are longer than the legal length (Jabber Timer)

Digital Signal Processors

The BRC includes two Receive Digital Signal Processors (RXDSPs) and a Transmit Digital Signal Processor (TXDSP). These DSPs and related circuitry process compressed station transmit and receive audio or data. The related circuitry includes the TDMA Infrastructure Support IC (TISIC) and the TISIC Interface Circuitry. The DSPs only accept input and output signals in digitized form.

The RXDSP inputs are digitized receiver signals. The TXDSP outputs are digitized voice audio and data (modulation signals). These signals pass from the DSP to the Exciter portion of the EXBRC. DSPs communicate with the Microprocessor via an eight-bit, host data bus on the host processor side. For all DSPs, interrupts drive communication with the host.

The RXDSP operates from an external 16.8 MHz clock, provided by the local station reference. The RXDSP internal operating clock signal is 150MHz, produced by an internal Phase-Locked Loop (PLL).

The RXDSP accepts digitized signals from the TISIC device through the RxDSP parallel bus. The RXDSP supports a single carrier (single 3 branch receiver) digital data input.

The RXDSP accesses its DSP program and signal-processing algorithms in 128k words of internal memory. The RXDSP communicates with the host bus on an 8-bit interface.

Additionally, a serial control path connects the two RXDSPs and the TXDSP. The Synchronous Communications Interface (SCI) port facilitates this serial control path.

For initialization and control purposes, the RXDSP connects to the TISIC device.

The TXDSP operates at an external clock speed of 16.8 MHz, provided by the EBRC local station reference. The TXDSP internal operating clock is 150MHz, produced by an internal Phase Lock Loop (PLL).

The TXDSP sends one carrier of digitized signal to the TISIC to reformat the date before sending it to the exciter. The exciter converts the digital signal to analog.

The TXDSP contains its own, internal address and data memory. The TXDSP can store 128k words of DSP program and data memory. An eight-bit interface handles TXDSP-to-host bus communications.

TISIC

The TISIC controls internal DSP operations. This circuit provides the following functions:

- ❐ For initialization and control, interfaces with the RXDSP via the DSP address and data buses.
- ❐ Accepts a 16.8 MHz signal from Station Reference Circuitry.
- ❐ Accepts a 5 MHz signal, modulated with one pulse per second (1 PPS) from the site reference.
- ❐ Demodulates the 1 PPS from the modulated 5 MHz signal
- ❐ Outputs a 1 PPS signal and a windowed version of this signal for network timing alignment.
- ❐ Outputs a 2.1 MHz reference signal used by the Exciter and Receiver(s).
- ❐ Generates 15 ms and 7.5 ms ticks. (These ticks synchronize to the 1 PPS time mark. The system decodes the time mark from the site reference. Then the system routes the reference to the TXDSP and RXDSP.)
- ❐ Provides a 4.8 MHz reference signal. This signal is used by the Exciter to clock data into the TRANLIN
- ❐ Accepts differential data from the Receiver(s) (Rx through Rx3) via the interface circuitry.
- ❐ Transmits serial control data to the Receiver(s) (Rx through Rx3) via the serial data bus.
- ❐ Accepts and formats differential data from the TXDSP for transmission to the Exciter via interface circuitry.
- ❐ Generates the Receiver SSI (RxSSI) frame sync interrupt for the RxDSP.

Station Reference Circuitry

The Station Reference Circuitry is a phase-locked loop (PLL). This PLL consists of a high-stability, Voltage-Controlled, Crystal Oscillator (VCXO) and a PLL IC. GPS output from the iSC connects to the 5 MHz/1 PPS BNC connector on the BR backplane. Wiring at this connector routes signals to EXBRC station reference circuitry.

The PLL compares the 5 MHz reference frequency to the 16.8 MHz VCXO output. Then the PLL generates a DC correction voltage. The PLL applies this correction voltage to the VCO through an analog gate. The analog gate closes when three conditions coexist: (1) The 5 MHz tests stable. (2) The PLL IC is programmed. (3) Two PLL oscillator and reference signal output alignments occur.

A loss in the 5MHz / 1PPS signal causes the control voltage enable switch to open. This complex PLL control allows the BR to maintain 16.5 MHz capability during short disconnects (of approximately one minute) of the 5 MHz / 1 PPS signal. (For example, during 5 MHz / 1 PPS cable maintenance work.)

When the gate enables, the control voltage from the PLL can adjust the high-stability VCXO frequency. The adjustment can achieve a stability nearly equivalent to that of the external, 5 MHz frequency reference.

The correction voltage from the PLL continuously adjusts the VXCO frequency. The VXCO outputs a 16.8 MHz clock signal. The circuit applies this clock signal to the receiver, and TISIC.

The TISIC divides the 16.8 MHz signal by seven, and outputs a 2.1 MHz signal. This output signal then becomes the 2.1 MHz reference for the Exciter and Receiver(s).

Input Ports

One general-purpose input register provides for EBRC and station circuit input signals. The register has 16 input ports. The Host Data Bus conveys input register data to the Host Microprocessor. Typical inputs include 16.8 Station Reference Circuitry status outputs and reset status outputs.

Output Ports

Two general-purpose output registers distribute control signals from the Host Microprocessor to the BRC and station circuitry. One register has 32 output ports and the other register has 8 output ports. Control signal distribution occurs over the backplane. The Host Data Bus drives the output ports' latched outputs. Typical control signals include front-panel LED signals and SPI peripheral enable and address lines.

Remote Station Shutdown

The EBRC contains power supply shutdown circuitry. This circuitry can send a shutdown pulse to the Base Radio Power Supply. BRC software generates the shutdown control pulse.

After receiving a shutdown pulse, the power supply turns off BR power. Shut down power sources include 3.3, 5.1, 28.6 and 14.2 Vdc sources throughout the BR. Due to charges retained by BR storage elements, power supply voltages may not reach zero. The shutdown only assures that the host processor enters a power-on-reset state.

A remote site uses the shutdown function to perform a hard reset of all BR modules.

900 MHz QUAD Channel Base Radio Controller

900 MHz QUAD Channel Base Radio Controller Overview

The Base Radio Controller (BRC) provides signal processing and operational control for Base Radio modules. The BRC module consists of a printed circuit board, a slide-in housing, and associated hardware.

The BRC memory contains the operating software and codeplug. The software defines BR operating parameters, such as output power and operating frequency.

The BRC connects to the Base Radio backplane with one 168-pin FutureBus+ connector and one blindmate RF connector. Two Torx screws secure the BRC in the Base Radio chassis.

Figure 3 shows a top view of the EX/CNTL (model CLF1560) with the cover removed.

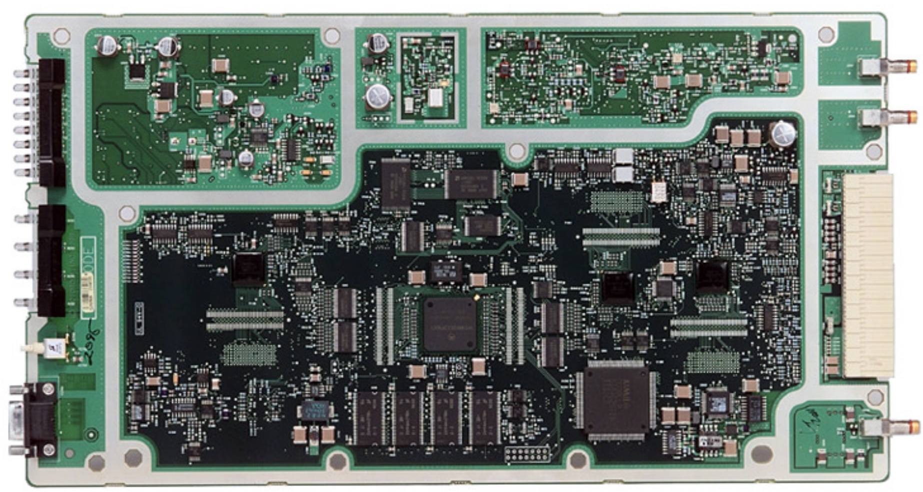


Figure 3 ***900 MHz QUAD Channel Base Radio Controller, version DLN1203 (with cover removed)***

900 MHz QUAD Channel Base Radio Controller Controls and Indicators

The BRC monitors the functions of other Base Radio modules. The LEDs on the front panel indicate the status of BRC-monitored modules. All LEDs on the BRC front panel normally flash three times upon initial power-up. A RESET switch allows a manual reset of the Base Radio. Figure 4 shows the front panel of the BRC.

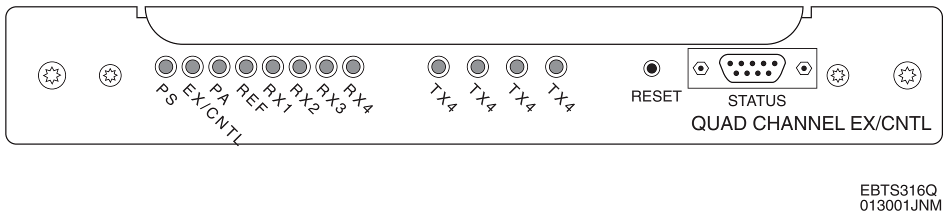


Figure 4 ***900 MHz QUAD Channel BR Controller (Front View)***

Indicators

Table 7 lists and describes the BRC LEDs.

Table 7 ***900 MHz QUAD Channel BR Controller Indicators***

LED	Color	Module Monitored	Condition	Indications
PS	Red	Power Supply	Solid (on)	FRU failure indication - Power Supply has a major alarm, and is out of service
			Flashing (on)	Power Supply has a minor alarm, and may be operating at reduced performance
			Off	Power Supply is operating normally (no alarms)
EXBRC	Red	Controller/ Exciter	Solid (on)	FRU failure indication - Controller/ Exciter has a major alarm, and is out of service (Note: Upon power-up of the BR, this LED indicates a failed mode until BR software achieves a known state of operation.)
			Flashing (on)	Controller/Exciter has a minor alarm, and may be operating at reduced performance
			Off	Controller/Exciter is operating normally (no alarms)
PA	Red	Power Amplifier	Solid (on)	FRU failure indication - PA has a major alarm, and is out of service
			Flashing (on)	PA has a minor alarm, and may be operating at reduced performance
			Off	PA is operating normally (no alarms)

Table 7 ***900 MHz QUAD Channel BR Controller Indicators (Continued)***

LED	Color	Module Monitored	Condition	Indications
REF	Red	Controller Station Reference	Solid (on)	FRU failure indication - Controller Station Reference has a major alarm, and is out of service
			Flashing (on)	BRC has a minor alarm, and may be operating in a marginal region
			Off	BRC is operating normally (no alarms)
RX1 RX2 RX3 RX4	Red	Receiver #1, #2, #3, or #4	Solid (on)	FRU failure indication - Receiver (#1, #2, #3 or #4) has a major alarm, and is out of service
			Flashing (on)	Receiver (#1, #2, #3 or #4) has a minor alarm, and may be operating at reduced performance
			Off	Receiver (#1, #2, #3 or #4) is operating normally (no alarms)
TX1	Green	BR	Solid (on)	Station Transmit Carrier #1 is keyed
			Flashing (on)	Station Transmit Carrier #1 is not keyed
			Off	Station is out of service, or power is removed
TX2	Green	BR	Solid (on)	Station Transmit Carrier #2 is keyed
			Flashing (on)	Station Transmit Carrier #2 is not keyed
			Off	Station is out of service, or power is removed
TX3	Green	BR	Solid (on)	Station Transmit Carrier #3 is keyed
			Flashing (on)	Station Transmit Carrier #3 is not keyed
			Off	Station is out of service, or power is removed
TX4	Green	BR	Solid (on)	Station Transmit Carrier #4 is keyed
			Flashing (on)	Station Transmit Carrier #4 is not keyed
			Off	Station is out of service, or power is removed

Controls

Table 8 lists the controls and descriptions.

STATUS Connector

Table 9 the pin-outs for the STATUS connector.

Table 8 ***900 MHz QUAD Channel BR Controller Controls***

Control	Description
RESET Switch	A push-button switch used to manually reset the BR.
STATUS connector	A 9-pin connector used for connection of a service computer, providing a convenient means for testing and configuring.

Table 9 ***Pin-outs for the STATUS Connector***

Pin-out	Signal
1	not used
2	TXD
3	RXD
4	not used
5	GND
6	not used
7	not used
8	not used
9	not used

900 MHz QUAD Channel Base Radio Controller Theory of Operation

Table 10 briefly describes the BRC circuitry. Figure 13 is a functional block diagram of the BRC.

Host Microprocessor

The host microprocessor is the main controller for the BR. The processor operates at a 50-MHz clock speed. The processor controls Base Radio operation according to station software in memory. Station software resides in FLASH memory. For normal operation, the system transfers this software to non-volatile memory. An EEPROM contains the station codeplug.

NOTE

At BR power-up, the EXBRC LED indicates a major alarm. This indication continues until BR software achieves a predetermined state of operation. Afterward, the software turns off the EXBRC LED.

Table 10 ***900 MHz QUAD Channel BR Controller Circuitry***

Circuit	Description
Host Microprocessor	Contains integrated circuits that comprise the central controller of the BRC and station
Non-Volatile Memory	Consists of: • FLASH containing the station operating software • EEPROM containing the station codeplug data
Volatile Memory	Contains SDRAM to store station software used to execute commands.
Ethernet Interface	Provides the BRC with a 10Base2 Ethernet communication port to network both control and compressed voice data
RS-232 Interface	Provides the BRC with an RS-232 serial interface
Digital Signal Processors	Performs high-speed modulation/demodulation of compressed audio and signaling data
TISIC	Contains integrated circuits that provide timing reference signals for the station
TX Reclock	Contains integrated circuits that provide highly stable, reclocked transmit signals and peripheral transmit logic
RX DSP SPI	Contains integrated circuits that provide DSP SPI capability and peripheral receive logic
Station Reference Circuitry	Generates the 16.8 MHz and 48 MHz reference signals used throughout the station
Input Ports	Contains 16 signal input ports that receive miscellaneous inputs from the BR
Output Ports	Contains 40 signal output ports, providing a path for sending miscellaneous control signals to circuits throughout the BR
Remote Station Shutdown	Provides software control to cycle power on the BR

Serial Communication Buses

The microprocessor provides a general-purpose SMC serial management controller bus.

The SMC serial communications bus is an asynchronous RS-232 interface with no hardware handshake capability. The BRC front panel includes a nine-pin, D-type connector. This connector provides a port where service personnel may connect a service computer. Service personnel can perform programming and maintenance tasks via Man-Machine Interface (MMI) commands. The interface between the SMC port and the front- panel STATUS connector is via EIA-232 Bus Receivers and Drivers.

Host Processor

The microprocessor incorporates 4k bytes of instruction cache and 4k bytes of data cache that significantly enhance processor performance.

The microprocessor has a 32-line address bus. The processor uses this bus to access non-volatile memory and SDRAM memory. Via memory mapping, the processor also uses this bus to control other BRC circuitry.

The microprocessor uses its Chip Select capability to decode addresses and assert an output signal. The eight chip-select signals select non-volatile memory, SDRAM memory, input ports, output ports, and DSPs.

The Host processor...

- ❒ Provides serial communications between the Host Microprocessor and other Base Radio modules.
- ❒ Provides condition signals necessary to access SDRAM.
- ❒ Accepts interrupt signals from BRC circuits (such as DSPs).
- ❒ Organizes the interrupts, based on hardware-defined priority ranking.
- ❒ The Host supports several internal interrupts from its Communications Processor Module. These interrupts allow efficient use of peripheral interfaces.
- ❒ The Host supports 10 Mbps Ethernet/IEEE 802.3.
- ❒ Provides a 32-line data bus transfers data to and from BRC SDRAM and other BRC circuitry. Buffers on this data bus allow transfers to and from non-volatile memory, general input and output ports and DSPs.

Non-Volatile Memory

Base Radio software resides in 2M x 32 bits of FLASH memory. The Host Microprocessor addresses the FLASH memory with 20 of the host address bus' 32 lines. The host accesses FLASH data over the 32-line host data bus. A host-operated chip-select line provides control signals for these transactions.

The FLASH contains the operating system and application code. The system stores application code in FLASH for fast recovery from reset conditions. Application code transfers from network or site controllers may occur in a background mode. Background mode transfers allow the station to remain operational during new code upgrades.

The data that determines the station personality resides in a 32K x eight bit codeplug EEPROM. The microprocessor addresses the EEPROM with 15 of the host address bus' 32 lines. The host accesses EEPROM data with eight of the data bus' 32 lines. A host-operated chip-select line provides control signals for these transactions.

During the manufacturing process, the factory programs the codeplug's default data. The BRC must download field programming data from network and site controllers. This data includes operating frequencies and output power level. The station permits adjustment of many station parameters, but the station does not store these adjustments. Refer to the Software Commands chapter for additional information.

Volatile Memory

Each BRC contains 8MB x 32 bits of SDRAM. The BRC downloads station software code into SDRAM for station use. SDRAM also provides short-term storage for data generated and required during normal operation. SDRAM is volatile memory. A loss of power or system reset destroys SDRAM data.

The system performs read and write operations over the Host Address and Data buses. These operations involve column and row select lines under control of the Host processor's DRAM controller. The Host address bus and column row signals sequentially refresh SDRAM memory locations.

Ethernet Interface

The Host processor's Communications Processor Module (CPM) provides the Local Area Network (LAN) Controller for the Ethernet Interface. The LAN function implements the CSMA/CD access method, which supports the IEEE 802.3 10Base2 standard.

The LAN coprocessor supports all IEEE 802.3 Medium Access Control, including the following:

- framing
- preamble generation
- stripping
- source address generation
- destination address checking

The PCM LAN receives commands from the CPU.

The Ethernet Serial Interface works directly with the CPM LAN to perform the following major functions:

- 10 MHz transmit clock generation (obtained by dividing the 20 MHz signal provided by on-board crystal)
- Manchester encoding/decoding of frames

- ❒ electrical interface to the Ethernet transceiver

An isolation transformer provides high-voltage protection. The transformer also isolates the Ethernet Serial Interface (ESI) and the transceiver. The pulse transformer has the following characteristics:

- ❒ Minimum inductance of 75 µH
- ❒ 2000 V isolation between primary and secondary windings
- ❒ 1:1 Pulse Transformer

The Coaxial Transceiver Interface (CTI) is a coaxial cable line driver and receiver for the Ethernet. CTI provides a 10Base2 connection via a coaxial connector on the board. This device minimizes the number of external components necessary for Ethernet operations.

A DC/DC converter provides a constant voltage of -9 Vdc for the CTI from a 3.3 Vdc source.

The CTI performs the following functions:

- ❒ Receives and transmits data to the Ethernet coaxial connection
- ❒ Reports any collision that it detects on the coaxial connection
- ❒ Disables the transmitter when packets are longer than the legal length (Jabber Timer)

Digital Signal Processors

The BRC includes two Receive Digital Signal Processors (RXDSPs) and a Transmit Digital Signal Processor (TXDSP). These DSPs and related circuitry process compressed station transmit and receive audio or data. The related circuitry includes the TDMA Infrastructure Support IC (TISIC) and the TISIC Interface Circuitry. The DSPs only accept input and output signals in digitized form.

The RXDSP inputs are digitized receiver signals. The TXDSP outputs are digitized voice audio and data (modulation signals). These signals pass from the DSP to the Exciter portion of the EXBRC. DSPs communicate with the Microprocessor via an eight-bit, host data bus on the host processor side. For all DSPs, interrupts drive communication with the host.

The RXDSPs operate from an external 16.8 MHz clock, provided by the local station reference. The RXDSP internal operating clock signal is 150MHz, produced by an internal Phase-Locked Loop (PLL).

The RXDSPs accept digitized signals from the receivers through Enhanced Synchronous Serial Interface (ESSI) ports. Each of two ESSI ports on a RXDSP supports a single carrier (single receiver) digital data input. The DSP circuitry includes two RXDSPs. These allow processing of up to four carriers (four receivers).

The RXDSP accesses its DSP program and signal-processing algorithms in 128k words of internal memory. The RXDSPs communicate with the host bus over an 8-bit interface.

Each RXDSP provides serial communications to its respective receiver module for receiver control via a Serial Peripheral Interface (SPI). The SPI is a parallel-to-serial conversion circuit, connected to the RXDSP data bus. Each RXDSP communicates to two receive modules through this interface.

Additionally, a serial control path connects the two RXDSPs and the TXDSP. The Synchronous Communications Interface (SCI) port facilitates this serial control path.

For initialization and control purposes, one RXDSP connects to the TISIC device.

The TXDSP operates at an external clock speed of 16.8 MHz, provided by the EXBRC local station reference. The TXDSP internal operating clock is 150MHz, produced by an internal Phase Lock Loop (PLL).

The TXDSP sends up to four carriers of digitized signal to the EX11 exciter. The exciter converts the digital signal to analog. Also at the exciter, a highly stable clock reclocks the digital data. Reclocking enhances transmit signal integrity. Two framed and synchronized data streams result. One data stream is I-data, and the other is the Q-data stream.

The TXDSP contains its own, internal address and data memory. The TXDSP can store 128k words of DSP program and data memory. An eight-bit interface handles TXDSP-to-host bus communications.

TISIC

The TISIC controls internal DSP operations. This circuit provides the following functions:

❒ For initialization and control, interfaces with one RXDSP via the DSP address and data buses.

❒ Accepts a 16.8 MHz signal from Station Reference Circuitry.

❒ Accepts a 5 MHz signal, modulated with one pulse per second (1 PPS) from the site reference.

❒ Demodulates the 1 PPS

❒ Outputs a 1 PPS signal and a windowed version of this signal for network timing alignment.

❒ Outputs a 2.4 MHz reference signal used by the Exciter.

❒ Generates 15 ms and 7.5 ms ticks. (These ticks synchronize to the 1 PPS time mark. The system decodes the time mark from the site reference. Then the system routes the reference to the TXDSP and RXDSPs.)

Station Reference Circuitry

The Station Reference Circuitry is a phase-locked loop (PLL). This PLL consists of a high-stability, Voltage-Controlled, Crystal Oscillator (VCXO) and a PLL IC. GPS output from the iSC connects to the 5 MHz/1 PPS BNC connector on the BR backplane. Wiring at this connector routes signals to EXBRC station reference circuitry.

The PLL compares the 5 MHz reference frequency to the 16.8 MHz VCXO output. Then the PLL generates a DC correction voltage. The PLL applies this correction voltage to the VCO through an analog gate. The analog gate closes when three conditions coexist: (1) The 5 MHz tests stable. (2) The PLL IC is programmed. (3) Two PLL oscillator and reference signal output alignments occur.

When the gate enables, the control voltage from the PLL can adjust the high-stability VCXO frequency. The adjustment can achieve a stability nearly equivalent to that of the external, 5 MHz frequency reference.

The correction voltage from the PLL continuously adjusts the VXCO frequency. The VXCO outputs a 16.8 MHz clock signal. The circuit applies this clock signal to the receiver, 48 MHz reference and TISIC.

The receivers use the 16.8MHz as the clock input and synthesizer reference.

The 48 MHz EXBRC synthesizer uses the 16.8 MHz as its synthesizer reference. The 48 MHz synthesizer output is the clock input for the TXDSP I and Q data reclock circuitry.

The TISIC divides the 16.8 MHz signal by seven, and outputs a 2.4 MHz signal. This output signal then becomes the 2.4 MHz reference for the Exciter.

Input Ports

One general-purpose input register provides for BRC and station circuit input signals. The register has 16 input ports. The Host Data Bus conveys input register data to the Host Microprocessor. Typical inputs include 16.8 and 48 MHz Station Reference Circuitry status outputs and reset status outputs.

Output Ports

Two general-purpose output registers distribute control signals from the Host Microprocessor to the BRC and station circuitry. One register has 32 output ports and the other register has 8 output ports. Control signal distribution occurs over the backplane. The Host Data Bus drives the output ports' latched outputs. Typical control signals include front-panel LED signals and SPI peripheral enable and address lines.

Remote Station Shutdown

The BRC contains power supply shutdown circuitry. This circuitry can send a shutdown pulse to the Base Radio Power Supply. BRC software generates the shutdown control pulse.

After receiving a shutdown pulse, the power supply turns off BR power. Shut down power sources include 3.3, 28.6 and 14.2 Vdc sources throughout the BR. Due to charges retained by BR storage elements, power supply voltages may not reach zero. The shutdown only assures that the host processor enters a power-on-reset state.

A remote site uses the shutdown function to perform a hard reset of all BR modules.

800 MHz QUAD Channel Base Radio Controller

800 MHz QUAD Channel Base Radio Controller Overview

The 800 MHz Base Radio Controller (BRC) provides signal processing and operational control for Base Radio modules. The BRC module consists of a printed circuit board, a slide-in housing, and associated hardware.

The BRC memory contains the operating software and codeplug. The software defines BR operating parameters, such as output power and operating frequency.

The BRC connects to the Base Radio backplane with one 168-pin FutureBus+ connector and one blindmate RF connector. Two Torx screws secure the BRC in the Base Radio chassis.

Figure 5 shows a top view of the EX/CNTL (model CLF1560) with the cover removed.

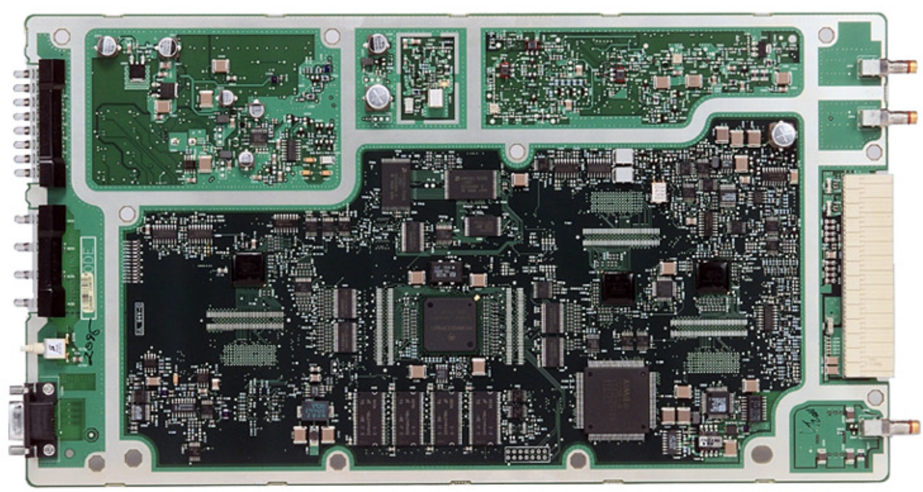


Figure 5 ***800 MHz QUAD Channel Base Radio Controller, version CLN1469 (with cover removed)***

800 MHz QUAD Channel Base Radio Controller Controls and Indicators

The BRC monitors the functions of other Base Radio modules. The LEDs on the front panel indicate the status of BRC-monitored modules. All LEDs on the BRC front panel normally flash three times upon initial power-up. A RESET switch allows a manual reset of the Base Radio. Figure 4 shows the front panel of the BRC.

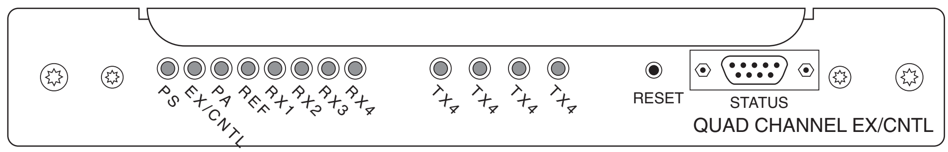


Figure 6 ***800 MHz QUAD Channel BR Controller (Front View)***

Indicators

Table 7 lists and describes the BRC LEDs.

Table 11 ***800 MHz QUAD Channel BR Controller Indicators***

LED	Color	Module Monitored	Condition	Indications
PS	Red	Power Supply	Solid (on)	FRU failure indication - Power Supply has a major alarm, and is out of service
			Flashing (on)	Power Supply has a minor alarm, and may be operating at reduced performance
			Off	Power Supply is operating normally (no alarms)
EXBRC	Red	Controller/ Exciter	Solid (on)	FRU failure indication - Controller/ Exciter has a major alarm, and is out of service (Note: Upon power-up of the BR, this LED indicates a failed mode until BR software achieves a known state of operation.)
			Flashing (on)	Controller/Exciter has a minor alarm, and may be operating at reduced performance
			Off	Controller/Exciter is operating normally (no alarms)
PA	Red	Power Amplifier	Solid (on)	FRU failure indication - PA has a major alarm, and is out of service
			Flashing (on)	PA has a minor alarm, and may be operating at reduced performance
			Off	PA is operating normally (no alarms)

Table 11 **800 MHz QUAD Channel BR Controller Indicators (Continued)**

LED	Color	Module Monitored	Condition	Indications
REF	Red	Controller Station Reference	Solid (on)	FRU failure indication - Controller Station Reference has a major alarm, and is out of service
			Flashing (on)	BRC has a minor alarm, and may be operating in a marginal region
			Off	BRC is operating normally (no alarms)
RX1 RX2 RX3 RX4	Red	Receiver #1, #2, #3, or #4	Solid (on)	FRU failure indication - Receiver (#1, #2, #3 or #4) has a major alarm, and is out of service
			Flashing (on)	Receiver (#1, #2, #3 or #4) has a minor alarm, and may be operating at reduced performance
			Off	Receiver (#1, #2, #3 or #4) is operating normally (no alarms)
TX1	Green	BR	Solid (on)	Station Transmit Carrier #1 is keyed
			Flashing (on)	Station Transmit Carrier #1 is not keyed
			Off	Station is out of service, or power is removed
TX2	Green	BR	Solid (on)	Station Transmit Carrier #2 is keyed
			Flashing (on)	Station Transmit Carrier #2 is not keyed
			Off	Station is out of service, or power is removed
TX3	Green	BR	Solid (on)	Station Transmit Carrier #3 is keyed
			Flashing (on)	Station Transmit Carrier #3 is not keyed
			Off	Station is out of service, or power is removed
TX4	Green	BR	Solid (on)	Station Transmit Carrier #4 is keyed
			Flashing (on)	Station Transmit Carrier #4 is not keyed
			Off	Station is out of service, or power is removed

Controls

Table 12 lists the controls and descriptions.

STATUS Connector

Table 13 the pin-outs for the STATUS connector.

Table 12 ***800 MHz QUAD Channel BR Controller Controls***

Control	Description
RESET Switch	A push-button switch used to manually reset the BR.
STATUS connector	A 9-pin connector used for connection of a service computer, providing a convenient means for testing and configuring.

Table 13 ***Pin-outs for the STATUS Connector***

Pin-out	Signal
1	not used
2	TXD
3	RXD
4	not used
5	GND
6	not used
7	not used
8	not used
9	not used

800 MHz QUAD Channel Base Radio Controller Theory of Operation

Table 14 briefly describes the BRC circuitry. Figure 13 is a functional block diagram of the BRC.

Host Microprocessor

The host microprocessor is the main controller for the BR. The processor operates at a 50-MHz clock speed. The processor controls Base Radio operation according to station software in memory. Station software resides in FLASH memory. For normal operation, the system transfers this software to non-volatile memory. An EEPROM contains the station codeplug.

NOTE

At BR power-up, the EXBRC LED indicates a major alarm. This indication continues until BR software achieves a predetermined state of operation. Afterward, the software turns off the EXBRC LED.

Serial Communication Buses

The microprocessor provides a general-purpose SMC serial management controller bus.

Table 14 ***BR Controller Circuitry***

Circuit	Description
Host Microprocessor	Contains integrated circuits that comprise the central controller of the BRC and station
Non-Volatile Memory	Consists of: • FLASH containing the station operating software • EEPROM containing the station codeplug data
Volatile Memory	Contains SDRAM to store station software used to execute commands.
Ethernet Interface	Provides the BRC with a 10Base2 Ethernet communication port to network both control and compressed voice data
RS-232 Interface	Provides the BRC with an RS-232 serial interface
Digital Signal Processors	Performs high-speed modulation/demodulation of compressed audio and signaling data
TISIC	Contains integrated circuits that provide timing reference signals for the station
TX Reclock	Contains integrated circuits that provide highly stable, reclocked transmit signals and peripheral transmit logic
RX DSP SPI	Contains integrated circuits that provide DSP SPI capability and peripheral receive logic
Station Reference Circuitry	Generates the 16.8 MHz and 48 MHz reference signals used throughout the station
Input Ports	Contains 16 signal input ports that receive miscellaneous inputs from the BR
Output Ports	Contains 40 signal output ports, providing a path for sending miscellaneous control signals to circuits throughout the BR
Remote Station Shutdown	Provides software control to cycle power on the BR

The SMC serial communications bus is an asynchronous RS-232 interface with no hardware handshake capability. The BRC front panel includes a nine-pin, D-type connector. This connector provides a port where service personnel may connect a service computer. Service personnel can perform programming and maintenance tasks via Man-Machine Interface (MMI) commands. The interface between the SMC port and the front- panel STATUS connector is via EIA-232 Bus Receivers and Drivers.

MPC860 Host Processor

The MPC860 microprocessor incorporates 4k bytes of instruction cache and 4k bytes of data cache that significantly enhance processor performance.

The microprocessor has a 32-line address bus. The processor uses this bus to access non-volatile memory and SDRAM memory. Via memory mapping, the processor also uses this bus to control other BRC circuitry.

The microprocessor uses its Chip Select capability to decode addresses and assert an output signal. The eight chip-select signals select non-volatile memory, SDRAM memory, input ports, output ports, and DSPs.

The Host processor...

- Provides serial communications between the Host Microprocessor and other Base Radio modules.
- Provides condition signals necessary to access SDRAM.
- Accepts interrupt signals from BRC circuits (such as DSPs).
- Organizes the interrupts, based on hardware-defined priority ranking.
- The Host supports several internal interrupts from its Communications Processor Module. These interrupts allow efficient use of peripheral interfaces.
- The Host supports 10 Mbps Ethernet/IEEE 802.3.
- Provides a 32-line data bus transfers data to and from BRC SDRAM and other BRC circuitry. Buffers on this data bus allow transfers to and from non-volatile memory, general input and output ports and DSPs.

Non-Volatile Memory

Base Radio software resides in 2M x 32 bits of FLASH memory. The Host Microprocessor addresses the FLASH memory with 20 of the host address bus' 32 lines. The host accesses FLASH data over the 32-line host data bus. A host-operated chip-select line provides control signals for these transactions.

The FLASH contains the operating system and application code. The system stores application code in FLASH for fast recovery from reset conditions. Application code transfers from network or site controllers may occur in a background mode. Background mode transfers allow the station to remain operational during new code upgrades.

The data that determines the station personality resides in a 32K x eight bit codeplug EEPROM. The microprocessor addresses the EEPROM with 15 of the host address bus' 32 lines. The host accesses EEPROM data with eight of the data bus' 32 lines. A host-operated chip-select line provides control signals for these transactions.

During the manufacturing process, the factory programs the codeplug's default data. The BRC must download field programming data from network and site controllers. This data includes operating frequencies and output power level. The station permits adjustment of many station parameters, but the station does not store these adjustments. Refer to the Software Commands chapter for additional information.

Volatile Memory

Each BRC contains 8MB x 32 bits of SDRAM. The BRC downloads station software code into SDRAM for station use. SDRAM also provides short-term storage for data generated and required during normal operation. SDRAM is volatile memory. A loss of power or system reset destroys SDRAM data.

The system performs read and write operations over the Host Address and Data buses. These operations involve column and row select lines under control of the

Host processor's DRAM controller. The Host address bus and column row signals sequentially refresh SDRAM memory locations.

Ethernet Interface

The Host processor's Communications Processor Module (CPM) provides the Local Area Network (LAN) Controller for the Ethernet Interface. The LAN function implements the CSMA/CD access method, which supports the IEEE 802.3 10Base2 standard.

The LAN coprocessor supports all IEEE 802.3 Medium Access Control, including the following:

- ❒ framing
- ❒ preamble generation
- ❒ stripping
- ❒ source address generation
- ❒ destination address checking

The PCM LAN receives commands from the CPU.

The Ethernet Serial Interface works directly with the CPM LAN to perform the following major functions:

- ❒ 10 MHz transmit clock generation (obtained by dividing the 20 MHz signal provided by on-board crystal)
- ❒ Manchester encoding/decoding of frames
- ❒ electrical interface to the Ethernet transceiver

An isolation transformer provides high-voltage protection. The transformer also isolates the Ethernet Serial Interface (ESI) and the transceiver. The pulse transformer has the following characteristics:

- ❒ Minimum inductance of 75 µH
- ❒ 2000 V isolation between primary and secondary windings
- ❒ 1:1 Pulse Transformer

The Coaxial Transceiver Interface (CTI) is a coaxial cable line driver and receiver for the Ethernet. CTI provides a 10Base2 connection via a coaxial connector on the board. This device minimizes the number of external components necessary for Ethernet operations.

A DC/DC converter provides a constant voltage of -9 Vdc for the CTI from a 3.3 Vdc source.

The CTI performs the following functions:

- ❒ Receives and transmits data to the Ethernet coaxial connection
- ❒ Reports any collision that it detects on the coaxial connection
- ❒ Disables the transmitter when packets are longer than the legal length (Jabber Timer)

Digital Signal Processors

The BRC includes two Receive Digital Signal Processors (RXDSPs) and a Transmit Digital Signal Processor (TXDSP). These DSPs and related circuitry process compressed station transmit and receive audio or data. The related circuitry includes the TDMA Infrastructure Support IC (TISIC) and the TISIC Interface Circuitry. The DSPs only accept input and output signals in digitized form.

The RXDSP inputs are digitized receiver signals. The TXDSP outputs are digitized voice audio and data (modulation signals). These signals pass from the DSP to the Exciter portion of the EXBRC. DSPs communicate with the Microprocessor via an eight-bit, host data bus on the host processor side. For all DSPs, interrupts drive communication with the host.

The RXDSPs operate from an external 16.8 MHz clock, provided by the local station reference. The RXDSP internal operating clock signal is 150MHz, produced by an internal Phase-Locked Loop (PLL).

The RXDSPs accept digitized signals from the receivers through Enhanced Synchronous Serial Interface (ESSI) ports. Each of two ESSI ports on a RXDSP supports a single carrier (single receiver) digital data input. The DSP circuitry includes two RXDSPs. These allow processing of up to four carriers (four receivers).

The RXDSP accesses its DSP program and signal-processing algorithms in 128k words of internal memory. The RXDSPs communicate with the host bus over an 8-bit interface.

Each RXDSP provides serial communications to its respective receiver module for receiver control via a Serial Peripheral Interface (SPI). The SPI is a parallel-to-serial conversion circuit, connected to the RXDSP data bus. Each RXDSP communicates to two receive modules through this interface.

Additionally, a serial control path connects the two RXDSPs and the TXDSP. The Synchronous Communications Interface (SCI) port facilitates this serial control path.

For initialization and control purposes, one RXDSP connects to the TISIC device.

The TXDSP operates at an external clock speed of 16.8 MHz, provided by the EXBRC local station reference. The TXDSP internal operating clock is 150MHz, produced by an internal Phase Lock Loop (PLL).

The TXDSP sends up to four carriers of digitized signal to the EX11 exciter. The exciter converts the digital signal to analog. Also at the exciter, a highly stable clock reclocks the digital data. Reclocking enhances transmit signal integrity. Two framed and synchronized data streams result. One data stream is I-data, and the other is the Q-data stream.

The TXDSP contains its own, internal address and data memory. The TXDSP can store 128k words of DSP program and data memory. An eight-bit interface handles TXDSP-to-host bus communications.

TISIC

The TISIC controls internal DSP operations. This circuit provides the following functions:

- For initialization and control, interfaces with one RXDSP via the DSP address and data buses.
- Accepts a 16.8 MHz signal from Station Reference Circuitry.
- Accepts a 5 MHz signal, modulated with one pulse per second (1 PPS) from the site reference.
- Demodulates the 1 PPS
- Outputs a 1 PPS signal and a windowed version of this signal for network timing alignment.
- Outputs a 2.4 MHz reference signal used by the Exciter.
- Generates 15 ms and 7.5 ms ticks. (These ticks synchronize to the 1 PPS time mark. The system decodes the time mark from the site reference. Then the system routes the reference to the TXDSP and RXDSPs.)

Station Reference Circuitry

The Station Reference Circuitry is a phase-locked loop (PLL). This PLL consists of a high-stability, Voltage-Controlled, Crystal Oscillator (VCXO) and a PLL IC. GPS output from the iSC connects to the 5 MHz/1 PPS BNC connector on the BR backplane. Wiring at this connector routes signals to EXBRC station reference circuitry.

The PLL compares the 5 MHz reference frequency to the 16.8 MHz VCXO output. Then the PLL generates a DC correction voltage. The PLL applies this correction voltage to the VCO through an analog gate. The analog gate closes when three conditions coexist: (1) The 5 MHz tests stable. (2) The PLL IC is programmed. (3) Two PLL oscillator and reference signal output alignments occur.

A loss of the 5 MHz/1PPS signal causes the control voltage enable switch to open. This permits the PLL to free run, which allows the BR to retain a clock for control purposes.

When the gate enables, the control voltage from the PLL can adjust the high-stability VCXO frequency. The adjustment can achieve a stability nearly equivalent to that of the external, 5 MHz frequency reference.

The correction voltage from the PLL continuously adjusts the VXCO frequency. The VXCO outputs a 16.8 MHz clock signal. The circuit applies this clock signal to the receiver, 48 MHz reference and TISIC.

The receivers use the 16.8MHz as the clock input and synthesizer reference.

The 48 MHz EXBRC synthesizer uses the 16.8 MHz as its synthesizer reference. The 48 MHz synthesizer output is the clock input for the TXDSP I and Q data reclock circuitry.

The TISIC divides the 16.8 MHz signal by seven, and outputs a 2.4 MHz signal. This output signal then becomes the 2.4 MHz reference for the Exciter.

Input Ports

One general-purpose input register provides for BRC and station circuit input signals. The register has 16 input ports. The Host Data Bus conveys input register data to the Host Microprocessor. Typical inputs include 16.8 and 48 MHz Station Reference Circuitry status outputs and reset status outputs.

Output Ports

Two general-purpose output registers distribute control signals from the Host Microprocessor to the BRC and station circuitry. One register has 32 output ports and the other register has 8 output ports. Control signal distribution occurs over the backplane. The Host Data Bus drives the output ports' latched outputs. Typical control signals include front-panel LED signals and SPI peripheral enable and address lines.

Remote Station Shutdown

The BRC contains power supply shutdown circuitry. This circuitry can send a shutdown pulse to the Base Radio Power Supply. BRC software generates the shutdown control pulse.

After receiving a shutdown pulse, the power supply turns off BR power. Shut down power sources include 3.3, 28.6 and 14.2 Vdc sources throughout the BR. Due to charges retained by BR storage elements, power supply voltages may not reach zero. The shutdown only assures that the host processor enters a power-on-reset state.

A remote site uses the shutdown function to perform a hard reset of all BR modules.

800 MHz Legacy Base Radio Controller

800 MHz Legacy Base Radio Controller Overview

The Base Radio Controller (BRC) serves as the main controller for the Base Radio. The BRC provides signal processing and operational control for other Base Radio modules. Figure 7 shows a top view of the BRC with the cover removed. The BRC module consists of two printed circuit boards (BRC board and LED/display board), a slide-in housing, and associated hardware.

The operating software and codeplug are contained within the BRC memory. The software defines operating parameters for the BR, such as output power and operating frequency.

The BRC interconnects to the Base Radio backplane using one 96-pin DIN connector and one blindmate RF connector. The BRC is secured in the Base Radio chassis using two Torx screws.F

There are two different BRC modules that serve as the main controller for the 1500 MHz Base Radio. The standard model is the same module used in the 800 MHz Base Radio. The model CLN1472 contains an additional Digital Signal Processing power for applications requiring a modified error correction routine (available for a specific customers only). Figure 8 shows a top view of the BRC (model CLN1472) with the cover removed.

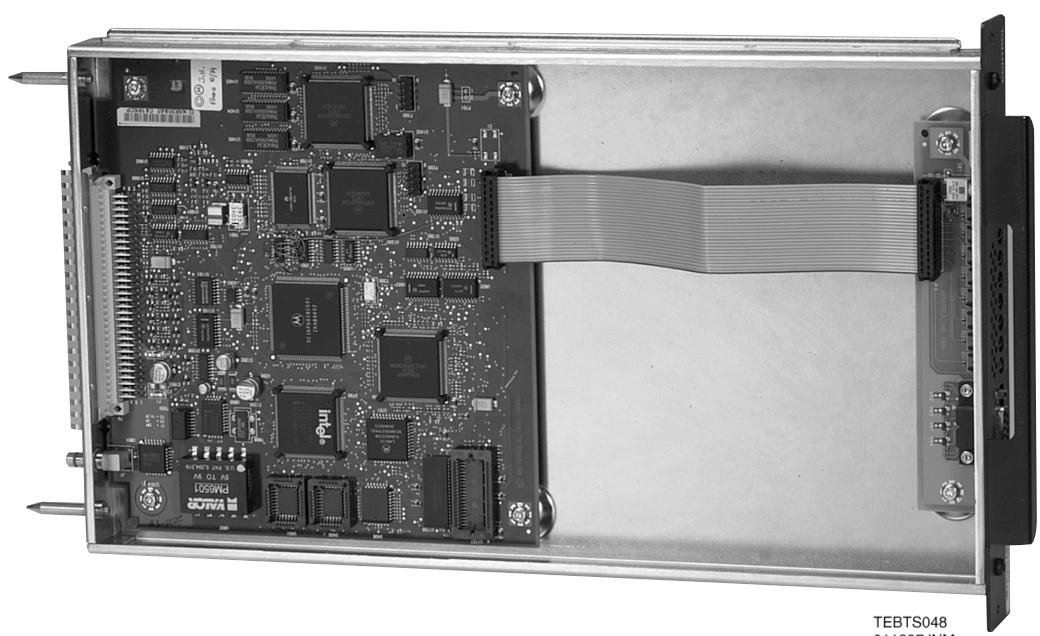
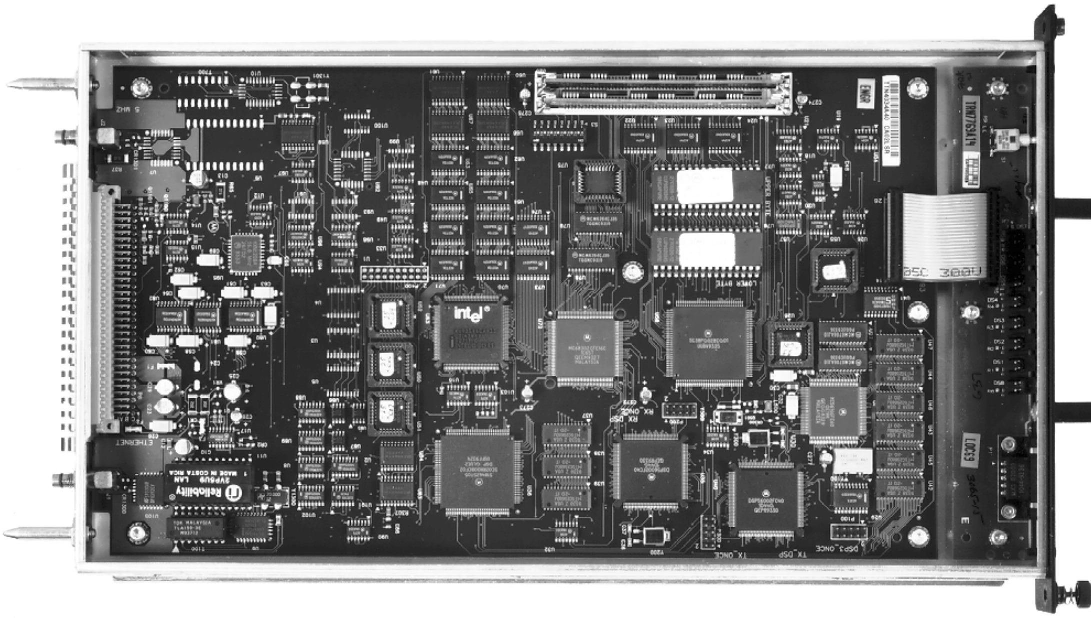


Figure 7 ***Legacy Base Radio Controller, version CLN1469 (with cover removed)***

800 MHz Legacy Base Radio Controller



1.5GHZ-A859

Figure 8 ***Legacy Base Radio Controller, version CLN1472 (with cover removed)***

800 MHz Legacy Base Radio Controller Controls and Indicators

The BRC monitors the functions of other Base Radio modules. The LEDs on the front panel indicate the status of the modules monitored by the BRC. All LEDs on the BRC front panel normally flash on/off three times upon initial power-up. A RESET switch is provided to allow a manual reset of the Base Radio. Figure 9 shows the front panel of the BRC.

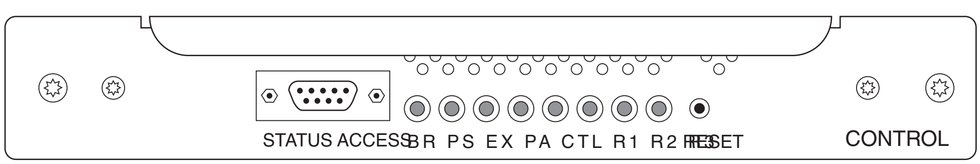


Figure 9 ***Legacy BR Controller (Front View)***

Indicators

Table 15 lists and describes the BRC LEDs.

Table 15 ***Legacy BR Controller Indicators***

LED	Color	Module Monitored	Condition	Indications
BR	Green	BR	Solid (on)	Station is keyed
			Flashing (on)	Station is not keyed
			Off	Station is out of service or power is removed
PS	Red	Power Supply	Solid (on)	FRU failure indication - Power Supply has a major alarm and is out of service
			Flashing (on)	Power Supply has a minor alarm and may be operating at reduced performance
			Off	Power Supply under normal operation (no alarms)
EX	Red	Exciter	Solid (on)	FRU failure indication - Exciter has a major alarm and is out of service
			Flashing (on)	Exciter has a minor alarm and may be operating at reduced performance
			Off	Exciter under normal operation (no alarms)
PA	Red	Power Amplifier	Solid (on)	FRU failure indication - PA has a major alarm and is out of service
			Flashing (on)	PA has a minor alarm and may be operating at reduced performance
			Off	PA under normal operation (no alarms)
CTL	Red	Controller	Solid (on)	FRU failure indication - BRC has a major alarm and is out of service
			Flashing (on)	BRC has a minor alarm and may be operating at reduced performance
			Off	BRC under normal operation (no alarms)
R1 R2 R3	Red	Receiver #1, #2, or #3	Solid (on)	FRU failure indication - Receiver (#1, #2, or #3) has a major alarm and is out of service
			Flashing (on)	Receiver (#1, #2, or #3) has a minor alarm and may be operating at reduced performance
			Off	Receiver (#1, #2, or #3) under normal operation (no alarms)

Controls

Table 16 lists the controls and descriptions.

STATUS Connector

Table 17 the pin-outs for the STATUS connector.

Table 16 ***Legacy BR Controller Controls***

Control	Description
RESET Switch	A push-button switch used to manually reset the BR.
STATUS connector	A 9-pin connector used for connection of a service computer, providing a convenient means for testing and configuring.

Table 17 ***Pin-outs for the STATUS Connector***

Pin-out	Signal
1	CD
2	TXD
3	RXD
4	not used
5	GND
6	not used
7	CTS
8	RTS
9	not used

800 MHz Legacy Base Radio Controller Theory of Operation

Table 18 briefly describes the BRC circuitry. Figures 10 through 12 are functional block diagrams of the BRC.

Host Microprocessor

The host microprocessor serves as the main controller for the BR. It operates at a clock speed of 16.5 MHz that is supplied from the Host Glue ASIC. The processor controls the operation of the Base Radio as determined by the station software contained in non-volatile memory. The station software is contained in two EPROMs. The station codeplug is stored in EEPROM.

Serial Communication Buses

The microprocessor provides a general-purpose SCC2 serial communications bus.

The SCC2 serial communications bus is an asynchronous RS-232 interface. A 9-pin D-type connector on the BRC front panel provides a port for service personnel to connect a service computer. A service computer allows the downloading of application code or diagnostic software. Service personnel can perform programming and maintenance tasks via Man Machine Interface (MMI) commands. The interface between the SCC2 port and the front panel STATUS connector is via EIA-232 Bus Receivers/Drivers.

Table 18 ***Legacy BR Controller Circuitry***

Circuit	Description
Host Microprocessor and Host Glue ASIC	Contains two integrated circuits that comprise the central controller of the BRC and station
Non-Volatile Memory	Consists of: • EPROMs containing the station operating software • one EEPROM containing the station codeplug data
Volatile Memory	Contains DRAM to store station software used to execute commands. Contains SRAM for general data space used by the host microprocessor
Ethernet Interface	Provides the BRC with a 10Base2 Ethernet communication port to network both control and compressed voice data
RS-232 Interface	Provides the BRC with two independent RS-232 serial interfaces
Digital Signal Processors and TISIC	Performs high-speed modulation/demodulation of compressed audio and signaling data
Station Reference Circuitry	Generates the 16.8 MHz and 2.1 MHz reference signal used throughout the station
Input Ports	Contains two 16-line input buses that receive miscellaneous inputs from the BR
Output Ports	Contains three 16-line output buses providing a path for sending miscellaneous control signals to various circuits throughout the BR
Remote Station Shutdown	Provides software control to cycle power on the BR

Address and Data Bus

The microprocessor is equipped with a 23-line address bus used to access the non-volatile memory, DRAM memory, and provide control via memory mapping for other circuitry in the BRC.

A 16-line data bus transfers data to/from the BRC memory, as well as other BRC circuitry. This data bus is buffered for transfers to and from the non-volatile and DRAM memory.

Host Glue ASIC

The Host Microprocessor controls the operations of the Host Glue ASIC which performs the functions described Table 19.

Non-Volatile Memory

The Base Radio software resides in two 512K x 8 EPROMs. These EPROMs are accessed by the Host Microprocessor via the 19 lines of the 23-line host address bus and the 16-line host data bus.

The data determining the station personality resides in an 8K x 8 codeplug EEPROM. The EEPROM is accessed by the microprocessor via 15 lines of the 23-line host address bus and the 16-line data bus.

Table 19 ***Host Glue ASIC Functions***

Function	Description
SPI Bus	Serves as a general-purpose serial communications bus providing communications between the Host Microprocessor and other Base Radio modules
DRAM Controller	Provides signals necessary to access and refresh the DRAM memory
System Reset	Generates a BRC Reset upon power up
Host Microprocessor Clock	Buffers the 33 MHz crystal outputs, performs a divide-by-2, and outputs a clock signal for the Host Microprocessor at 16.5 MHz
Address Decoding	Provides decoding of addressing from Host Microprocessor and generates corresponding chip select signals for various BRC devices, such as DRAM, EPROM, I/O Ports, DSPs, and internal Host Glue ASIC registers
Interrupt Controller	Accepts interrupt signals from various BRC circuits (such as the DSPs), prioritizes the interrupts based on hardware-defined priority ranking, and sends interrupt and priority level information to Host Microprocessor (via IPL lines 1-3)

Stations are manufactured with default data programmed into the codeplug. Field programming information is downloaded from the network/site controllers. This data includes operating frequencies and output power level. Many of the station parameters may be adjusted but will not be stored within the station. Refer to the Software Commands section of this manual for additional information.

Volatile Memory

Each BRC contains 2MB of DRAM. The BRC downloads the station software code into DRAM for the station to use. Data is lost upon loss of power or reset since the DRAM is volatile memory.

The DRAM also provides short-term storage for data generated and required during normal operation. Read and write operations are performed via the Host Address and Data buses in conjunction with column and row select lines that are controlled by the Host Glue ASIC. DRAM memory locations are sequentially refreshed by the address bus and column row signals from the Host Glue ASIC during normal operation.

Two 32K x 8 fast Static RAM (SRAM) ICs are also provided on the BRC. The SRAM is accessed by the Microprocessor via 15 lines of the 23-line Host Address Bus and the 16-line Data Bus.

Ethernet Interface

The Local Area Network (LAN) Controller for the Ethernet Interface is provided by a 32-bit address, 16-bit data LAN coprocessor. The LAN coprocessor implements the CSMA/CD access method which supports the IEEE 802.3 10Base2 standard. The LAN coprocessor communicates to the Host Microprocessor via DRAM. Of the LAN coprocessor’s 32 address lines, 22 are used for the Ethernet interface.

The LAN coprocessor supports all IEEE 802.3 Medium Access Control, including the following:

- framing
- preamble generation
- stripping
- source address generation
- destination address checking

The LAN coprocessor receives commands from the CPU by reading a specified block in memory. Internal FIFOs of the LAN Controller optimize the microprocessor bus performance.

In addition, the on-chip Direct Memory Access (DMA) controller of the LAN coprocessor transfers data blocks (buffers and frames) from Ethernet to DRAM. This automatic transfer of data by the LAN coprocessor relieves the host CPU of byte transfer overhead.

The Ethernet Serial Interface works directly with the LAN coprocessor to perform the following major functions:

- 10 MHz transmit clock generation (obtained by dividing the 20 MHz signal provided by on board crystal)
- Manchester encoding/decoding of frames
- electrical interface to the Ethernet transceiver

An isolation transformer provides high voltage protection and isolates the Ethernet Serial Interface (ESI) and the transceiver. The pulse transformer has the following characteristics:

- Minimum inductance of 75 μH
- 2000 V isolation between primary and secondary windings
- 1:1 Pulse Transformer

The Coaxial Transceiver Interface (CTI) is a coaxial cable line driver/receiver for the Ethernet. CTI provides a 10Base2 connection via a coaxial connector on the board. This device minimizes the number of external components necessary for Ethernet operations.

A DC/DC converter provides a constant voltage of -9 VDC for the CTI from a 5 VDC source.

The CTI performs the following functions:

- Receives and transmits data to the Ethernet coaxial connection
- Reports any collision detected on the coaxial
- Disables the transmitter when packets are longer than the legal length (Jabber Timer)

Digital Signal Processors

The Receive Digital Signal Processor (RXDSP), Transmit Digital Signal Processor (TXDSP), and related circuitry process the station transmit and receive compressed audio/data. This circuitry includes the RXDSP and TXDSP, the TDMA Infrastructure Support IC (TISIC), and the TISIC Interface Circuitry. All signals input to or output from the DSP are in digitized format.

The inputs are digitized receive signals from the Receivers. The outputs are digitized voice audio/data (modulation signals) that are sent from the DSP to the Exciter. The DSPs communicate with the Microprocessor via an 8-bit host data bus on the Host Processor side. Communication is interrupt driven for all DSPs.

The RXDSP operates from a 40 MHz clock provided by an on-board crystal. The RXDSP accepts redigitized signal from the receivers. The RXDSP provides address and data buses to receive digitized audio from the TISIC.

The RXDSP also accesses its DSP program and signal processing algorithms contained in three 32K x 8 SRAM ICs. The RXDSP communicates with the host bus via an 8-bit interface.

Additionally, there is a serial data path to the TXDSP via the Synchronous Serial Interface (SSI) port. A serial control path is also provided from the TXDSP via the Serial Communications Interface (SCI) port.

The TXDSP also operates at a clock speed of 40 MHz, provided by a clock oscillator. The TXDSP sends the digitized signal to the TISIC where it is then passed to the Exciter.

The TXDSP contains its own address and data bus to access its DSP program and signal processing algorithms contained in local memory. The TXDSP memory consists of six 32K x 8 SRAM ICs. The TXDSP communicates with the host bus via an 8-bit interface.

Error Correction Digital Signal Processor *(CLN1472 Only)*

The Error Correction Digital Signal Processor (U30) used in the Model CLN1472 operates at a clock speed of 60 MHz. An on-board oscillator (Y100) operating at 10 MHz is multiplied internal to the ECDSP to generate the required clock signal.

The main function of the Error Correction Digital Signal Processor (ECDSP) is decoding. It accepts data from the Synchronous Serial Interface (SSI) bus. Various algorithms are performed on the signal before it is sent to the TXDSP via the SSI bus.

The ECDSP contains its own address and data bus to access its DSP program and signal processing algorithms contained in local memory. Two 32K x 8 SRAM ICs (U27 and U31) comprise the ECDSP memory. The ECDSP communicates with the host bus via an 8-bit interface.

TISIC

The TISIC controls all internal DSP operations. This circuit provides a number of functions, including the following:

- Interfaces with the DSPs via the DSP address and data buses.
- Accepts a 16.8 MHz signal and a 1 PPS signal from Station Reference Circuitry.
- Outputs a 2.1 MHz reference signal used by the Exciter and Receivers.
- Outputs a 4.8 MHz reference signal used by the Exciter to clock data into the TRANLIN IC.
- Accepts differential data from Receiver (RX1 through RX3) via interface circuitry.
- Accepts and sends serial data from the Receiver (RX1 through RX3) via serial data bus.
- Accepts and formats differential data from the TXDSP for transmission to the Exciter via interface circuitry.
- Generates 15 ms and 7.5 ms ticks. These are synchronized to the 1 PPS time mark from the iSC for routing to the TXDSP and RXDSP, respectively.
- Generates the Receive SSI (RXSSI) frame sync interrupt for the RXDSP.

Station Reference Circuitry

The Station Reference Circuitry is a phase-locked loop consisting of a high-stability Voltage Controlled Crystal Oscillator (VCXO) and a Phase Locked Loop IC. The GPS output from the iSC is connected to the 5 MHz/1 PPS A BNC connector on the EBTS junction panel. In this mode, the PLL compares the reference frequency to the 16.8 MHz VCXO output and generates a DC correction voltage. The control voltage enable switch is closed. This allows the control voltage from the PLL to adjust the high-stability VCXO frequency to a stability equivalent to that of the external 5 MHz frequency reference.

The VXCO is continually frequency-controlled by the control voltage from the PLL and outputs a 16.8 MHz clock signal which is applied to the TISIC.

The TISIC divides the 16.8 MHz signal by 8 and outputs a 2.1 MHz signal. This signal is separated and buffered by a splitter. The output signal is then sent to the Exciter and Receivers as a 2.1 MHz reference via the backplane.

The 4.8 MHz reference signal generated by the TISIC is applied to the Exciter module, where it is used to clock data into and out of the TRANLIN IC.

Input Ports

Two general purpose, 16-line input ports provide for various input signals from the BRC and station circuitry. These inputs are sent to the Host Microprocessor.

Input Port P0 In and Port P1 In each consist of 16 lines from circuitry in the BRC, as well as other modules in the station via the backplane. The buses communicate with the buffers to make data available to the Host Microprocessor via the Host Data Bus. The DIP switch and the Station Reference Circuitry are typical inputs for these ports.

Output Ports

Three general purpose 16-line output ports provide various control signals from the Host Microprocessor to the BRC and station circuitry via the backplane.

The three output ports, Port P0 Out through Port P2 Out, each consist of 16 lines from the Host Data Bus via latches.

Typical control signals from these output ports vary from the control signals for the eight front panel LEDs and the address select lines for SPI peripherals.

Remote Station Shutdown

The BRC contains circuitry to send a shutdown pulse to the Base Radio Power Supply. After receiving this pulse, the power supply cycles the power for the BR, including the 5.1 VDC, 28.6 VDC and 14.2 VDC distributed through the BR. The BRC generates the shutdown pulse through software control. A remote site uses the shutdown function to perform a hard reset of all modules in the BR.

Base Radio Controller

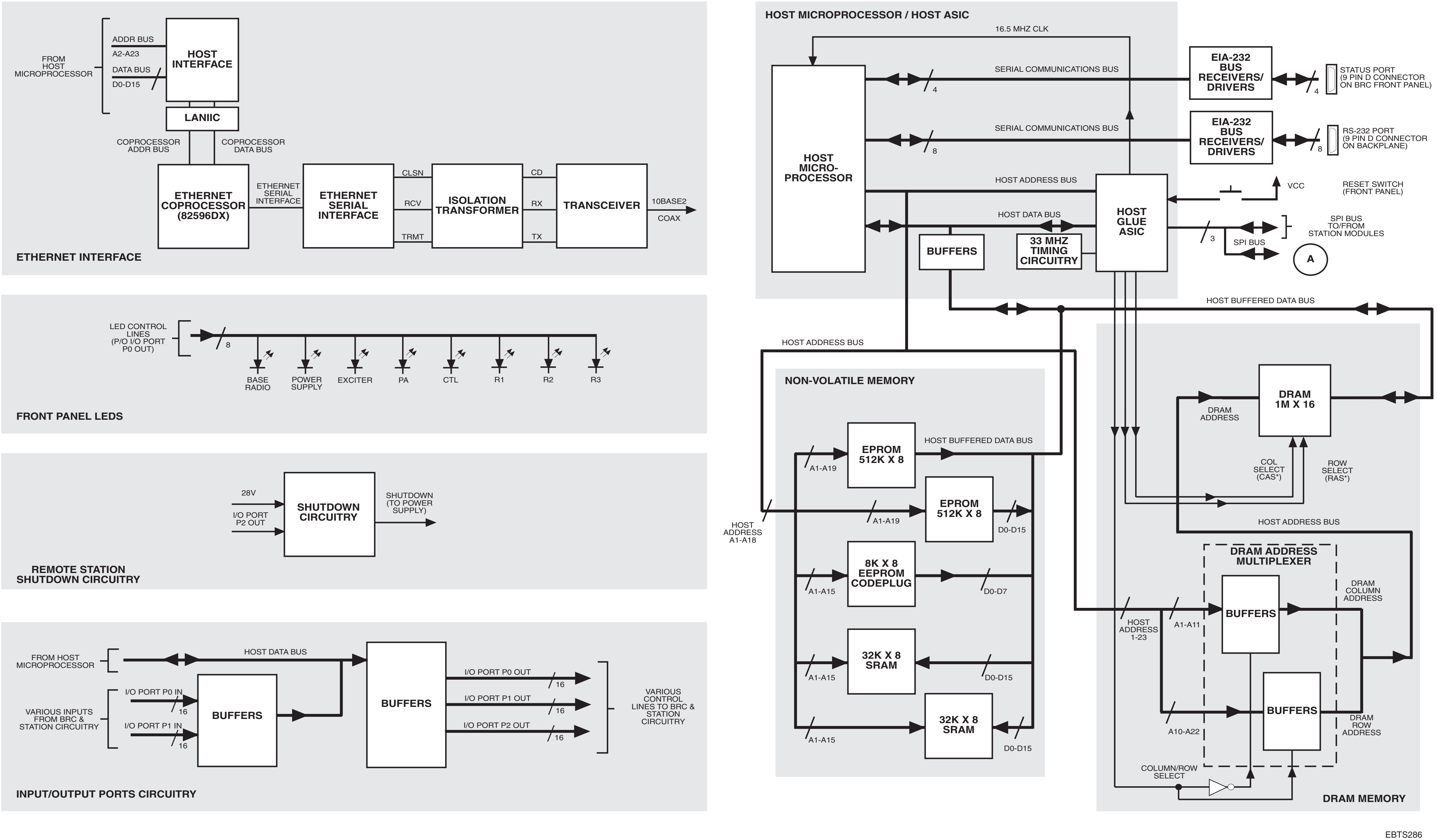


Figure 10 ***800/900 MHz Base Radio Controller Functional Block Diagram (Sheet 1 of 2)***

Base Radio Controller

Functional Block Diagram
Model TLN3424
(Includes Front Panel Board)

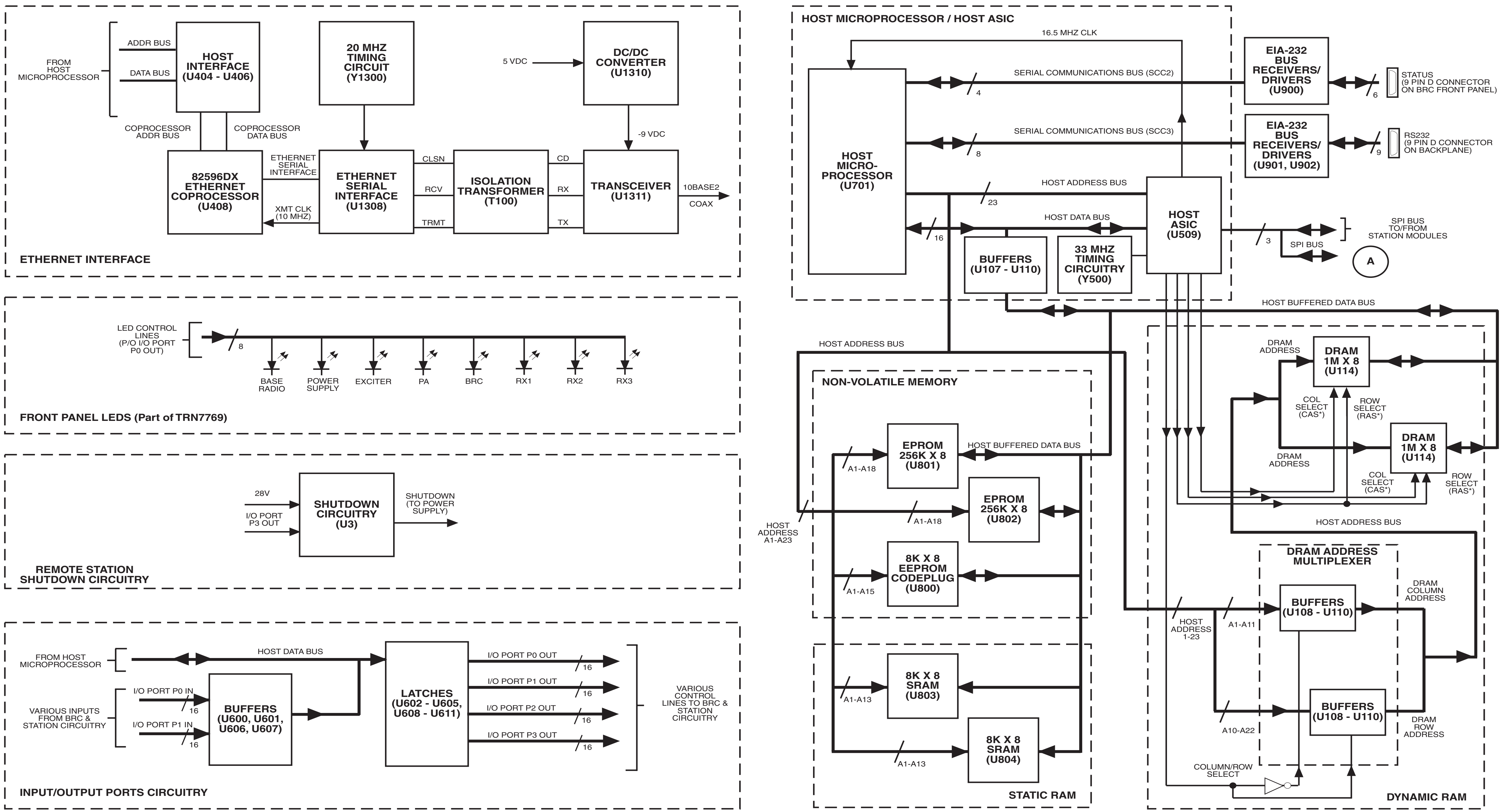


Figure 10 ***800/900 MHz QUAD Channel Base Radio Functional Block Diagram Sheet 2 of 2)***

Base Radio Controller

Functional Block Diagram
Model TLN3425
(Includes Front Panel Board)

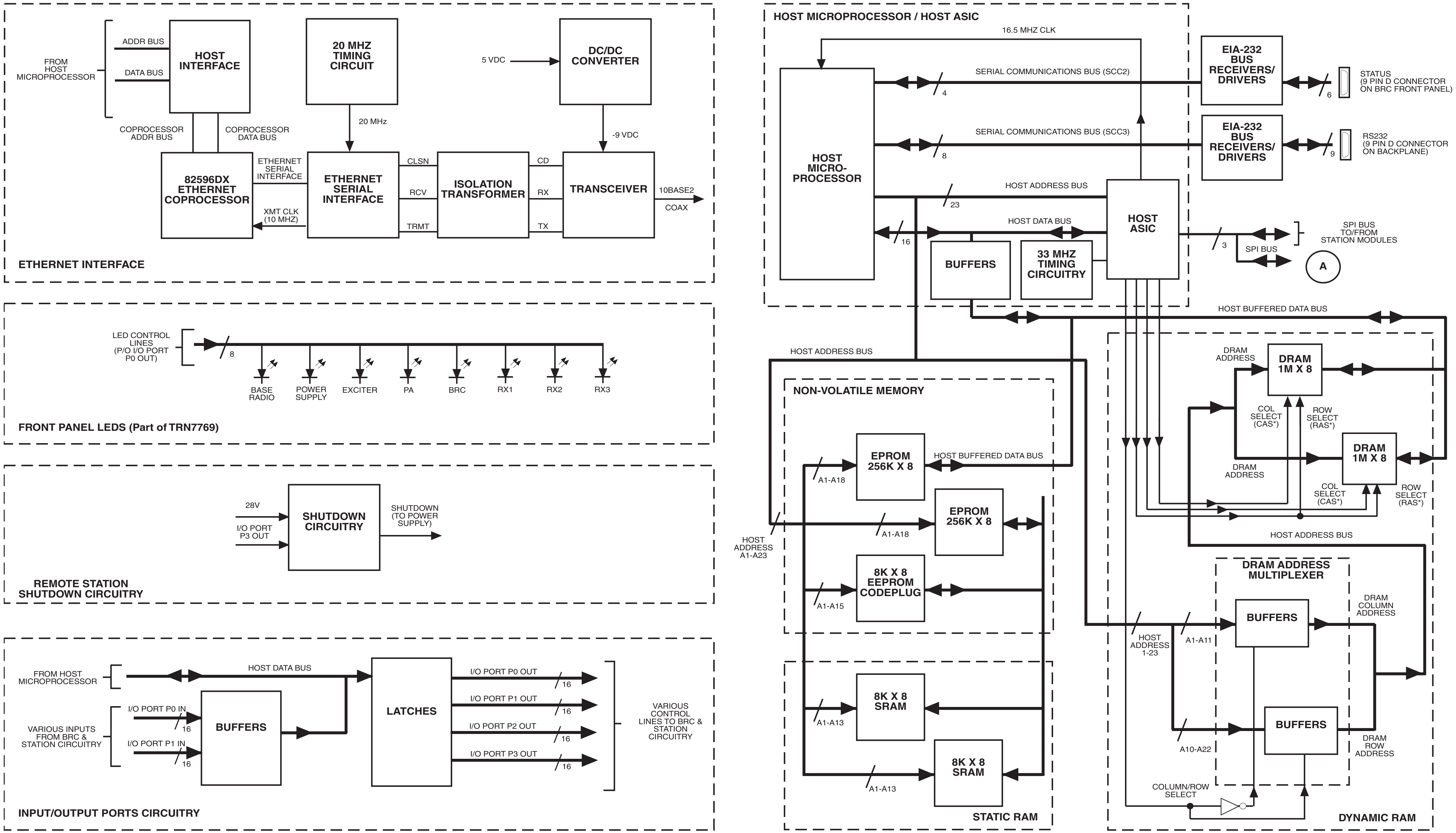


Figure 11 ***1500 MHz Base Radio Controller Functional Block Diagram (Sheet 1 of 2)***

Base Radio Controller

Functional Block Diagram
Model TLN3425
(Includes Front Panel Board)

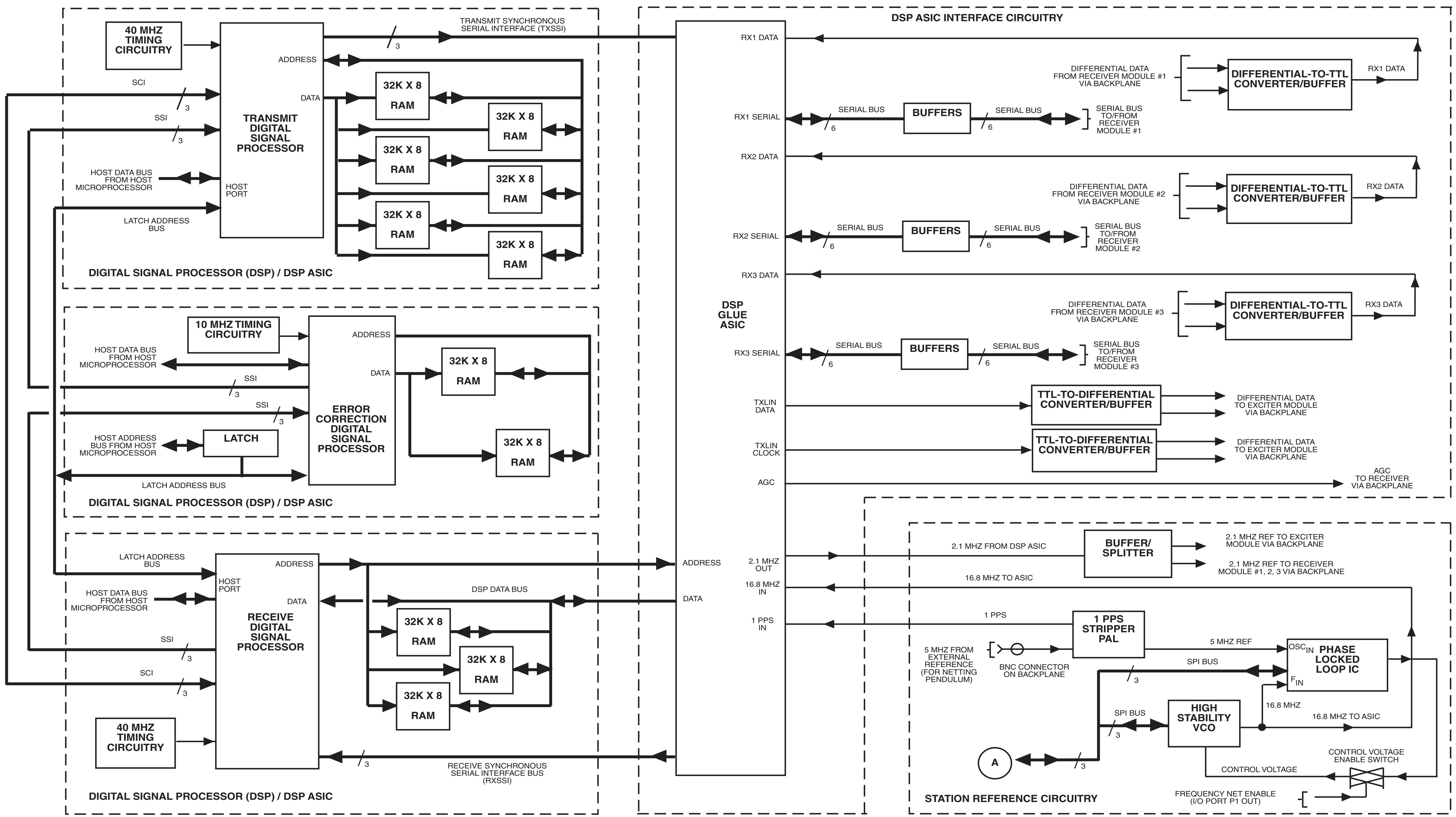


Figure 12 ***1500 MHz Base Radio Controller Functional Block Diagram (Sheet 2 of 2)***

QUAD Channel Base Radio Controller

Functional Block Diagram

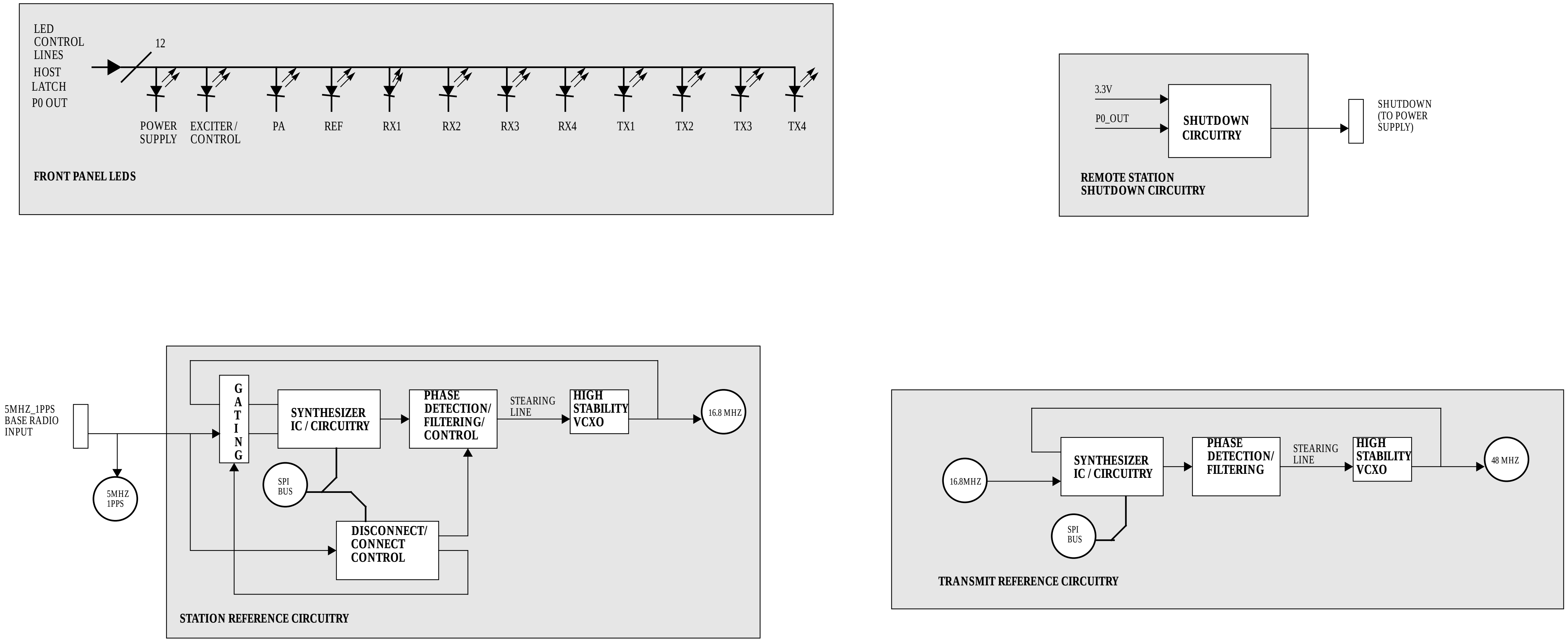


Figure 13 ***800 and 900 MHz QUAD Channel Base Radio Controller Functional Block Diagram (Sheet 1 of 2)***

QUAD Channel Base Radio Controller

Functional Block Diagram

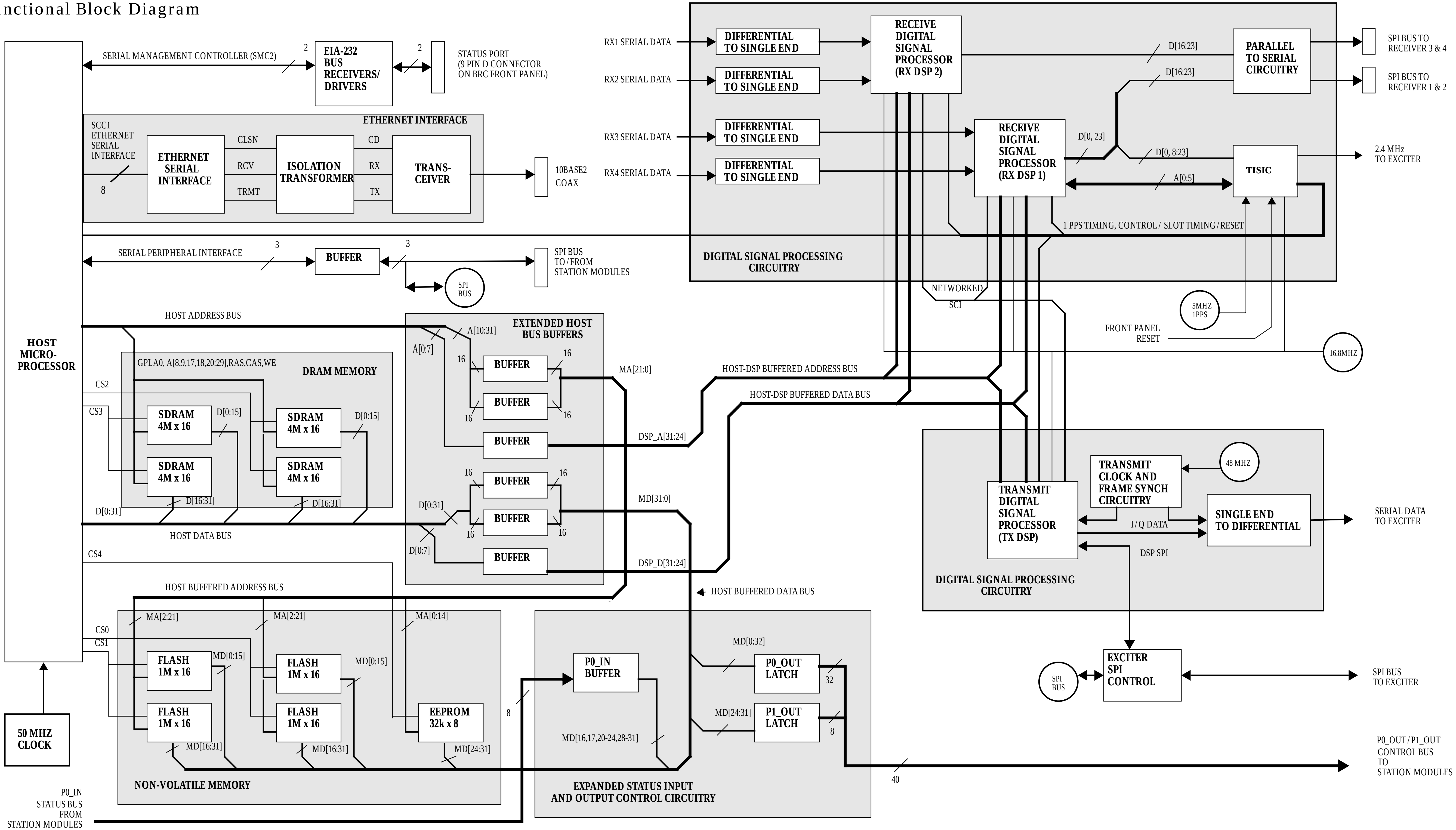


Figure 14 ***800 and 900 MHz QUAD Channel Base Radio Controller Functional Block Diagram (Sheet 2 of 2)***

Enhanced Base Radio Controller

Functional Block Diagram
Model CLN1653A

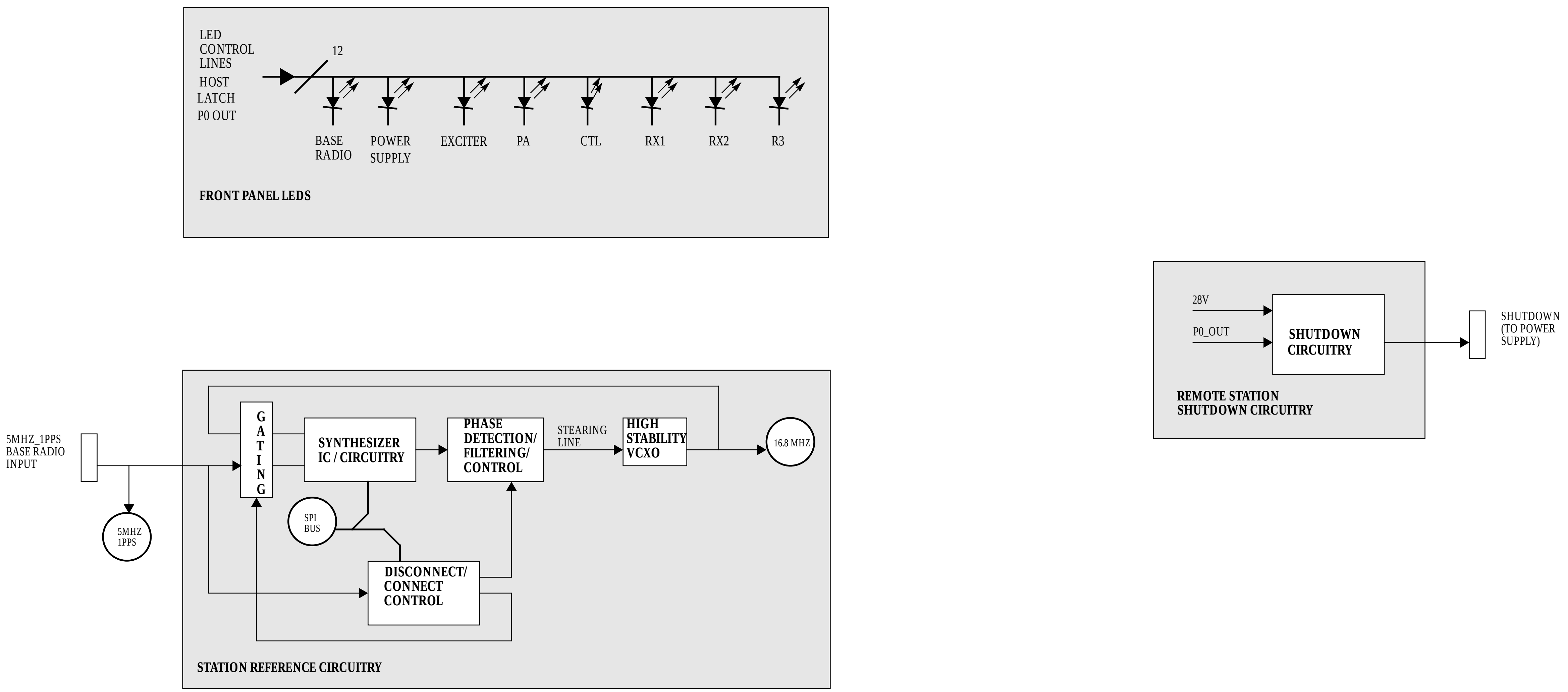


Figure 15 ***Enhanced Base Radio Controller Functional Block Diagram (Sheet 1 of 2)***

EnhancedBase Radio Controller

Functional Block Diagram
Model CLN1653A

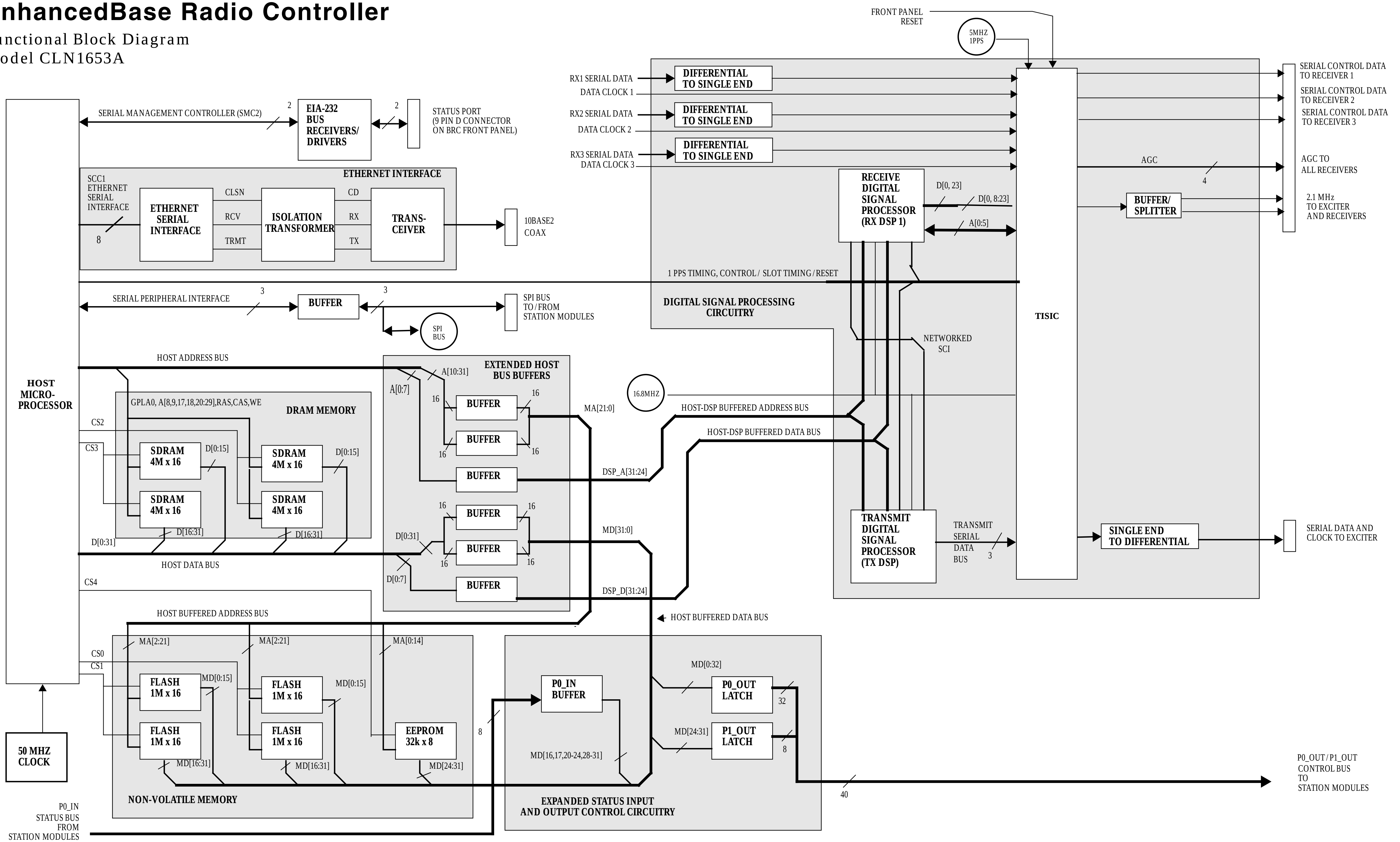


Figure 16 ***Enhanced Base Radio Controller Functional Block Diagram (Sheet 2 of 2)***

MOTOROLA

Base Radio Exciter

Overview

This chapter provides technical information for the Exciter (EX).

FRU Number to Kit Number Cross Reference

Exciter Field Replaceable Units (FRUs) are available for the iDEN EBTS. The FRU contains the Exciter kit and required packaging. Table 1 provides a cross reference between Exciter FRU numbers and kit numbers.

Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
Single Channel Exciter (800 MHz)	TLN3337	CLF1490
QUAD Channel 900 MHz Exciter/ Base Radio Controller)	CLN1497	CLF6452
QUAD Channel 800 MHz Exciter/ Base Radio Controller	CLN1497	CLF1560
LNODCT (Low Noise Offset Direct Conversion Transmit) Exciter (800 MHz)	TLN3337	CLF1789

800 Legacy MHz Exciter – TLN3337

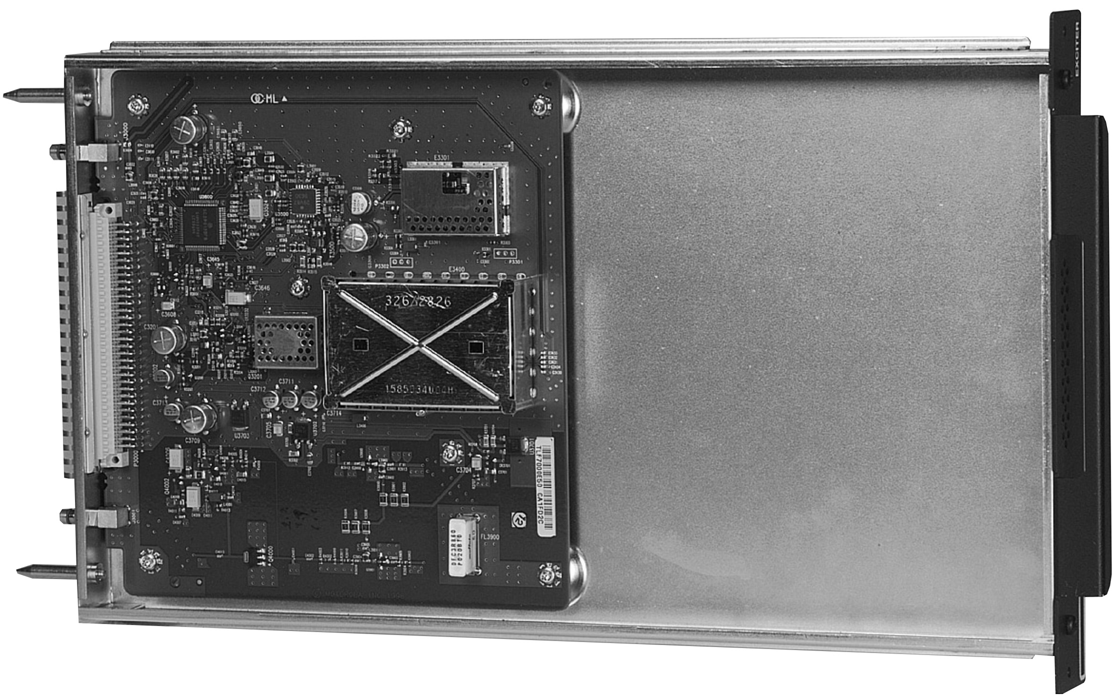
800 MHz Exciter Overview

The Exciter, in conjunction with the Power Amplifier (PA), provides the transmitter functions for the Base Radio. The Exciter module consists of a printed circuit board, a slide in housing, and associated hardware.

The Exciter interconnects to the Base Radio backplane using a 96-pin DIN connector and two blindmate RF connectors. Two Torx screws on the front of the Exciter hold it in the chassis.

There are no controls or indicators on the Exciter. Specifications of the transmitter circuitry, including the Exciter and PAs, are provided in the Base Radio section of the manual.

Figures 1 shows the Exciter with the cover removed.



EBTS330
012197JNM

Figure 1 ***800 MHz Exciter (with cover removed)***

800 MHz Exciter Theory of Operation

Table 2 lists and describes the basic circuitry of the Exciter. Figures 6 shows the functional block diagram of the Exciter.

Table 2 ***Exciter Circuitry***

Circuit	Description
Tranlin IC	Performs the following functions: • up-converts the baseband data to the first IF • down-converts the IF feedback signal to baseband • uses a baseband Cartesian feedback loop system, necessary to obtain linearity from the transmitter and avoid splattering power into adjacent channels • performs training functions for proper linearization of the transmitter
Exciter IC	Interfaces with Tranlin IC to perform: • up-conversion from first IF to the transmit operating frequency • down-conversion to IF of PA output feedback signal for input to Tranlin IC
Address Decode, Memory, & A/D Converter	Serves as the main interface between the synthesizer, Tranlin IC, A/D, and EEPROM on the Exciter and the BRC via the SPI bus
Frequency Synthesizer Circuitry	Consists of a phase-locked loop and VCO to provide a LO signal to the Exciter IC for the second up-conversion and for the first down-conversion of the feedback signal from the PA
970 MHz VCO (800 MHz BR)	Provides a LO signal to the Exciter IC for the second up-conversion to the transmit frequency
237 MHz VCO (800 MHz BR)	Provides a LO signal to Tranlin IC for the first up-conversion and for the second down-conversion of the feedback signal. The synthesizer and divide by 2 circuitry within the Tranlin IC set the first IF to 118.5 MHz
Regulator Circuitry	Provides a regulated voltage to various ICs and RF devices located on the Exciter
Linear RF amplifier Stages	Amplifies the RF signal from the Exciter IC to an appropriate level for input to the PA
Automatic Gain Control (AGC)	provides automatic gain control of the transmitter (Exciter and Power Amplifier modules) to maintain a level forward gain of the RF amplifier stages.

Address Decode Circuitry

The address decode circuitry enables the BRC to use the address bus to control Exciter circuitry. The BRC can select a specific device on the Exciter via the SPI bus for control or data communication purposes.

If the board select circuitry decodes address lines A2 through A5 as the Exciter address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 to generate the chip select signals for the EEPROM, A/D converter, Tranlin IC, and PLL IC. Once selected, the BRC uses the SPI bus to send and receive data to and from the device.

Memory Circuitry

The memory circuitry consists of an EEPROM located on the Exciter. The BRC performs all memory read and write operations via the SPI bus. Information stored in this memory device includes the kit number, revision number, module specific scaling and correction factors, and free form information (scratch pad).

A/D Converter Circuitry

Analog signals from various areas throughout the Exciter board are fed to the A/D converter. These analog signals are converted to a digital signal and are output to the BRC via the SPI lines upon request of the BRC. All signals are periodically monitored and controlled by the BRC.

Some of the signals monitored include the regulated voltages, the external wattmeter (optional), the PLL circuit, and other internal signals.

Tranlin IC Circuitry

The Tranlin IC is a main interface between the Exciter and BRC. Digitized signals (baseband data) are sent via the DSP data bus from the Digital Signal Processors (DSP) of the BRC to the Exciter. These data signals are clocked via the DSP clock signal provided by the Receiver.

The differential data clock signal also serves as a 4.8 MHz reference signal to the internal synthesizer circuit of the Tranlin IC. The Tranlin compares the reference signal with the output of the 237 MHz Voltage Controlled Oscillator (VCO). If the VCO output is out of phase or differs in frequency, correction pulses are sent to the Oscillator and the VCO output is adjusted.

The Tranlin IC up-converts the baseband data received from the BRC to the first IF of 118.5 MHz. It also down-converts an IF feedback signal from the Exciter IC to baseband data for summing.

The Serial Peripheral Interface (SPI) bus is used to communicate with the Tranlin IC. The SPI bus serves as a general purpose bi-directional serial link between the BRC and other modules of the Base Radio, including the Exciter. The SPI bus is used to send control and operational data signals to and from the various circuits of the Exciter.

Exciter IC Circuitry

The Exciter IC interfaces directly with the Tranlin IC to perform up-conversion from the first IF to the programmed transmit operating frequency. The first IF signal is passed through a band-pass filter before it reaches the Exciter IC.

The Exciter IC also down-converts the RF feedback signal from the PA to its IF signal. The IF signal is then input to the Tranlin IC for conversion to baseband data that computes the Cartesian feedback.

Synthesizer Circuitry

The synthesizer circuitry consists of the Phase-Locked Loop (PLL) IC and associated circuitry. The output of this circuit is combined with the 970 MHz VCO to supply a Local Oscillator (LO) signal to the Exciter IC for the second up-conversion of the programmed transmit frequency. This signal is also used for the first down-conversion of the feedback signal from the PA.

An internal phase detector generates a logic pulse in proportion to the difference in phase or frequency between the reference frequency and loop pulse signal.

If the reference frequency is faster than the VCO feedback frequency, an up signal is output from the PLL IC. If the reference frequency is slower than the VCO feedback frequency, a down signal is output from the PLL IC. These pulses are used as correction signals and are fed to a charge pump circuit.

The charge pump circuit consists of five transistors and its associated biasing components. This circuit generates the correction signal and causes it to move up or down in response to the phase detector output pulses. The correction signal is passed through the low-pass loop filter to the 970 MHz Voltage Controlled Oscillator (VCO) circuit.

970 MHz Voltage Controlled Oscillator (VCO)

The 970 MHz VCO generates the second injection frequency for the Exciter IC.

The VCO requires a very low-noise DC supply voltage of +10 VDC for proper operation. The oscillator is driven by a Super Filter that contains an ultra low-pass filter. The Super Filter obtains the required low-noise output voltage for the oscillator.

The output of the oscillator is tapped and sent to the VCO Feedback Filter. This feedback signal is supplied to the Synthesizer circuitry for the generation of correction pulses.

The untapped output of the 970 MHz VCO is sent to the second LO injection circuitry.

236 MHz Voltage Controlled Oscillator (VCO)

The 237 MHz VCO provides a LO signal to Tranlin IC for the first up-conversion and for the second down-conversion of the feedback signal. The synthesizer and divide by 2 circuitry within the Tranlin IC set the first IF to 118.5 MHz.

Regulator Circuity

This circuit generates three regulated voltages of +5 VDC, +10 VDC, and +11.8 VDC. All voltages are obtained from the +14.2 VDC backplane voltage. These voltages are used to power various ICs and RF devices of the Exciter.

Linear RF Amplifier Stages

This circuitry is used to amplify the RF signal from the Exciter IC to an appropriate level for input to the PA.

Low Noise 800 MHz Exciter

LNODCT (Low Noise Offset Direct Conversion Transmit) 800 MHz Exciter Overview

The Low Noise Exciter and the Power Amplifier (PA) provide the transmitter functions of the Generation 2 Base Radio. The Low Noise Exciter module consists of a printed circuit board, a slide in housing, and associated hardware.

The Low Noise Exciter connects to the Base Radio backplane through a 96-pin DIN connector and two blindmate RF connectors. Two Torx screws on the front of the Exciter secure it to the chassis.

There are no controls or indicators on the Exciter. Specifications of the transmitter circuitry, including the Exciter and PAs, are provided in the Base Radio section of the manual.

Figure 2 shows the Exciter with the cover removed.

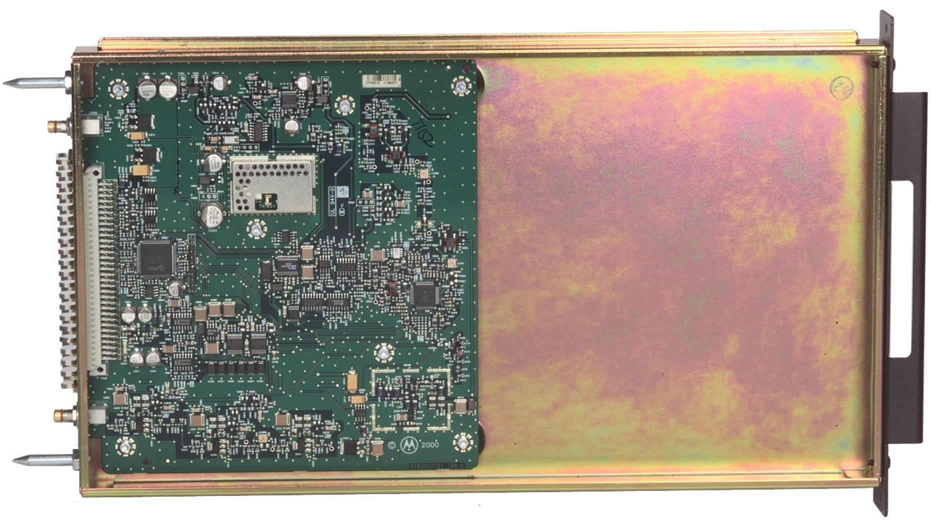


Figure 2 ***Low Noise 800 MHz Exciter (with cover removed)***

Low Noise Exciter Theory of Operation

Table 3 describes the basic circuitry of the Low Noise Exciter. Figures 8 show the Low Noise Exciter's functional block diagram.

Table 3 ***Exciter Circuitry***

Circuit	Description
Low Noise IC	• Up-converts baseband data to the transmit frequency • Down-converts the PA feedback signal to baseband • Uses a baseband Cartesian feedback loop system, necessary to obtain linearity from the transmitter and avoid splattering power into adjacent channels • Performs training functions for proper linearization of the transmitter
Memory & A/D Converter	Serves as the main interface between the synthesizer, Tranlin IC, A/D, and EEPROM on the Exciter, and the BRC via the SPI bus
Frequency Synthesizer Circuitry	• Consists of a phase-locked loop and VCO • Provides a LO signal to the Low Noise IC for the second up-conversion and first down-conversion of the feedback signal from the PA
970 MHz VCO (800 MHz BR)	Provides a LO signal to the Low Noise IC, for up-conversion to the transmit frequency
90.3 MHz VCO (800 MHz BR)	Provides a LO signal to Low Noise IC, for the up-conversion and for the down-conversion of the feedback signal. The mixed output becomes the LO signal for Transmit signal up- and down- conversion
Regulator Circuitry	Provides a regulated voltage to various ICs and RF devices located on the Exciter
Linear RF amplifier Stages	Amplifies the RF signal from the Exciter IC to an appropriate level for input to the PA

Memory Circuitry

The memory circuitry is loaded on an EEPROM on the Exciter. The EBRC performs memory read and write operations via the SPI bus. Information stored in this memory device includes the kit number, revision number, module-specific scaling, and correction factors, operations, parameters, and free-form information (scratch pad) kit number

A/D Converter Circuitry

Analog signals from various areas throughout the Exciter board enter the A/D converter (A/DC). The A/DC converts these analog signals to digital form. Upon request of the BRC, A/DC output signals enter the BRC via SPI lines. The Controller periodically monitors all signals.

Some of the monitored signals include amplifier bias and synthesizer signals.

LNODCT IC Circuitry

The LNODCT IC (Low Noise Offset Direct Conversion Transmit IC) is a main interface between the Exciter and BRC. The BRC's Digital Signal Processor (DSP) sends digitized signals (baseband data) to the Exciter over the DSP data bus.

The differential data clock signal serves as a 2.4 MHz reference signal to the LNODCT IC's internal synthesizer. The LNODCT compares the reference signal with the outputs of Voltage Controlled Oscillators (VCOs). The LNODCT might sense that a VCO's output is out of phase or off-frequency. If so, then the LNODCT sends correction pulses to the VCO. The pulses adjust VCO output, thereby matching phase and frequency with the reference.

The LNODCT IC up-converts baseband data from the EBRC to the transmit frequency. The LNODCT IC also down-converts the Transmit signal from the Power Amplifier to baseband data for cartesian feedback linearization.

The EBRC uses the Serial Peripheral Interface (SPI) bus to communicate with the LNODCT IC. The SPI bus serves as a general purpose, bi-directional, serial link between the EBRC and other Base Radio modules, including the Exciter. The SPI carries control and operational data signals to and from Exciter circuits.

Synthesizer Circuitry

The synthesizer circuit consists of the Phase-Locked Loop (PLL) IC and associated circuitry. This circuit's controls the 970 MHz VCO signal. An internal phase detector generates a logic pulse. This pulse is proportional to the phase or frequency difference between the reference frequency and loop pulse signal.

The charge pump circuit generates a correction signal. The correction signal moves up or down in response to phase detector output pulses. The correction signal passes through the low-pass loop filter. The signal then enters the 970 MHz Voltage Controlled Oscillator (VCO) circuit.

970 MHz Voltage Controlled Oscillator (VCO)

For proper operation, the VCO requires a very low-noise, DC supply voltage. An ultra low-pass filter prepares the necessary low-noise voltage and drives the oscillator.

A portion of the oscillator output signal enters the synthesizer circuitry. The circuitry uses this feedback signal to generate correction pulses.

The 970 MHz VCO output mixes with the 90.3 MHz VCO output. The result is a Local Oscillator [LO) signal for the LNODCT IC. The LNODCT uses this LO signal to up-convert the programmed transmit frequency. The LNODCT also uses the LO signal to down-convert the PA feedback signal.

90.3 MHz Voltage Controlled Oscillator (VCO)

The synthesizer within the LNODCT IC sets the 90.3 MHz signal. The 90.3 MHz VCO provides a LO signal to the LNODCT IC. The LNODCT uses this signal in up-converting and down-converting the feedback signal.

Regulator Circuitry

The voltage regulators generate three regulated voltages: +3 Vdc, +5 Vdc and +11.7 Vdc. The regulators obtain input voltages from the +3.3 Vdc and +14.2 Vdc backplane voltages. The regulated voltages power various ICs and RF devices in the Exciter.

Linear RF Amplifier Stages

The linear RF amplifiers boost the RF signal from the LNODCT IC. The RF Amplifier generates an appropriate signal level to drive the PA.

QUAD Channel 900 MHz Exciter

QUAD Channel 900 MHz Exciter Overview

The Exciter and the Power Amplifier (PA) provide the transmitter functions of the QUAD Channel 900 MHz Base Radio. The Exciter module consists of a printed circuit board, a slide in housing, and associated hardware. The BRC shares the printed circuit board and housing.

The Exciter connects to the Base Radio backplane through a 168-pin connector and two blindmate RF connectors. Controller and exciter circuitry also interconnect on the Exciter/Controller module. Two Torx screws on the front of the Exciter secure it to the chassis.

An LED identifies the Exciter's operational condition, as described in the manual's Controller section. The Base Radio section of the manual provides specifications for transmitter circuitry. This information includes data on the Exciter and PAs.

Figures 4 shows the Exciter with the cover removed.

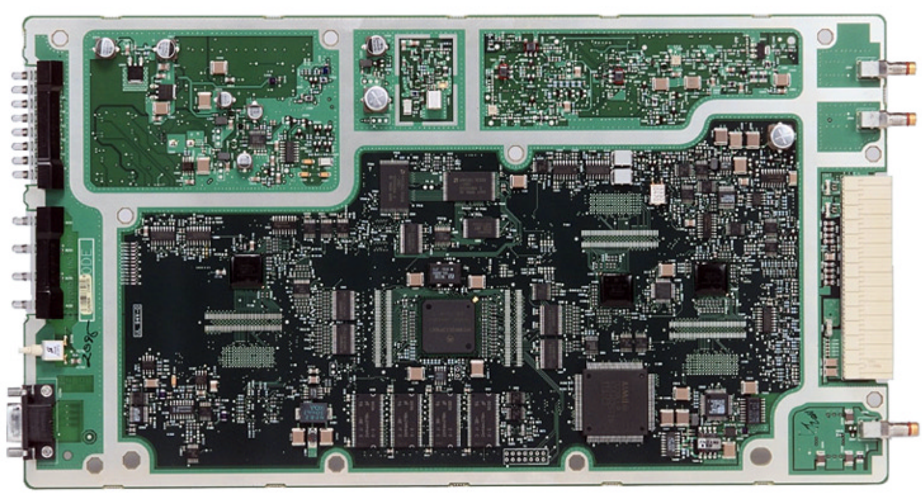


Figure 3 ***900 MHz QUAD Channel Exciter (with cover removed)***

900 MHz QUAD Channel Exciter Theory of Operation

Table 4 describes the basic circuitry of the Exciter. Figures 8 show the QUAD Carrier Exciter's functional block diagram.

Table 4 ***900 MHz Exciter Circuitry***

Circuit	Description
LNODCT IC	• Up-converts baseband data to the transmit frequency • Down-converts the PA feedback signal to baseband • Uses a baseband Cartesian feedback loop system, necessary to obtain linearity from the transmitter and avoid splattering power into adjacent channels • Performs training functions for proper linearization of the transmitter
Memory & A/D Converter	Serves as the main interface between the synthesizer, Tranlin IC, A/D, and EEPROM on the Exciter, and the BRC via the SPI bus
Frequency Synthesizer Circuitry	• Consists of a phase-locked loop and VCO • Provides a LO signal to the LNODCT IC for the second up-conversion and first down-conversion of the feedback signal from the PA
1025 MHz VCO (900 MHz BR)	Provides a LO signal to the LNODCT IC, for up-conversion to the transmit frequency
90.3 MHz VCO (900 MHz BR)	Provides a LO signal to LNODCT IC, for the up-conversion and for the down-conversion of the feedback signal. The mixed output becomes the LO signal for Transmit signal up- and down- conversion
Regulator Circuitry	Provides a regulated voltage to various ICs and RF devices located on the Exciter
Linear RF amplifier Stages	Amplifies the RF signal from the Exciter IC to an appropriate level for input to the PA

Memory Circuitry

The memory circuitry is an EEPROM on the Controller portion of the Exciter/Controller module. The Controller performs memory read and write operations over the parallel bus. The memory device stores the following data...

❒ kit number
❒ revision number
❒ module specific scaling and correction factors
❒ serial number
❒ free form information (scratch pad)

A/D Converter Circuitry

Analog signals from various areas throughout the Exciter board enter the A/D converter (A/DC). The A/DC converts these analog signals to digital form. Upon request of the BRC, A/DC output signals enter the BRC via SPI lines. The Controller periodically monitors all signals.

Some of the monitored signals include amplifier bias and synthesizer signals.

Low Noise Offset Direct Conversion Transmit (LNODCT) IC Circuitry

The Low Noise IC is a main interface between the Exciter and BRC. The BRC's Digital Signal Processor (DSP) sends digitized signals (baseband data) to the Exciter over the DSP data bus.

The differential data clock signal serves as a 2.4 MHz reference signal to the Low Noise IC's internal synthesizer. The Low Noise IC compares the reference signal with the outputs of Voltage Controlled Oscillators (VCOs). The Low Noise IC might sense that a VCO's output is out of phase or off-frequency. If so, then the Low Noise IC sends correction pulses to the VCO. The pulses adjust VCO output, thereby matching phase and frequency with the reference.

The Low Noise IC up-converts baseband data from the BRC to the transmit frequency. The Low Noise IC also down-converts the Transmit signal from the Power Amplifier to baseband data for cartesian feedback linearization.

The BRC uses the Serial Peripheral Interface (SPI) bus to communicate with the Low Noise IC. The SPI bus serves as a general purpose, bi-directional, serial link between the BRC and other Base Radio modules, including the Exciter. The SPI carries control and operational data signals to and from Exciter circuits.

Synthesizer Circuitry

The synthesizer circuit consists of the Phase-Locked Loop (PLL) IC and associated circuitry. This circuit's controls the 1025 MHz VCO signal. An internal phase detector generates a logic pulse. This pulse is proportional to the phase or frequency difference between the reference frequency and loop pulse signal.

The charge pump circuit generates a correction signal. The correction signal moves up or down in response to phase detector output pulses. The correction signal passes through the low-pass loop filter. The signal then enters the 1025 MHz Voltage Controlled Oscillator (VCO) circuit.

1025 MHz Voltage Controlled Oscillator (VCO)

For proper operation, the VCO requires a very low-noise, DC supply voltage. An ultra low-pass filter prepares the necessary low-noise voltage and drives the oscillator.

A portion of the oscillator output signal enters the synthesizer circuitry. The circuitry uses this feedback signal to generate correction pulses.

The 1025MHz VCO output mixes with the 90.3 MHz VCO output. The result is a Local Oscillator [LO) signal for the Low Noise IC. The LNODCT uses this LO signal to up-convert the programmed transmit frequency. The Low Noise IC also uses the LO signal to down-convert the PA feedback signal.

90.3 MHz Voltage Controlled Oscillator (VCO)

The synthesizer within the Low Noise IC sets the 90.3 MHz signal. The 90.3 MHz VCO provides a LO signal to the LNODCT IC. The Low Noise IC uses this signal in up-converting and down-converting the feedback signal.

Regulator Circuitry

The voltage regulators generate three regulated voltages: +3 Vdc, +5 Vdc and +11.7 Vdc. The regulators obtain input voltages from the +3.3 Vdc and +14.2 Vdc backplane voltages. The regulated voltages power various ICs and RF devices in the Exciter.

Linear RF Amplifier Stages

The linear RF amplifiers boost the RF signal from the Low Noise IC. The RF Amplifier generates an appropriate signal level to drive the PA.

QUAD Channel 800 MHz Exciter

QUAD Channel 800 MHz Exciter Overview

The Exciter and the Power Amplifier (PA) provide the transmitter functions of the QUAD Channel Base Radio. The Exciter module consists of a printed circuit board, a slide in housing, and associated hardware. The BRC shares the printed circuit board and housing.

The Exciter connects to the Base Radio backplane through a 168-pin connector and two blindmate RF connectors. Controller and exciter circuitry also interconnect on the Exciter/Controller module. Two Torx screws on the front of the Exciter secure it to the chassis.

An LED identifies the Exciter's operational condition, as described in the manual's Controller section. The Base Radio section of the manual provides specifications for transmitter circuitry. This information includes data on the Exciter and PAs.

Figures 4 shows the Exciter with the cover removed.

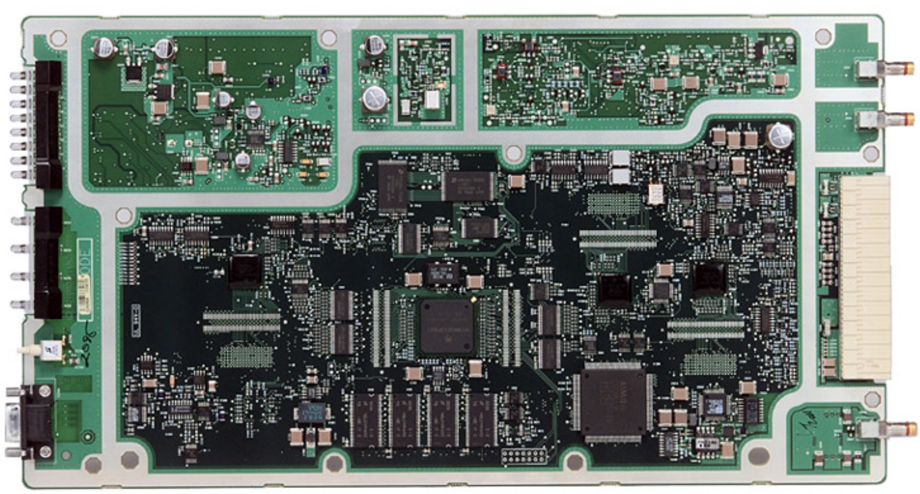


Figure 4 ***800 MHz QUAD Channel Exciter (with cover removed)***

QUAD Channel 800 MHz Exciter Theory of Operation

Table 5 describes the basic circuitry of the Exciter. Figures 8 show the QUAD Carrier Exciter's functional block diagram.

Table 5 ***Exciter Circuitry***

Circuit	Description
LNODCT IC	• Up-converts baseband data to the transmit frequency • Down-converts the PA feedback signal to baseband • Uses a baseband Cartesian feedback loop system, necessary to obtain linearity from the transmitter and avoid splattering power into adjacent channels • Performs training functions for proper linearization of the transmitter
Memory & A/D Converter	Serves as the main interface between the synthesizer, Tranlin IC, A/D, and EEPROM on the Exciter, and the BRC via the SPI bus
Frequency Synthesizer Circuitry	• Consists of a phase-locked loop and VCO • Provides a LO signal to the LNODCT IC for the second up-conversion and first down-conversion of the feedback signal from the PA
970 MHz VCO (800 MHz BR)	Provides a LO signal to the LNODCT IC, for up-conversion to the transmit frequency
90.3 MHz VCO (800 MHz BR)	Provides a LO signal to LNODCT IC, for the up-conversion and for the down-conversion of the feedback signal. The mixed output becomes the LO signal for Transmit signal up- and down- conversion
Regulator Circuitry	Provides a regulated voltage to various ICs and RF devices located on the Exciter
Linear RF amplifier Stages	Amplifies the RF signal from the Exciter IC to an appropriate level for input to the PA

Memory Circuitry

The memory circuitry is an EEPROM on the Controller portion of the Exciter/ Controller module. The Controller performs memory read and write operations over the parallel bus. The memory device stores the following data...

❐ kit number

❐ revision number

❐ module specific scaling and correction factors

❐ serial number

❐ free form information (scratch pad)

A/D Converter Circuitry

Analog signals from various areas throughout the Exciter board enter the A/D converter (A/DC). The A/DC converts these analog signals to digital form. Upon request of the BRC, A/DC output signals enter the BRC via SPI lines. The Controller periodically monitors all signals.

Some of the monitored signals include amplifier bias and synthesizer signals.

Low Noise Offset Direct Conversion Transmit (LNODCT) IC Circuitry

The Low Noise IC is a main interface between the Exciter and BRC. The BRC's Digital Signal Processor (DSP) sends digitized signals (baseband data) to the Exciter over the DSP data bus.

The differential data clock signal serves as a 2.4 MHz reference signal to the Low Noise IC's internal synthesizer. The Low Noise IC compares the reference signal with the outputs of Voltage Controlled Oscillators (VCOs). The Low Noise IC might sense that a VCO's output is out of phase or off-frequency. If so, then the Low Noise IC sends correction pulses to the VCO. The pulses adjust VCO output, thereby matching phase and frequency with the reference.

The Low Noise IC up-converts baseband data from the BRC to the transmit frequency. The Low Noise IC also down-converts the Transmit signal from the Power Amplifier to baseband data for cartesian feedback linearization.

The BRC uses the Serial Peripheral Interface (SPI) bus to communicate with the Low Noise IC. The SPI bus serves as a general purpose, bi-directional, serial link between the BRC and other Base Radio modules, including the Exciter. The SPI carries control and operational data signals to and from Exciter circuits.

Synthesizer Circuitry

The synthesizer circuit consists of the Phase-Locked Loop (PLL) IC and associated circuitry. This circuit's controls the 970 MHz VCO signal. An internal phase detector generates a logic pulse. This pulse is proportional to the phase or frequency difference between the reference frequency and loop pulse signal.

The charge pump circuit generates a correction signal. The correction signal moves up or down in response to phase detector output pulses. The correction signal passes through the low-pass loop filter. The signal then enters the 970 MHz Voltage Controlled Oscillator (VCO) circuit.

970 MHz Voltage Controlled Oscillator (VCO)

For proper operation, the VCO requires a very low-noise, DC supply voltage. An ultra low-pass filter prepares the necessary low-noise voltage and drives the oscillator.

A portion of the oscillator output signal enters the synthesizer circuitry. The circuitry uses this feedback signal to generate correction pulses.

The 970 MHz VCO output mixes with the 90.3 MHz VCO output. The result is a Local Oscillator [LO) signal for the Low Noise IC. The LNODCT uses this LO signal to up-convert the programmed transmit frequency. The Low Noise IC also uses the LO signal to down-convert the PA feedback signal.

90.3 MHz Voltage Controlled Oscillator (VCO)

The synthesizer within the Low Noise IC sets the 90.3 MHz signal. The 90.3 MHz VCO provides a LO signal to the LNODCT IC. The Low Noise IC uses this signal in up-converting and down-converting the feedback signal.

Regulator Circuitry

The voltage regulators generate three regulated voltages: +3 Vdc, +5 Vdc and +11.7 Vdc. The regulators obtain input voltages from the +3.3 Vdc and +14.2 Vdc backplane voltages. The regulated voltages power various ICs and RF devices in the Exciter.

Linear RF Amplifier Stages

The linear RF amplifiers boost the RF signal from the Low Noise IC. The RF Amplifier generates an appropriate signal level to drive the PA.

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Exciter
800 MHz
Functional Block Diagram

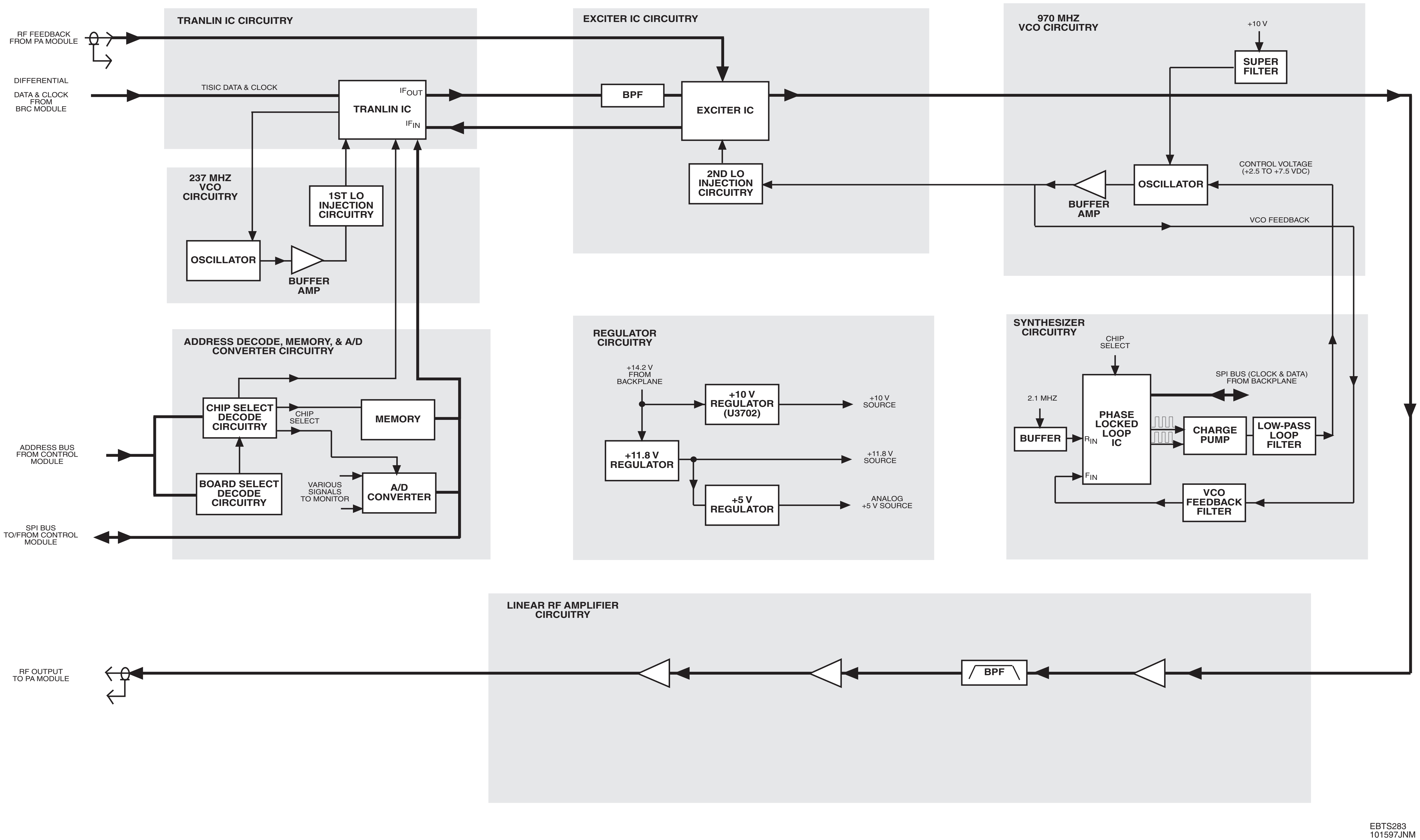
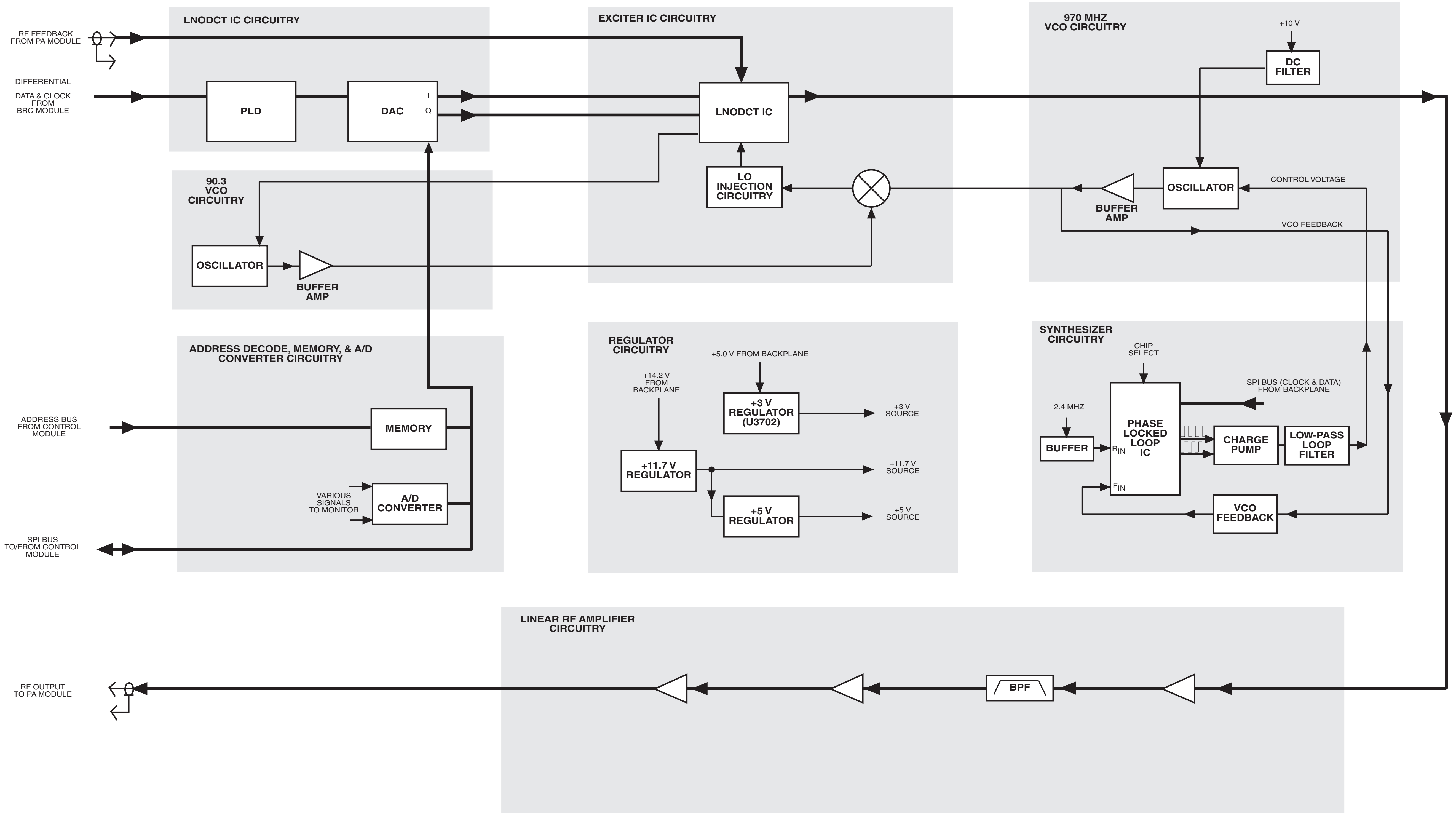


Figure 6 ***Legacy Exciter Functional Block Diagram***



NOTE: Where two frequencies are given, frequency without parentheses applies to 800 MHz BR only and frequency with parentheses applies to 900 MHz BR only.

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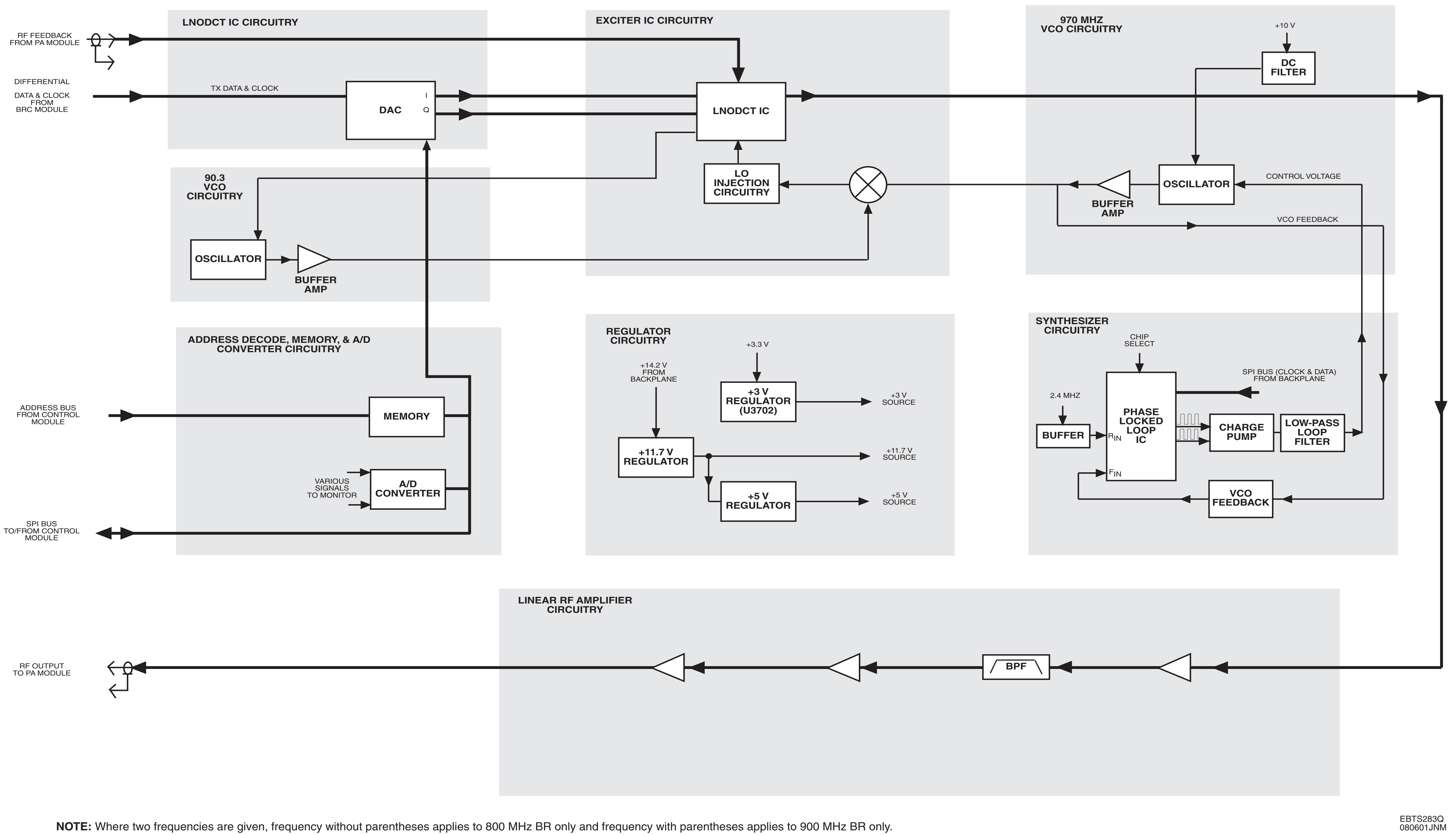
080601JNM

Figure 7 ***Low Noise Exciter Functional Block Diagram***



NOTE: Where two frequencies are given, frequency without parentheses applies to 800 MHz BR only and frequency with parentheses applies to 900 MHz BR only.

Figure 8 ***800 and 900 MHz MHz QUAD Channel Exciter Functional Block Diagram***

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MOTOROLA

Power Amplifier (PA)

Overview

This section provides technical information for the Power Amplifier (PA).

FRU Number to Kit Number Cross Reference

Power Amplifier (PA) Field Replaceable Units (FRUs) are available for the iDEN EBTS. The FRU contains the PA kit and required packaging. Table 1 provides a cross reference between PA FRU numbers and kit numbers.

Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
40 W- 800 MHz Single Channel Base Radio PA	TLF2020	CLF1772
70 W- 800 MHz Single Channel Base Radio PA	TLN3335	CLF1771
52 W- 900 MHz QUAD Channel Base Radio PA	DLN1202	CTF1082
52 W- 800 MHz QUAD Channel Base Radio PA	CLF1499	CLF1400

Power Amplifer Overview

NOTE

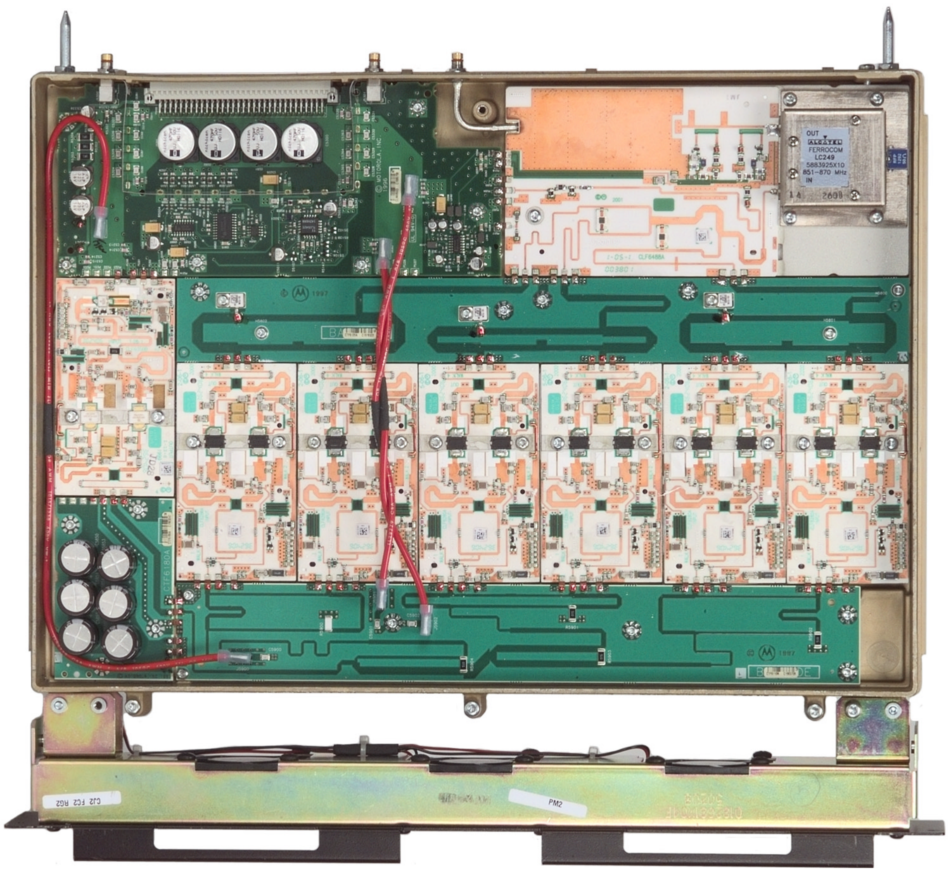
The power outputs discussed on this section for the 800 MHz QUAD and 900 MHz QUAD Power Amplifiers are referenced to the single carrier mode, operating at 52 W average power output from the Power Amplifier's output connector.

The Power Amplifier (PA), with the Exciter, provides the transmitter functions for the Base Radio. The PA accepts the low-level modulated RF signal from the Exciter. The PA then amplifies the signal for transmission and distributes the signal through the RF output connector.

The 800 MHz Base Radio can be equipped with either 40 Watt PA, TLF2020 (version CLF1771) or 70 Watt PA, TLN3335 (version CLF1772). The 40W PA module consists of five hybrid modules, four pc boards, and a module heatsink/housing assembly. The 70W PA module consists of eight hybrid modules, four pc boards, and a module heatsink/housing assembly.

The PA connects to the chassis backplane through a 96-pin DIN connector and three blindmate RF connectors. Two Torx screws located on the front of the PA hold it in the chassis.

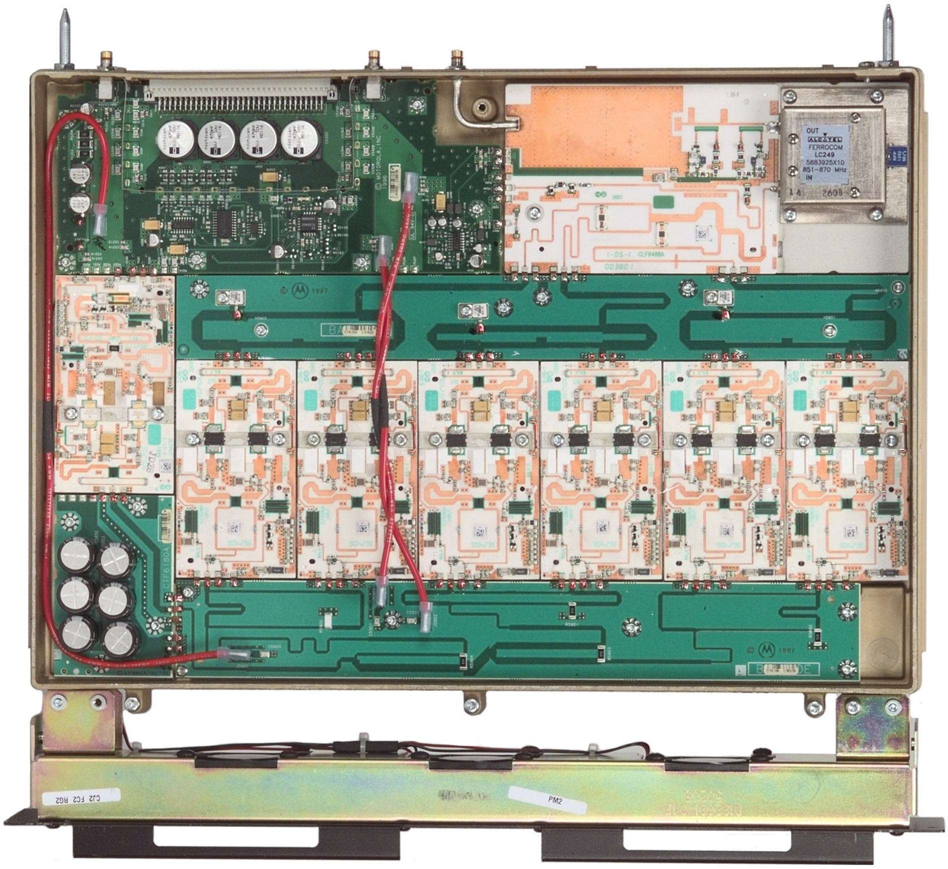
Specifications of the transmitter circuitry, including the Exciter and PAs, are provided in Base Radio Overview section. Figure 1 shows the 40W, 800 MHz PA. Figure 2 shows the 70W, 800 MHz PA. Figure 3 shows the 800 MHz QUAD PA (the 900 MHz QUAD PA is similar in appearance)



NOTE: 70W PA shown. 40W PA is similar.

Figure 1 ***40W - 800 MHz PA – TLF2020 (cover removed)***

Power Amplifer Overview



NOTE: 70W PA shown. 40W PA is similar.

Figure 2 ***70W - 800 MHz PA – TLN3335 (cover removed)***

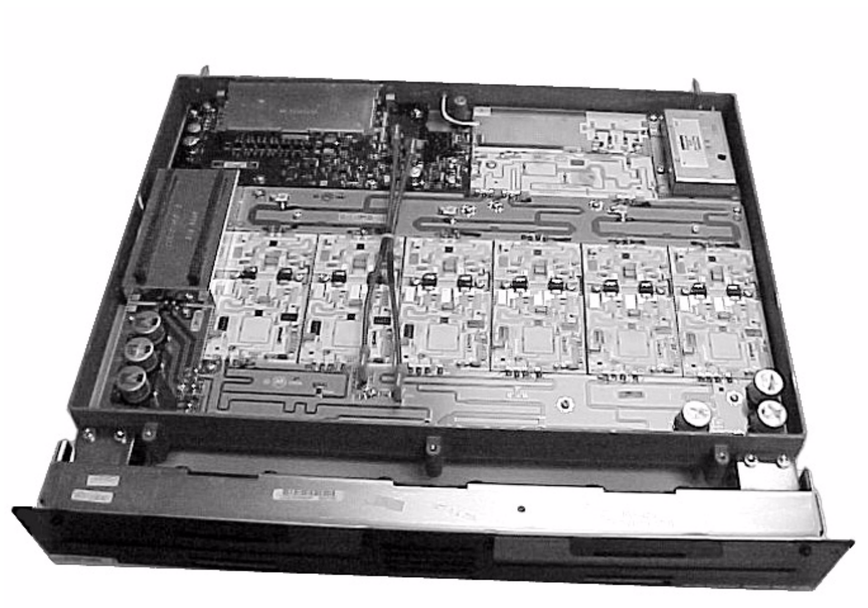


Figure 3 ***800/900 MHz QUAD PA***

PA Theory of Operation

Table 2 describes the basic functions of the PA circuitry. Figures 4 and 5 show the functional block diagrams of 40W, 800 MHz and 70W, 800 MHz PA, respectively. Figure 6 shows a functional block diagram of 800 QUAD MHz. Figure 7 shows a functional block diagram of 900 MHz QUAD PA.

Table 2 ***Power Amplifier Circuitry***

Circuit	Description
DC/Metering Board	• Serves as the main interface between the PA and the backplane board • Accepts RF input from the Exciter via a blindmate RF connector • Routes the RF input via a 50 Ω stripline to the Linear Driver Module RF amplifier • Routes the RF feedback from the RF Combiner/Peripheral Module to the Exciter via a blindmate RF connector • Provides digital alarm and metering information of the PA to the BRC via the SPI bus • Routes DC power to the fans and PA • Contains the thermistor that senses the PA temperature (800 MHz QUAD and 900 MHz QUAD) • Contains a Linear Driver Module and Linear Final Module Bias Enable Circuit (900 MHz QUAD) • Contains a Voltage Variable Attenuator Circuit (900 MHz QUAD)
Linear Driver Module (LDM)	• Contains two Class AB stages with the final stage in a parallel configuration (70W-800 MHz, 40W-800 MHz, 800 MHz QUAD) • Contains three cascaded Class AB stages with the first two stages configured as distributed amplifiers and the final stage in parallel configuration (900 MHz QUAD) • Amplifies the low level RF signal ~11mW average power from the Exciter via the DC/Metering Board (70W-800 MHz, 800 MHz QUAD*, 900 MHz QUAD*) • Amplifies the low-level RF signal ~8 mW average power from the Exciter via the DC/Metering Board (40W- 800 MHz) • Provides an output of: ~8 W (70W, 800MHz) average power ~4 W (40W, 800 MHz) average power ~6 W (800 MHz QUAD* and 900 MHz QUAD*) average power
Interconnect Board (70W-800 MHz, 40W-800 MHz, 800 QUAD, and 900 MHz QUAD	• Provides RF interconnection from the LDM to the RF Splitter board • Provides DC supply filtering
RF Splitter/DC board	• Interfaces with the DC/Metering Board to route DC power to the LFMs • Interfaces with the DC/Metering Board to route PA Bias Enable to the six Linear Final Modules (900 MHz Quad) • Contains splitter circuits that split the RF output signal of the LDM to the three Linear Final Modules (40W- 800 MHz) • Contains splitter circuits that split the RF output signal of the LDM to the six Linear Final Modules (70W- 800 MHz, 800 MHz QUAD and 900 MHz QUAD)

Table 2 ***Power Amplifier Circuitry (Continued)***

Circuit	Description
Linear Final Module (LFM)	• Each module contains two Class AB amplifiers in parallel. Each module amplifies one of three RF signals (~ 84 W average power) from the LDM (via the Splitter/DC board). Three LFMs provide a sum RF output of approximately 48 W average power, before losses. (40W, 800MHz) • Each module contains two Class AB amplifiers in parallel. Each module amplifies one of six RF signals (~ 8 W average power) from the LDM (via the Splitter/DC board). Six LFMs provide a sum RF output of approximately 97 W average power, before losses. (70W, 800MHz) • Each module contains two Class AB amplifiers in parallel. Each module amplifies one of six RF signals (~6W average power) from the LDM (via the splitter/DC Board). Six LFMs provide a sum RF output of approximately 73W average power , before losses. (800 MHZ QUAD* and 900 MHz QUAD*)
RF Interconnect Board (40W- 800 MHz PA only)	• Contains three transmission lines that interconnect the LFMs to the RF Combiner/Peripheral Module
Combiner Board (70W-800 MHz PA, 800 MHz QUAD, 900 MHz QUAD)	• Contains three separate Quadrature combiner circuits that respectively combine the six RF outputs from the LFMs into three signals. These three signals, in turn, are applied to the RF Combiner/Peripheral Module.
RF Combiner/Peripheral Module	• Contains a combiner circuit that combines the three RF signals from the RF Interconnect Board (40W- 800 MHz PA) or the Combiner Board (70W-800 MHz PA). It then routes the combined RF signal through a single stage circulator and a Low Pass Filter. The final output signal is routed to the blindmate RF connector (40W-800 MHz and 70W-800 MHz PAs). • Contains a combiner circuit that combines the three RF signals from the Combiner Board. It then routes the combined RF signal through a dual stage circulator and a Low Pass Filter. The final output signal is routed to the blindmate RF output connector. (800 MHz QUAD and 900 MHz QUAD PAs) • Contains an RF coupler that provides an RF feedback signal to the Exciter via a blindmate RF connector on the DC/Metering Board. Also contains a forward and reverse power detector for alarm and power monitoring purposes. • Contains the thermistor that senses PA temperature and feeds the signal back to the DC/Metering Board for processing (40W-800 MHz, 70W-800 MHz)
Fan Assembly	• Consists of three fans used to keep the PA within predetermined operating temperatures
NOTE: * The power outputs described in this section for the 800 QUAD and 900 QUAD PAs are references to the single carrier mode operating at 52W average power out from the PA output connector.	

DC/Metering Board (Non-QUAD PA)

The DC/Metering Board provides the interface between the PA and the Base Radio backplane. The preamplified/modulated RF signal is input directly from the Exciter via the Base Radio backplane.

The RF input signal is applied to the input of the Linear Driver Module (LDM). The RF feedback signal is fed back to the Exciter, where it is monitored for errors.

The primary function of the DC/Metering Boards is to monitor proper operation of the PA. This information is forwarded to the Base Radio Controller (BRC) via the SPI bus. The alarms diagnostic points monitored by the BRC on the PA include the following:

- Forward power
- Reflected power
- PA temperature sense
- Fan Sensor

DC/Metering Board (QUAD PA Only)

The DC/Metering Board in the QUAD Radio serves the same function as it does in other radios. However, its circuitry is modified for compatibility with the QUAD Station. As a result, its logic circuitry is operated at 3.3 VDC.

In addition to the functions listed for non-QUAD versions above, the following meter points are ported to the SPI bus:

- A and B Currents
- Thermistor (for PA temperature sensing circuit on the DC/Metering Board)
- Voltage Variable Attenuator Circuit (900 MHz QUAD version)
- PA Bias Enable Circuitry (900 MHz QUAD version)

Linear Driver Module

40W-800 MHz, 70W-800 MHZ and 800 MHZ QUAD PAs

The Linear Driver Module (LDM) amplifies the low-level RF signal from the Exciter. The LDM consists of a two-stage cascaded Class AB amplifier, with the final stage in a parallel configuration.

See Table 2 for the approximate input and output levels of the various LDMs. The LDM output is fed to the RF Splitter/DC Distribution Board via an Interconnect Board.

900 QUAD PA

The Linear Driver Module (LDM) amplifies the low-level RF signal from the Exciter. The LDM consists of a three stage, cascaded, Class AB amplifier, with the final stage in a parallel configuration.

See Table 2 for the approximate input and output power of the 900 MHz QUAD LDM.

The LDM Output is fed to the RF Splitter/DC Distribution Board via the Interconnect Board.

Interconnect Board (40W-800 MHz, 70W-800 MHz , 800 MHz QUAD and 900 MHz QUAD)

The output of the LDM is applied to the Interconnect Board, which provides an RF connection to the RF Splitter/DC Distribution Board. As a separate function, area on the Interconnect Board serves as a convenient mounting location for electrolytic capacitors used for filtering the +28 VDC supply.

RF Splitter/DC Distribution Board

40W-800 MHz, 70W-800 MHz, 800 MHz QUAD and 900 MHz QUAD

The RF Splitter portion of this board accepts the amplified signal from the LDM (via the Interconnect Board). The primary function of this circuit is to split the RF signal into drive signals for the LFMs.

In the 40W-800 MHz PA, this circuit splits the drive signal into three separate paths to be applied to the three LFMs, where the signals will be amplified further. In the 70W-800 MHz, 800 MHz QUAD and 900 MHZ QUAD PAs, this circuit splits the drive signal into six separate paths to be applied to the six LFMs, where the signals will be amplified further.

The DC Distribution portion of this board interfaces directly with the DC/ Metering Board to route DC power to the LFMs and provide PA Bias Enable (900 MHz QUAD only)

Linear Final Modules

40W-800 MHz, 70W-800 MHz, 800 MHz QUAD and 900 MHz QUAD

The RF Splitter output signals are applied directly into the LFMs for final amplification. Each LFM contains a coupler that splits the LFM input signal and feeds the parallel Class AB amplifiers that amplify the RF signals.

In the 40W PA, the amplified signals are then combined on the LFM and sent directly to the RF Interconnect Board. In the 70W PA, the amplified signals are then combined on the LFM and sent directly to the Combiner Board.

See Table 2 for the approximate total summed output powers of the various LFMs, before output losses.

RF Interconnect Board (40W- 800 MHz PA Only)

The RF Interconnect Board consists of transmission line paths which route the three output signals from the LFMs to the three inputs of the RF Combiner/ Peripheral Module.

Combiner Board (40W- 800 MHz, 70W- 800 MHz, 800 MHz QUAD and 900 MHz QUAD PAs)

The Combiner Board combines pairs of signals into single signals, thereby combining the six signals from the LDMs into three signals. The resulting three signals are applied to the RF Combiner/Peripheral Module.

RF Combiner/Peripheral Module (40- 800 MHz, 70W- 800 MHz PAs)

This module consists of two portions: an RF combiner and a peripheral module. The RF Combiner portion of the module combines the three RF signals from the RF Interconnect Board (40W- 800 MHz PA) or the Combiner Board (70W- 800 MHz PA) into a single signal using a Wilkinson coupler arrangement.

Following the combiner circuit, the single combined RF signal is then passed through a directional coupler which derives a signal sample of the LFM RF power output. Via the coupler, a sample of the RF output signal is fed to the Exciter, via the DC/Metering Board, as a feedback signal. Following the coupler, the power output signal is passed through a single stage circulator, which protects the PA in the event of high reflected power.

The peripheral portion of the module provides a power monitor circuit that monitors the forward and reflected power of the output signal. This circuit furnishes the A/D converter on the DC/Metering Board with input signals representative of the forward and reflected power levels.

For forward power, a signal representative of the measured value is sent to the BRC via the SPI bus. The BRC determines if this level is within tolerance of the programmed forward power level. If the level is not within parameters, the BRC will issue a warning to the site controller which, in turn, will shut down the Exciter if required.

Reflected power is monitored in the same manner. The BRC uses the reflected power to calculate the voltage standing wave ratio (VSWR). If the VSWR is determined to be excessive, the forward power is rolled back. If it is extremely excessive, the BRC issues a shut-down command to the Exciter.

A thermistor is located on the RF Combiner/Peripheral module to monitor the operating temperature of the PA. The thermistor signal indicating excessive temperature is applied to the A/D converter and then sent to the BRC. The BRC issues a cut-back command to the Exciter module if the monitored temperature is greater than 185˚ F (85˚ C).

RF Combiner/Peripheral Module (800 MHz QUAD and 900 MHz QUAD)

This module consists of two parts: an RF combiner and a Peripheral module. The RF combiner combines three RF signals from the Combiner Board into a single signal using a Wilkinson coupler arrangement. Following the combiner circuit, the single combined RF signal is then passed through a directional coupler, which derives a signal sample of the LFM RF power output. Via the coupler, a sample of the RF output signal is fed to the Exciter, via the DC/Metering Board, as a feedback signal. Following the coupler, the power output signal is passed through a dual stage circulator, which protects the PA in the event of high reflected power.

The Peripheral module provides a power monitor circuit that monitors the forward and reflected power of the output signal. This circuit furnishes the A/D converter on the DC/Metering Board with input signals, representative of the forward and reflected power levels.

For forward power, a signal representative of the measured value is sent to the BRC via the SPI bus. The BRC determines if this level is within tolerance of the programmed forward power level. If the level is not within tolerance, the BRC will issue a warning to the site controller, which, in turn, will shut down the Exciter, if required.

Reflected power is monitored in the same manner. The BRC uses the reflected power to calculate the voltage standing wave ratio (VSWR). If the VSWR is calculated as excessive, forward power is rolled back. If the VSWR calculation is exceedingly out of tolerance, the BRC issues a shut-down command to the Exciter.

NOTE

The Thermistor that monitors the operating temperature of the 800 MHZ QUAD and 900 MHz QUAD PAs is located on the DC/Metering Board

Fan Module

The PA contains a fan assembly to maintain normal operating temperature through the use of a cool air intake. The fan assembly consists of three individual fans in which airflow is directed across the PA heatsink.

The current draw of the fans is monitored by the DC/Metering Board. A voltage representative of the current draw is monitored by the BRC. The BRC flags the iSC if an alarm is triggered. The PA LED on the front panel of the BRC also lights, however the PA does not shut down due to a fan failure alone.

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40W - 800 MHz Power Amplifier – TLF2020 (CLF1772)

Functional Block Diagram

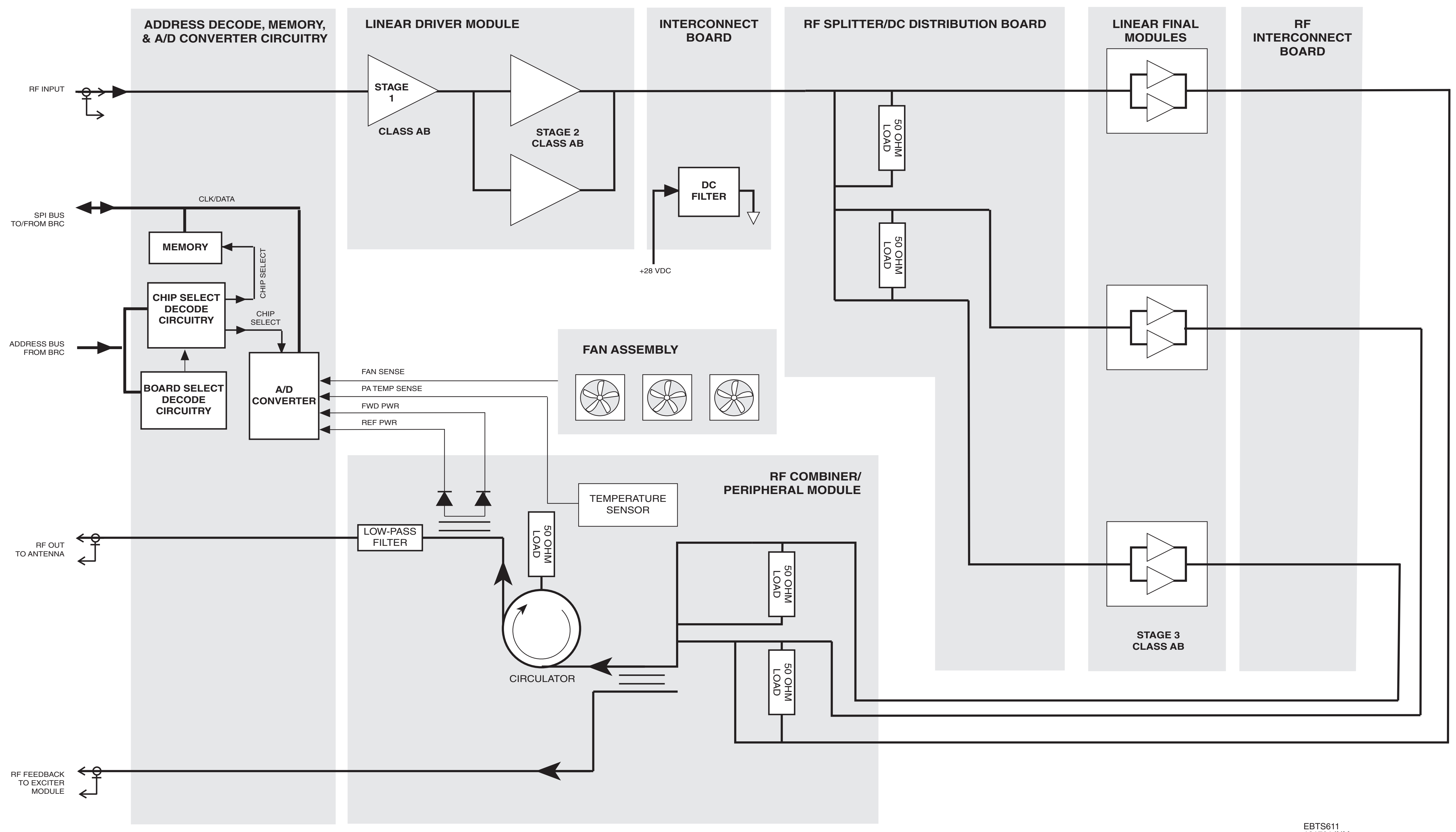

Figure 4 ***40W - 800 MHz PA Functional Block Diagram (Sheet 1 of 1)***

70W - 800 MHz Power Amplifier – TLN3335 (CLF1771)

Functional Block Diagram

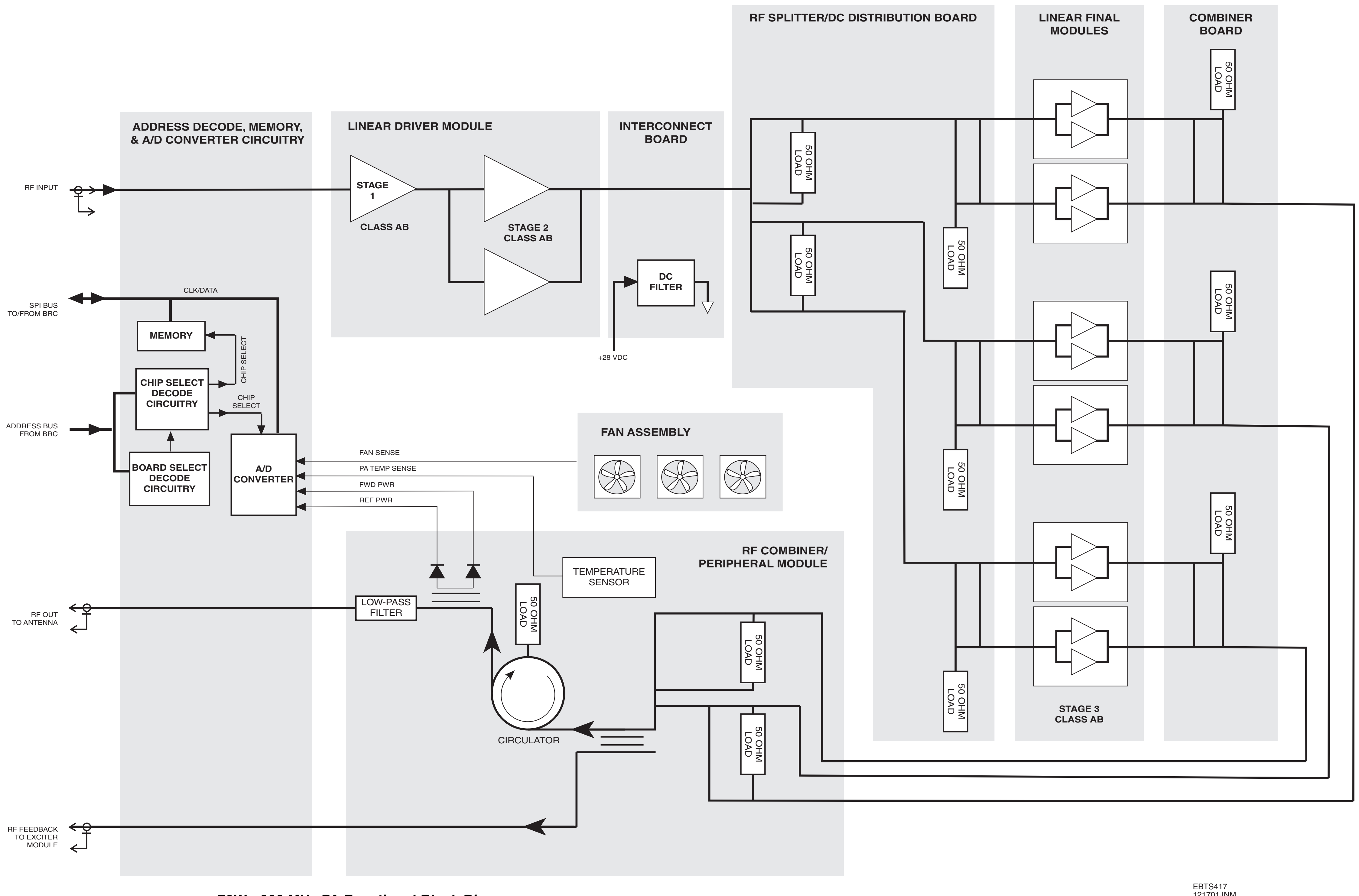

Figure 5 ***70W - 800 MHz PA Functional Block Diagram (Sheet 1 of 1)***

800 MHz QUAD Power Amplifier – CLN1499 (CLF1400)

Functional Block Diagram

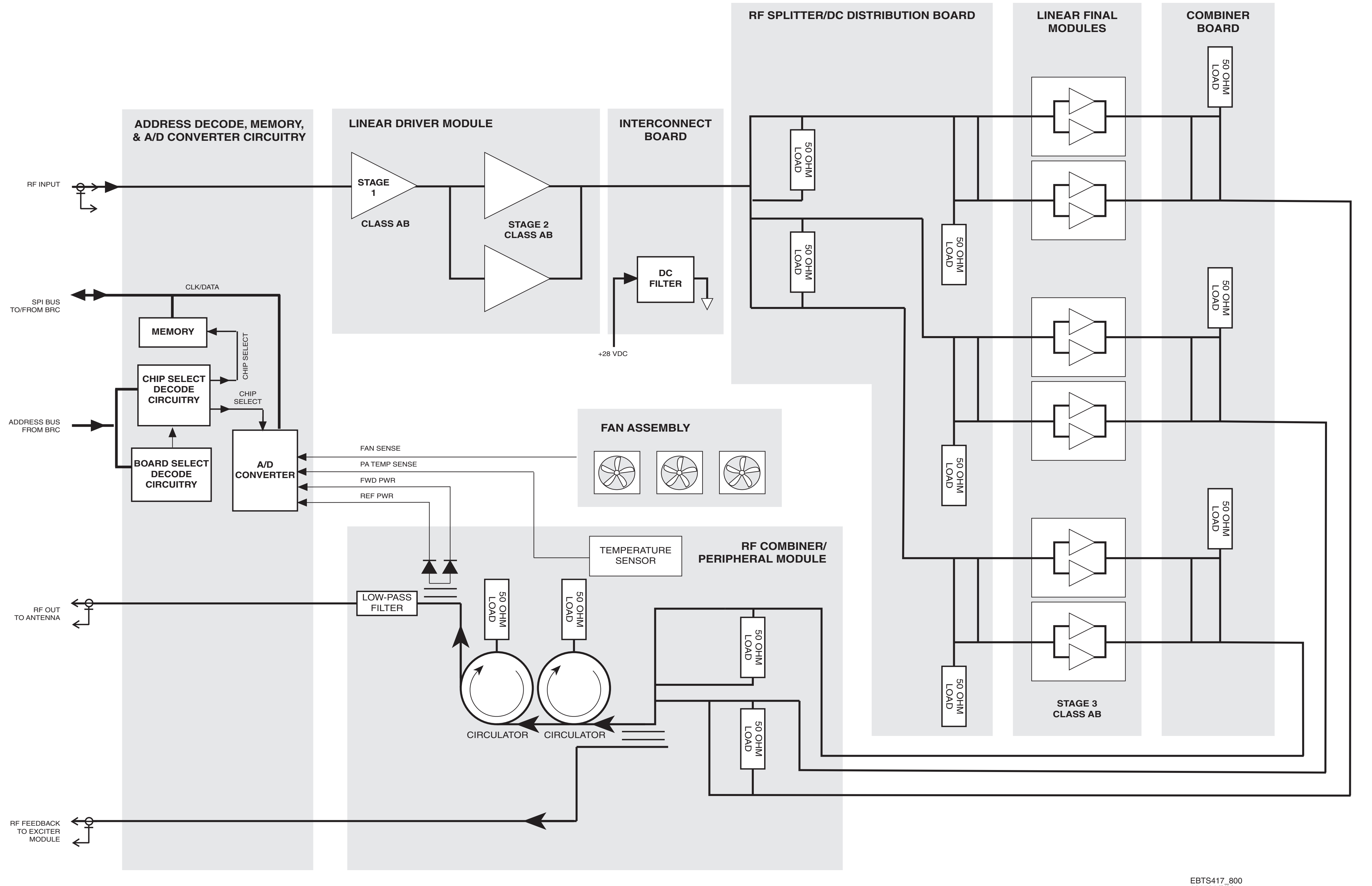

Figure 6 ***800 MHz QUAD Channel BR PA Functional Block Diagram (Sheet 1 of 1)***

900 MHz QUAD Power Amplifier – DLN1202 (CTF1082)

Functional Block Diagram

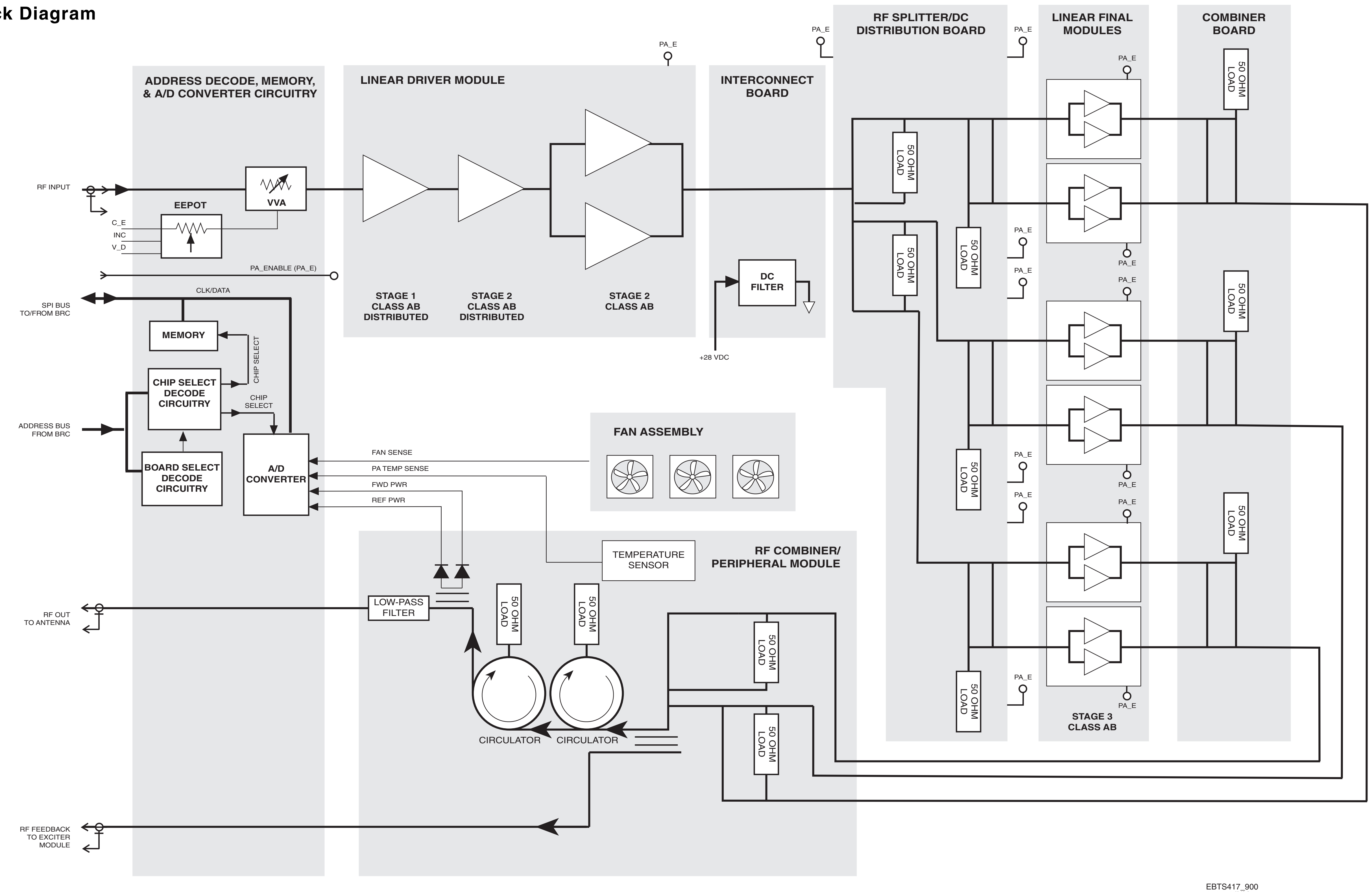

Figure 7 ***900 MHz QUAD Channel BR PA Functional Block Diagram (Sheet 1 of 1)***

DC Power Supply

Overview

This section provides technical information for the DC Power Supply (PS).

FRU Number to Kit Number Cross Reference

DC Power Supply Field Replaceable Units (FRUs) are available for the iDEN EBTS. The FRU contains the Power Supply kit and required packaging. Table 1 provides a cross reference between Exciter FRU numbers and kit numbers.

Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
Single Channel DC Power Supply	TLN3338	CPN1027
QUAD Channel DC Power Supply	CLN1498	CLN1461

Single Channel DC Power Supply Overview

The DC Power Supply provides DC operating voltages to the Base Radio FRUs. It accepts input voltages from 41VDC to 60VDC. The voltage source may be either positive or negative ground.

On initial start up, the supply requires nominal 43 VDC. If the voltage drops below 41 VDC, the DC Power Supply reverts to a quiescent mode and does not supply output power.

The DC Power Supply is designed for sites with an available source of DC voltage. Output voltages supplied from the DC Power Supply are 28.6 VDC, 14.2 VDC and 5.1 VDC with reference to output ground. The supply is rated for 575 Watts continuous output at up to 113˚ F (45˚ C) inlet air. At 140˚ F (60˚ C), the 28.6 VDC output lowers to 80% of maximum.

The DC Power Supply consists of the Power Supply and front panel hardware. The DC Power Supply connects to the chassis backplane using an edgecard style connector. The DC power supply is secured in the chassis with two Torx screws located on the front panel.

Figure 1 shows the DC Power Supply with the cover removed.

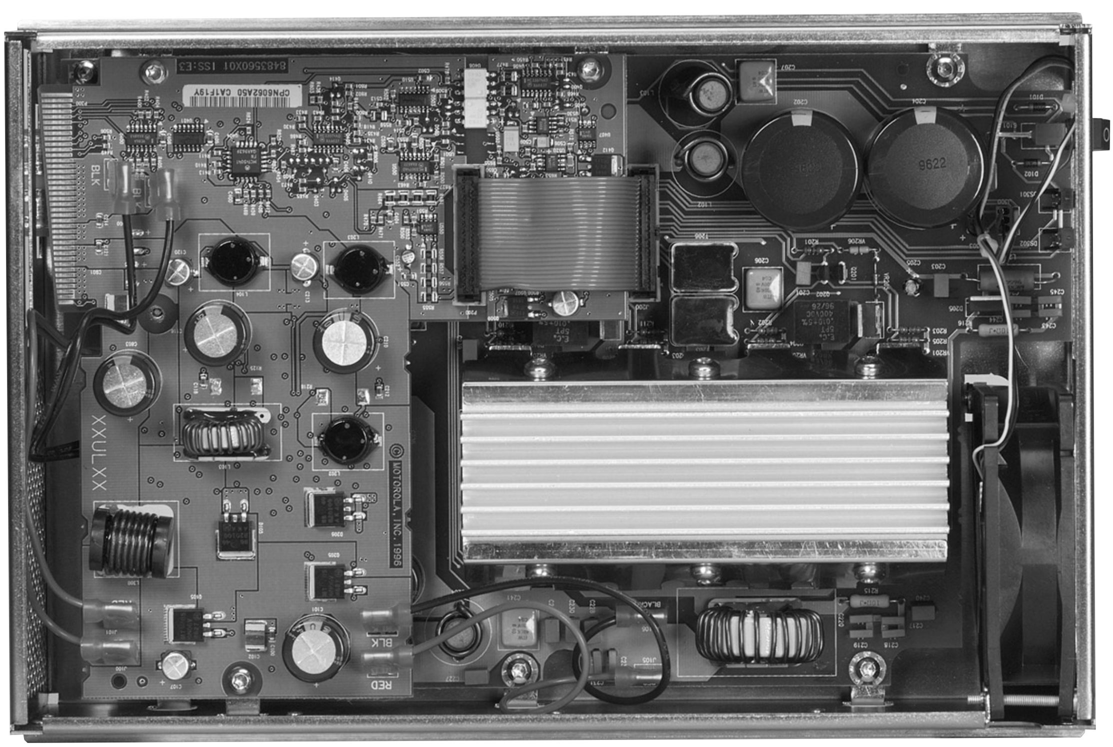

Figure 1 ***Single Channel DC Power Supply***

Single Channel DC Power Supply Controls and Indicators

Table 2 summarizes the LED indicators on the DC Power Supply during normal operation. The ON/OFF switch, located behind the front panel, turns the DC power supply on and off.

Table 2 ***DC Power Supply Indicators***

LED	Condition	Indications
Green	Solid (on)	Power Supply is on and operating under normal conditions with no alarms
	Off	Power Supply is turned off or required power is not available
Red	Solid (on)	Power Supply fault or load fault on any output, or input voltage is out of range
	Off	Power Supply is under normal operation with no alarms

Single Channel DC Power Supply Performance Specifications

Table 3 lists the specifications for the DC Power Supply.

Table 3 ***DC Power Supply Specifications***

Description	Value or Range	
Operating Temperature	0° to +40° C (no derating) +41° to +60° C (derating)	
Input Voltage	41 to 60 VDC	
Input Polarity	Positive (+) ground system	
Start-up Voltage	43 VDC (minimum)	
Input Current	15.6 A (maximum) @ 41 VDC	
Steady State Output Voltages	28.6 VDC ±5% 14.2 VDC ±5% 5.1 VDC ±5%	
Total Output Power Rating	575 W (no derating) 485 W (derating)	
Output Ripple	All outputs 150mV p-p (measured with 20 MHz BW oscilloscope at 25°C) High Frequency individual harmonic voltage limits (10kHz to 100MHz) are:	
	28.6 VDC	1.5 mV p-p
	14.2 VDC	3.0 mV p-p
	5.1 VDC	5.0 mV p-p
Short Circuit Current	0.5 A average (maximum)	

Single Channel DC Power Supply Theory of Operation

Table 4 briefly describes the basic DC Power Supply circuitry. Figure 3 shows the functional block diagrams for the DC Power Supply.

Table 4 **DC Power Supply Circuitry**

Circuit	Description
Input Circuit	Routes input current from the DC power input cable through the high current printed circuit edge connector, EMI filter, panel mounted combination circuit breaker, and on/off switch
Start-up Inverter Circuitry	Provides VDC for power supply circuitry during initial power-up
Main Inverter Circuitry	Consists of a switching-type power supply to generate the +28.6 VDC supply voltage
Temperature Protection	The Power Supply contains a built-in cooling fan that runs whenever the supply is powered on. The supply shuts down if temperature exceeds a preset threshold
+14.2 VDC Secondary Converter Circuitry	Consists of a switching-type power supply to generate the +14.2 VDC supply voltage
+5 VDC Secondary Converter Circuitry	Consists of a switching-type power supply to generate the +5.1 VDC supply voltage
Clock Generator Circuitry	Generates the 267 kHz and 133 kHz clock signals used by the pulse width modulators in the four inverter circuits
Address Decode, Memory, & A/D Converter	Serves as the main interface between A/D on the Power Supply and the BRC via the SPI bus

DC Power Supply for QUAD Channel Base Radios

QUAD Channel DC Power Supply Overview

The QUAD Channel DC Power Supply provides DC operating voltages to QUAD Channel Base Radio FRUs. The power supply accepts input voltage sources from 41VDC to 60VDC. Input sources may be either positively or negatively grounded.

On initial startup, the supply requires a nominal 43 VDC. If the voltage drops below 41 VDC, the QUAD Channel DC Power Supply enters quiescent mode. In quiescent mode, the power supply emits no power.

The QUAD Channel DC Power Supply is designed for sites with an available DC voltage source. Output voltages from the DC Power Supply are 28.6 VDC, 14.2 VDC and 3.3 VDC, with reference to output ground. The supply is rated for 575 Watts of continuous output, with up to 113˚ F (45˚ C) inlet air. At 140˚ F (60˚ C), the 28.6 VDC output reduces to 80% of maximum.

The QUAD Channel DC Power Supply consists of the Power Supply and front panel hardware. The QUAD Channel DC Power Supply connects to the chassis backplane through an edgecard connector. Two Torx screws on the front panel secure the QUAD Channel DC power supply to the chassis.

Figure 2 shows the QUAD Channel Power Supply with the cover removed.

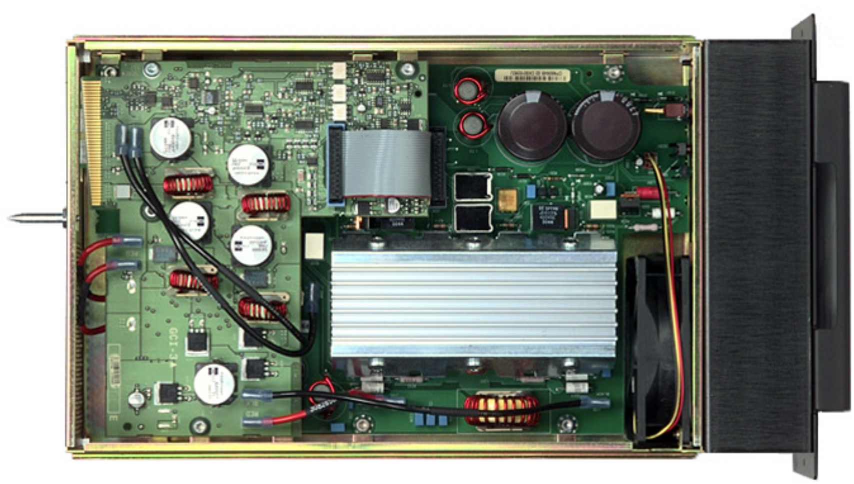

Figure 2 ***Quad Carrier Power Supply***

QUAD Channel DC Power Supply Controls and Indicators

Table 5 summarizes LED indications on the QUAD Channel DC Power Supply during normal operation. The ON/OFF switch behind the front panel turns DC power supply on and off.

Table 5 ***DC Power Supply Indicators***

LED	Condition	Indications
Green	Solid (on)	Power Supply is on, and operating under normal conditions with no alarms
	Off	Power Supply is turned off or required power is not available
Red	Solid (on)	Power Supply fault or load fault on any output, or input voltage is out of range
	Off	Power Supply is operating normally, with no alarms

QUAD Channel DC Power Supply Performance Specifications

Table 6 lists the specifications for the QUAD Channel DC Power Supply.

Table 6 ***DC Power Supply Specifications***

Description	Value or Range	
Operating Temperature	0° to +40° C (no derating) +41° to +60° C (derating)	
Input Voltage	41 to 60 VDC	
Input Polarity	Positive (+) ground system	
Startup Voltage	43 VDC (minimum)	
Input Current	18.0 A (maximum) @ 41 VDC	
Steady State Output Voltages	28.6 VDC ±5% 14.2 VDC ±5% 3.3 VDC ±5%	
Total Output Power Rating	575 W (no derating) 485 W (derating)	
Output Ripple	All outputs 150mV p-p (measured with 20 MHz BW oscilloscope at 25°C) High Frequency individual harmonic voltage limits (10kHz to 100MHz) are:	
	28.6 VDC	1.5 mV p-p
	14.2 VDC	3.0 mV p-p
	3.3 VDC	5.0 mV p-p
Short Circuit Current	0.5 A average (maximum)	

QUAD Channel DC Power Supply Theory of Operation

Table 7 briefly describes the basic DC Power Supply circuitry. Figure 5 shows the functional block diagrams for the DC Power Supply.

Table 7 ***DC Power Supply Circuitry***

Circuit	Description
Input Circuit	Routes input current from the DC power input cable through the high current printed circuit edge connector, EMI filter, panel mounted combination circuit breaker, and on/off switch
Startup Inverter Circuitry	Provides VDC for power supply circuitry during initial power-up
Main Inverter Circuitry	Consists of a switching-type power supply to generate the +28.6 VDC supply voltage
Temperature Protection	The Power Supply contains a built-in cooling fan that runs whenever the supply is powered on. The supply shuts down if the temperature exceeds a preset threshold
+14.2 VDC Secondary Converter Circuitry	Consists of a switching-type power supply to generate the +14.2 VDC supply voltage
+3.3 VDC Secondary Converter Circuitry	Consists of a switching-type power supply to generate the +3.3 VDC supply voltage
Clock Generator Circuitry	Generates the 267 kHz and 133 kHz clock signals used by the pulse width modulators in the four inverter circuits
Address Decode, Memory, & A/D Converter	Serves as the main interface between A/D on the Power Supply and the BRC via the SPI bus

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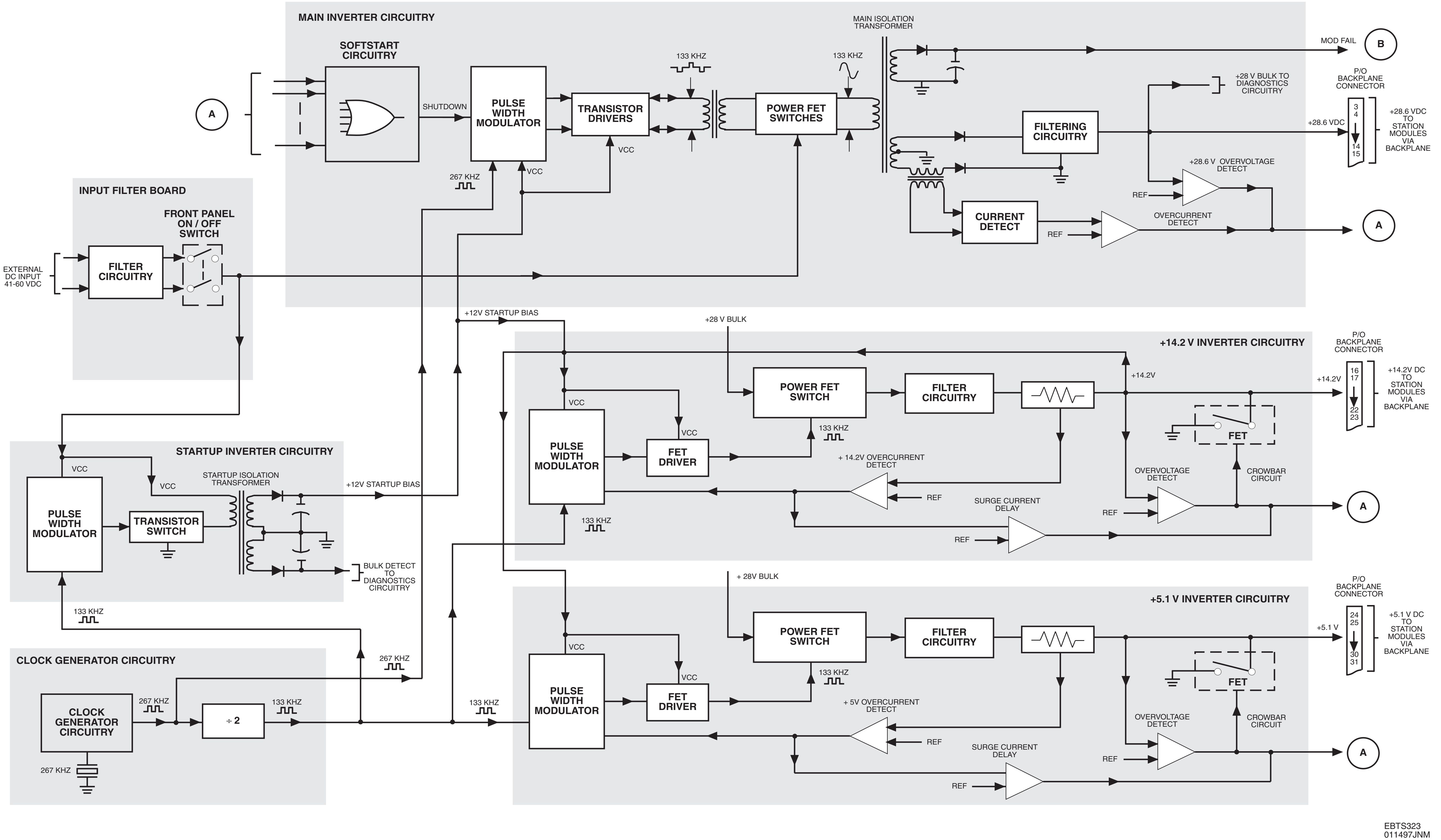


Figure 3 ***DC Power Supply Functional Block Diagram (Sheet 1 of 2)***

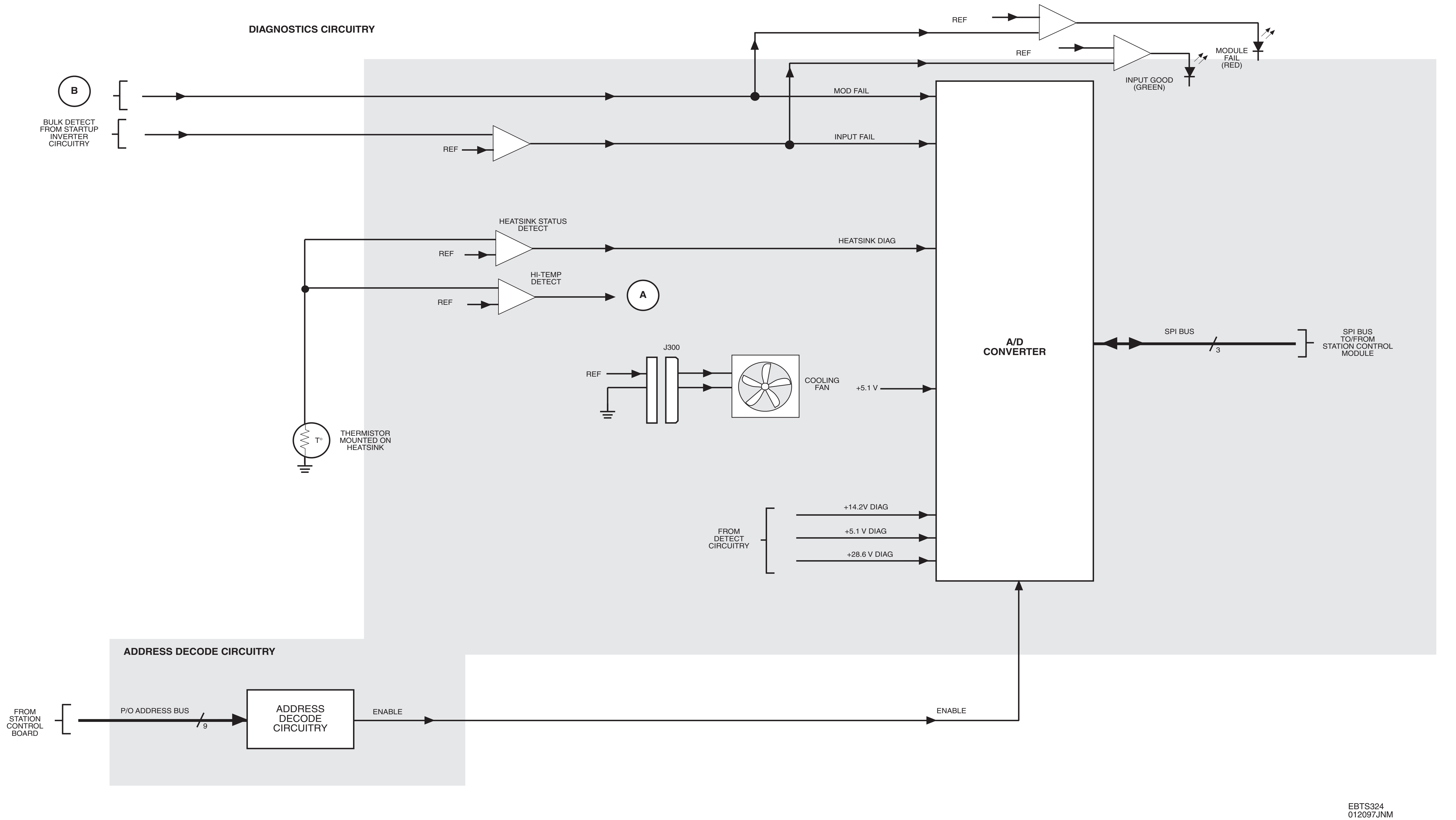


Figure 4 ***DC Power Supply Functional Block Diagram (Sheet 2 of 2)***

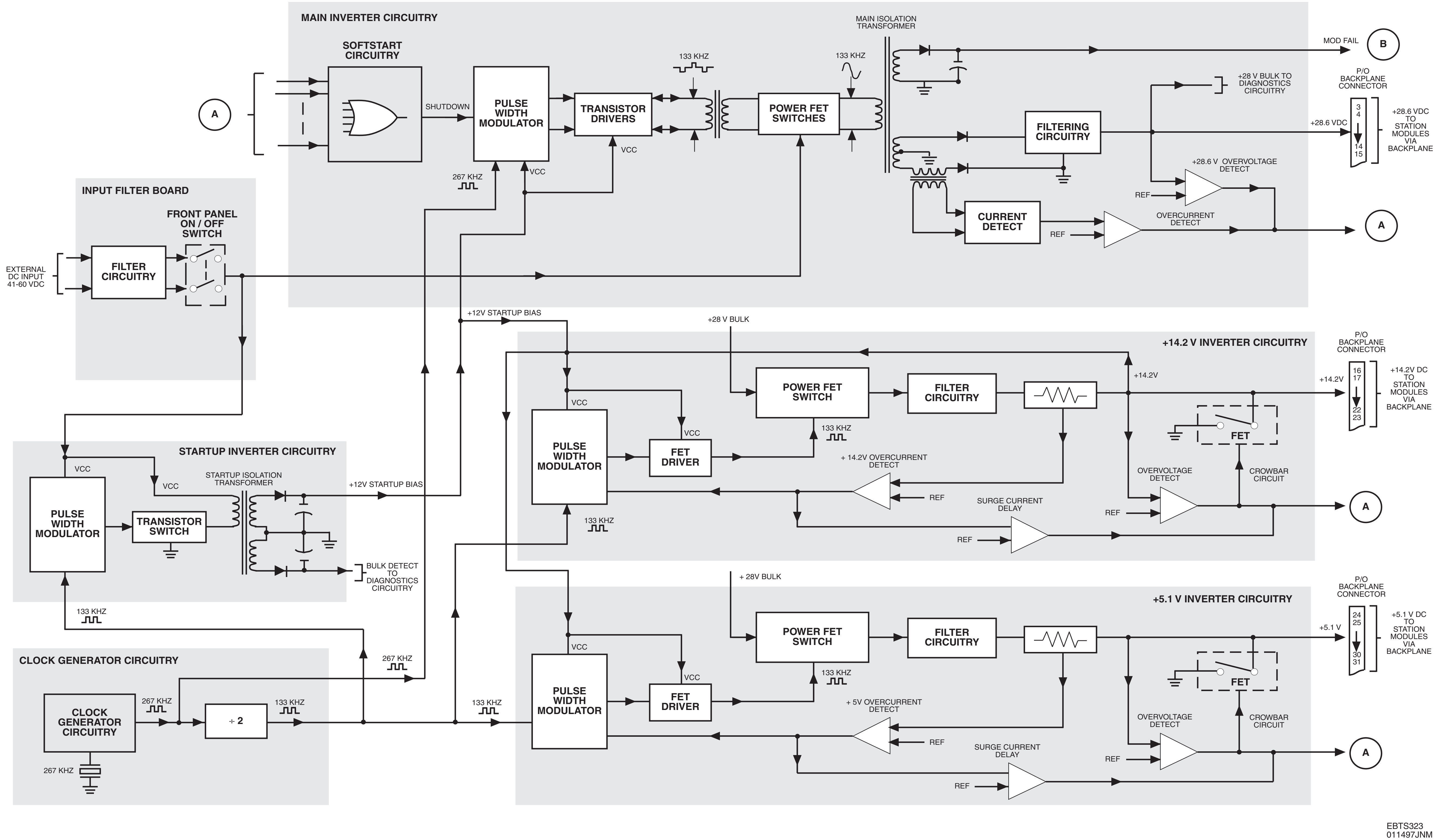


Figure 5 ***QUAD BR DC Power Supply (Sheet 1 of 2)***

DC Power Supply

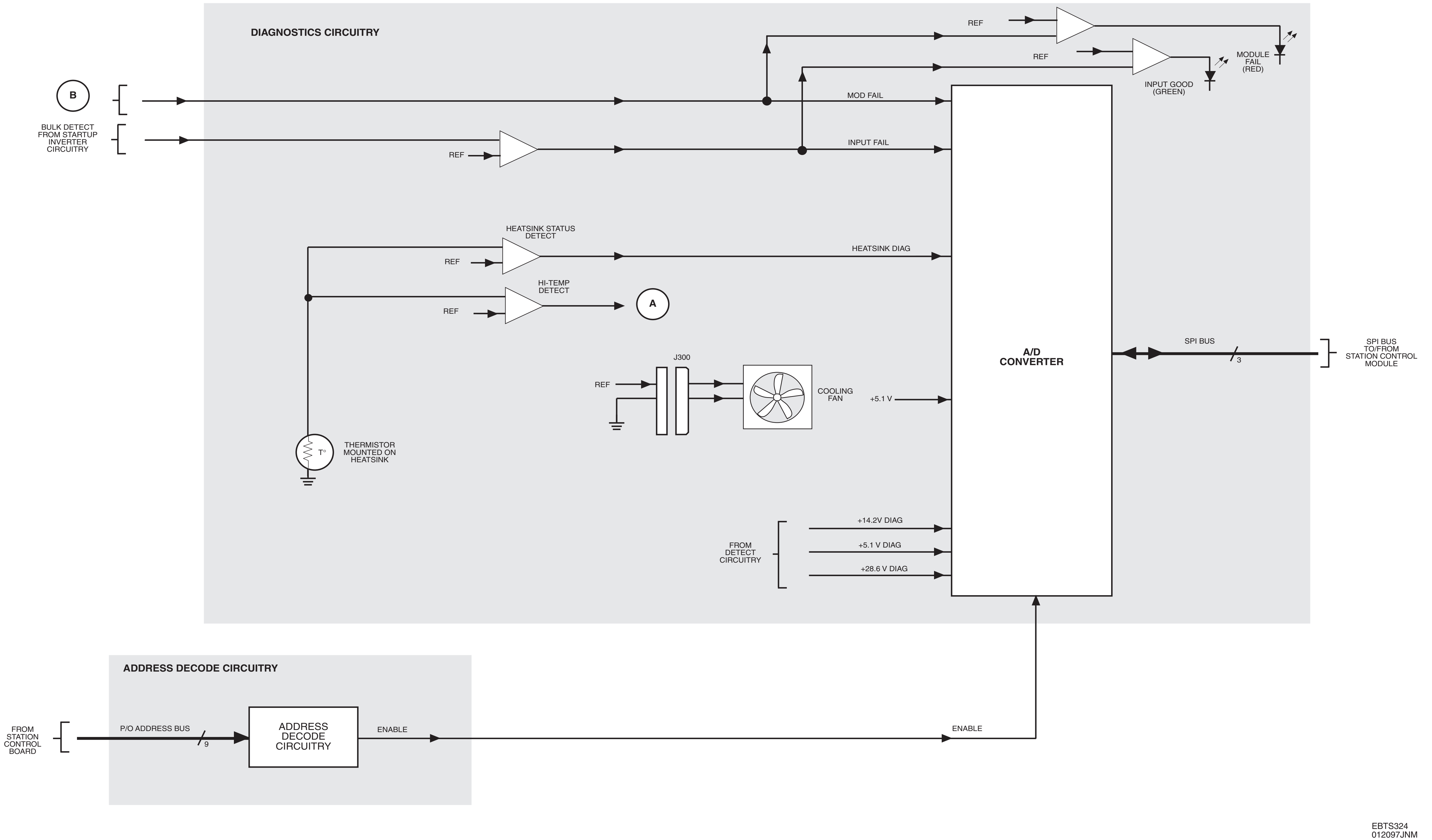


Figure 6 ***QUAD BR DC Power Supply Functional Block Diagram (Sheet 2 of 2)***

Receiver

Overview

This section provides technical information for the Receiver (RX).

FRU Number to Kit Number Cross Reference

Receiver (RX) Field Replaceable Units (FRUs) are available for the iDEN EBTS. The FRU contains the RX kit and required packaging. Table 1 provides a cross reference between RX FRU numbers and kit numbers.

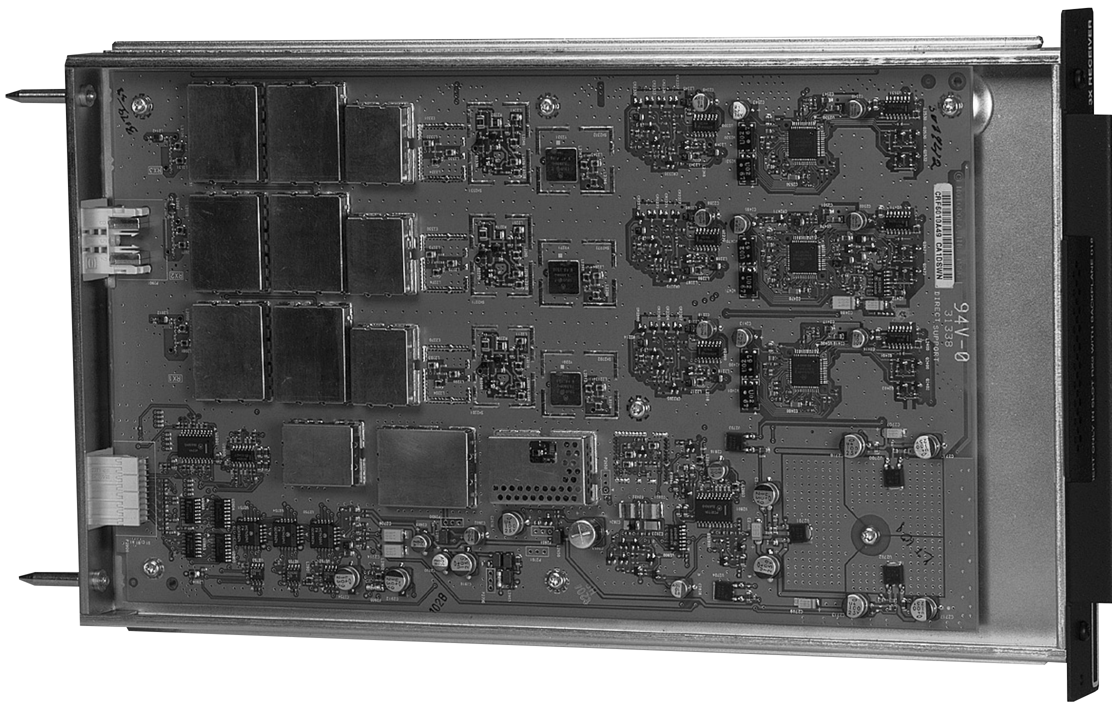
Table 1 ***FRU Number to Kit Number Cross Reference***

Description	FRU Number	Kit Number
3 branch Receiver for 800 MHz Single Channel BR	CLN1283	CLF1470
3 branch Receiver for 900 MHz Single Channel BR	CLN1356	CLF1480
Receiver for 1500 MHz Single Channel BR	TLN3427	CRX1020
3 Branch Receiver for 900 MHz QUAD Channel BT	DLN1201	CLF6453
3 branch Receiver for 800 MHz QUAD Channel BR	CLN1496	CLF1550

800 MHz 3X Receiver – CLN1283

800 MHz 3X Receiver Overview

The 3X Receiver provides the receiver functions for the Base Radio. It consists of a receiver board, a slide-in housing, and associated hardware. The 3X Receiver incorporates one to three diversity branches on a single module. Figure 1 shows a top view of the Receiver with the cover removed.



EBTS331
012197JNM

Figure 1 ***3X Receiver (with cover removed)***

800 MHz 3X Receiver Definition and Identification

The 3X receiver kit contains three receivers on a single board. This allows a single module to provide three-branch diversity BR functionality. To identify 3X receiver boards in the EBTS, use the MMI command **get_rx1_kit_no**. This command can be used on all receiver models, and reports the kit number from the receiver's EEPROM. The 3X receiver can also be identified by visual inspection of the front panel. Because the 3X receiver can only be inserted into the middle receiver slot, the front panel of a 3X receiver reads: **INSERT ONLY IN SLOT RX2 WITH BACKPLANE 0183625X 3X RECEIVER**.

The two remaining receiver slots are covered with blank panels. A summary of the Receiver FRUs available for the Base Radio is provided in the chart below.

Table 2 ***Receiver FRUs***

Receiver FRUs		Chassis FRUs	
3X Receiver: 800 MHz	CLN1283	With 3x Receiver Backplane: 800 MHz	CLN1282
Single Receiver: 800 MHz	TLN3336	With Single Receiver Backplane: 800 MHz	TLN3333

800 MHz 3X Receiver Replacement Compatibility

The 3X Receiver board (CRF6010 or CRF6030) can only be used in receive slot 2 (middle receiver slot) with backplane 0183625X _ _. The backplane connector is different than the TRF6560 version of the receiver board. This is why there is a need for a new backplane. The receiver will function only when it is installed in slot 2. The TRF6560 receiver will not make electrical connection in any slot of the new backplane. Compatibility between the new and old receiver boards is summarized in Tables 3 and 4 for 800 MHz Base Radios, respectively.

Table 3 ***800 MHz Base Radio Receiver Board/BR Backplane Compatibility***

	CRF6010 3X Receiver	TRF6560 Receiver
New backplane 0183265X--	Compatible	Not compatible
Old backplane 0182416W--	Not compatible	Compatible

Table 4 ***900 MHz Base Radio Receiver Board/BR Backplane Compatibility***

	CRF6030A 3X Receiver
New backplane 0183265X--	Compatible
Old backplane 0182416W--	Not compatible

800 MHz 3X Receiver Diversity Configuration

There is a new software parameter used for diversity purposes with the CLN1283 and CLN1356 3X Receivers. The parameter is the **rx_fru_config** parameter. The diversity issues to consider are described in the following paragraph. This parameter can be accessed through the MMI commands using the Motorola password. ROMs prior to version R06.06.17 do not support the **rx_fru_config** parameter. The ROM version in a base repeater can be checked using the MMI command **ver**. If a repeater contains the CRF6010 or CRF6030 receiver, the BRC board must be populated with a compatible version of ROM. Table 5 lists the ROM compatibilities.

Table 5 ***Receiver ROM Compatibility***

	CRF6010/CRF6030	TRF6560
ROM version R06.03.40	Not compatible	Compatible
ROM version R06.06.09	Not compatible	Compatible
ROM version R06.06.17	Not compatible	Compatible
ROM versions newer than R06.06.17	Compatible	Compatible

NOTE

When replacing FRUs, ensure that the ROM version on the BRC installed in the base radio is compatible with the ROM version on the Receiver.

NOTE

If downloaded code is used, then the downloaded code can be used to change the needed parameter (the **rx_fru_config** parameter).

800 MHz 3X Receiver Diversity Uses and Cautions

The 3X receiver board can be used in one, two, or three branch diversity systems. The number of active receivers is determined by the **rx_fru_config** parameter stored on the Base Radio Control (BRC) board. The **rx_fru_config** parameter is only valid, and must be set properly for, systems utilizing the CRF6010 or CRF6030 3X Receiver board. The **rx_fru_config** parameter is ignored by Base Radios that have ROM older than version R06.06.17 installed on the Base Radio Controller board.

To view the **rx_fru_config** parameter, use the MMI command **get rx_fru_config**. The configuration of each repeater can be changed in the field to match the number of receivers connected to antennas. To change the rx_fru_config parameter, use the command set **rx_fru_config yyy**, where yyy is the active receiver (yyy is 1 for one branch, 12 for two branch, and 123 for three branch diversity. For the iDEN system to work optimally, the **rx_fru_config** parameter must match the number of receivers connected to antennas.

▲ CAUTION

There will be significant system degradation if the **rx_fru_config** parameter is not properly set in systems with the CLN1283 or CLN1356 3X receiver kit.

Modifying Base Radios from Three Branch to Two Branch Diversity

NOTE

This procedure is applicable only to Base Radios equipped with the CRF6010 or CRF6030 3X Receiver Board.

When modifying a three branch Base Radio to a two branch Base Radio, it is important to observe all precautionary statements in the previous paragraph.

To modify a three branch Base Radio to a two branch Base Radio:

1. Disconnect the RF cable from the RX3 connector on the Base Radio.
2. Connect an SMA male load (Motorola part number 5882106P03) to the RX3 connector on the Base Radio.

   The SMA male load is required to limit the amount of radiated emissions.
3. Verify that the **rx_fru_config** parameter is set properly as described in the Diversity Uses and Caution paragraph above.

Modifying Base Radios from Two Branch to Three Branch Diversity

1. Remove the SMA male load from the RX3 connector of the Base Radio you wish to convert from two branch diversity to three branch diversity.
2. Connect the Receive Antenna #3 RF cable to the RX3 connector on the Base Radio.
3. Verify that the **rx_fru_config** parameter is set properly as described in the Diversity Uses and Cautions paragraph.

800 MHz 3X Receiver Theory of Operation

The Receiver performs highly selective bandpass filtering and dual down conversion of the station receive RF signal. A custom Receiver IC outputs the baseband information in a differential data format and sends it to the BRC.

Table 6 lists the Receiver circuitry and Figure 3 shows a functional block diagram for the Receiver.

Table 6 ***Receiver Circuitry***

Circuit	Description
Frequency Synthesizer Circuitry	Consists of a phase-locked loop and VCO. It generates the 1st LO injection signal for all three receivers.
Receiver Front-End Circuitry	Provides filtering, amplification, and the 1st down conversion of the receive RF signal. Digital step attenuators at the 1st IF are included in this block.
Custom Receiver IC Circuitry	Consists of a custom IC to perform the 2nd down conversion, filtering, amplification, and conversion of the receive signal. This block outputs the receive signal as differential data to the BRC.
Address Decode, A/D Converter, & Memory Circuitry	Performs address decoding for board and chip select signal, converts analog status signals to digital format for use by the BRC. A memory device holds module specific information.
Local Power Supply Regulation	Accepts +14.2 VDC input from the backplane interconnect board and generates two +10 VDC, a +11.5 VDC, and two +5 VDC signals for the receiver.

Frequency Synthesizer and VCO Circuitry

The synthesizer and VCO circuitry generate the RF signal used to produce the 1st LO injection signal for the first mixer in all the Receiver front end circuits. Functional operation of these circuits involves a Phase-Locked Loop (PLL) and VCO.

The PLL IC receives frequency selection data from the BRC module microprocessor via the SPI bus. Once programmed, the PLL IC compares a 2.1 MHz reference signal from the BRC with a feedback sample of the VCO output from its feedback buffer.

Correction pulses are generated by the PLL IC, depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference. The width of these pulses is dependent on the amount of difference between the 2.1 MHz reference and the VCO feedback.

The up/down pulses are fed to a charge pump circuit that outputs a DC voltage proportional to the pulse widths. This DC voltage is low-pass filtered and fed to the VCO circuit as the control voltage. The control voltage is between +2.5 VDC and +7.5 VDC.

The DC control voltage from the synthesizer is fed to the VCO, which generates the RF signal used to produce the 1st LO injection signal. The VCO responds to the DC control voltage by generating the appropriate RF signal. This signal is fed through a buffer to the 1st LO injection amplifier. A sample of this signal is returned to the PLL IC through a buffer to close the VCO feedback loop.

Receiver Front End Circuitry

The station receive RF signal enters the Receiver through the RF-type connector located on the back of the Receiver board. This signal is low-pass filtered and amplified. The amplified output is image filtered before being input to the 1st mixer. The signal mixes with the 1st LO injection signal to produce a 73.35 MHz 1st IF signal.

The 1st IF signal is sent through a 4-pole bandpass filter and fed to a buffer amplifier. The buffer amplifier output signal is 4-pole bandpass filtered again and the resultant signal is then passed through a digital attenuator. This attenuation is determined by the BRC. The resulting signal is then fed to the RF input of the custom receive IC.

Custom Receiver IC Circuitry

The custom Receiver IC provides additional amplification, filtering, and a second down-conversion. The 2nd IF signal is converted to a digital signal and is output via differential driver circuitry to the BRC. This data signal contains the necessary I and Q information, AGC information, and other data transfer information required by the BRC to process the receive signal.

The remainder of the custom Receiver IC circuitry consists of timing and tank circuits to support the internal oscillator, 2nd LO synthesizer circuitry, and 2nd IF circuitry.

A serial bus provides data communications between the custom Receiver IC and the DSP Glue ASIC (DGA) located on the BRC. This bus enables the DGA to control various current and gain settings, establish the data bus clock rate, program the 2nd LO, and perform other control functions.

Address Decode Circuitry

The address decode circuitry enables the BRC to use the SPI bus to select a specific device on a specific Receiver for control or data communication purposes.

If the board select circuitry decodes address lines A2 through A5 as the Receiver address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1 to generate the chip select signals for the EEPROM, A/D converter, and PLL IC.

Memory Circuitry

The memory circuitry consists of three EEPROMs located on the Receiver. The BRC performs all memory read and write operations via the SPI bus. Information stored in this memory device includes the kit number, revision number, module specific scaling and correction factors, and free form module information (scratch pad).

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the Receiver board are fed to the A/D converter. These analog signals are converted to a digital signal and are output to the BRC via the SPI lines upon request of the BRC.

Voltage Regulator Circuitry

The voltage regulator circuitry consists of two +10 VDC, a +10.8 VDC, and two +5 VDC regulators. The two +10 VDC and the +10.8 VDC regulators accept the +14.2 VDC input from the backplane interconnect board and generate the operating voltages for the Receiver circuitry.

The +10 VDC regulators each feed a +5 VDC regulator, one of which outputs Analog +5 VDC, and the other Digital +5 VDC operating voltages for use by the custom Receiver IC.

A +5.1 VDC operating voltage is also available from the backplane interconnect board to supply +5.1 VDC to the remainder of the Receiver circuitry.

800 MHz QUAD Receiver - CLN1283
900 MHz QUAD Receiver - DLN1201

QUAD Channel Receiver Overview

The QUAD Channel BR Receiver provides receiver functions for the QUAD Channel Base Radio. The QUAD Channel BR Receiver consists of a receiver board, a slide-in housing, and associated hardware. A single module of the QUAD receiver incorporates one to three diversity branches. Figure 2 shows a top view of the Receiver with the housing removed.

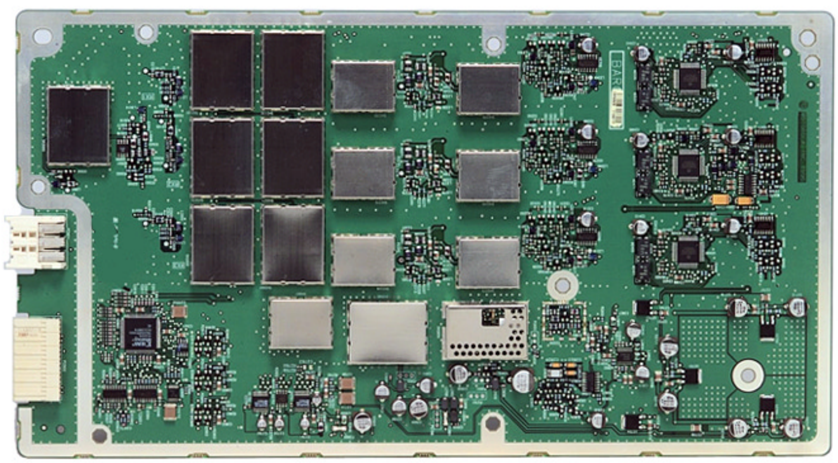


Figure 2 ***QUAD Receiver (with housing removed)***

QUAD Channel Receiver Diversity Uses and Cautions

The QUAD Channel BR Receiver board can be used in one, two, or three-branch diversity systems. The **diversity** parameter determines the number of active receivers. To view the **diversity** parameter, use the MMI command. **(See software commands.)** Each repeater's configuration can be changed in the field to match the number of receivers connected to antennas. To change the **diversity** parameter, use the command **(see software commands)**. For the iDEN system to work optimally, the **diversity** parameter must match the number of receivers connected to antennas.

▲ CAUTION

Improperly setting the **diversity** parameter will cause serious system degradation.

Modifying Base Radios from Three Branch to Two Branch Diversity

When modifying a three-branch Base Radio to a two-branch Base Radio, observing all precautionary statements in the previous paragraph is important.

To modify a three-branch Base Radio to a two-branch Base Radio:

1. Disconnect the RF cable from the RX3 connector on the Base Radio.
2. Connect an SMA male load (Motorola part number 5882106P03) to the RX3 connector on the Base Radio.

   The SMA male load is required to limit the amount of radiated emissions.
3. Verify that the **diversity** parameter is set properly, according to the Diversity Uses and Caution paragraph above.

Modifying Base Radios from Two Branch to Three Branch Diversity

1. Remove the SMA male load from the RX3 connector of the Base Radio that you wish to convert from two-branch diversity to three-branch diversity.
2. Connect the Receive Antenna #3 RF cable to the RX3 connector on the Base Radio.
3. Verify that the **diversity** parameter is set properly, according to the Diversity Uses and Cautions paragraph.

QUAD Channel Receiver Theory of Operation

The Receiver performs highly selective bandpass filtering and dual down conversion of the station receive RF signal. A custom Receiver IC outputs the baseband information in a differential data format and sends it to the BRC.

Table 7 lists the Receiver circuitry. Figure 4 shows a functional block diagram for the Receiver.

Table 7 ***QUAD Receiver Circuitry***

Circuit	Description
Frequency Synthesizer Circuitry	Consists of a phase-locked loop and VCO. It generates the 1st LO injection signal for all three receivers.
Receiver Front-End Circuitry	Provides filtering, amplification, and the 1st down conversion of the receive RF signal. This block includes digital step attenuators at the 1st IF.
Custom Receiver IC Circuitry	Consists of a custom IC to perform the 2nd down conversion, filtering, amplification, and conversion of the receive signal. This block outputs the receive signal as differential data to the BRC.
Address Decode, A/D Converter, & Memory Circuitry	Performs address decoding for board and chip-select signals. Converts analog status signals to digital format for use by the BRC. A memory device holds module-specific information.
Local Power Supply Regulation	Accepts +14.2 VDC input from the backplane interconnect board. Also generates two +10 VDC, a +11.5 VDC, and two +5 VDC signals for the receiver.

Frequency Synthesizer and VCO Circuitry

The synthesizer and VCO circuitry generate the RF signal used to produce the 1st LO injection signal for the first mixer in all the Receiver front end circuits. Functional operation of these circuits involves a Phase-Locked Loop (PLL) and VCO.

The PLL IC receives frequency selection data from the BRC module microprocessor via the SPI bus. Once programmed, the PLL IC compares a 2.1 MHz reference signal from the BRC with a feedback sample of the VCO output from its feedback buffer.

The PLL ICC generates correction pulses, depending on whether the feedback signal is higher or lower in frequency than the 2.1 MHz reference. The width of these pulses depends on the amount of difference between the 2.1 MHz reference and the VCO feedback.

The up/down pulses enter a charge pump circuit. The charge pump outputs a DC voltage proportional to the pulse widths. After low-pass filtering, this DC voltage enters the VCO circuit as the control voltage. The control voltage measures between +2.5 VDC and +7.5 VDC.

The DC control voltage from the synthesizer enters the VCO. The VCO generates the RF signal that the circuit uses to produce the 1st LO injection signal. The VCO responds to the DC control voltage by generating the appropriate RF signal. This signal passes through a buffer to the 1st LO injection amplifier. A sample of this signal returns to the PLL IC through a buffer to close the VCO feedback loop.

Receiver Front End Circuitry

The station receive RF signal enters the Receiver through the RF-type connector on the back of the Receiver board. The circuit low-pass filters and amplifies this signal. The amplified output passes through an image filter before entering the 1st mixer. The signal mixes with the 1st LO injection signal to produce a 73.35 MHz 1st IF signal.

The 1st IF signal passes through a four-pole, bandpass filter and enters a buffer amplifier. The buffer amplifier output signal again undergoes four-pole, bandpass filtering. The resultant signal then passes through a digital attenuator. The BRC determines the amount of attenuation. The resulting signal then enters the RF input of the custom Receiver IC.

Custom Receiver IC Circuitry

The custom Receiver IC provides additional amplification, filtering, and a second down-conversion. The IC converts the 2nd IF signal to a digital signal. The digital signal exits the receiver IC via differential driver circuitry, and passes to the BRC. This data signal contains I and Q information, AGC information, and other data transfer information. The BRC uses this information to facilitate processing of the receive signal.

The remainder of the custom Receiver IC circuitry consists of timing and tank circuits. These circuits support the internal oscillator, 2nd LO synthesizer, and 2nd IF circuitry.

A serial bus provides data communications between the custom Receiver IC and the DSP Glue ASIC (DGA). These circuits are on the BRC. The serial bus enables the DGA to perform several control functions...

- ❐ control various current and gain settings
- ❐ establish the data bus clock rate
- ❐ program the 2nd LO
- ❐ perform other control functions

Address Decode Circuitry

Address decode circuitry enables the BRC to use the SPI bus to select a specific device on a specific Receiver for control or data communication purposes.

If board-select circuitry decodes address lines A2 through A5 as the Receiver address, it enables the chip select circuitry. The chip select circuitry then decodes address lines A0 and A1. The decoding process generates the chip select signals for the EEPROM, A/D converter, and PLL IC.

Memory Circuitry

The memory circuitry consists of three EEPROMs located on the Receiver. The BRC performs memory read and write operations via the SPI bus. Information stored in this memory device includes...

- ❒ the kit number
- ❒ revision number
- ❒ module specific scaling and correction factors
- ❒ free form module information (scratch pad)

A/D Converter Circuitry

Analog signals from various strategic operating points throughout the Receiver board pass through the A/D converter. These analog signals become a digital signal. Upon request of the BRC, this signal travels to the BRC via the SPI lines.

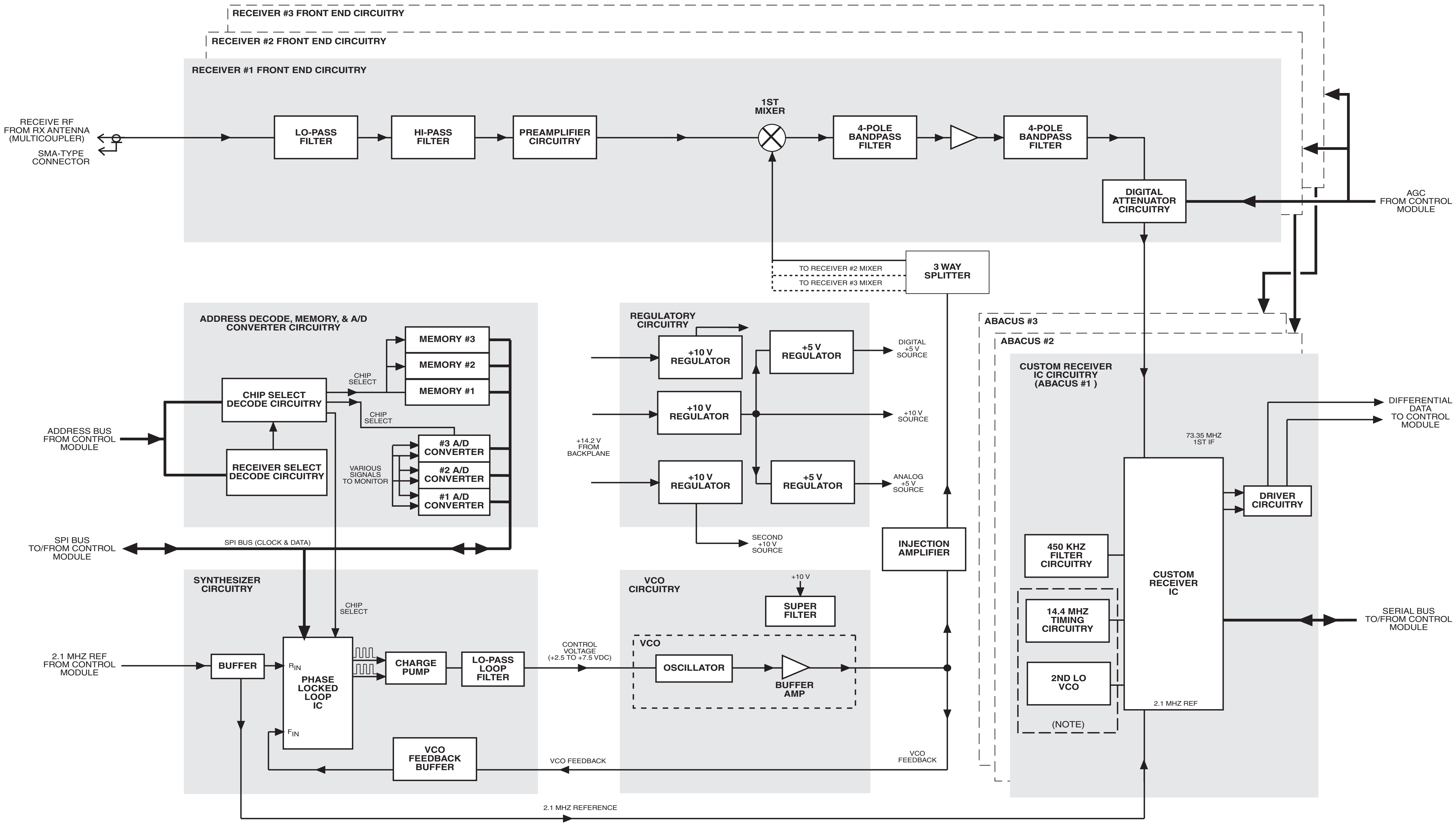
Voltage Regulator Circuitry

The voltage regulator circuitry consists of two +10 VDC, a +10.8 VDC, and two +5 VDC regulators. The two +10 VDC and the +10.8 VDC regulators accept the +14.2 VDC input from the backplane interconnect board. These regulators produce operating voltages for the Receiver circuitry.

The +10 VDC regulators each feed a +5 VDC regulator. One of these regulators outputs Analog +5 VDC. The other regulator outputs Digital +5 VDC operating voltages for use by the custom Receiver IC.

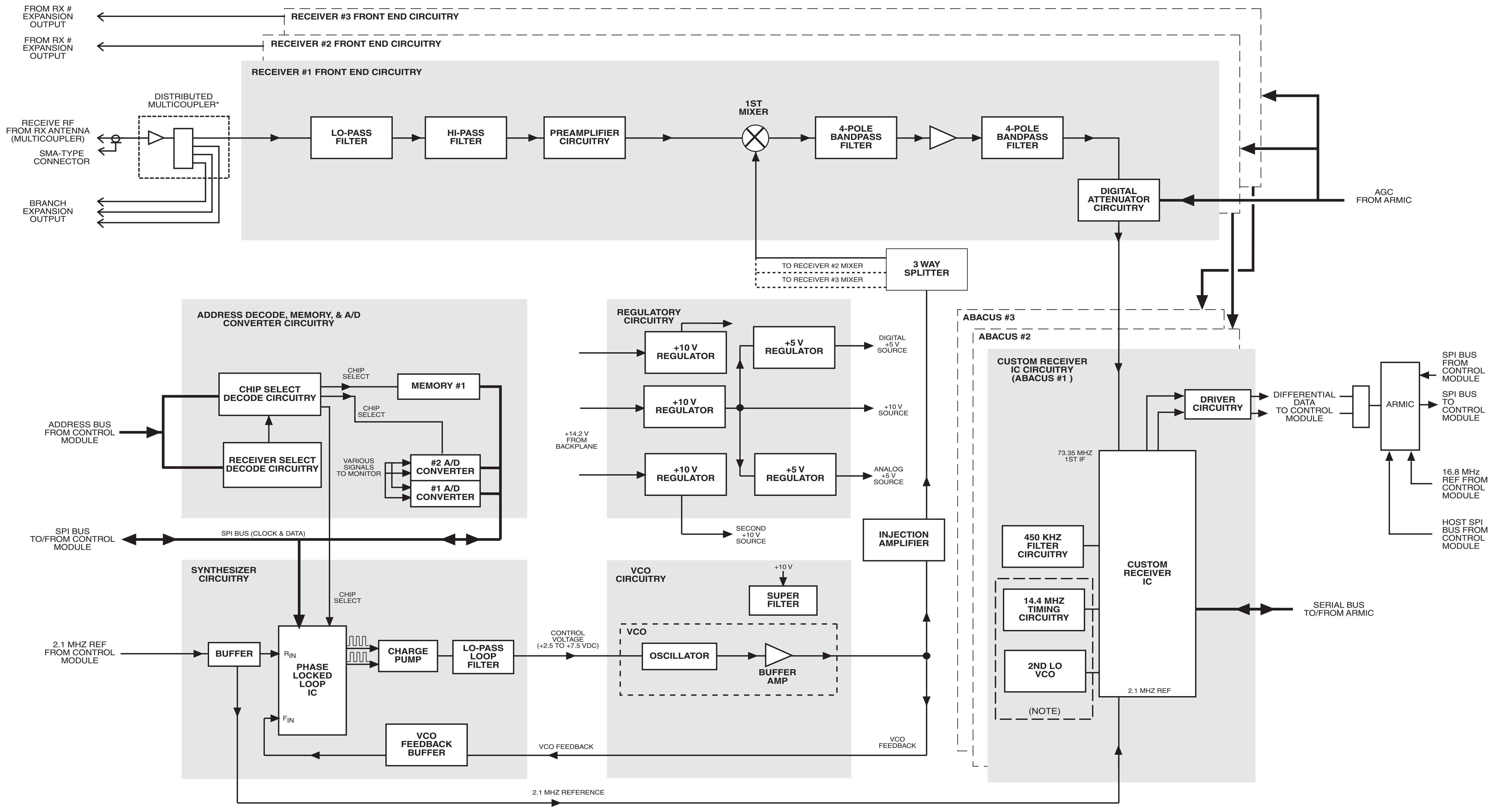
The backplane interconnect board also produces a +5.1 VDC operating voltage. This voltage powers the remainder of the Receiver circuitry.

3X Receiver
Functional Block Diagram



NOTE: 14.4 MHz TIMING CIRCUITRY AND 2ND LO VCO PRESENT ONLY ON ABACUS #2. FUNCTIONS ARE SHARED FOR ALL THREE ABACUS SECTIONS.

Figure 3 ***3X Receiver Functional Block Diagram***



NOTE: 14.4 MHz TIMING CIRCUITRY AND 2ND LO VCO PRESENT ONLY ON ABACUS #2. FUNCTIONS ARE SHARED FOR ALL THREE ABACUS SECTIONS.

* MULTICOUPLER BYPASSED ON CH4 RX

Figure 4 ***800 and 900 MHz QUAD Channel Receiver Functional Block Diagram***

MOTOROLA

Troubleshooting

Overview

This chapter is a guide for isolating Base Radio failures to the FRU level. There are three sections- one each for Generation 2 Single Channel Base Radios, QUAD Channel Base Radios and Legacy Single Channel Base Radios. Each section contains procedures for:

- ❒ Troubleshooting
- ❒ Verification/Station Operation

The maintenance philosophy for any Base Radio is to repair by replacing defective FRUs with new FRUs. This method limits down-time.

Two troubleshooting procedures are included. Each procedure is designed to quickly identify faulty FRUs.

Ship defective FRUs to a Motorola repair depot for repair.

NOTE

Any product damage resulting from improperly packaged equipment will not be covered under the standard Motorola warranty agreement.

Troubleshooting Preliminaries

Recommended Test Equipment

Table 1 lists recommended test equipment necessary for performing Base Radio troubleshooting/verification procedures.

Table 1 ***Recommended Test Equipment***

Test Equipment	Model Number	Use
Communications Analyzer	R2660 w/iDEN option	Used for checking receive and transmit operation (iDEN signaling capability) and station alignment
Dummy Load (50 Ω, 150 W)	none	Used to terminate output
Service Computer	IBM or clone, 80286 or better	Local service terminal
Portable Rubidium Frequency Standard	Ball Efratom	Frequency standard for R2660, netting TFR
Power Meter	none	Used to measure reflected and forward power
RF Attenuator, 250 W, 10 dB	Motorola 0180301E72	Protection for R2660
Software:		
Communication	Procomm Plus	Local service computer
File Compression	PKZip	Compress/Decompress data (Single Channel BR only)
RF Power Mete	HP438A	Used for calibration of the R2660 signal (QUAD BR only)
Low Power Sensor Head	HP8481D	Used in conjunction with Power Meter (QUAD BR only)

Troubleshooting Procedures

Many of the troubleshooting and station operation procedures require Man-Machine Interface (MMI) commands. These commands are used to communicate station level commands to the Base Radio via the RS-232 communications port located on the front of the BRC.

Routine Checkout

Procedure One is a quick, non-intrusive test performed during a routine site visit. Use this procedure to verify proper station operation without taking the station out of service. Figure 1 shows the Procedure One Troubleshooting Flowchart.

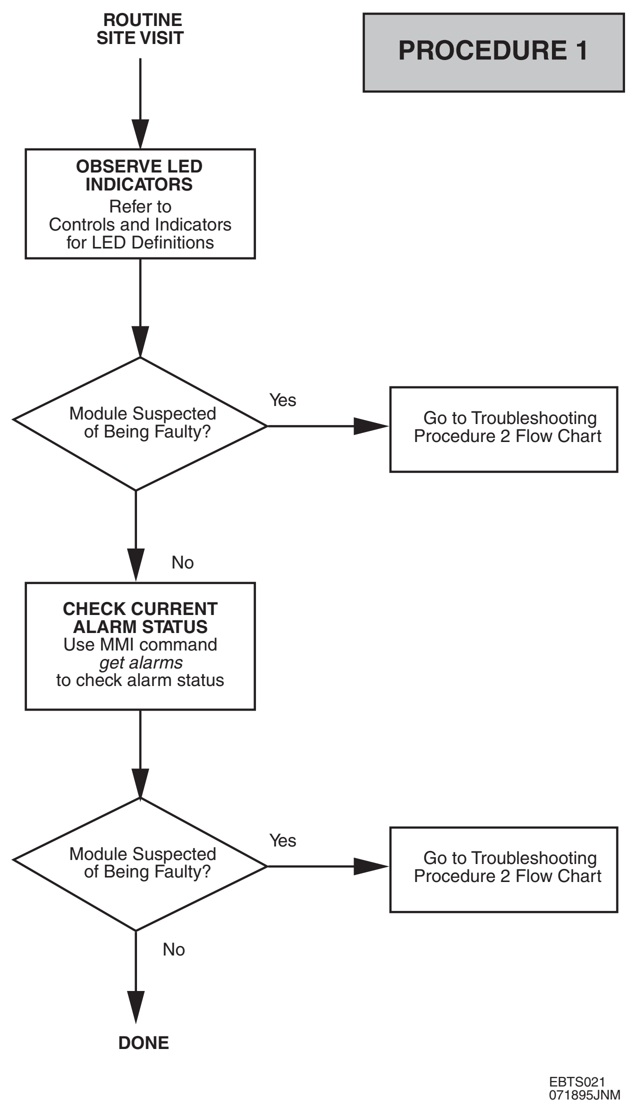


Figure 1 ***Procedure One Troubleshooting Flowchart***

Reported/Suspected Problem

Use Procedure Two to troubleshoot reported or suspected equipment malfunctions. Perform this procedure with equipment in service (non-intrusive) and with equipment taken temporarily out of service (intrusive).

Figure 2 shows the Procedure Two Troubleshooting Flowchart.

Troubleshooting Preliminaries

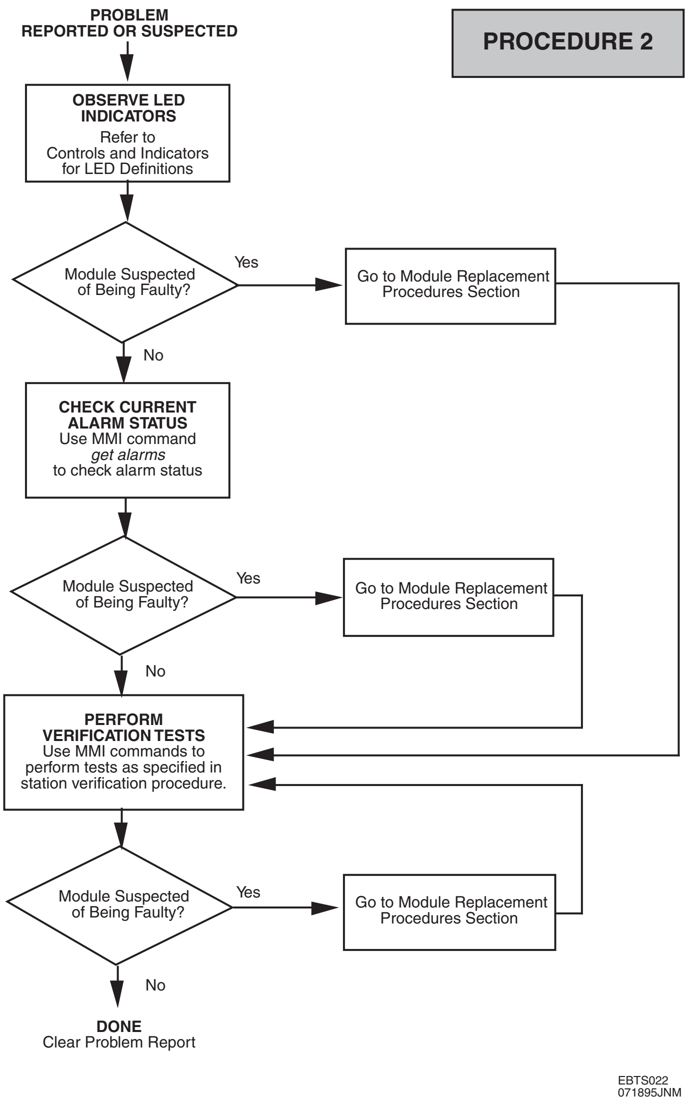


Figure 2 ***Procedure Two Troubleshooting Flowchart***

Generation 2 Single Channel Base Radio FRU Replacement Procedures

Replace suspected station modules with known non-defective modules to restore the station to proper operation. The following procedures provide FRU replacement instructions and post-replacement adjustments and/or verification instructions.

Generation 2 Single Channel Base Radio Replacement Procedure

NOTE

The Base Radio removal and installation procedures are included for reference or buildout purposes. Field maintenance of Base Radios typically consists of replacement of FRUs within the Base Radio. Perform Base Radio FRU replacement in accordance with "Base Radio FRU Replacement Procedure" below.

Perform Base Radio (BR) replacement as described in the following paragraphs.

Removal

Remove BR from Equipment Cabinet as follows:

1. Remove power from the Base Radio by setting the Power Supply ON/OFF switch to the OFF position.
2. Tag and disconnect the cabling from the BR rear panel connectors.
3. Remove the four M6 TORX screws which secure the BR front panel to the Equipment Cabinet mounting rails.

⚠ WARNING

BR WEIGHT EXCEEDS 60 LBS (27 KG). USE TWO-PERSON LIFT WHEN REMOVING OR INSTALLING BR FROM EQUIPMENT CABINET. MAKE CERTAIN BR IS FULLY SUPPORTED WHEN BR IS FREE FROM MOUNTING RAILS.

4. While supporting the BR, carefully remove the BR from the Equipment Cabinet by sliding the BR from the front of cabinet.

Installation

Install BR in Equipment Cabinet as follows:

1. If adding a BR, install side rails in the appropriate BR mounting position in the rack.
2. While supporting the BR, carefully lift and slide the BR in the Equipment Cabinet mounting position.
3. Secure the BR to the Equipment Cabinet mounting rails using four M6 TORX screws. Tighten the screws to 40 in-lb (4.5 Nm).
4. Connect the cabling to the BR rear panel connectors as tagged during the BR removal. If adding a BR, perform the required cabling in accordance with the Cabling Information subsection of the RFDS section applicable to the system.
5. Perform BR activation in accordance with Station Verification Procedures below.

Anti-Static Precautions

▲ CAUTION

The Base Radio contains static-sensitive devices. when replacing Base Radio FRUs, always wear a grounded wrist strap and observe proper anti-static procedures to prevent electrostatic discharge damage to Base Radio modules.

Motorola publication 68P81106E84 provides complete static protection information. This publication is available through Motorola National Parts.

Observe the following additional precautions:

- ❐ Wear a wrist strap (Motorola Part No. 4280385A59 or equivalent) at all times when servicing the Base Radio to minimize static build-up.
- ❐ A grounding clip is provided with each EBTS cabinet. If not available, use another appropriate grounding point.
- ❐ DO NOT insert or remove modules with power applied to the Base Radio. ALWAYS turn the power OFF using the Power Supply rocker switch on the front of the Power Supply module.
- ❐ Keep spare modules in factory packaging for transporting. When shipping modules, always pack in original packaging.

FRU Replacement Procedure

Perform the following steps to replace any of the Base Radio FRUs:

NOTE

When servicing Base Radios (BRs) in situations where the Control Board or the entire BR is replaced, the integrated Site Controller (iSC) will automatically reboot the serviced BR if the BR has been off-line for a period not less than the value contained in “Replacement BRC Accept Timer” (default is 3 minutes). If the BR is turned on prior to that time value, power the BR down and wait the minimum timer length before re-powering the BR.

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Loosen the front panel fasteners. These are located on each side of the module being replaced.
3. Pull out the module.
4. Insert the non-defective replacement module by aligning the module side rails with the appropriate rail guides inside the Base Radio chassis.
5. Gently push the replacement module completely into the Base Radio chassis assembly using the module handle(s).

▲ CAUTION

DO NOT slam or force the module into the chassis assembly. This will damage the connectors or backplane.

6. Secure the replacement module by tightening the front panel fasteners to the specified torque of 5 in-lbs.
7. Apply power to the Base Radio by setting the switch to the ON position.
8. Perform the Station Verification Procedure provided below.

Generation 2 Single Channel BR Power Amplifier (PA) Fan FRU Replacement

Perform the following steps to replace the Power Amplifier (PA) fans.

1. Remove the Power Amplifier from the Base Radio per FRU Replacement Procedure.
2. Disconnect fan power cable from PA housing.
3. Remove front panel from fan assembly.
4. Remove fan assembly from PA chassis.

NOTE

Reverse above procedure to install new fan kit.

Generation 2 Single Channel BR Station Verification Procedures

Perform the Station Verification Procedures whenever you replace a FRU. The procedures verify transmit and receive operations. Each procedure also contains the equipment set-up.

Generation 2 Single Channel BR Replacement FRU Verification

All module specific information is programmed in the factory prior to shipment. Base Radio specific information (e.g., receive and transmit frequencies) is downloaded to the Base Radio from the network/site controller.

Replacement FRU alignment is not required for the Base Radio.

Generation 2 Base Repeater FRU Hardware Revision Verification

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. Performing this procedure then minimizes or eliminates disruption of service to system users.

1. Connect one end of the RS-232 cable to the service computer.

2. Connect the other end of the RS-232 cable to the Service Access port, located on the front panel of the CNTL module.

3. After the BR is powered up using the front switch on the Power Supply Module, press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the field password, log in to the BR.

   To enter field mode, at the > prompt type **login -ufield.**

   After entering the correct field password, the `field>` prompt is displayed on the service computer.

   The default factory set field password is **motorola**.

NOTE

The ‘Out of Box’ default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

4. The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

5. Collect revision numbers from the station by typing the following command:

```
field> fv -oplatform
field>
```

6. If all modules return revision numbers of the format “Rxx.xx.xx”, then all revision numbers are present. In that case, verification requires no further action. If revision numbers return as blank, or not in the format “Rxx.xx.xx”, contact your local Motorola representative or Technical Support.

7. Set desired cabinet id and position and of BR by typing the following commands, with the final number on each command being the desired cabinet id and position. The command example below sets cabinet id to 5, and cabinet position to 2.

```
field> ci -oplatform -c5
field> pi -oplatform -p2

field>
```

8. After checking all BRs, log out by keying the following command:

```
field> logout
field>
```

Generation 2 Transmitter Verification

The transmitter verification procedure verifies the transmitter operation and the integrity of the transmit path. This verification procedure is recommended after replacing an Exciter, Power Amplifier, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of service to system users.

Equipment Setup

To set up the equipment, use the following procedure:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the Service Access port located on the front panel of the BRC.
4. Disconnect the existing cable from the connector labeled PA OUT. This connector is located on the backplane of the Base Radio.

⚠ CAUTION

Make sure power to BR is OFF before disconnecting transmitter RF connectors. Disconnecting transmitter RF connectors while the BR is keyed may result in RF burns from arcing.

5. Connect a test cable to the PA OUT connector.

6. Connect a 10 dB attenuator on the other end of the test cable.

7. From the attenuator, connect a cable to the RF IN/OUT connector on the R2660 Communications Analyzer.

8. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.

9. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

10. Set the R2660 to the EXT REF mode.

11. Apply power to the R2660.

12. Set the R2660 to the SPECTRUM ANALYZER mode with the center frequency set to the transmit frequency of the Base Radio under test.

13. Perform the appropriate transmitter verification procedure below for the particular Power Amplifier used in the Base Radio.

Transmitter Verification Procedure

This procedure provides commands and responses to verify proper operation of the transmit path for 800 MHz Base Radios.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the field password**,** login to the BR.

To enter field mode, at the > prompt type **login -ufield.**

After entering the correct field password, the field> prompt is displayed on the service computer.

The default factory set field password is **motorola**.

NOTE

The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Dekey the BR to verify that no RF power is being transmitted. Set the transmit DSP test mode to "stop." At the BRC> prompt, type:

```
field> power -otxch1 -p0
field> ptm -otx_all -mstop
```

NOTE

The following command keys the transmitter. Make sure that transmission only occurs on licensed frequencies or into an RF dummy load.

3. Key the BR to 40 watts, following the steps below from the BRC> prompt:

   3.1 Set the transmitter frequency.

```
field> freq -otxch1 -f860
```

   3.2 Enable the channel by setting a data pattern to “iden”

```
field> dpm -otxch1 -miden
```

NOTE

After the following command is entered, power will be transmitted at the output of the Power Amplifier.

   3.3 Set the transmit power to 40 watts and key the BR.

```
field> ptm -otx_all -mdnlk_framed
field> power -otxch1 -p40
```

4. After keying the Base Radio, verify the forward and reflected powers of the station along with the station VSWR with the parameters listed in Table 2.

Table 2 ***Generation 2 BR Transmitter Parameters***

Parameter	Value or Range
Forward Power	Greater than 36 Watts
Reflected Power	Less than 2.0 Watts
VSWR	Less than 1.6:1

NOTE

The reported value for forward power is not indicative of Base Radio performance. This value is reported from the internal wattmeter. These limits are only for verification of operation and are not representative of true operating power of the transmitter.

4.1 At the BRC> prompt, type:

```
field> power -otx_all
```

This command returns all active alarms of the Base Radio.

4.2 At the BRC> prompt, type:

```
field> alarms -ofault_hndlr
```

If the **alarms** command displays alarms, refer to the System Troubleshooting section of this manual for corrective actions.

5. View the spectrum of the transmitted signal on the R2660 Communications Analyzer in the Spectrum Analyzer mode. Figure 5 shows a sample of the spectrum.

Generation 2 Single Channel BR Station Verification Procedures

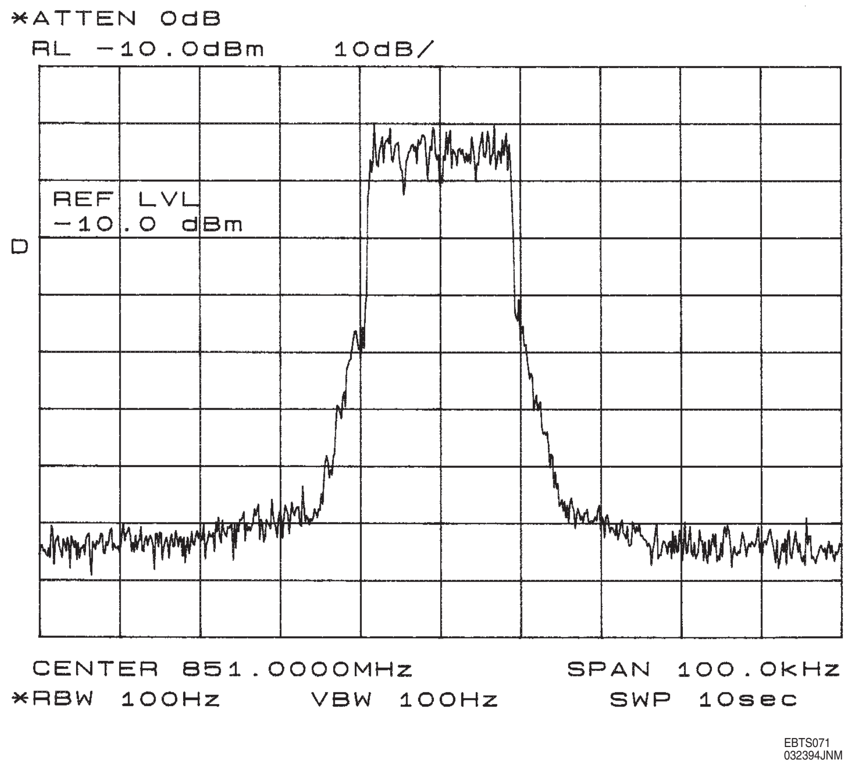


Figure 3 ***Generation 2 Carrier Spectrum***

6. Dekey the BR to verify no RF power is being transmitted. Set the transmit DSP test mode to “stop.” At the field> prompt, type:

```
field> power -otxch1 -p0
field> ptm -otx_all -mstop
```

Equipment Disconnection

Use the following steps to disconnect equipment after verifying the transmitter.

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Disconnect the RS-232 cable from the connector on the service computer.
3. Disconnect the other end of the RS-232 cable from the RS-232 connector located on the front panel of the BRC.

⚠ CAUTION

Make sure power to BR is OFF before disconnecting transmitter RF connectors. Disconnecting transmitter RF connectors while the BR is keyed may result in RF burns from arcing.

4. Disconnect the test cable from the PA OUT connector located on the backplane of the Base Radio.
5. Connect the standard equipment cable to the PA OUT connector.
6. Disconnect the 10 dB attenuator from the other end of the test cable.
7. From the attenuator, disconnect the cable to the R2660 Communications Analyzer.
8. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.
9. If necessary, continue with the Receiver Verification Procedure.

Receiver Verification Procedure: Generation 2 Base Radio with RFDS

This procedure provides commands and responses to verify proper operation of the Base Radio receiver paths. Perform the procedure on all four channels in each Base Radio in the EBTS.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the front of the EX/BRC module. Using the terminal

program on the service computer, log onto the BR. Bold type indicates user input commands.

To enter field mode, at the > prompt type **login -ufield.**

After entering the correct field password, the field> prompt is displayed on the service computer.

The default factory set field password is **motorola**.

NOTE

The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Set the Frequency of the R2660 to 810MHz. Power out should be set to –80 dBm.

3. Set the channel frequency.

```
field> freq -orxch1 -f810
```

4. Verify the R2660 signal level:

```
field> enable -orxch1 -dbr1 -son
field> ppc -orxch1 -mchn -s1
field> ppr -orxch1 -r1 -a50
```

5. The resulting output will look similar to this:

```
field> ppr -orxch1 -r1 -a100

SGC Atten.(dBm)=0.000000
Freq. Offset=-15.059323
Sync. Attempts=1.000000
Sync. Successes=1.000000
BER%=0.000000
RX Path1 RSSI=-80.934021
RX Path2 RSSI=-127.012520
RX Path3 RSSI=-127.012520
Chn sig. strength=-57.098698
Chn intf. strength=-91.696739

field>
```

NOTE

RX Path1 RSSI must read -80dBm ±1dBm for the BER Floor verification to be accurate. Adjust the output level of the R2660 to compensate for loss in the test cables and three-way splitter.

BER Floor Measurement: Generation 2 Base Radio with RFDS

1. Verify that the R2660 is set to 810MHz and is producing a power level of -80dBm. (See “Receiver Verification Procedure: QUAD Base Radio with RFDS” on page 63.)

2. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 0.01%, the receiver has passed the test.

3. Check Receiver 1. At the prompt, type (inputs are in bold, comments are in italics):

```
field> freq -orxch1 -f810
field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppc -orxch1 -mchn -s1
field> ppr -orxch1 -a1000 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -db3 -son
field> ppr -orxch1 -a1000 -r1
```

4. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

5. As shown below respectively for 800 MHz Generation 2 Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Receiver Sensitivity Measurement: Generation 2 Base Radio with RFDS

The receiver sensitivity measurement consists of sending a calibrated RF level of -113.5dBm to the antenna ports at the top of the rack. This includes the RFDS in the receive channel and measures the combined performance of the Base Radio and the RFDS. The R2660 output must be calibrated prior to the taking of this measurement.

Calibration of the R2660 output level

1. Verify that the R2660 is set to 810MHz and adjust the output power to a level of -50dBm

2. Calibrate HP438A Power Meter. Refer to the HP users guide that came with the Meter. Below is a general procedure that can be followed.

   2.1 Attach 8481D Power Sensor to the Sensor input on the front of the 437B.

   2.2 Attach the included HP 11708A 30dB pad to the Power input on the front on the 473B.

   2.3 Power on the 437B.

   2.4 Connect the Power Meter to the female end of the 30dB pad extruding from the Power input.

   2.5 Press the “Zero” button on the 437B.

   2.6 Wait for Zeroing operation to complete.

   2.7 Press “Shift-Zero” to enter the Cal value. This is listed as CF on the Power Sensor.

   2.8 Wait for Cal operation to complete.

   2.9 Press “Shift-Freq” to enter the Cal Factor. This is listed as Cf in a chart vs. freq on the Power Sensor. Choose the closest frequency range for the application. For 800MHz measurements, interpolate between 1.0GHz and 0.5GHz to obtain a Cf of 99.0

   2.10 For measurement of iDEN or Tornado 6:1 waveforms, press “Offset” and enter 7.78dB.

3. Disconnect Cable A (see Figure 7 on page -62) from the Base Radio and connect it to the Power Sensor Head.

4. Increase the power level on the R2660 until the HP 437B Power Meter reads -50dB.

5. Record the DISPLAYED power level of the R2660 as Calfactor A.

6. The path loss through the cable and splitter system is Calfactor A + 50.

    Example: R2660 reads -44dBm

    HP 437B reads -50dBm

    Calfactor A = -44, path loss = 6dB

7. Path loss must be determined for each Antenna cable A,B,C (see Figure 7 on page -62). If comparable cables are used for all three the path losses of all three should be the same.

8. Additional power will be added to the R2660 in the sensitivity measurement to balance out the additional path loss value.

9. Reconnect cables A,B,C (see Figure 7 on page -62) to Antenna Ports 1,2,3.

10. Set the R2660 to Frequency 810MHz and a Power level of -113.5dBm + path loss.

    Example: If your path loss was 6dB, set the R2660 to-107.5dBm.

11. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 8.00%, the receiver has passed the test.

```
field> freq -orxch1 -f810
field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppc -ortch1 -mchn -s1
field> ppr -orxch1 -a100 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -db3 -son
field> ppr -orxch1 -a100 -r1
```

12. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

13. As shown below respectively for 800 MHz Generation 2 Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Receiver Verification: Measurement of the Generation 2 Base Radio (No RFDS)

The receiver verification procedure sends a known test signal into the Base Radio to verify the receive path. The signal is fed DIRECTLY into the ANTENNA PORTS in the back of the Base Radio. This excludes the RFDS and antenna cabling from the measurement. This verification procedure is recommended after replacing a Receiver, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the base radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of services to system users.

Equipment Setup

Set up the equipment for the receiver verification as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.
4. Disconnect the existing cables from the connectors labeled RX1, RX2, and RX3 on the back of the Base Radio. If the radio is configured for 2 Branch diversity, disconnect the RX1 and RX2 cables.
5. Connect test cables from each of the RX1, RX2, and RX3 connectors (Cables A,B,C in Figure 8) to the input ports of the 3-way splitter. For 2 Branch diversity tests, load the RX3 cable with an appropriate 50ohm load or connect it to the RX3 antenna port on the radio.

6. Connect an additional test cable (Cable D in Figure 7 on page -62) from the summed port of the 3-way splitter to the RF IN/OUT connector on the R2660 Communications Analyzer.

7. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.

8. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

9. Set the R2660 to the EXT REF mode

.

10. Apply power to the R2660.

Receiver Verification Procedure: Generation 2 Base Radio

This procedure provides commands and responses to verify proper operation of the Base Radio receiver paths. Perform the procedure on the receiver in each Base Radio in the EBTS.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the front of the EBRC module. Using the terminal program on the service computer, log onto the BR. Bold type indicates user input commands.

   To enter field mode, at the > prompt type **login -ufield.**

   After entering the correct field password, the `field>` prompt is displayed on the service computer.

   The default factory set field password is **motorola**.

NOTE

The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Set the Frequency to of the R2660 to 810MHz. Power out should be set to –80 dBm.

3. Enable Global Synchronization.

```
field> es -orx_all -tglobal
field> freq -orxch1 -f810
```

4. Disable System Gain.

```
field> sge -orx_all -soff
```

NOTE

This step should only be performed if the Base Radio is being connected directly to the Base Radio Antenna ports. If verification is being performed at the top of the rack (adding an RFDS), disregard the above command.

5. Verify the R2660 signal level.

```
field> enable -orxch1 -dbr1 -son
field> ppc -orych1 -mchn -s1
field> ppr -orxch1 -r1 -a100
```

6. The resulting output will look similar to this:

```
field> ppr -orxch1 -r1 -a100

SGC Atten.(dBm)=0.000000
Freq. Offset=-15.059323
Sync. Attempts=1.000000
Sync. Successes=1.000000
BER%=0.000000
RX Path1 RSSI=-80.934021
RX Path2 RSSI=-127.012520
RX Path3 RSSI=-127.012520
Chn sig. strength=-57.098698
Chn intf. strength=-91.696739
field>
```

NOTE

RX Path1 RSSI must read -80dBm ± 1dBm for the BER Floor verification to be accurate. Adjust the output level of the R2660 to compensate for loss in the test cables and three-way splitter.

BER Floor Measurement: Generation 2 Base Radio

1. Verify that the R2660 is set to 810MHz and is producing a power level of -80dBm. (See “Receiver Verification Procedure: Generation 2 Base Radio” on page 25.)
2. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 0.01%, the receiver has passed the test.
3. Check Receiver. At the prompt, type (inputs are in bold, comments are in italics):

```
field> ppc -orxch1 -mchn -s1
field> freq -orxch1 -f810

field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a1000 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -db3 -son
field> ppr -orxch1 -a1000 -r1
```

4. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

5. As shown below respectively for 800 MHz Generation 2 Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the BRC> prompt, type:

```
field> fc –oplatform
```

Receiver Sensitivity Measurement: Generation 2 Base Radio

1. Verify that the R2660 is set to 810MHz and adjust the output power to a level of -50dBm.

2. Calibrate HP438A Power Meter. Refer to the HP users guide that came with the Meter. Below is a general procedure that can be followed.

   2.1 Attach 8481D Power Sensor to the Sensor input on the front of the 437B.

   2.2 Attach the included HP 11708A 30dB pad to the Power input on the front on the 473B.

   2.3 Power on the 437B.

   2.4 Connect the Power Meter to the female end of the 30dB pad extruding from the Power input.

   2.5 Press the "Zero" button on the 437B.

   2.6 Wait for Zeroing operation to complete.

   2.7 Press "Shift-Zero" to enter the Cal value. This is listed as CF on the Power Sensor.

   2.8 Wait for Cal operation to complete.

   2.9 Press "Shift-Freq" to enter the Cal Factor. This is listed as Cf in a chart vs. freq on the Power Sensor. Choose the closest frequency range for the application. For 800MHz measurements, interpolate between 1.0GHz and 0.5GHz to obtain a Cf of 99.0

   2.10 For measurement of iDEN or Tornado 6:1 waveforms, press "Offset" and enter 7.78dB.

3. Disconnect Cable A (see Figure 7 on page -62) from the Base Radio and connect it to the Power Sensor Head.

4. Increase the power level on the R2660 until the HP 437B Power Meter reads -50dB.

5. Record the DISPLAYED power level of the R2660 as Calfactor A.

6. The path loss through the cable and splitter system is Calfactor A + 50.

   Example: R2660 reads -44dBm

   HP 437B reads -50dBm

   Calfactor A = -44, path loss = 6dB

7. Path loss must be determined for each Antenna cable A,B,C (see Figure 7 on page -62). If comparable cables are used for all three, the path losses of all three should be the same.

8. Additional power will be added to the R2660 in the sensitivity measurement to balance out the additional path loss value.

9. Reconnect cables A,B,C (see Figure 7 on page -62) to Antenna Ports 1,2,3.

10. Set the R2660 to Frequency 810MHz and a Power level of -108dBm + path loss.

    Example: If your path loss was 6dB, set the R2660 to -102dBm.

11. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 8.00%, the receiver has passed the test.

```
field> ppc -orxch1 -mchn -s1
field> freq -orxch1 -f810

field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a100 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -db3 -son
field> ppr -orxch1 -a100 -r1
```

12. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

13. As shown below respectively for 800 MHz Generation 2 Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Equipment Disconnection

Disconnect equipment after verifying the receiver as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Disconnect the RS-232 cable from the connector on the service computer.
3. Disconnect the other end of the RS-232 cable from the RS-232 connector on the front panel of the BRC.
4. Disconnect the test cable from the RX 1 connector located on the backplane of the Base Radio.
5. Connect the standard equipment cable to the RX 1 connector.
6. Disconnect the cable to the R2660 Communications Analyzer.
7. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.

   This completes the Receiver Verification Procedure for the receiver.

Generation 2/EBRC Single Channel Base Radio Backplane

Backplane Signals

Table 3 provides a list of all signals routed on the backplane interconnect board.

Table 3 ***BR Backplane Signal Descriptions***

Signal	Description
GND	Station Ground
28.6 V	28.6 VDC Output from PS
14.2 V	14.2 VDC Output from PS
5.1 V	5.1 VDC Output from PS
A0, A1, A2, A3, A4, A5, A6**	The BRC uses these lines to address station modules and devices on those modules
SPI_MOSI	Serial Processor Interface- Master out, slave in Data
SPI_MISO	Serial Processor Interface- Master in, slave out Data
SPI_CLK	Serial Processor Interface- Clock Signal (100 KHz- 1MHz)
ACG1, ACG2, ACG3, ACG4	BRC uses these lines to set digital attenuators on the receiver(s) for SGC functionality
2.1MHZ_RX	2.1 MHz generated on the BRC and used as a reference by the Receiver(s)
2.1MHZ_TX	2.1 MHz generated on the BRC and used as a reference by the Exciter
DATA1, DATA1*	This differential pair carries Receiver 1 data to the Base Radio Controller
DATA2, DATA2*	This differential pair carries Receiver 2 data to the Base Radio Controller
DATA3, DATA3*	This differential pair carries Receiver 3 data to the Base Radio Controller
ODC_1, ODC_2, ODC_3	Clocks used to clock differentiual receive data from each respective receiver to the BRC
SBI_1,S BI_2, SBI_3	Serial Bus Interface - these lines are used to program the custom receiver IC oin each receiver
SSI, SSI*	Differentiual transmit data from the Exciter to the BRC
CLK, CLK*	Differential Data clock used to clock transmit data from the BRC to the Exciter
VBLIN	Programmable bias voltage generated on the Exciter and used to bias PA stages
RESET*	Output from BRC to Exciter
EXT_VFWD	DC voltage representing the forward power at the antenna as measured by the external watt meter
EXT_VREF	DC voltage representing the reflected power at the antenna as measured by the external watt meter.
WP*	Write protect line used by the BRC to write serial EPROMs located on each module
BAT_STAT	Binary flag used to signal BRC to monitor the External battery supply alam
METER_STAT	Binary Flag used by the BRC to indicate to the BRC it should monitor
PA_ENABLE*	The BRC uses this line to control PA bias.
1PPS	Global Positioning System- 1 pulse per second (this may be combined with 5 MHz at the site frequency reference)

Table 3 ***BR Backplane Signal Descriptions***

Signal	Description
RCLK	RS-232- Receive Clock
TCLK	RS-232- Transmit Clock
CTS	RS-232- Clear To Send
RTS	RS-232- Request To Send
CD	RS232- Carrier Detect
RxD	RS232- RX Data
TxD	RS232- TX Data
BRG	RS-232 Baud Rate Generator
5 MHZ / Spare	signal not currently used
EXCITER OUT	Forward transmit path QQAM at approximately an 11 dBm level
EXCITER_FEEDBACK	Signal comes from PA at approximately 16 dBm. Used to close the cartesian RF_LOOP
PA_IN	4 dBm QQAM forward path of the transmitter
PA_FEEDBACK	Signal to the Exciter at approximately 16 dBm. Used to close the cartesian RF_LOOP
Rx1_IN	RF into Receiver 1
Rx2_IN	RF nto Receiver nto Receiver 2
Rx3_IN	RF nto Receiver 3
5MHZ REFERENCE	5 MHZ Station/Site reference. Signal comes from the redundant site frequency reference and usually is multiplexed with the 1 PPS signal from the Global Positrioning Satellite input to the site frequency reference.
ETHERNET	Interface between the BRC and the ACG. This connects the Base to the 10 MHz LAN
SCR_SHUT	Not Used
SCR_THRESH	Not Used
RELAY ENABLE	Not Used
SHUTDOWN	Input signal from the BRC to the Power Supply. Used to exercise a station “hard start”
28V_AVG	Not Used
BATT_TEMP	Not Used
NOTE: *= enabled low **NOTE:** ** SPI address A6 was added to enable additional SPI addresses. The Eciter only needs to be changed if the change is required to take advantage of additional SPI addresses. A6 pin A13 should be a NO CONNECT to enable A6 functionality on other modules.	

Generation 2 Single Channel BR Backplane Connections

All external equipment connections are made on the Base Radio backplane. Table 4 lists and describes each of the connectors on the backplane.

Table 4 ***Generation 2 Base Radio Backplane Connectors***

Connector	Module	Description	Type
P1	EBRC	Signal	96 pin EURO
P2	Rx	Signal	48 pin AMP Z-Pack Futurebus
P3	Rx	RF	Harting Harpac
P4	not used	not used	not used
P5	EX	Signal	96 pin EURO
P6	PA	Signal	96 pin EURO
P7	External/Alarm	Signal	DB25
P8	External/RS232	Signal	DB9
P9	PS	Signal	78 pin AMP Teledensity
P10	Ethernet B/5 MHz Spare	not used/not populated	BNC blindmate
P11	Ethernet	Signal	BNC Blindmate
P12	DC Input	-48 VDC IN (not part of the backplane assembly)	8 pin AMP 530521-3
P13	5 MHz/ 1 PPS	Signal	BNC
P14	External/EX	RF (EX to PA)	SMA blindmate
P15	External/EX	EX Feedback	SMA blindmate
P16	External/PA	PA Feedback	SMA blindmate
P17	External/PA	PA IN	SMA blindmate
P18	External/PA	PA OUT	SMA blindmate
P19	Rx Branch 1	RF	SMA
P20	Rx Branch 2	RF	SMA
P21	Rx Branch 3	RF	SMA

Figure 4 shows the locations of the Generation 2 Base Radio external connections.

Generation 2/EBRC Single Channel Base Radio Backplane

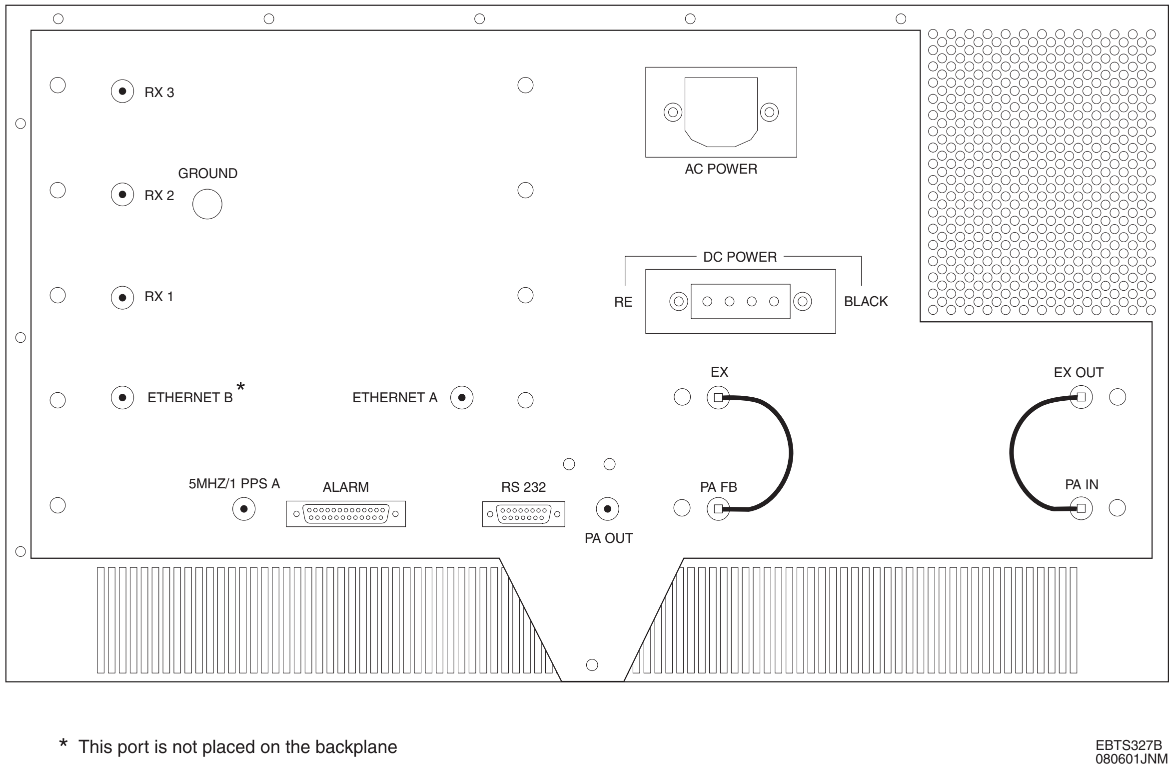


Figure 4 ***Generation 2 Base Radio Backplane Connectors***

Generation 2 Single Channel BR Backplane Connector Pinouts

Table 5 lists the pin-outs for the 96-PIN P1 connector. P1 provides power, digital signal, and analog signal interconnect to the BRC.

Table 5 ***P1 Gen 2/BR Connector Pin-outs***

Pin	Row A	Row B	Row C
1	AGC3	28.6 VDC	AGC1
2	AGC4	14.2 VDC	AGC2
3	GND	GND	GND
4	RESET*	GND	GND
5	BATT_STAT	GND	GND
6	CTS	GND	GND
7	RTS	5.1 VDC	5.1 VDC
8	5.1 VDC	5.1 VDC	5.1 VDC
9	5.1 VDC	5.1 VDC	5.1 VDC
10	SHUTDOWN	5.1 VDC	
11	RCLK	5.1 VDC	DATA1
12	ODC_1	5.1 VDC	DATA1*
13	TCLK	GND	DATA3
14	ODC_3	GND	DATA3*
15	RxD	GND	DATA2
16	ODC_2	BP ID_0	DATA2*
17	TxD	BP ID_1	A6
18	SSI	EXT_GPI_1	SBI_1
19	SSI*	EXT_GPO_1*	SBI_3
20	BRG	GND	SBI_2
21	CLK	EXT_GPI_2′*	EXT_GPO_2*
22	CLK*	GND	A4
23	GND	PA_ENABLE*	A3
24	A5	GND	A2
25	A0	GND	A1
26	CD	GND	5MHZ/1PPS (5 MHz SPARE)
27	METER_STAT	GND	SPI_MISO
28	WP*	GND	SPI_CLK
29	GND	GND	SPI_MOSI
30	GND	GND	GND
31	1PPS_GPS	GND	2.1MHZ_TX
32	GND	GND	2.1MHZ_RX
NOTE: * = enabled low			

Table 6 lists 48-PIN P2 3X Receiver pin-outs

Table 6 ***Gen 2 BR P2 Rx Signal Connector Pinouts***

Pin	Row A	Row B	Row C	Row D
1	GND	AGC4	AGC3	A6
2	GND	AGC2	AGC1	A0
3	GND	RX1_DATA1	RX1_DATA1*	A1
4	GND	RX1_SBI	RX1_ODC	A2
5	GND	RX2_DATA	RX2_DATA*	A3
6	5.1 VDC	RX2_SBI	RX2_ODC	A4
7	GND	RX3_DATA	RX3_DATA*	A5
8	GND	RX3_SBI	RX3_ODC	WP*
9	14.2 VDC	SPI_SCLK	SPI_MOSI	SPI_MISO
10	14.2 VDC	GND	GND	GND
11	14.2 VDC	GND	2.1MHZ_RX	GND
12	GND	GND	GND	GND

NOTE: * Enabled low

NOTE: Row A is the lowest row of pins. Pins on Row A are longer for mate first and break last connection

NOTE: Pin1, Row D was changed from Ground to A6 between Legacy and Gen2 BR

Table 7 lists the 48-pin P3 pin-outs for the 3X Receiver.

Table 7 ***Gen 2 BR P3 3X Receiver Pin-outs***

Pin	Row A	Row B	Row C	Row D	Row E
1	GND		GND		GND
2		RX1			
3	GND		GND		GND
4					
5					
6					
7	GND		GND		GND
8		RX2		RX3	
9	GND		GND		GND

NOTE: All pins in columns A, C and D are connected to ground.

NOTE: Connections in columns B and D are Rx input signals

Table 8 lists the pin-outs for the 96-pin P5 connector of the Exciter.

Table 9 Lists the pinouts, signals and power for the 96-PIN P6 connector of the Power Amplifier.

Generation 2/EBRC Single Channel Base Radio Backplane

Table 8 ***Gen 2 BR P5 Exciter Connector Pin-outs***

Pin	Row A	Row B	Row C
1	28.6 V	28.6 V	28.6 V
2	28.6 V	28.6 V	28.6 V
3	14.2V	14.2V	14.2V
4	14.2V	14.2V	14.2V
5	5.1 V	5.1 V	5.1 V
6	5.1 V	5.1 V	5.1 V
7	GND	GND	EXT_VFWD
8	GND	GND	EXT_VREF
9			
10	GND	GND	GND
11	GND	GND	VBLIN
12	GND	GND	RESET*
13	A6		
14	GND	GND	GND
15	GND	GND	SPI_MISO
16	A0	GND	GND
17	GND	GND	SPI_CLK
18	A1	GND	WP*
19	GND	GND	GND
20	A5	GND	SPI_MOSI
21	GND	GND	GND
22	A4	GND	GND
23	GND	GND	CLK*
24	A3	GND	GND
25	GND	GND	CLK
26	GND	GND	GND
27	GND	GND	SSI*
28	GND	GND	GND
29	GND	GND	SSI
30	GND	GND	GND
31	GND	GND	2.1MHz_TX
32	GND	GND	GND

NOTE: * = enabled low

NOTE: SPI address A6 was added to the EBRC to enable additional SPI addresses. Only change the EX if taking advantage of additional SPI addresses via A6. A6 pin A13 should be no connect to enable A6 functionality on other modules.

Table 9 **Gen 2 BR P6 PA Connector Pin-outs**

Pin	Row A	Row B	Row C
1	VBLIN	GND	28.6 VDC
2	GND	GND	28.6 VDC
3	A0	GND	28.6 VDC
4	GND	GND	28.6 VDC
5	A1	GND	28.6 VDC
6	GND	GND	28.6 VDC
7	A2	GND	28.6 VDC
8	GND	GND	28.6 VDC
9	A3	GND	28.6 VDC
10	GND	GND	28.6 VDC
11	SPI_MISO	GND	28.6 VDC
12	GND	GND	28.6 VDC
13	SPI_MOSI	GND	28.6 VDC
14	GND	GND	28.6 VDC
15	SPI_CLK	GND	28.6 VDC
16	GND	PA_ENABLE*	28.6 VDC
17	WP*	GND	28.6 VDC
18	GND	GND	28.6 VDC
19	A6	GND	28.6 VDC
20	GND	GND	28.6 VDC
21	GND	GND	28.6 VDC
22	GND	GND	28.6 VDC
23	GND	GND	28.6 VDC
24	GND	GND	28.6 VDC
25	GND	5.1 VDC	28.6 VDC
26	GND	5.1 VDC	28.6 VDC
27	GND	14.2 VDC	28.6 VDC
28	GND	14.2 VDC	28.6 VDC
29	GND	14.2 VDC	28.6 VDC
30	GND	14.2 VDC	28.6 VDC
31	GND	28.6 VDC	28.6 VDC
32	GND	28.6 VDC	28.6 VDC

NOTE: * Enabled low

NOTE: Pin B2 was re-defined for use with the EBRC- it went from GND for Legacy Controllers to PA_ENABLE with the EBRC.

NOTE: SPI address A6 was added to the EBRC to enable additional SPI addresses. If the PA does not use A6 pin A19, A6 Pin 19 should be no connect to enable A6 functionality on other modules.

Table 10 lists the pin-outs for the 25-pin P7 Alarm connector.

Table 10 ***Gen 2 BR P7 External Alarm Connector Pin-outs***

Pin	Signal
1	EXT_GPI_1*
2	EXT_GPO_1*
3	GND
4	EXT_GPI_2*
5	EXT_GPO_2*
6	
7	
8	
9	
10	GND
11	28.6 VDC
12	14.2 VDC
13	14.2 VDC
14	
15	5.1 VDC
16	GND
17	BAT_STAT*
18	MTR_STAT*
19	EXT_VFWD
20	EXT_VREF
21	GND
22	GND
23	BATT_TEMP
24	
25	GND
NOTE: * = enabled low	

Table 12 lists the pin-outs for the 9-pin P8 RS-232 connector.

Table 11 ***Gen 2 BR P8 External RS232 Connector Pin-outs***

Pin No.	Signal
1	CD
2	RxD
3	TxD
4	DTR (RCLK)
5	GND
6	DSR (TCLK)
7	RTS
8	CTS
9	BRG

Table 12 lists the pinouts for the 78-pin P9 Power Supply Connector

Table 12 ***Gen2 BR P9 Power Connector***

Pin No.	Signal
1	GND
2	GND
3	28.6 V
4	28.6 V
5	28.6 V
6	28.6 V
7	28.6 V
8	28.6 V
9	28.6 V
10	28.6 V
11	28.6 V
12	28.6 V
13	28.6 V
14	28.6 V
15	28.6 V
16	14.2 V
17	14.2 V
18	14.2 V
19	14.2 V

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Table 12 ***Gen2 BR P9 Power Connector***

Pin No.	Signal
20	14.2 V
21	14.2 V
22	14.2 V
23	14.2 V
24	5.1 V
25	5.1 V
26	5.1 V
27	5.1 V
28	5.1 V
29	5.1 V
30	5.1 V
31	5.1 V
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	GND
54	SCR_SHUT

Table 12 ***Gen2 BR P9 Power Connector***

Pin No.	Signal
55	SCR_THRESH
56	RELAY_ENABLE
57	SHUTDOWN
58	28V_AVG
59	BATT_TEMP
60	SPI_MISO
61	SPI_MOSI
62	SPI_CLK
63	A6
64	
65	
66	
67	A0(CS1)
68	A1(CS2)
69	A5
70	
71	A4
72	
73	A3
74	GND
75	A2
76	GND
77	GND
78	GND

Table 13 describes the coaxial P11 Ethernet connector on the Gen 2 BR.

Table 13 ***Gen 2 BR P11 Ethernet Connector Pinout***

Coaxial	Description
Center	Ethernet
Outer	GND
NOTE: Ethernet ground on the outer conductor of P11 is DC isolated from station ground.	

Table 14 **Gen 2 BR P12 DC In Connector**

Pin	Description
1	+ BATTERY
2	+ BATTERY
3	- BATTERY (RTN)
4	- BATTERY (RTN)
5	+ BATTERY
6	+ BATTERY
7	- BATTERY (RTN)
8	- BATTERY (RTN)

Table 15 lists the pin-outs for the 5 MHz/1PPS P13 connector.

Tables 16 through 19 list the pin-outs for the SMA and blindmate connectors for Receivers 1- 3, BRC, Exciter and PA.

Table 15 **Gen 2 BR P13 Connector Pin-outs**

Connector	Signal
1	ETHERNET - A (or 5MHZ IN*)
* May appear as indicated in parenthesis on some production units.	

Table 16 **Gen 2 BR SMA Connectors- Receivers**

Connector	Signal
P19	RCV ONE RF IN
P20	RCV TWO RF IN
P21	RCV THREE RF IN

Table 17 **Gen 2 BR Blind Mates - BRC**

Connector	Signal
P10	SPARE* (or 5MHZ/1 PPS - A)
P11	ETHERNET* (or ETHERNET - A)
*May appear as indicated in parenthesis on some production units.	

Table 18 ***Gen 2 BR Blind Mates - Exciter***

Connector	Signal
P14	EXCITER OUT
P15	EXCITER FEEDBACK

Table 19 ***Gen 2 BR Blind Mates - PA***

Connector	Signal
P16	PA FEEDBACK
P17	PA IN
P18	PA RF OUT

QUAD Channel Base Radio/Base Radio FRU Replacement Procedures

Replace suspected station modules with known non-defective modules to restore the station to proper operation. The following procedures provide FRU replacement instructions, post-replacement adjustments and verification instructions.

QUAD Base Radio Replacement Procedure

NOTE

Base Radio removal and installation procedures appear for reference or buildout purposes. Field maintenance of Base Radios typically consists of replacement of FRUs within the Base Radio. Perform Base Radio FRU replacement according to "Base Radio FRU Replacement Procedure" below.

Perform Base Radio (BR) replacement as described in the following paragraphs.

⚠ CAUTION

Improper lifting or dropping the BR could result in serious personal injury or equipment damage.

Base Radios are HEAVY!

Handle the BR with extreme caution, and according to local health and safety regulations.

Removal

Remove the BR from the Equipment Cabinet as follows:

⚠ CAUTION

A Single Carrier BR can weigh up to 76 LBS (34 KG). A Quad Carrier BR can weigh up to 91 LBS (41 KG). Handle the BR with extreme caution, and according to local health and safety regulations.

1. Remove power from the Base Radio by setting the Power Supply ON/OFF switch to the OFF position.
2. Tag and disconnect the cabling from the BR rear panel connectors.
3. Remove the Power Amplifier module to reduce the BR weight. Remove the two M10 Torx screws that secure the Power Amplifier module. Slide the module out of the chassis.
4. Remove the four M30 TORX screws which secure the BR front panel to the Equipment Cabinet mounting rails.
5. While supporting the BR, carefully remove the BR from the Equipment Cabinet by sliding the BR from the front of cabinet. When the BR becomes free from its mounting rails, be sure to fully support it.

Installation

Install BR in Equipment Cabinet as follows:

⚠ CAUTION

A Single Carrier BR can weigh up to 76 LBS (34 KG). A Quad Carrier BR can weigh up to 91 LBS (41 KG). Handle the BR with extreme caution, and according to local health and safety regulations.

1. If adding a BR, install side rails in the appropriate BR mounting position in the rack.
2. Remove the Power Amplifier module to reduce the BR weight. Remove the two M10 Torx screws that secure the Power Amplifier module. Slide the module out of the chassis.
3. While supporting the BR, carefully lift and slide the BR in the Equipment Cabinet mounting position.
4. Secure the BR to the Equipment Cabinet mounting rails using four M30 Torx screws. Tighten the screws to 40 in-lb (4.5 Nm).
5. Slide the Power Amplifier module back into the BR chassis. Replace two M10 Torx screws that secure the Power Amplifier module. Secure the module by tightening the screws to the specified torque of 5 in-lbs.
6. Connect the cabinet cabling to the BR. Refer to Backplane figure XX.
7. Perform BR activation as described below.

NOTE

Base Radio removal and installation procedures appear for reference or buildout purposes. Field maintenance of Base Radios typically consists of replacement of FRUs within the Base Radio. Perform Base Radio FRU replacement according to “Base Radio FRU Replacement Procedure” below.

Anti-Static Precautions

▲ CAUTION

The Base Radio contains static-sensitive devices. Prevent electrostatic discharge damage to Base Radio modules! When replacing Base Radio FRUs, wear a grounded wrist strap. Observe proper anti-static procedures.

Motorola publication 68P81106E84 provides complete static protection information. This publication is available through Motorola National Parts.

Observe the following additional precautions:

- ❒ Wear a wrist strap (Motorola Part No. 4280385A59 or equivalent) at all times when servicing the Base Radio to minimize static build-up.
- ❒ A grounding clip is provided with each EBTS cabinet. If not available, use another appropriate grounding point.
- ❒ DO NOT insert or remove modules with power applied to the Base Radio. ALWAYS turn the power OFF using the Power Supply rocker switch on the front of the Power Supply module.
- ❒ Keep spare modules in factory packaging for transporting. When shipping modules, always pack in original packaging.

QUAD BRs Radio FRU Replacement Procedure

Perform the following steps to replace any of the Base Radio FRUs:

NOTE

After a Control Board or BR replacement, the integrated Site Controller (iSC) reboots the BR. Whenever the BR goes off-line, the Replacement BRC Accept Timer begins counting down. A BR reboot occurs if the BR remains off-line as the timer times out. (The timer's default period is three minutes.) If someone turns on the BR before the timer times out, power down the BR. Then wait for the minimum timer period before turning on the BR.

1. Notice the Power Supply rocker switch, behind the front panel of the Power Supply. Set the Power Supply rocker switch to the OFF (0) position. Turning off this switch removes power from the Base Radio.
2. Loosen the front panel fasteners. These are located on each side of the module being replaced.
3. Pull out the module.
4. Insert the non-defective replacement module by aligning the module side rails with the appropriate rail guides inside the Base Radio chassis.
5. Gently push the replacement module completely into the Base Radio chassis assembly using the module handle(s).

▲ CAUTION

DO NOT slam or force the module into the chassis assembly. Rough handling can damage the connectors or backplane.

6. Secure the replacement module by tightening the front panel fasteners to the specified torque of 5 in-lbs.
7. Apply power to the Base Radio by setting the switch to the ON position.
8. Perform the Station Verification Procedure.

QUAD BR Power Amplifier (PA) Fan FRU Replacement

Perform the following steps to replace the Power Amplifier (PA) fans.

1. Remove the Power Amplifier from the Base Radio per FRU Replacement Procedure.
2. Disconnect fan power cable from PA housing.
3. Remove front panel from fan assembly.
4. Remove fan assembly from PA chassis.

NOTE

To install the new fan kit, reverse above procedure.

QUAD Base Radio Station Verification Procedures

Perform the Station Verification Procedures whenever you replace a FRU. The procedures verify transmit and receive operations. Each procedure also contains the equipment setup.

QUAD BR Replacement FRU Verification

Before shipment, the factory programs all module-specific information. Base Radio specific information (e.g., receive and transmit frequencies) involves a download to the Base Radio from the network/site controller.

The Base Radio does not require replacement FRU alignment.

QUAD BR Base Repeater FRU Hardware Revision Verification

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. Performing this procedure then minimizes or eliminates disruption of service to system users.

1. Connect one end of the RS-232 cable to the service computer.

2. Connect the other end of the RS-232 cable to the STATUS port, located on the front panel of the EX/CNTL module.

3. After the BR is powered up using the front switch on the Power Supply Module, press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the field password, log in to the BR.

   To enter field mode, at the > prompt type **login -ufield.**

   After entering the correct field password, the `field>` prompt is displayed on the service computer.

   The default factory set field password is **motorola**.

NOTE

The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

NOTE

Future versions of the QUAD BR will ship with software that recognizes the BR cabinet position. Default Motorola Manufacturing BR programmed cabinet position is (0,0), which automatically sends the radio to Test Application software mode upon power up. Upon setting a valid cabinet position, the radio will default to the Call Processing mode of operation.

4. Collect revision numbers from the station by typing the following command:

```
field> fv -oplatform
field>
```

5. If all modules return revision numbers of the format "Rxx.xx.xx", then all revision numbers are present. In that case, verification requires no further

action. If revision numbers return as blank, or not in the format “Rxx.xx.xx”, contact your local Motorola representative or Technical Support.

6. Set desired cabinet id, position, and of BR by typing the following commands, with the final number on each command being the desired cabinet id and position. The command example below sets cabinet id to 5, and cabinet position to 2.

```
field> ci -oplatform -c5
field> pi -oplatform -p2

field>
```

7. After checking all BRs, log out by keying the following command:

```
field> logout
```

NOTE

To start Call Processing mode of operation, reset the Base Radio using the front panel switch.

QUAD BR Transmitter Verification

The transmitter verification procedure verifies the transmitter operation and the integrity of the transmit path. This verification procedure is recommended after replacing an Exciter, Power Amplifier, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of service to system users.

Equipment Setup

To set up the equipment, use the following procedure:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.

2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.

⚠ CAUTION

Make sure power to BR is OFF before disconnecting transmitter RF connectors. Disconnecting transmitter RF connectors while the BR is keyed may result in RF burns from arcing.

4. Disconnect the existing cable from the connector labeled PA OUT. This connector is located on the backplane of the Base Radio.
5. Connect a test cable to the PA OUT connector.
6. Connect a 10 dB attenuator (100 W or more average power dissipation) on the other end of the test cable.
7. From the attenuator, connect a cable to the RF IN/OUT connector on the R2660 Communications Analyzer.
8. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.
9. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

10. Set the R2660 to the EXT REF mode.
11. Apply power to the R2660.
12. Set the R2660 to the SPECTRUM ANALYZER mode with the center frequency set to the transmit frequency of the Base Radio under test.
13. Perform the appropriate transmitter verification procedure below for the particular Power Amplifier used in the Base Radio.

Transmitter Verification Procedure (QUAD Carrier 800 MHz and 900 MHz Power Amplifiers)

This procedure provides commands and responses to verify proper operation of the transmit path for 800 MHz and 900 MHz QUAD Channel Base Radios.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the Control Module front panel. At the prompt, hit a Carriage Return on the service computer to enter the test application mode. Using the user_id -ufield and the field password**,** login to the BR.

To enter field mode, at the > prompt type **login -ufield.**

After entering the correct field password, the field> prompt is displayed on the service computer.

The default factory set field password is **motorola**.

> **NOTE**
>
> The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

> **NOTE**
>
> The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Dekey the BR to verify that no RF power is being transmitted. Set the transmit DSP test mode to "stop." At the field > prompt, type:

```
field> power -otxch1 -p0
field> ptm -otx_all -mstop
field> dpm -otxch1 -mnone
field> dpm -otxch2 -mnone
field> dpm -otxch3 -mnone
field> dpm -otxch4 -mnone
```

NOTE

The following command keys the transmitter. Make sure that transmission only occurs on licensed frequencies or into an RF load.

3. Key the BR to 40 watts, following the steps below from the field > prompt:

3.1 **800 MHz QUAD**: Set the frequency of transmit channel 1 through 4.

```
field> freq -otxch1 -f860
field> freq -otxch2 -f860.025
field> freq -otxch3 -f860.05
field> freq -otxch4 -f860.075
```

3.2 **900 MHz QUAD:** Set the frequency of transmit channel 1 through 4.

```
field> freq -otxch1 -f935
field> freq -otxch2 -f935.025
field> freq -otxch3 -f935.05
field> freq -otxch4 -f935.075
```

3.3 Enable the channels by setting a data pattern to “iden”

```
field> dpm -otxch1 -miden
field> dpm -otxch2 -miden
field> dpm -otxch3 -miden
field> dpm -otxch4 -miden
```

NOTE

After the following command is entered, power will be transmitted at the output of the Power Amplifier.

3.4 Set the transmit power to 40 watts and key the BR.

```
field> ptm -otx_all -mdnlk_framed
field> power -otxch1 -p40
```

4. After keying the Base Radio, verify the forward and reflected powers of the station along with the station VSWR with the parameters listed in Table 2.

Table 20 ***QUAD BR Transmitter Parameters***

Parameter	Value or Range
Forward Power	Greater than 36 Watts
Reflected Power	Less than 2.0 Watts
VSWR	Less than 1.6:1

NOTE

The reported value for forward power are not indicative of Base Radio performance. This value is reported from the internal wattmeter. These limits are only for verification of operation and are not representative of true operational power of the transmitter.

4.1 At the field > prompt, type:

```
field> power -otx_all
```

This command returns all active alarms of the Base Radio.

4.2 At the field > prompt, type:

```
field> alarms -ofault_hndlr
```

If the **alarms** command displays alarms, refer to the System Troubleshooting section of this manual for corrective actions.

5. View the spectrum of the transmitted signal on the R2660 Communications Analyzer in the Spectrum Analyzer mode. Figure 5 and Figure 6 shows a sample of the 800MHz and 900MHz spectrum, respectively.

6. Dekey the BR to verify no RF power is being transmitted. Set the transmit DSP test mode to "stop." At the field> prompt, type:

```
field> power -otxch1 -p0
field> ptm -otx_all -mstop
field> dpm -otxch1 -mnone
field> dpm -otxch2 -mnone
field> dpm -otxch3 -mnone
field> dpm -otxch4 -mnone
```

Equipment Disconnection

Use the following steps to disconnect equipment after verifying the transmitter.

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.

2. Disconnect the RS-232 cable from the connector on the service computer.

3. Disconnect the other end of the RS-232 cable from the RS-232 connector located on the front panel of the BRC.

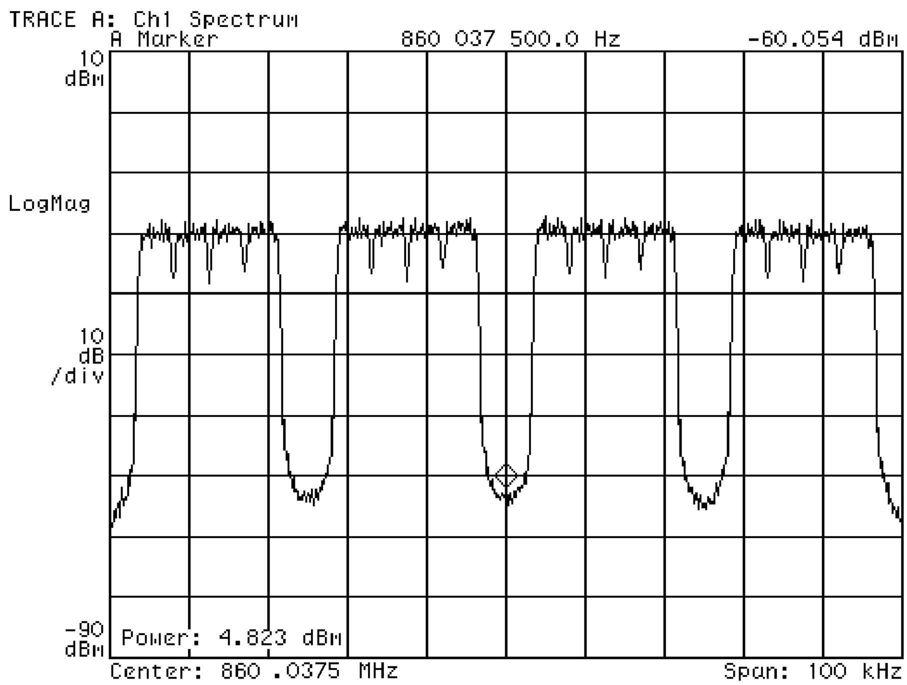

Figure 5 ***800 MHz Quad Carrier Spectrum***

⚠ CAUTION

Make sure power to BR is OFF before disconnecting transmitter RF connectors. Disconnecting transmitter RF connectors while the BR is keyed may result in RF burns from arcing.

4. Disconnect the test cable from the PA OUT connector located on the backplane of the Base Radio.
5. Connect the standard equipment cable to the PA OUT connector.
6. Disconnect the 10 dB attenuator from the other end of the test cable.
7. From the attenuator, disconnect the cable to the R2660 Communications Analyzer.
8. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.

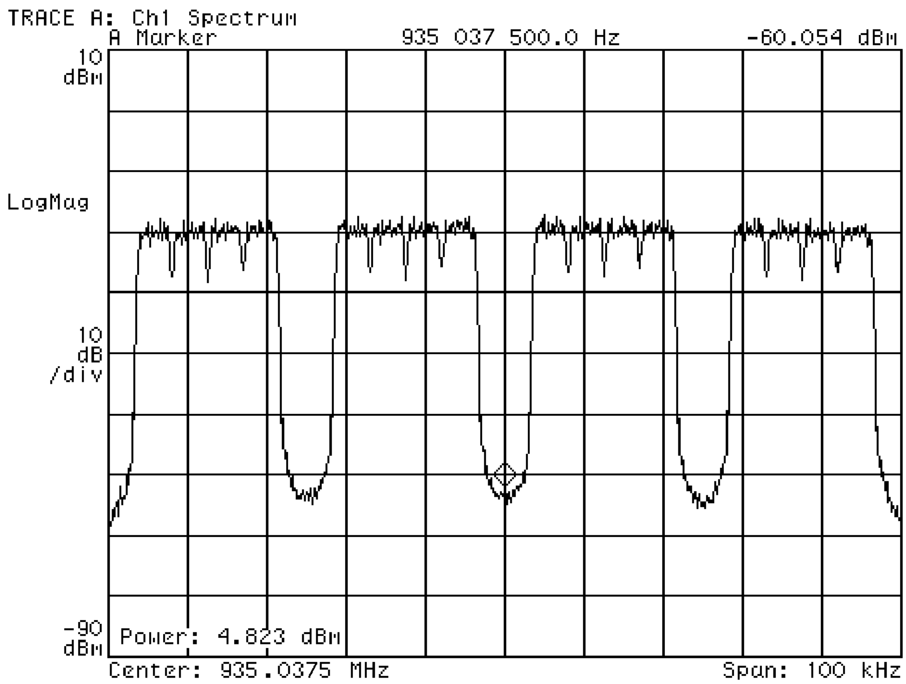

Figure 6 ***900 MHz Quad Carrier Spectrum***

9. If necessary, continue with the Receiver Verification Procedure.

QUAD BR Receiver Verification: Base Radio with RFDS (Measurement at the top of Rack)

The receiver verification procedure sends a known test signal into the Base Radio via the antenna ports at the top of the rack to verify the receive path. This verification procedure is recommended after replacing a Receiver, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the base radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of services to system users.

Equipment Setup

Set up equipment for the receiver verification as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.
4. Disconnect the existing cables from the connectors labeled RX1, RX2, and RX3 at the top of the EBTS rack. If the radio is configured for 2 Branch diversity, disconnect the RX1 and RX2 cables.

NOTE

Connecting the R2660 to the EBTS rack antenna ports will introduce extra system gain into the measurement, which must be accounted for. This must be accounted for in the calibration procedure. (See "Calibration of the R2660 output level" on page 69.).

5. Connect test cables from each of the RX1, RX2, and RX3 connectors (Cables A,B,C in Figure 7) to the input ports of the 3-way splitter. For 2 Branch diversity tests, load the RX3 cable with an appropriate 50ohm load or connect it to the RX3 antenna port on the radio.

6. Connect an additional test cable (Cable D in Figure 7) from the summed port of the 3-way splitter to the RF IN/OUT connector on the R2660 Communications Analyzer.

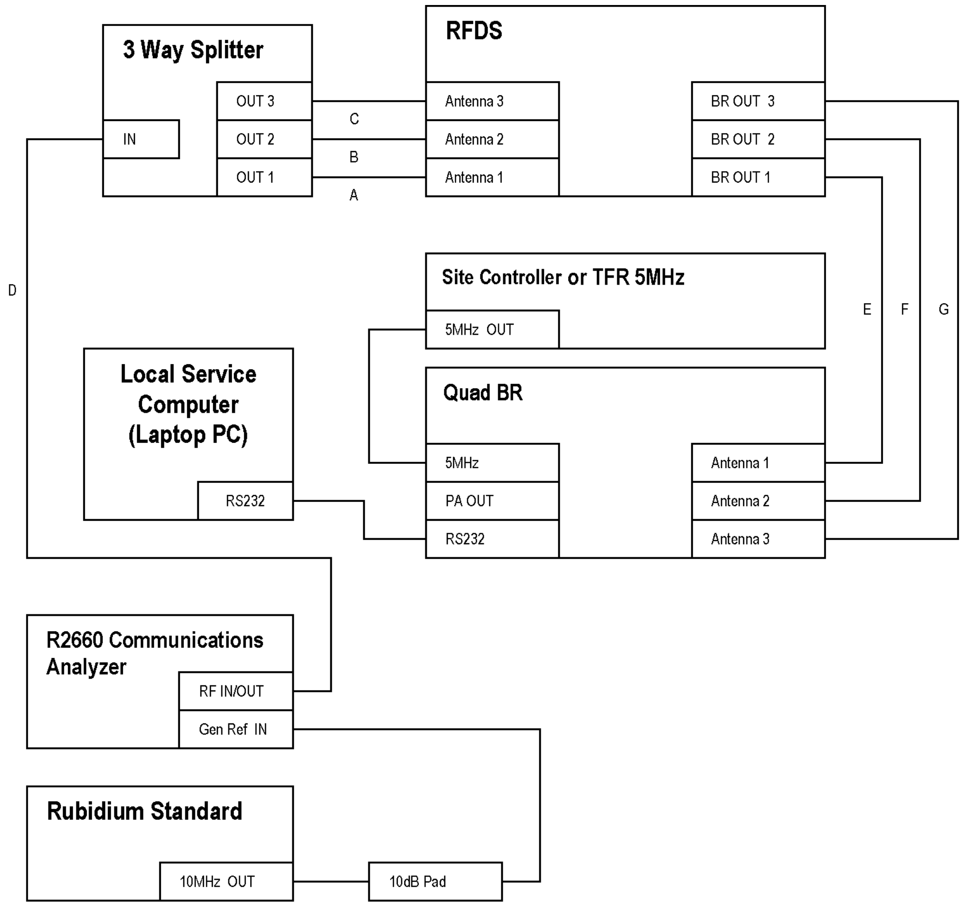

Figure 7 ***QUAD BR w/ RFDS Verification Test Setup***

7. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.

8. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

9. Set the R2660 to the EXT REF mode.

10. Apply power to the R2660.

NOTE

Due to the nature of the Quad BR configuration, Antenna 2 MUST be connected to the R2660 for synchronization (This is not required for SR9.6 and above). All three RX inputs on the back of the EBTS must be connected to the R2660 and calibrated such that EACH input receives the calibrated RF signal. (See “Calibration of the R2660 output level” on page 69.) If all RX inputs are not connected, some receive paths will not receive properly.

Receiver Verification Procedure: QUAD Base Radio with RFDS

This procedure provides commands and responses to verify proper operation of the Base Radio receiver paths. Perform the procedure on all four channels in each Base Radio in the EBTS.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the front of the EX/BRC module. Using the terminal program on the service computer, log onto the BR. Bold type indicates user input commands.

   To enter field mode, at the > prompt type **login -ufield.**

   After entering the correct field password, the `field>` prompt is displayed on the service computer.

   The default factory set field password is **motorola**.

NOTE

The ‘Out of Box’ default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Set the Frequency of the R2660 to 810MHz for 800 MHz QUAD Channel or 896 MHz for 900 MHz QUAD Channel. Power out should be set to –80 dBm.

3. **800 MHz QUAD**: Set all channel frequencies:

```
field> freq -orxch1 -f810
field> freq -orxch2 -f810
field> freq -orxch3 -f810
field> freq -orxch4 -f810
```

3.1 **900 MHz QUAD:** Set all channel frequencies:

```
field> freq -orxch1 -f896
field> freq -orxch2 -f896
field> freq -orxch3 -f896
field> freq -orxch4 -f896
```

4. Verify the R2660 signal level:

```
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -r1 -a100
```

5. The resulting output will look similar to this:

```
field> ppr -orxch1 -r1 -a100

SGC Atten.(dBm)=12.000000
Freq. Offset=-2.197266
Sync. Attempts= 1.000000
Sync. Successes=1.000000
BER%=0.000000
RX Path1 RSSI=-80.557007
RX Path2 RSSI=-127.012520
RX Path3 RSSI=-127.012520
Chn sig. strength=-78.163368
Chn intf. strength=-180.57670

field>
```

NOTE

RX Path1 RSSI must read -80dBm ±1dBm for the BER Floor verification to be accurate. Adjust the output level of the R2660 to compensate for loss in the test cables and three-way splitter.

BER Floor Measurement: QUAD Base Radio with RFDS

1. Verify that the R2660 is set to 810MHz (896 MHz for 900 MHZ QUAD Channel BR) and is producing a power level of -80dBm. (See "Receiver Verification Procedure: QUAD Base Radio with RFDS" on page 63.)

2. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 0.01%, the receiver has passed the test.

3. Check Receiver 1. At the prompt, type (inputs are in bold, comments are in italics).

NOTE

Use -**f896** for 900 MHz QUAD Channel BR in the following steps instead of **-f810.**

```
field> freq -orxch1 -f810
field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a1000 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -dbr3 -son
field> ppr -orxch1 -a1000 -r1
```

Check Receiver 2. At the prompt, type:

```
field> freq -orxch2 -f810
field> enable -orxch2 -soff
field> enable -orxch2 -dbr1 -son
field> ppr -orxch2 -a1000 -r1

field> enable -orxch2 -soff
field> enable -orxch2 -dbr2 -son
field> ppr -orxch2 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch2 -soff
field> enable -orxch2 -dbr3 -son
field> ppr -orxch2 -a1000 -r1
```

Check Receiver 3. At the prompt, type:

```
field> freq -orxch3 -f810
field> enable -orxch3 -soff
field> enable -orxch3 -dbr1 -son
field> ppr -orxch3 -a1000 -r1

field> enable -orxch3 -soff
field> enable -orxch3 -dbr2 -son
field> ppr -orxch3 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch3 -soff
field> enable -orxch3 -dbr3 -son
field> ppr -orxch3 -a1000 -r1
```

Check Receiver 4. At the prompt, type:

```
field> freq -orxch4 -f810
field> enable -orxch4 -soff
field> enable -orxch4 -dbr1 -son
field> ppr -orxch4 -a1000 -r1

field> enable -orxch4 -soff
field> enable -orxch4 -dbr2 -son
field> ppr -orxch4 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch4 -soff
field> enable -orxch4 -dbr3 -son
field> ppr -orxch4 -a1000 -r1
```

4. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

5. As shown below respectively for 800/900 MHz Quad Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Receiver Sensitivity Measurement: QUAD Base Radio with RFDS

The receiver sensitivity measurement consists of sending a calibrated RF level of -113.5dBm to the antenna ports at the top of the rack. This includes the RFDS in the receive channel and measures the combined performance of the Base Radio and the RFDS. The R2660 output must be calibrated prior to the taking of this measurement.

Calibration of the R2660 output level

1. Verify that the R2660 is set to 810 MHz for the 800 MHz QUAD Channel or 896 MHz for the 900 MHz QUAD, then adjust the output power to a level of -50dBm

2. Calibrate HP438A Power Meter. Refer to the HP users guide that came with the Meter. Below is a general procedure that can be followed.

   2.1 Attach 8481D Power Sensor to the Sensor input on the front of the 438A.

   2.2 Attach the included HP 11708A 30dB pad to the Power REF output on the front on the 438A.

2.3 Power on the 438A.

2.4 Connect the Power Sensor to the female end of the 30dB pad extruding from the Power Reference output.

2.5 Press the “Zero” button on the 438A.

2.6 Wait for Zeroing operation to complete.

2.7 Press “Shift-Zero” to enter the Cal value. This is listed as CF on the Power Sensor.

2.8 Wait for Cal operation to complete.

2.9 Press “Shift-Freq” to enter the Cal Factor. This is listed as Cf in a chart vs. freq on the Power Sensor. Choose the closest frequency range for the application. For 800/900 MHz measurements, interpolate between 1.0GHz and 0.5GHz.

2.10 For measurement of iDEN or 6:1 waveforms, press “Offset” and enter 7.78dB.

3. Disconnect Cable A (see Figure 7) from the Base Radio or Antenna Port and connect it to the Power Sensor Head.

4. Increase the power level on the R2660 until the HP 438A Power Meter reads -50dB.

5. Record the DISPLAYED power level of the R2660 as Calfactor A.

6. The path loss through the cable and splitter system is Calfactor A + 50.

   Example: R2660 reads -44dBm

   HP 438A reads -50dBm

   Calfactor A = -44, path loss = 6dB

7. Path loss must be determined for each Antenna cable A,B,C (see Figure 7). If comparable cables are used for all three paths, losses of all three should be approximately the same.

8. Additional power will be added to the R2660 in the sensitivity measurement to balance out the additional path loss value.

9. Reconnect cables A,B,C (see Figure 7) to Antenna Ports 1,2,3.

10. Set the R2660 to Frequency 810 MHz for the 800 MHz QUAD Channel or 896 MHz for the 900 MHz Quad and a Power level of -113.5dBm + path loss.

    Example: If your path loss was 6dB, set the R2660 to-107.5dBm.

11. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 8.00%, the receivers passed the test.

NOTE

Substitute **-f896** for a 900 MHz QUAD BR for **-f810** **(**which is the for the 800 MHz BR) in the steps below.

```
field> freq -orxch1 -f810
field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a100 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -dbr3 -son
field> ppr -orxch1 -a100 -r1
```

Check Receiver 2. At the prompt, type:

```
field> freq -orxch2 -f810
field> enable -orxch2 -soff
field> enable -orxch2 -dbr1 -son
field> ppr -orxch2 -a100 -r1

field> enable -orxch2 -soff
field> enable -orxch2 -dbr2 -son
field> ppr -orxch2 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch2 -soff
field> enable -orxch2 -dbr3 -son
field> ppr -orxch2 -a100 -r1
```

Check Receiver 3. At the prompt, type:

```
field> freq -orxch3 -f810
field> enable -orxch3 -soff
field> enable -orxch3 -dbr1 -son
field> ppr -orxch3 -a100 -r1

field> enable -orxch3 -soff
field> enable -orxch3 -dbr2 -son
field> ppr -orxch3 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch3 -soff
field> enable -orxch3 -dbr3 -son
field> ppr -orxch3 -a100 -r1
```

Check Receiver 4. At the prompt, type:

```
field> freq -orxch4 -f810
field> enable -orxch4 -soff
field> enable -orxch4 -dbr1 -son
field> ppr -orxch4 -a100 -r1

field> enable -orxch4 -soff
field> enable -orxch4 -dbr2 -son
field> ppr -orxch4 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch4 -soff
field> enable -orxch4 -dbr3 -son
field> ppr -orxch4 -a100 -r1
```

12. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

13. As shown below respectively for 800/900 MHz Quad Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Receiver Verification: Measurement of the QUAD Base Radio (No RFDS)

The receiver verification procedure sends a known test signal into the Base Radio to verify the receive path. The signal is fed DIRECTLY into the ANTENNA PORTS in the back of the Base Radio. This excludes the RFDS and antenna cabling from the measurement. This verification procedure is recommended after replacing a Receiver, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the base radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of services to system users.

Equipment Setup

Set up the equipment for the receiver verification as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.
4. Disconnect the existing cables from the connectors labeled RX1, RX2, and RX3 on the back of the Base Radio. If the radio is configured for 2 Branch diversity, disconnect the RX1 and RX2 cables.
5. Connect test cables from each of the RX1, RX2, and RX3 connectors (Cables A,B,C in Figure 8) to the input ports of the 3-way splitter. For 2 Branch diversity tests, load the RX3 cable with an appropriate 50ohm load or connect it to the RX3 antenna port on the radio.
6. Connect an additional test cable (Cable D in Figure 7) from the summed port of the 3-way splitter to the RF IN/OUT connector on the R2660 Communications Analyzer.
7. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.
8. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

9. Set the R2660 to the EXT REF mode

.

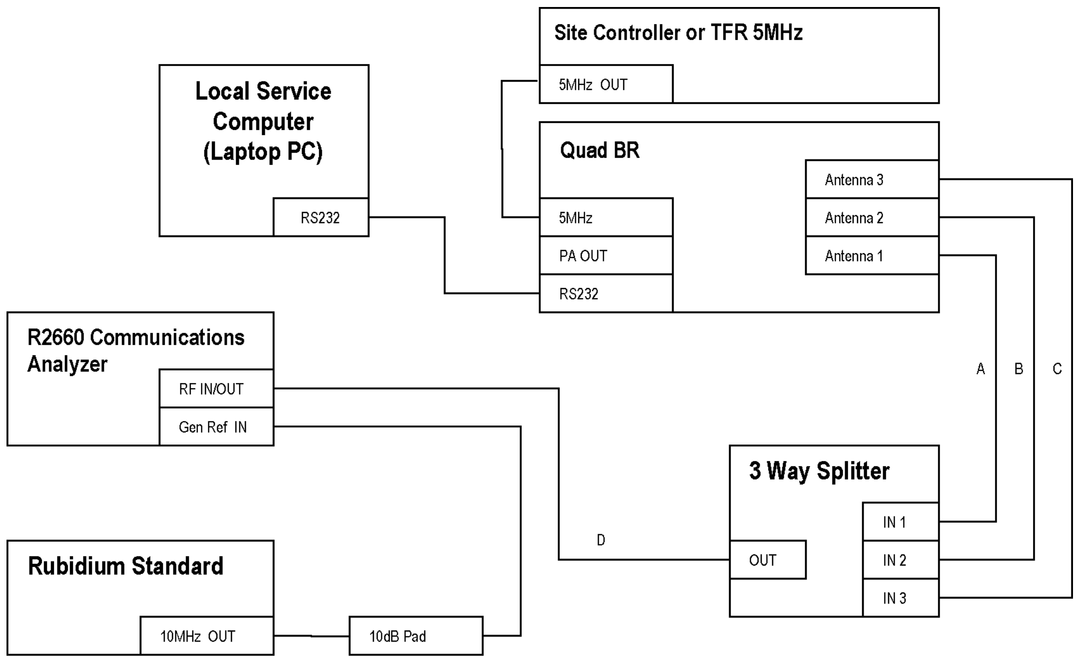

Figure 8 ***QUAD BR Rx Verification Test Setup***

10. Apply power to the R2660.

NOTE
Due to the nature of the Quad BR configuration, Antenna 2 MUST be connected to the R2660 for synchronization (This is not required for SR9.6 and above) . All three RX inputs on the back of the EBTS must be connected to the R2660 and calibrated such that EACH input receives the calibrated RF signal. (See "Calibration of the R2660 output level" on page 69.) If all RX inputs are not connected, some receive paths will not receive properly.

QUAD BR Distributed Multicoupler

The Quad BR uses an internal distributed multicoupler to distribute the RF signals from the 3 Antenna ports to the 4 Channels of the BR. Each Channel has 3 receivers.

Receiver Verification Procedure: QUAD Base Radio

This procedure provides commands and responses to verify proper operation of the Base Radio receiver paths. Perform the procedure on all four channels in each Base Radio in the EBTS.

1. Power on the BR using the front switch on the Power Supply Module. Press the reset button on the front of the EX/BRC module. Using the terminal program on the service computer, log onto the BR. Bold type indicates user input commands.

   To enter field mode, at the > prompt type **login -ufield.**

   After entering the correct field password, the `field>` prompt is displayed on the service computer.

   The default factory set field password is **motorola**.

   NOTE

   The 'Out of Box' default factory set field password is deleted and is replaced by the customer defined field password contained within the OMC. This occurs as soon as the controller module receives its initial OMC download.

   The default OMC set field password is **Motorola**.

NOTE

The OMC field password is customer configurable. Please contact the Operations and Maintenance Center (OMC) operator on duty to obtain your customer unique field password.

```
>login -ufield
password:<login password>

field>
```

2. Set the Frequency to of the R2660 to 810MHz. for 800 MHZ QUAD Channel BR, 896 MHZ for 900 MHz QUAD BR. Power out should be set to –80 dBm.

NOTE

Substitute **-f896** for a 900 MHz QUAD BR, for **-f810** **(**which is the for the 800 MHz BR) in the step below

3. Disable System Gain.

```
field> sge -orx_all -soff
```

NOTE

This step should only be performed if the R2660, 3 way splitter and cables connected directly to the Base Radio Antenna ports. If verification is being performed at the top of the rack (adding an RFDS), disregard the above command.

4. Verify the R2660 signal level.

```
field> freq -orxch1 -f810
field> freq -orxch2 -f810
field> freq -orxch3 -f810
field> freq -orxch4 -f810
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -r1 -a100
```

5. The resulting output will look similar to this:

```
field> ppr -orxch1 -r1 -a100

SGC Atten.(dBm)=0.000000
Freq. Offset=-15.059323
Sync. Attempts=1.000000
Sync. Successes=1.000000
BER%=0.000000
RX Path1 RSSI=-80.934021
RX Path2 RSSI=-127.012520
RX Path3 RSSI=-127.012520
Chn sig. strength=-57.098698
Chn intf. strength=-91.696739
field>
```

NOTE

RX Path1 RSSI must read -80dBm ± 1dBm for the BER Floor verification to be accurate. Adjust the output level of the R2660 to compensate for loss in the test cables and three-way splitter.

BER Floor Measurement: QUAD Base Radio

1. Verify that the R2660 is set to 810MHz for the 800 MHz QUAD or 896 MHz for the 900 MHz QUAD and is producing a power level of -80dBm. (See “Receiver Verification Procedure: QUAD Base Radio with RFDS” on page 63.)

2. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 0.01%, the receiver has passed the test.

NOTE
Substitute **-f896** for a 900 MHz QUAD BR, for **-f810** **(**which is the for the 800 MHz BR) in the steps below

3. Check Receiver 1. At the prompt, type (inputs are in bold, comments are in italics):

```
field> ppc -orxch1 -mchn -s1
field> freq -orxch1 -f810

field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a1000 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -dbr3 -son
field> ppr -orxch1 -a1000 -r1
```

Check Receiver 2. At the prompt, type:

```
field> ppc -orxch2 -mchn -s1
field> freq -orxch2 -f810

field> enable -orxch2 -soff
field> enable -orxch2 -dbr1 -son
field> ppr -orxch2 -a1000 -r1

field> enable -orxch2 -soff
field> enable -orxch2 -dbr2 -son
field> ppr -orxch2 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch2 -soff
field> enable -orxch2 -dbr3 -son
field> ppr -orxch2 -a1000 -r1
```

Check Receiver 3. At the prompt, type:

```
field> ppc -orxch3 -mchn -s1
field> freq -orxch3 -f810

field> enable -orxch3 -soff
field> enable -orxch3 -dbr1 -son
field> ppr -orxch3 -a1000 -r1

field> enable -orxch3 -soff
field> enable -orxch3 -dbr2 -son
field> ppr -orxch3 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch3 -soff
field> enable -orxch3 -dbr3 -son
field> ppr -orxch3 -a1000 -r1
```

Check Receiver 4. At the prompt, type:

```
field> ppc -orxch4 -mchn -s1
field> freq -orxch4 -f810

field> enable -orxch4 -soff
field> enable -orxch4 -dbr1 -son
field> ppr -orxch4 -a1000 -r1

field> enable -orxch4 -soff
field> enable -orxch4 -dbr2 -son
field> ppr -orxch4 -a1000 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch4 -soff
field> enable -orxch4 -dbr3 -son
field> ppr -orxch4 -a1000 -r1
```

4. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

5. As shown below respectively for 800 MHz Quad Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the field > prompt, type:

```
field> fc –oplatform
```

Receiver Sensitivity Measurement: QUAD Base Radio

1. Verify that the R2660 is set to 810MHz (800 MHz QUAD BR) or 896 MHz (900 MHz BR) and adjust the output power to a level of -50dBm.

2. Calibrate HP438A Power Meter. Refer to the HP users guide that came with the Meter. Below is a general procedure that can be followed.

   2.1 Attach 8481D Power Sensor to the Sensor input on the front of the 438A.

   2.2 Attach the included HP 11708A 30dB pad to the Power REF output on the front on the 438A.

   2.3 Power on the 438A.

   2.4 Connect the Power Sensor to the female end of the 30dB pad extruding from the Power Reference output.

   2.5 Press the "Zero" button on the 438A.

   2.6 Wait for Zeroing operation to complete.

   2.7 Press "Shift-Zero" to enter the Cal value. This is listed as CF on the Power Sensor.

   2.8 Wait for Cal operation to complete.

2.9 Press "Shift-Freq" to enter the Cal Factor. This is listed as Cf in a chart vs. freq on the Power Sensor. Choose the closest frequency range for the application. For 800/900 MHz measurements, interpolate between 1.0GHz and 0.5GHz.

2.10 For measurement of iDEN or Tornado 6:1 waveforms, press "Offset" and enter 7.78dB.

3. Disconnect Cable A (see Figure 7) from the Base Radio and connect it to the Power Sensor Head.

4. Increase the power level on the R2660 until the HP 438A Power Meter reads -50dB.

5. Record the DISPLAYED power level of the R2660 as Calfactor A.

6. The path loss through the cable and splitter system is Calfactor A + 50.

Example: R2660 reads -44dBm

HP 438A reads -50dBm

Calfactor A = -44, path loss = 6dB

7. Path loss must be determined for each Antenna cable A,B,C (see Figure 8). If comparable cables are used for all three, the path losses of all three should be the same.

8. Additional power will be added to the R2660 in the sensitivity measurement to balance out the additional path loss value.

9. Reconnect cables A,B,C (see Figure 8) to Antenna Ports 1,2,3 on the Base Radio.

10. Set the R2660 to Frequency 810 MHz (896 MHz for 900 MHz QUAD) and a Power level of -108dBm + path loss.

Example: If your path loss was 6dB, set the R2660 to -102dBm.

NOTE

Substitute **-f896** for a 900 MHz QUAD BR for **-f810** **(**which is the for the 800 MHz BR) in the steps below

11. Using the MMI commands below, issue the command to put the BR into single branch mode. If the resulting bit error rate for receiver branches 1, 2, and 3 is less than 8.00%, the receiver has passed the test.

```
field> ppc -orxch1 -mchn -s1
field> freq -orxch1 -f810

field> enable -orxch1 -soff
field> enable -orxch1 -dbr1 -son
field> ppr -orxch1 -a100 -r1

field> enable -orxch1 -soff
field> enable -orxch1 -dbr2 -son
field> ppr -orxch1 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch1 -soff
field> enable -orxch1 -dbr3 -son
field> ppr -orxch1 -a100 -r1
```

Check Receiver 2. At the prompt, type:

```
field> ppc -orxch2 -mchn -s1
field> freq -orxch2 -f810

field> enable -orxch2 -soff
field> enable -orxch2 -dbr1 -son
field> ppr -orxch2 -a100 -r1

field> enable -orxch2 -soff
field> enable -orxch2 -dbr2 -son
field> ppr -orxch2 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch2 -soff
field> enable -orxch2 -dbr3 -son
field> ppr -orxch2 -a100
```

Check Receiver 3. At the prompt, type:

```
field> ppc -orxch3 -mchn -s1
field> freq -orxch3 -f810

field> enable -orxch3 -soff
field> enable -orxch3 -dbr1 -son
field> ppr -orxch3 -a100 -r1

field> enable -orxch3 -soff
field> enable -orxch3 -dbr2 -son
field> ppr -orxch3 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch3 -soff
field> enable -orxch3 -dbr3 -son
field> ppr -orxch3 -a100
```

Check Receiver 4. At the prompt, type:

```
field> ppc -orxch4 -mchn -s1
field> freq -orxch4 -f810

field> enable -orxch4 -soff
field> enable -orxch4 -dbr1 -son
field> ppr -orxch4 -a100 -r1

field> enable -orxch4 -soff
field> enable -orxch4 -dbr2 -son
field> ppr -orxch4 -a100 -r1

(skip this step if the system is configured for 2 Branch Diversity)

field> enable -orxch4 -soff
field> enable -orxch4 -dbr3 -son
field> ppr -orxch4 -a100
```

12. Enter the command to return all active alarms of the Base Radio. At the prompt, type:

```
field> alarms -ofault_hndlr
```

NOTE

If the command displays alarms, refer to the System Troubleshooting section for corrective actions.

13. As shown below for 800/900 MHz QUAD Base Radios, the following command returns the kit numbers of the receiver and all other modules. At the prompt, type:

```
field> fc –oplatform
```

Equipment Disconnection

Disconnect equipment after verifying the receiver as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Disconnect the RS-232 cable from the connector on the service computer.
3. Disconnect the other end of the RS-232 cable from the RS-232 connector on the front panel of the BRC.
4. Disconnect the test cable from the RX 1, RX2, and RX3 connectors located on the backplane of the Base Radio.
5. Connect the standard equipment cable to the RX 1, RX2, and RX3 connectors.
6. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.

   This completes the Receiver Verification Procedure.
7. Repeat the Receiver Verification Procedure for each Quad receiver in every Base Radio in the EBTS.

QUAD Channel BR Backplane

Backplane Connectors

The Base Radio backplane includes all external equipment connections. Table 21 lists and describes the backplane connectors.

Table 21 ***QUAD BR Backplane Connectors***

Connector	Module	Description	Connector Type
P1	EXBRC	Signal	168 Pin AMP Z-Pack Futurebus
P2	RX1	Signal	72 Pin AMP Z-Pack Futurebus
P3	RX1	RF	6 coax Harting Harpak
P4	RX2	Signal	72 Pin AMP Z-Pack Futurebus
P5	RX2	RF	6 coax Harting Harpak
P6	RX3	Signal	72 Pin AMP Z-Pack Futurebus
P7	RX3	RF	6 coax Harting Harpak
P8	RX4	Signal	72 Pin AMP Z-Pack Futurebus
P9	RX4	RF	6 coax Harting Harpak
P10	PA	Signal	96 Pin EURO
P11	PS	Signal & Power	78 Pin AMP Teledensity
P12[a]	PS	-48 Vdc Power In	8 Pin AMP 530521-3
P13	EX	RF(EX from PA)	SMA blindmate
P14	EX	RF(EX to PA)	SMA blindmate
P15	External / EXBRC	Ethernet	BNC blindmate
P16	External / PA	RF (PA from EX)	SMA blindmate
P17	External / PA	RF (PA to EX)	SMA Blindmate
P18	External / PA	TX Output	SMA blindmate
P19	RX Branch 1	RF	SMA
P20	RX Branch 2	RF	SMA
P21	RX Branch 3	RF	SMA
P22[b]	External	RS232	Dsub-9
P23	External	Alarm	Dsub-25
P24	External	5MHz/1PPS	BNC

a. P12 is a cutout in the backplane with threaded inserts for securing the connector which mates directly to the power supply.

b. P22 will not be placed on the backplane. However, the backplane shall be designed with P22 to allow for reuse on future products.

Figure 9 shows the locations of the QUAD Base Radio external connections.

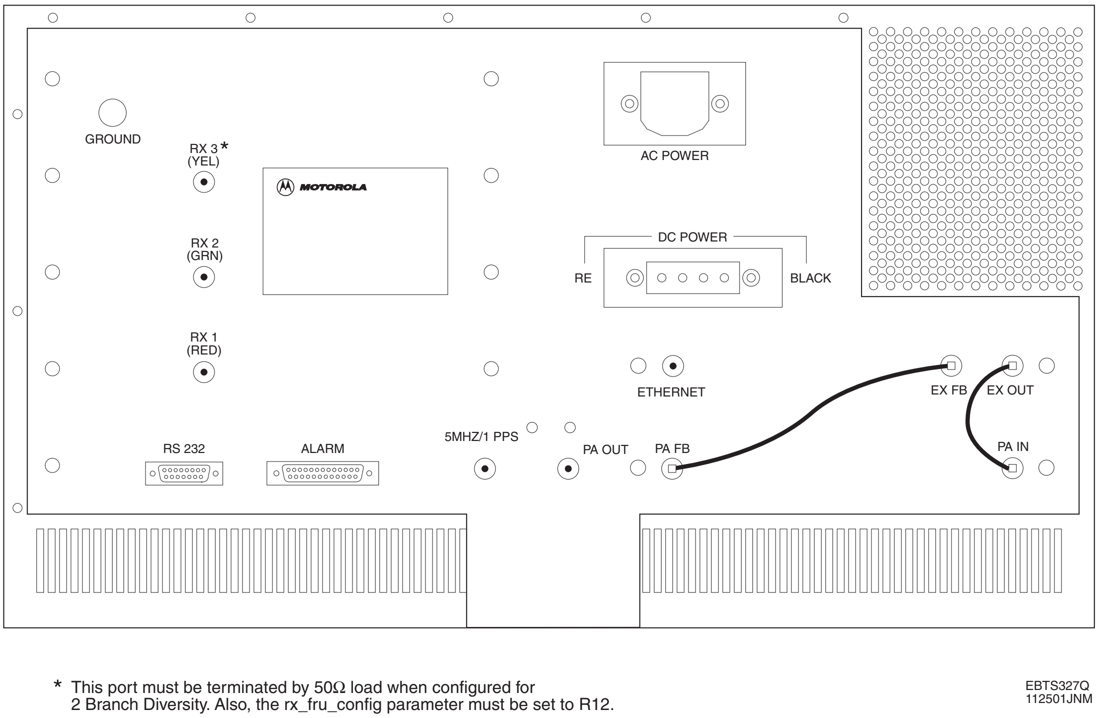

Figure 9 ***QUAD Base Radio Backplane Connectors***

QUAD BR Backplane Connector Pinouts

Table 22 lists the pin-outs for the Base Radio Controller board's 168-pin P1 connector.

Table 22 ***EXBRC P1 Pinout, Signal and Power***

Row	A	B	C	D
1	GND	3.3 Vdc	3.3 Vdc	NC
2	GND	3.3 Vdc	14.2 Vdc	14.2 Vdc
3	GND	3.3 Vdc	14.2 Vdc	14.2 Vdc
4	GND	GND	GND	GND
5	NC	NC	NC	NC

Table 22 ***EXBRC P1 Pinout, Signal and Power***

Row	A	B	C	D
6	GND	GND	GND	GND
7	GND	16.8MHz_RX	16.8MHz_RX_RTN	GND
8	GND	GND	GND	GND
9	GND	5 MHz/1 PPS	3.3 Vdc	3.3 Vdc
10	NC	NC	NC	3.3 Vdc
11	TxD	CTS	DTR	BRG
12	RTS	RxD	DSR	CD
13	NC	NC	NC	3.3 Vdc
14	NC	NC	SHUTDOWN_	SLEEP_
15	PA_ENABLE	NC	28.6 Vdc	14.2 Vdc
16	NC	NC	NC	3.3 Vdc
17	EXT_GPI_1_	EXT_GPI_2_	EXT_GPO_1_	EXT_GPO_2_
18	BAT_STAT_	MTR_STAT_	EXT_VFWD	EXT_VREV
19	SPI_M3	SPI_M2	SPI_M1	SPI_M0
20	SPI_ENABLE	SPI_MOSI	SPI_MISO	SPI_CLK
21	SPI_A2	SPI_A1	SPI_A0	WP_
22	NC	RxRESET_	NC	NC
23	NC	Clock_SyncB_	NC	NC
24	GND	GND	3.3 Vdc	3.3 Vdc
25	SSI_Data_D	SSI_CLK_D	SSI_FS_D	3.3 Vdc
26	SSI_Data_D_RTN	SSI_CLK_D_RTN	NC	3.3 Vdc
27	GND	GND	3.3 Vdc	3.3 Vdc
28	DSPIb_MOSI	DSPIb_CLK	DSPIb_EN_1	DSPIb_EN_2
29	DSPIb_MOSI_RTN	DSPIb_CLK_RTN	DSPIb_EN_3	NC
30	GND	GND	3.3 Vdc	3.3 Vdc
31	GND	SSI_Data_C	SSI_CLK_C	SSI_FS_C
32	GND	SSI_Data_C_RTN	SSI_CLK_C_RTN	NC
33	NC	Clock_SyncA_	NC	NC
34	GND	GND	3.3 Vdc	3.3 Vdc
35	SSI_Data_B	SSI_CLK_B	SSI_FS_B	3.3 Vdc
36	SSI_Data_B_RTN	SSI_CLK_B_RTN	NC	3.3 Vdc
37	GND	GND	3.3 Vdc	3.3 Vdc
38	DSPIa_MOSI	DSPIa_CLK	DSPIa_EN_1	DSPIa_EN_2
39	DSPIa_MOSI_RTN	DSPIa_CLK_RTN	DSPIa_EN_3	NC
40	GND	GND	3.3 Vdc	3.3 Vdc
41	GND	SSI_Data_A	SSI_CLK_A	SSI_FS_A
42	GND	SSI_Data_A_RTN	SSI_CLK_A_RTN	NC

Table 23 **EXBRC P13 Pinout, Exciter from PA**

Coaxial	Description
Center	PA IN
Outer	GND

Table 24 **EXBRC P14 Pinout, Exciter to PA**

Coaxial	Description
Center	PA Feedback
Outer	GND

Table 25 **EXBRC P15 Pinout, Ethernet**

Coaxial	Description
Center	Ethernet
Outer	GND

RX1 Connections

Table 26 ***RX1 P2 Pinout, Signal and Power***

Row	A	B	C	D
1	NC	GND	GND	Clock_SyncA_
2	GND	DSPIa_MOSI_RTN	DSPIa_CLK_RTN	DSPIa_EN_1
3	GND	DSPIa_MOSI	DSPIa_CLK	DSPIa_EN_2
4	GND	GND	GND	GND
5	14.2	SSI_CLK_A_RTN	SSI_FS_B	SSI_CLK_B_RTN
6	14.2	SSI_CLK_A	SSI_FS_A	SSI_CLK_B
7	14.2	GND	GND	GND
8	14.2	SSI_Data_A_RTN	GND	SSI_Data_B
9	GND	SSI_Data_A	GND	SSI_Data_B_RTN
10	GND	NC	NC	NC
11	3.3	RxRESET_	GND (ID0)	GND (ID1)
12	3.3	WP_	SPI_A0	SPI_A1
13	3.3	SPI_MISO	SPI_CLK	SPI_A2
14	GND	SPI_M0	SPI_ENABLE	SPI_MOSI
15	GND	SPI_M1	SPI_M2	SPI_M3
16	GND	GND	GND	NC
17	GND	16.8MHz_RX	GND	NC (WB switch)
18	GND	16.8MHz_RX_RTN	GND	NC (MC switch)

Table 27 ***RX1 P3 Pinout, RF Input and Output Connection***

Row	A	B	C	D	E
1	GND	-	GND	-	GND
2	-	RX3_EXP3	-	RX1_EXP3	-
3	GND	-	GND	-	GND
4	GND	-	GND	-	GND
5	-	RX2_EXP2	-	RX1_EXP2	-
6	GND	-	GND	-	GND
7	GND	-	GND	-	GND
8	-	RX Branch 1	-	RX1_EXP1	-
9	GND	-	GND	-	GND

RX2 Connections

Table 28 ***RX2 P4 Pinout, Signal and Power***

Row	A	B	C	D
1	NC	GND	GND	Clock_SyncA_
2	GND	DSPIa_MOSI_RTN	DSPIa_CLK_RTN	DSPIa_EN_3
3	GND	DSPIa_MOSI	DSPIa_CLK	DSPIa_EN_2
4	GND	GND	GND	GND
5	14.2	SSI_CLK_B_RTN	NC	NC
6	14.2	SSI_CLK_B	SSI_FS_B	NC
7	14.2	GND	GND	GND
8	14.2	SSI_Data_B_RTN	GND	NC
9	GND	SSI_Data_B	GND	NC
10	GND	NC	NC	NC
11	3.3	RxRESET_	NC (ID0)	GND (ID1)
12	3.3	WP_	SPI_A0	SPI_A1
13	3.3	SPI_MISO	SPI_CLK	SPI_A2
14	GND	SPI_M0	SPI_ENABLE	SPI_MOSI
15	GND	SPI_M2	SPI_M1	SPI_M3
16	GND	GND	GND	NC
17	GND	16.8MHz_RX	GND	NC (WB switch)
18	GND	16.8MHz_RX_RTN	GND	NC (MC switch)

Table 29 ***RX2 P5 Pinout, RF Input and Output Connection***

Row	A	B	C	D	E
1	GND	-	GND	-	GND
2	-	RX3_EXP2	-	RX2_EXP3	-
3	GND	-	GND	-	GND
4	GND	-	GND	-	GND
5	-	RX1_EXP1	-	RX2_EXP2	-
6	GND	-	GND	-	GND
7	GND	-	GND	-	GND
8	-	RX Branch 2	-	RX2_EXP1	-
9	GND	-	GND	-	GND

RX3 Connections

Table 30 ***RX3 P6 Pinout, Signal and Power***

Row	A	B	C	D
1	NC	GND	GND	Clock_SyncB_
2	GND	DSPIb_MOSI_RTN	DSPIb_CLK_RTN	DSPIb_EN_1
3	GND	DSPIb_MOSI	DSPIb_CLK	DSPIb_EN_2
4	GND	GND	GND	GND
5	14.2	SSI_CLK_C_RTN	SSI_FS_D	SSI_CLK_D_RTN
6	14.2	SSI_CLK_C	SSI_FS_C	SSI_CLK_D
7	14.2	GND	GND	GND
8	14.2	SSI_Data_C_RTN	GND	SSI_Data_D
9	GND	SSI_Data_C	GND	SSI_Data_D_RTN
10	GND	NC	NC	NC
11	3.3	RxRESET_	GND (ID0)	NC (ID1)
12	3.3	WP_	SPI_A0	SPI_A1
13	3.3	SPI_MISO	SPI_CLK	SPI_A2
14	GND	SPI_M2	SPI_ENABLE	SPI_MOSI
15	GND	SPI_M1	SPI_M0	SPI_M3
16	GND	GND	GND	NC
17	GND	16.8MHz_RX	GND	GND (WB switch)
18	GND	16.8MHz_RX_RTN	GND	NC (MC switch)

Table 31 ***RX3 P7 Pinout, RF Input and Output Connection***

Row	A	B	C	D	E
1	GND	-	GND	-	GND
2	-	RX1_EXP2	-	RX3_EXP3	-
3	GND	-	GND	-	GND
4	GND	-	GND	-	GND
5	-	RX2_EXP1	-	RX3_EXP2	-
6	GND	-	GND	-	GND
7	GND	-	GND	-	GND
8	-	RX Branch 3	-	RX3_EXP1	-
9	GND	-	GND	-	GND

RX4 Connections

Table 32 ***RX4 P8 Pinout, Signal and Power***

Row	A	B	C	D
1	NC	GND	GND	Clock_SyncB_
2	GND	DSPIb_MOSI_RTN	DSPIb_CLK_RTN	DSPIb_EN_3
3	GND	DSPIb_MOSI	DSPIb_CLK	DSPIb_EN_2
4	GND	GND	GND	GND
5	14.2	SSI_CLK_D_RTN	NC	NC
6	14.2	SSI_CLK_D	SSI_FS_D	NC
7	14.2	GND	GND	GND
8	14.2	SSI_Data_D_RTN	GND	NC
9	GND	SSI_Data_D	GND	NC
10	GND	NC	NC	NC
11	3.3	RxRESET_	NC (ID0)	NC (ID1)
12	3.3	WP_	SPI_A0	SPI_A1
13	3.3	SPI_MISO	SPI_CLK	SPI_A2
14	GND	SPI_M0	SPI_ENABLE	SPI_MOSI
15	GND	SPI_M3	SPI_M2	SPI_M1
16	GND	GND	GND	NC
17	GND	16.8MHz_RX	GND	NC (WB switch)
18	GND	16.8MHz_RX_RTN	GND	GND (MC switch)

Table 33 ***RX4 P9 Pinout, RF Input and Output Connection***

Row	A	B	C	D	E
1	GND	-	GND	-	GND
2	-	RX1_EXP3	-	NC	-
3	GND	-	GND	-	GND
4	GND	-	GND	-	GND
5	-	RX2_EXP3	-	NC	-
6	GND	-	GND	-	GND
7	GND	-	GND	-	GND
8	-	RX3_EXP1	-	NC	-
9	GND	-	GND	-	GND

PA Connections

Table 34 ***QUAD BR PA P10 Pinout, Signal and Power***

Row	A	B	C
1	SPI_ENABLE	GND	28.6 Vdc
2	GND	GND	28.6 Vdc
3	SPI_A0	GND	28.6 Vdc
4	GND	GND	28.6 Vdc
5	SPI_A1	GND	28.6 Vdc
6	GND	GND	28.6 Vdc
7	SPI_A2	GND	28.6 Vdc
8	GND	GND	28.6 Vdc
9	SPI_M0	GND	28.6 Vdc
10	GND	GND	28.6 Vdc
11	SPI_M1	GND	28.6 Vdc
12	GND	GND	28.6 Vdc
13	SPI_M2	GND	28.6 Vdc
14	GND	GND	28.6 Vdc
15	SPI_M3	GND	28.6 Vdc
16	GND	GND	28.6 Vdc
17	SPI_MISO	GND	28.6 Vdc
18	GND	GND	28.6 Vdc
19	SPI_MOSI	GND	28.6 Vdc
20	GND	GND	28.6 Vdc
21	SPI_CLK	GND	28.6 Vdc
22	GND	3.3 Vdc	28.6 Vdc
23	WP*	3.3 Vdc	28.6 Vdc
24	GND	GND	28.6 Vdc
25	PA_ENABLE	GND	28.6 Vdc
26	GND	14.2 Vdc	28.6 Vdc
27	GND	14.2 Vdc	28.6 Vdc
28	GND	14.2 Vdc	28.6 Vdc
29	GND	14.2 Vdc	28.6 Vdc
30	GND	28.6 Vdc	28.6 Vdc
31	GND	28.6 Vdc	28.6 Vdc
32	GND	28.6 Vdc	28.6 Vdc

Table 35 ***EXBRC P16 Pinout, PA from Exciter***

Coaxial	Description
Center	PA IN
Outer	GND

Table 36 ***EXBRC P17 Pinout, PA to Exciter***

Coaxial	Description
Center	PA Feedback
Outer	GND

Table 37 ***EXBRC P18 Pinout, PA RF OUT***

Coaxial	Description
Center	PA RF OUT
Outer	GND

External Connections

Table 38 ***QUAD BR Backplane Coaxial and DC***

	Signal
P12	-48 Vdc Power
P13	EX Out
P14	Feedback
P15	Ethernet
P16	PA In
P17	PA Feedback
P18	PA RF OUT
P19	RX Branch 1
P20	RX Branch 2
P21	RX Branch 3
P24	5 MHz/1 PPS

Table 39 **QUAD BR Backplane Alarm 25 Pin Dsub (P23)**

	Alarm Signal
1	EXT_GPI_1_
2	EXT_GPO_1_
3	GND
4	EXT_GPI_2_
5	EXT_GPO_2_
6	
7	
8	
9	
10	GND
11	
12	
13	
14	
15	
16	GND
17	BAT_STAT_
18	MTR_STAT_
19	EXT_VFWD
20	EXT_VREV
21	GND
22	GND
23	
24	
25	GND

Table 40 **QUAD BR Backplane RS-232 9 Pin Dsub (P22)**

	RS-232 Signal
1	CD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	BRG*

PS Connections

Table 41 ***QUAD PS Power and Signal (P11)***

Pin	Description	Pin	Description	Pin	Description
1	GND (Plug In)	31	3.3 Vdc	61	SPI_MOSI
2	GND	32	GND	62	SPI_CLK
3	GND	33	GND	63	N.C.
4	28.6 Vdc	34	GND	64	N.C.
5	28.6 Vdc	35	GND	65	N.C.
6	28.6 Vdc	36	GND	66	N.C.
7	28.6 Vdc	37	GND	67	SPI_A0
8	28.6 Vdc	38	GND	68	SPI_A1
9	28.6 Vdc	39	GND	69	SPI_M2
10	28.6 Vdc	40	GND	70	SPI_M3
11	28.6 Vdc	41	GND	71	SPI_M1
12	28.6 Vdc	42	GND	72	SLEEP_
13	28.6 Vdc	43	GND	73	SPI_M0
14	28.6 Vdc	44	GND	74	WP_
15	28.6 Vdc	45	GND	75	SPI_A2
16	14.2 Vdc	46	GND	76	GND
17	14.2 Vdc	47	GND	77	GND
18	14.2 Vdc	48	GND	78	GND
19	14.2 Vdc	49	GND		
20	14.2 Vdc	50	GND		
21	14.2 Vdc	51	GND		
2	14.2 Vdc	52	GND		
23	14.2 Vdc	53	GND		
24	3.3 Vdc	54	NC (FAN CON-TROL)		
25	3.3 Vdc	55	N.C.		
26	3.3 Vdc	56	N.C.		
27	3.3 Vdc	57	SHUTDOWN_		
28	3.3 Vdc	58	NC (Power shar-ing)		
29	3.3 Vdc	59	SPI_ENABLE		
30	3.3 Vdc	60	SPI_MISO		

-

Table 42 ***QUAD BR 48 Vdc Battery Power (P12)***

Pin	Description	Description	Pin
1	+ BATTERY	+ BATTERY	5
2	+ BATTERY	+ BATTERY	6
3	- BATTERY (RTN)	- BATTERY (RTN)	7
4	- BATTERY (RTN)	- BATTERY (RTN)	8

QUAD Base Radio Signals

Table 43 lists and describes signals for the QUAD Base Radio.

Table 43 ***QUAD Base Radio Signal Descriptions***

Signal Name	Description	Special
28.6 Vdc	28.6 Vdc output from PS	
14.2 Vdc	14.2 Vdc output from PS	
3.3 Vdc	3.3 Vdc output from PS	
GND	Station Ground	
RX Branch 1	RX Branch 1 from RFDS	50 Ω
RX Branch 2	RX Branch 2 from RFDS	50 Ω
RX Branch 3	RX Branch 3 from RFDS	50 Ω
RX1_EXP1	RX1 (branch 1) expansion output 1	50 Ω
RX1_EXP2	RX1 (branch 1) expansion output 2	50 Ω
RX1_EXP3	RX1 (branch 1) expansion output 3	50 Ω
RX2_EXP1	RX2 (branch 2) expansion output 1	50 Ω
RX2_EXP2	RX2 (branch 2) expansion output 2	50 Ω
RX2_EXP3	RX2 (branch 2) expansion output 3	50 Ω
RX3_EXP1	RX3 (branch 3) expansion output 1	50 Ω
RX3_EXP2	RX3 (branch 3) expansion output 2	50 Ω
RX3_EXP3	RX3 (branch 3) expansion output 3	50 Ω
5 MHz/1 PPS	5 MHz/1 PPS reference to the BRC	
SPI_ENABLE	Host Centric SPI Enable	
SPI_MISO	Host Centric SPI MISO	
SPI_MOSI	Host Centric SPI MOSI	
SPI_CLK	Host Centric SPI Clock	
SPI_A0	Host SPI Device Address Line A0	
SPI_A1	Host SPI Device Address Line A1	
SPI_A2	Host SPI Device AddressLine A2	
SPI_M0	Host SPI Module Address Line M0	
SPI_M1	Host SPI Module Address Line M1	
SPI_M2	Host SPI Module Address Line M2	
SPI_M3	Host SPI Module Address Line M3	
WP_	Write Protect (active low)	
PA_ENABLE	Turns off PA bias with active low	
SLEEP_	Sleep signal from PS	
SHUTDOWN_	PS reset line from BRC	
CD	RS232 Carrier Detect	
RxD	RS232 RX Data	

Table 43 ***QUAD Base Radio Signal Descriptions (Continued)***

Signal Name	Description	Special
TxD	RS232 TX Data	
DTR	RS232 Data Terminal Ready	
DSR	RS232 Data Set Ready	
RTS	RS232 Request to Send	
CTS	RS232 Clear to Send	
BRG	Baud Rate Generator	
RxRESET_	Reset Signal to RX modules	
16.8MHz_RX	16.8 MHz reference to RX	differential
16.8MHz_RX_RTN	16.8 MHz reference to RX return	differential
Clock_SyncA_	Clock Sync signal to RX1 & RX2	For Abacus III
Clock_SyncB_	Clock Sync signal to RX3 & RX4	For Abacus III
SSI_Data_A	RX Data from RX module 1	differential
SSI_Data_A_RTN	RX Data from RX module 1return	differential
SSI_Data_B	RX Data from RX module 2	differential
SSI_Data_B_RTN	RX Data from RX module 2 return	differential
SSI_Data_C	RX Data from RX module 3	differential
SSI_Data_C_RTN	RX Data from RX module 3 return	differential
SSI_Data_D	RX Data from RX module 4	differential
SSI_Data_D_RTN	RX Data from RX module 4 return	differential
SSI_CLK_A	RX Clock from RX module 1	differential
SSI_CLK_A_RTN	RX Clock from RX module 1 return	differential
SSI_CLK_B	RX Clock from RX module 2	differential
SSI_CLK_B_RTN	RX Clock from RX module 2 return	differential
SSI_CLK_C	RX Clock from RX module 3	differential
SSI_CLK_C_RTN	RX Clock from RX module 3 return	differential
SSI_CLK_D	RX Clock from RX module 4	differential
SSI_CLK_D_RTN	RX Clock from RX module 4 return	differential
SSI_FS_A	RX Frame Sync from RX module 1	
SSI_FS_B	RX Frame Sync from RX module 2	
SSI_FS_C	RX Frame Sync from RX module 3	
SSI_FS_D	RX Frame Sync from RX module 4	
DSPIa_En_1	DSPa SPI RX1 Abacus enable	
DSPIa_En_3	DSPa SPI RX2 Abacus enable	
DSPIa_En_2	DSPa SPI RX1 & RX2 SGC enable	
DSPIb_En_1	DSPb SPI RX3 Abacus enable	
DSPIb_En_3	DSPb SPI RX4 Abacus enable	
DSPIb_En_2	DSPb SPI RX3 & RX4 SGC enable	
DSPIa_MOSI	DSPa SPI MOSI	differential
DSPIa_MOSI_RTN	DSPa SPI MOSI return	differential
DSPIb_MOSI	DSPb SPI MOSI	differential

Table 43 ***QUAD Base Radio Signal Descriptions (Continued)***

Signal Name	Description	Special
DSPIb_MOSI_RTN	DSPb SPI MOSI return	differential
DSPIa_CLK	DSPa SPI Clock	differential
DSPIa_CLK_RTN	DSPa SPI CLK return	differential
DSPIb_CLK	DSPb SPI Clock	differential
DSPIb_CLK_RTN	DSPb SPI CLK return	differential
MTR_STAT_	External Wattmeter Status	
BAT_STAT_	Battery Status	
EXT_VFWD	External Wattmeter Forward meter	
EXT_VREV	External Wattmeter Reflected meter	
EXT_GPO_1_	General purpose output 1	
EXT_GPO_2_	General purpose output 2	
EXT_GPI_1_	General purpose input 1	
EXT_GPI_2_	General purpose input 2	
NC	Not connected	reserved

Legacy Single Channel Base Radio FRU Replacement Procedures

Replace suspected station modules with known non-defective modules to restore the station to proper operation. The following procedures provide FRU replacement instructions and post-replacement adjustments and/or verification instructions.

Legacy Single Channel Base Radio Replacement Procedure

NOTE

The Legacy Base Radio removal and installation procedures are included for reference or buildout purposes. Field maintenance of Legacy Base Radios typically consists of replacement of FRUs within the Legacy Base Radio. Perform Legacy Base Radio FRU replacement in accordance with "Legacy Base Radio FRU Replacement Procedure" below.

Perform Legacy Base Radio (BR) replacement as described in the following paragraphs.

Removal

Remove BR from Equipment Cabinet as follows:

1. Remove power from the Base Radio by setting the Power Supply ON/OFF switch to the OFF position.
2. Tag and disconnect the cabling from the BR rear panel connectors.
3. Remove the four M6 TORX screws which secure the BR front panel to the Equipment Cabinet mounting rails.

⚠ WARNING

BR WEIGHT EXCEEDS 60 LBS (27 KG). USE TWO-PERSON LIFT WHEN REMOVING OR INSTALLING BR FROM EQUIPMENT CABINET. MAKE CERTAIN BR IS FULLY SUPPORTED WHEN BR IS FREE FROM MOUNTING RAILS.

4. While supporting the BR, carefully remove the BR from the Equipment Cabinet by sliding the BR from the front of cabinet.

Installation

Install BR in Equipment Cabinet as follows:

1. If adding a BR, install side rails in the appropriate BR mounting position in the rack.
2. While supporting the BR, carefully lift and slide the BR in the Equipment Cabinet mounting position.
3. Secure the BR to the Equipment Cabinet mounting rails using four M6 TORX screws. Tighten the screws to 40 in-lb (4.5 Nm).
4. Connect the cabling to the BR rear panel connectors as tagged during the BR removal. If adding a BR, perform the required cabling in accordance with the Cabling Information subsection of the RFDS section applicable to the system.
5. Perform BR activation in accordance with Station Verification Procedures below.

Anti-Static Precautions

▲ CAUTION

The Base Radio contains static-sensitive devices. when replacing Base Radio FRUs, always wear a grounded wrist strap and observe proper anti-static procedures to prevent electrostatic discharge damage to Base Radio modules.

Motorola publication 68P81106E84 provides complete static protection information. This publication is available through Motorola National Parts.

Observe the following additional precautions:

- ❒ Wear a wrist strap (Motorola Part No. 4280385A59 or equivalent) at all times when servicing the Base Radio to minimize static build-up.
- ❒ A grounding clip is provided with each EBTS cabinet. If not available, use another appropriate grounding point.
- ❒ DO NOT insert or remove modules with power applied to the Base Radio. ALWAYS turn the power OFF using the Power Supply rocker switch on the front of the Power Supply module.
- ❒ Keep spare modules in factory packaging for transporting. When shipping modules, always pack in original packaging.

Legacy BR FRU Replacement Procedure

Perform the following steps to replace any of the Legacy Base Radio FRUs:

NOTE

When servicing Legacy Base Radios (BRs) in situations where the Control Board or the entire Legacy BR is replaced, the integrated Site Controller (iSC) will automatically reboot the serviced BR if the BR has been off-line for a period not less than the value contained in "Replacement BRC Accept Timer" (default is 3 minutes). If the BR is turned on prior to that time value, power the BR down and wait the minimum timer length before re-powering the BR.

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Loosen the front panel fasteners. These are located on each side of the module being replaced.
3. Pull out the module.
4. Insert the non-defective replacement module by aligning the module side rails with the appropriate rail guides inside the Base Radio chassis.
5. Gently push the replacement module completely into the Base Radio chassis assembly using the module handle(s).

▲ CAUTION

DO NOT slam or force the module into the chassis assembly. This will damage the connectors or backplane.

6. Secure the replacement module by tightening the front panel fasteners to the specified torque of 5 in-lbs.
7. Apply power to the Base Radio by setting the switch to the ON position.
8. Perform the Station Verification Procedure provided below.

Legacy Single Channel BR Power Amplifier (PA) Fan FRU Replacement

Perform the following steps to replace the Power Amplifier (PA) fans.

1. Remove the Power Amplifier from the Base Radio per FRU Replacement Procedure.
2. Disconnect fan power cable from PA housing.
3. Remove front panel from fan assembly.
4. Remove fan assembly from PA chassis.

NOTE

Reverse above procedure to install new fan kit.

Legacy Single Channel BR Station Verification Procedures

Perform the Station Verification Procedures whenever you replace a FRU. The procedures verify transmit and receive operations. Each procedure also contains the equipment set-up.

Legacy Single Channel BR Replacement FRU Verification

All module specific information is programmed in the factory prior to shipment. Base Radio specific information (e.g., receive and transmit frequencies) is downloaded to the Base Radio from the network/site controller.

Replacement FRU alignment is not required for the Base Radio.

Legacy Single Channel BR Base Repeater FRU Hardware Revision Verification

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of service to system users.

1. Connect one end of the RS-232 cable to the service computer.
2. Connect the other end of the RS-232 cable to the STATUS port, located on the front panel of the BRC.
3. Using the field password, login to the BR.

4. Collect revision numbers from the station by typing the following commands:

```
BRC>dekey
BRC>test_mode
BRC>get brc_rev_no
BRC>get rx1_rev_no
BRC>get rx2_rev_no
BRC>get rx3_rev_no              (if BR is 3 branch)
BRC>get pa_rev_no
BRC>get ex_rev_no

BRC>
```

5. If all modules return revision numbers of the format "Rxx.xx.xx", then all revision numbers are present and no further action is required. Log out and repeat steps 1 through 5 for each additional BR.

   If revision numbers were returned as blank or not in the format "Rxx.xx.xx", contact your local Motorola representative or Technical Support.

6. When all BRs have been checked, log out.

Legacy Single Channel BR Transmitter Verification

The transmitter verification procedure verifies the transmitter operation and the integrity of the transmit path. This verification procedure is recommended after replacing an Exciter, Power Amplifier, BRC, or Power Supply module.

NOTE

The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of service to system users.

Equipment Setup

To set up the equipment, use the following procedure:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.

2. Connect one end of the RS-232 cable to the service computer.

3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.

⚠ CAUTION

Make sure power to BR is OFF before disconnecting transmitter RF connectors. Disconnecting transmitter RF connectors while the BR is keyed may result in RF burns from arcing.

4. Disconnect the existing cable from the connector labeled PA OUT. This connector is located on the backplane of the Base Radio.
5. Connect a test cable to the PA OUT connector.
6. Connect a 10 dB attenuator on the other end of the test cable.
7. From the attenuator, connect a cable to the RF IN/OUT connector on the R2660 Communications Analyzer.
8. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.
9. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

10. Set the R2660 to the EXT REF mode.
11. Apply power to the R2660.
12. Set the R2660 to the SPECTRUM ANALYZER mode with the center frequency set to the transmit frequency of the Base Radio under test.
13. Perform the appropriate transmitter verification procedure below for the particular Power Amplifier used in the Base Radio.

Legacy Single Channel BR Transmitter Verification Procedure (40W, 800 MHz Power Amplifier – TLF2020)

This procedure provides commands and responses to verify proper operation of the transmit path for 800 MHz Base Radios using a 40 Watt Power Amplifier.

1. Apply power to the Base Radio by setting the switch to the 1 position.

   The following message displays on the service computer during power-up.

```
Base Radio
firmware revision RXX.XX.XX
Copyright © 1998
Motorola, Inc. All rights reserved.

Unauthorized access prohibited

Enter login password:
```

2. Enter the proper password. After entering the correct password, the BRC> prompt is displayed on the service computer.

   The default password is **motorola**

NOTE

Motorola recommends changing the default password, once proper operation of the equipment is verified.

3. At the BRC> prompt, type: **dekey**

   This command verifies that there is no RF power being transmitted.

```
BRC> dekey
XMIT OFF INITIATED
```

▲ CAUTION

The following command keys the transmitter. Make sure that transmission only occurs on licensed frequencies or into a RF load.

4. At the BRC> prompt, type: **set tx_power 40**

This command sets the transmitter output to 40 Watts.

```
BRC> set tx_power 40
setting transmitter power to 40 watts

TXLIN ATTENUATION: 5.000000


TARGET POWER: 40.00 watts [46.02 dBm]
ACTUAL POWER: 37.77 watts [45.07 dBm]
POWER WINDOW: 38.20-> 41.89 watts [45.82 -> 46.22 dBm]
TXLIN LEVEL REGISTER REDUCED 59 STEPS [-2.30 dB].
TXLIN LEVEL: 0x6f
```

After keying the Base Radio, verify the forward and reflected powers of the station along with the station VSWR with the parameters listed in Table 44.

Table 44 ***Legacy BR 40W, 800 MHz PA Transmitter Parameters***

Parameter	Value or Range
Forward Power	Greater than 38.0 Watts
Reflected Power	Less than 4.0 Watts
VSWR	Less than 2:1

5. At the BRC> prompt, type: **get fwd_pwr**

This command returns the current value of forward power from the RF Power Amplifier.

```
BRC> get fwd_pwr
FORWARD POWER is 39.13 watts [45.92 dBm]
```

6. At the BRC> prompt, type: **get ref_pwr**

   This command returns the current value of reflected power from the RF Power Amplifier.

```
BRC> get ref_pwr
REFLECTED POWER is 0.27 watts [24.28 dBm]
```

7. At the BRC> prompt, type: **get vswr**

   This command calculates the current Voltage Standing Wave Ratio (VSWR) from the RF Power Amplifier.

```
BRC> get vswr
VSWR is 1.17:1
```

8. At the BRC> prompt, type: **get alarms**

   This command returns all active alarms of the Base Radio.

```
BRC> get alarms
NO ALARM CONDITIONS DETECTED
```

NOTE

If the **get alarms** command displays alarms, refer to the *System Troubleshooting* section of this manual for corrective actions.

9. View the spectrum of the transmitted signal on the R2660 Communications Analyzer in the Spectrum Analyzer mode. Figure 11 shows a sample of the spectrum.

10. At the BRC> prompt, type: **dekey**

    This command stops all transmitter activity.

```
BRC> dekey
XMIT OFF INITIATED
```

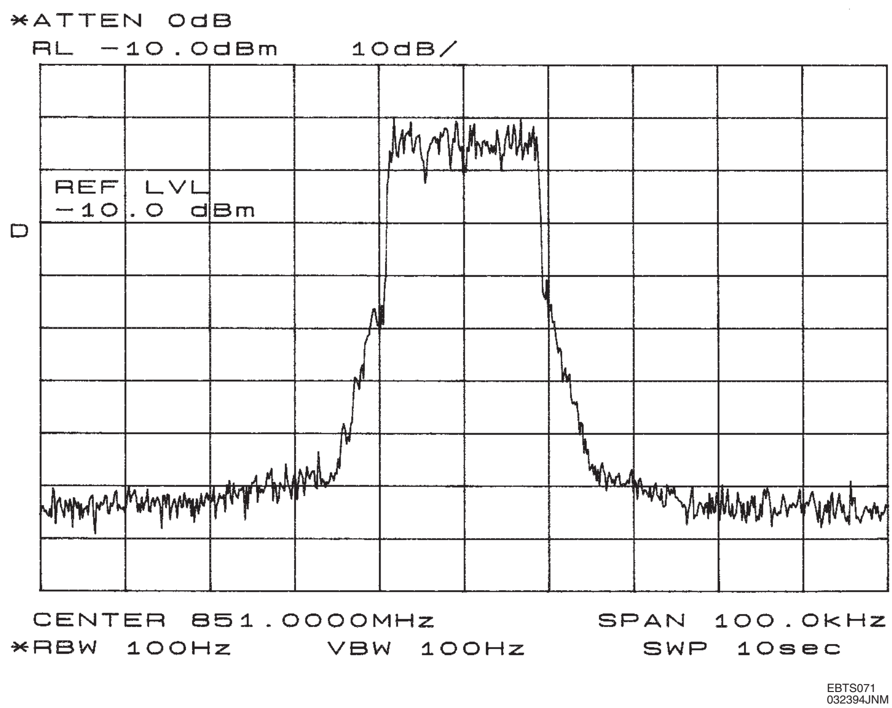

Figure 10 ***Transmitted Signal Spectrum (800 MHz Legacy BR)***

Legacy Single Channel BR Transmitter Verification Procedure (70W, 800 MHz Power Amplifiers – CTF1040)

This procedure provides commands and responses to verify proper operation of the transmit path for 800 MHz Base Radios using a 70 Watt Power Amplifier.

1. Apply power to the Base Radio by setting the switch to the 1 position.

The following message displays on the service computer during power-up.

```
Base Radio
firmware revision RXX.XX.XX
Copyright © 1998
Motorola, Inc. All rights reserved.

Unauthorized access prohibited

Enter login password:
```

2. Enter the proper password. After entering the correct password, the BRC> prompt is displayed on the service computer.

   The default password is **motorola**

NOTE

Motorola recommends changing the default password once proper operation of the equipment is verified.

3. At the BRC> prompt, type: **dekey**

   This command verifies that there is no RF power being transmitted.

```
BRC> dekey
XMIT OFF INITIATED
```

▲ CAUTION

The following command keys the transmitter. Make sure that transmission only occurs on licensed frequencies or into an RF load.

4. At the BRC> prompt, type: **set tx_power 70**

   This command sets the transmitter output to 70 Watts.

```
BRC> set tx_power 70
setting transmitter power to 70 watts

TXLIN ATTENUATION: 5.000000


TARGET POWER: 70.00 watts [48.45 dBm]
ACTUAL POWER: 56.70 watts [47.54 dBm]
POWER WINDOW: 66.85 -> 73.30 watts [48.25 -> 48.65 dBm]
TXLIN LEVEL REGISTER REDUCED 85 STEPS [-3.32 dB].
TXLIN LEVEL: 0x55
```

After keying the Base Radio, verify the forward and reflected powers of the station along with the station VSWR with the parameters listed in Table 45.

Table 45 **Legacy BR 70W, 800 MHz PA Transmitter Parameters**

Parameter	Value or Range
Forward Power	Greater than 66.5 Watts
Reflected Power	Less than 7.0 Watts
VSWR	Less than 2:1

5. At the BRC> prompt, type: **get fwd_pwr**

This command returns the current value of forward power from the RF Power Amplifier.

```
BRC> get fwd_pwr
FORWARD POWER is 68.55 watts [48.36 dBm]
```

6. At the BRC> prompt, type: **get ref_pwr**

This command returns the current value of reflected power from the RF Power Amplifier.

```
BRC> get ref_pwr
REFLECTED POWER is 2.10 watts [33.22 dBm]
```

7. At the BRC> prompt, type: **get vswr**

This command calculates the current Voltage Standing Wave Ratio (VSWR) from the RF Power Amplifier.

```
BRC> get vswr
VSWR is 1.42:1
```

8. At the BRC> prompt, type: **get alarms**

This command returns all active alarms of the Base Radio.

```
BRC> get alarms
NO ALARM CONDITIONS DETECTED
```

> **NOTE**
>
> If the **get alarms** command displays alarms, refer to the *System Troubleshooting* section of this manual for corrective actions.

9. View the spectrum of the transmitted signal on the R2660 Communications Analyzer in the Spectrum Analyzer mode. Figure 11 shows a sample of the spectrum.

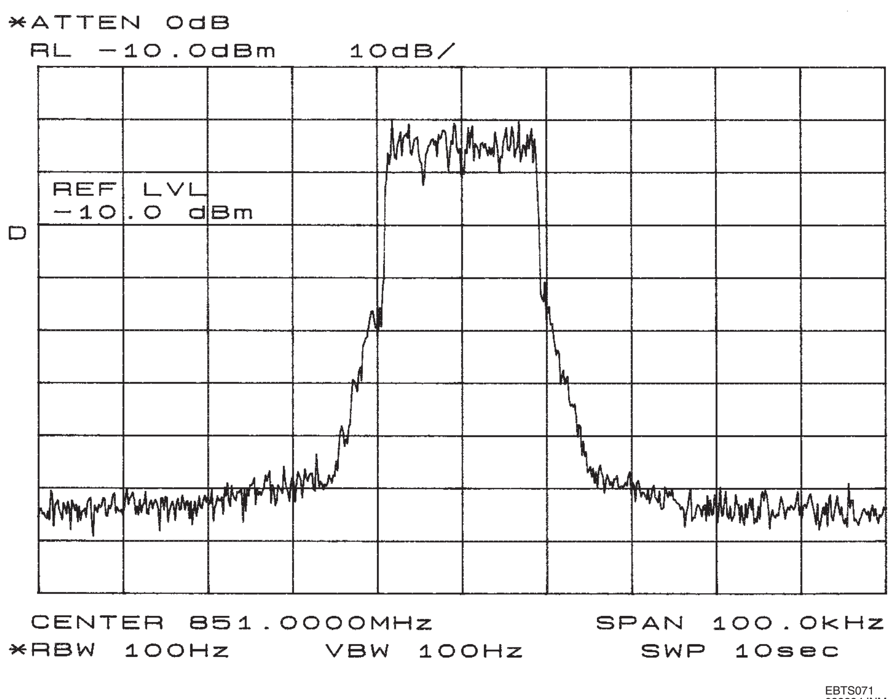

Figure 11 ***Transmitted Signal Spectrum (800 MHz Legacy BR)***

10. At the BRC> prompt, type: **dekey**

    This command stops all transmitter activity.

```
BRC> dekey
XMIT OFF INITIATED
```

Legacy Single Channel BR Receiver Verification

The receiver verification procedure sends a known test signal to the Base Radio to verify the receive path. This verification procedure is recommended after replacing a Receiver, BRC, or Power Supply module.

NOTE
The following procedure requires the Base Radio to be out of service. Unless the Base Radio is currently out of service, Motorola recommends performing this procedure during off-peak hours. This minimizes or eliminates disruption of service to system users.

Equipment Setup

Set up the equipment for the receiver verification procedure as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Connect one end of the RS-232 cable to the service computer.
3. Connect the other end of the RS-232 cable to the STATUS port located on the front panel of the BRC.
4. Disconnect the existing cable from the connector labeled RX1 (or the connector corresponding to the receiver under test).

   This connector is located on the backplane of the Base Radio.
5. Connect a test cable to the RX 1 connector.
6. Connect the other end of the test cable to the RF IN/OUT connector on the R2660 Communications Analyzer.
7. Remove power from the R2660 and connect the Rubidium Frequency Standard 10MHZ OUTPUT to a 10 dB attenuator.
8. Connect the other end of the 10 dB attenuator to the 10MHZ REFERENCE OSCILLATOR IN/OUT connector on the R2660.
9. Set the R2660 to the EXT REF mode.
10. Apply power to the R2660.

NOTE

Refer to the equipment manual provided with the R2660 for further information regarding mode configuration of the unit (Motorola Part No. 68P80386B72).

11. Set the R2660 to the receive frequency of the Base Radio under test.

    All receivers within a single Base Radio have the same receive frequency.

12. Set the R2660 to generate the test signal at an output level of -80dBm.

Receiver Verification Procedure

This procedure provides commands and responses to verify proper operation of the Base Radio receive path. Perform the procedure on all three receivers in each Base Radio in the EBTS.

The Bit Error Rate (BER) measurement meets specifications at less than 0.01% (1.0e-02%) to pass the process.

Before you begin the verification procedure, put the Base Radio into the test mode of operation to take it out of service. Enable the desired receiver under test and disable the other receiver(s). In this case the receiver under test is receiver #1.

In the following procedures, enter the software commands as they appear after the prompt. These commands are in bold letters.

For example, BRC> **get rx_freq**

13. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.

    The following message displays on the service computer during power-up.

```
Base Radio
firmware revision RXX.XX.XX
Copyright © 1998
Motorola, Inc. All rights reserved.

Unauthorized access prohibited

Enter login password:
```

14. Enter the proper password. After entering the correct password, the BRC> prompt is displayed on the service computer.

    The default password is **motorola**

NOTE

Motorola recommends changing the default password, once proper operation of the equipment is verified.

15. At the BRC> prompt, type: **get rx_freq**

    This command displays the receive frequency for the current Base Radio. For 800/900/1500 MHz Base Radios, the message respectively appears as:

    800 MHz BR:

```
BRC> get rx_freq
The RX FREQUENCY is: 806.00000
```

16. Verify that the R2660 transmit frequency is set to the frequency determined in the previous step.

17. At the BRC> prompt, type: **set rx_mode 1**

    This command is used to enable the antenna/receiver under test.

```
BRC>set rx_mode 1
set RECEIVER 1 to ENABLED in RAM
set RECEIVER 2 to DISABLED in RAM
set RECEIVER 3 to DISABLED in RAM
```

18. At the BRC> prompt, type: **get rssi 1 1000**

    This commands returns the receive signal strength indication. To pass the BER floor test, the Bit Error Rate must be less than 0.01% (1.0e-02%) for the displayed results.

```
BRC> get rssi 1 1000
Starting RSSI monitor for 1 repetitions averaged each 1000 reports.

Line                    RSSI1     RSSI2RSSI3SGC CI
BER                               OffsetSyncMiss
                        dBm       dBmdBm  dB dBmdBm
%                                 Hz%
```

19. Verify that the RSSI dBm signal strength, for the receiver under test, is -80.0 dBm ± 1.0 dBm. Adjust the R2660 signal output level to get the appropriate RSSI dBm level. The BER floor% value is valid only if the RSSI signal strength is within the limits of -81.0 dBm to -79.0 dBm.

20. At the prompt, type: **get alarms**

This command returns all active alarms of the Base Radio.

```
BRC> get alarms
NO ALARM CONDITIONS DETECTED
```

NOTE

If the **get alarms** command displays alarms, refer to the System Troubleshooting section for corrective actions.

21. At the BRC> prompt, type: **get rx1_kit_no**

As shown below respectively for 800 /900/1500 MHz Base Radios, this command returns the kit number of the receiver.

800 MHz BR:

```
BRC> get rx1_kit_no
RECEIVER 1 KIT NUMBER IS CRF6010A
```

NOTE

If the kit number is CRF6010 or CRF6030, continue to step 22, otherwise to Equipment Disconnection.

22. At the BRC> prompt, type: **get rx_fru_config**

This command lists the receivers active for diversity.

```
BRC> get rx_fru_config
RECEIVER CONFIGURATION {RX1 RX2 RX3}
```

NOTE

If the antenna configuration does not match the receiver configuration, use the **set rx_fru_config** MMI command to properly set the parameter.

Equipment Disconnection

Disconnect equipment after verifying the receiver as follows:

1. Remove power from the Base Radio by setting the Power Supply rocker switch (located behind the front panel of the Power Supply) to the OFF (0) position.
2. Disconnect the RS-232 cable from the connector on the service computer.
3. Disconnect the other end of the RS-232 cable from the RS-232 connector on the front panel of the BRC.
4. Disconnect the test cable from the RX 1 connector located on the backplane of the Base Radio.
5. Connect the standard equipment cable to the RX 1 connector.
6. Disconnect the cable to the R2660 Communications Analyzer.
7. Restore power to the Base Radio by setting the Power Supply rocker switch to the ON (1) position.

   This completes the Receiver Verification Procedure for the receiver under test.

Repeat the Receiver Verification Procedure for each receiver in every Base Radio in the EBTS.

Legacy Single Channel Base Radio Backplane

Legacy Single Channel BR Backplane Connectors

All external equipment connections are made on the Base Radio backplane. Table 4 lists and describes each of the connectors on the backplane.

Table 46 ***Legacy Base Radio Backplane Connectors***

Connector	Description	Type
RX 1 through RX 3	Provides the input path for the received signal to the Base Radio. Each receiver has an input for one of these signals. Connect these ports to a multicoupler distribution system and surge protection circuitry before connecting them to the receive antennas.	RF-type connector in Table 5
EX OUT/EX FB PA IN/PA FB	Connects the exciter and PAs together to form the transmitter for the Base Radio. These connections are usually made at the factory These four ports close the feedback loop between these two modules by connecting EX OUT to the PA IN and the EX FB to the PA FB	RF-type connectors in Table 18 and Table 19
PA OUT	Transmits the RF output of the Base Radio. Connect this port to a combiner or duplexer before connecting to the transmit antenna	RF-type connector in Table 19
ETHERNET A (or labeled ETHERNET on some production units)	Provides Ethernet connectivity to the Base Radio from the site controller. This Ethernet port connects directly to the BRC	BNC-type connector in Table 15
5MHZ/ 1 PPS-A (or labeled SPARE on some production units)	Serves as both the timing and frequency reference port for the Base Radio This port is connected to the site timing/frequency reference.	BNC-type connector in Table 17
RS-232	This is a DTE RS-232 interface provided for future use and is not currently enabled	DB-9-type connectors in Table 11
ALARM	Provides the connection for external calibrated power monitors to the Base Radio This connector also provides station DC voltages and programming lines (SPI) for monitoring/potential future expansion	DB-25-type connector
AC POWER	Provides connection to AC power supply, if the Base Radio is equipped with an AC power supply	Line cord connector
DC POWER	Provides DC power connection, if the Base Radio is equipped with a DC power supply or an AC power supply to support the battery revert feature	Card edge connector
GROUND	Connects the station to ground. A ground stud and a ground braid on the back of the Base Radio connect the station to a site ground, such as an appropriately grounded cabinet This ground provides increased transient/surge protection for the station	Ground stud

Figure 4 shows the locations of the Legacy Base Radio external connections.

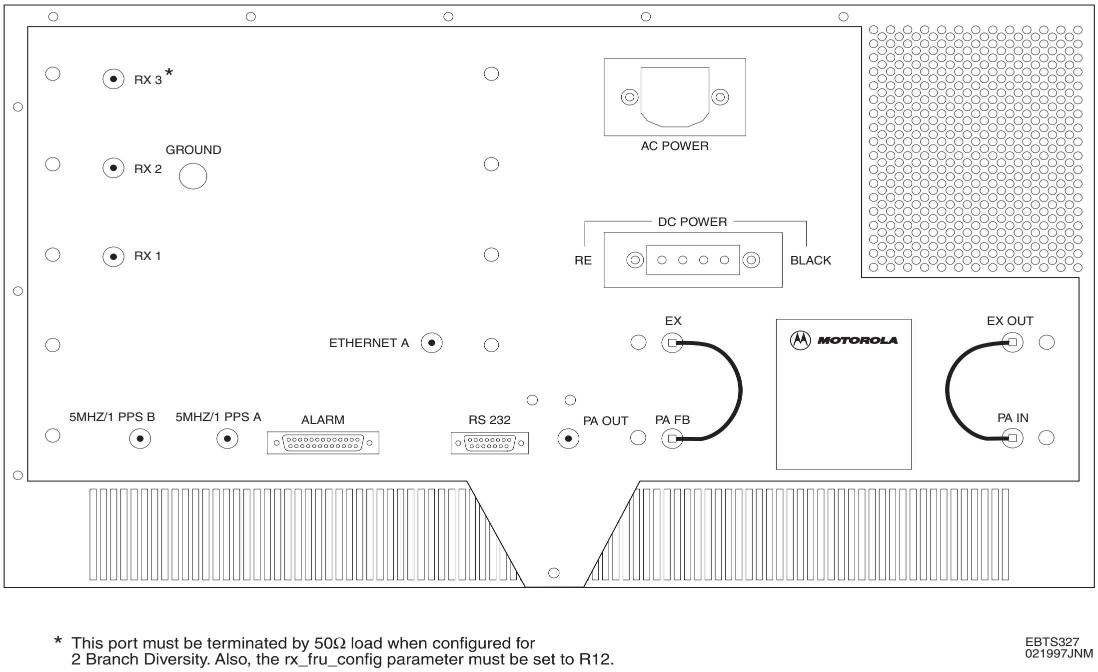

Figure 12 ***Legacy Base Radio Backplane Connectors***

Legacy Single Channel BR Backplane RF Connections

When Base Radios are shipped from the factory as FRUs, each connection on the back of a repeater has a designated color dot beside it as listed in Table 47. To find where a cable should be connected, match the label wrapped around the cable to the dot on the back of the repeater.

Table 47 ***Legacy BR RF Connector Code***

Connectors	Color Dot Code
TX	Orange
RX 1	Red
RX 2	Green
RX 3	Yellow
Ethernet	White
5 MHz/1 pps A or Spare	Gray

Legacy Single Channel BR Backplane Connector Pinouts

Table 48 lists the pin-outs for the 96-pin P1 connector of the Base Radio Controller board.

Table 48 ***Legacy BR P1 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	AGC3	14.2V	AGC1
2	AGC4	14.2V	AGC2
3	GND	GND	GND
4	RESET	GND	GND
5	BATT_STAT	GND	GND
6	CTS	GND	GND
7	RTS	5V	5V
8	5V	5V	5V
9	5V	5V	5V
10	SHUTDOWN	5V	
11	RCLK	5V	DATA1
12	ODC_1	5V	DATA1*
13	TCLK	GND	DATA3
14	ODC_3	GND	DATA3*
15	RXD	GND	DATA2
16	ODC_2		DATA2*
17	TXD		
18	SSI		SBI_1
19	SSI*		SBI_3
20	BRG	GND	SBI_2
21	CLK		
22	CLK*	GND	A4
23	GND		A3
24	A5	GND	A2
25	A0	GND	A1
26	CD	GND	5MHZ/ SPARE
27	METER_STAT	GND	SPI_MISO
28	WP*	GND	SPI_CLK
29	GND	GND	SPI_MOSI
30	GND	GND	GD
31	1PPS_GPS	GND	2.1MHZ_TX
32	GND	GND	2.1MHZ_RX
NOTE: * = enabled low			

Table 49 lists the pin-outs for the 96-pin P1 connector for Receiver 1.

Table 49 ***Legacy BR P1 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	AGC3	GND	AGC1
2	AGC4	GND	AGC2
3	GND	GND	GND
4	GND	GND	GND
5	14.2V	14.2V	14.2V
6	14.2V	14.2V	14.2V
7	GND	GND	GND
8	GND	GND	GND
9	5V	5V	5V
10	5V	5V	5V
11	GND	GND	GND
12	GND	GND	GND
13	DATA1*	GND	GND
14	DATA1	GND	GND
15	ODC_1	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	SBI_1	GND	GND
19	GND	GND	GND
20	GND	GND	GND
21			A0_CS1
22	A1_CS2		
23			A5
24			WP*
25	A4_RXSEL		
26			
27	SPI_MISO		
28			SPI_MOSI
29	SPI_CLK		
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	2.1MHZ_RX
NOTE: * Enabled low			

Table 50 lists the pin-outs for the 96-pin P2 connector for Receiver 2.

Legacy Single Channel Base Radio Backplane

Table 50 ***Legacy BR P2 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	AGC3	GND	AGC1
2	AGC4	GND	AGC2
3	GND	GND	GND
4	GND	GND	GND
5	14.2V	14.2V	14.2V
6	14.2V	14.2V	14.2V
7	GND	GND	GND
8	GND	GND	GND
9	5V	5V	5V
10	5V	5V	5V
11	GND	GND	GND
12	GND	GND	GND
13	DATA2*	GND	GND
14	DATA2	GND	GND
15	ODC_2	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	SBI_2	GND	GND
19	GND	GND	GND
20	GND	GND	GND
21			A0_CS1
22	A1_CS2		
23			A5
24			WP*
25	A3_RXSEL		
26			
27	SPI_MISO		
28			SPI_MOSI
29	SPI_CLK		
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	2.1MHZ_RX
NOTE: * Enabled low			

Table 51 lists the pin-outs for the 96-pin P3 connector for Receiver 3.

Table 51 ***Legacy BR P3 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	AGC3	GND	AGC1
2	AGC4	GND	AGC2
3	GND	GND	GND
4	GND	GND	GND
5	14.2V	14.2V	14.2V
6	14.2V	14.2V	14.2V
7	GND	GND	GND
8	GND	GND	GND
9	5V	5V	5V
10	5V	5V	5V
11	GND	GND	GND
12	GND	GND	GND
13	DATA3*	GND	GND
14	DATA3	GND	GND
15	ODC_3	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	SBI_3	GND	GND
19	GND	GND	GND
20	GND	GND	GND
21			A0_CS1
22	A1_CS2		
23			A5
24			WP*
25	A2_RXSEL		
26			
27	SPI_MISO		
28			SPI_MOSI
29	SPI_CLK		
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	2.1MHZ_RX
NOTE: * Enabled low			

Table 52 lists the pin-outs for the 48-pin P2 connector of the 3X Receiver.

Table 53 lists the pin-outs for the 16-pin P3 connector of the 3X Receiver.

Table 54 lists the pin-outs for the 96-pin P5 connector of the Exciter.

Table 55 lists the pin-outs for the 96-pin P6 connector of the Power Amplifier.

Legacy Single Channel Base Radio Backplane

Table 52 ***Legacy BR P2 Connector Pin-outs***

Pin No.	Row A	Row B	Row C	Row D
1	GND	AGC4	AGC3	GND
2	GND	AGC2	AGC1	A0
3	GND	RX1_DATA	RX1_DATA	A1
4	GND	RX1_SBI	RX1_ODC	A2
5	GND	RX2_DATA	RX2_DATA	A3
6	5V	RX2_SBI	RX2_ODC	A4
7	GND	RX3_DATA	RX3_DATA	A5
8	GND	RX3_SBI	RX3_ODC	WP*
9	14.2V	SCLK	MOSI	MISO
10	14.2V	GND	GND	GND
11	14.2V	GND	REF	GND
12	GND	GND	GND	GND
NOTE: Row A is make first, break last.				

Table 53 ***Legacy BR P3 Connector Pin-outs***

Pin No.	Row A	Row B	Row C	Row D	Row E
1	GND		GND		GND
2		RX1			
3	GND		GND		GND
4					
5					
6					
7	GND		GND		GND
8		RX2		RX3	
9	GND		GND		GND

Table 56 lists the pin-outs for the 25-pin P7 Alarm connector.

Table 57 lists the pin-outs for the 9-pin P8 RS-232 connector.

Table 58 lists the pin-outs for P13. Tables 59 through 62 list the pin-outs for the SMA and blindmate connectors for Receivers 1- 3, BRC, Exciter and PA.

Table 63 lists the pin-outs for 78-pin P9 connector of the Power Supply.

Table 54 ***Legacy BR P5 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	28V	28V	28V
2	28V	28V	28V
3	14.2V	14.2V	14.2V
4	14.2V	14.2V	14.2V
5	5V	5V	5V
6	5V	5V	5V
7	GND	GND	EXT_VFWD
8	GND	GND	EXT_VREF
9			
10	GND	GND	GND
11	GND	GND	VBLIN
12	GND	GND	RESET
13			
14	GND	GND	GND
15	GND	GND	SPI_MISO
16	A0	GND	GND
17	GND	GND	SPI_CLK
18	A1	GND	WP*
19	GND	GND	GND
20	A5	GND	SPI_MOSI
21	GND	GND	GND
22	A4	GND	GND
23	GND	GND	CLK*
24	A3	GND	GND
25	GND	GND	CLK
26	GND	GND	GND
27	GND	GND	SSI*
28	GND	GND	GND
29	GND	GND	SSI
30	GND	GND	GND
31	GND	GND	2.1MHz_TX
32	GND	GND	GND
NOTE: * = enabled low			

Legacy Single Channel Base Radio Backplane

Table 55 ***Legacy BR P6 Connector Pin-outs***

Pin No.	Row A	Row B	Row C
1	VBLIN	GND	28V
2	GND	GND	28V
3	A0	GND	28V
4	GND	GND	28V
5	A1	GND	28V
6	GND	GND	28V
7	A2	GND	28V
8	GND	GND	28V
9	A3	GND	28V
10	GND	GND	28V
11	SPI_MISO	GND	28V
12	GND	GND	28V
13	SPI_MOSI	GND	28V
14	GND	GND	28V
15	SPI_CLK	GND	28V
16	GND	GND	28V
17	WP*	GND	28V
18	GND	GND	28V
19	GND	GND	28V
20	GND	GND	28V
21	GND	GND	28V
22	GND	GND	28V
23	GND	GND	28V
24	GND	GND	28V
25	GND	5V	28V
26	GND	5V	28V
27	GND	14.2V	28V
28	GND	14.2V	28V
29	GND	14.2V	28V
30	GND	14.2V	28V
31	GND	28V	28V
32	GND	28V	28V
NOTE: * = enabled low			

Table 56 ***Legacy BR P7 Connector Pin-outs***

Pin No.	Signal
1	SPI_MISO
2	SPI_MOSI
3	SPI_CLK
4	A0
5	A1
6	A2
7	A3
8	A4
9	A5
10	GND
11	28V
12	14.2V
13	14.2V
14	WP*
15	5V
16	GND
17	BATT_STAT
18	MTR_STAT
19	EXT_VFWD
20	EXT_VREF
21	GND
22	GND
23	BAT_TEMP
24	VAT_TEMP
25	GND
NOTE: * = enabled low	

Legacy Single Channel Base Radio Backplane

Table 57 ***Legacy BR P8 Connector Pin-outs***

Pin No.	Signal
1	CD
2	RxD
3	TxD
4	RCLK
5	GND
6	TCLK
7	RTS
8	CTS
9	BRG

Table 58 ***Legacy BR P13 Connector Pin-outs***

Connector	Signal
1	ETHERNET - A (or 5MHZ IN*)
* May appear as indicated in parenthesis on some production units.	

Table 59 ***Legacy BR SMA Connectors- Receivers***

Connector	Signal
P19	RCV ONE RF IN
P20	RCV TWO RF IN
P21	RCV THREE RF IN

Table 60 ***Legacy BR Blind Mates - BRC***

Connector	Signal
P10	SPARE* (or 5MHZ/1 PPS - A)
P11	ETHERNET* (or ETHERNET - A)
*May appear as indicated in parenthesis on some production units.	

Table 61 ***Legacy BR Blind Mates - Exciter***

Connector	Signal
P14	EXCITER OUT
P15	EXCITER FEEDBACK

Table 62 ***Legacy BR Blind Mates - PA***

Connector	Signal
P16	PA FEEDBACK
P17	PA IN
P18	PA RF OUT

Table 63 ***Legacy BR P9 Connector Pin-outs***

Pin No.	Signal
1	GND
2	GND
3	28V
4	28V
5	28V
6	28V
7	28V
8	28V
9	28V
10	28V
11	28V
12	28V
13	28V
14	28V
15	28V
16	14.2V
17	14.2V
18	14.2V
19	14.2V
20	14.2V
21	14.2V
22	14.2V
23	14.2V
24	5V
25	5V
26	5V
27	5V
28	5V
29	5V
30	5V
31	5V

Legacy Single Channel Base Radio Backplane

Table 63 ***Legacy BR P9 Connector Pin-outs (Continued)***

Pin No.	Signal
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	GND
54	SCR_SHUT
55	SCR_THRESH
56	RELAY_ENABLE
57	SHUTDOWN
58	28V_AVG
59	BATT_TEMP
60	SPI_MISO
61	SPI_MOSI
62	SPI_CLK
63	
64	
65	
66	
67	A0(CS1)
68	A1(CS2)

Table 63 ***Legacy BR P9 Connector Pin-outs (Continued)***

Pin No.	Signal
69	A5
70	
71	A4
72	
73	A3
74	GND
75	A2
76	GND
77	GND
78	GND

Legacy Single Channel Base Radio Signals

Table 64 lists and describes the Base Radio signals.

Table 64 ***Legacy Base Radio Signal Descriptions***

Signal Name	Signal Description
GND	Station ground
28V	28VDC
14.2V	14.2VDC
5.1V	5.1 VDC
A0,A1,A2,A3,A4,A5	The BRC uses these lines to address station modules and devices on those modules
SPI_MOSI	Serial Processor Interface - Master out slave in Data
SPI_MISO	Serial Processor Interface - Master in slave out Data
SPI_CLK	Serial Processor Interface - Clock signal (100 KHz - 1 MHz)
AGC1, AGC2, AGC3, AGC4	BRC uses these lines to set the digital attenuator's on the receiver(s) for SGC functionality
2.1MHz_RX	2.1MHz generated on the BRC and used as a reference by the Receiver(s)
2.1MHz_TX	2.1MHz generated on the BRC and used as a reference by the Exciter
DATA1, DATA1*	This differential pair carries receiver 1 data to the Base Radio Controller
DATA2 DATA2*	This differential pair carries receiver 2 data to the Base Radio Controller
DATA3, DATA3*	This differential pair carries receiver 3 data to the Base Radio Controller
ODC_1, ODC_2, ODC_3	Clocks used to clock differential receive data from each respective receiver to the BRC
SBI_1, SBI_2, SBI_3	Serial Bus Interface - These lines are used to program the custom receiver IC on each receiver
SSI, SSI*	Differential transmit data from the Exciter to the BRC
CLK, CLK*	Differential Data clock used to clock transmit data from the BRC to the Exciter
BRCVBLIN	Programmable bias voltage generated on the Exciter and used to bias the Power amplifier devices
VBLIN	Programmable bias voltage generated on the Exciter and used to bias the Power amplifier devices
RESET	Output from BRC to Exciter (currently not used)
EXT_VFWD	DC voltage representing the forward power at the antenna as measured by the external wattmeter
EXT_VREF	DC voltage representing the reflected power at the antenna as measured by the external wattmeter
WP*	Write protect line used by the BRC to write to serial EEPROMs located on each module
BAT_STAT	Binary flag used to signal BRC to monitor the External battery supply alarm

Table 64 ***Legacy Base Radio Signal Descriptions (Continued)***

Signal Name	Signal Description
METER_STAT	Binary flag used by the BRC to indicate to the BRC it should monitor
1PPS	Global Positioning System - 1 pulse per second (this may be combined with 5MHz at the site frequency reference
RCLK	RS-232 - Receive clock
TCLK	RS-232 - Transmit clock
CTS	RS-232 - Clear to send
RTS	RS-232 - Request to send
CD	RS-232 - Carrier detect
RXD	RS-232 - Receive data
TXD	RS-232 - Transmit data
BRG	RS-232 - Baud rate generator
5MHz / Spare	signal currently not used
EXCITER_OUT	Forward transmit path QQAM at approximately a 11dBm level
EXCITER_FEEDBACK	Signal comes from the PA at approximately a 16dBm. Used to close the cartesian RF_LOOP
PA_IN	4 dBm QQAM forward path of the transmitter
PA_FEEDBACK	Signal to the Exciter at approximately 16dBm. Used to close the cartesian RF_LOOP
RX1_IN	RF into Receiver 1
RX2_IN	RF into Receiver 2
RX3_IN	RF into Receiver 3
5MHZ REFERENCE	5MHz station/site reference. Signal comes from the redundant site frequency reference and usually is multiplexed with the 1PPS signal from the global positioning satellite input to the site frequency reference
ETHERNET	Interface between the BRC and the ACG. This connects the Base to the 10 MHz LAN
SCR_SHUT	Signal currently not used
SCR_THRESH	Signal currently not used
RELAY ENABLE	Signal currently not used
SHUTDOWN	Input signal from the BRC to the Power supply. Used to exercise a station “hard start”
28V_AVG	Signal currently not used
BATT_TEMP	DC voltage from the external batteries used to represent the temperature of the batteries. Signal used only with AC power supplies
NOTE: * = enabled low	

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Acronyms

A/D	Analog-to-Digital
A	Amperes
AC	Alternating Current
ACT	active
ADA	Americans with Disabilities Act
AGC	Automatic Gain Control
AIC	Ampere Interrupting Capacity
AIS	Alarm Indication Signal (Keep Alive)
ANSI	American National Standards Institute
ASCII	American National Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
Aux	auxiliary
avg	average
AWG	American Wire Gauge
bd	baud
BDM	Background Debug Mode
BER	Bit Error Rate
BERT	Bit Error Rate Test
BMR	Base Monitor Radio
BNC	Baby "N" Connector
BPV	Bipolar Variation
BR	Base Radio
BRC	Base Radio Controller
BSC	Base Site Controller
BTU	British Thermal Unit
BW	bandwidth
C/N + I	Carrier Power to Noise + Interference Ratio
CC	Control Cabinet
CD	Carrier Detect
cd	change directory
CLK	Clock
CLT	Controller
cm	centimeter
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSMA/CD	Carrier Sense Multiple Access with Collision Detect
CTI	Coaxial Transceiver Interface
CTL	Control (Base Radio Control)
CTS	Clear-to-Send
D/A	Digital-to-Analog
DAP	Dispatch Application Processor
DB-15	15-pin D-subminiature
DB-9	9-pin D-subminiature
dB	Decibel
dBc	Decibels relative to carrier
dBm	Decibels relative to 1mW
DC	Direct Current
DCE	Data Circuit-Terminating Equipment
DCSPLY	DC Supply
DDM	Dual Device Module
deg	degree
DIN	*Deutsche Industrie-Norm*
DIP	Dual In-line Package
div	division

DMA	Direct Memory Access
DOP	Dilution of Precision
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTTA	Duplexed Tower-Top Amplifier
DVM	Digital Volt Meter
E1	European telephone multiplexing standard
EAS	Environmental Alarm System
E-NET	Ethernet
EBTS	Enhanced Base Transceiver System
EGB	Exterior Ground Bar
EIA	Electronics Industry Association
EMI	Electro-Magnetic Interference
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electronically Erasable Programmable Read Only Memory
ERFC	Expansion RF Cabinet
ESI	Ethernet Serial Interface
ESMR	Enhanced Special Mobile Radio
EX	Exciter
FB	feedback
FCC	Federal Communications Commission
FIFO	First-In, First-Out
FNE	Fixed Network Equipment
freq	frequency
FRU	Field Replaceable Unit
Gen 3 SC	Generation 3 Site Controller
GFI	Ground Fault Interrupter
GND	ground
GPS	Global Positioning System
GPSR	Global Positioning System Receiver
HDLC	High-level Data Link
HSMR	High Elevation Specialized Mobile Radio
HSO	High Stability Oscillator
HVAC	Heating/Ventilation/Air Conditioning
Hz	Hertz
I/O	Input/Output
IC	Integrated Circuit
iDEN	integrated Dispatch Enhanced Network
IEEE	Institute of Electrical and Electronic Engineers
IF	intermediate frequency)
iMU	iDen Monitor Unit
in	inches
in	injection
iSC	integrated Site Controller
ISA	Industry Standard Architecture
kg	kilogram
kHz	kiloHertz
LAN	Local Area Network
LANIIC	Local Area Network Interface IC
LAPD	Link Access Procedure D-Channel
lbs	pounds
LDM	Linear Driver Module
LED	Light Emitting Diode
LFM	Linear Final Module
LIU	Line Interface Unit
LLC	Link Layer Controller
LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Loss of Signal
MAU	Media Access Unit
max	maximum
MC	Multicoupler
MGB	Master Ground Bar
MGN	Multi-Grounded Neutral

MHz	MegaHertz
min	minimum
min	minute
MISO	Master In/Slave Out
mm	millimeter
MMI	Man-Machine-Interface
MOSI	Master Out/Slave In
MPM	Multiple Peripheral Module
MPS	Metro Packet Switch
MS	Mobile Station
ms	millisecond
MSC	Mobile Switching Center
MSO	Mobile Switching Office
MST	Modular Screw Terminals
mV	milliVolt
mW	milliWatt
N.C.	Normally Closed
N.O.	Normally Open
NEC	National Electric Code
NIC	Network Interface Card
no.	number
NTM	NIC Transition Module
NTWK	Network
OMC	Operations and Maintenance Center
OSHA	Occupational Safety and Health Act
PA	Power Amplifier
PAL	Programmable Array Logic
PC	Personal Computer
PCCH	Primary Control Channel
PDOP	Position Dilution of Precision
pF	picoFarad
PLL	Phase Locked Loop
P/N	Part Number
P/O	Part Of
ppm	parts per million
PPS	Pulse Per Second
PS	Power Supply
PSTN	Public Switched Telephone Network
PVC	Polyvinyl Chloride
pwr	power
QAM	Quadrature Amplitude Modulation
QRSS	Quasi Random Signal Sequence
Qty	Quantity
R1	Receiver #1
R2	Receiver #2
R3	Receiver #3
RAM	Random Access Memory
RCVR	Receiver
Ref	Reference
RF	Radio Frequency
RFC	RF Cabinet
RFDS	RF Distribution System
RFS	RF System
ROM	Read Only Memory
RPM	Revolutions Per Minute
RSSI	Received Signal Strength Indication
RTN	Return
RU	Rack Unit
Rx	Receive
RXDSP	Receive Digital Signal Processor
SCI	Serial Communications Interface
SCON	VME System Controller
SCRF	Stand-alone Control and RF Cabinet (configuration)
SCSI	Small Computer System Interface
sec	second
SGC	Software Gain Control
SINAD	Signal Plus Noise Plus Distortion to Noise Plus Distortion Radio

SMART	Systems Management Analysis, Research and Test
SPI	Serial Peripheral Interface
SQE	Signal Quality Estimate
SRAM	Static Random Access Memory
SRC	Subrate Controller
SRI	Site Reference Industry standard
SRIB	SMART Radio Interface Box
SRRC	Single Rack, Redundant Controller (configuration)
SRSC	Single Rack, Single Controller (configuration)
SS	Surge Suppressor
SSC	System Status Control
SSI	Synchronous Serial Interface
ST	Status
STAT	Status
Std	Standard
S/W	Software
T1	North american telephone mutiplexing standard
TB	Terminal Board
TDM	Time Division Multiplex
telco	telephone company
SCON	VME System Controller
TISIC	TDMA Infrastructure Support IC
TSI	Time Slot Interface
TSI	Time Slot Interchange
TTA	Tower-Top Amplifier
TTL	Transistor - Transistor Logic
Tx	Transmit
TXD	Transmit Data
TXDSP	Transmit Digital Signal Processor
Txlin	Tranlin IC
typ	typical
UL	Underwriters Laboratories
V	Volts
VAC	Volts - alternating current
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VDC	Volts - direct current
VFWD	Voltage representation of Forward Power
VME	Versa-Module Eurocard
Vp-p	Voltage peak-to-peak
VREF	Voltage representation of Reflected Power
VSWR	Voltage Standing Wave Radio
W	Watt
WDT	Watchdog Timer
WP	Write Protect
WSAPD	Worldwide Systems and Aftermarket Products Division

Parts and Suppliers

This appendix contains recommended part numbers (p/n) and manufacturers for various hardware, tools, and equipment used during installation of the EBTS.

Also contained in this appendix is other installation related information, such as determining types of wire lugs, lengths and sizes of various wires and cables, custom cabling information, and fuses.

All suppliers and model numbers listed are included due to their performance record in previous installations. Motorola cannot guarantee the effectiveness of the installation or performance of the system when using these or other suppliers' parts.

Addresses, phone numbers, fax numbers, websites, and other information is presented for each of the recommended suppliers, when possible.

NOTE

In some listings, phone number and address are for corporate or main sales office. Other sales locations may be available. Call number given or go to website for expanded listings.

Information herein is subject to change without notice.

Surge Arrestors

Two types of surge arrestors should be used in the EBTS site, including:

- ❐ AC Power and Telco
- ❐ Antenna Surge Arrestors

AC Power and Telco Surge Arrestors

The recommended AC Power and Telco surge arrestors are both manufactured by Northern Technologies. The model numbers are:

- AC power - *LAP-B* for 120/240 single-phase
  LAP-C for 208 Vac three-phase
- Telco - *TCS T1DS*

Northern Technologies

23123 E. Mission
Liberty Lake, WA 99019
Phone: 800-727-9119
Fax: 509-927-0435
Internet: http://www.northern-tech.com

Antenna Surge Arrestors

The recommended antenna surge arrestors are manufactured by Polyphaser Inc. The following models are recommended:

- Base Monitor Radio antennas - *ISS50NXXC2MA*
- Base Radio antenna (800 MHz tower top amplifier only) - *094-0801T-A*
- Base Radio antenna (800 MHz cavity combined, transmit only; up to 5 channels) - *IS-CT50HN-MA*
- Base Radio antennas (800 MHz duplexed) - *IS-CT50HN-MA*
- Base Radio antennas (900 MHz duplexed) - 097-0311G-A.2
- GPS antennas - *092-082-0T-A*
- Lightning arrestor bracket kit - *Contact your local Motorola Sales representative to order this kit*
- Receive Tower Top amplifier - *094-0801T-A*
- Tower top test port cable - *IS-50NX-C2*

Polyphaser, Inc.

P.O. Box 9000
Minden, NV 89423-9000
Phone: 800-325-7170
775-782-2511
Fax: 775-782-4476
Internet: http://www.polyphaser.com

Motorola has set up several kits that contain the necessary arrestors with proper mounting hardware for the various antenna configurations. Contact your local Motorola representative for these OEM kits.

RF Attenuators

Several RF attenuators are needed at a site to ensure proper receive adjustments. The attenuators are used at the LNA sites to offset the excess gain from the Tower Top amplifiers, to balance the receive path, and to attenuate the BMR signal path. Use the following specifications when choosing vendors:

- Specified frequency range
  - **800 MHz systems –** requires attenuator specification to include 806-821 MHz range
  - **900 MHz systems –** requires attenuator specification to include 896-901 MHz range
- 1 dB increments
- 0.5 dB accuracy or better
- Female N connector / Male N connector

Alan Industries, Inc.

745 Green Way Drive
P.O. Box 1203
Columbus, IN 47202
Phone: 800-423-5190
812-372-8869
Fax: 812-372-5909

Internet: http://www.alanindustries.com

Huber + Suhner, Inc.

19 Thompson Drive
Essex, VT 05452
Phone: 802-878-0555
Fax: 802-878-9880
Internet: http://www.hubersuhnerinc.com

JFW Industries, Inc.

5134 Commerce Square Drive
Indianapolis, IN 46237
Phone: 877-887-4JFW
317-887-1340
Fax: 317-881-6790

Internet: http://www.jfwindustries.com

Pasternack Enterprises

P.O. Box 16759
Irvine, CA 92623-6759
Phone: 949-261-1920
Fax: 949-261-7451

Internet: http://www.pasternack.com

RF attenuators are also needed for test equipment. The attenuators must be used between frequency reference equipment, service monitors, and the Motorola

EBTS equipment. The following attenuators should be used at the site during optimization:

- ❒ Female BNC connector / Male BNC connector, 10 dB attenuator (1 W) between the Rubidium Standard and the R2660 Communications Analyzer. Refer to the System Testing section.
- ❒ Female BNC connector / Male BNC connector, 30 dB attenuator (1 W) between the Rubidium Standard and the R2660. Refer to the System Testing, section.

Emergency Generator

Several different sizes of generators are available. Determine the loading requirements of the site prior to ordering a generator. A recommended manufacturer of the emergency backup generator power system is:

Generac Corporation

P.O. Box 8
Waukesha, WI 53187
Phone: 262-544-4811
Fax: 262-544-0770

Portable Generator Connection

The recommended portable generator connection is the *AJA200-34200RS*, manufactured by Appleton Electric. Figure 1 is a view of a connector located on the building. An adapter may be required if local electrical standards conflict with the wiring configuration.

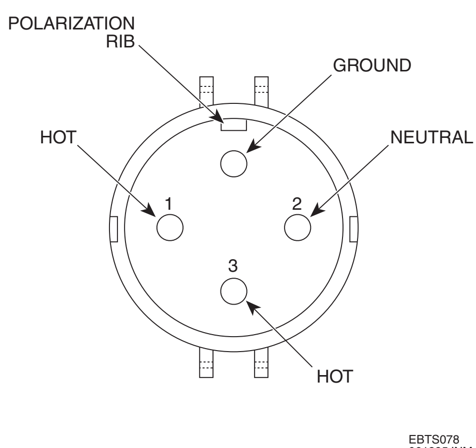

Figure 1 **Portable Generator Connector**

An alternate supplier of the portable generator connection is the *ARKTITE Heavy Duty Receptacle Model 80, Style 2, 200 Amps*, manufactured by Crouse-Hinds.

Cooper Industries
Crouse-Hinds, Inc.

P.O. Box 4999
Syracuse, NY 13221
Phone: 315-477-5531
Fax: 315-477-5719

Internet: http://www.crouse-hinds.com

GPS Evaluation Kit

The Motorola GPS evaluation kit (Motorola part number DQGTEVAL0002) is available from Synergy Systems.

Synergy Systems

P.O. Box 262250
San Diego, CA 92196
Phone: 858-566-0666

Internet: http://www.synergy-gps.com

GPS Antenna Amplifier

There are two recommended manufacturers of the GPS antenna amplifiers.

❒ LA20RPDC-N (GPS Networking)

❒ LA-21-L1/L2 (Starlink, Inc.)

GPS Networking

710A West 4th St.
Pueblo, CO 81003
Phone: 800-463-3063
719-595-9880
Fax: 719-595-9890
Internet: http://www.gpsnetworking.com

Starlink Inc.

6400 Highway 290 East
Suite 202
Austin, TX 78723
Phone: 512 454-5511
800 460-2167
Fax: 512 454-5570
Internet: http://www.starlinkdgps.com

Specifications	Type 1	Type 2
Dimensions	3.293″ x 2″ x 1″	0.6″ Dia. x Approx. 3.8″
Connectors	Type N female, both ends	Type N female, both ends
Gain	23 dB gain typical 20 dB min.	20 dB ± 3 dB
Noise Figure	2.6 dB typical	<3.0 dB
VSWR	< 2.2:1	Not Specified
Frequency Range	1575.42 ± 50 MHz	L1/L2
Filtering	Yes	Yes
Maximum Input Power	+ 13 dBm	Not Specified
Voltage	4.5 - 15 VDC	3 - 28 VDC
Current @ 5 V	< 15 mA @ 5V typical	8mA @ 3V

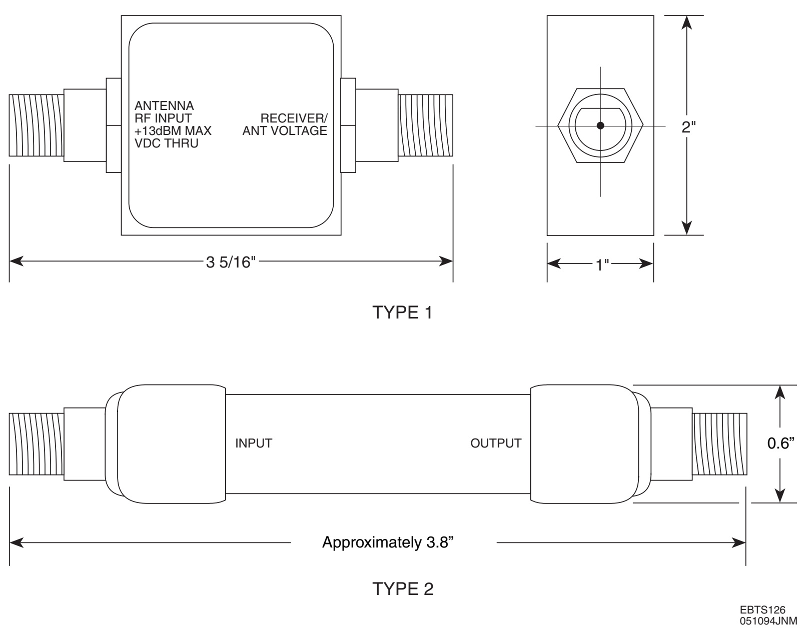

Figure 2 ***GPS Antenna Amplifiers***

Site Alarms

Three types of alarms should be used in an EBTS site, including:

- Intrusion Alarm
- Smoke Alarm
- Temperature Alarm

Intrusion Alarm

The intrusion alarm is the *Sonitrol Door contact 29A*.

Sonitrol

211 N. Union Street, Suite 350
Alexandria, VA 22314
Phone: 800-326-7475
703-684-6606
Fax: 703-684-6612
Internet: http://www.sonitrol.com

Smoke Alarm

An available smoke alarm is the *Sentrol 320CC*. This smoke alarm provides a relay closure for the iMU alarm. These smoke detectors are available from many electrical wholesale distributors. For the location nearest you, call between 6 a.m. and 5 p.m. Pacific Standard Time and ask Sales for the location of the nearest EW (Electric Wholesale) distributor.

Sentrol, Inc.
GE Interlogix

12345 SW Leveton Drive
Tualatin, OR 97062
Phone: 800-547-2556
503-692-4052
Internet: http://www.sentrol.com

Temperature Alarm

The recommended temperature alarm is the *Grainger #2E206* thermostat. This alarm is manufactured by Dayton Electronics and distributed by W.W. Grainger:

W.W. Grainger

Locations Nationwide

Phone: 888-361-8649
Internet: http://www.grainger.com

Cabinet Mounting Hardware

The cabinet mounting hardware is site dependent and must be procured locally.

Equipment Cabinets

The mounting hardware used to secure the Equipment Cabinets containing control and/or RF hardware must be able to provide 1545 pounds of retention force.

- ❐ If the cabinets are to be secured to a concrete floor, 1/2" grade 8 bolts with anchors are recommended.
- ❐ If the cabinets are to be secured to another type of floor, determine the appropriate mounting hardware.

Power Supply Rack

The Motorola offered Power Supply rack from Power Conversion Products is available in a standard and an earthquake rack.

Power Conversion Products, Inc.

115 Erick Street
Crystal Lake, IL 60039-0380
Phone: 800-435-4872 (customer service)
815-479-0682
Fax: 815-459-0453
Internet: http://www.eltekenergy.com

If the earthquake rack is used, it must be bolted to the floor using the *02100-13 High Performance Anchor Kit*, consisting of:

- ❐ anchors (qty. 4)
- ❐ load sharing plates (qty. 2)
- ❐ large square washers (qty. 8)

Hendry Telephone Products

55 Castilian Drive
Santa Barbara, CA 93117-3080
Phone: 805-968-5511
Fax: 805-968-9561
Internet: http://www.hendry.com

Cable Connections

The recommended manufacturer for all wire lugs used during EBTS installation is Thomas & Betts. All wire lug part numbers listed are for Thomas & Betts.

Thomas & Betts

8155 T&B Boulevard
Memphis, TN 38125
Phone: 800-888-0211 (general information)
800-248-7774 (sales/technical support)
Internet: http://www.tnb.com

NOTE

Double hole wire lugs are preferred, but single hole wire lugs can be used where mounting requirements dictate their use.

Selecting Master Ground Bar Lugs

Table 1 identifies recommended part numbers for wire lugs used to connect chassis ground wiring to the master ground bar from each cabinet.

Table 1 ***Recommended Master Ground Bar Lugs***

Wire Size	Wire Type	Lug Color	Description	P/N †
#2 AWG	Stranded	Brown	Single 1/4" diameter hole	54107
#2 AWG	Stranded	Brown	Double 1/4" diameter hole, 5/8" center	54207
#6 AWG	Stranded	Blue	Single 1/4" diameter hole	54105
#6 AWG	Stranded	Blue	Double 1/4" diameter hole, 5/8" center	54205
NOTE: These lugs require the use of the TBM5-S crimping tool. † All part numbers are Thomas & Betts.				

Selecting Cabinet Ground Lugs

Table 2 identifies recommended part numbers for wire lugs used to connect chassis ground wiring to the grounding point of each cabinet.

Table 2 ***Recommended Junction Panel Ground Lugs***

Wire Size	Wire Type	Lug Color	Description	P/N †
#2 AWG	Stranded	Brown	Single 1/2" diameter hole	54145
#6 AWG	Stranded	Blue	Single 3/8" diameter hole	E6-12
NOTE: These lugs require the use of the TBM5-S crimping tool. † All part numbers are Thomas & Betts.				

Battery System Connections

The cable loop length refers to the total length of wire within a given circuit. For example, the combined length of the -48 VDC (hot) lead and the DC return lead equals the cable loop length. This would mean that a cabinet that needs 16 feet of wire between the batteries and Power Supply Rack has a total loop length of 32 feet.

Determining Battery System Wire Size

The wire size for the connection between the batteries and the Power Supply Rack is determined by the required wire length and the maximum allowable voltage drop. The voltage drop in the loop must be kept to below 200 mV. The wire selected should be UL approved and contain a high number of strands for flexibility.

For a standard configuration, the Power Supply rack is located directly adjacent to the batteries with a cable loop length of 20 feet or less, which requires the use of a 4/0 wire. Table 3 shows recommended wire sizes for various loop lengths. Larger wire sizes may be used if the recommended sizes are not available. The recommended wire sizes are large enough to allow site expansion to a fully loaded site.

Table 3 **Battery System Wire Size**

Loop Length	Wire size
20 feet	4/0 (or 250 MCM)
30 feet	350 MCM
45 feet	500 MCM

Selecting Battery System Lugs

Depending on the wire size used and the manufacturer of the Batteries, different wire lugs are crimped onto the power cable ends. After the wire size has been determined from Table 3, verify the manufacturer of the Batteries (*Dynasty or Absolyte*).

Two different battery systems are offered with the EBTS. The *Dynasty* system is a low to medium capacity, field expandable system supplied for smaller sites or sites with minimal backup hour requirements. This system is custom designed to Motorola specifications. The *Dynasty* system is manufactured by Johnson Controls:

C & D Technologies
Dynasty Division

900 East Keefe Avenue
P.O. Box 591
Milwaukee, WI 53212
Phone: 800-396-2789
414-967-6500
Fax: 414-961-6506
Internet: www.dynastybattery.com

The *Absolute IIP* battery system is a heavy duty, high capacity battery system manufactured by GNB Technologies:

GNB Technologies

829 Parkview Boulevard
Lombard, IL 60148
Phone: 630-629-5200
Fax: 630-629-2635
Internet: www.gnb.com/stationary/stat-absp.html

Refer to Table 4 to determine the proper wire lug for the connection of that wire to the Power Supply rack.

Table 4 ***Power Supply Rack Connection Lugs***

Wire Size	Cabinet Lug	Crimp Tool	Lug P/N †
4/0	Double 3/8" hole, 1" center	TBM5-S	54212
250 MCM	Double 3/8" hole, 1" center	TBM8-S	54213
350 MCM	Double 3/8" hole, 1" center	TBM8-S	54215
500 MCM	Double 3/8" hole, 1" center	TBM8-S	54218
† All part numbers are Thomas & Betts.			

Refer to Table 5 to determine the proper wire lug for the connection to the batteries, based on the wire size and battery manufacturer. One column lists the selection for *Dynasty* and the other lists the selection for *Absolyte IIP*.

Table 5 ***Battery Connection Lugs***

Wire Size	Lug Color	Dynasty		Absolyte IIP	
		Description	P/N	Description	P/N
4/0	Purple	Double 3/8" hole, 1" center	54212	Single 1/2" hole	54170
250 MCM	Yellow	Double 3/8" hole, 1" center	54215	Single 1/2" hole	54113
350 MCM	Red	Double 3/8" hole, 1" center	54218	Single 1/2" hole	54115
500 MCM	Brown	Double 3/8" hole, 1" center	54220	Single 5/8" hole	54118

Anti-Oxidant Greases

Any one of the following anti-oxidant greases are recommended for connections to the positive (+) and negative (-) terminals of the batteries:

- ❒ No-Ox
- ❒ OxGuard
- ❒ Penetrox

Intercabinet Cabling

Ethernet and alarm cables connecting to the junction panels of each cabinet are supplied with the system. These cables may not be suitable for every EBTS site. It may be necessary to locally manufacture cables for a custom fit. Information is provided for both supplied cables and custom cables.

Supplied Cables

The cables listed in Table 6 are supplied with the system. The length of these cables should be sufficient if the considerations outlined in the Pre-Installation section are followed.

Table 6 ***Supplied Inter-Cabinet Cabling***

Description	Qty.	P/N †
120" long, N-type Male to N-type male cable	3	0112004B24
108" long, BNC Male-to-BNC Male, RG400 cable	2*	0112004Z29
210" long, 8-pin Modular plug cable	1*	3084225N42
186" long, PCCH redundancy control cable	1**	3082070X01
Phasing Harness	1	0182004W04

† All part numbers are Motorola.
* Per RF rack.
** Per Control rack.

Making Custom Cables

If custom Ethernet or 5 MHz cables must be locally manufactured, use the part numbers listed in Table 7 for ordering the required materials.

Table 7 ***Parts for Ethernet and 5 MHz Cables***

Description	Qty.	P/N †
Connector, BNC male	As required	2884967D01
Cable, RG400	As required	3084173E01

† All part numbers are Motorola.

Table 8 lists the part numbers for custom alarm cables.

Table 8 ***Parts for Alarm Cables***

Description	Qty.	P/N †
Connector, 8-pin modular	As required	2882349V01
Cable, 8-wire	As required	Locally procured
† All part numbers are Motorola.		

Table 9 lists the part numbers for custom PCCH cables.

Table 9 ***Parts for Extending PCCH Redundancy Control Cables***

Description	Qty.	P/N †
186″ long, PCCH redundancy control cable	1*	3082070X01
8-pin male Telco to 8-pin male Telco extension cable, length: as needed	As required	Locally procured
Modular, 8-pin female-to-female adaptor	As required	Locally procured
NOTE: Motorola does not guarantee proper operation of system if longer PCCH cable is used. † All part numbers are Motorola. * Per Control rack.		

Equipment Cabinet Power Connections

Selecting Power Connection Lugs

Table 10 identifies recommended part numbers for lugs used for power connections between the Power Supply rack and the Control and RF Cabinets. The maximum wire size accepted by the Control and RF Cabinets is 2/0. The Control and RF Cabinets use screw type compression connectors and do not require lugs.

Table 10 ***Recommended Power Connection Lugs for Power Supply Rack***

Size	Lug Color	Description	P/N †
2/0	Black	Double 3/8″ hole, 1″ center	54210
#2 AWG	Brown	Double 1/4″ hole, 5/8″ center	54207
#4 AWG	Gray	Double 1/4″ hole, 5/8″ center	54206
#6 AWG	Blue	Double 1/4″ hole, 5/8″ center	54205
† All part numbers are Thomas & Betts.			

Determining Power Connection Wire Size

The cable loop length refers to the total length of wire within a given circuit. For example, the combined length of the -48 VDC (hot) lead and the DC return lead equals the cable loop length. This would mean that a cabinet which needs 16 feet of wire between the Power Supply rack and equipment cabinets has a total loop length of 32 feet.

The wire size for the connection between the Power Supply rack and the equipment cabinets is determined by the required wire length and the maximum allowable voltage drop. The voltage drop in the loop must be kept to below 500 mV. The wire selected should be UL approved and contain a high number of strands for flexibility. Table 11 shows the recommended wire sizes for various loop lengths of the RF Cabinet. Table shows the recommended wire sizes for loop lengths of the Control Cabinet

For a standard configuration, the equipment cabinets are located adjacent to the Power Supply rack with a cable loop length less than 35'.

Table 11 ***Power Connection Wire Size***

Loop Length	Wire Size
25 feet or less	#6 AWG
25 to 40 feet	#4 AWG
40 to 60 feet	#2 AWG
60 to 130 feet	1/0 AWG
NOTE: The wire sizes listed are large enough to allow full RF Cabinet Base Radio capacity.	

Table 12 ***Power Connection Wire Size for Control Cabinet***

Loop Length	Wire Size
150 feet or less	#6 AWG

Each equipment cabinet has a total of four Power Supply Rack connections; two -48 VDC (hot) and two DC return. Each equipment cabinet contains two separate power distribution systems. A single hot wire and a single return wire are used for each side of the bus. Two return leads provide redundancy and allow a uniform wire size to be used for all 48 VDC power distribution system connections.

Other Recommended Suppliers

The following are the addresses of various suppliers for tools and equipment used during installation of the EBTS.

Test Equipment

- ❐ PRFS Rubidium Frequency Standard

  Datum Inc.

  3 Parker
  Irvine, CA 92618-1605
  Phone: 800-EFRATOM (337-2866)
  949-590-7600
  Fax: 949-598-7650
  Internet: http://www.datum.com

- ❐ Fluke 77 Digital Multimeter

  Fluke Corporation

  P.O. Box 9090
  Everett, WA 98206-9090
  Phone: 800-44-FLUKE
  425-347-6100
  Fax: 425-356-5116
  Internet: http://www.fluke.com

Drive Test Equipment

A PC can be used for EBTS optimization and field service. The following are the minimum requirements:

- ❐ 19,200 bps serial port
- ❐ one floppy drive
- ❐ communication software, such as Smartcomm II or Procomm Plus

A drive test application is only available for the PC platform and is currently called iFTA (iDEN Field Test Application). Contact your local Motorola sales representative for more information.

Software

- ❒ ProComm Plus software

  Symantec Corporation

  20330 Stevens Creek Blvd.
  Cupertino, CA 95014
  Phone: 408-517-8000
  Internet: http://www.symantec.com

Spare Parts Ordering

Motorola Inc.

Accessories and Aftermarket Division

Attn: Order Processing

1307 E. Algonquin Road
Schaumburg, IL 60196

Returns:
2222 Glavin Drive
Elgin, IL 60123

Phone: 800-422-4210 (sales/technical support)
Fax: 847-538-8198

Newark Electronics

Call for a local phone number in your area to order parts

Phone: 800-463-9275 (catalog sales)
773-784-5100
Fax: 847-310-0275
Internet: http://www.newark.com

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