1A-RDS SIGNAL MONITOR TEST SET
DESCRIPTION, OPERATION, AND MAINTENANCE
TRANSMISSION TEST EQUIPMENT

CONTENTS — PAGE

1. GENERAL

1.01 This section describes the 1A-RDS Signal Monitor Test Set and provides information for its operation and maintenance. The test set is used to assist in trouble isolation of the 1A Radio Digital System (1A-RDS).

1.02 When this section is reissued, the reason for reissue will appear in this paragraph.

1.03 The 1A-RDS Signal Monitor Test Set enables monitoring for partial response violation (PRVed) seconds (see paragraph 1.09) at points on a 1A-RDS route other than terminal bay locations.

1.04 The test set, shown in Fig. 1, consists of two units, a J68435AF IF and Baseband Unit and a J68435AG Receiving Digital Processor unit. Information in this section is limited to these units.

1.05 Input signals to the test set can be at either intermediate (IF) or baseband (BB) frequencies. An IF amplifier is provided as a part of the IF and Baseband unit to allow access at low-level IF points within a switching section. A frequency modulation receiver (FMR) is also included to convert the IF signals to baseband frequencies.

1.06 A 124-ohm balanced to 75-ohm unbalanced transformer (TRANSF) allows access to 7-level signal monitor points at baseband.

1.07 The output of the FMR or the transformer is a composite signal consisting of the 7-level partial encoded data signal, the 386-kHz pilot, and the analog message band.

1.08 The IF and Baseband portion of the test set filters out all but the 1A-RDS frequency spectrum (0 to 386 kHz), equalizes the signal for amplitude and delay, and applies it to the digital processor unit.

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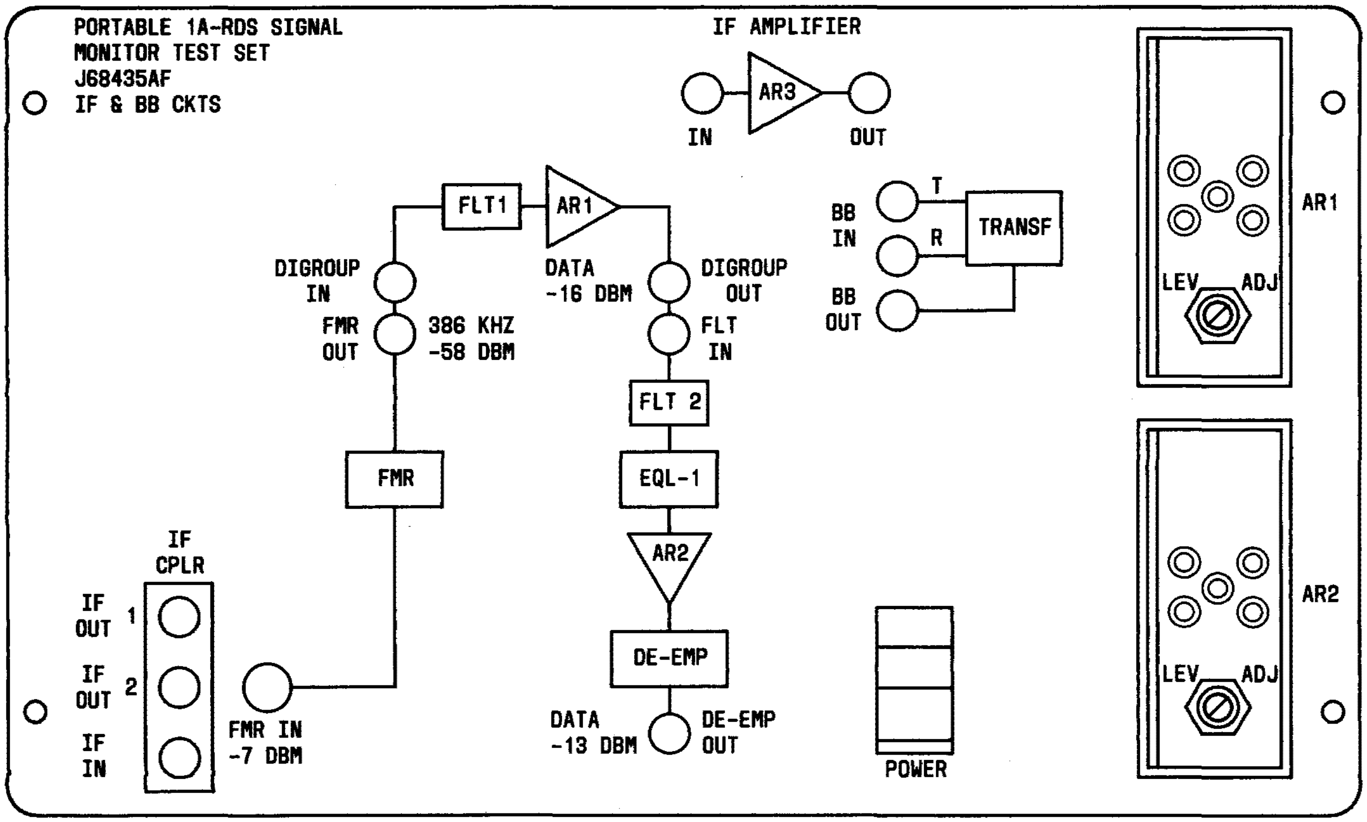
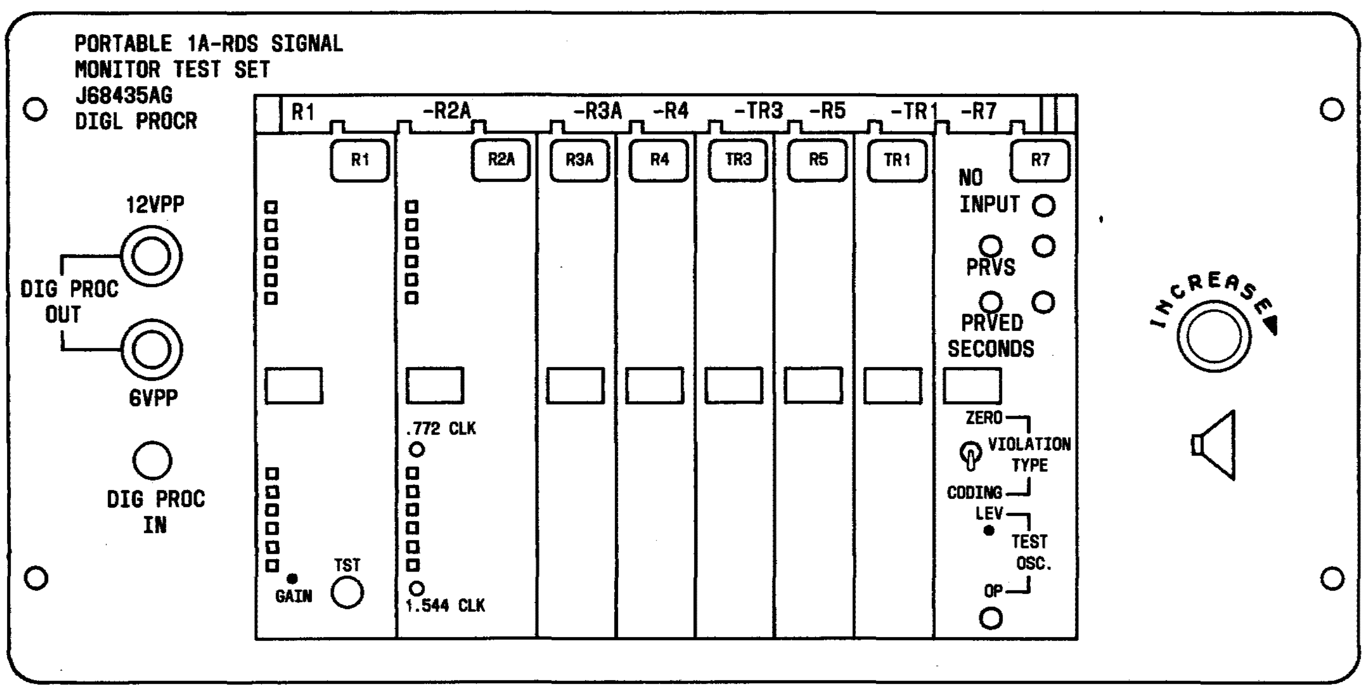


A - FRONT VIEW J68435AF IF AND BASEBAND UNIT (NEW VERSION WITH INTERNAL IF AMPLIFIER)



B - FRONT VIEW J68435AG RECEIVING DIGITAL PROCESSOR UNIT

Fig. 1—1A-RDS Signal Monitor Test Set

1.09 The receiving digital processor monitors the 7-level signal for violations in the partial response encoded signal (PRVs) and translates the PRVs into PRVed seconds. A PRV is a violation in the 7-level signal caused by a disturbance such as baseband switching, IF switching, etc. A PRVed second is a second that contains one or more PRVs.

1.10 The 7-level signal is translated into a DS-1 signal format and appears at the DIG PROC OUT jacks so the DS-1 signal is available for external use.

2. EQUIPMENT DESCRIPTION

A. General

2.01 The J68435AG Digital Processor unit weighs approximately 30 pounds. Both units of the test set are approximately 10 × 14 × 22 inches. The J68435AF IF and Baseband unit houses the power supplies for both units and weighs approximately 47 pounds. Both units are contained in cases designed for durability and portability. The cases have front and rear covers that must be removed during operation.

2.02 Table A is a list of jacks, controls, and indicators of the J68435AF IF and Baseband unit and their function. Table B is a list of jacks, controls, and indicators of the J68435AG Digital Processor unit and their function.

2.03 Three cable assemblies are provided as part of the test set. One of the cables provides ac power to the IF and Baseband unit. Another cable connects between the two units to provide dc power to the receiving digital processor. A third cable provides a 75-ohm unbalanced signal connection between the faceplates of the two units.

2.04 The test set can be used at three points: 7-level signal monitor points, IF signal at radio repeater sites, and IF monitor points.

B. J68435AF IF and Baseband Unit—Functional

2.05 A simplified block diagram of the AF unit is shown in Fig. 2.

2.06 The TRANSF provides access for monitoring the 7-level signal. It converts the 124-ohm balanced signal at **BB IN** to a 75-ohm unbalanced signal at **BB OUT**. The signal loss from **BB IN** to **BB OUT** is approximately 0.2 dB. The output is patched to the **DIGROUP IN** jack when the TRANSF is used.

2.07 The IF coupler (CPLR) enables IF signals to be accessed at radio repeater sites. The thru loss between **IF IN** and **IF OUT1** is approximately 0.2 dB. The thru loss between **IF IN** and **IF OUT2** is approximately 18.0 dB.

2.08 The IF amplifier (AR3) allows bridging low-level IF monitor points at radio main stations. The IF amplifier has a fixed gain of 26.0 dB.

2.09 The FM receiver (FMR) accepts a 70 or 74.1 MHz IF signal and produces a baseband spectrum which can be processed further in the baseband circuits. A 20-dB pad (not shown) between the FMR and the **FMR OUT** jack provides a level control point for the 1A-RDS pilot signal so that a pilot of −58 dBm can be observed.

2.10 The low-pass filter (LPF-1) and amplifier (AR1) act as a terminal digroup connector. The LPF-1 has a nominal insertion loss of 0.15 dB ± 0.1 dB from 300 Hz to 500 kHz and provides high loss to any analog message signal above 564 kHz. Amplifier AR1 is a 75-ohm redundant amplifier that provides adjustable gain between 20 and 30 dB. The amplifier output level is adjusted by a front panel potentiometer designated **LEV ADJ**.

2.11 Another 75-ohm unbalanced low-pass filter (LPF-2 in Fig. 2) provides wave shaping and passes the 0 to 386 kHz band and adds 65.0 dB of attenuation to frequencies above 500 kHz.

2.12 A 75-ohm unbalanced delay equalizer (EQL-1) equalizes the delay distortion introduced by LPF-2. The combined loss to the data signal through LPF-2 and EQL-1 is approximately 1.0 dB.

2.13 Amplifier AR2 is a 75-ohm redundant line amplifier that provides adjustable gain between 20 and 30 dB. The output level of the amplifier is adjusted by a front panel potentiometer designated **LEV ADJ**.

2.14 The de-emphasis network (DE-EMP) is a complement of the pre-emphasis network in the transmitting access panel. The network reduces the pulse response time constant caused by frequency modulation (FM) terminal switching. The network

TABLE A

J68435AF IF AND BASEBAND UNIT — JACKS, CONTROLS, AND INDICATORS

DESIGNATION	FUNCTION
BB IN	124-ohm balanced input to the transformer (TRANSF).
BB OUT	75-ohm unbalanced output of the transformer (TRANSF).
IF IN	75 ohm unbalanced input to the IF coupler.
IF OUT 1	75-ohm unbalanced low loss output of the coupler through path (.2 dB loss)
IF OUT 2	75 ohm unbalanced drop leg of the coupler (18 dB loss).
FMR IN	75-ohm unbalanced input to the FMR (-7 dBm input).
FMR OUT	75-ohm unbalanced output of FMR normally through to DIGROUP IN. Data level normally -40 dBm.
DIGROUP IN	75-ohm unbalanced input to the terminal digroups. Normally through to FMR OUT jack.
DIGROUP OUT	75-ohm unbalanced output of the terminal digroups. Normally through to FLT IN jack.
FLT IN	The 75-ohm unbalanced input to the access circuits (low-pass filter, pads, delay equalizer, AR2 and de-emphasis network). Normal through to DIGROUP OUT.
DE-EMP OUT	75-ohm unbalanced output of the receive access circuits
LEV ADJ (2)	Gain adjustment for output levels of amplifier AR1 and AR2
IF AMPLIFIER IN	Input to 26 dB fixed gain IF amplifier
IF AMPLIFIER OUT	Output of 26 dB fixed gain IF amplifier
POWER	Rocker style illuminated power switch, illuminated when on.
DC POWER CORD	Used to provide DC power from the J68435AF unit to the J68435AG unit.
AC POWER CORD	Located behind rear cover.

also removes the amplitude shaping performed on the low and high frequency ends. This improves signal-to-noise (S/N) ratio throughout the data band. The de-emphasis network introduces approximately 5.6 dB loss to the data signal.

C. J68435AG Receiving Digital Processor Unit—Functional

2.15 A simplified block diagram of the J68435AG Receiving Digital Processor unit is shown in Fig. 3.

2.16 The 7-level signal from the J68435AF IF and Baseband unit enters the receiving digital processor unit via the automatic gain control (AGC) amplifier. The AGC amplifier amplifies and level stabilizes the signal and splits the signal into two

TABLE B

J68435AG RECEIVING DIGITAL PROCESSOR UNIT — JACKS, CONTROLS, AND INDICATORS

DESIGNATION	FUNCTION
GAIN	Control on AGC AMPL circuit pack R1 used to adjust output level of amplifier.
TST	Jack access to AGC AMPL circuits used to measure AGC AMPL output level and during noise margin tests to insert a 10-kHz tone.
.722 CLK	Control on CLOCK RECOVERY circuit pack R2A to adjust the phase of the strobe sampling the 7-level signal.
1.544 CLK	Control on CLOCK RECOVERY circuit pack R2A to adjust gating of the full-rate information in proper phase relative to the .772 clock.
VIOLATION TYPE	Switch on MON & TST OSC circuit pack R7 used to select type of violation to be monitored. Two positions: CODING and ZERO.
TEST OSC LEV	Control on MON & TST OSC circuit pack R7 to adjust output level of 10 kHz oscillator from approximately -20 to +14 dBm.
TEST OSC OP	Jack on MON OSC circuit pack R7 used to access the 10-kHz signal.
NO INPUT	LED on the MON & TST OSC circuit pack R7 illuminates to indicate loss of data signal input.
PRVS	LED on the MON & OSC circuit pack R7 flashes each time that a PRV is detected.
PRVED SECONDS	LED on the MON & TST OSC circuit pack R7 flashes for each occurrence of a PRVed second even though many PRVs may have occurred during the one second interval.
PRVS	Jack on the MON & OSC circuit pack R7 used to connect external test equipment for counting the number of PRVs occurring.
PRVED SECONDS	Jack on the MON & OSC circuit pack R7 used to connect external test equipment for counting the number of PRVed seconds over an extended period.
DIG PROC IN	The input jack to the receiving processor AGC amplifier.
DIG PROC OUT	Output jack for 12-Vpp and 6-Vpp, 50-percent duty cycle, bipolar DS-1 signal of the original transmitted data for balanced transmission. Accepts 310-type telephone plugs.
POWER IN	A multi-pin connector plug to provide DC power and ground to the digital processor.
BAY GRD	A 3-foot cord with alligator clip to be attached to a bay ground.

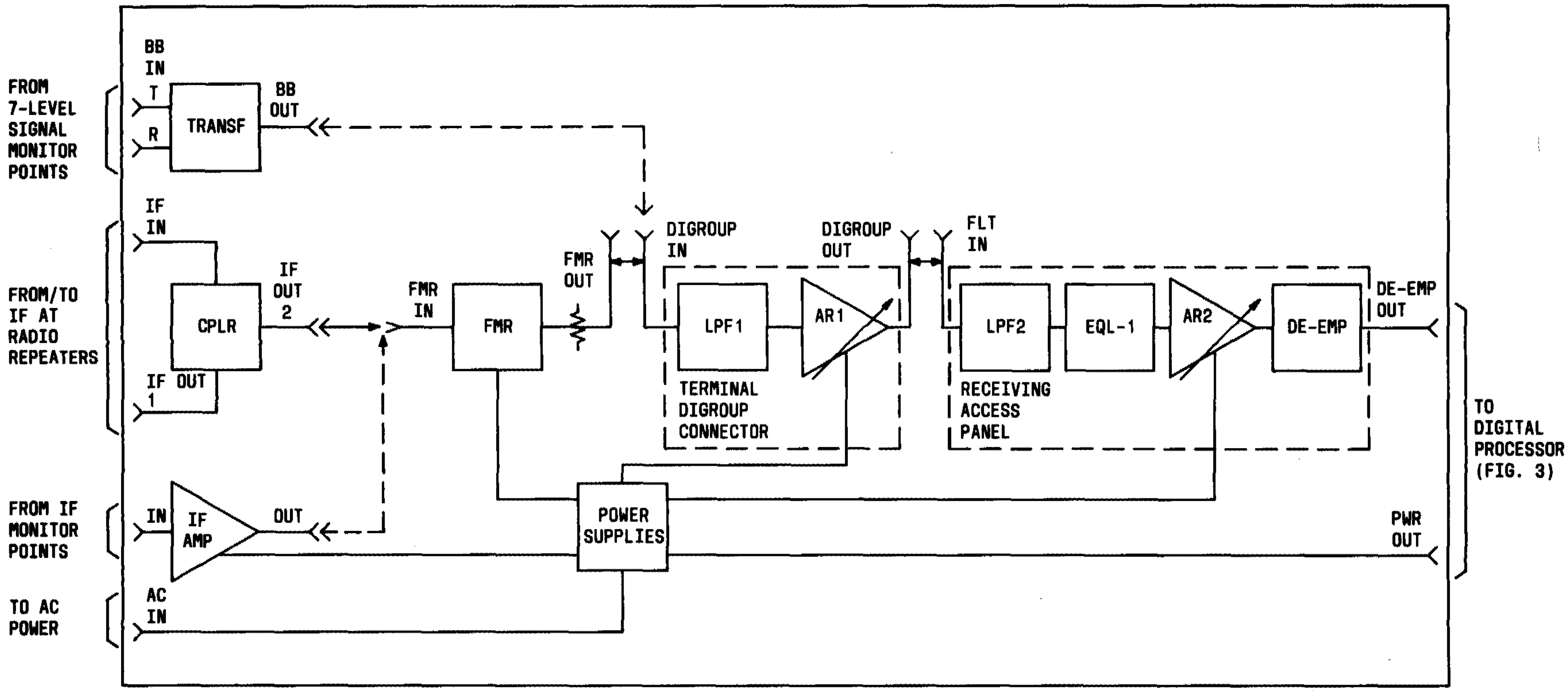


Fig. 2 —Simplified Block Diagram—J68435AF IF and Baseband Unit

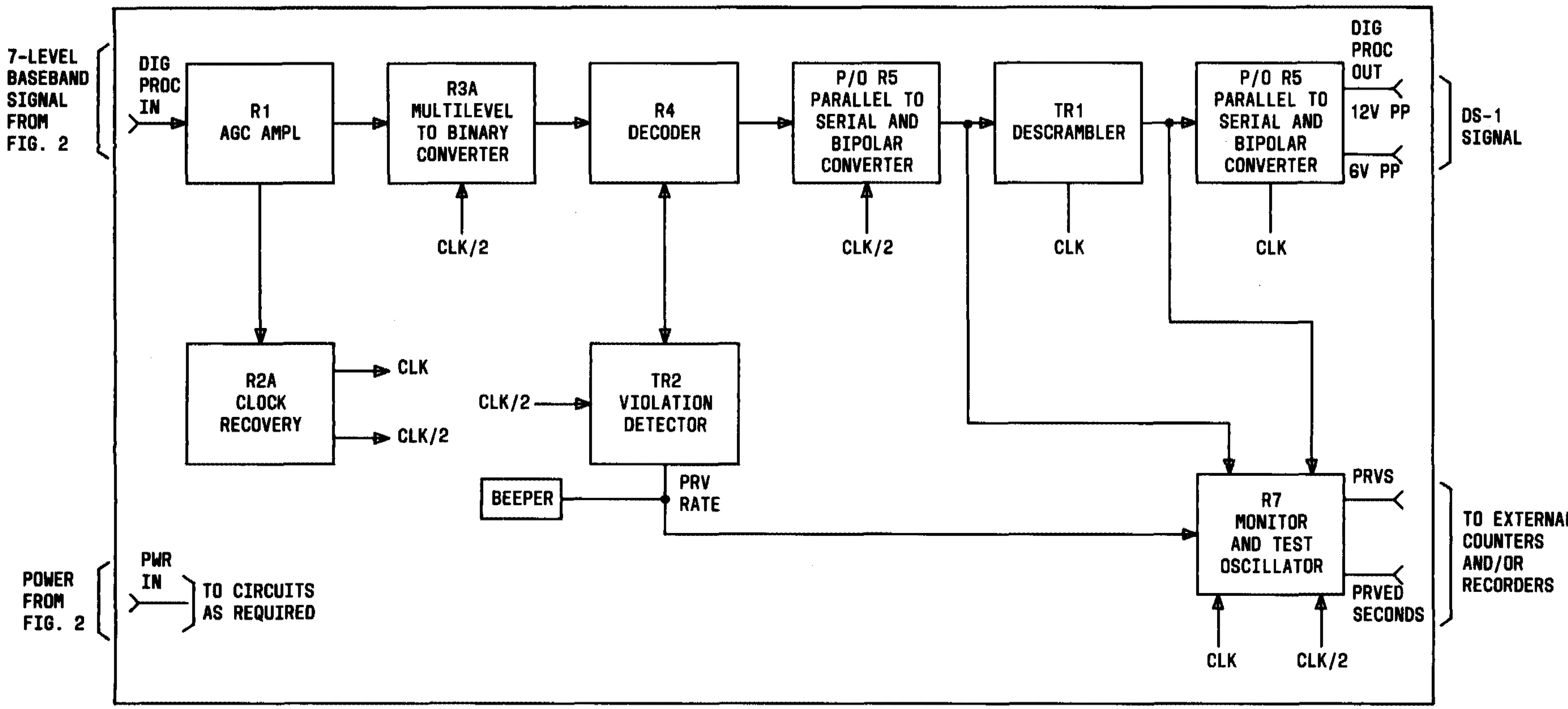


Fig. 3 —Simplified Block Diagram—J68435AG Digital Processor Unit

paths. The nominal input to the AGC amplifier is −13.0 dBm measured at the **DIG PROC IN** jack. The AGC amplifier **GAIN** control provides automatic gain control of approximately 15 dB (between −10 and +5 dB) about the nominal input level of −13.0 dBm.

2.17 The AGC amplifier (R1) has two outputs. The output to the R3A multilevel-to-binary converter has the 386-kHz pilot removed by a filter in the AGC amplifier; thus only the 7-level signal enters the R3A converter circuit. Each of the seven levels is detected by threshold circuits and converted into six data streams. These six data streams are translated into two parallel streams by the decoder (R4) for further processing.

2.18 The 386-kHz pilot is passed by a bandpass filter, amplified, and applied to the phase locked clock recovery circuit (R2A). This is the composite signal and contains both the 7-level signal and the 386-kHz pilot. The R2A clock recovery circuit controls the output phase of the clocks to the receiving circuits. The R2A circuit has front panel adjustments for full-rate (1.544 CLK) and half-rate (.772 CLK) clock pulses.

2.19 The six data streams from the R3A mutilevel-to-binary converter are translated into two parallel streams of information by the R4 decoder circuit. The decoder generates two additional streams of correlated information for verification purposes by the violation detector circuit (TR2).

2.20 The parallel data streams enter the parallel-to-serial converter (part of R5) where they are combined into a single unipolar data stream at a 1.544 Mb/s, 100 percent duty cycle rate. This scrambled signal is fed to a descrambler (TR1) that converts it into an output which is the unipolar representation of the transmitted 1.544 Mb/s data signal.

2.21 The unipolar signal is fed to the bipolar converter circuit (part of R5) where it is translated back into the original DS-1 1.544 Mb/s, 50 percent duty cycle, bipolar data signal.

2.22 The monitor and test oscillator (R7) allows in-service monitoring and initial or routine alignment of the receiving digital processor unit. The inputs to the R7 are the outputs of the violation detector circuit (TR2) and the descrambler circuit (TR1). The R7 translates input violations into external outputs for recording individual PRVs and PRVed seconds. Both PRVs and PRVed seconds outputs are intended to drive external high impedance monitoring equipment.

2.23 A beeper provides an audible indication when a PRV occurs in the 7-level encoded signal. The beeper source is the PRV RATE signal from the violation detector. The beeper will alarm approximatley one-half second when a single PRV occurs. If the PRV RATE is high, the beeper will be on continuously.

3. OPERATION

A. General

3.01 Part 3C is an alignment procedure to assist in pre-service alignment of the test set. This procedure ***must*** be performed each time the test set is used. Figure 4 shows the various signals and locations that may be accessed in a 1A-RDS system. Table C is a list of possible error sources in the 1A-RDS system and can be used for trouble location.

3.02 A PRV is a level violation that has been introduced into the 7-level signal. The receiving digital processor determines PRVS based on previously received levels. One or more PRVs falling within 1 second will result in 1 PRVed second. PRVed seconds is a count at the 1.544 Mb/s rate of every second in which one or more PRVs occurs.

B. Pre-service Alignment

3.03 The alignment procedure in Part 3C ***must*** be performed each time the test set is used. The following test equipment is required:

Fluke 8920A TRUE RMS Voltmeter or Hewlett-Packard 3400A RMS Voltmeter. See Note.

Termination plug (100-ohm, KS-20616 on a 310 plug)

57A Attenuator

75-ohm unbalanced cable

Cable 840956494 (WECo. 440 plug on one end and one BNC male on the other end)

Tektronix Oscilloscope 465B or Hewlett-Packard 182C

W1BG Cord

Note: When using the FLUKE 8920A, the following is required:

Feed-thru termination TEKTRONIX 011-0055-00

When using the HP 3400A, the following items are required:

BNC T Adapter coded 31208 Amphenol

75-ohm terminating plug coded 46650 Amphenol.

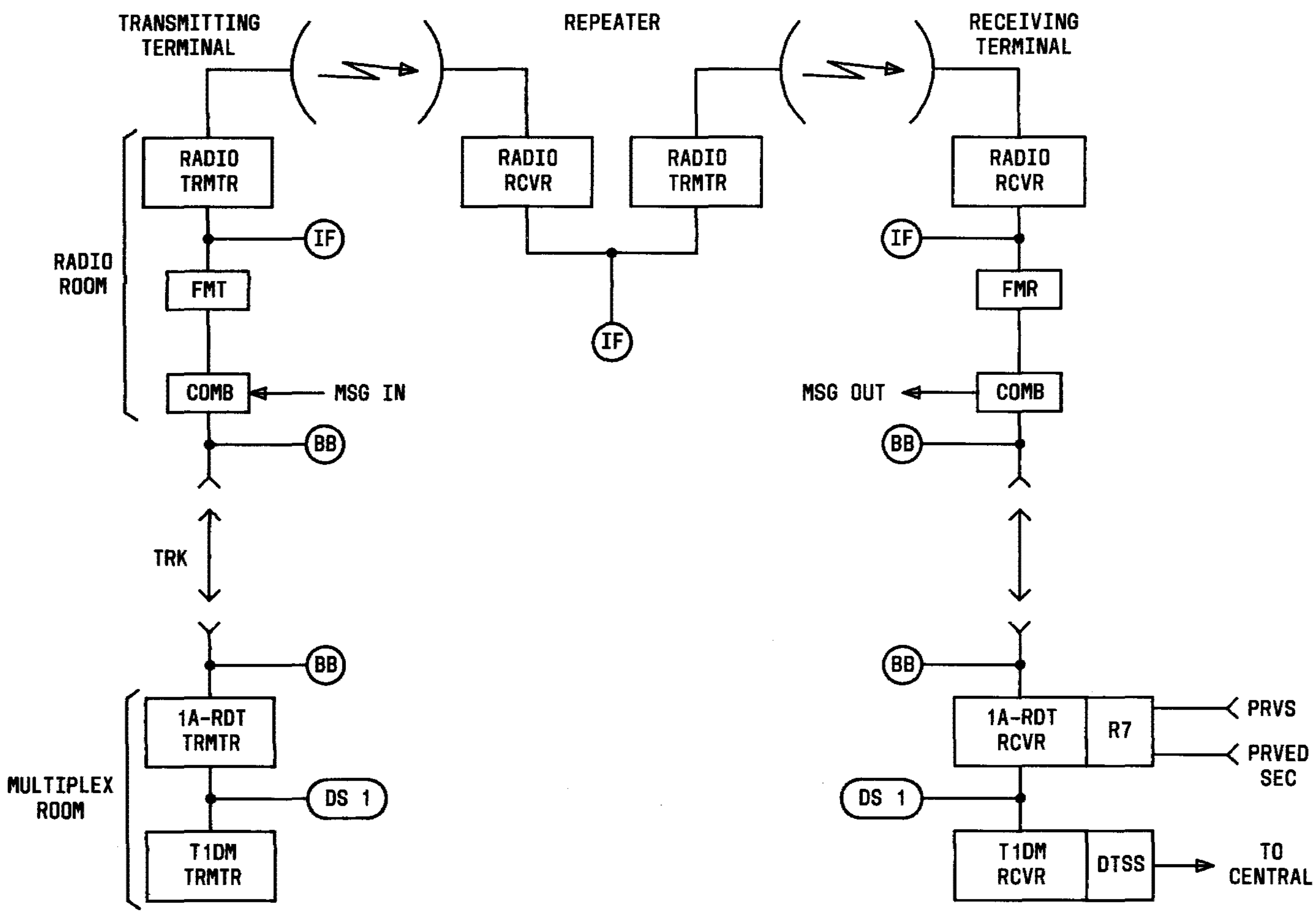


Fig. 4 —Test Access Points— 1A-RDS Route

TABLE C

POSSIBLE ERROR SOURCES — 1A-RDS

A. INSTALLATION FACTORS

- 7-level signal cables improperly installed
- Poor cable splices
- Poor solder joints
- Noise pickup due to poor grounding
- Inadequate C/I ratio on radio route
- Negative fade margin on radio
- Failure to meet pre-service BSP requirements
- AC coupling into 7-level signal
- Relay transients
- RF leakage
- Carrier spreader on 4-Type FMT should be "OFF"

B. MAINTENANCE FACTORS

- Switching
  - Radio switching (IF), cross-band diversity
  - FM terminal (Baseband)
  - 1A-RDT terminal (head-end bridge and transfer)
  - TH-1 microwave carrier supplies
  - Exerciser operation
- Tip-ring turnover in cross-band switching (400A)
- Improper signal levels
- Improper FM transmitter or receiver alignment
- Failure to do routine test
  - PRVed Seconds Test
  - Noise margin test
- Microwave generator off frequency or causing tones
- Carrier spread switch on 4-Type FMT not in "OFF" position
- Human errors

C. EQUIPMENT MALFUNCTIONS

- Defective relay contacts
- Microphonics
- Defective amplifiers
  - Digroup connector
  - 1A-RDT access panels
- Failure in microwave radio circuits
  - TH-1 microwave carrier supply
  - Tube failure
  - Improper signal levels
- Failure in 1A-RDT terminals
  - DC/DC converter
  - Loss of stress
  - Plug-ins become marginal, intermittent, or inoperative

D. OTHER

- Power hits

E. RADIO FADING FACTORS

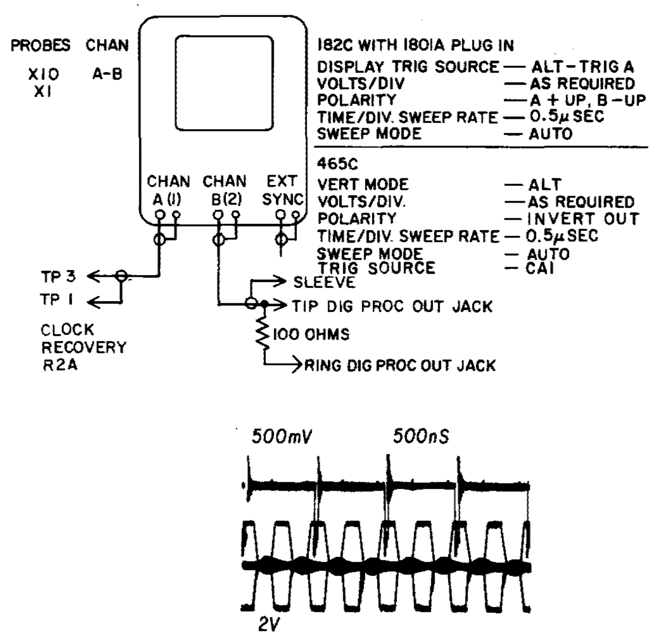
- IF protection switch operation
- Coincident fading (protection channel not available)
- Protection channel in use and not available during fading
- Improper initiator setting
- Improper carrier resupply operation setting

C. Alignment Procedure

STEP	PROCEDURE
1	Remove the front and rear covers from the J68435AF and J68435AG units.
2	Connect the dc power cord on the AF unit to the POWER IN plug on the AG unit.
3	Connect the ground clip on the AG unit to bay ground.
4	Using the attached ac power cord, connect the AF unit to a 115-volt source (see ***Note.***) ***Note:*** The ac power cord must be connected to a circuit that does not have fluorescent lights, soldering irons, etc. This causes PRVs to occur and will be indicated at the R7 board of the digital processor unit.
5	Connect the RMS voltmeter to a 115-volt ac source.
6	**TURN ON** all units and allow a 10-minute warm-up period.
7	On the AG unit, set the **VIOLATION TYPE** switch on the MON & TST OSC circuit pack (R7) to **CODING.**
8	Perform appropriate protection switching procedures, if required; connect selected IF or BB monitoring point to the AF unit.
9	Terminate the RMS voltmeter with a 75-ohm feed-thru termination, and connect the voltmeter to the **DIGROUP OUT** jack on the AF unit. If using the 8920A, use the **LOW RANGE ENABLE** function.
10	While observing the RMS voltmeter, adjust the AR1 amplifier **LEV ADJ** control for a signal level of −16.0 dBm. ***Note:*** If unable to obtain the level requirements, measure the power level between test points **GROUND** and **A** and **GROUND** and **B** on the amplifiers. The difference between **GROUND** and **A** and **GROUND** and **B** can be no greater than 3 dB. If necessary, replace the amplifier.
11	Disconnect the RMS voltmeter from the **DIGROUP OUT** jack and connect the voltmeter to the **DE-EMP OUT** jack.
12	Observe the RMS voltmeter while adjusting the AR2 amplifier **LEV ADJ** control for a signal level of −13.0 dBm. ***Note:*** If unable to obtain the level requirements, measure the power level between test points **GROUND** and **A** and **GROUND** and **B** on the amplifiers. The difference between **GROUND** and **A** or **GROUND** and **B** can be no greater than 3 dB. If necessary, replace the amplifier.
13	Disconnect the RMS voltmeter from the **DE-EMP OUT** jack.
14	Using the 75-ohm unbalanced cable, connect the **DE-EMP OUT** jack on the AF unit to the **DIG PROC IN** jack on the AG unit.
15	Connect the RMS voltmeter to the **TST** jack on the AGC AMPL circuit pack (R1) on the AG unit.

STEP	PROCEDURE
16	Observe the RMS voltmeter while adjusting the **R1 GAIN** control for a meter indication of −35.3 dBm. Slow adjustment is necessary for adequate response time.
17	Disconnect the RMS voltmeter from the **R1 TST** jack.
18	Adjust the **0.772 CLK** control on the **CLOCK RECOVERY** circuit pack **(R2A)** until the **R7 PRVS** indicator is extinguished. No adjustment is necessary if indicator is extinguished.
19	Connect the RMS voltmeter to the **R7 PRVS** jack and measure the signal level. The signal level should be less than −51 dBm (−52 dBm is less than −51 dBm). If necessary, adjust the **R2A 0.772 CLK** control for a signal level less than −51 dBm.
20	With the RMS voltmeter still connected to the **R7 PRVS** jack, using another 75-ohm unbalanced cable, connect the **R7 TST OSC OP** jack to the **R1 TST** jack.
21	Adjust the **R7 TST OSC LEV** control for a digital meter indication of approximately −29 dBm at the **R7 PRVS** jack. This will be a near mid-scale reading on the peaking meter and the meter indication may oscillate.
22	Adjust the **R2A 0.772 CLK** control for a minimum peaking meter indication. If the peaking meter drops off-scale, bring the meter back to mid-scale by adjusting the **R7 TST OSC LEV** control. ***See Note.*** ***Note:*** Continue this step until you obtain a null, and adjustment of the **0.772 CLK** control has no minimizing effect.
23	Adjust the **R1 GAIN** control for a minimum peaking meter indication. If the meter drops off-scale, bring the meter back to mid-scale by adjusting the **R7 TST OSC LEV** control. ***See Note.*** ***Note:*** Continue this step until you obtain a minimum indication, and adjustment of the **R1 GAIN** control has no minimizing effect.
24	Disconnect the RMS voltmeter from the **R7 PRVS** jack.
25	Adjust the **R7 TST OSC LEV** control ***counterclockwise*** until the **R7 PRVS** indicator flash rate is approximately one flash per second.
26	Remove the connection between the **R7 TST OSC OP** jack and the **R1 TST** jack. Connect the RMS voltmeter to the **R7 TST OSC OP** jack and measure the signal level. The signal level should be +3.0 dBm or greater. If the signal level is not +3.0 dBm or greater, repeat this procedure from the beginning.
27	Disconnect the RMS voltmeter from the **R7 TST OSC OP** jack.
28	Follow local procedures when setting up the counter or printer for monitoring the data signal. The test setup is complete and ready to monitor PRVs and PRVed seconds. If a proper 1.544 Mb/s bipolar output is necessary (i.e., if a test set such as the Bowmar 271B or the J68435AH

STEP	PROCEDURE
	Digital Signal Monitor Test Set is to be connected to the **DIG PROC OUT** jack), condition and connect the oscilloscope as shown in Fig. 5.
29	While observing the oscilloscope display, adjust the **R2A 1.544 CLK** control until the 1.544 Mb/s strobe is centered as shown in Fig. 5. When the strobe is centered, disconnect the oscilloscope.
30	The test set is ready for monitoring the 1.544 Mb/s DS-1 digital signal.



NOTE:
IF SIMILAR INDICATION CANNOT BE OBTAINED VERIFY POLARITY OF LOOPING PATCH AND/OR TRANSMITTING AND RECEIVING ACCESS PANELS

Fig. 5—Full Rate (1.544 MHz) Clock Adjustment

4. MONITORING POINTS

A. Test Access Points—Monitoring Arrangements

4.01 The Signal Monitor Test Set measures PRVs, which are violations that have been introduced in the encoded 7-level signal. These violations are measured in terms of PRVed seconds. Tables of PRVed seconds requirements are provided in Table D of this section. Test access points of the 1A-RDS system are shown in Fig. 4.

4.02 The PRVed seconds, as measured by the signal monitor test set, can only be compared to the PRVed seconds measured by another Signal Monitor Test Set or a terminal 1A-RDT. PRVed seconds cannot be compared to the pilot phase hits measured by the J68448A set or errored seconds as measured by Digital Transmission Surveillance System (DTSS).

> ***Caution: Any of the following patching or switching procedures must be performed only by a qualified radio technician.***

B. IF Access

4.03 The IF input power to the FMR must be a nominal −7 dBm. The 386-kHz pilot power to the DIGROUP IN must be a nominal −58 dBm. There are many points in a radio room where the IF signal can be accessed; therefore, the information in this table is intended only as a guide.

> *Note:* Use of an IF amplifier (external or built into AF units) is required when accessing the IF signal at **MON** jacks.

JACK DESIGNATION	IF ACCESS LOCATION
MON	Terminal Patch Bays
MON	100A and 400A Switch Bays

C. IF Access at Repeater Locations

4.04 Request the receive radio terminal to switch the channel to protection.

4.05 Make the following patches after the switch is completed.

(a) Remove the cable from the **IF MAIN AMP OUT** jack and connect it to the **IF OUT 1** jack on the AF unit.

TABLE D

LONG-HAUL (TD-TH) SYSTEM PRVed SECONDS REQUIREMENTS

N + 5K (See Note)	MAXIMUM PRVed SECONDS— 24-HOUR TEST
10	54
15	80
20	107
25	133
30	159
35	186
40	212
45	238
50	264
55	290
60	316
65	341
70	367
75	393
80	419
85	444
90	470
95	496
100	522
105	547
110	572
115	598
120	623
125	648
130	674
135	699
140	724
145	750
150	775
155	800
160	825

Note: PRVed seconds requirements can be calculated by the formula:

N + 5K

where N = Number of radio hops between 1A-RDTs
and K = Number of DMURs between 1A-RDTs.

(b) Using 724 or 720-type cable equipped with proper plugs, patch the **IF MAIN AMP OUT** jack to the **IF IN** jack of the AF unit.

(c) Using the 481B plug, connect the **IF OUT 2** jack to the **FMR IN** jack on the AF unit.

(d) Request the receive radio terminal to release the protection switch.

JACK DESIGNATION	* BASEBAND ACCESS LOCATION
FMR OUT	FMR TERM Patch Bays
BB OUT	†3-Type FM Equipment
FMR OUT	†4-Type FM Equipment

* Requires a switch to protection channel

† Requires use of external pads to obtain −58 dBm level at DIGROUP IN jack

5. MAINTENANCE

5.01 For convenience in on-site maintenance, circuits in the J68435AG unit, which contain active components, are mounted on replaceable plug-in circuit boards. The boards are identical to and interchangeable with similar boards in the bay mounted terminal digital processor. The AR1 and AR2 amplifiers in the AF unit are replaceable Farinon units.

5.02 When a plug-in board must be replaced, care should be exercised to prevent damage to the board, connector, wiring, etc. To remove a board in the AG unit, slide the locking bar and pull the board forward (toward you) until it can be removed from its mounting slot. To insert a board into its designated mounting slot, ensure it is the correct board for the slot, then slide it into the mounting slot until it is seated in the connector and slide the locking bar.

5.03 Each board is mechanically keyed to prevent insertion into the wrong connector. If a board does not readily fit into its connector, verify that the circuit board is the correct one for that particular slot.

Caution: Do not force a plug-in circuit board into a connector.

5.04 If replacement of plug-in circuit boards or amplifiers does not clear a trouble in the 1A-RDS Signal Monitor Test Set, follow local procedures for repair or replacement of the set.

6. REFERENCES

6.01 The following reference material provides additional information:

Drawings	Title
SD-51901-01	1A-RDS Signal Monitor Test Set
SECTION	
356-454-100	1A-RDS Overall Description
356-454-300	1A-RDT Operation
356-454-500	1A-RDS General Test Information
356-454-511	1A-RDS In-Service Trouble Locating Tests
356-454-512	1A-RDS Out-of-Service Trouble Locating Tests
356-454-520	1A-RDS Routine Tests