

905A AND 905B DATA TEST SET

DATASPEED SIGNAL GENERATOR

GENERAL DESCRIPTION AND PRINCIPLES OF OPERATION

1. GENERAL

1.001 This addendum supplements Section 107-201-100, Issue 2. The attached pages must be inserted into the section in accordance with the filing instructions above.

1.002 This addendum is reissued to incorporate the latest changes in electrical adjustments.

1.003 Arrows in the margins indicate changes or additions.

Attached:

Page 9, revised November 1964; reissued, February, 1965
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Page 11, dated February, 1965, revised

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CONTENTS	PAGE	CONTENTS	PAGE
1. GENERAL DESCRIPTION	1	MECHANICAL ADJUSTMENTS	10
GENERAL	1	A. Striker Adjustment	10
TECHNICAL DATA	1	B. Cable Storage	11
A. Output Data	1	4. MAINTENANCE	11
B. Physical Description	3	5. DIAGRAM INDEX	11
C. Operational Features	3	1. GENERAL DESCRIPTION	
D. Alternate Letters-Blank Plug	4	GENERAL	
E. Miscellaneous Power Requirements	4	1.01 This section is reissued to include latest engineering changes and to add information concerning an optional "alternate letters-blank" plug and to include the circuit board diagrams.	
F. Detailed Testing Procedures	4	1.02 The DATASPEED 905A and 905B Data Test Sets generate a variety of test patterns, adding controlled amounts of mark or space bias distortion, and are used in testing type 1 and 2 DATASPEED Tape Senders and Receivers. A panel connector enables the 905A or 905B to be used with a 902A Data Test Set (error counter and distortion measuring device). Both the 905A and 905B operate from a nominal 115 volt 60 cycle source.	
2. PRINCIPLES OF OPERATION	4	TECHNICAL DATA	
GENERAL	4	A. Output Data	
DESCRIPTION	5	1.03 Signal Format - Serial start-stop 10.0 unit Baudot code.	
A. Power Supply	5	(a) Type 1 Format - The zero, sixth and seventh levels are always transmitted as marking signals.	
B. Internal Oscillator and Control	5	(b) Type 2 - 7-level Format - The seventh level is always transmitted as a marking signal.	
C. Bit Ring Counter	5		
D. Character Ring Counter	6		
E. Message Matrix	6		
F. Space and Start Pulse Inserter	7		
G. Signal Regenerator	7		
H. Distortion Inserter	7		
I. Output Amplifiers	8		
J. Synchronization with the 902A Data Test Set	9		
3. ADJUSTMENTS	9		
TEST EQUIPMENT REQUIRED	9		
ELECTRICAL ADJUSTMENTS	9		
A. Adjustable Supply Voltages	9		
B. Non-Adjustable Supply Voltages	9		
C. Internal Oscillator	9		
D. Clock Delay	10		
E. Distortion Generator	10		

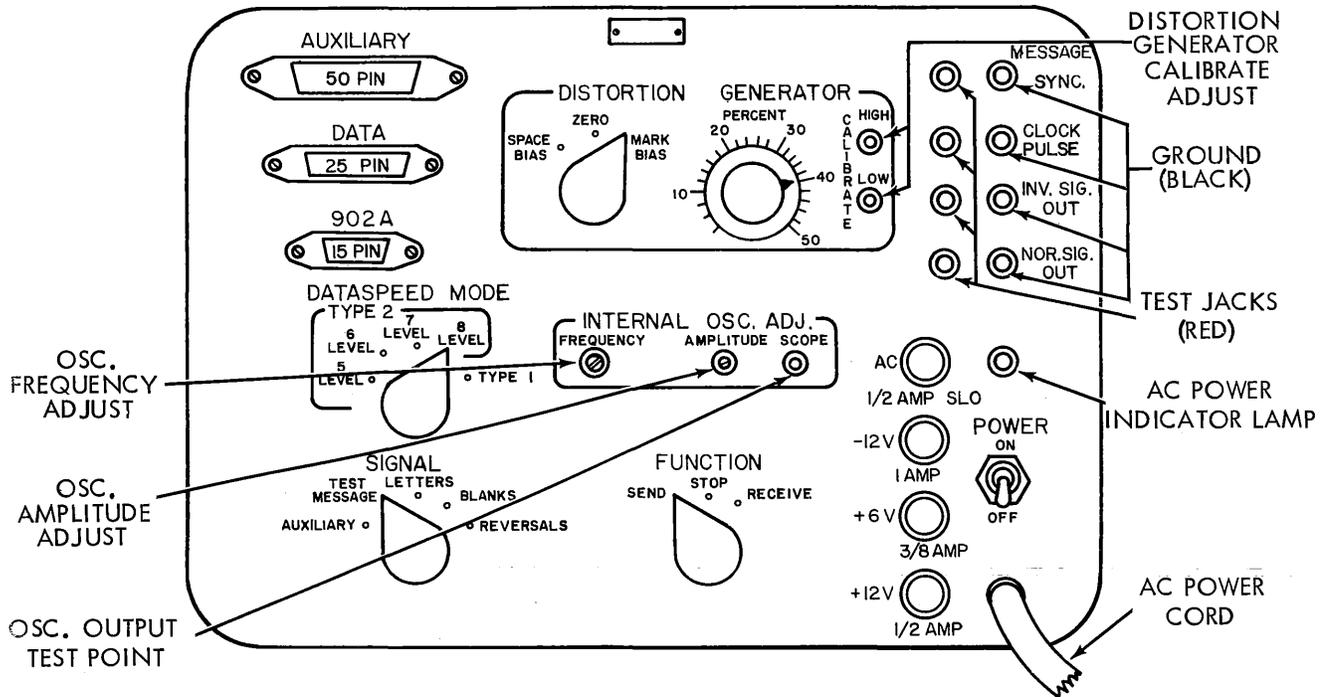


Figure 1 - 905A/905B Data Test Set - Front Panel

- (c) Type 2 - 6-level Format - The sixth and seventh levels are always transmitted as marking signals.
 - (d) Type 2 - 5-level Format - The sixth and seventh levels are always transmitted as marking signals and the zero level is always transmitted as a space signal.
- 1.04 Output Test Patterns
- (a) Test Message: 14-character (140 bits). See Figure 4.
 - (b) Letters: See Figure 4.
 - (c) Blanks: See Figure 4.
 - (d) Reversals: Alternate mark and space signals. See Figure 4.
- 1.05 Normal Output Signal Amplifier Characteristics
- (a) Normal Signal Voltage: Meets EIA standard, +6 volts $\pm 10\%$ (space) and -6 volts $\pm 10\%$ (mark).
 - (b) Rise and Fall Time: Less than 2 microseconds.
 - (c) Minimum Load Resistance: 3000 ohms.
- 1.06 Inverted Output Signal Amplifier Characteristics
- (a) Inverted Signal Voltage: -0.6 ± 0.3 volt (mark) and -6 volts $\pm 10\%$ (space).
 - (b) Rise and Fall Time: Less than 2 microseconds.
 - (c) Minimum Load Resistance: 1000 ohms to -6 or -12 volts; 5000 ohms to ground.
- 1.07 Signal Speed
- (a) Words Per Minute: 1050 wpm.
 - (b) Bit Rate: 1050 $\pm 0.1\%$ bits per second internally driven. Can be externally driven from a Bell System type 902A Data Test Set.
- 1.08 Output Signal Accuracy (Referenced to start pulse).
- (a) Mark or space bias distortion can be added, up to 50%, to the output signal with an over-all accuracy of better than $\pm 3\%$ peak accumulative error as read from the distortion control.

(b) With no distortion added to the output signal the peak accumulative distortion is less than $\pm 1\%$.

B. Physical Description

1.09 905A dimensions: 19" x 8-3/4" x 6-7/8", weight - 18 pounds. With adapters (TP146753), dimensions: 23" x 8-3/4" x 6-7/8", weight - 18 pounds.

1.10 905B dimensions: 19" x 12" x 8-7/8", weight - 17 pounds.

C. Operational Features

1.11 Controls (See Figure 1)

(a) POWER Switch: In the ON position ac line voltage is applied to the self-contained power supply.

(b) DATASPEED MODE Switch: This switch selects DATASPEED TYPE 1 - 5 LEVEL, TYPE 2 - 5 LEVEL, TYPE 2 - 6 LEVEL, TYPE 2 - 7 LEVEL, or TYPE 2 - 8 LEVEL mode of operation.

(c) SIGNAL Switch: This switch selects one of four output signals, namely, the 14 character TEST MESSAGE, LETTERS, BLANKS, or REVERSALS. An AUXILIARY position is provided.

(d) FUNCTION Switch: This switch selects the SEND mode, RECEIVE mode, or STOP mode of operation.

(1) SEND Mode: In this position the 905A/905B acts as a transmitter. The output signal is determined by the position of the SIGNAL and the DATASPEED MODE switch. It is operating at a bit rate determined by the internal oscillator (1050 bits per second).

(2) RECEIVE Mode: In this position the 905A/905B acts as a receiver and must be used in conjunction with the Bell System type 902A Data Test Set. The SIGNAL and DATASPEED MODE switch are set to positions corresponding to the received data signal. The 905A/905B is driven externally from the 902A at a bit rate (1050 bits per second) determined by the received data signal. The received data signal and the output of the 905A/905B are compared bit by bit in the 902A. Any errors are detected and counted by the 902A.

The two signals are initially phased by depressing the WORD SYNC. and RESET button on the 902A.

(3) STOP Mode: In this position the output signal goes to a mark hold condition at the end of the test message or character.

(e) DISTORTION Switch: This switch selects MARK BIAS, SPACE BIAS, or ZERO BIAS distortion.

(f) PER CENT Control: This potentiometer determines the per cent bias distortion to be added to the output data signal. When the DISTORTION switch is in the ZERO position, the PER CENT control is disabled. The calibrated scale is marked off in 2% intervals from a minimum of 4% to a maximum of 50%.

1.12 Test Jacks (See Figure 1)

(a) MESSAGE SYNC: A nominal -6 to 0 volt pulse occurring once every 14 characters of the test message appears at this test jack. It is intended for use as an external trigger for an oscilloscope when observing the entire test message.

(b) CLOCK PULSE: A nominal -6 to 0 volt pulse occurring approximately in the center of every bit appears at this test jack. When the 905A/905B is in the SEND condition, these pulses occur at the bit rate of the internal oscillator (1050 bits per second). When in the RECEIVE condition, these pulses occur at the bit rate of the received data signal. This test jack is used when checking the bit rate of the internal oscillator, or checking the bit rate of the received data signal.

(c) NOR. SIG. OUT: The polar output data signal appears at this test jack. This signal has mark represented by -6 volts and space represented by +6 volts.

(d) INV. SIG. OUT: A neutral inverted data signal appears at this test jack. Mark is represented by 0 volt and space is represented by -6 volts. This signal has the proper polarity to drive a DATASPEED receiving distributor module.

1.13 Indicator (See Figure 1). An indicator lamp lights when the POWER switch is placed in the ON position.

SECTION 107-201-100

1.14 Connectors (See Figure 1)

- (a) 902A: This 15-pin connector (and cable supplied with 902A Data Test Set) connects the 905A/905B to the 902A.
- (b) DATA: This 25-pin connector, together with associated cables (TP146743 and TP146744), connects the 905A/905B to a DATASPEED Cabinet of a Data Set 202A or 202B (furnished with 905B only).
- (c) AUXILIARY: This 50-pin connector, together with associated cable, is for future use.

D. Alternate Letters-Blank Plug

1.15 An auxiliary "alternate letters-blank" plug is available as an optional feature. With the SIGNAL switch in the AUXILIARY position and the alternate letters blank plug inserted in the AUXILIARY connector, the data output will be alternately a letter character then a blank character.

E. Miscellaneous Power Requirements

1.16 AC Line Requirements

- (a) Voltage: 105-125 volts 60 cps.
- (b) Power Input: 18 watts maximum without 902A, 25 watts maximum with 902A.

1.17 Fuses (See Figure 1)

- (a) AC Line - 1/2 amp slow blow.
- (b) +12 volts - 1/2 amp fast blow.
- (c) +6 volts - 3/8 amp fast blow.
- (d) -12 volts - 1.0 amp fast blow.

1.18 DC Power for Auxiliary Equipment: Regulated ± 12 volts is supplied to the 902A. Reserve DC power for other auxiliary equipment is supplied through the AUXILIARY 50-pin connector as follows:

- (a) With 902A Data Test Set: -12 volts regulated at 125 ma maximum and +17 volts unregulated at 125 ma maximum.
- (b) Without 902A Data Test Set: -12 volts regulated at 300 ma maximum and +17 volts unregulated at 250 ma maximum.

F. Detailed Testing Procedures

1.19 For detailed testing procedures refer to Bell System Practice 314-825-502.

2. PRINCIPLES OF OPERATION

GENERAL

2.01 For descriptive purposes, the circuit may be divided into ten major parts. (Refer to schematic - Figure 5.)

(a) Power Supply

(b) Internal Oscillator and Control: Circuit elements Z19-B, Z20-B, Z23-C, Z22, Z21, Z19-A, Z20-A, and associated components.

(c) Bit Ring Counter: Circuit elements Z16, Z4-C, Z4-D, Z5-A, Z5-B, Z5-C, Z5-D, Z6-A, Z6-B, Z6-C, Z6-D, and associated components.

(d) Character Ring Counter: Circuit elements Z17-A, Z1-A, Z1-B, Z1-C, Z1-D, Z2-A, Z2-B, Z2-C, Z2-D, Z3-A, Z3-B, Z3-C, Z3-D, Z4-A, Z4-B, and associated components.

(e) Message Matrix: Circuit elements Z20-C, Z13-A, Z13-B, Z13-C, Z13-D, Z14-A, Z14-B, Z14-C, Z14-D, Z15, Z20-E, and associated components.

(f) Space and Start Pulse Inserter: Circuit elements Z8, Z19-C, and associated components.

(g) Signal Regenerator: Circuit elements Z18, Z9, Z23-D, and associated components.

(h) Distortion Inserter: Circuit elements Z10-A, Z10-B, Z10-C, Z11-A, Z11-B, Z12-A, and associated components.

(i) Normal and Inverted Output Amplifier: Circuit elements Z12-B, Z20-F, and associated components.

(j) Synchronization with the 902A Data Test Set: Circuit elements Z24, Z23-A, Z23-B, Z7-A, and associated components.

DESCRIPTION

A. Power Supply (See Figure 5)

2.02 The AC power line is connected to terminals 3, 4, and 5 of the electrical noise suppressor, Z25. (The ground wire from the power line is connected directly to the frame. An additional wire connects the frame to terminal 4 of the suppressor.) The output of Z25, terminals 1 and 2, passes through the POWER switch S4 and fuse F1 to the primary of the power transformer, T1. The indicator lamp, DS1, is lighted when AC power is delivered to T1.

2.03 The secondary of T1 drives three full wave rectifier circuits consisting of diodes CR8, CR9, and filter capacitor C2, diodes CR2, CR3 and filter capacitor C3, diodes CR1, CR4, and filter capacitor C4. The three rectified voltages are fused by F3, F4, and F2 respectively.

(a) An unregulated +6 and +1.5 volts is derived from the rectifier circuit consisting of CR8, CR9, C2 and associated components. Rheostats R1 and R2 must be adjusted to obtain the required voltages (refer to Paragraph 3.04).

(b) A regulated +12 and +6 volts is derived from the rectifier circuit consisting of CR2, CR3, C3 and associated components. Resistors R13, R10 and zener diode CR7 regulate the +12 volts. When the 902A Data Test Set is plugged into J3, 902A connector, resistor R10 is shunted by the parallel combination of resistors R134 and R135 located in the 902A. This enables the +12 volt regulated supply to handle the increased load of the 902A. Element Z17-B regulates the +6 volts which is only used by element Z11.

(c) A regulated -12 volts is derived from the rectifier circuit consisting of CR1, CR4, C4, and associated components. Power transistor Q1 acts as a series regulator. Resistor R12, varistor CR10, and zener diode CR5 keep a constant voltage at the base of Q1. The emitter voltage of Q1 is approximately equal to the base voltage and independent of load. Zener diode CR6, resistor R9, and the external load shunting R9 provide the -6 volt regulated source.

B. Internal Oscillator and Control

2.04 When the FUNCTION switch S3 is in the SEND position, zero volts is applied through R18 to terminal E of the oscillator Z22.

This causes the oscillator to turn on. The sinusoidal output at terminal A is reshaped by the squaring amplifier Z21. Its output, a narrow -6 to 0 volt pulse, passes through the Z19-A OR gate and the Z20-A emitter follower with no change in polarity or signal level.

2.05 When the FUNCTION switch S3 is in the STOP position, the oscillator Z22 will turn off when the following conditions are satisfied: (1) When the output signal is marking, (2) when the test message has completed its cycle (if in the TEST MESSAGE position), and (3) when the character is in the stop bit (if in the LETTERS or BLANKS position). The three input AND gate Z19-B monitors the condition of the output signal. When the above conditions are met, the output of Z19-B at terminal B goes from -6 to 0 volts. This signal passes through emitter follower Z20-B and is inverted by element Z23-C. The output of Z23-C at terminal K, which goes from 0 to -6 volts, is tied to terminal E of the oscillator Z22 through S3. This -6 volt signal overrides the zero volt bias through R18 and turns element Z22 off, thus keeping the output signal in the mark hold condition.

2.06 When the FUNCTION switch S3 is in the RECEIVE position, -6 volts is applied to terminal E of the oscillator Z22 through S3. This keeps element Z22 off. At the same time conditions are set up by S3 to allow the external oscillator in the 902 Data Test Set to be switched into the circuit. See Subpart 2J for further description.

C. Bit Ring Counter

2.07 The bit ring counter has 10 elements. Each element corresponds to one bit of the serial start-stop 10.0 unit code.

2.08 The internal oscillator drives the bit ring counter through the ring driver Z16 when the FUNCTION switch S3 is in the SEND position. The clock pulse from the 902A Data Test Set drives the bit ring counter when the FUNCTION switch S3 is in the RECEIVE position.

2.09 The narrow -6 to 0 volt clock pulses from Z20-A terminal E are tied to the input of the bit ring driver Z16 terminal N. The output at terminal R drives the bit ring counter with a +2 to -6 volt narrow drive pulse.

2.10 All the outputs of the bit ring counter are at -6 volts except one element which is at 0 volt. Each time a drive pulse occurs, the

element whose output is at 0 volt goes to -6 volts, and the output of the adjacent element goes from -6 volts to 0 volt. When the output of the stop bit element Z6-D goes from 0 to -6 volts, the output of the start bit element Z4-C goes from -6 to 0 volt. This process continues while the drive pulses are present.

D. Character Ring Counter

2.11 The character ring counter has 14 elements. Each element corresponds to one character of the 14-character test message.

2.12 The character ring counter operates only when the bit ring counter is operating and when the SIGNAL switch S2 is in the AUXILIARY, TEST MESSAGE, LETTERS or REVERALS positions. The leading edge of the stop bit, the -6 to 0 volt transition of element Z6-D at output terminal H, drives the character ring driver Z17-A at terminal S. The output at terminal N drives the character ring counter with a +2 to -6 volt narrow drive pulse.

2.13 The theory of operation is identical to the bit ring counter except the character ring counter steps once for every ten steps of the bit ring counter.

E. Message Matrix

2.14 The outputs of the bit ring counter and the character ring counter are interconnected by a modified cross-point diode matrix. The eight AND gates, elements Z13-A, Z13-B, Z13-C, Z13-D, Z14-A, Z14-B, Z14-C, and Z14-D, comprise the cross-point matrix. The outputs from each of these eight AND gates are tied to the inputs of the matrix OR gate, Z15, which has twelve inputs. The four remaining inputs of element Z15 are tied to outputs of the three character ring counter elements (LTRS elements) Z1-A, Z1-B, and Z1-C plus the output of emitter follower Z20-C which is driven by Z6-D terminal H, the ring counter element for the stop bit.

2.15 At the output of Z15, terminal J, appears the desired serial data signal minus the start pulse and other spacing pulses necessary to obtain the DATASPEED type 2 format. These spacing pulses are added by the space and start pulse inserter circuit described in Paragraph 2.22. The serial data, signal at terminal J of element Z15 has space represented by -6 volts and mark represented by 0 volt. The start pulse appears as a mark signal (0 volt).

2.16 Type 1: The type 1 (5 level) DATASPEED format has the zero, six and seven bits of the data signal marking at all times. This is accomplished by placing the DATASPEED MODE switch S1 in the TYPE 1 position which in turn puts +6 volts at one of the inputs of the elements Z13-A, Z14-C and Z14-D matrix AND gates. Thus, the outputs of the zero, six and seven level elements of the bit ring counter are allowed to pass through their respective matrix AND gates to the matrix OR gate independent of the character ring counter, making the zero, six and seven level bits of the data signal at element Z15 terminal J, MARK (0 volt) at all times. See Figure 4 for typical outputs at the output J11 for type 1 mode operation.

2.17 Type 2: 5, 6, 7, 8-level: See Paragraph 2.22 for space inserter description.

2.18 Test Message: The test message 14-character sequence originates in the character ring counter. The output of the character ring counter and bit ring counter are interconnected to the modified cross-point diode matrix, and the matrix OR gate Z15. When the SIGNAL switch S2 is in the TEST MESSAGE position, the serial signal at the matrix OR gate (terminal J) is tied to the emitter follower Z20-E terminal S through one section of S2.

2.19 Blanks: When the SIGNAL switch S2 is in this position, +12 volts through one section of S2, is applied at terminal L of element Z17-A, the character ring driver, this causes the output of element Z17-A at terminal N to be -6 volts independent of the input signal at terminal S. When the output of the character ring driver is at -6 volts, all of the outputs of the character ring counter are at -6 volts. With the character ring counter outputs all at -6 volts, the only MARK (0 volt) pulses entering the matrix OR gate Z15 are the stop bits from element Z20-C and the output pulses from the AND gates Z13-A, Z14-B and Z14-C which are a function of the position of the S1 MODE switch.

2.20 Letters: When the SIGNAL switch S2 is in this position, the data signal at element Z15 terminal J is not allowed to pass through emitter follower Z20-E. Instead, +1.5 volts is applied to the input of this emitter follower at terminal S. This represents a steady mark signal. The start pulse and other space bits are added by the space and start pulse inserter circuit described in Paragraphs 2.22 through 2.25. The emitter follower Z20-D is used for current amplification of the OR gate Z15 for use in the auxiliary position of the SIGNAL switch (S2).

2.21 Auxiliary: When the SIGNAL switch S2 is in this position, terminal S of emitter follower is connected to pin 35 of AUXILIARY receptacle J1. An external device is thus required to obtain an output signal. One such device is the optional "alternate letters-blank" connector. This connector is essentially an 8-input OR gate. Seven of the OR gate inputs are taken from alternate characters of the character ring counter. The eighth input is connected to the output of the bit ring counter stop element. The output of the OR gate connector (pin 35) is connected to emitter follower Z20-E (pin 5) through contacts 13 and 18 of the SIGNAL switch. The OR gate output will be alternately marking then spacing as the character ring counter is stepped through its cycle.

F. Space and Start Pulse Inserter

2.22 Flip-flop Z8, in conjunction with the bit ring counter and DATASPEED MODE switch S1, generate at terminal K of Z8, a waveform such that when gated with the data signal at element Z20-E terminal A (0 volt mark, -6 volts space), it inserts the proper start pulse and space pulses required for the DATASPEED type 1 and 2 formats.

2.23 Type 1 (5-level) or type 2 (6, 7, and 8-level): When the DATASPEED MODE switch S1 is in either of these positions, terminal K of element Z8 has the following waveform: -6 volts during the start bit interval of the data signal and 0 volt during the rest of the time.

2.24 Type 2 (5-level): When the DATASPEED MODE switch S1 is in this position, terminal K of element Z8 has the following waveform: -6 volts during the start and zero bit interval of the data signal and 0 volt during the rest of the time.

2.25 The two input AND gate Z19-C is driven by the signal from element Z20-E terminal A and element Z8 terminal K. The output signal of element Z19-C terminal A is the serial data signal with 0 volt representing mark and -6 volts representing space for the type 1 or type 2 formats.

G. Signal Regenerator

2.26 Regenerating the data signal at terminal A of element Z19-C is two-fold. First, the final output data signal must be delayed approximately a half bit in order to have the proper phase with respect to the external oscillator in

the 902A Data Test Set. Second, regenerating the data signal removes distortion added at the message matrix.

2.27 One-shot Z18 delays the clock pulses approximately a half bit. The -6 to 0 volt transition at terminal K of element Z18 drives the signal flip-flop Z9 at terminals E and F, the mark and space inputs. The data signal at element Z19-C terminal A drives the prime 1 input of element Z9, and the inverted data signal at terminal L of element Z23-D drives the prime 0 input of element Z9.

Note: A prime input may be considered a conditioning input. A prime signal is generally a long duration type of signal -- in this case longer than the mark and space signals of the clock pulse -- which conditions the circuit to operate upon reception of the input (clock) signal.

2.28 The output of element Z9 at terminal K is the regenerated data signal delayed a half bit and with all bias distortion removed.

2.29 This data signal at element Z9 terminal K has -6 volts representing mark and 0 volt representing space, and is inverted with respect to the output signal of element Z19-C terminal A (see Paragraph 2.25).

2.30 REVERSALS - When the SIGNAL switch S2 is in this position, circuitry is set up by switch S2 to convert the signal flip-flop, element Z9, to a binary counter or frequency divider. The inputs to element Z9 at terminals E and F are the delayed clock pulses. The output of element Z9 at terminal K is a symmetrical square wave with one bit length at 0 volt (space) and one bit length at -6 volts (mark). This waveform represents the reversals data signal.

H. Distortion Inserter

2.31 Mark Bias Distortion

(a) When the DISTORTION switch S5 is in the MARK BIAS position, the data signal at element Z9 terminal K is connected to terminal N, the input of the element Z10-B integrator. When this input at terminal N is at -6 volts (mark), the output at terminal K is at 0 volt. When the input at terminal N switches from -6 to 0 volt (space), the output at terminal K goes from 0 to -6 volts along a ramp of slope -6 volts per bit width. This waveform is passed through emitter follower Z10-C.

(b) This integrated data signal at terminal C of element Z10-C is tied to the input of the slicing amplifier Z11-A at terminal N. The slicing or switching level of element Z11-A is determined by the setting of the PER CENT control R5, which acts as an adjustable voltage divider. The output of R5 at terminal 2 passes through emitter follower Z12-A which in turn drives the slicing amplifier Z11-A at terminal M, the slicing level input. The output of element Z11-A at terminal J is the distorted data signal with 0 volt for mark and -6 volts for space. This signal is then inverted by element Z11-B which then drives element Z12-B, the normal output amplifier.

(c) When the PER CENT control is set at 10% the slicing voltage at terminal M of Z11-A will be approximately -1 volt. When the control is set at 40%, the slicing voltage at terminal M of Z11-A will be approximately -3.5 volts. Potentiometers R3 and R4 must be adjusted in order to have correspondence between the actual bias distortion added to the data signal and the scale markings on the PER CENT control R5 (see Paragraph 3.11).

2.32 Space Bias Distortion

(a) When the DISTORTION switch S5 is in the SPACE BIAS position, inverter Z11-B is bypassed and inverter Z10-A inverts the undistorted data signal entering integrator Z10-B at terminal N.

(b) The same theory of operation then applies as for mark bias distortion.

2.33 Zero Distortion: When the DISTORTION switch S5 is in the ZERO position, no distortion is added to the data signal at terminal K of element Z9. Instead this signal is switched directly to the normal output amplifier Z12-B.

I. Output Amplifiers

2.34 Normal Output Amplifier: The data signal, whether distorted or not, is tied to terminal F of the normal output amplifier Z12-B. The input signal is 0 volt for space and -6 volt for mark. The output data signal at terminal P is a polar signal with +6 volts representing space and -6 volts representing mark.

2.35 Inverted Output Amplifier: Terminal H of the normal output amplifier Z12-B is an inverted data signal which is 0 volt for mark and -12 volts for space. This inverted data signal

is connected to emitter follower Z20-F at terminal P, the inverted output amplifier. The output at terminal D is clamped to -6 volts through CR11. The resulting inverted output data signal is 0 volt for mark and -6 volts for space.

J. Synchronization with the 902A Data Test Set

2.36 The purpose of this portion of the circuit is to enable the 905A/905B in conjunction with the 902A Data Test Set, to detect and count transmission errors in a received data signal. It is assumed that the 902A is plugged into the 15 pin connector marked 902A and a received data signal is present.

2.37 When the FUNCTION switch S3 is in the RECEIVE position, 0 volt is applied to the two pulse AND gates Z23-A and Z23-B at terminals C and A respectively. This makes the two pulse AND gates become ordinary pulse amplifiers responding to the negative going transition at their inputs. At the same time -6 volts are applied to terminal E of oscillator Z22 turning it off, which puts -6 volts at the output of squaring amplifier Z21 terminal A.

2.38 The output of the phase-locked oscillator in the 902A Data Test Set, a +6 to -6 volt sawtooth, is connected to the input of element Z23-B at terminal F. The +6 to -6 volt transition of the sawtooth occurs approximately at the center of every bit of the received data signal. This 12 volt negative going transition produces a narrow -6 to 0 volt transition at the output of element Z23-B terminal H. This signal is then fed into OR gate Z19-A where it serves as the new clock pulse, which is at the exact bit rate of the received data signal.

2.39 Element Z7-A acts as the collector load of transistor Q202 in the 902A Data Test Set. Normally terminal K of element Z7-A is at -6 volts. When the WORD SYNC AND RESET button on the 902A is depressed, a narrow -6 to 0 volt pulse appears at terminal K of element Z7-A each time the received data signal contains a marking bit. This pulse then drives one-shot Z24 at terminal C.

2.40 Element Z24 has two functions: (1) to delay the signal at its input and, (2) to act as a gate in comparing the received data signal with the output data signal from the 905A/905B.

2.41 Terminal J of element Z24, the prime input (see Paragraph 2.27), is tied to the output data signal at terminal L of the signal

flip-flop Z9. The output data signal at this point is 0 volt for mark and -6 volts for space. If the received data signal is out of word sync with this output data signal when the WORD SYNC AND RESET button on the 902A is depressed, a -6 to 0 volt transition will occur at terminal C of Z24 when terminal J of Z24 is at 0 volt. This condition fires element Z24 causing a -6 to 0 volt pulse, approximately a quarter bit wide, to appear at its output terminal L. The trailing edge of this pulse, 0 to -6 volts, drives element Z23-A producing a narrow -6 to 0 volt pulse at its output terminal J.

2.42 This narrow -6 to 0 volt pulse at terminal J of element Z23-A is connected to the Z19-A OR gate where it serves as a secondary clock pulse. This secondary clock pulse is a quarter of a bit delayed from the normal clock pulse causing the bit ring counter to step at twice its normal rate until word sync is achieved. When the two data signals are in word sync -6 volts appears at terminal J of Z24 each time a -6 to 0 pulse appears at terminal C of Z24, thus inhibiting further secondary clock pulses.

3. ADJUSTMENTS

TEST EQUIPMENT REQUIRED

3.01 Hewlett-Packard 122AR Oscilloscope (904 Data Test Center), or Tektronix 531 Oscilloscope or equivalent.

3.02 Bell System KS-19247 Electronic Counter (904 Data Test Center), or Beckman 7360 Universal EPUT and Timer or equivalent.

3.03 Bell System KS-14510-L1 VOM or equivalent.

ELECTRICAL ADJUSTMENTS

A. Adjustable Supply Voltages

3.04 These adjustments should be made with the ac power on, the ac line voltage at 115 volts, all circuit cards plugged in, and FUNCTION switch S3 in the STOP position.

3.05 +6 V: Adjust +6 volts within ± 0.1 volt by adjusting rheostat R1.

3.06 +1.5 V: This adjustment should always be made after +6 V adjustment. Adjust +1.5 volts to within ± 0.1 volt by adjusting rheostat R2.

B. Non-adjustable Supply Voltages

3.07 The non-adjustable voltages should be within the following limits when all circuit cards are plugged in.

- (a) -12 Volts: Must be between -11.2 and -12.8 volts.
- (b) -6 Volts: Must be between -5.6 and -6.2 volts.
- (c) +12 Volts: Must be between +11.4 and +12.6 volts.
- (d) +6 Volts: Must be between +5.8 and +6.6 volts.

C. Internal Oscillator (1050 cps)

3.08 Oscilloscope Method

- (1) Before adjusting the internal oscillator, turn power on and put FUNCTION switch S3 in SEND position.
- (2) Connect oscilloscope and 905A/905B Data Test Set to a common ground. Connect vertical input of oscilloscope to J12, the SCOPE jack. Set vertical sensitivity at 2 volts/cm. Set horizontal sweep at 200 microseconds/cm. Set trigger at 60 cps line.
- (3) Adjust R6, the AMPLITUDE adjustment, for maximum amplitude without flattening the positive portion of the waveform observed on oscilloscope. The observed waveform will be two superimposed sine waves 180° out of phase with each other.
- (4) Adjust L1, the FREQUENCY adjustment, until trace on oscilloscope does not drift either to the right or left.
- (5) Repeat until both conditions are satisfied, the peak-to-peak voltage of this waveform should be between 9 and 11 volts and the frequency will be 1050 cycles per second.

3.09 Frequency Counter Method

- (1) Before adjusting internal oscillator, turn power on and put FUNCTION switch S3 in SEND position.
- (2) Connect oscilloscope and 905A/905B Data Test Set to a common ground. Connect vertical input of oscilloscope to J12, the SCOPE jack. Set vertical sensitivity at 2

volts/cm. Set horizontal sweep at 200 microseconds/cm. Set trigger at internal positive.

(3) Connect frequency counter to J9, the CLOCK PULSE jack. Set frequency counter for positive trigger and set to measure frequency or period, whichever is more convenient. The waveform at J9 is a narrow -6 to 0 volt pulse.

(4) Adjust R6, the AMPLITUDE adjustment, for maximum amplitude without flattening the positive portion of the sinusoidal waveform observed on oscilloscope.

(5) Adjust L1, the FREQUENCY adjustment, until the frequency counter indicates 1050 \pm 1 cycle per second (if frequency is measured) or 952 \pm 1 microsecond (if period is measured).

(6) Repeat steps (4) and (5) until both are satisfied. When both conditions are satisfied the peak to peak voltage of the sinusoidal waveform should be between 9 and 11 volts.

D. Clock Delay

3.10 Oscilloscope Method

(1) Turn power on, place FUNCTION switch S3 in the SEND position.

(2) Connect vertical input of oscilloscope to test point 2 on element Z18, clock delay. Set horizontal sweep at 100 microseconds/cm, vertical sensitivity at 2 volts/cm, and trigger at internal negative.

(3) Adjust R11 on element Z18 to make the 0 to -6 v pulse 400 \pm 20 microseconds wide.

E. Distortion Generator (See Figure 1)

3.11 Oscilloscope Method

(1) Perform all necessary adjustments on internal oscillator (see Paragraphs 3.08 and 3.09).

(2) Turn power on, place FUNCTION switch S3 in SEND position, place DISTORTION switch S5 in SPACE BIAS position, and place SIGNAL switch S2 in REVERSALS position.

(3) Connect oscilloscope and 905A/905B Data Test Set to a common ground. Connect vertical input of oscilloscope to J11, the

NORMAL OUTPUT SIGNAL jack. Set vertical sensitivity at 5 volts/cm. Set horizontal sweep at 200 microseconds/cm. Set trigger at positive internal.

(4) Set PERCENT control at 40%. Adjust HIGH calibrate R3 until oscilloscope indicates a positive (+6 v) signal duration of approximately 1333 microseconds.

(5) Set PERCENT control at 10%. Adjust LOW calibrate R4 until oscilloscope indicates a positive (+6 v) signal duration of approximately 1048 microseconds.

(6) Repeat steps (4) and (5) until both conditions are satisfied.

3.12 Electronic Timer Method

(1) Perform all necessary adjustments on internal oscillator (see Paragraphs 3.08 and 3.09).

(2) Turn power on, place FUNCTION switch S3 in SEND position, place DISTORTION switch S5 in SPACE BIAS position, and place SIGNAL switch S2 in REVERSALS position.

(3) Connect timer and 905A/905B Data Test Set to a common ground. Connect the timer to J11, the NORMAL OUTPUT SIGNAL

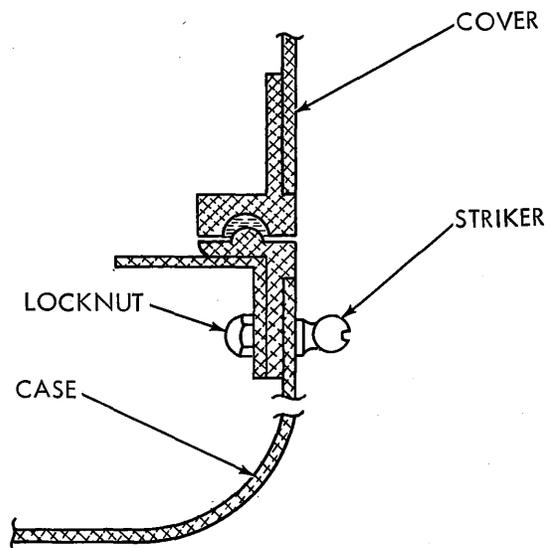


Figure 2 - Striker Adjustment

jack. The START gate of the timer should trigger on positive going transitions and the stop gate of the timer should trigger on negative going transitions.

(4) Set PERCENT control at 40%. Adjust HIGH calibrate R3 until timer indicates 1333 \pm 2 microseconds.

(5) Set PERCENT control at 10%. Adjust LOW calibrate R4 until timer indicates 1048 \pm 2 microseconds.

(6) Repeat steps (4) and (5) until both conditions are satisfied.

MECHANICAL ADJUSTMENTS

A. Striker Adjustment (See Figure 2)

→ 3.13 Remove cover and equipment from case and proceed as follows:

(1) Loosen locknut and turn striker clockwise or counterclockwise to raise or lower striker. Tighten locknut.

(2) Place cover on case and engage latches. Latches should snap on case firmly and securely.

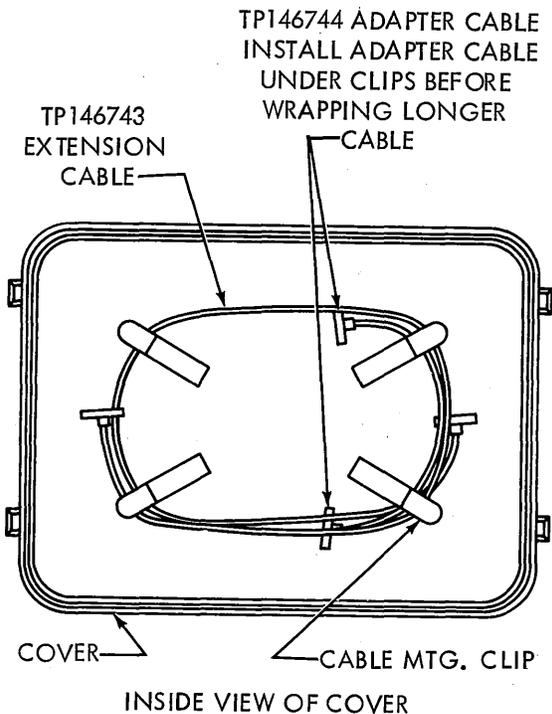


Figure 3 - Cable and Adapter Storage

(3) If latch engagement is too loose, readjust striker position as described in step (1).

B. Cable Storage (905B only)

→ 3.14 Wrap longer cable (TP146743) over shorter cable (TP146744) on clips in carrying case cover (see Figure 3).

4. MAINTENANCE

4.01 Adjustments of the internal oscillator and distortion generator should be checked and adjusted if necessary at monthly intervals, or more frequently if calibration error is suspected. These adjustments can be made on the control panel without removing the 905A/905B assemblies from the cases. Refer to Paragraphs 3.08 through 3.12 for detailed adjustment instructions.

4.02 Adjustments of the clock delay, element Z18, and the adjustable power supply voltages will not normally require periodic maintenance, but should be checked and adjusted whenever malfunction is suspected, or whenever extensive trouble shooting is carried out.

5. DIAGRAM INDEX

5.01 Drawings of each of the circuit cards used in the 905A/905B Data Test Set are bound at the rear of the section. The tabulation following lists these diagrams and the issue.

DRAWING NUMBER	SECTION ISSUE					
	1	2	3	4	5	6
172320		9				
172327		4				
172350		7				
172359		5				
172368		3				
172380		7				
172395		3				
172420		4				
172472		Orig.				
177502		3				
177526		Orig.				
177527		2				
177533		3				
177534		2				
177535		Orig.				
177536		Orig.				
177537		2				
177539		Orig.				

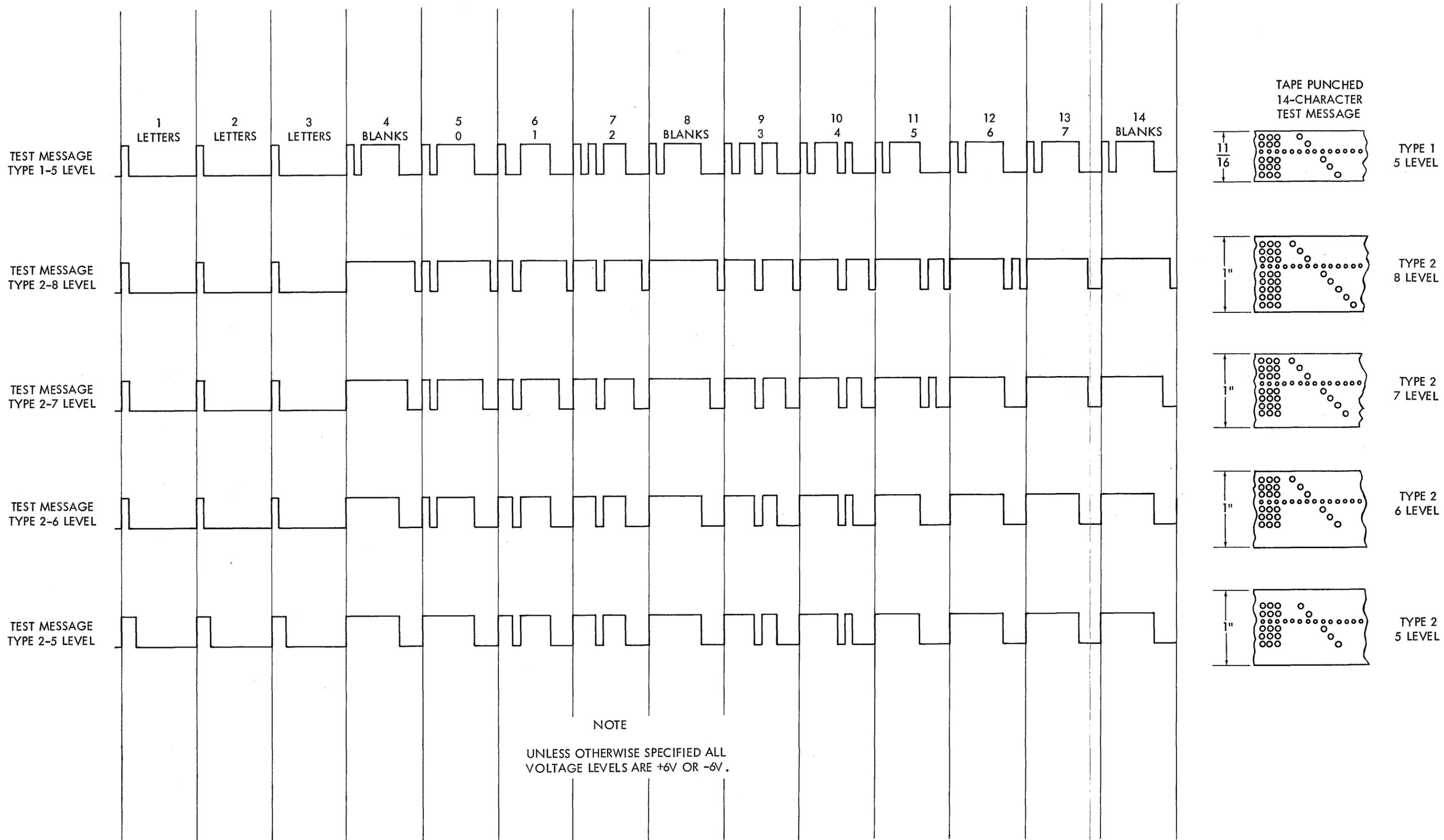


Figure 4 - Polar Output Signals (Sheet 1 of 2)

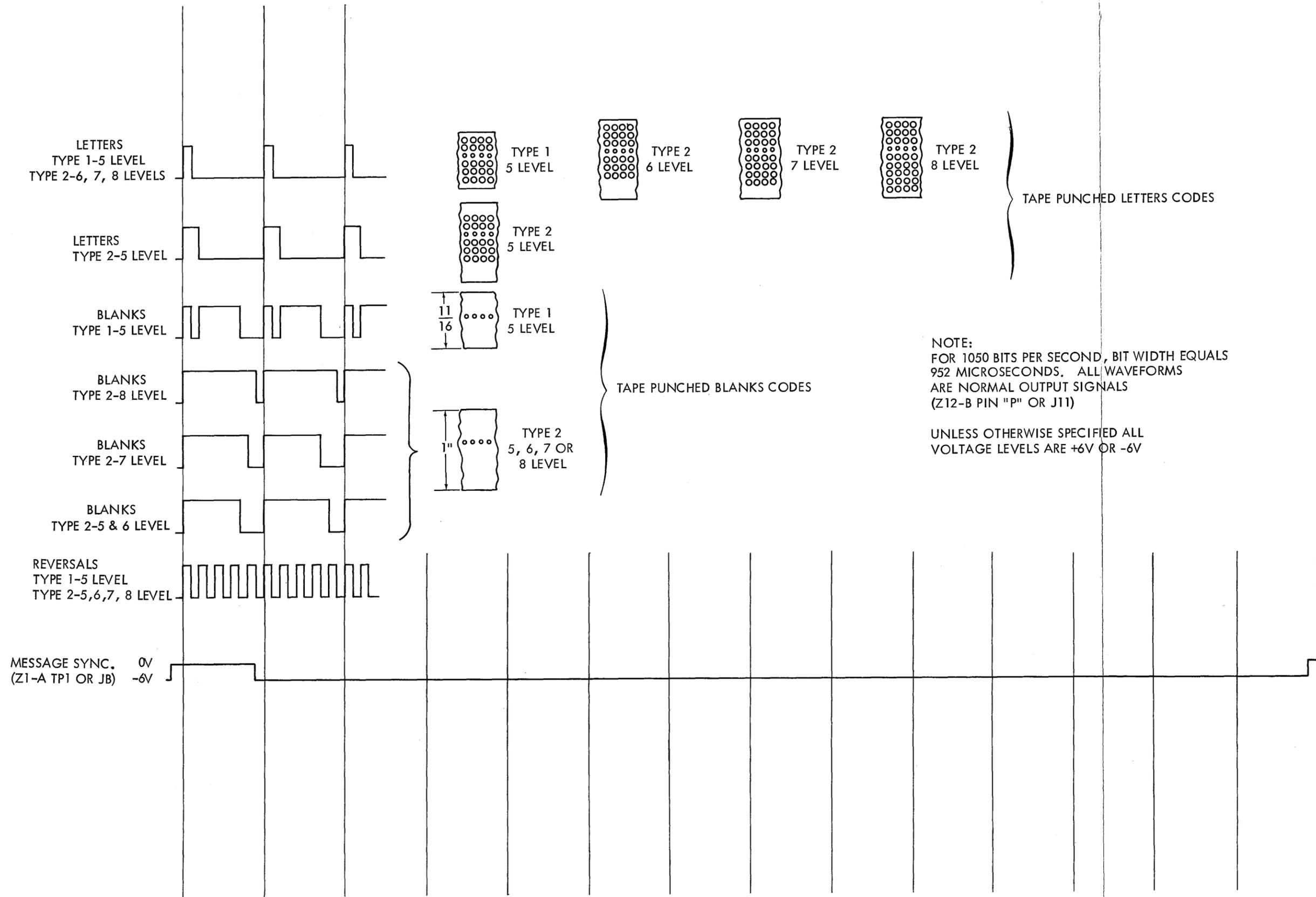


Figure 4 - Polar Output Signals (Sheet 2 of 2)

NOTES

- SWITCHES SHOWN IN POSITIONS AS FOLLOWS:
- S1 - DATA SPEED MODE SWITCH-TYPE 2-8 LEVEL
 - S2 - SIGNAL SWITCH TEST MESSAGE
 - 1 S3 - FUNCTION SWITCH-SEND
 - S4 - POWER SWITCH-OFF
 - S5 - DISTORTION SWITCH-MARK BIAS
- 2 CIRCLED NUMBERS INDICATE TEST POINTS ON CIRCUIT CARDS
- 3 FOR ACTUAL WIRING DIAGRAM REFER TO 4961 WD
- 4 Z - NUMBER DENOTES ELEMENT POSITION
EC - NUMBER DENOTES ETCHED CIRCUIT CARD NUMBER

Z ELEMENT	EC CARD
Z1	EC327
Z2	EC320
Z3	EC320
Z4	EC320
Z5	EC320
Z6	EC327
Z7	EC536
Z8	EC359
Z9	EC359
Z10	EC535
Z11	EC533
Z12	EC526
Z13	EC368
Z14	EC368
Z15	EC380
Z16	EC350
Z17	EC539
Z18	EC472
Z19	EC502
Z20	EC527
Z21	EC420
Z22	EC534
Z23	EC537
Z24	EC395

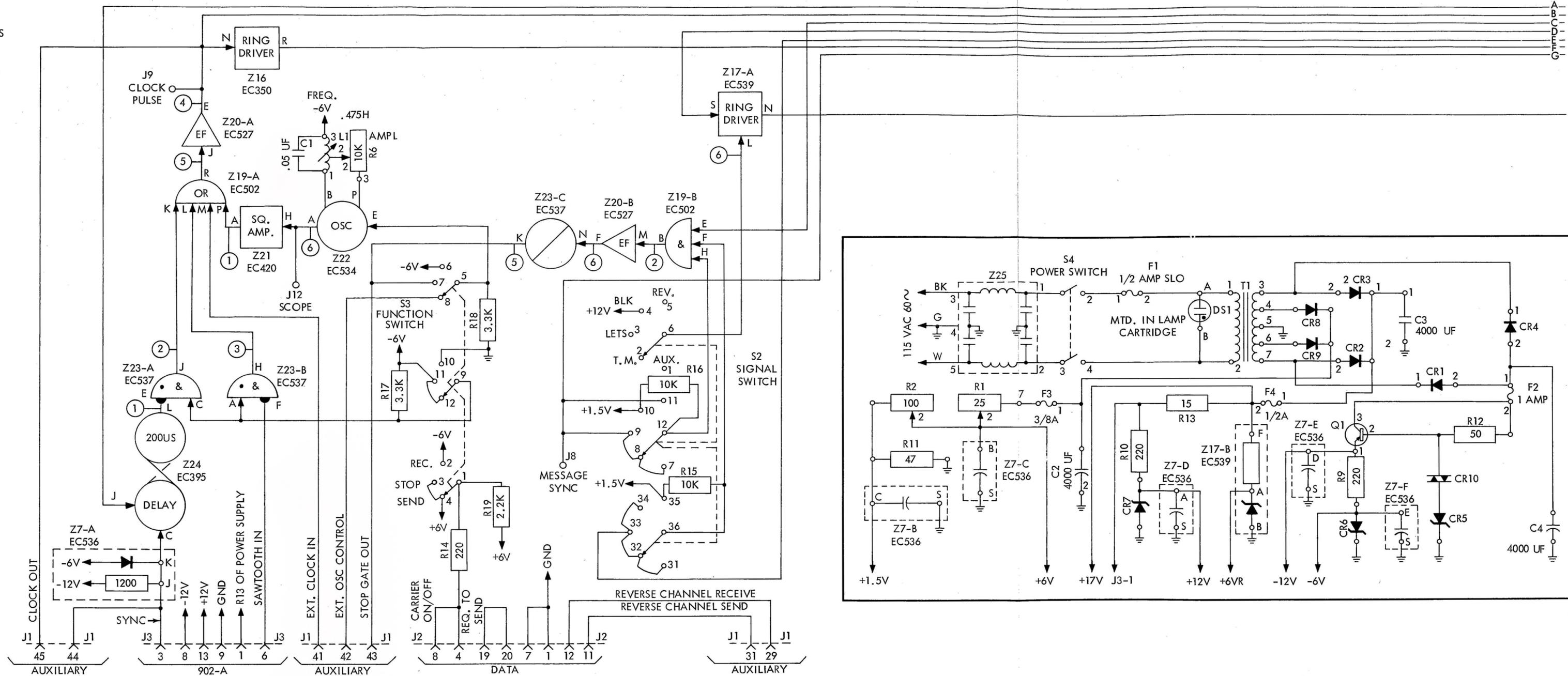


Figure 5 - Schematic Wiring Diagram, Data Test Set 905A & 905B (Sheet 1 of 3)

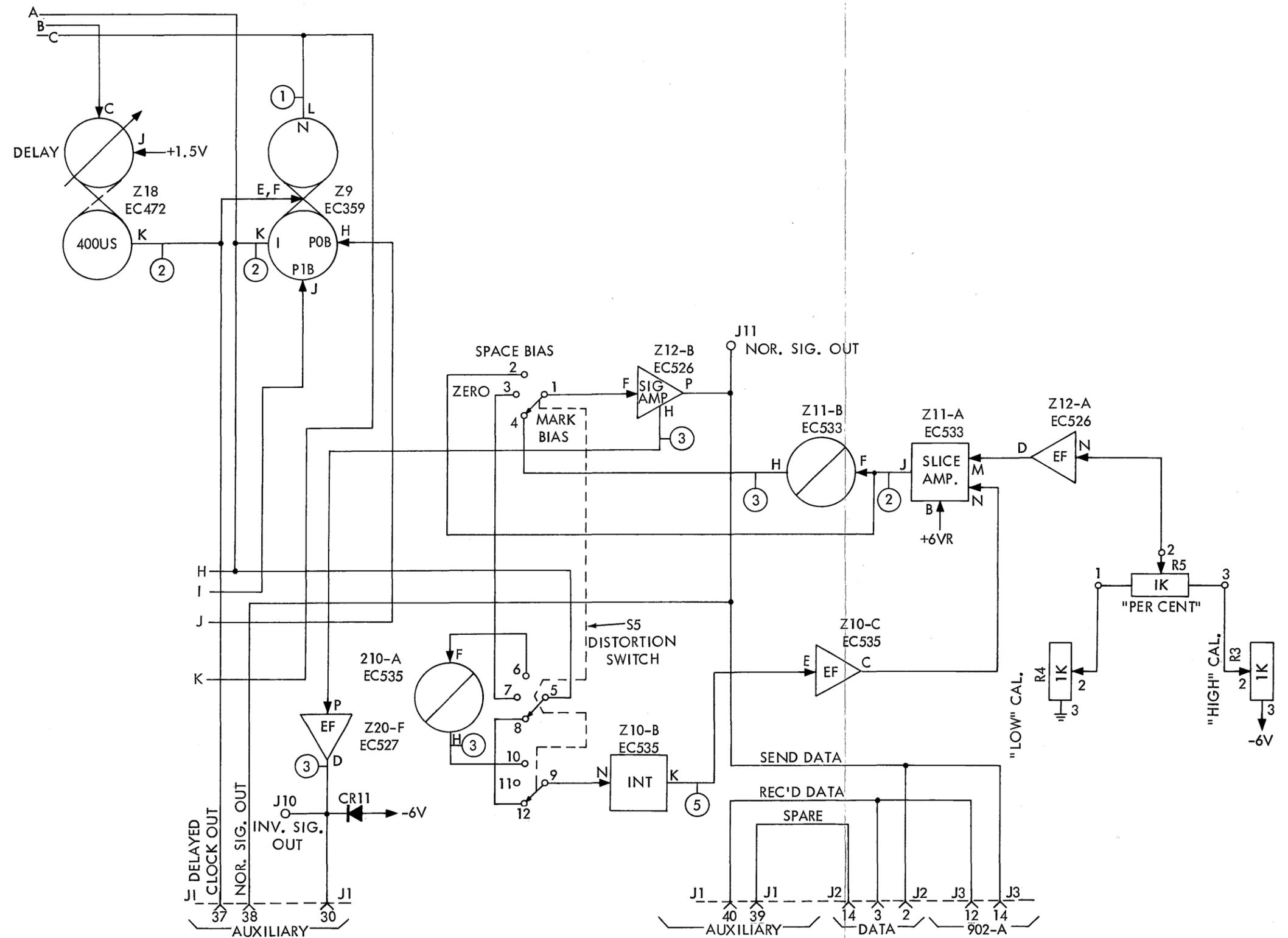


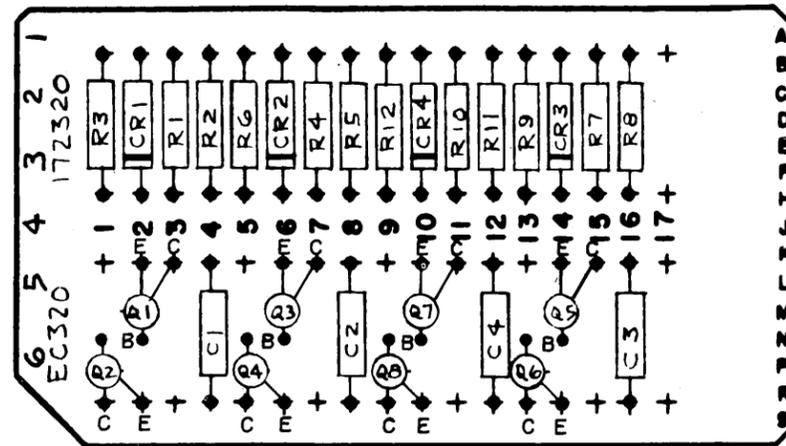
Figure 5 - Schematic Wiring Diagram, Data Test Set 905A & 905B (Sheet 3 of 3)

EC 320

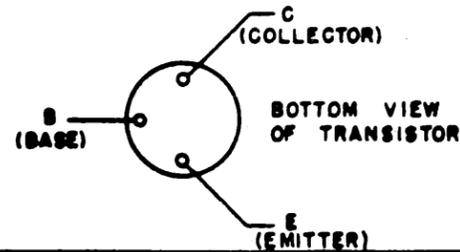
TRUNCATED-N DISTRIBUTOR

CIRCUIT BOARD EC 320

172320



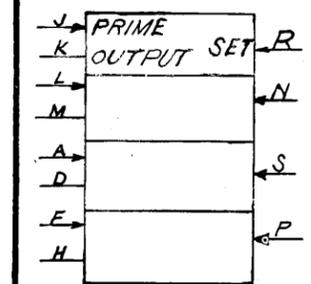
172074



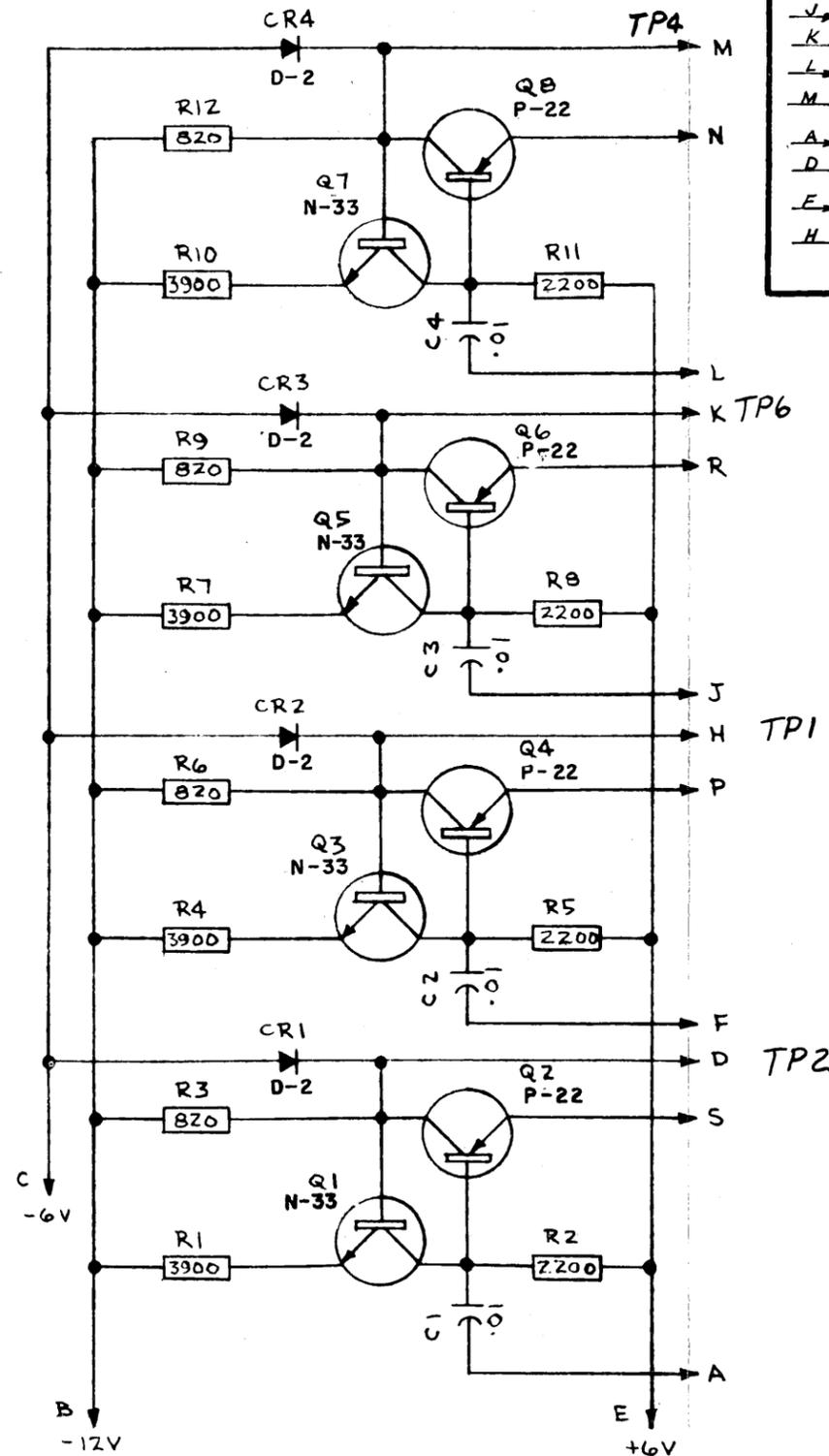
NOTE: REFER TO 5016 FOR MARKING INFORMATION

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
C1	137304	4	Capacitor, TUBULAR .01 MF	Priming
C2			Same as C1	"
C3			Same as C1	"
C4			Same as C1	"
CR1	177108	4	Diode D-2	Clamp
CR2			Same as CR1	"
CR3			Same as CR1	"
CR4			Same as CR1	"
R1	143667	4	Resistor, Fixed 3900 Ohms	Emitter Load
R2	129852	4	" " 2200 Ohms	Collector Load
R3	137139	4	" " 820 Ohms	" " "
R4			Same as R1	Emitter Load
R5			Same as R2	Collector Load
R6			Same as R3	" " "
R7			Same as R1	Emitter Load
R8			Same as R2	Collector Load
R9			Same as R3	" " "
R10			Same as R1	Emitter Load
R11			Same as R2	Collector Load
R12			Same as R3	" " "
Q1	144495	8	PAD, TRANSISTOR	
Q1	177106	4	Transistor N-33	Dxtr Element
Q2	177105	4	Transistor P-22	" " "
Q3			Same as Q1	" " "
Q4			Same as Q2	" " "
Q5			Same as Q1	" " "
Q6			Same as Q2	" " "
Q7			Same as Q1	" " "
Q8			Same as Q2	" " "
EC	172074	1	Circuit Card, Etched	

SYMBOLS



ISSUE	DATE	AUTH. NO.
2	8-24-59	H3-1116
3	9-8-59	H3-1139
4	11-16-59	H3-1291
5	11-27-60	H3-2019
6	3-22-61	69385
7	5-26-61	69892
8	1-4-62	72075
9	5-13-63	76845



NOTE: CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R E OF M

PROG. NO. 172320

DATE: 4-23-59

P.D. FILE NO. 70-A97/25AA

DRAWN R.S. CHKD. J. ENGR. AV. APPR. J.

TELETYPE CORPORATION

172320

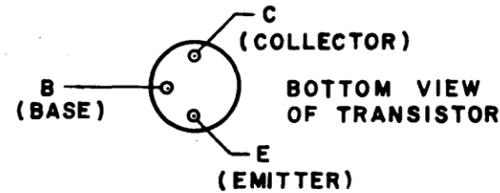
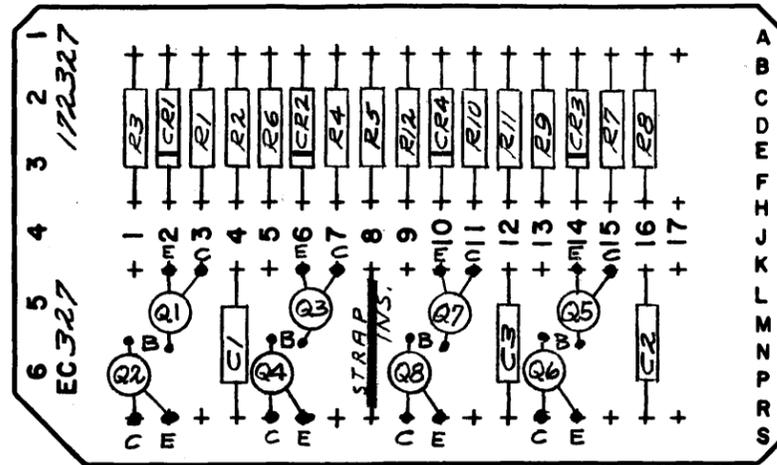
EC 327

172327

TRUNCATED-N DISTRIBUTOR
WITH RESET STOP ELEMENT

CIRCUIT BOARD EC 327

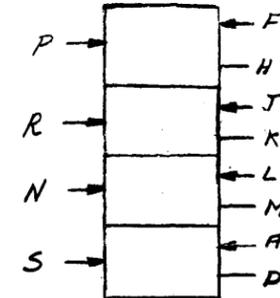
172327



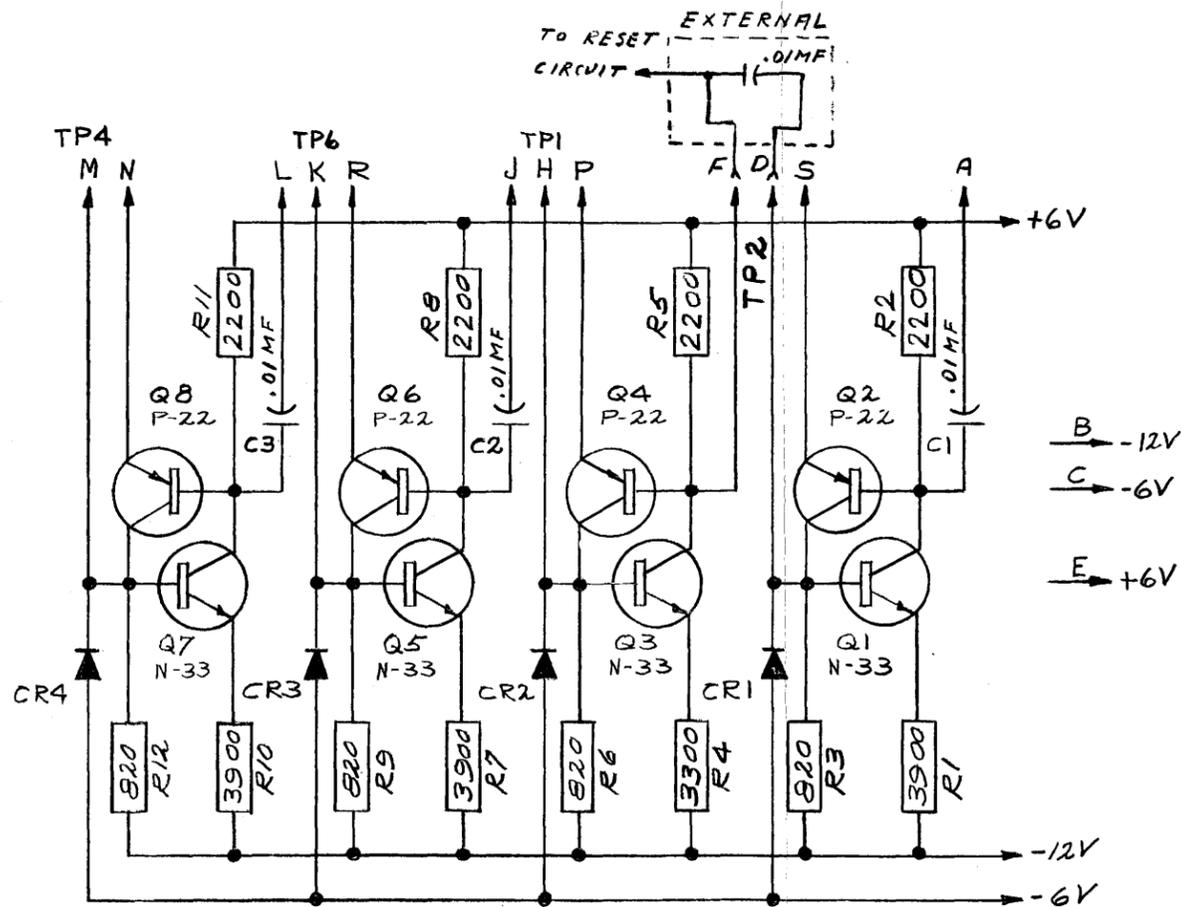
NOTE:
REFER TO 5016WD FOR MARKING
INFORMATION

REF DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
C1	137304	3	Capacitor, Tubular .01 MF	Priming	
C2			Same as C1	"	
C3			Same as C1	"	
CR1	177108	4	Diode, D-2	Clamp	
CR2			Same as CR1	"	
CR3			Same as CR1	"	
CR4			Same as CR1	"	
R1	143667	3	Resistor Fixed, 3900 ohms	Emitter Load	
R2	129852	4	" " 2200 "	Collector Load	
R3	137439	4	" " 820 "	" " "	
R4	129851	1	" " 3300 "	Emitter Load	
R5			Same as R2	Collector Load	
R6			Same as R3	" "	
R7			Same as R1	Emitter Load	
R8			Same as R2	Collector Load	
R9			Same as R3	" "	
R10			Same as R1	Emitter Load	
R11			Same as R2	Collector Load	
R12			Same as R3	" "	
	144138	31	Eyelets		
Q1	177106	4	Transistor N-33	DXTR Element	
Q2	177105	4	Transistor, P-22	" "	
Q3			Same as Q1	" "	
Q4			Same as Q2	" "	
Q5			Same as Q1	" "	
Q6			Same as Q2	" "	
Q7			Same as Q1	" "	
Q8			Same as Q2	" "	
EC	172074	1	Circuit Card, Etched		
		1	Strap, 24 AWG INSULATED WITH SLEEVE		
	144495	8	Pad, Transistor		

SYMBOLS



ISSUE	DATE	AUTH. NO.
2	12-26-62	75423
3	7-15-63	76006
4	4-23-65	76667



ALL DIODES D-2
ALL CAPACITORS .01 MF.

NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R E OF M

E-NUMBER

PROD. NO. 172327

DATE: 5-5-62

P.O. FILE NO. 1-A48/134.53A

DRAWN: SMV CHKD: M

ENG. JMG APPD. ROR

TELETYPE CORPORATION

172327

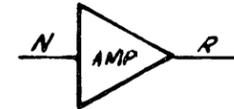
EC 350

CIRCUIT BOARD EC 350

172350

DISTRIBUTOR DRIVER

SYMBOLS

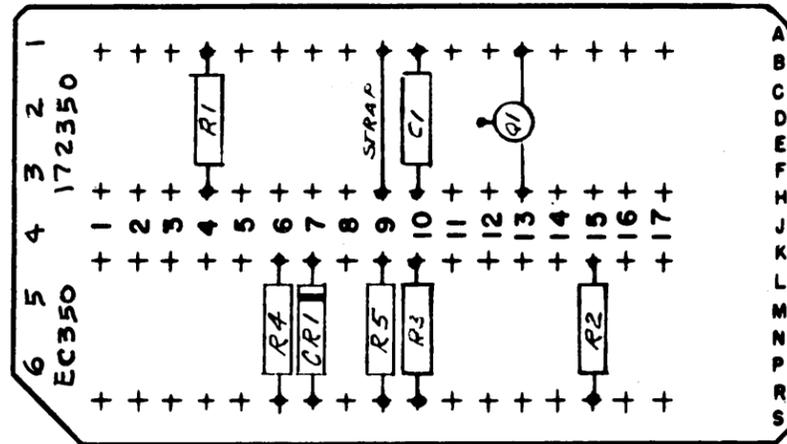


ISSUE	DATE	AUTH. NO.
2	8-6-59	HS-1082
3	9-8-59	HS-1139
4	10-28-59	HS-1238
5	11-13-59	HS-1285
6	11-23-59	HS-1314
7	5-26-61	69892

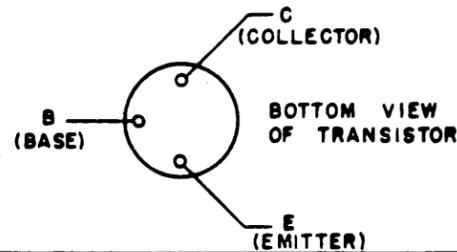
This circuit consists of a common emitter amplifier which provides voltage and current gain.

Q1 is normally saturated, since base current flows from ground, through R1 and the base-emitter junction of Q1, to +6V. Consequently the collector potential is normally +6 volts. R4 and R5 form a voltage divider which develops a voltage of approximately -4.5 volts at C1. Since the input applied to N is normally -6 V, CR1 is reversed biased 1.5 volts. Noise pulses having less than 1.5 volts amplitude are therefore inhibited.

A positive 6 volt pulse applied at the base, through CR1 and C1, drives Q1 into cut-off. A negative going pulse less than 10 micro seconds in duration therefore appears at the collector, which is applied through R2 to the associated distributor.

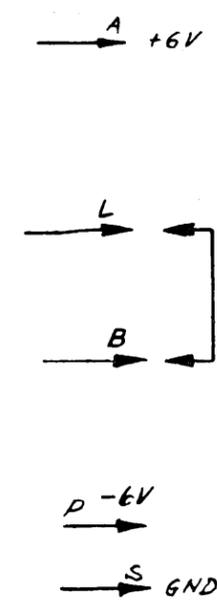
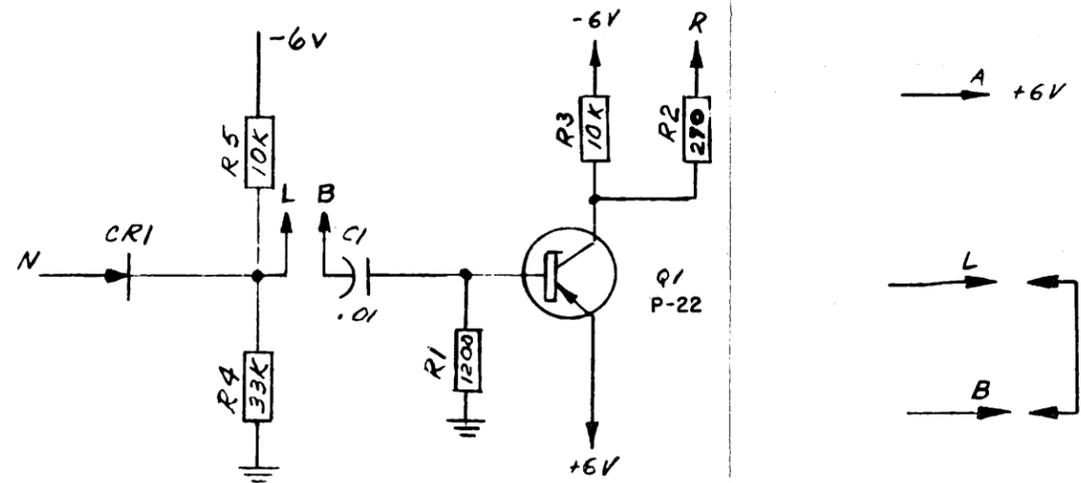


172065



NOTE: REFER TO 5016 WD FOR MARKING INFORMATION

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
C1	171566	1	Capacitor, Ceramic .01 MF	Coupling	
CR1	177108	1	Diode D-2	Coupling	
R1	137441	1	Resistor, Fixed 1200 Ohms	Bias	
R2	118725	1	" " 270 "	Output Limiting	
R3	118180	2	" " 10 K Ohms	Collector Load	
R4	118153	1	" " 33 K "	Voltage Divider	
Q1	177105	1	Transistor, P-22	Driver	
EC	172065	1	Circuit Card, Etched		
R5		1	SAME AS R3	Voltage Divider	
		1	STRAP 24 AWG BARE		
	144495	1	PAD, TRANSISTOR		



NOTE: CARD CONNECTIONS ARE REPRESENTED BY LETTERS

APPROVALS

D AND E OF M

E NUMBER

PROD. NO. 172350

DATE: 4-23-59

P.D. FILE NO. 20-A97/25A

DRAWN. VV CHKD.

ENG. 20 APPR.

TELETYPE CORPORATION

172350

EC 359

172359

CIRCUIT BOARD EC 359

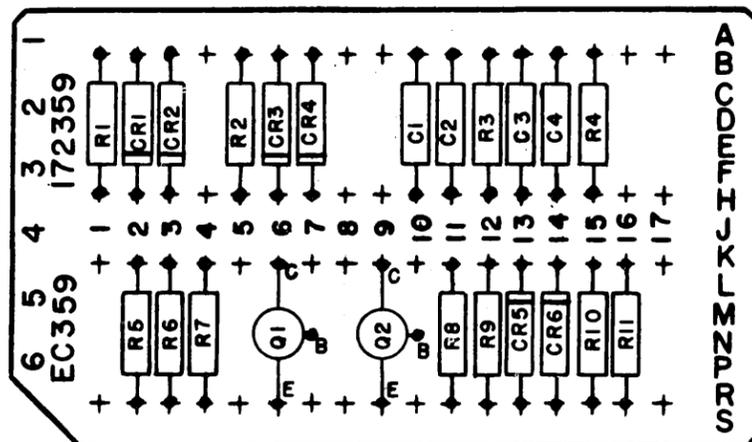
172359

FLIP-FLOP

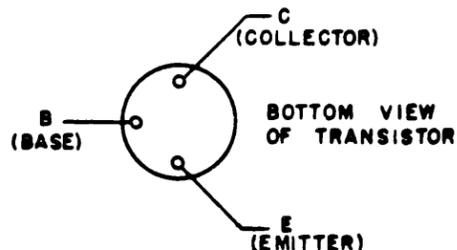
SYMBOLS



ISSUE	DATE	AUTH. NO.
2	9-8-59	HS-1139
3	10-28-59	HS-1238
4	5-26-61	69892
5	11-16-61	71626



172062



NOTE: REFER TO 5016WD FOR MARKING INFORMATION

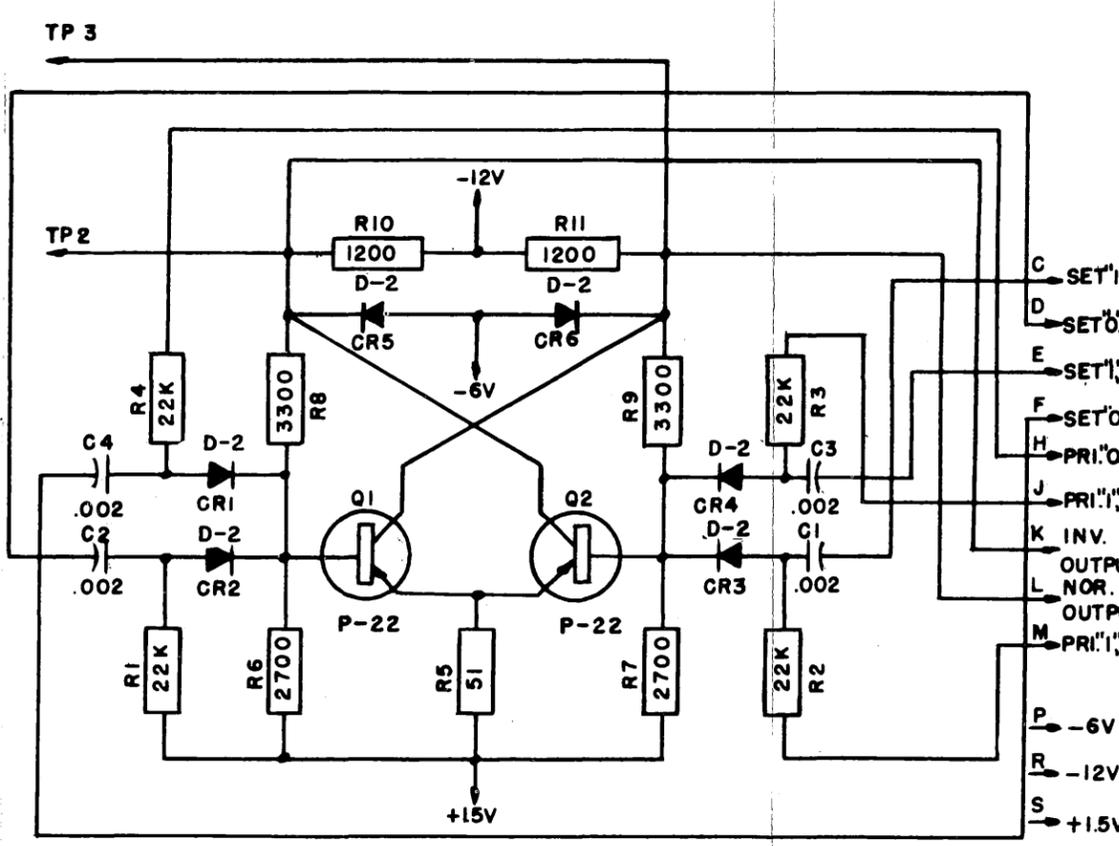
Static Description

The flip-flop employs two PNP junction transistors, so arranged that when one is conducting, the other is held in a cutoff condition. Q1 and Q2 are connected in a symmetrical circuit; each collector has a 1200 ohm load returned to a -12V supply. When either of the transistors is cutoff, collector current will drop to almost zero, and the OFF collector potential will be clamped to -6 volts by action of CR5 or CR6. When either transistor is ON, its collector potential will be approximately +1V. The OFF base will be at +1.23 volts; the common emitter point will be at +1.0 volts and the ON base will be at +.7 volts.

Operation

The circuit is normally driven by applying a positive 6 volts pulse through C1 and CR3, C2 and CR2, C3 and CR4, or C4 and CR1 to the base which is ON. This results in the ON stage turning OFF and the OFF stage turning ON. The flip flop may be driven by either of two pulses applied to each base. The positive pulses may be inhibited by returning R2, R3 and R4 to -6 volts. This prevents diodes CR1, CR3 and CR4 from conducting and coupling the pulse to the base of the corresponding transistor. The resistors R2, R3 and R4 must be returned to ground potential or +1.5V for the drive pulse to be passed by the corresponding diode.

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
C1	177332	4	Capacitor, Ceramic .002 mf		differentiating coupling
C2			Same as C1		" "
C3			Same as C1		" "
C4			Same as C1		" "
CR1	177108	6	Diode, D-2	OR gate with CR2	
CR2			Same as CR1	" " " CR1	
CR3			Same as CR1	" " " CR4	
CR4			Same as CR1	" " " CR3	
CR5			Diode, D-2	-6 volts clamp	
CR6			Same as CR5		
R1	118177	4	Resistor, Fixed 22K	C2 discharge	
R2			Same as R1	C1 discharge-inhibit gate	
R3			Same as R1	C3 discharge-inhibit gate	
R4			Same as R1	C4 " " " "	
R5	143656	1	Resistor, Fixed 51 Ohm	Common emitter bias	
R6	118144	2	Resistor, Fixed 2700 Ohm	Base bias	
R7			Same as R6		
R8	129851	2	Resistor, Fixed 3300 Ohm	Base current limiting	
R9			Same as R8		
R10	137441	2	Resistor, Fixed 1200 Ohm	collector load	
R11			Same as R10		
Q1	177195	2	Transistor, P-22	Flip-flop active element	
Q2			Same as Q1		
EC	172062	1	Circuit card, etched		
	144495	2	PAD, TRANSISTOR		



FLIP-FLOP

APPROVALS

D AND R E OF M

PROD. NO. 172359

DATE: 2-18-59

P.D. FILE NO.

DRAWN. G.J.M. CHKD.

ENG. R.J.R. APPD.

TELETYPE CORPORATION

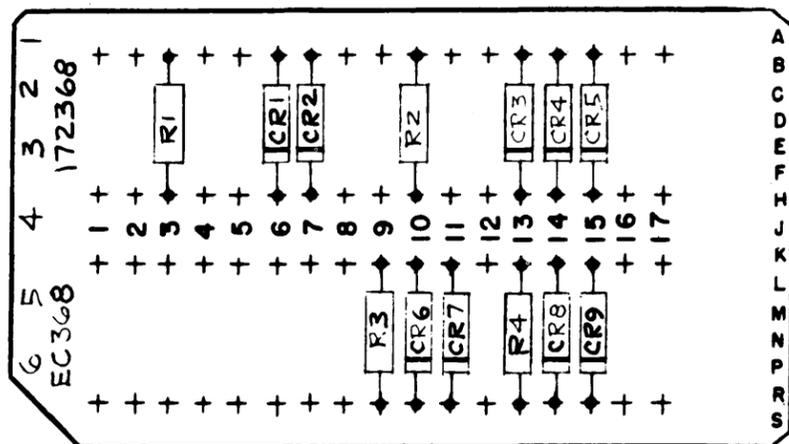
172359

EC 368

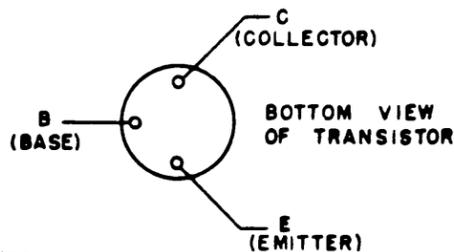
DIODE GATES

CIRCUIT BOARD EC 368

172368



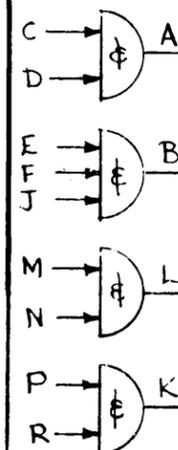
172066



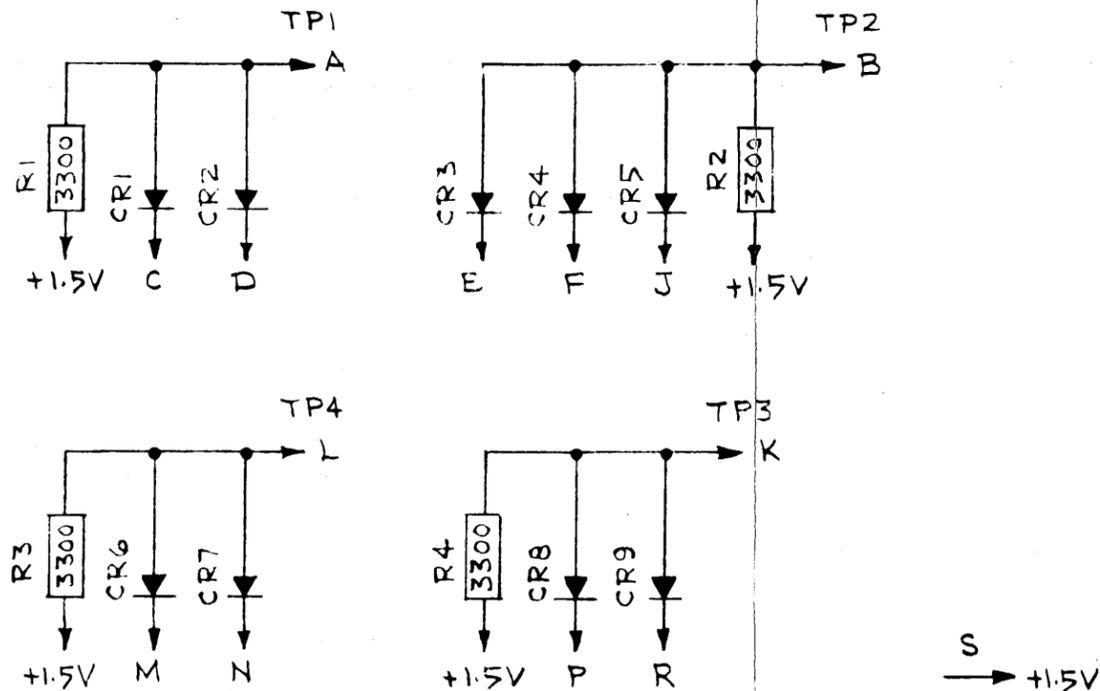
NOTE:
REFER TO 5016 WD FOR MARKING INFORMATION

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
CR1	177108	9	Diode, D-2		Gate
CR2			Same as CR1		"
CR3			Same as CR1		"
CR4			Same as CR1		"
CR5			Same as CR1		"
CR6			Same as CR1		"
CR7			Same as CR1		"
CR8			Same as CR1		"
CR9			SAME AS CR1		"
R1	129861	4	Resistor, Fixed 3300 Ohms		Bias Resistor
R2			Same as R1		"
R3			Same as R1		"
R4			Same as R1		"
EC	172066	1	Circuit Card, Etched		

SYMBOLS



ISSUE	DATE	AUTH. NO.
2	11-16-59	HS-1288
3	5-26-61	69892



ALL DIODES ARE D-2

NOTE:
CORD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND E OF M

E-NUMBER

PROD. NO. 172368

DATE: 9-25-59

P.D. FILE NO.

DRAWN. P.J. CHKD.

ENGD. J.F. APPD.

TELETYPE CORPORATION

172368

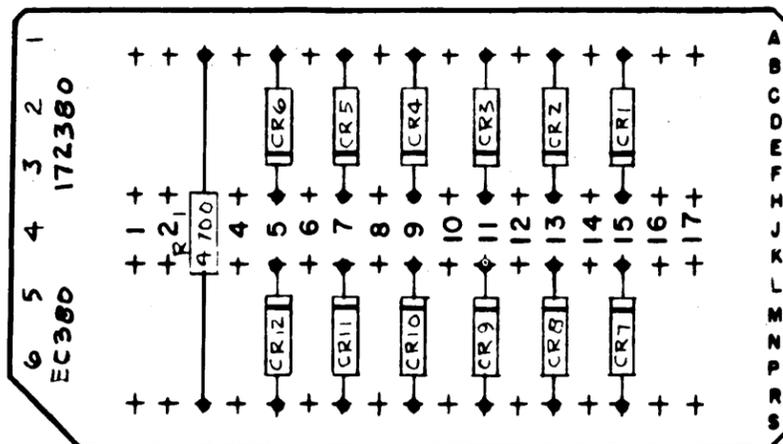
EC 380

DIODE GATE (12)

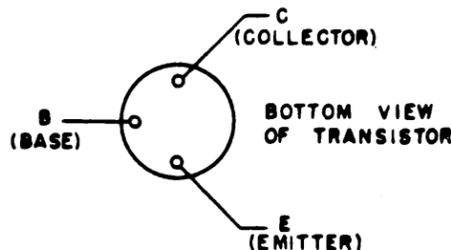
CIRCUIT BOARD EC 380

172380

172380



172070

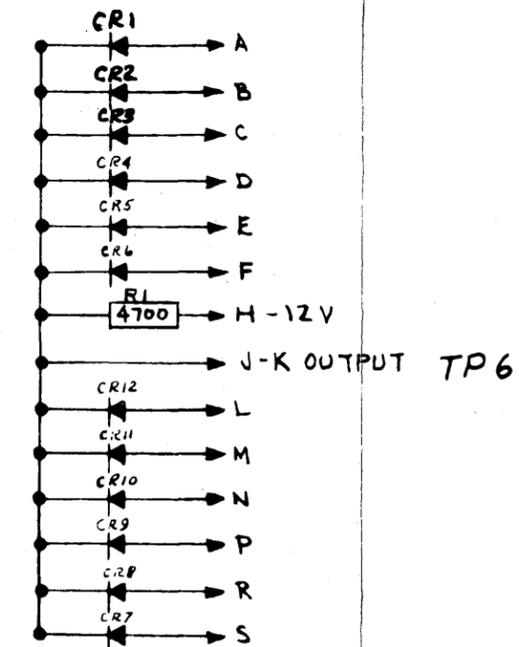
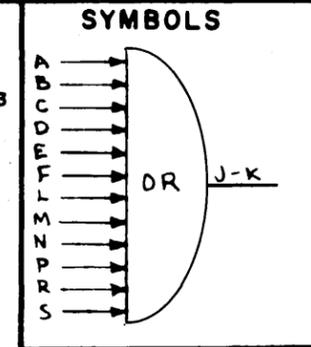


NOTE:
REFER TO 5016 WD FOR MARKING INFORMATION

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
CR1	177108	12	Diode, D-2	Gate
CR2			Same as CR1	"
CR3			" " "	"
CR4			" " "	"
CR5			" " "	"
CR6			" " "	"
CR7			" " "	"
CR8			" " "	"
CR9			" " "	"
CR10			" " "	"
CR11			" " "	"
CR12			" " "	"
R1	118146	1	Resistor, Fixed 4700 Ohms	Bias Resistor
EC	172070	1	Circuit Card, Etched	

This card consists of one "OR" gate. Diodes CR1 through CR12 together with R1 comprise the "OR" gate.

When 0 volts is applied to any or more of the inputs to an "OR" gate (A, B, C, D, E, F, H, L, M, N, P, R and S), the output of that gate is 0 volts (J and K). When negative 6 volts is applied to all the inputs of an "OR" gate, the output is negative 6 volts.



ALL DIODES D-2

NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

ISSUE	DATE	AUTH. NO.
2	7-31-59	HS-1072
3	9-8-59	HS-1139
4	10-28-59	HS-1238
5	5-26-61	69892
6	8-2-61	70507
7	4-9-63	AID33376

APPROVALS

D AND E OF M

E-NUMBER

PROD. NO. 172380

DATE:

P.D. FILE NO.

DRAWN. R. H. CHKD.

ENGD. J. B. APPD. J. A.

TELETYPE CORPORATION

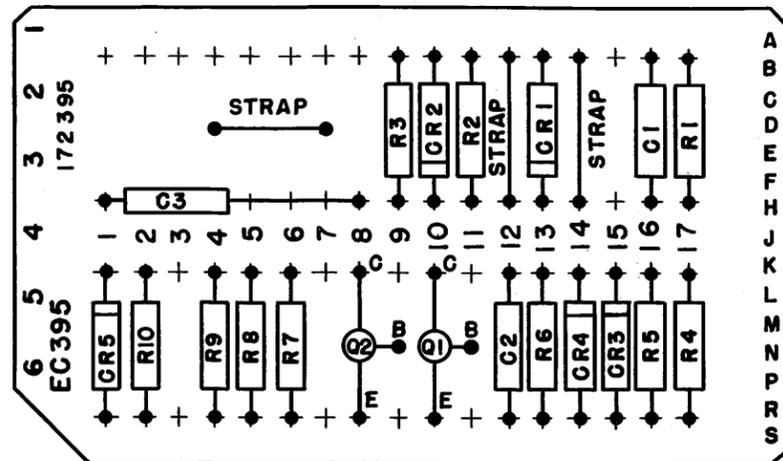
172380

EC 395
172395

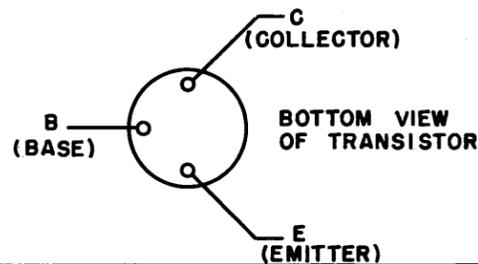
FIXED ONE - SHOT
200 μ S

CIRCUIT BOARD EC 395

172395

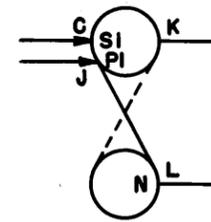


172063



NOTE
REFER TO 5016WD FOR MARKING INFORMATION

SYMBOLS



ISSUE	DATE	AUTH. NO.
2	5-26-61	69892
3	11-16-61	71626

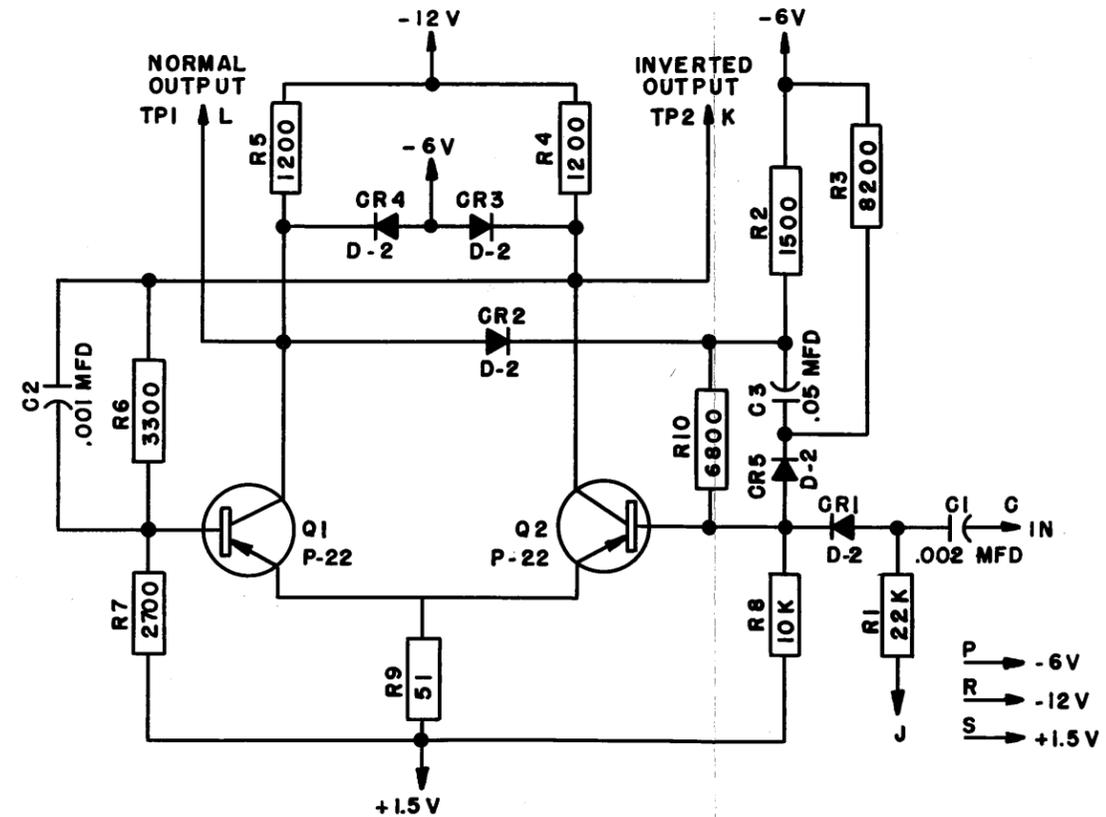
THE PURPOSE OF THIS CIRCUIT IS TO GENERATE A PULSE OF 200 MICROSECONDS IN WIDTH IN RESPONSE TO AN INPUT. NORMAL (POSITIVE GOING) AND INVERTED OUTPUTS ARE PROVIDED.

THE QUIESCENT STATE OF THIS CIRCUIT IS THAT Q2 IS SATURATED, RECEIVING ITS BIAS CURRENT PRIMARILY THROUGH R2 AND R10 CONNECTED IN PARALLEL WITH CR5, R3 TO -6V. THE COLLECTOR OF Q2 IS APPROXIMATELY 0V AND THE COLLECTOR OF Q1 IS -6V. Q1 IS MAINTAINED CUT-OFF BY CROSS COUPLING OF R6 AND R7 RETURNED TO +1.5V, HOLDING THE BASE POTENTIAL OF Q1 AT APPROXIMATELY +IV. THE COMMON EMITTER POTENTIAL IS 0V SINCE Q2 IS SATURATED.

CAPACITOR C1, R1 AND CR1 COMBINE TO FORM AN INHIBIT GATE, WHEREBY WHEN -6V IS APPLIED AT POINT J, INPUTS RECEIVED AT POINT G WILL FAIL TO TRIGGER THE CIRCUIT. CONVERSELY THE CIRCUIT IS ENABLED WHEN POINT J IS RETURNED TO 0V SINCE CR1 WILL NOW PASS POSITIVE GOING TRANSITIONS.

THE CIRCUIT IS TRIGGERED AS FOLLOWS: A POSITIVE TRANSITION APPLIED AT POINT C DRIVES Q2 INTO CUT-OFF WHICH, IN TURN, ALLOWS Q1 TO CONDUCT. AS THE COLLECTOR OF Q1 APPROACHES 0V, CR2 CONDUCTS CHARGING C3, AND MAINTAINING Q2 IN CUT-OFF. Q2 REMAINS CUT-OFF UNTIL C3 CAN DISCHARGE SUFFICIENTLY THROUGH R3 TO PERMIT CONDUCTION OF Q2. THE PERIOD OF CONDUCTION OF Q1 IS PRIMARILY DETERMINED BY THE SIZE OF C3 AND R3.

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
C1	177332	1	CAPACITOR, CARAMIC .002 MF		COUPLING
C2	177331	1	CAPACITOR, CARAMIC .001 MF		FEED BACK
C3	171680	1	CAPACITOR, CARAMIC .05 MF		TIMING
CR1	177108	5	DIODE, D-2		COUPLING
CR2			DIODE, D-2		GATE
CR3			SAME AS CR2		CLAMP
CR4			SAME AS CR2		CLAMP
CR5			SAME AS CR2		GATE
R1	118177	1	RESISTOR, FIXED 22K OHM		GATE
R2	137442	1	RESISTOR, FIXED 1500 OHM		BIAS
R3	137444	1	RESISTOR, FIXED 8200 OHM		TIMING
R4	137441	2	RESISTOR, FIXED 1200 OHM		COLLECTOR LOAD
R5			SAME AS R4		COLLECTOR LOAD
R6	129851	1	RESISTOR, FIXED 3300 OHM		FEED BACK
R7	118144	1	RESISTOR, FIXED 2700 OHM		BIAS
R8	118180	1	RESISTOR, FIXED 10K OHM		BIAS
R9	143656	1	RESISTOR, FIXED 51 OHM		COMMON EMITTER LOAD
R10	118147	1	RESISTOR, FIXED 6800 OHM		BIAS
Q1	177105	2	TRANSISTOR, P-22		SWITCH
Q2			SAME AS Q1		SWITCH
EC	172063	1	CIRCUIT CARD, ETCHED		
		3	STRAP 24AWG BARE		
	144495	2	PAD, TRANSISTOR		



NOTE
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R E OF M

E-NUMBER

PROD. NO. 172395

DATE: 3-1-60

P.D. FILE NO. 1-11.134AA

DRAWN. AB CHKD.

ENGD. E.H.P. APPD.

TELETYPE CORPORATION

172395

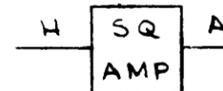
EC 420
172420

SQUARING AMPLIFIER

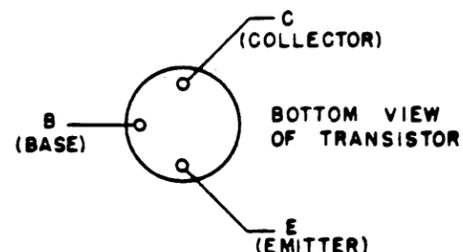
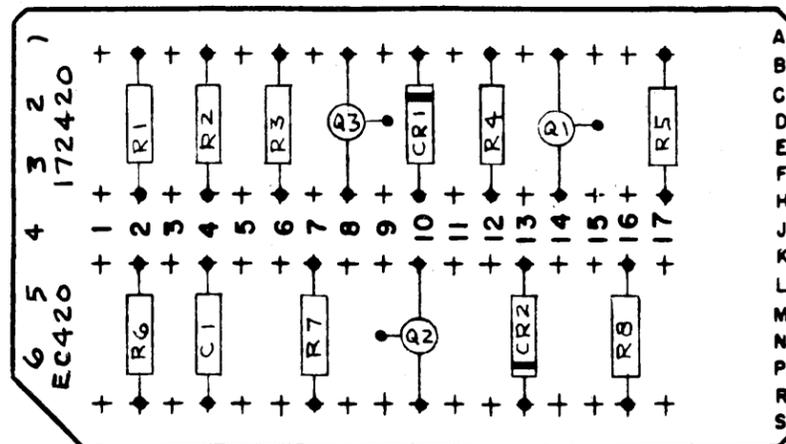
CIRCUIT BOARD EC 420

172420

SYMBOLS



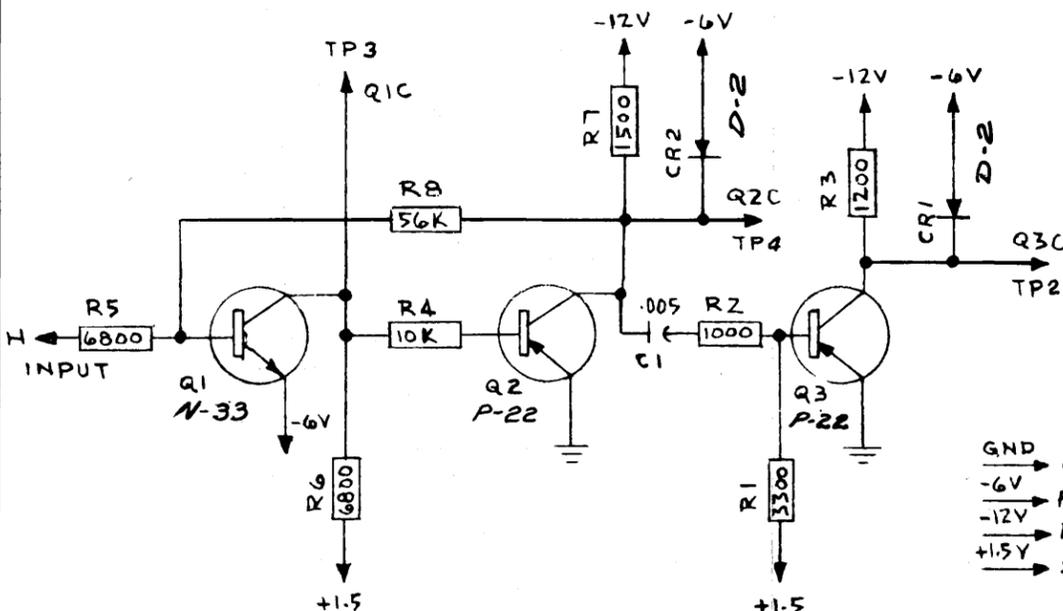
ISSUE	DATE	AUTH. NO.
2	9-19-60	HS-1905
3	5-26-61	69892
4	4-5-62	73031



NOTE

Refer to 5016WD for marking information.

REF. DESIGN.	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
C1	171567	1	Capacitor, Ceramic .005 Mf	Coupling
CR1	177108	2	Diode, D-2	Clamping Diode
CR2			Same as CR1	" "
R1	129851	1	Resistor, Fixed 3300 Ohms	Base Bias
R2	137440	1	" " 1000 "	" "
R3	137441	1	" " 1200 "	Collector Load
R4	118180	1	" " 10 K "	Base Bias
R5	118147	2	" " 6800 "	" "
R6			Same as R5	Collector Load
R7	137442	1	Resistor, Fixed 1500 Ohms	" "
R8	118156	1	" " 56 K Ohms	Feed Back Resistor
Q1	177106	1	Transistor, N-33	Amplifier
Q2	177105	2	Transistor, P-22	" "
Q3			Same as Q2	Amplifier
EC	172068	1	Circuit Card, Etched	
	144495	3	PAD, TRANSISTOR	



NOTE:

CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND E OF M

E-NUMBER

PROD. NO. 172420

DATE:

P.D. FILE NO.

DRAWN. P. H. CHKD.

ENGD. J. APPD. J.

TELETYPE CORPORATION

172420

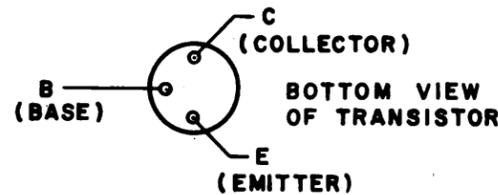
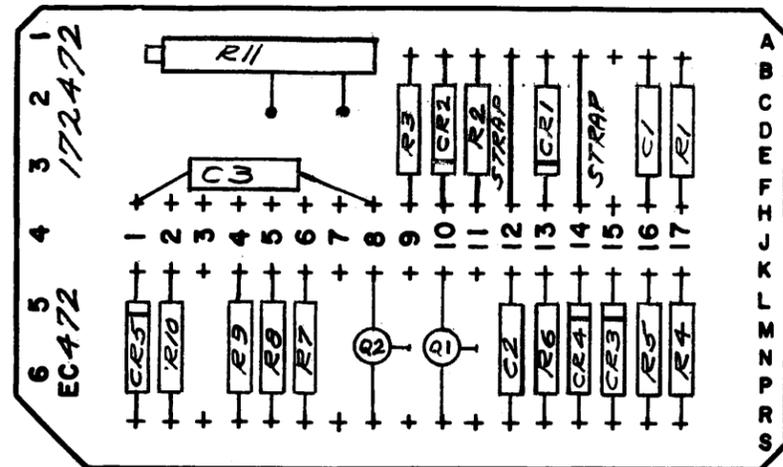
EC 472

172472

VARIABLE ONE-SHOT
300 TO 700 μSEC.

CIRCUIT BOARD EC 472

172472



NOTE:
REFER TO 5016WD FOR MARKING
INFORMATION

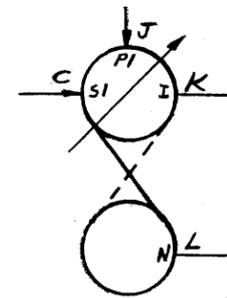
The purpose of this circuit is to generate a pulse of known width in the range of 0.3 to 0.7 milliseconds in response to an input. Normal (positive going) and inverted outputs are provided.

The quiescent state of this circuit is that Q2 is saturated, receiving its bias current primarily through R2 and R10 connected in parallel with CR5, R3 and R11 to -6 V. The collector of Q2 is approximately at zero volts and the collector of Q1 is -6 V. Q1 is maintained cut-off by cross coupling resistor R6 and resistor R7 returned to +1.5 V, holding the base potential of Q1 at approximately +1 V. The common emitter potential is zero volts since Q2 is saturated.

Capacitor C1, R1 and CR1 combine to form an inhibit gate, whereby when -6 V is applied at point J, inputs received at point C will fail to trigger the circuit. Conversely the circuit is enabled when point J is returned to 0 V since CR1 will now pass positive going transitions.

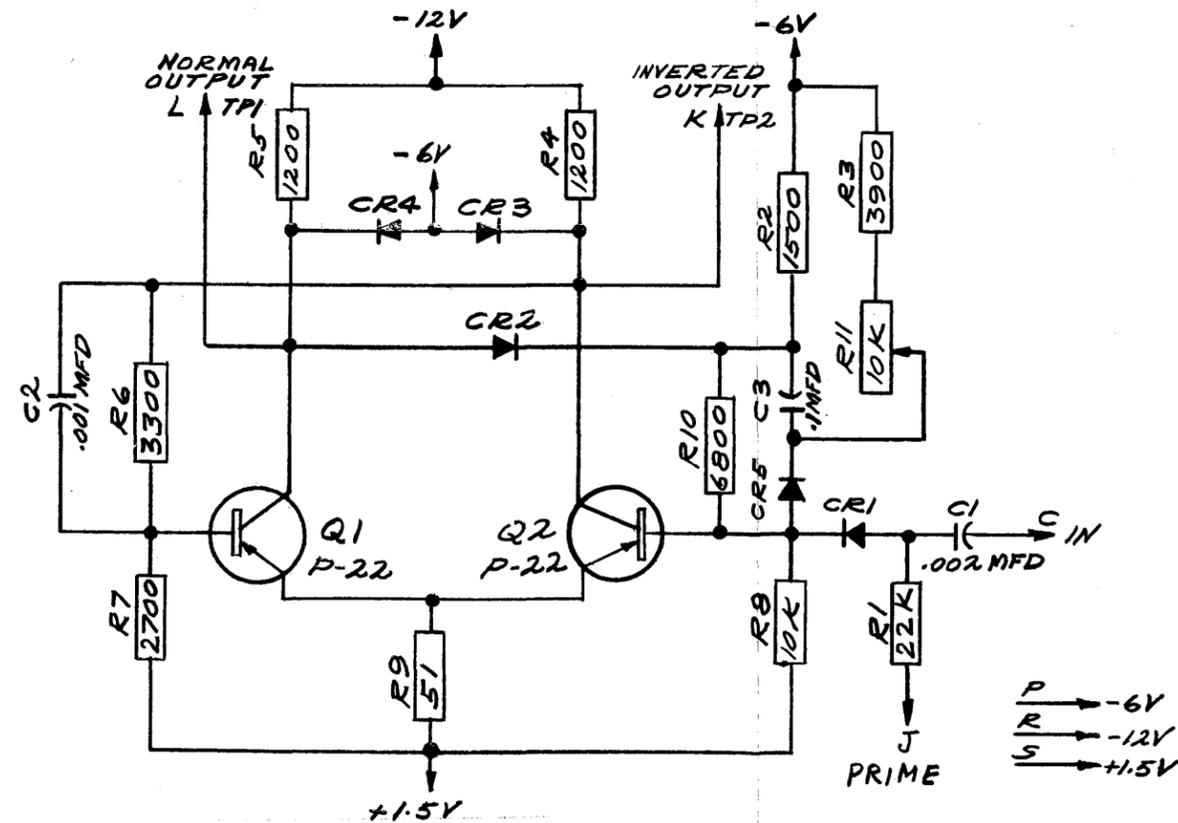
The circuit is triggered as follows: A positive transition applied at point C drives Q2 into cut-off which, in turn, allows Q1 to conduct. As the collector of Q1 approaches 0 V, CR2 conducts charging C3, and maintaining Q2 in cut-off. Q2 remains cut-off until C3 can discharge sufficiently through variable resistor R11 and R3 to permit conduction of Q2. The period of conduction of Q1 is primarily determined by the size of C3, R3 and the setting of R11.

SYMBOLS



ISSUE	DATE	AUTH. NO.

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING	FUNCTION
C1	177332	1	Capacitor, Ceramic .002 MF	Coupling	
C2	177331	1	" " .001 MF	Feed Back	
C3	171436	1	Capacitor, Mylar .1 MF	Timing	
CR1	177108	5	Diode, D-2	Coupling	
CR2			Same as CR1	Gate	
CR3			Same as CR1	Clamp	
CR4			Same as CR1	"	
CR5			Same as CR1	Gate	
R1	118177	1	Resistor, Fixed 22K ohms	Gate	
R2	137442	1	" " 1500 "	Bias	
R3	143667	1	" " 3900 "	Timing	
R4	137441	2	" " 1200 "	Collector Load	
R5			Same as R4	"	
R6	129851	1	Resistor, Fixed 3300 ohms	Feed Back	
R7	118144	1	" " 2700 "	Bias	
R8	118180	1	" " 10K "	"	
R9	143656	1	" " 51 "	Common Emitter Load	
R10	118147	1	" " 6800 "	Bias	
R11	171565	1	Resistor, Variable 10K ohms	Timing	
Q1	177105	2	Transistor, P-22	Switch	
Q2			Same as Q1	"	
EC	172063	1	Circuit Card, Etched		
	1178	2	Screw .437 - 2 x 56 Fil.		
	110446	2	Nut 2 x 56 Hex.		
		2	Strap 24 AWG. Bare		
	144495	2	Pad, Transistor		



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

E-NUMBER

PROD. NO. 172472

DATE: 5-3-62

P.D. FILE NO. 1-A148/34.54

DRAWN: JMG

CHKD: JMG

ENGD: JMG

APPD: JMG

TELETYPE CORPORATION

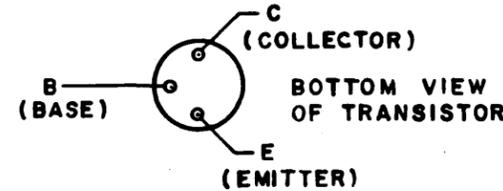
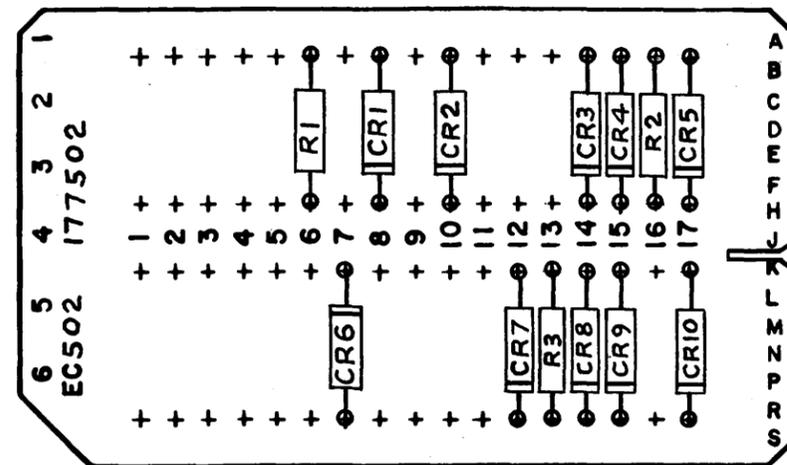
172472

EC 502
177502

DIODE GATES

CIRCUIT BOARD EC502

177502

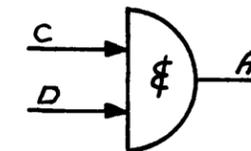
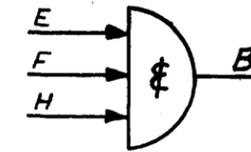
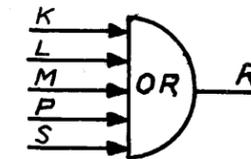


177499

NOTE:
REFER TO 5016WD FOR MARKING
INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
CR1	177108	10	Diode D2	Gate
CR2			Same as CR1	"
CR3			" " "	"
CR4			" " "	"
CR5			" " "	"
CR6			" " "	"
CR7			" " "	"
CR8			" " "	"
CR9			" " "	"
CR10			" " "	"
R1	118180	2	Resistor, Fixed 10K ohms	Bias Resistor
R2			Same as R1	" "
R3	129851	1	Resistor Fixed 3300 ohms	" "
EC	177499	1	Circuit Card, Etched	

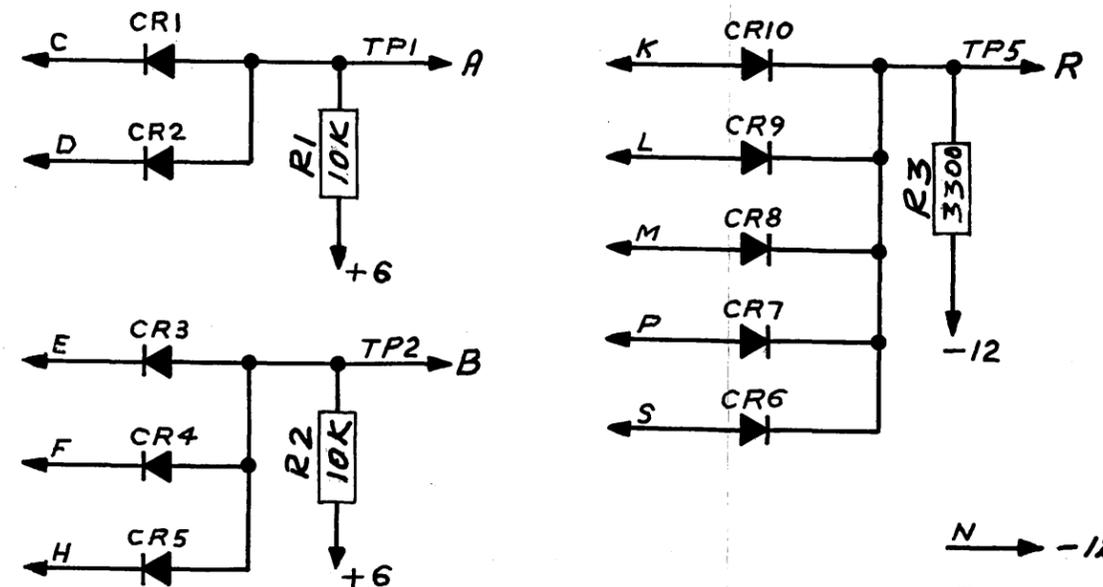
SYMBOLS



This card consists of one "OR" gate and two "AND" gates. Diodes CR6 through CR10 combine together with R3 to form a five input "OR" gate. CR1 and CR2 combine with R1 to form a two input "AND" gate while CR3, CR4 and CR5 combine with R2 to form a three input "OR" gate.

When 0 volts is applied to all of the inputs of an "AND" gate (C and D), the output (A) will be 0 volts. When -6 volts is applied to any of the inputs, the output will be -6 volts.

When -6 volts is applied to all of the inputs of an "OR" gate (K,L,M,P or S) the output (R) will be -6 volts. When 0 volts is applied to any of the inputs, the output will be 0 volts.



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

ISSUE	DATE	AUTH NO
2	10-31-61	71472
3	10-23-63	77918

APPROVALS	
D AND R <i>[Signature]</i>	E OF M <i>[Signature]</i>
E-NUMBER	
PROD. NO. 177502	
DATE: 1-11-61	
PD. FILE NO 24-A25/134AA	
DRAWN <i>[Signature]</i>	CHKD <i>[Signature]</i>
ENGD <i>[Signature]</i>	APPD <i>[Signature]</i>
TELETYPE CORPORATION	
177502	

R3

EC 526

177526

OUTPUT AMPLIFIER
EMITTER FOLLOWER

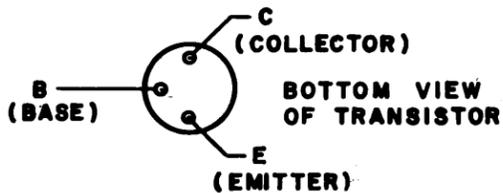
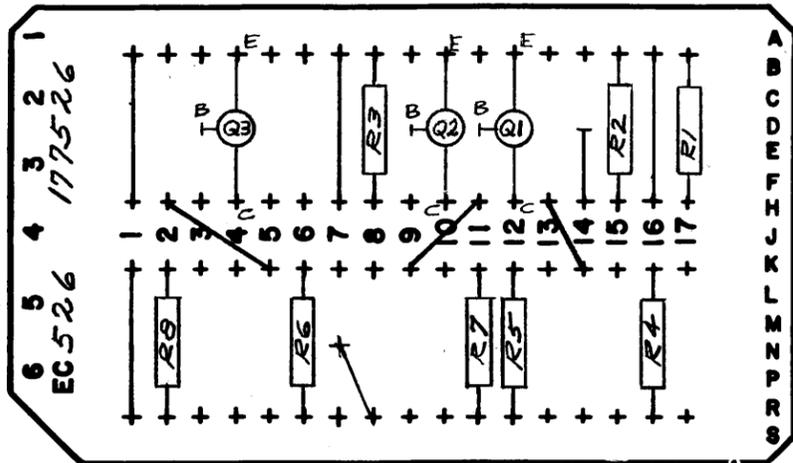
CIRCUIT BOARD EC 526

177526

SYMBOLS



ISSUE	DATE	AUTH. NO.



NOTE:
REFER TO 5016WD FOR MARKING INFORMATION

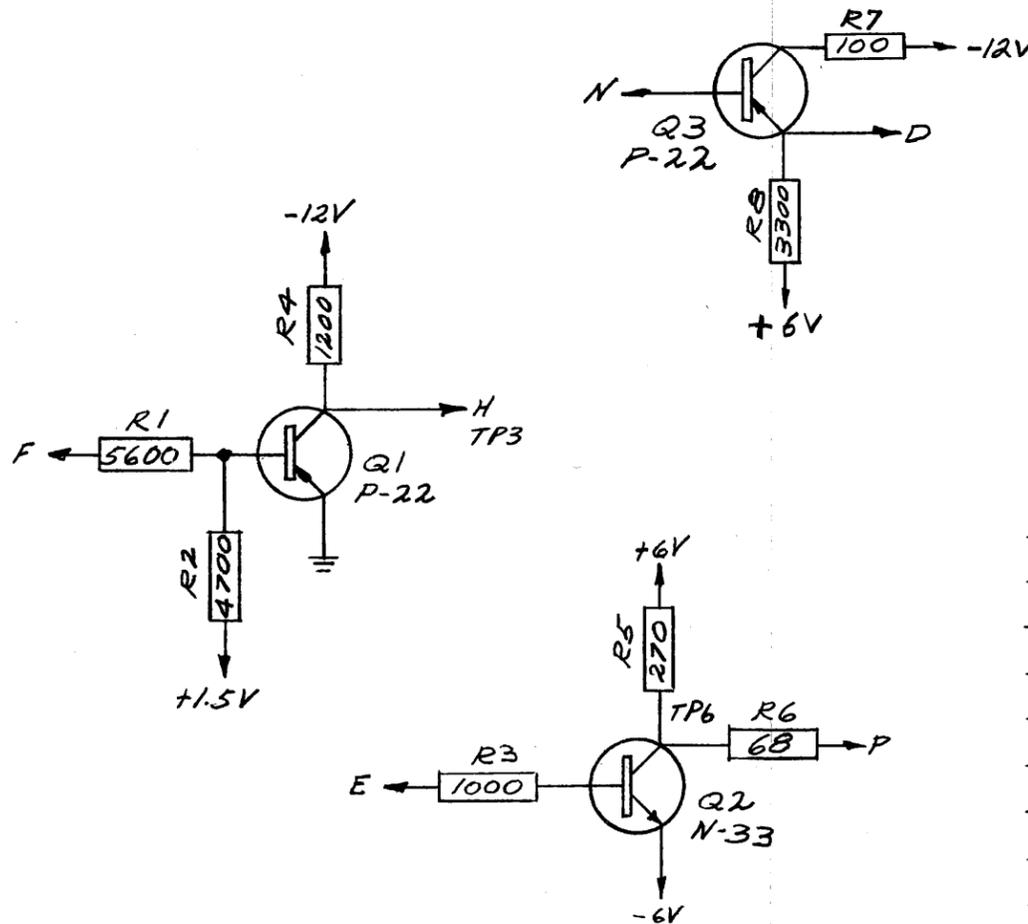
REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	118186	1	Resistor Fixed 5600 ohms	Base Resistor
R2	118146	1	" " 4700 "	Bias
R3	137440	1	" " 1000 "	Base Resistor
R4	137447	1	" " 1200 "	Collector Load
R5	118725	1	" " 270 "	" "
R6	137601	1	" " 68 "	Output Limiting
R7	137438	1	" " 100 "	Collector Limiting
R8	129851	1	" " 3300 "	Emitter Load
Q1	177105	2	Transistor P-22	Switch
Q2	177106	1	" N-33	Switch
Q3			Same as Q1	Amplifier
EC	172067	1	Circuit Card, Etched	
		9	Straps 24 AWG. Bare	
	144495	3	Pad, Transistor	

This card basically consists of two common emitter amplifiers plus one emitter follower.

The output of Q1 is connected to the input of Q2 by means of a strap in the connector between points E and H.

Q1 and Q2 are both cut-off with 0 volts applied at point F. R1 and R2 returned to +1.5 V reverse bias Q1 approximately +.75 V. Q2 is held cut-off by -12 V collector potential of Q1. The output at point F is therefore +6 V. With -6 V applied at point F, Q1 conducts, which in turn drives Q2 into conduction. The output at P therefore becomes -6 V.

Q3 the emitter follower provides high current gain with no signal inversion. The output potential of the emitter follower at D follows the input potential at N.



- A → GND.
 - B → +1.5V
 - C → -6V
 - E →
 - H →
 - M →
 - D →
 - R → -12V
 - S → +6V
- STRAPS

NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R	E OF M
<i>[Signature]</i>	<i>[Signature]</i>

E-NUMBER

PROD. NO. 177526

DATE: 8-FEB-62

P.D. FILE NO.

DRAWN. SW

ENG. JMG

TELETYPE CORPORATION

177526

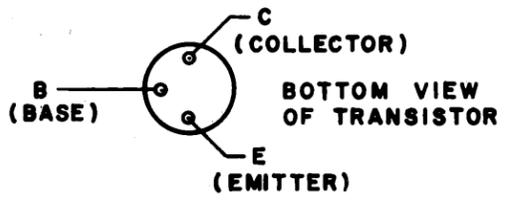
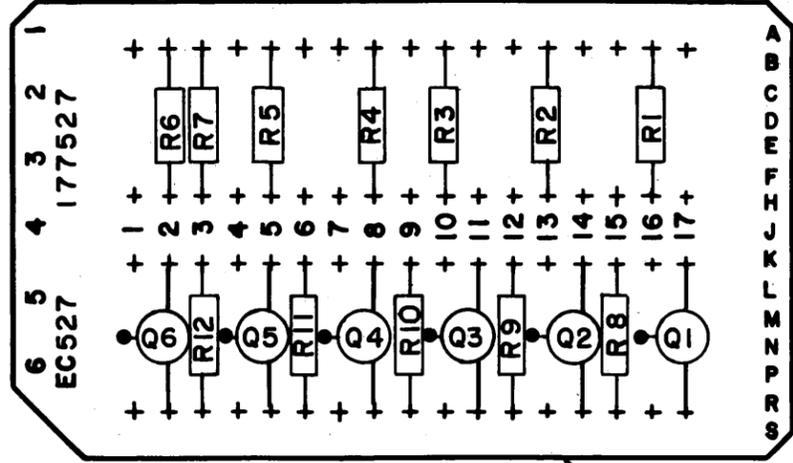
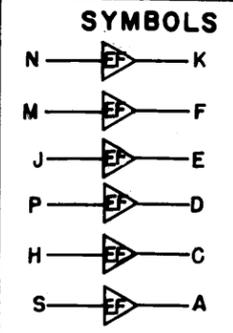
EC527
177527

NPN EMITTER FOLLOWER (6)

CIRCUIT BOARD EC527

177527

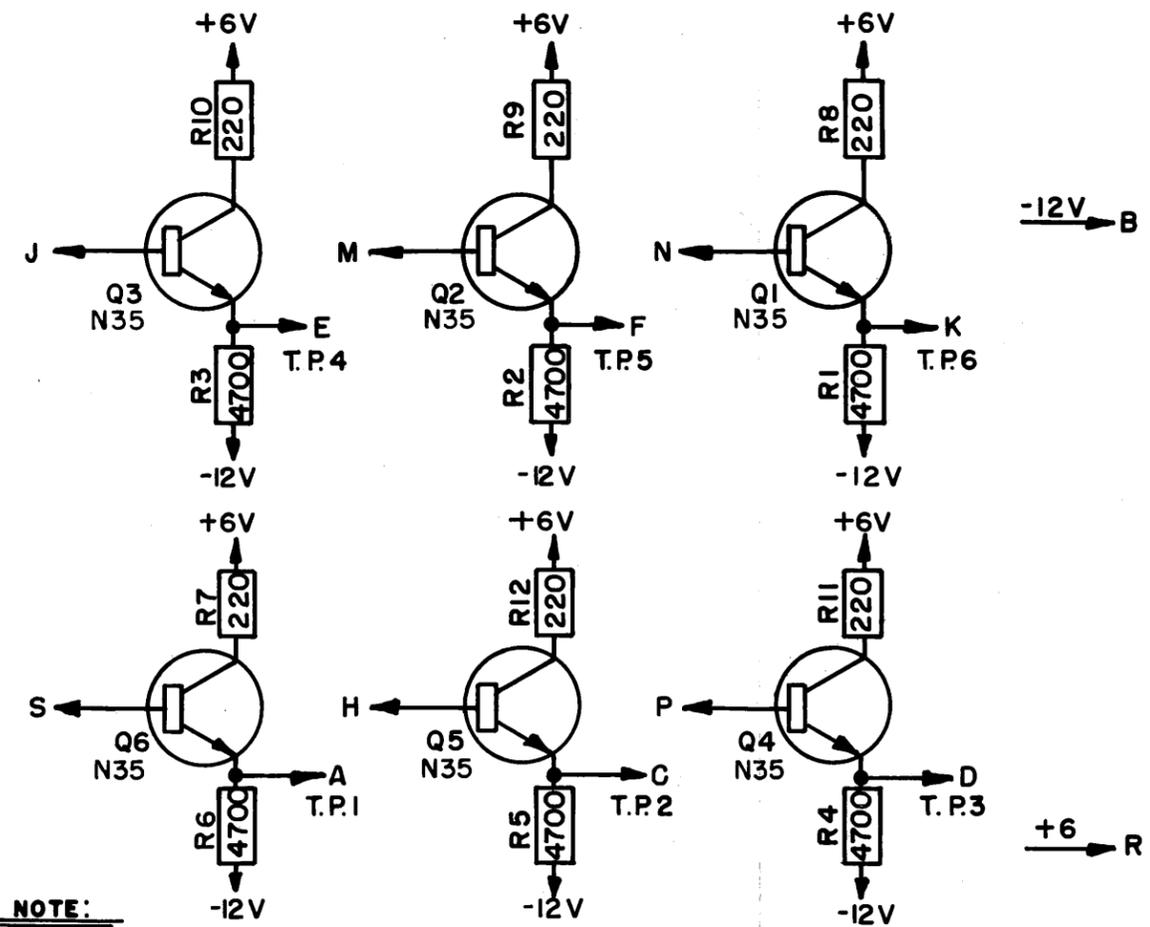
ISSUE	DATE	AUTH. NO.
2	1-7-63	75582



NOTE:
REFER TO 5016WD FOR MARKING INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	118146	6	Resistor Fixed 4700 ohms	Emitter Load
R2	"	"	" " " "	" "
R3	"	"	" " " "	" "
R4	"	"	" " " "	" "
R5	"	"	" " " "	" "
R6	"	"	" " " "	" "
R7	118724	6	Resistor, Fixed 220 ohms	Collector Load
R8	"	"	" " " "	" "
R9	"	"	" " " "	" "
R10	"	"	" " " "	" "
R11	"	"	" " " "	" "
R12	"	"	" " " "	" "
Q1	193134	6	Transistor (NPN) N35	Emitter Follower
Q2	"	"	" " " "	" "
Q3	"	"	" " " "	" "
Q4	"	"	" " " "	" "
Q5	"	"	" " " "	" "
Q6	"	"	" " " "	" "
EC	144138	19	EYELETS	
EC	172076	1	Circuit Card, Etched	
RM	60263		Sleeving as required	
RM	144495	6	Pad, Transistor	

This card consists of six medium power emitter followers used to provide current gain with no inversion or change in the input signal level. With zero volts applied at the base, zero volts appears at the emitter. With -6 V applied, -6 V appears at the emitter. The NPN Emitter follower is used to provide low output impedance (high current gain) on the positive going voltage transition (-6 to 0 volts.)



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R	E OF M
<i>[Signature]</i>	<i>[Signature]</i>
E-NUMBER	
PROD. NO. 177527	
DATE: 2-21-61	
P.D. FILE NO.	
DRAWN: E.E.	CHKD: <i>[Signature]</i>
ENGD: C.U.R.	APPD: <i>[Signature]</i>
TELETYPE CORPORATION	
177527	

R3

EC 533

177533

CIRCUIT BOARD EC 533

177533

1. INVERTER & SLICING AMPLIFIER.

This card consists of two independent circuits. One is an inverter, the other is a slicing amplifier.

Q1, the inverter, has reverse bias applied at the base through R2, holding Q2 cut-off with 0V signal applied. With a negative 6 volt signal applied at F, Q1 is driven into saturation, causing the collector potential to rise (-6 volts to 0) for the duration of the input signal. Q1 collector is clamped to -6 volts by CR1 when in cut-off.

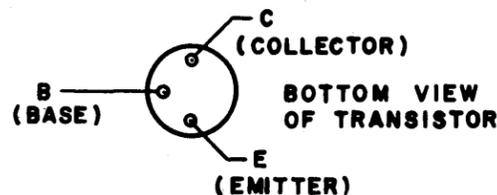
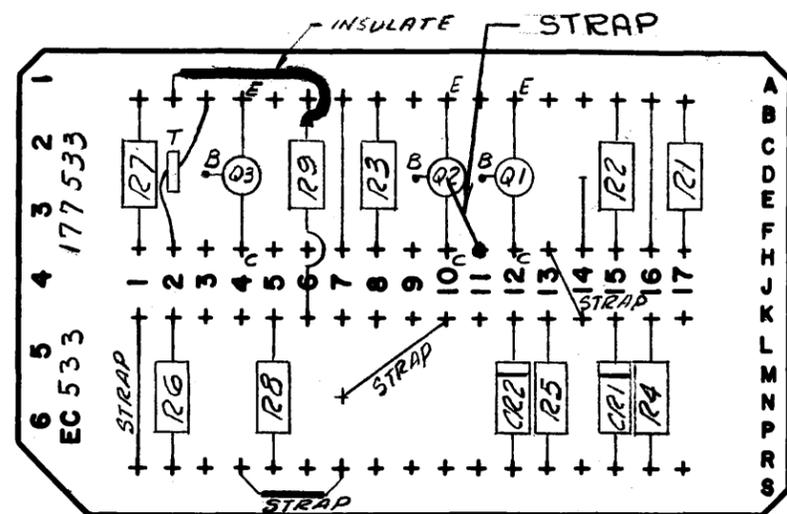
The slicing amplifier basically is a voltage sensitive switch. The bias voltage at point M determines the slicing or switching level. This bias voltage will normally vary between -1 volt and -5 volts from an external source. With point N approximately 0.5 volts more positive than the bias voltage at M, Q3 is biased into saturation. Its collector goes from +6 volts to approximately the bias voltage at M plus 0.5 volts. With point N approximately equal to the bias voltage, Q3 is biased into cut-off. Its collector returns to +6 volts.

With Q3 in saturation Q2 is biased into saturation through R3. Q2 collector goes to zero volts. With Q3 in cut-off Q2 is biased into cut-off. Q2 collector is clamped to -6 volts through CR2. Current through resistor R9 produces positive feedback in order to improve rise time of Q3. R8 and thermistor T are used to temperature stabilize switching level.

SYMBOLS

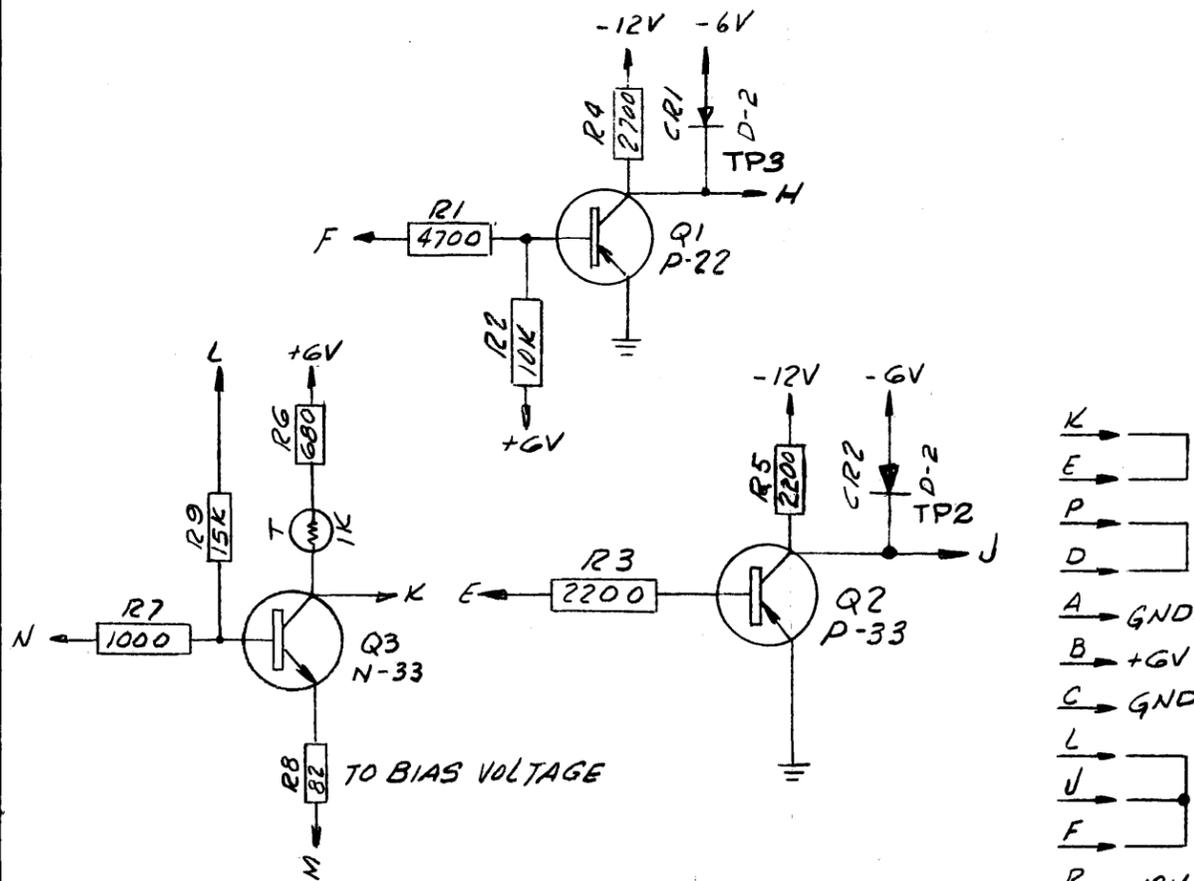


ISSUE	DATE	AUTH. NO.
2	7-2-62	7561004
3	8-13-62	74214



NOTE:
REFER TO 5016WD FOR MARKING INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	118146	1	Resistor Fixed 4700 Ohms	Base Resistor
R2	118180	1	" " 10K "	Bias Resistor
R3	129852	1	" " 2200 "	Base Resistor
R4	118144	2	" " 2700 "	Collector Load
R5			Same as R4	" "
R6	129850	1	Res. Fixed 680 "	" "
R7	137440	1	" " 1000 "	Base Resistor
Q1	177105	2	Transistor P-22	Amplifier
Q2			Same as Q1	"
Q3	177106	1	Transistor N-33	"
CR1	177108	2	Diode D-2	Clamp
CR2			Same as CR1	"
T	146738	1	Thermistor 1000 Ohms	Collector Load
		7	Strap 24 Awg. Bare	
		1	" " " Insulated	
	144495	3	Pad Transistor	
R8	146739	1	Fixed Resistor 82 Ohms	Bias Resistor
R9	118150	1	" " 15K "	Feedback Resistor
EC	172067	1	Circuit Card, Etched	



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS.
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D. AMER E OF M

E-NUMBER

PROD. NO. 177533

DATE: 3-17-62

P.D. FILE NO. 1-AVR/134.53A

DRAWN. N.G. CHKD. J.M.G.

ENG. J.M.G. APPD. J.M.G.

TELETYPE CORPORATION

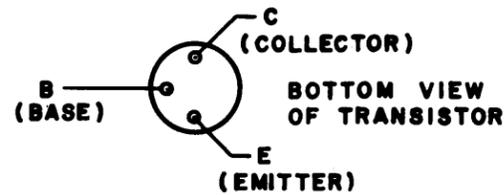
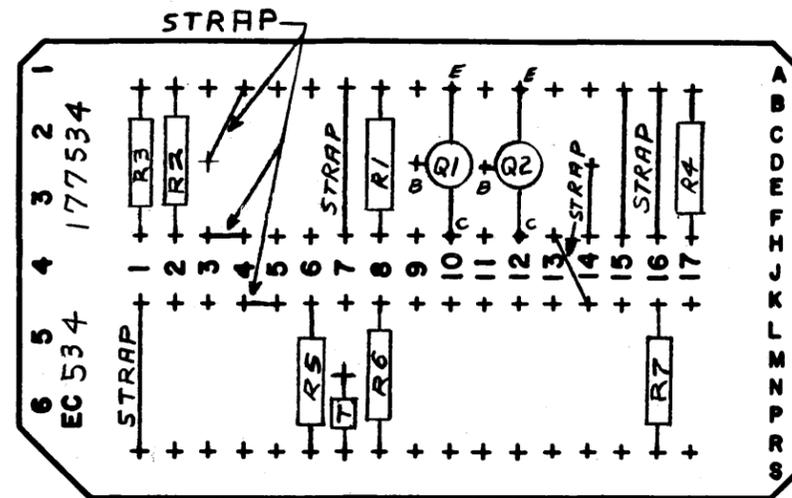
177533

EC 534

177534

CIRCUIT BOARD EC 534

177534



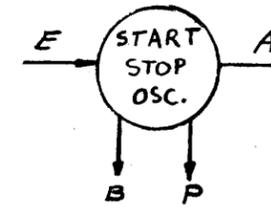
NOTE:
REFER TO 5016WD FOR MARKING
INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	118147	1	Resistor Fixed 6800 OHMS	Base Resistance
R2	129856	2	Resistor Fixed 150 OHMS	Emitter Bias
R3			Same as R2	Emitter Bias
R4	137442	1	Resistor Fixed 1500 OHMS	Collector Load
R5	137441	1	Resistor Fixed 1200 OHMS	Feed Back Shunt
R6	129852	1	Resistor Fixed 2200 OHMS	Emitter Load
R7	118724	1	Resistor Fixed 220 OHMS	Collector Load
T	171830	1	Thermistor 10K OHMS	Feed Back
Q1	172105	1	Transistor P-22	Switch
Q2	193135	1	" P-24	Amplifier
EC	172067	1	Circuit card, Etched	
		9	Strap 24AWG Bare	
	144495	2	Pad. Transistor	

START-STOP OSCILLATOR
1050 BAUD

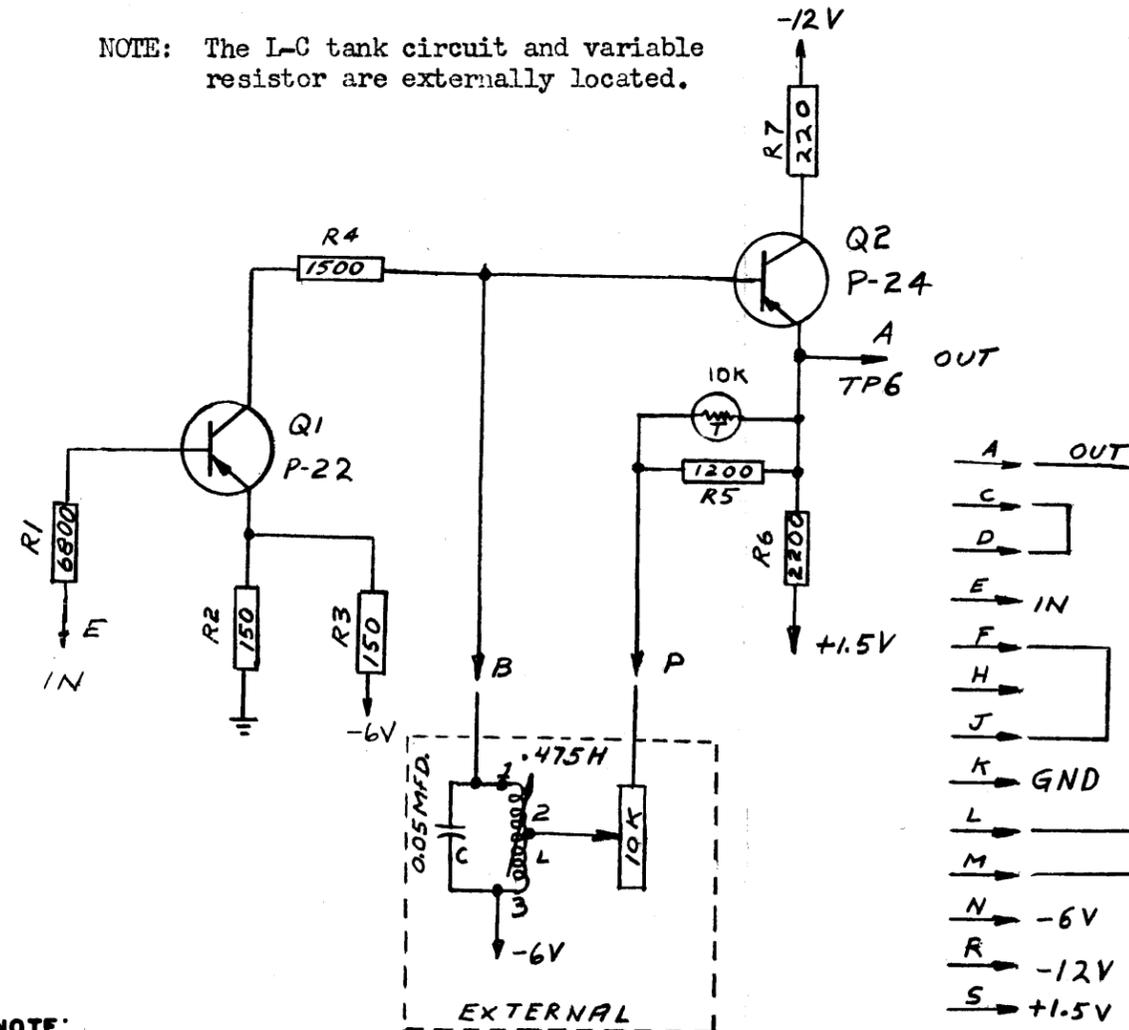
This circuit is a sine wave oscillator arranged to start or stop under control of an external signal and to oscillate at a frequency of 1050 CPS. The negative half cycle of the sine wave is produced immediately when 0 volts (ground) is applied at the input. The circuit employs two PNP junction transistors. Q2 is connected as a Hartley oscillator with the output taken from its emitter. Q1 is arranged to act as a damper across the resonant circuit L-C when the input is at -6V, Q1 is conducting and the circuit is prevented from oscillating due to low resistance in parallel with resonant circuit (its Q down to a value too low to sustain oscillation). In the static condition the output is clamped at approximately -5.5V. During sustained oscillation the output swings between -1 and -9 volts. A small range of adjustment for frequency is provided by means of a variable inductor. A variable resistor is provided to adjust feedback current to sustain oscillation.

SYMBOLS



ISSUE	DATE	AUTH. NO.
2	1-4-63	75569

NOTE: The L-C tank circuit and variable resistor are externally located.



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

DESIGNER	E OF M
<i>[Signature]</i>	

E-NUMBER
PROD. NO. 177534

DATE: 3-17-62
P.D. FILE NO. 1-A148/134.534

DRAWN. JG | CHKD. *[Signature]*
ENG. J. M. GAPPD. *[Signature]*

TELETYPE CORPORATION

177534

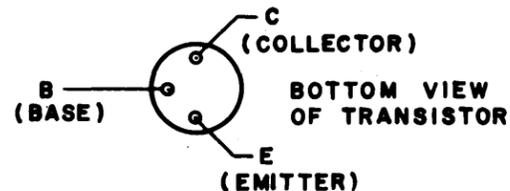
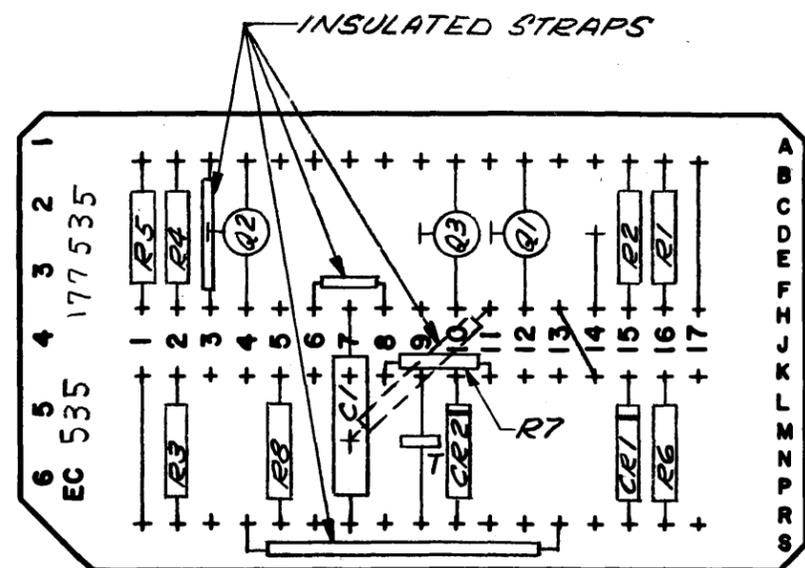
EC 535

177535

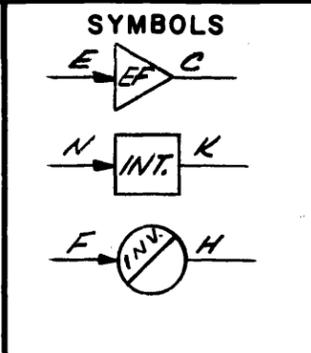
1 EMITTER FOLLOWER
1 INTEGRATOR (1050 BAUD)
1 INVERTER

CIRCUIT BOARD EC 535

177535



NOTE:
REFER TO 5016WD FOR MARKING INFORMATION



ISSUE	DATE	AUTH. NO.

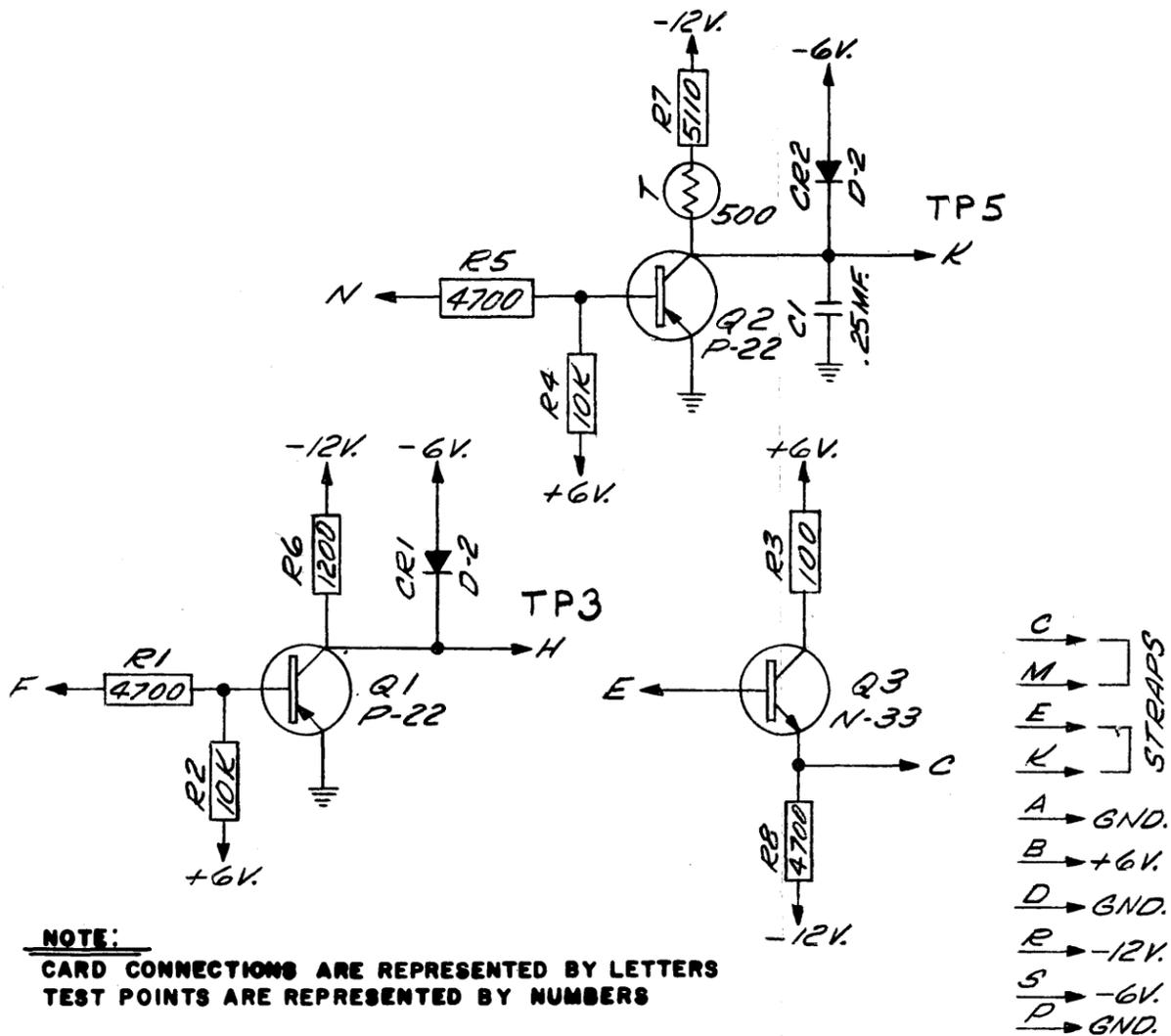
This card consists of a common emitter amplifier, an integrating amplifier and an emitter follower.

Q1 is reverse biased when zero volts is applied to its input Pin F. Its collector is clamped to -6 volts by diode CR1. When -6 volts is applied to Pin F Q1 is saturated causing the collector potential to rise to approximately zero volts.

Q2 is saturated when -6 volts is applied to Pin N and its collector potential is approximately zero volts. When zero volts is applied to Pin N Q2 is reverse biased and its collector potential decreases towards -6 volts at a rate determined by the RC time constant of Resistor R7, Thermistor T, and Capacitor C1 with the aiming potential of -12 volts.

Q3 is an NPN emitter follower that does not change the phase or signal level of the input signal, but has a high current gain for positive going transistions and a low output impedance.

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
CR1	177108	2	Diode D-2	Clamp
CR2			Same as CR1	"
R1	118146	3	Resistor Fixed 4700 ohms	Base Resistor
R2	118180	2	Resistor Fixed 10K ohms	Bias Resistor
R3	137438	1	Resistor Fixed 100 ohms	Limiting Resistor
R4			Same as R2	Bias Resistor
R5			Same as R1	Base Resistor
R6	137441	1	Resistor Fixed 1200 ohms	Collector Load
R7	146742	1	Resistor Fixed 5110 ohms	Timing Resistor
R8			Same as R1	Emitter Load
C1	171587	1	Capacitor 25 MF	Timing Capacitor
Q1	177105	2	Transistor P-22	Amplifier
Q2			Same as Q1	"
Q3	177106	1	Transistor N-33	Amplifier
EC	172067	1	Circuit Card, Etched	
T	146737	1	Thermistor 500 ohms	Temp. Compensate
		5	Strap 24 AWG Bare	
		3	" " " Insulated	
	144495	3	Pad Transistor	



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R	E OF M
E-NUMBER	
PROD. NO. 177535	
DATE: 3-17-62	
P.D. FILE NO. 1-A148/134,53A	
DRAWN. K.F.L.	CHKD. S.M.
ENG. J.M.G.	APPD. S.M.

TELETYPE CORPORATION

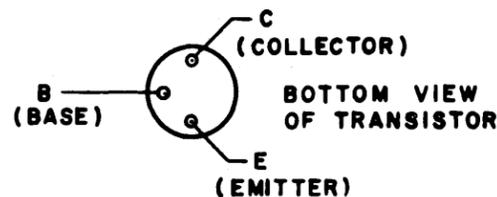
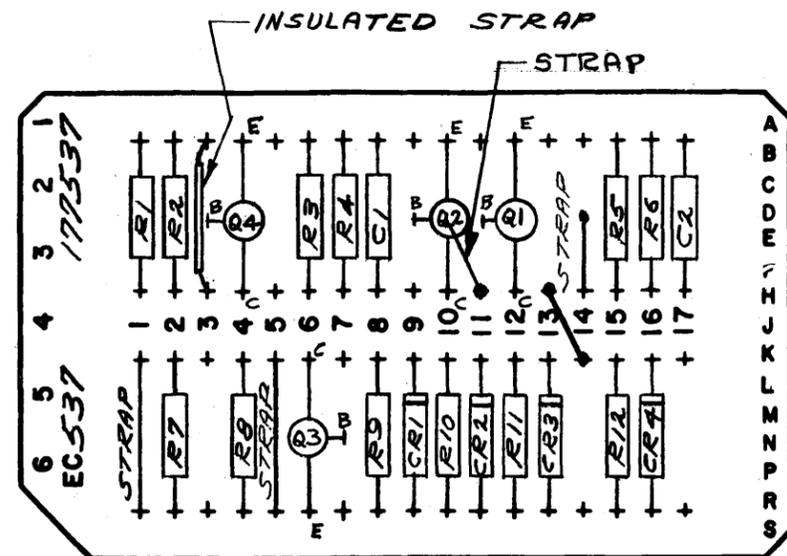
177535

EC 537

177537

CIRCUIT BOARD EC 537

177537



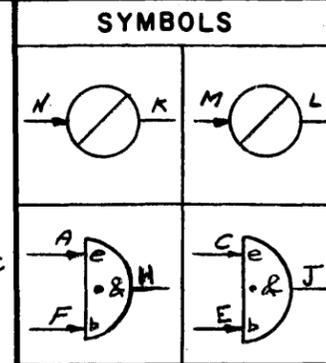
NOTE:
REFER TO 5016WD FOR MARKING INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	118186	4	Resistor Fixed, 5600 ohms	Base Resistor
R2	118146	4	" " 4700 "	Bias Resistor
R3			Same as R2	" "
R4	137440	2	Resistor Fixed, 1000 ohms	Base Resistor
R5			Same as R2	Bias Resistor
R6			Same as R4	Base Resistor
R7			Same as R2	Bias Resistor
R8			Same as R1	Base Resistor
R9	137441	2	Resistor Fixed, 1200 ohms	Load Resistor
R10			Same as R9	" "
R11			Same as R1	" "
R12			Same as R1	" "
C1	172332	2	Capacitor .002 MFD.	Coupling
C2			Same as C1	"
CR1	177108	4	Diode, D-2	Clamp
CR2			Same as CR1	"
CR3			Same as CR1	"
CR4			Same as CR1	"
Q1	177105	4	Transistor, P-22	Amplifier
Q2			Same as Q1	"
Q3			Same as Q1	"
Q4			Same as Q1	"
EC	172067	1	Circuit Card, Etched	
	144495	4	Pad, Transistor	
		5	Strap 24 AWG. Bare	
		1	Strap 24 AWG. Insulated	

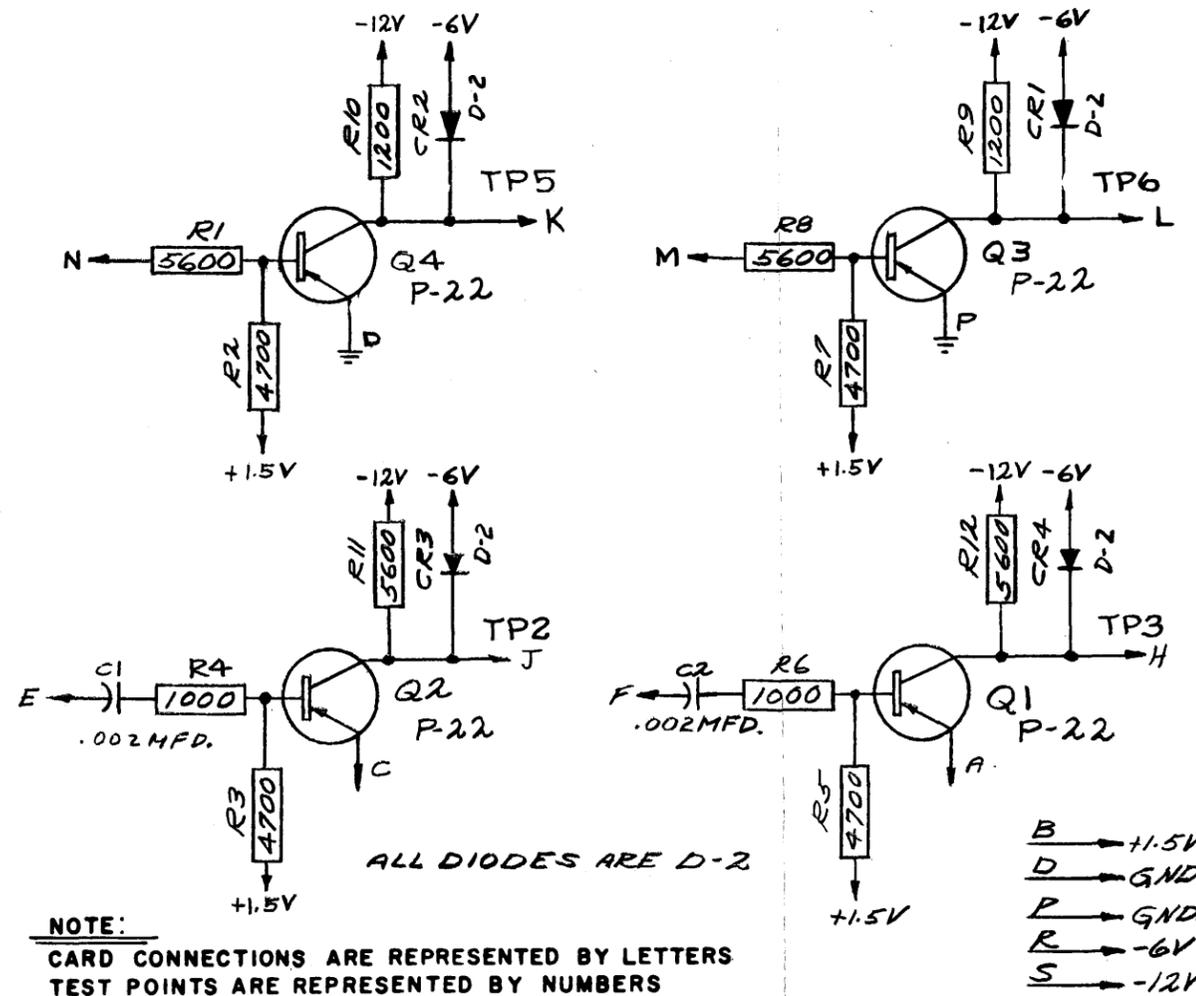
2 PULSE "AND" GATES
2 INVERTERS

Q1, the pulse "AND" gate, has two independent inputs at A and F. With 0 volts applied at A, Q1 is reversed biased +1.5 volts through R5. The output at H is clamped to -6 volts. A negative going voltage transition at F causes a pulse of negative current to be coupled through C2 and R6 saturating Q1. The output at H goes to approximately 0 volts for the duration of this current pulse. With -6 volts applied at A, the output at H is clamped to -6 volts independent of the signal at F. The same description applies to Q2.

Q3, the inverter, is reversed biased approximately +.8 volts through R7 with 0 volts applied at M. The output L is clamped to -6 volts. With -6 volts at M base current through R8 saturates Q3 putting the output L at approximately 0 volts. The same description applies to Q4.



ISSUE	DATE	AUTH. NO
2	8-13-62	74215



NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

B → +1.5V
D → GND.
P → GND.
R → -6V
S → -12V

APPROVALS

D W B E OF M

E-NUMBER

PROD. NO. 177537

DATE: 5-5-62

P.D. FILE NO. 1-448/134-53A

DRAWN: SV CHKD: JM

ENGD: JMG APPD: RM

TELETYPE CORPORATION

177537

EC 539

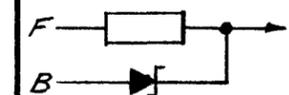
177539

CIRCUIT BOARD EC 539

177539

DISTRIBUTOR DRIVER
VOLTAGE REGULATOR

SYMBOLS



ISSUE	DATE	AUTH. NO.

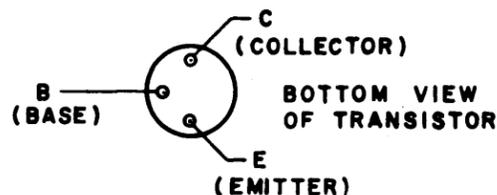
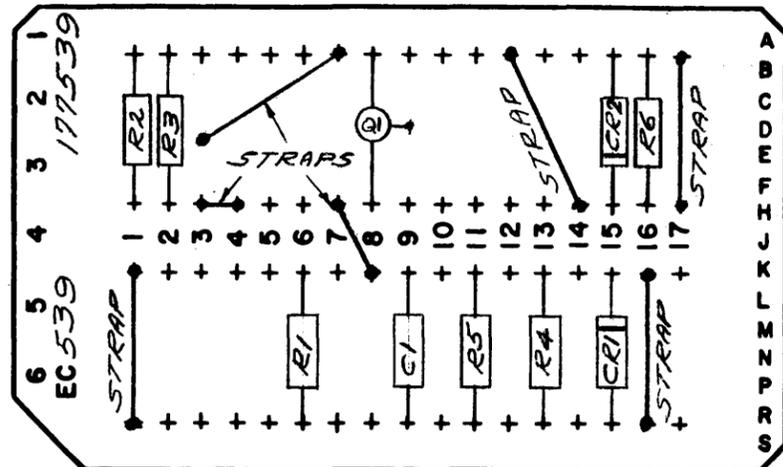
This card consists of a common emitter amplifier which provides voltage and current gain plus a voltage regulator using a zener diode.

Q1 is normally saturated, since base current flows from ground through R1 and the base emitter junction of Q1 to +6 V. R4 and R5 form a voltage divider which develops a voltage of -4.5 volts at C1. Since the input applied at N is normally -6 V, CR1 is reversed biased 1.5 volts. Noise pulses having less than 1.5 volts amplitude are therefore inhibited.

A positive 6 volt pulse applied at the base, through CR1 and C1, drives Q1 into cut-off. A negative going pulse less than 10 microseconds in duration therefore appears at the collector which is applied through R2 to the associated distributor.

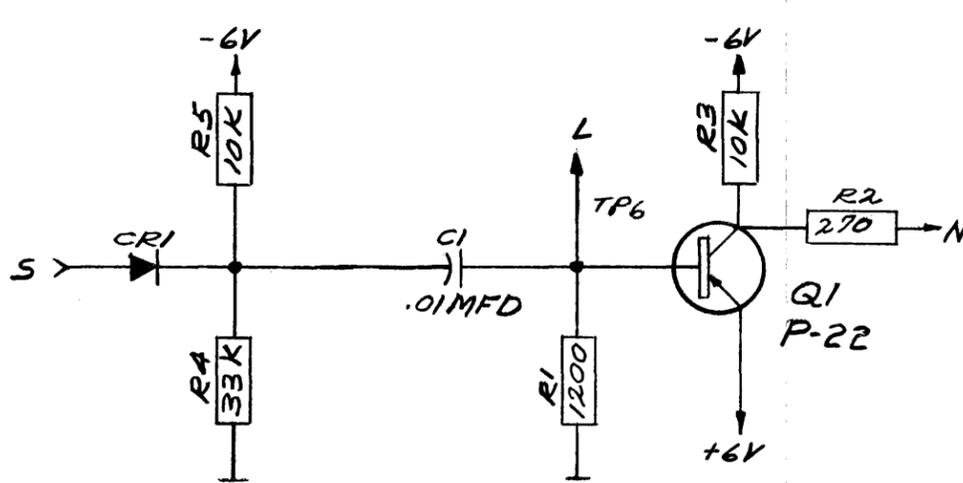
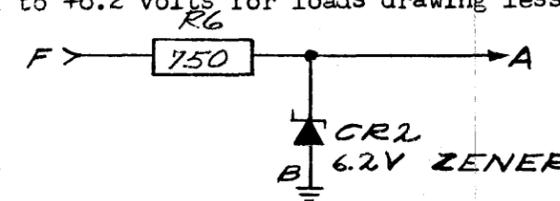
Applying +12 volts at L reverse biases Q1 supplying -6 volts through R3 and R2 to the output N.

The voltage regulator consists of R6 and zener diode CR2. Normally an unregulated voltage of approximately +15 volts is applied at F. The output A is regulated to +6.2 volts for loads drawing less than approximately 10 milliamps.



NOTE:
REFER TO 5016WD FOR MARKING INFORMATION

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
C1	171566	1	Capacitor, Ceramic .01 mf.	Coupling
CR1	172108	1	Diode, D-2	Coupling
CR2	146762	1	Diode, Zener 6.2 V	Regulator
R1	137441	1	Resistor, Fixed 1200 ohms	Bias
R2	118225	1	" " 270 "	Output Limiting
R3	118180	2	" " 10K "	Collector Load
R4	118153	1	" " 33K "	Voltage Divider
R5			Same as R3	" "
R6	143660	1	Resistor Fixed, 750 ohms	Current Limiting
Q1	177105	1	Transistor, P-22	Amplifier
EC	172067	1	Circuit Card, Etched	
	144495	1	Pad, Transistor	
		7	Strap 24 AWG. Bare	



- B → GND.
- E → +6V
- J → GND.
- P → GND.
- K → -6V

NOTE:
CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

APPROVALS

D AND R: [Signature]
E OF M: [Signature]

E-NUMBER

PROD. NO. 177539

DATE: 6-12-62

P.D. FILE NO. 1-A148/134.53A

DRAWN: SW CHKD: [Signature]

ENG. JMS APPD. RYR

TELETYPE CORPORATION

177539