905C DATA TEST SET

FOR USE WITH

1A DATA SELECTIVE CALLING SYSTEM

CIRCUIT DESCRIPTION AND WIRING DIAGRAMS

CONTENTS PAGE

1. GENERAL

1.01 This section is issued to provide wiring diagrams and a description of the circuitry of the Data Test Set 905C.

1.02 The circuitry of this unit is divided into six major groups in order to simplify the discussion of the circuit description.

2. CIRCUIT DESCRIPTION

A. Power Supply

2.01 The -24 v dc power supply provides the operating voltage for the TEST RESPONSE indicator (DS-2) and the TEST ON indicator (DS-3). The 117 v ac, 60-cycle power is applied through a three-conductor line cord (5723WD, Sheet 3) to terminal board TB1 (pins 1 and 2). The third wire is a ground from the test set frame to the power line ground. Power is applied to the primary of transformer T1 and power indicator DS-1, and through the power switch S1 and fuse F1. The secondary voltage of T1 (approximately 36 v ac center tap) is rectified by CR1 and CR2, and C1 is charged to approximately 24 v dc. R1 discharges C1 after power is turned off.

2.02 The -12 v dc required by the test set is supplied by the 905A/B data test set (5723WD, Sheet 2). Resistor R1 and diode CR1 develop the -6 v dc reference voltage. Capacitor C1 filters any noise appearing across CR1 caused by load variations.

2.03 The +17 v dc required by the test set is supplied by the 905A/B data test set. Resistor R2 and diode CR2 develop the +6 v dc required. Capacitor C2 filters any noise appearing across CR2 caused by load variations.

2.04 Both the -6 v dc and +6 v dc are fused by F2 and F3 respectively. These fuses are low resistance units and should be replaced by the same type supplied.

2.05 When power is shut off, a ground is placed on the matrix output and the oscillator control signal by power switch S1, contact C. This allows normal operation of the 905A/B data test set, independent of any control voltages the test set may develop.

B. Oscillator Control and Test Indicator (5723WD, Sheet 2).

2.06 Oscillator control flip-flop Z106 controls the bit timer in the 905A/B data test set with the TEST SINGLE/CONTINUOUS switch S7 and the TEST START switch S8. To initiate a single test sequence, place switch S7 to SINGLE and depress switch S8.

2.07 This places a ground on inverters Z108, pins 5 and 7, and set 1 of flip-flop Z106, pin 3. The output of the flip-flop goes to 0 volt and is fed through two complimentary emitter followers, Z208 and Z209, which apply a 0 volt oscillator start signal to connector J1, pin 42. This same signal, through power amplifier Z206, illuminates TEST ON lamp DS-3, indicating a test sequence is being generated. The dual inverters Z108 serve as a set-reset flip-flop to eliminate false trigger signals which may develop due to switch contact bounce.

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2.08 With TEST SINGLE/CONTINUOUS switch in the CONTINUOUS position, the Z106, pin 7, to ground contact is open, thereby biasing the set 0 prime of Z106 to -12 v dc through R1. The output of character ring counter element 1 (applied to set 0 input, pin 6) now, cannot reset flip-flop Z106 due to the presence of the bias voltage. Placing the TEST SINGLE/CONTINUOUS switch to the SINGLE position closes the contact between Z106, pin 7, and ground, allowing the character ring counter element 1 output to reset flip-flop Z106 at the completion of a test sequence. Resetting the flip-flop to the set 0 state places output pin 10 of Z106 at -6 volts. This signal is fed through emitter followers, Z208 and Z209, to extinguish the TEST ON lamp DS-3 and to connector J1, pin 42, to stop the bit timer in the 905A/B data test set.

C. Test Response Indicator Circuit (5723WD, Sheet 2)

2.09 The test response circuit gives a visual indication when a line break is being received as a test response.

2.10 The response from a system is usually a two-second line break. The 6 v dc (spacing) signal from the data set is applied to connector J1, pin 40. From there, it is applied through emitter follower Z209 to power amplifiers Z206, pins 35 and 32. Output pin 28 completes the circuit to the TEST RESPONSE lamp DS-2. Output pin 29 is connected to pin 5 of the TEST SINGLE/CONTINUOUS switch (S7).

2.11 Some system responses are too short in duration to completely illuminate the TEST RESPONSE lamp. To make sure the lamp fully lights, a 70 millisecond one-shot multivibrator (Z217) is in the test response indicator circuit. When a mark to space transition is received, the Z217 output (pin 33) reinforces the short response at the OR gate associated with power amplifier Z206 at pin 34.

D. Character Selection Circuit (5723WD, Sheet 1).

2.12 The character selection circuit selects and generates the two alpha characters required for a call directing code or transmitter start code (CDC/TSC).

2.13 With the FUNCTION switch S4 in the CDC/TSC position, the 905C data test set generates two alpha characters followed by at least one letters/rubout character, when the TEST START button is depressed. A 0 volt signal, received from the character ring counter (in the 905A/B data test set) at connector J1, pin 1, is applied to inverter Z107, pin 5. The inverted signal, -6 v dc, with its power level increased by emitter follower Z208, is applied to the LEVEL FIVE/EIGHT switch S3 at pin 5. With switch S3 in the LEVEL FIVE position, the signal is then sent from contact 6 to the FUNCTION switch S4, pin 1. In the CDC/TSC position, pin 5 carries the signal to the character selector switch S6, section 1, through the preselected alpha character position to the diode matrix. The diode matrix encodes the signal for the selected alpha character. The resultant parallel 8-bit output is used to prime eight, 2-input AND gates, Z110 and Z210, in the serializing circuit (5723WD, Sheet 2). At this point, the character ring counter is advanced to element 2, and the same process is repeated for alpha character 2.

2.14 For special codes not programmed into the test set, the FUNCTION switch can be placed to EXT, and special matrix cards (TP177598, Figure 1) can be inserted into the EXTERNAL PROGRAMMING jacks, CHARACTER 1, and CHARACTER 2.

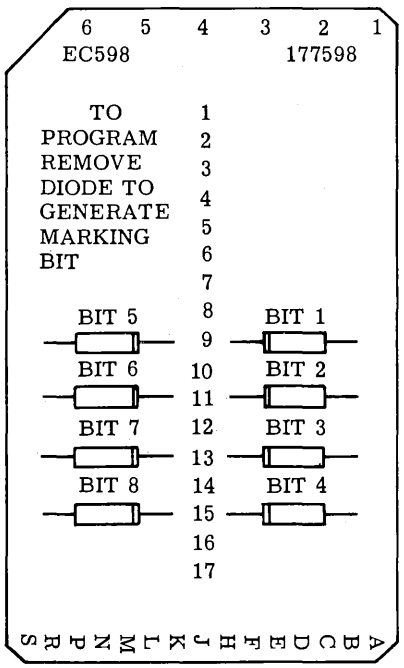

Figure 1 - Universal Programming Card

E. Character Serialization (5723WD, Sheet 2)

2.15 Serializing of characters is accomplished by scanning the eight, 2-input AND gates, with the bit ring elements from the 905A/B data test set.

2.16 If a bit is programmed for a space, its output will be -6 volts. Since only one element of the bit ring is 0 volt at any one time, the outputs fed to OR gate Z109, are -6 volts. The output is then fed through double inverters Z107. The -6 volt signal is then sent to the 905A/B data test set as a spacing signal.

2.17 A marking signal is generated by leaving the AND gate input floating (no diode). The output of the gate will then follow the 0 volt bit ring signal through the OR gate, and the double inverters to the 905A/B data test set. This 0 volt signal generates a marking bit. When all eight gates have been scanned, the character ring advances and the same sequence of events is provided for character 2.

2.18 The double inverters at the output of OR gate Z109 square up the signals and reestablish the standout signal levels before they leave this unit. The OUTPUT jack (TP-1), located on the front panel of the 905C data test set, allows signals to be monitored after they leave the double inverters.

F. Parity Circuit (5723WD, Sheet 3)

2.19 The parity circuit determines if the 8-level signal generated will have an odd or even number of bits. This is accomplished by using the 8-bit output to determine what type of parity to generate. The 8-level matrix cards, Z114, Z115, and Z116, are programmed to give all 8-level characters an even number of marking bits.

2.20 The PARITY ODD/OFF/EVEN switch allows selection of the type of parity to be generated. In the EVEN position, the 8-bit output is allowed to directly program the serial circuitry. In the OFF position the eighth level is left floating, making the eighth bit for all characters, marking. In the ODD position, additional circuitry is needed. Basically, this circuitry inverts the 8-bit level, producing an odd bit signal. This is accomplished by having a 5-input AND gate Z117 sample the first five levels of the matrix output. Since at least one of the first five levels is spacing (-0 v) when a valid character is being sent, output pin 2 of the AND gate is driven to -6 volts. This signal, inverted to 0 volt by inverter Z108 and fed to a 2-input AND gate Z117, an input pin 10, allows whatever signal is present at input pin 9 to pass through the AND gate. These signals, inverted by another inverter Z108, prime the eighth level of the AND gate in the serializing circuit. LEVEL selector switch S3 disconnects the parity circuit for 5-level operation.

2.21 To generate a rubout, all inputs to the 5-input AND gate Z117 go to 0 volt, driving output pin 2 to 0 volt. After being inverted to -6 volts it is fed to the 2-input AND gate, holding its output at -6 volts. This signal is again inverted to 0 volt, allowing an all marking signal to be generated.

NO NOTES

REFER TO SHEET 3 OF 3 FOR NOTES

EXTERNAL CHARACTER PROGRAMING

CHAR. 1 J2

CHAR. 2

LEVEL S3 SECT. 1A

5-LEVEL

8-LEVEL

ALL 2 → SRV. 2F6

Z107 EC495-1/4

Z208 EC528-1/6

CHARACTER RING ELEM. 1 J1 P 2F3

EF

LEVEL S3 SECT. 1B

5-LEVEL

8-LEVEL

FUNCTION S4 SECT. 1A

EXT.

CDC/TSC

EOM/ETX

EOA/STX

V/ACK

NACK

S4 SECT. 1B

EXT.

CDC/TSC → A 3A2

EOM/ETX → B 3F4

EOA/STX → C 3F4

V/ACK → D 3F4

NACK → E 3F4

Z107 EC495-1/4

Z208 EC528-1/6

CHARACTER RING ELEM. 2 J1

EF

LEVEL S3 SECT. 1C

5-LEVEL

8-LEVEL

FUNCTION S4 SECT. 2A

EXT.

CDC/TSC

EOM/ETX

EOA/STX

V/ACK

NACK

S4 SECT. 2B

EXT.

CDC/TSC → F 3A2

EOM/ETX

EOA/STX

V/ACK

NACK

CHARACTER 2

S5 SECT. 1

CHARACTER 1

S6 SECT. 1

Z111 EC620 DIODE MATRIX

Z112 EC621 DIODE MATRIX

Z113 EC622 DIODE MATRIX

AUX. 1

AUX. 2

AUX. 3

AUX. 4

AUX. 5

AUX. 6

G 2A6, 3E5, 1A3

H 2A6, 3E5, 1A3

I 2B6, 3F5, 1B3

J 2B6, 3F5, 1B3

K 2C6, 3F5, 1B3

L 2C6, 3F5, 1B3

M 2C6, 3F5, 1B3

N 2D6, 3C5, 1B3

NOTE: REVISION INFORMATION MUST ALSO BE REFLECTED ON THE ISSUE CONTROL RECORD.

5723WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	1-26-65	15831R
2	5-12-65	86223
3	11-11-65	88573

SHEET 1 OF 3

SCHEMATIC WIRING DIAGRAM FOR

HIGH SPEED SELECTIVE CALLING SYSTEM TEST SET

ASSEMBLY NO. TSG 802

APPROVALS

D AND R	E OF M

E-NUMBER

PROD. NO. 5723 WD

DATE 10-5-64

P.D. FILE NO. 33-A25 AA

DRAWN N.A.R. CHKD.

ENGD. R.E.P. APPD.

TELETYPE CORPORATION

5723WD

TC 434 3-65

NO.	NOTES
	REFER TO SHEET 3 OF 3 FOR NOTES.

NOTE:
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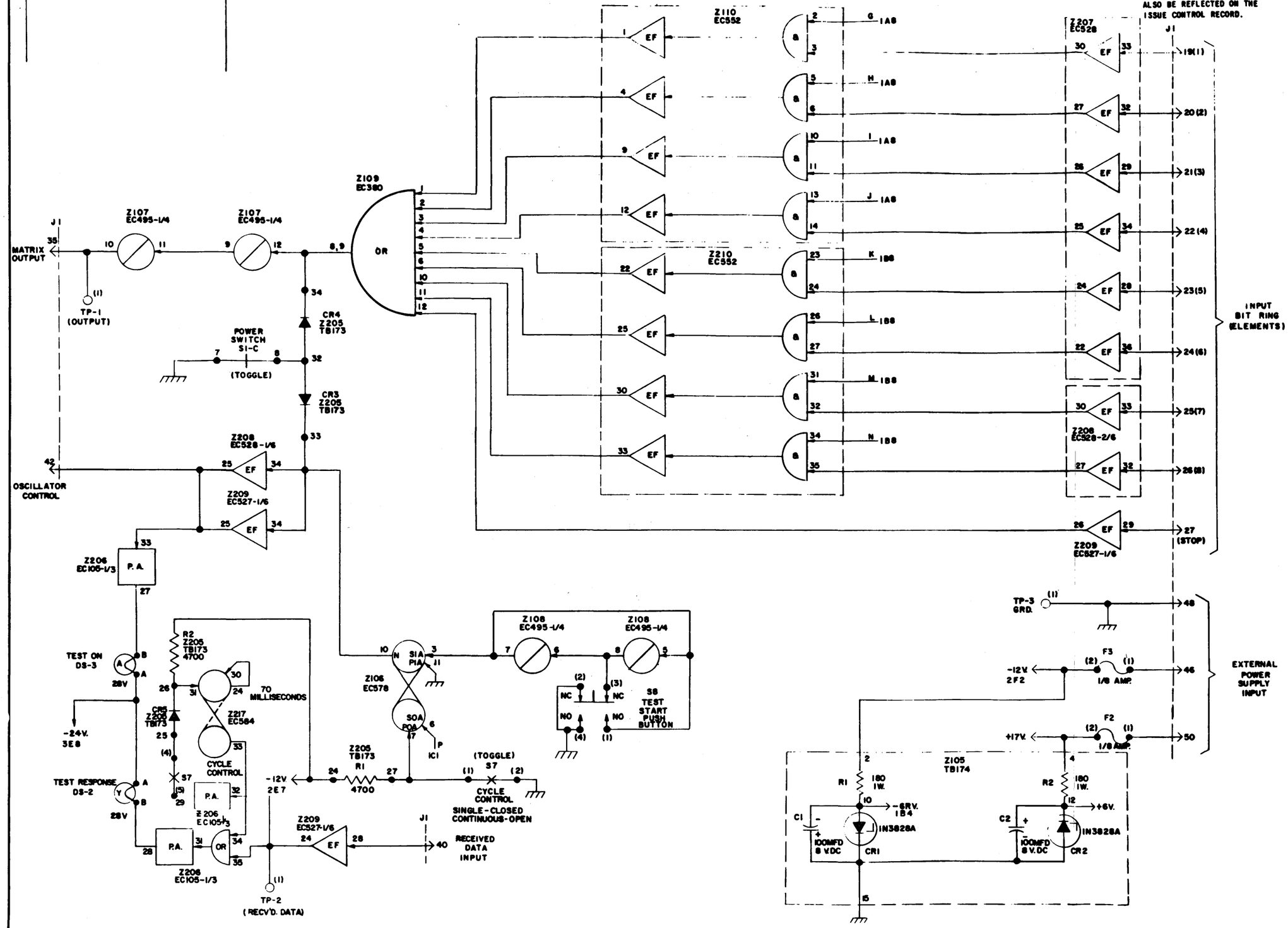
5723WD

REVISIONS

ISSUE	DATE	AUTH. NO.
1	1-26-65	15831R
2	5-21-65	86960
3	11-12-65	88569



SHEET 2 OF 3

SCHEMATIC WIRING DIAGRAM FOR HIGH SPEED SELECTIVE CALLING SYSTEM TEST SET

ASSEMBLY NO. TSS 802

APPROVALS	
D AND R	E OF M

E-NUMBER

PROD. NO. 5723 WD

DATE 10-5-64

P.D. FILE NO. 33-A25AA

DRAWN N. A. R. CHKD.

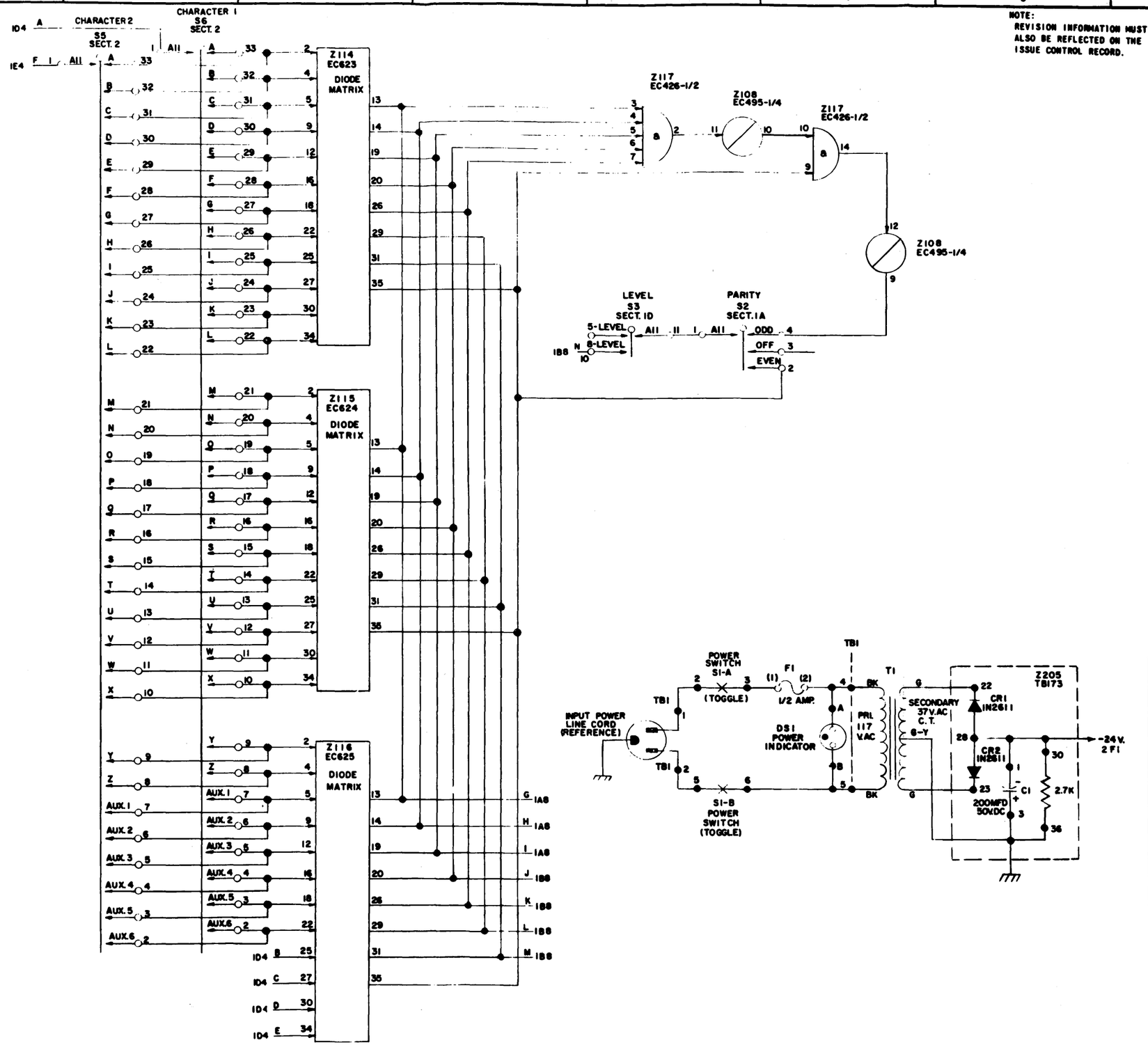
ENGD. R. E. P. APPD.

TELETYPE CORPORATION

5723 WD

NO.	NOTES
1.	ALL VOLTAGE DC UNLESS OTHERWISE SPECIFIED.
2.	TERMINAL DESIGNATIONS IN PARENTHESIS ( ) ARE FOR REFERENCE AND NOT MARKED ON COMPONENT.
3.	ALL RESISTORS 1/2 WATT AND RESISTANCE VALUES IN OHMS, UNLESS OTHERWISE SPECIFIED.
4.	WIRING LEGEND: F — REFERENCE POINT; 1E4 — PAGE NUMBER, PAGE AREA
5.	WIRING COLOR CODE: BK—BLACK, BR—BROWN, R—RED, O—ORANGE, Y—YELLOW, G—GREEN, BL—BLUE, P—PURPLE, S—SLATE, W—WHITE
6	SPARE CIRCUITS AVAILABLE: 1—PNP EMITTER FOLLOWER Z208, EC528-1/6; 3—NPN EMITTER FOLLOWERS Z209, EC527-3/6; 1—POWER AMPLIFIER Z206, EC105-1/3
7.	REFER TO 5724WD FOR ACTUAL WIRING DIAGRAM.
8.	
9.	LAMP COLOR CODE: A — AMBER, Y — YELLOW
10.	RESISTANCE OF WINDINGS ON TRANSFORMER T1. PRIMARY (BK TO BK) 26 OHMS. SECONDARY (G TO G) 3.25 OHMS. EITHER G LEAD TO G-Y 1.625 OHMS.
11.	ALPHA-NUMERIC CONVERSION CHART FOR 15 POINT CIRCUIT CARDS. (WHEN 15 POINT CKT. CARD IS USED IN THE UPPER HALF OF A 36 PIN CONNECTOR IT EMPLOYS PINS 1-15. WHEN USED IN LOWER HALF OF CONNECTOR IT EMPLOYS PINS 22-36.)

STAMPING ON CKT CARD	NUMERICAL CONVERSION FOR 15 PT. CARDS WHEN USED WITH 36 PT. CONNECTOR. WHEN INSERTED IN UPPER HALF OF CONNECTOR	WHEN INSERTED IN LOWER HALF OF CONNECTOR
A	1	22
B	2	23
C	3	24
D	4	25
E	5	26
F	6	27
H	7	28
J	8	29
K	9	30
L	10	31
M	11	32
N	12	33
P	13	34
R	14	35
S	15	36



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SHEET 3 OF 3

SCHEMATIC
WIRING DIAGRAM
FOR
HIGH SPEED
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APPROVALS	
D AND R	E OF M
H/K	L1

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CORPORATION

5723WD

TC 434 (3-65)