906A DATA DISTORTION TEST CIRCUIT

GENERAL DESCRIPTION AND OPERATING PRINCIPLES

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1. GENERAL

GENERAL DESCRIPTION

1.01 The 906A data distortion test equipment is designed for use in maintaining the B1 data carrier system and is included as part of the 20A toll testboard. Using the 906A, the 20A testboard

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can simulate subscribers' calls through the B1 system and determine over-all performance of a B1 link by measuring the data distortion of a signal transmitted over the link. It is also possible to make sectionalizing tests on the 4-wire facility which connects two B1 data terminals in order to locate trouble to the faulty B1 terminal or facility. In these sectionalizing tests, transmission, frequency offset, noise, and data distortion measurements may be made on each of the six data channels and the supervisory channel. It is also possible to monitor the supervisory E lead signals. Although designed primarily for use with the B1 system, the 906A can perform similar over-all and sectionalizing tests on voice-band WADS circuits.

1.02 In performing all tests, the 906A is controlled by the data test cord circuit (SD- and CD-56528-01) of the 20A testboard. This section is necessarily not a description of the operation of the testboard but rather a description of the 906A and how it is used in those tests. This section is reissued to reflect circuit changes. Due to extensive changes, marginal arrows have been omitted.

EQUIPMENT FEATURES

1.03 The 906A is composed of three parts:

- Data Distortion Measuring Unit (Fig. 1).
- Data Distortion Display Panel (Fig. 2).
- Data Distortion Calibrator Panel (Fig. 3).

1.04 *The data distortion measuring unit* comprises the electronic circuits and their associated relays. It is composed of six functional units: signal generator, modulator, F1/F2 demodulator, distortion measuring circuit, channel selector, supervisory demodulator-demultiplexer, and calibrator circuit. These functional units are primarily composed of basic transistorized logic building block circuits such as gates, binary cells, monopulsers, etc, which are described in CD-73022-01.

1.05 *The data distortion display panel* contains the data distortion read-out devices and associated controls which include the calibrate adjust controls. There is a meter for reading peak telegraph distortion or bias distortion and a message register for counting the number of times the peak distortion exceeds some preset amount.

1.06 *The data distortion calibrator panel* is used in maintaining the 906A and in checking the accuracy, or calibration, of the distortion readings.

1.07 A block diagram of the 906A is given in Fig. 4.

1.08 In some B1 data terminal installations, more than one 20A testboard position will be needed to serve all the B1 data trunks. Therefore, the 906A has been designed to be used cooperatively by more than one test position. As will be shown, it may be used simultaneously for different functions. A completely equipped 906A can serve two test positions. However, for three or four positions only a partially equipped 906A need be added since one channel selector and one supervisory demodulator-demultiplexer can serve up to four positions (see Fig. 4).

1.09 Fig. 5 shows the equipment codes and cabling for a typical installation of up to four positions. If desired, positions 3 and 4 could be identical to positions 1 and 2 and thus independent of them.

OPERATING FEATURES

1.10 This section describes the many testing functions the 906A can perform and, in a summary, lists the conditions under which certain functions may be performed simultaneously.

(a) The 906A data distortion test circuit can generate signals as follows:

(1) For use in both over-all and sectionalizing tests of B1 data channels, it can send to the data trunk on the 2-wire side of a B1 data terminal a frequency shift keyed (FSK) signal in either the F1 (1170 cps) or F2 (2125 cps) frequency band. This signal may have any one of four levels which at the 2-wire side of a B1 data terminal correspond to the nominal input power, the two extreme ends of the range of input power over which the AGC circuit in the B1 data terminal will operate, and a low level upon which the AGC circuit must not operate. For an F1 signal,

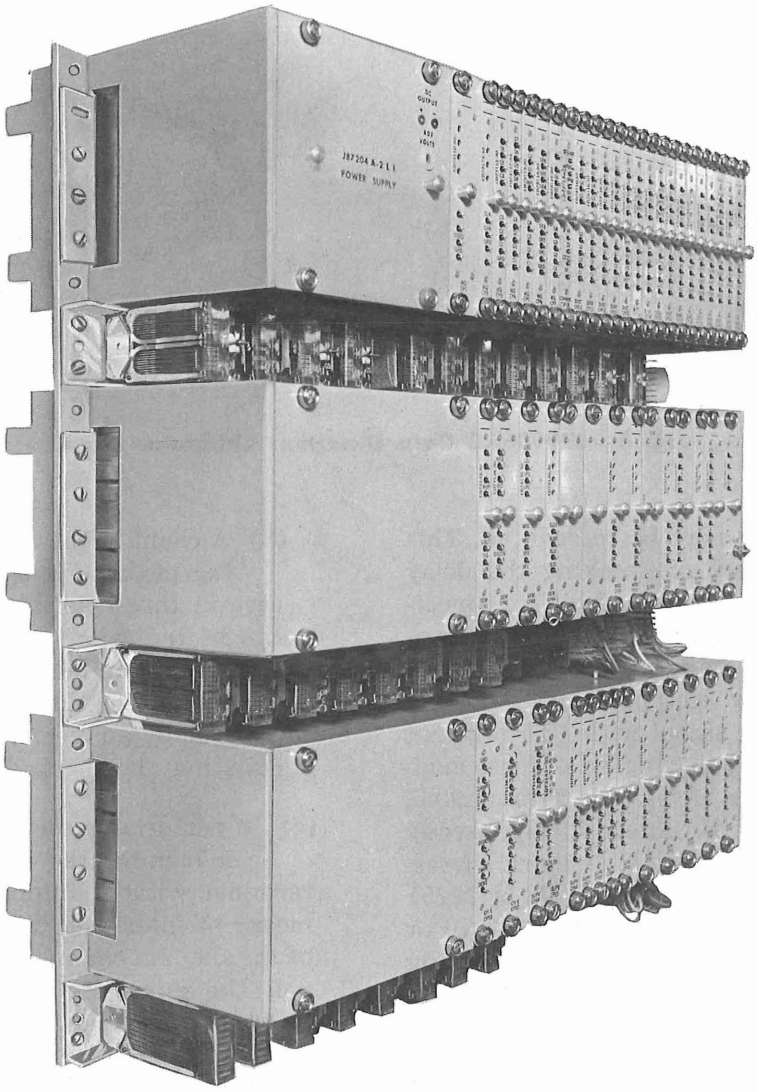


Fig. 1 — J79906AA Data Distortion Measuring Unit

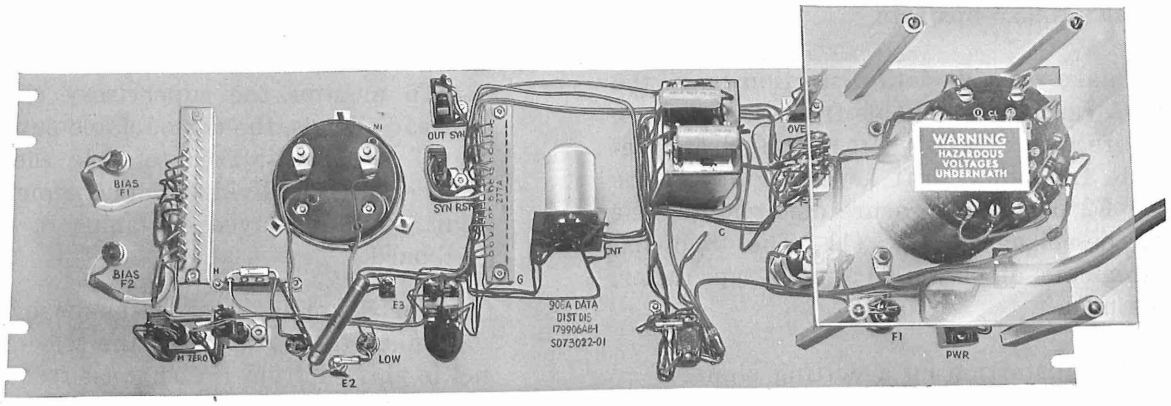


Fig. 2 — J79906AB Data Distortion Display Panel

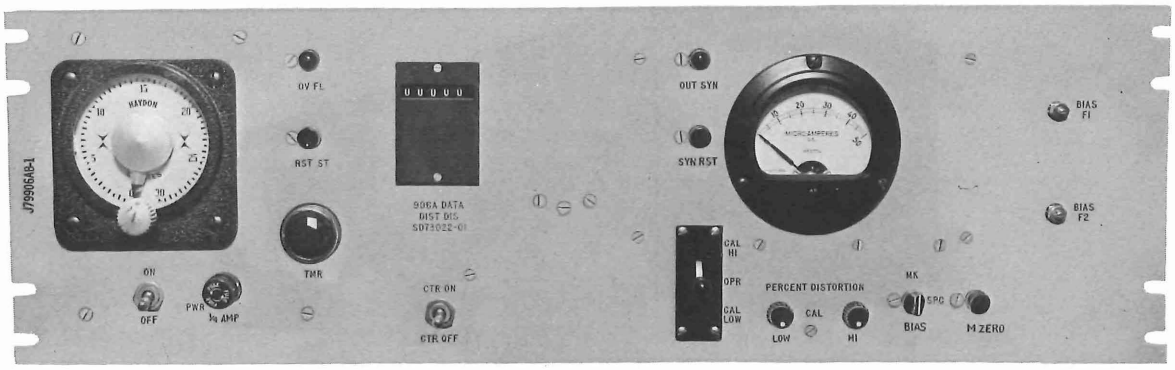


Fig. 3 — J79906AC Data Distortion Calibrator Panel

delay predistortion may be introduced. This predistortion is used in checking the delay distortion of the 4-wire voice facility connecting two B1 data terminals. The frequency shift keyed signal can be modulated by a quasi-random 4-row teletype signal, a dotting signal, or a dotting signal with 12.5 per cent of either marking or spacing bias. These modulating signals may have a bit rate of 99.5, 110, 150, or 200 bps. Alternatively, steady mark or space may be sent. A mark corresponds to the higher frequency (1270 or 2225) and a space to the lower frequency (1070 or 2025). These signals can be used for checking voice-band circuits as well as the B1 data carrier system.

(2) For sectionalizing tests of the B1 supervisory channel, the 906A can send directly to the 4-wire facility of a B1 data link in the supervisory (350 cps) frequency band a frequency shift signal modulated as in (1) but only at the 95.5-bps rate.

(b) To make over-all data distortion tests, the 906A can receive signals from the trunk on the 2-wire side of a B1 data terminal and demodulate frequency shift keyed signals in the F1 and F2 bands to measure distortion of the signals described in (a) (1). The following measurements, displayed on a panel-type meter, may be made:

(1) Bias distortion on a dotting signal

(2) Peak telegraph distortion

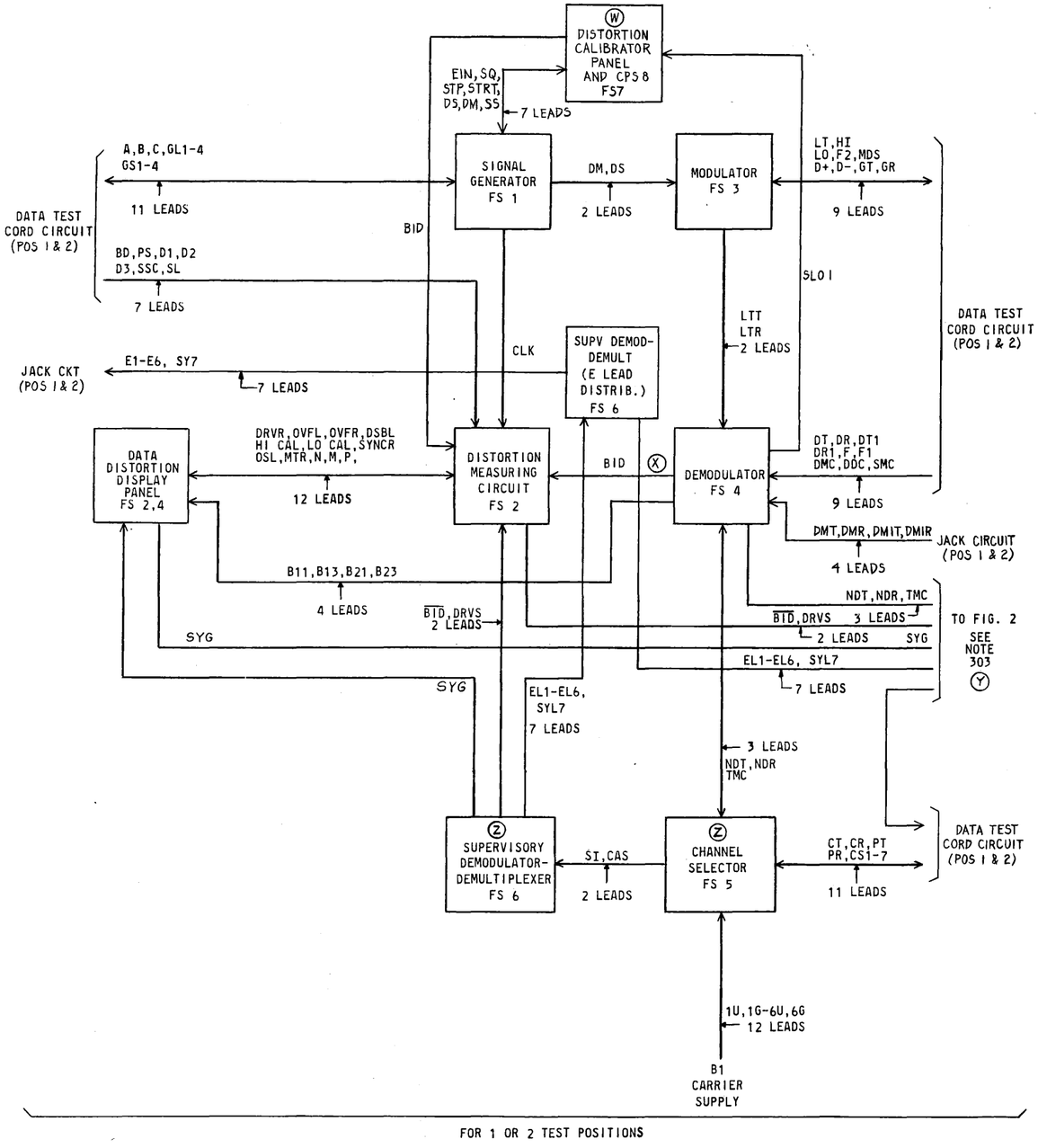
(3) A count of the number of characters having peaks of telegraph distortion above a certain threshold during some time interval can be indicated on a message register. The threshold may be 4, 8, 12, 16, or 20 per cent distortion. The timing may be controlled manually or by an electric timer. Voice-band circuits may be checked this way also.

(c) In performing sectionalizing tests, the 906A can monitor the 4-wire side of a B1 data terminal without interrupting service and, by means of filters, select the signal from any one of the six data channels or the supervisory channel. The signal from the selected channel may be treated as follows:

(1) For transmission, noise, or frequency measurements, the signal may be sent back to the data test card circuit at the same level as it appeared on the 4-wire line. Connections to the necessary measuring equipment are made through the data test cord circuit.

(2) To monitor the supervisory channel E lead signals, the demodulated supervisory signal is demultiplexed to yield the E lead signals for the individual data channels. These signals are displayed on lamps in the 20A testboard.

(3) For distortion measurements of a data channel, the signal from the selected channel is shifted from the channel frequency to F2 (2125 cps) so that distortion measurements may be made as in (b).



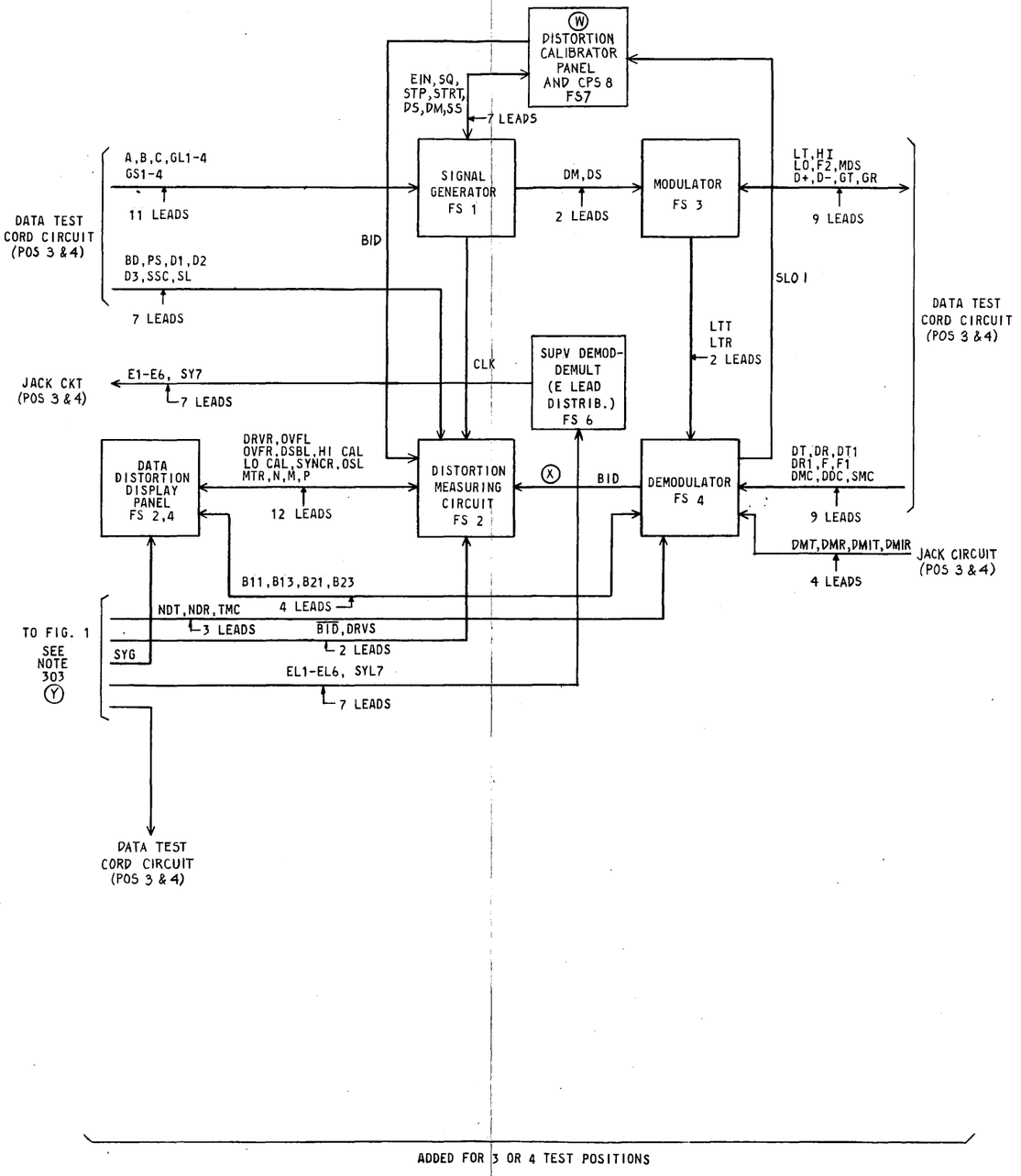
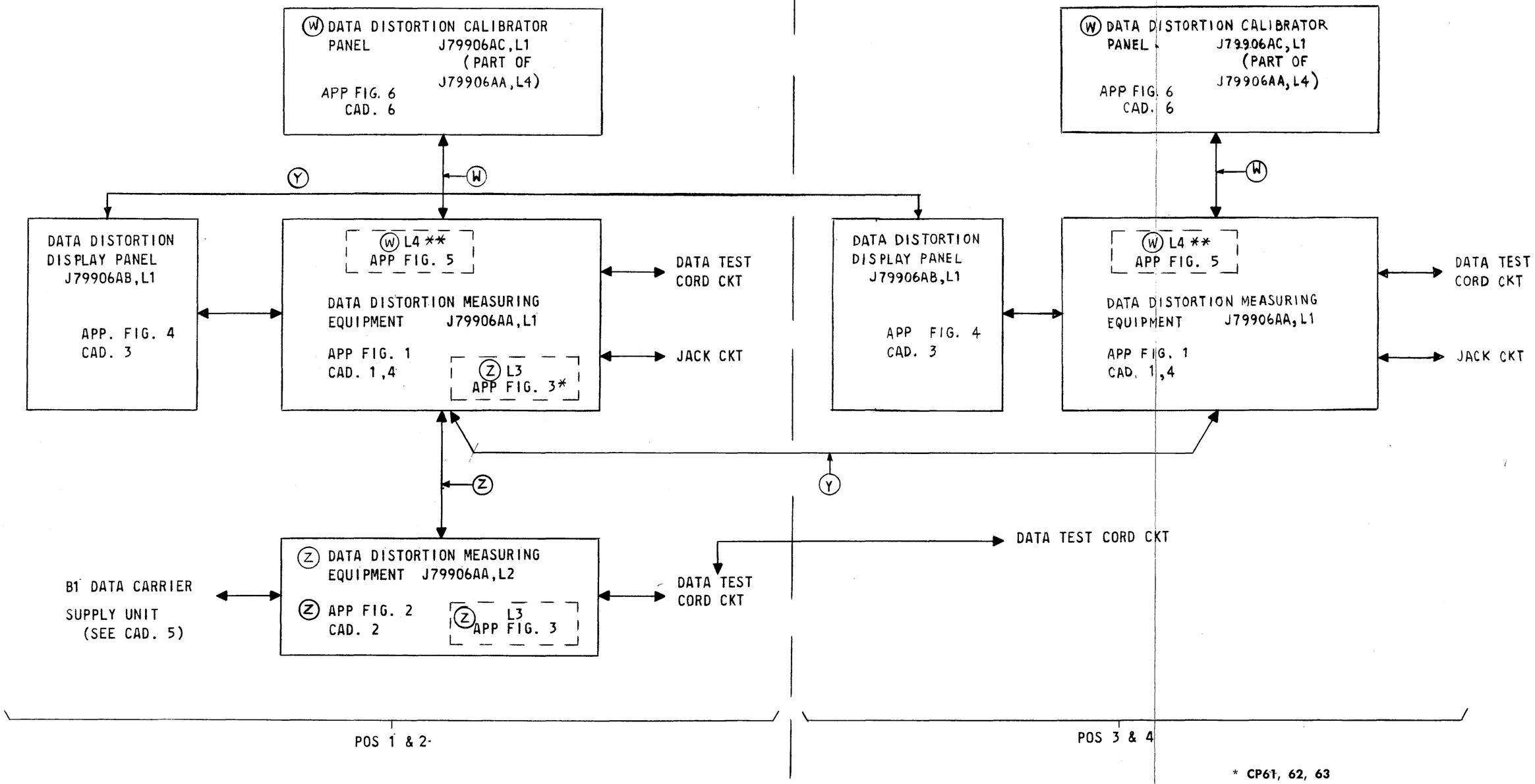


Fig. 4 — Over-All Block Diagram



* CP61, 62, 63
** CP8

Fig. 5 — Equipment Interconnection Block Diagram

(4) For distortion measurements of the supervisory channel, its signal is demodulated and the distortion measurements of (b) are made at 95.5 bps. In this case the tests of (c) (2) are performed simultaneously. The number of times the demultiplexer loses sync during some time interval may be counted. The supervisory channel signal may be generated either as in (a) (2) or by the supervisory channel of a B1 data terminal. In the latter case, controls exist in the jack circuit of the 20A testboard to permit sending any desired combination of E lead signals.

(d) To perform sectionalizing tests on a voiceband circuit, the following tests of the signal on the 4-wire facility can be made:

(1) The frequency shift signals at either F1 or F2 can be demodulated and the data distortion measured as in (b).

(2) Transmission, frequency offset, or noise measurements may be performed. The 906A is not involved in making these wideband tests.

(e) The calibrating and self-testing functions are available to check the accuracy of the distortion measurements and to adjust the calibration of the distortion meter when necessary.

(1) Calibration adjustment of the meter affects only the meter and its immediate drive circuitry. Hence, the meter calibration adjustment can be made even while counting distortion hits. Only the distortion meter readings are affected.

(2) Provision is made for local test of the signal generator, modulator, demodulator, and distortion measuring circuit. In performing this local test, the modulator and demodulator can be connected internally with all the features of (a) and (b) available. Alternatively, the output of the signal generator can be connected directly to the distortion measuring circuit. It is also possible to introduce distortion to check the calibration of the distortion measuring circuit.

(3) The operation of a supervisory demodulator-demultiplexer may be checked locally through the data test cord circuit by combining (a) (2) and (c) (4).

(f) The aforementioned operations may be performed simultaneously in certain combinations. The operations are summarized and the possible combinations of simultaneous operations are listed in Table I.

DESCRIPTION OF OPERATION

A. Distortion

1.11 Since the major object of the 906A is to accurately measure telegraph (or data) distortion, it is probably best to start with a discussion of what distortion is and how it arises. Distortion is a measure of perturbation of the transitions from mark to space or space to mark in the baseband data signal. Fig. 6A shows a typical baseband teletype character. The quasi-random teletype signal produced by the signal generator is a repetitive sequence of 63 different characters. Fig. 6B shows the same character distorted. Distortion is measured for each transition and is a measure of the amount a transition is distorted from its ideal location relative to the stop-start position even if the stop-start transition is itself distorted. Distortion in excess of 50 per cent will be read as 100 per cent minus the true distortion. Normally, if the repetitive pattern of the stop-start signal is missing, the distortion measuring circuit is disabled to prevent readings from being made on noise since in that case the readings are meaningless.

1.12 It is also possible to measure peak distortion of a signal without regard to the stop-start signals. In this case, the disabling feature described above is eliminated and the distortion is measured relative to some arbitrary mark to space transition for a period of nine bits following that transition. The measurement is then repeated relative to the next mark to space transition.

1.13 Bias distortion is measured as shown in Fig. 7. The readings are meaningful only when made on a dotting signal. The maximum reading is 50 per cent.

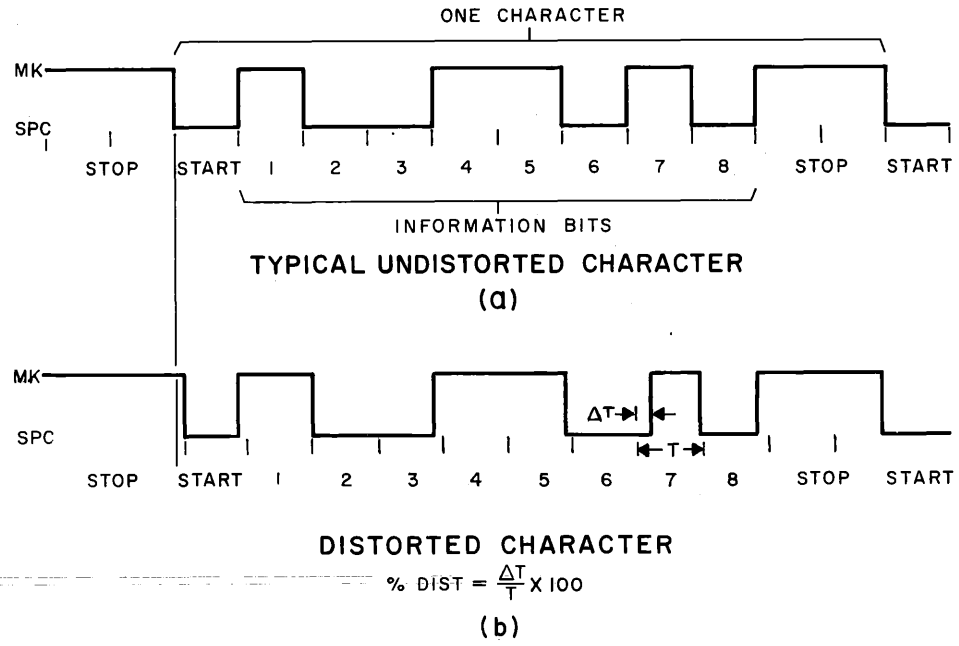


Fig. 6 — Definition of Peak Telegraph Distortion

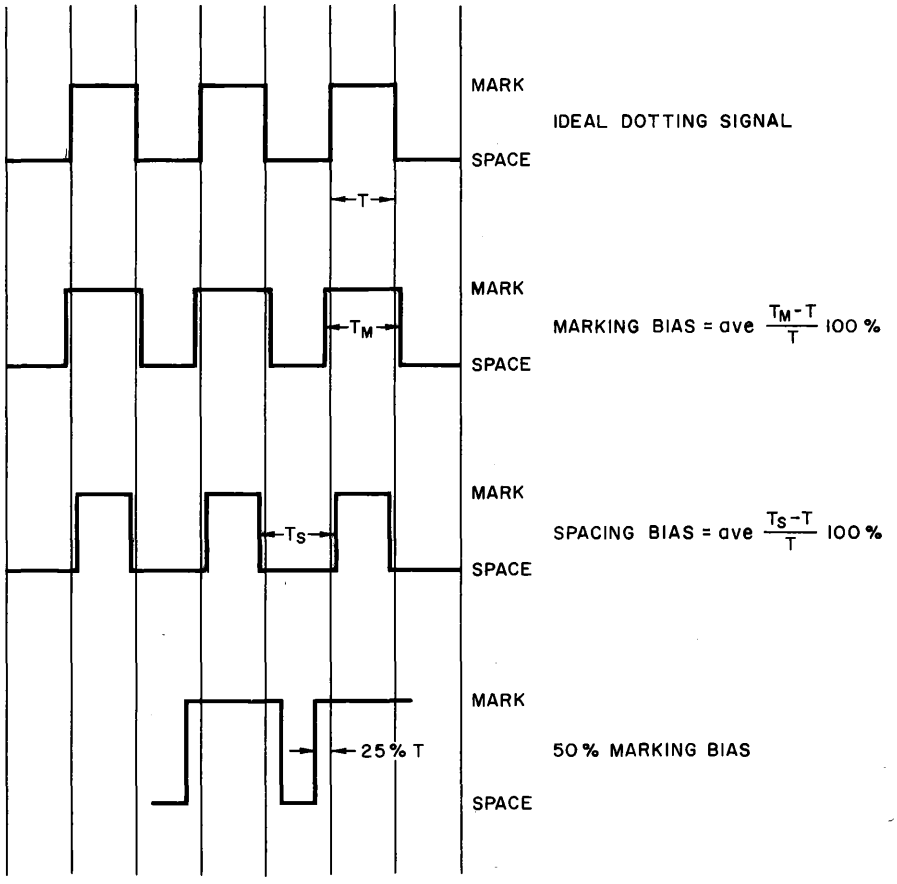


Fig. 7 — Definition of Bias Distortion

1.14 Distortion can be introduced in the frequency shift keyed signal by noise, amplitude distortion, and phase distortion. Phase distortion is usually given in terms of envelope delay distortion. There is in addition, of course, the inherent distortion of the modulator and demodulator but in the 906A this is kept to a minimum and should be minor compared to the amount of distortion necessary to cause transmission trouble.

1.15 Fig. 8 shows the effect of delay distortion and noise on data distortion. Along the abcissa is plotted the difference in envelope delay from space frequency to the mark frequency.

B. Generation of Test Data Signals (Table A)

1.16 Test signals are generated by the signal generator and the frequency shift keyed (FSK) modulator. The signal generator generates a baseband data signal much like that from the teletypewriter. The modulator performs the function of the subscriber's data set in converting the baseband signal into an FSK signal.

1.17 The various bit rates and signal formats that the signal generator can produce are listed in Table A along with controls that select them. The steady mark and space signals can be used to make transmission or frequency offset tests. The quasi-random signal is for making peak distortion measurements. Since the data system has some memory, the distortion of any transition will depend somewhat on the message that preceded it. Therefore, in measuring distortion it is necessary to generate different characters. The dotting signal is used in making bias distortion measurements. The biased dotting signal can be used as a self-checking feature.

1.18 The modulator output can be in either of two frequency bands, F1 or F2, have any of various powers, or be predistorted with delay distortion (see Table A). The subscriber subset transmits signals in either the F1 band which is centered around 1170 cps or the F2 band at 2125 cps depending on whether it originated or answered the call. Hence, these are the two frequency bands in which the B1 data terminals can accept signals. The various output powers available from the modulator are shown in Table A. These powers correspond to the range of signals with which the B1 data carrier terminals are expected to operate. Delay distortion of a transmission facility is very difficult to measure directly so the 906A is used to measure the increase in data distortion due to adding a known amount of delay distortion and then using the relation giving the dependence of data distortion upon noise and delay distortion. A sample graph of this relation is given in Fig. 8. At low noise levels the data distortion is fairly constant until the delay distortion exceeds about 2 msec. Thus, the delay distortion of a facility may be checked by adding a known amount of delay distortion. If the delay distortion of the facility is too great, the added delay distortion will cause the data distortion to increase sharply. This is the purpose of the delay predistortion networks. Since in the B1 terminal both F1 and F2 are shifted to the same line frequency (the particular frequency is determined by the channel assignment), the predistortion is built in for the F1 band only.

C. Signal Generation for Sectionalizing B1 Supervisory Channel (Table B)

1.19 The signal generator and the modulator are used to generate the test signal. In this function, they take the place of the supervisory multiplexer and modulator in the transmitting portion of the B1 data terminal.

1.20 The signal generator can generate signals with the same formats as for the data signal, but since the supervisory channel is designed for a bit rate of 95.5 bps, only that bit rate is used. The modulator produces an FSK signal centered about 350 cps with mark equal to 385 and space equal to 315. The output power is equivalent to that transmitted from the B1 data terminal on the 4-wire facility.

D. Over-All Distortion Measurement (Table C)

1.21 This distortion measurement involves the F1/F2 demodulator, the distortion measuring circuit, and the display panel. The demodulator which converts the FSK signals in the F1 or F2 band to baseband signals performs the same function as the receiving subscriber data set. The distortion measurements described in 1.11 through 1.15 are performed by the distortion measuring

TABLE A

GENERATION OF TEST SIGNALS

Condition			Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
Output frequency band					
2125 cps (2025-2125)			F2	F2 operated; S unoperated	F2
1170 cps (1070-1270)			F1	F2, S unoperated	—
Output power					
	F2	F1			
	dbm				
HI	−4.7 ±0.8	+0.3 ±0.8	High end of AGC range in B1 data terminal	LEV2 operated; LEV1 unoperated	HI
NORM	−9.7 ±0.8	−4.7 ±0.8	Expected average power into B1 WADS trunk	LEV1, LEV2 unoperated	—
LO	−21.7 ±0.8	−16.7 ±0.8	Low end of AGC range in B1	LEV1 operated; LEV2 unoperated	LO
SUB AGC	−30.7 ±0.8	−25.7 ±0.8	Below threshold of AGC range in B1	LEV1, LEV2 operated	HI, LO
Delay predistortion			Usable at F1 only		
−delay			1.4 msec more delay at 1045 cps than at 1295 (see Fig. 7)	D− operated; D+, F2 unoperated	D+
+delay			1.4 msec more delay at 1295 cps than at 1045 cps (see Fig. 8)	D+ operated; D−, F2 unoperated	D−
none			————	D+, D− unoperated	—
Bit rate					
95.5 bps			Bit rate of B1 supervisory channel	GS2, GS4 operated GS1, GS3 unoperated	GS2, GS4
110 bps			Bit rate of 4-row, 100 words per minute teletype which is used for WADS	GS1, GS4 operated GS2, GS3 unoperated	GS1, GS4, GS2
150 bps			The design objective for a 3-link B1 connection	GS3, GS2 operated GS1, GS4 unoperated	GS3, GS2, GS4

TABLE A (Cont)

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
Bit rate (Cont)			
200 bps	The address signaling rate of the FSP (frequency shift pulsing) outgoing sender	GS1, GS3 operated GS2, GS4 unoperated	GS1, GS3 GS2, GS4
Signal format			
steady space		A, B, C unoperated	—
steady mark		B operated; A, C unoperated	B
quasi-random	A 4-row teletype signal having a start bit, 8 information bits, and 2 stop bits per character; 63 different characters are produced before repeating.	A, B, C operated	A, B, C
dotting	Alternating mark and space bits	B, C operated;A unoperated	B, C
dotting with marking bias	Mark bits longer than space bits	A, C operated; B unoperated	A, C
dotting with spacing bias	Space bits longer than mark bits	C operated; A, B unoperated	C

circuit and are shown on the display panel which has a meter for indicating peak or bias distortion, an OUT SYN lamp, message register for counting occurrances of distortion in excess of a threshold, an OVFL lamp, a timer, and a CTR ON-CTR OFF switch.

1.22 The F1/F2 demodulator can demodulate signals which are modulated at bit rates as high as 200 bps, and the distortion measuring circuit, which shares the timing oscillator of the signal generator, can measure distortion of signals at bit rates of 95.5, 110, 150, and 200 bps.

1.23 When the distortion is caused by noise, the noise (and hence the data distortion) is not constant with time. This is especially true with impulse noise. Therefore, a brief distortion measurement with the meter could be misleading as to the quality of transmission. Thus, in some cases readings must be made for a longer length of time. The hit register can be set to count for predetermined periods of time by means of the timer. Thus a count of the number of distortion hits which exceeds a certain threshold can be made without presence of the tester. The automatically timed period can be up to 30 minutes in length. If at any time the mechanical register cannot count fast enough, an indication is given on the OVFL lamp. This lamp stays on to indicate that the true count is greater than the count registered on the message register.

E. Sectionalizing Tests on the 4-Wire Facility Narrow-Band (Tables D, E, F, and G)

1.24 The sectionalizing tests of the B1 data carrier system are made by means of the channel selector. It is designed to work in conjunction

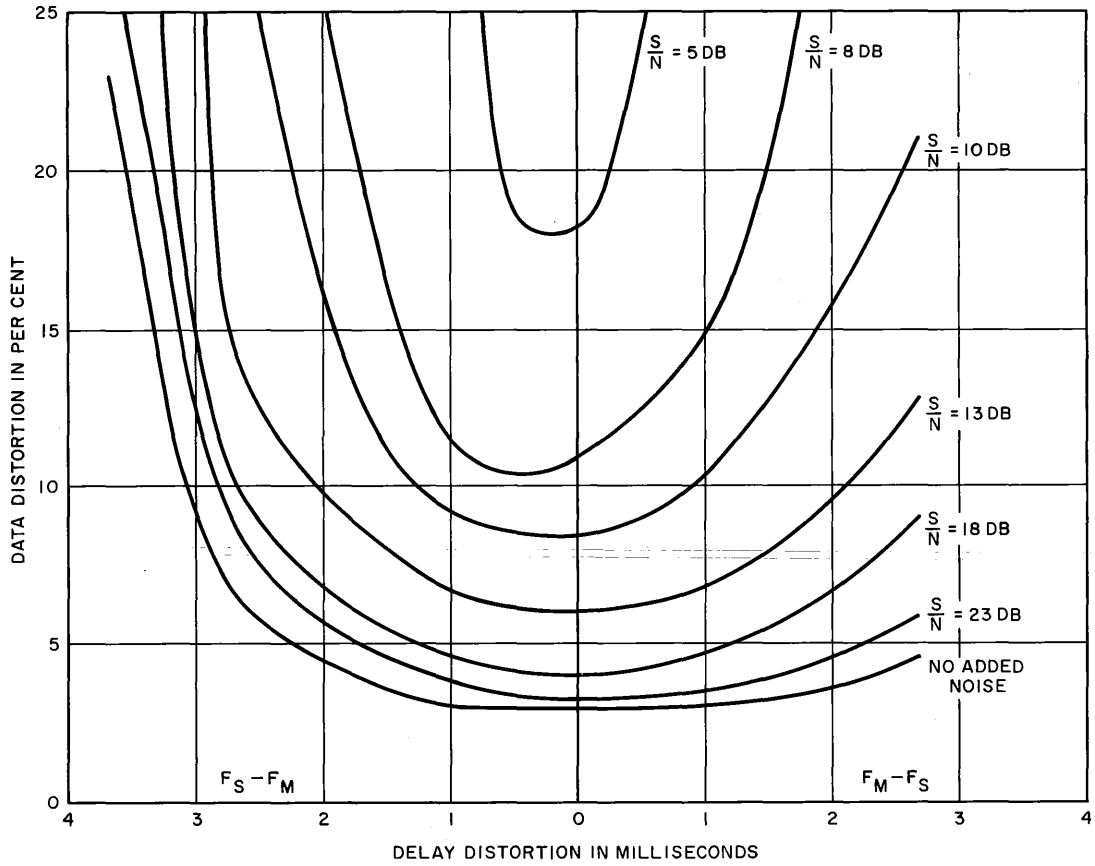


Fig. 8 — Effect of Noise and Delay Distortion on FSK Data Signals (150 bps)

with the MON jack which builds out the impedance of the 4-wire facility to approximately 10,000 ohms. The channel selector which has an input impedance of approximately 10,000 ohms can be connected across a 4-wire facility through a MON jack without degrading the normal operation of the B1 system. Furthermore, the channel selector uses the B1 data terminal receive filters to select any one of the data channels or the supervisory channel without interference from any other channel. (See Table D.)

1.25 The signal from the selected channel can be sent back to the data test cord circuit through which it may be connected to the appropriate measuring set for transmission noise or frequency offset measurement. (See Table D.)

1.26 By using the supervisory demodulator-demultiplexer, the signal from the supervisory channel can be demodulated and demultiplexed so that the E lead signals may be monitored and displayed on the SPV DEMULT lamps in the 20A jack field. Connections to these lamps are made through the SMC relay. When the supervisory demodulator-demultiplexer is shared by more than two positions, its output is connected to the proper set of lamps by the SMC relay associated with the position performing the test. (See Table E.)

1.27 To measure data distortion on one of the data channels, the channel selector shifts the signal from the channel frequency to the F2 frequency band. The signal can then be applied to the F1/F2 demodulator through contacts on the DDC relay so the data distortion can be measured as in 1.21 through 1.23. When the channel selector is shared by more than two positions, it is connected to the demodulator associated with the position performing the test by the DDC relay associated with that demodulator. (See Table F.)

TABLE B

SIGNAL GENERATION FOR SECTIONALIZING B1 SUPERVISORY CHANNEL

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
Frequency band 350 cps (315-385)	Frequency of supervisory channel	S operated; F2 unoperated	MDS
Output power −24 ±1 dbm	The nominal power of the supervisory signal transmitted from a B1 data terminal; this is the only available output power.	LEV1, LEV2 unoperated	—
Bit rate 95.5 bps	Bit rate of the supervisory channel; this is the only available bit rate.	GS2, GS4 operated GS1, GS3 unoperated	GS2, GS4
Signal format See Table A			

TABLE C

OVER-ALL DISTORTION MEASUREMENT

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
Frequency 1170 cps band (1070-1270)	F1	F1 operated	F1
2125 cps band (2025-2225)	F2	F1 unoperated	—
Type of data distortion measurement Peak (DTA)	Measures peak telegraph distortion with respect to stop-start transition; meter is disabled if stop-start transitions are lacking	BD, PS unoperated	—

TABLE C (Cont)

OVER-ALL DISTORTION MEASUREMENT

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
Type of data distortion measurement (Cont)			
Peak without framing (SUPV)	Measures peak telegraph distortion with respect to arbitrary mark to space transition; meter is not disabled when stop-start transition is lacking.	PS operated; BD unoperated	PS
Bias (BIAS)	Measures bias distortion on a dotting signal. BIAS key on display panel determines if MK or SPC bias is measured.	BD operated; PS unoperated	BD
Bit rate			
See Table A			
Distortion hit threshold (per cent)			
4	Distortion hit register is turned on and off by the CTR switch or the timer.	D1, D1-1, D2, D3 unoperated	—
8		D1, D1-1 operated; D2, D3 unoperated	D1
12		D3 operated; D1, D1-1, D2 unoperated	D3
16		D1, D1-1, D3 operated; D2 unoperated	D1, D3
20		D1, D1-1, D2, D3 operated	D1, D2, D3

1.28 To measure data distortion of the supervisory channel, the supervisory channel signal is connected to the supervisory demodulator. The demodulator output, a baseband signal at 95.5 bps, is connected to the distortion measuring circuit as well as the supervisory demultiplexer. Connection to the distortion measuring circuit is made through the SSC relay which disconnects the FSK data demodulator from the input of the distortion measuring circuit. When the supervisory demodulator-demultiplexer is shared by more than two positions, it is connected to the distortion measuring circuit associated with the position doing the testing by the SSC relay associated with that distortion measuring circuit. Distortion is measured as in 1.21 through 1.23. Since the demultiplexer is also connected to the demodulator, E lead signals may be monitored while making distortion measurements. It is also possible to use the distortion hit register to count the number of times the demultiplexer loses synchronism. The SL relay disconnects the distortion measuring circuit and connects the demultiplexer to the register. When the supervisory demodulator-demultiplexer is shared by more than two positions, it is connected to the register associated with the position performing the test by the SL relay associated with that register. (See Table G.)

F. Sectionalizing on the 4-Wire Facility, Voice-band (Table H)

1.29 In making data distortion sectionalizing tests on voice-band circuits, the demodulator and distortion measuring circuit are used in the same way as for over-all distortion measurements of the B1 data carrier system. The only difference is that the signal is connected to the demodulator through the DMC relay.

1.30 A summary of possible operations is shown in Table I.

G. Calibrating and Self-Testing Functions

1.31 Calibrating and self-testing features are provided for checking the performance of the signal generator modulator, demodulator, and distortion measuring circuit. Calibration adjustment of the meter is discussed in Part 5. A local test mode, in which the modulator is connected to the demodulator through the LT relay and a 20-db pad, is provided so that distortion may be measured for all the conditions of the transmitted data signals.

1.32 For checking the calibration and operation of parts of the word generator and the distortion measuring circuit, a distortion calibrator circuit is incorporated in the 906A and consists of one circuit card and the calibrator panel. The distortion calibrator is capable of distorting certain bits in the quasi-random sequence from the signal generator of the 906A. The amount of distortion is varied by the setting of the DIST potentiometer. Rotation in a clockwise direction increases the amount of distortion. In order to calibrate the distortion measuring circuit, the OFF-TST key and the MDM-SG key must be operated to TST and SG. For normal operation, they must be operated to OFF and MDM. If either key is not normal, the red warning lamp will be on. The distortion calibrator has the following modes of operation.

1.33 *Single Hit Every Complete Sequence (63 Characters of the Signal Generator)*: Used for checking the distortion meter on single hits and for timing the sequence of the word generator. The sequence of 63 characters takes 7.26 seconds at a bit rate of 95.5 bps; therefore, a single hit should occur every 7.26 seconds at this bit rate.

1.34 *Burst of Five Hits Every 63 Characters*: For testing the counter in the distortion hit indicator. If the distortion produced by the distortion calibrator is greater than the setting on the DIST CTR switch on the 20A toll testboard and if the CTR ON-CTR OFF switch on the display panel is operated to CTR ON, a burst of five hits will occur every 63 characters indicating that the distortion counter is counting correctly. The measuring circuit must be in the SUPV mode. If it is the DTA mode, only one hit is counted since the burst of five occurs in one character.

1.35 *Continuous Hits*: Used for calibrating the meter on the distortion measuring set. The calibration points are determined by the threshold at which the hit counter starts to indicate, and the error in the meter can be determined as a difference between its reading and the setting on the DIST CTR switch. If the meter reading increases smoothly as the potentiometer is rotated

TABLE D

SECTIONALIZING TESTS – TRANSMISSION, NOISE, FREQUENCY OFFSET

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
To measure level, frequency, noise	Output of channel selector connected back to data test cord circuit.	SMC, DDC, TMC unoperated	—
Channel selection			
Channel 1		CH1 operated	CS1
Channel 2		CH2	CS2
Channel 3		CH3 other CH relays unoperated	CS3
Channel 4		CH4	CS4
Channel 5		CH5	CS5
Channel 6		CH6	CS6
Supervisory		CH7	CS7

TABLE E

SECTIONALIZING TESTS – SUPV MONITOR

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
To monitor supervisory channel E lead signals	The signals are displayed only on the lamps associated with the position performing the test since only the SMC relay associated with that position operates.	SMC, TMC operated	SMC
Select supervisory channel	This also supplies demultiplexer with necessary clock signal.	CH7, operated; CH1 through CH6 unoperated.	CS7

TABLE F

SECTIONALIZING TESTS — DATA DISTORTION

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
To measure data distortion on data channels	The distortion measurement appears only on the display panel associated with the position making the test because only the DDC relay associated with that position operates. Demodulator conditioned for F2.	DDC, TMC operated	DDC
Channel selection See Table D	The carrier frequency needed to shift from the channel frequency to F2 is automatically supplied to the channel demodulator according to which data channel is chosen.		
Type of data distortion measurement See Table C			
Bit rate See Table A			
Distortion hit threshold See Table C			

TABLE G

SETIONALIZING TESTS — SUPV CHANNEL DISTORTION

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
To measure data distortion of supervisory signal See Table E	The distortion measurement appears only on the display panel associated with position making the test because only the SSC relay associated with that position operates.	SMC, SSC, TMC operated	SSC, SMC
Select supervisory channel See Table E			
Type of data distortion measurement See Table C	Cannot make DTA test.		
Bit rate See Table A			
Distortion hit threshold See Table C			
Sync loss count	Disconnects distortion hit register from distortion measuring circuit and connects it to supervisory demodulator-demultiplexer.	SL operated	SL

TABLE H

SECTIONALIZING TESTS — WIDE BAND

Condition	Comments	Controlling Relays in 906A	Leads Grounded by Data Test Cord Circuit of 20A
To connect demodulator to 4W facility		DMC operated	DMC
Type of distortion measurement See Table C			
Bit rate See Table A			
Distortion hit threshold See Table C			
Frequency band			
1170 cps (1070-1270)	F1	F1, DMC operated	F, DMC
2125 cps (2025-2225)	F2	DMC operated; F1 unoperated	DMC

evenly clockwise, this suffices to indicate that the distortion counter is working at other than the calibrating points.

1.36 *Bias*: Used mainly as an indication that the distortion calibrator is working. If a 908A logic circuit test set, set to indicate bias, is plugged into either the D1 or D2 test point on the distortion calibrator panel and if the distortion calibrator is working, a bias indication will be indicated on the meter. This bias indication should be approximately half that indicated on the meter on the 906A.

1.37 *Modem or Back-to-Back*: If the MDM-SG key is set to MDM, the output of the modem is fed to the input of the distortion measuring circuit. This is fed through the buffer inverter (8-12) on CP8 to the distortion measuring circuit for normal operation of the 906A. If the MDM-SG key is in the SG position, the output of the word generator is connected through the buffer inverter to the distortion measuring circuit for checking calibration of the distortion measuring circuit.

2. SIGNAL GENERATOR

2.01 The following outputs are available from the signal generator:

(a) Quasi-random 11-bit characters, starting with a start pulse (space); 8 bits of quasi-random data; and stop pulse (mark), 2 bits long.

(b) A dotting signal, consisting of alternate mark and space, each exactly 1 bit long.

(c) Dotting with +12.5 per cent distortion. Mark is 9/8 of a bit long, space 7/8 bit.

(d) Dotting with −12.5 per cent distortion. Mark is 7/8 of a bit long, space 9/8 bit.

(e) Steady space.

(f) Steady mark.

Examples of these are shown in Fig. 6 and 7.

2.02 Output is available at 4 bit rates: 95.5, 110, 150, and 200 bps.

TABLE I

OPERATIONS OF HORIZONTAL LINE

Summary of Possible Operations	All Operations on a Horizontal Line May Be Performed Simultaneously with Restrictions Listed			
	Signal Generation	**Distortion Measurement**	**Narrow Band Section-alizing**	**Wide Band Section-alizing**
(a) Signal generation (a1) Data signals to data trunk on 2-wire side of B1 data terminal (Table A) (a2) Signal in supervisory band to 4-wire side of B1 data terminal (Table B)	(a1) 1	(b) 1	(c1) OR (c2)	
(b) Over-all distortion measurement (Table C) (b1) Bias distortion (b2) Peak telegraph distortion (b3) Distortion hit count	(a1) 1	(b) 1		(d2)
(c) Narrow band sectionalizing tests at 4-wire (c1) Transmission, frequency, noise (Table D) (c2) Monitor E lead state (Table E) (c3) Measure distortion on data channels (Table F) (c4) Measure distortion on supervisory channel (Table G)	(a2) 1 2	(b) 1	(c1) OR (c2) 2	
	(a2) 1 2	(b) 1		(d2) 2
	(a2) 1 2		(c) 1 2	
	(a2) 1 2			(d) 1 2
(d) Wide band sectionalizing tests at 4-wire (d1) Measure data distortion (Table H) (d2) Transmission, frequency, noise (906A not used)	(a1) 1		(c1) OR (c2) 2	(d1) 1 2
(e) Self testing feature (e1) Meter calibration adjustment (e2) Local test including calibration check (e3) Local test of supervisory circuit	(a1) 1		(c3) OR (c4) 1 2	(d2) 2
	local test (e2) (e2)		(c1) OR (c2)	(d2)

Restrictions: 1. Must be performed at same bit rate.

Restrictions: 2. Restricted by data test cord circuit; must be done at different test position.

2.03 Fig. 9 is a simplified functional schematic for the signal generator.

CLOCK CIRCUIT

2.04 The clock circuit consists of a crystal oscillator and a 10-stage countdown chain (A1 through A10). In the oscillator, there is a common output stage and a separate first stage for each crystal. The correct frequency is chosen by applying +12 volts to the appropriate first stage through relays GS1 and GS3. The OSC frequencies are at 1024 times the bit rate. At A10, the OSC frequency has been divided down by 2^{10} (1024). Hence, the frequency there is at the bit rate.

2.05 A crystal oscillator is used for accuracy and stability since an error of ±0.01 per cent in the frequency of the oscillator can introduce 0.18 per cent distortion into data distortion measurements.

STOP-START PULSES

2.06 The B binary counter chain (B1, B2, B3, B4) is driven at the bit rate by the output of the oscillator countdown (A10) and is reset every 11 bits by the monopulser (MP). Gate STRT forms a start pulse, one bit long. Gate STP forms a stop pulse, two bits long. A stop pulse is always followed by a start pulse.

QUASI-RANDOM CHARACTER GENERATOR

2.07 The quasi-random character is produced by the shift register and the exclusive-OR circuit EXO. Every negative going transition on the clock line causes the reading in the shift register to advance one position to the right. The EXO puts a 1 in the first stage when the states of SR5 and SR6 differ and puts a zero in when the states of SR5 and SR6 are the same. Gate ADO keeps the clock line at ground during the time when the start and stop pulses appear in the output. Output gates SS and W1 insert the start and stop pulses into the quasi-random characters. This process is shown graphically in Fig. 9. There are 63 different characters of 11 bits each before the sequence is repeated.

2.08 EIN causes the EXO circuit to put a 1 into the first state of the shift register when the shift register is in the state 000001 or 000000. 000001 occurs eight times every 693 bits. If the shift register should go in the state 000000 when power is first turned on, the EIN circuit causes a one to be shifted into the first shift register stage; otherwise the quasi-random word generator would not start.

2.09 In each 11-bit character there are eight data bits, hence there is a total of 2^8 (256) possible characters. Of these, the 63 which are produced are considered enough to give an accurate indication of performance for the narrowband data channel under test. Disturbances which are set up on the line by mark to space or space to mark transition have no significant effect beyond the third bit, and hence it is unnecessary to produce all possible 8-bit combinations.

DOTTING

2.10 For dotting signals, the B binary acts as a simple frequency divider. This is done by blocking the MP with +12 volts through the A, B, and C relays. The frequency at A10 is at the bit rate. The frequency at B1 is one-half the bit rate, which means one-half cycle equals one bit. This forms the desired dotting signal. B2, B3, and B4 are not used in this mode.

2.11 Dotting with 12.5 per cent marking or spacing distortion is available at the output of the DIS circuit. This is done by subtracting 1/8 bit from the trailing edge of alternate bits.

OUTPUT SWITCHING

2.12 Fig. 10 shows the output switching circuitry. On the DM lead, a positive voltage of 4 to 5 volts dc corresponds to mark, and ground corresponds to space. The signal on the DS lead is an inverted version of the DM signal.

3. MODULATOR

3.01 A block diagram of the frequency shift modulator of the 906A is shown in Fig. 11. In order to give a low distortion frequency shift signal with precise mark and space frequencies, the basic modulator consists of two crystal con-

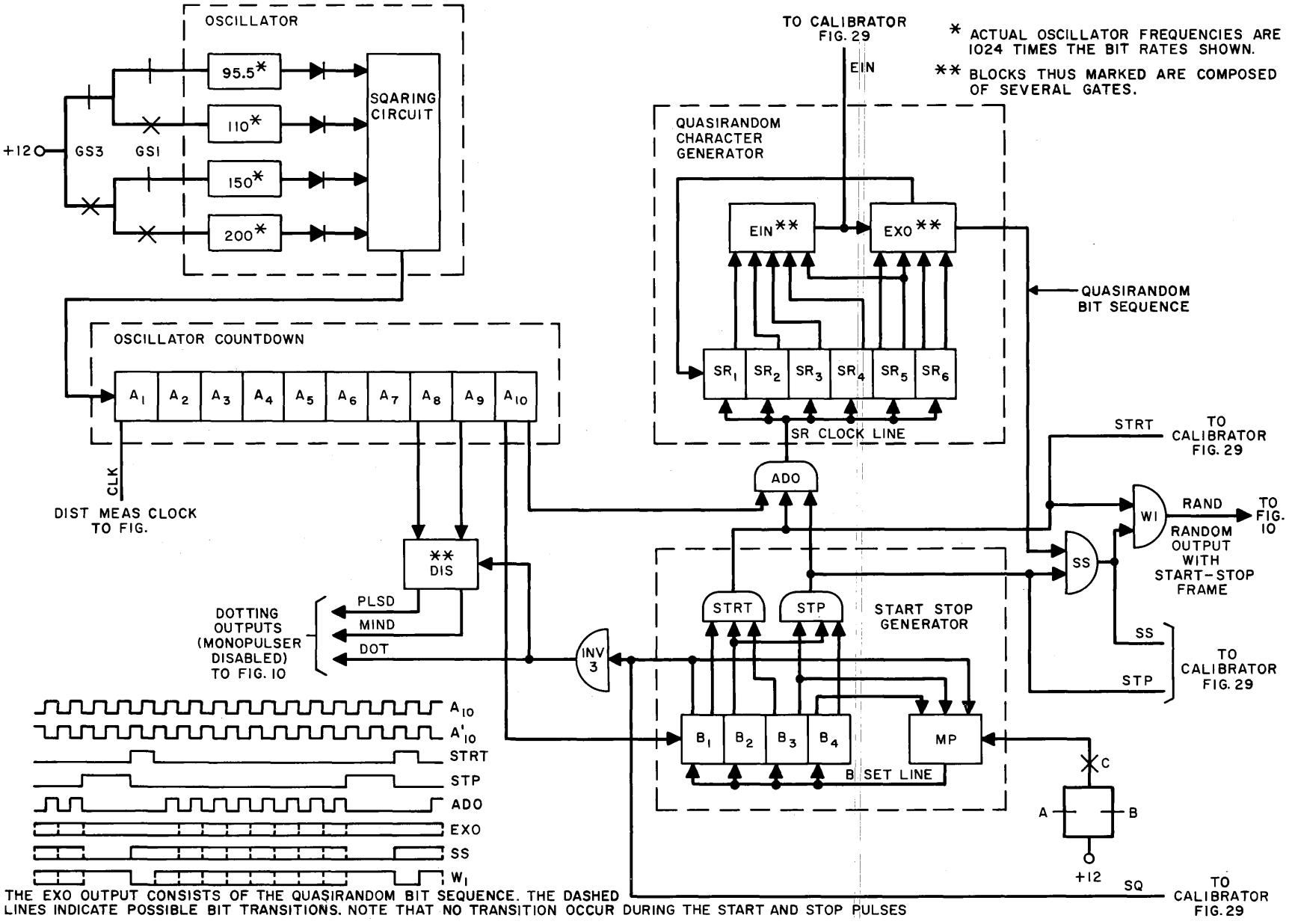


Fig. 9 — Signal Generator — Simplified Functional Schematic

trolled oscillators, one at 128 times the mark frequency and the other at 128 times the space frequency. The output of these oscillators is shifted back and forth from one oscillator to the other according to the data pattern, and their frequencies are divided through a frequency divider consisting of a 7-stage binary counter and passed through the appropriate filter, delay distortion network, line amplifier, and pads to bring the signal to the desired level.

3.02 Four oscillators are provided, two for data signals and two for supervisory signals, and are selected through gates by the contacts of the S relay. When the S relay is operated, the data oscillator is inhibited and vice versa. The data signal is fed to the oscillator DS-DM leads and by means of the controlling gates determines whether the outut of the mark or space oscillator is selected.

3.03 Operating in the data mode, there are two pairs of crystals for F1 (originate) and F2 (answer) frequencies. These crystals are selected by means of the contacts of the F2 relay. When the F2 relay is operated, the F2 frequency is selected and vice versa. The signal is filtered through supervisory, F1, and F2 filters; these filters are selected by means of contacts on the S and F2 relays. The characteristic for the F1 filter is shown in Fig. 12. The F2 filter is essentially the same but centered around 2125 cps. The characteristic for the supervisory filter is shown in Fig. 21.

3.04 In order to do marginal testing on the B1 data trunk, slope delay of ±1.4 msec across the F1 band (Fig. 13 and 14) is provided and selected by contacts on the D+ and D− relays. When the delay networks are not in the circuit, a pad with the same attenuation is provided so that no level changes are made when the delay networks are inserted.

3.05 Various levels are provided: normal, high, low, and SUB AGC (level below which the automatic gain control of the B1 data carrier terminal is not supposed to take effect). The attenuators are selected by contacts of the LEV1 and LEV2 relays. The signal on the output of the attenuators is presented to the data test cord circuit.

4. F1/F2 DEMODULATOR (Fig. 15)

4.01 The demodulator of the 906A is a conventional frequency shift demodulator consisting of the following functional blocks:

(a) Line transformer.

(b) Line amplifier.

(c) Line filter.

(d) Limiter.

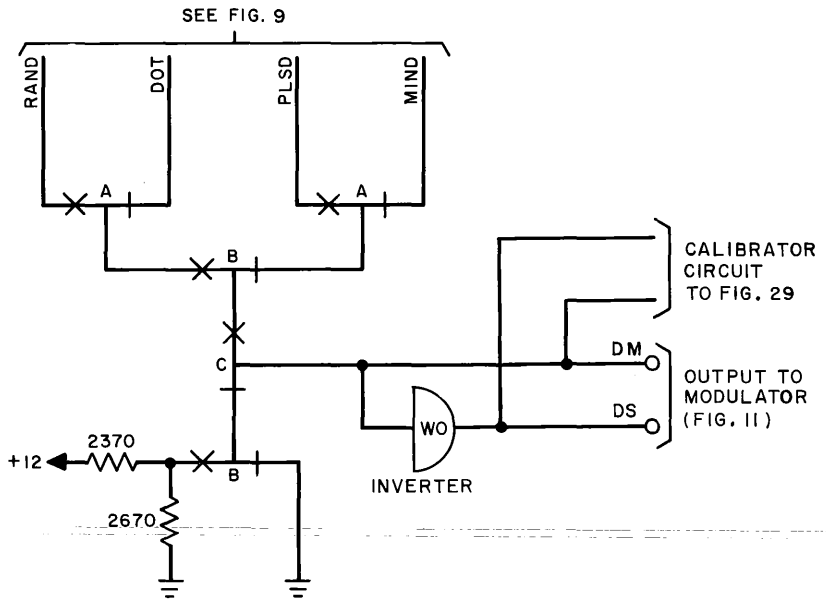
(e) Discriminator (including full-wave rectifiers).

(f) Low-pass filter.

(g) Slicer.

4.02 The F1/F2 demodulator has an input signal range of −12 to −48 dbm. The frequency shift signal enters the line transformer balanced and is fed from the line transformer unbalanced, through the line amplifier to the line filter. The signal is then fed to the limiter. The output of the limiter consists of two square waves 180 degrees out of phase, which are fed to a balanced discriminator. The discriminator consists of balanced push-pull transistor drivers feeding the primaries of tuned transformers. The tuned transformers are tuned to slightly below the space and above the mark frequencies. The outputs of the tuned transformers are fed to two full wave rectifiers. The outputs of the full wave rectifiers are passed through a balanced low-pass filter (option G) or individual low-pass filters (option F) which serve to remove carrier frequency components and harmonics, as well as noise appearing in the signal. A differential variable load on the two filters is supplied by means of a potentiometer in order to adjust for bias errors in the demodulator. The output of the low-pass filter is fed to a balanced slicer, which may be thought of as a saturating differential amplifier. The output of this slicer is then fed to the distortion measuring circuit.

4.03 As the discriminator is designed for both F1 and F2 frequencies, F1 and F2 line filters are provided and are switched in and out by means of the contacts on the F1 relay which



RELAY POSITION	OUTPUT
ABC	RANDOM
$BC^{'}$	STEADY MARK
$AB^{'}C$	DOTTING WITH SPACE BIAS
$B^{'}C^{'}$	STEADY SPACE
$A^{'}BC$	DOTTING
$A^{'}B^{'}C$	DOTTING WITH MARK BIAS

PRIME DESIGNATION ($A^{'}, B^{'}, C^{'}$) MEANS RELAY IS NOT OPERATED.

Fig. 10 — Signal Generator — Output Signaling Circuitry

is controlled from the 20A toll testboard. Tuned circuits are required and are selected by means of a relay on the F1 and F2 discriminator card (F1A relay), which in turn is switched by a contact on the F1 relay. Similarly, bias adjustment potentiometers are provided for both F1 and F2 and are switched by means of the contacts on the F1 relay.

5. DISTORTION MEASURING CIRCUIT

5.01 The measuring circuit accepts data in the form of dc levels (+4.5 volts or ground) and measures very accurately the data distortion present in these signals (see Fig. 16).

5.02 The distortion is read out by means of a meter indicating peak distortion on a random signal or bias on a dotting signal. A hit counter records hits of distortion above a preselected level in the SUPV mode of operation. (The counter counts the number of characters that have one or more hits of distortion over the preselected level in the DTA mode.) In this mode, peak telegraph distortion is measured with respect to stop-start transitions. In the SUPV mode, peak telegraph distortion is measured with respect to arbitrary mark to space transitions, and the meter is not disabled if the stop-start transitions are lacking. Peak distortion of a telegraph signal is defined as shown in Fig. 6.

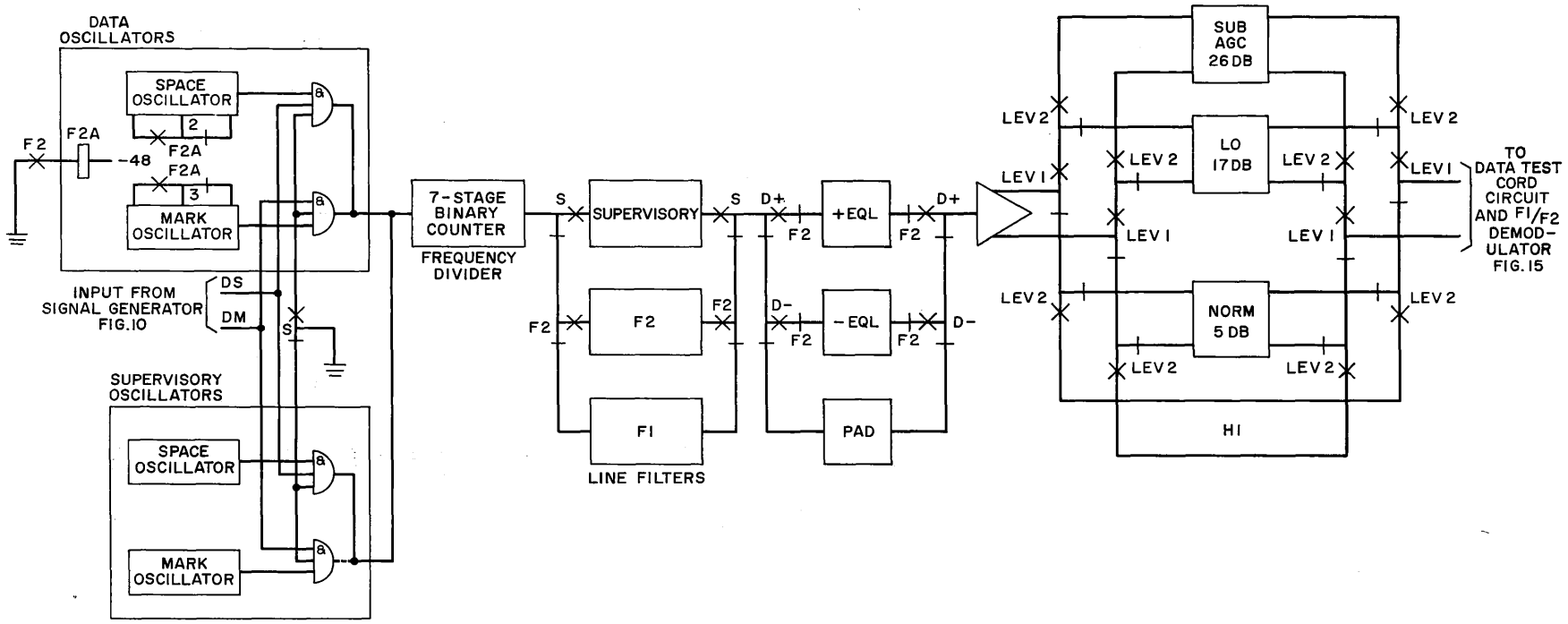


Fig. 11 — Modulator — Simplified Functional Schematic

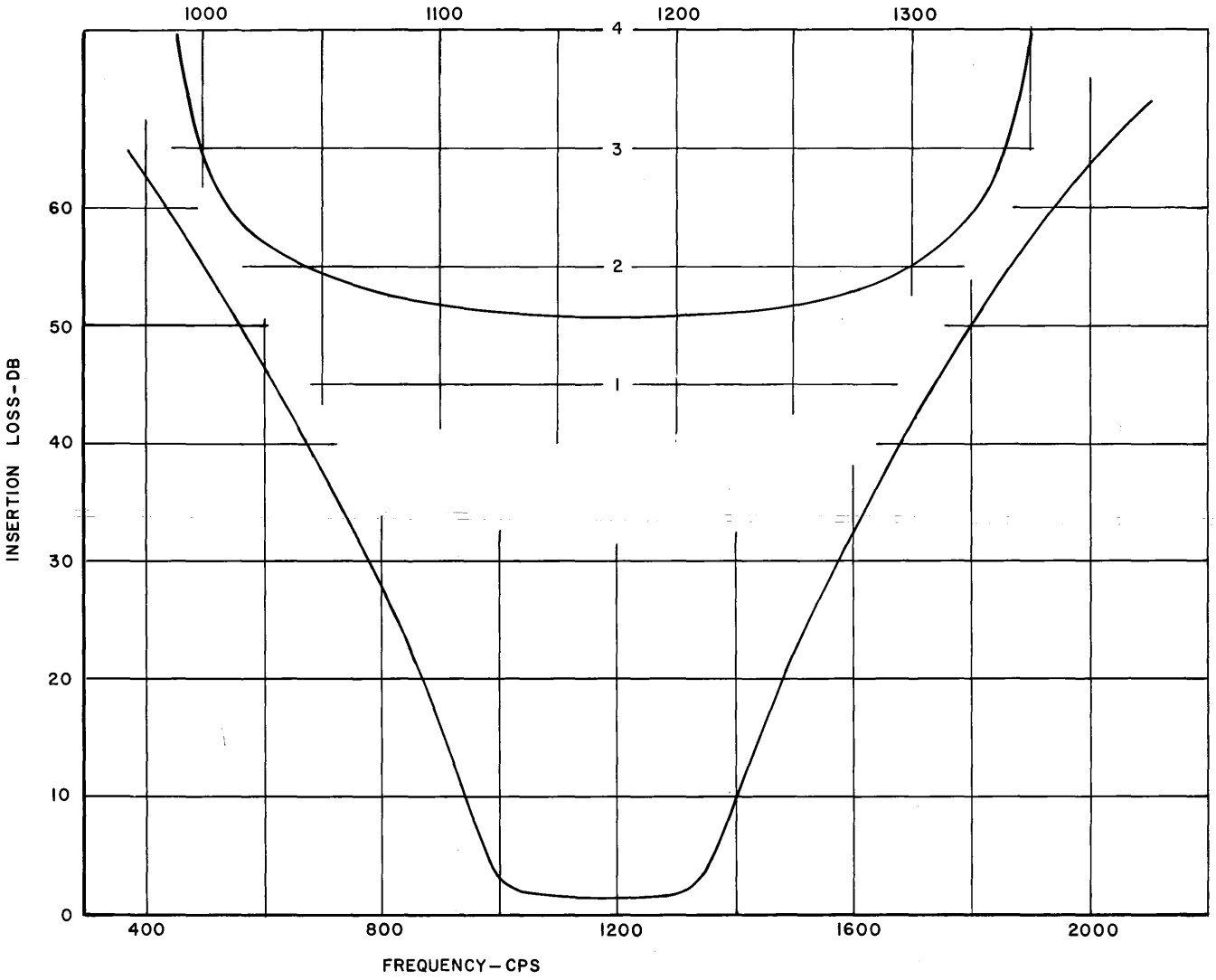


Fig. 12—F1 Line Filter (Insertion Loss)

DESCRIPTION OF OPERATION IN THE DTA MODE (Fig. 17)

5.03 A negative going transition from stop to start is detected by the transition detector.. The transition detector causes the frame sync logic to allow the counter reset and clock circuit to rest the binary counter and feed clock pulses to it. The binary counter starts counting at the stop to start transition. All measurements in any character are with respect to this stop-start transition.

5.04 Each data transition that occurs in the character (the start-stop readout inhibit blocks readings during the stop-start transition) causes the transition detector to operate the gate enabling circuit. The gate enabling circuit allows the count in the binary counter to be sampled. This sample is then translated into an equivalent per cent distortion (see definition Fig. 6) which is then loaded into distortion registers. These distortion registers hold the reading until the next transition occurs. The distortion reading is converted to analog form by the digital to analog converter circuit. The output of the digital to analog converter drives a display circuit which causes a meter to indicate the magnitude of any distortion hit. After the hit of distortion is registered by the meter, the needle tends to drop very slowly, thus increasing the ease and accuracy of

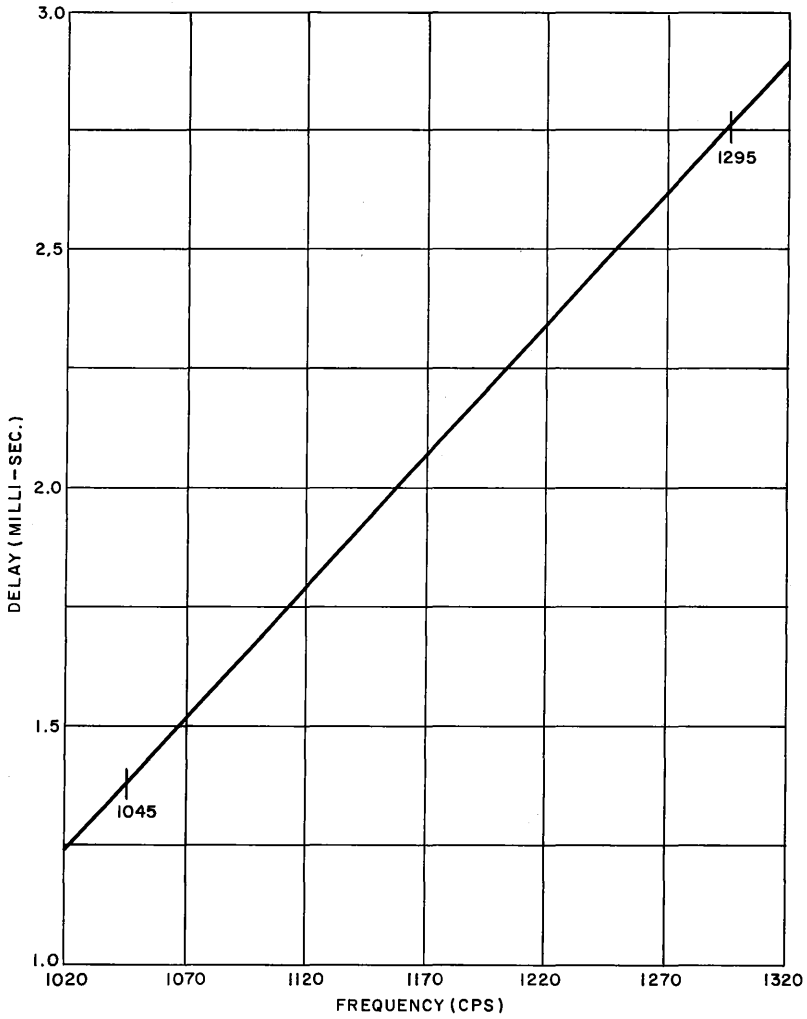


Fig. 13 — Delay Characteristic of Plus Delay Predistortion Network

reading peaks of distortion. A discharge circuit causes the reading to drop rapidly after a 1-to-3-second wait (long enough for an observer to note the reading). This feature makes it possible to get more readings in a given period of time. If a new peak of higher distortion occurs before the meter drops, the new reading will be indicated and the discharge circuit will start timing for another 1-to-3-second period.

CHARACTER SYNC CHECKS

5.05 The frame sync logic verifies the occurrence of two marks (the stop) at the end of each character followed by a mark to space (stop to start) transition (see Fig. 18). If any check fails, the counter gets reset and the sync register circuit indicates an out of synchronism condition by means of an OUT SYN lamp. During this out of synchronism condition, no measurements are made. The circuit waits for the next negative going transition which is assumed to be a stop to start transition. At this transition, the binary counter begins to count. After nine bits have passed, the above mentioned stop-start checks are made. The frame sync counter circuit counts the number of characters that pass these tests. If four characters in succession pass, the sync register indicates in sync, and readings are made from that time as before. Now the OUT SYN

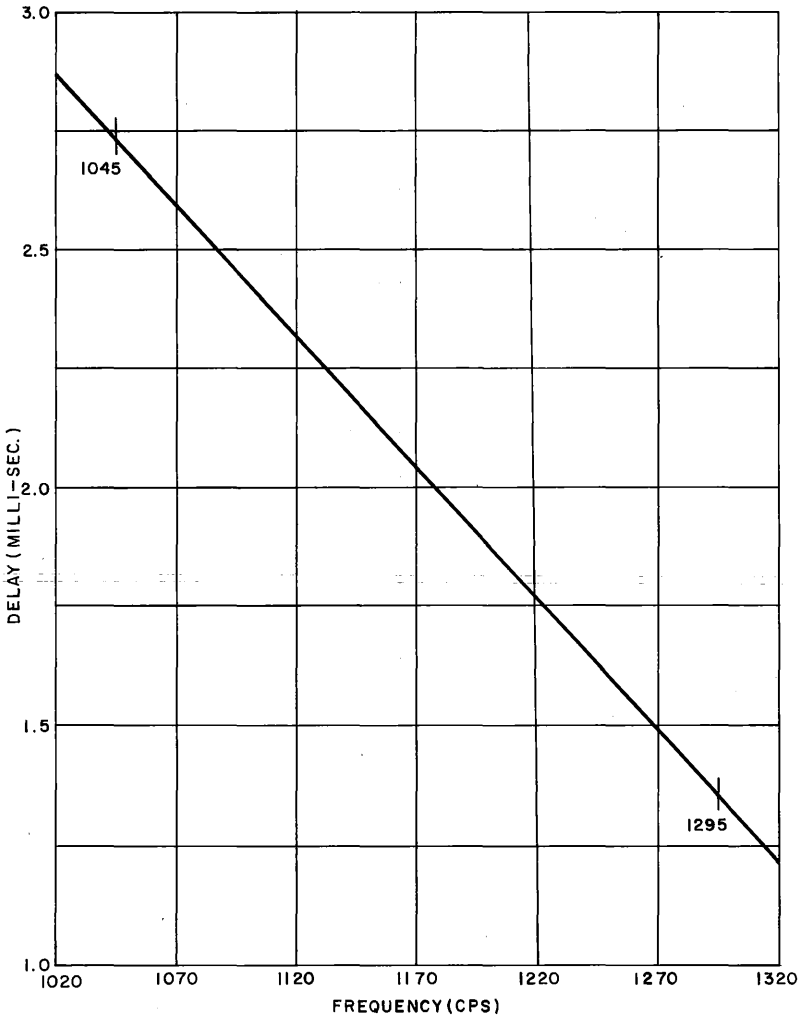


Fig. 14 — Delay Characteristic of Minus Delay Predistortion Network

lamp can be extinguished by means of the SYN RESET button on the display panel.

HITS ABOVE THRESHOLD FOR DTA AND SUPV MODES

5.06 The threshold detector circuit picks transitions which are distorted by an amount greater than a preselected threshold. (4, 8, 12, 16, and 20 per cent levels may be selected by the D1, D1-1, D2, and D3 relays in the distortion threshold circuit). When the timer is set, the RST-ST key is depressed and the TMR lamp lights. While this lamp is on, hits will be recorded unless the timer is bypassed.

5.07 In the SUPV mode the distortion hits picked by the threshold detector are fed into a buffer. Once every character, the buffer is sampled. If there are any counts stored in the buffer at this time, the hit counter circuit puts a count of one in the message register and, at the same time, subtracts one count from the buffer. The buffer circuit is necessary because hits can occur too fast for the message register to handle them. If hits occur so fast that more than seven get stored in the buffer, the OVFL lamp goes on, and some hits are not counted although the circuit still functions. A switch on the display panel (CTR ON-CTR OFF) enables one to bypass the timer circuit and time tests manually. Set switch to CTR ON. In the DTA mode, the buffer store circuit is disabled from the circuit since it is

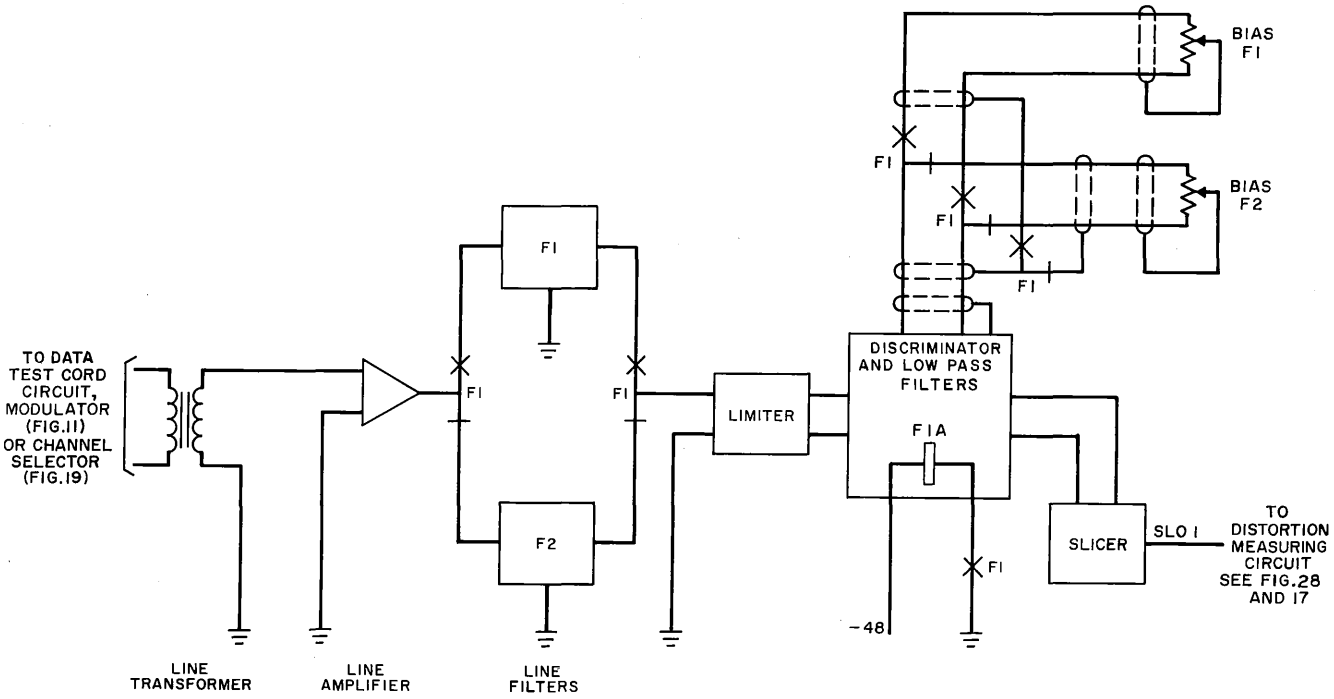


Fig. 15 — F1/F2 Demodulator — Simplified Functional Schematic

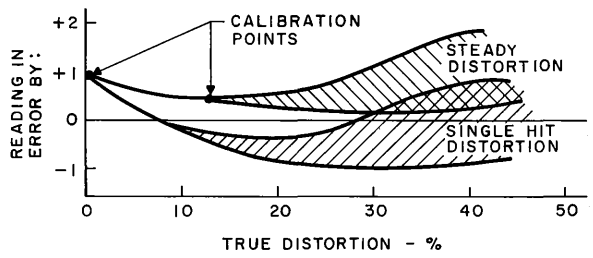


Fig. 16 — Typical Expected Accuracy of 906A Data Distortion Meter

desired to count characters and the message register is capable of counting at the character rate.

BIAS MEASUREMENT

5.08 In this mode, the BD relay is operated. This causes all negative transitions to reset the main binary counter. Measurements are made of each positive going transition with respect to the previous negative going transitions. The meter indicates the average of all the measurements. The threshold detector circuit is made inoperative while bias measurements are being made. If the OUT SYN lamp is on, it will go out and stay out when the SYN RESET button is reset.

5.09 Marking and spacing bias are not measured at the same time. (See definition Fig. 7.) To measure either marking or spacing bias, the MK-SPC switch must be in the correct position.

SUPV MODE

5.10 The PS relay is operated. The measuring circuit works the same way in this mode as it does in the DTA mode except that readings are made even if the circuit is not in sync, and the counter counts hits in the SUPV mode and distorted characters in the DTA mode. Consequently, peak distortion measurements can be made on signals such as the supervisory signal of the B1 data carrier terminals which do not have the telegraph stop-start format.

5.11 If the OUT SYN lamp is on, it will go out and stay out when the SYN RESET button is depressed. The threshold circuit also works in this mode.

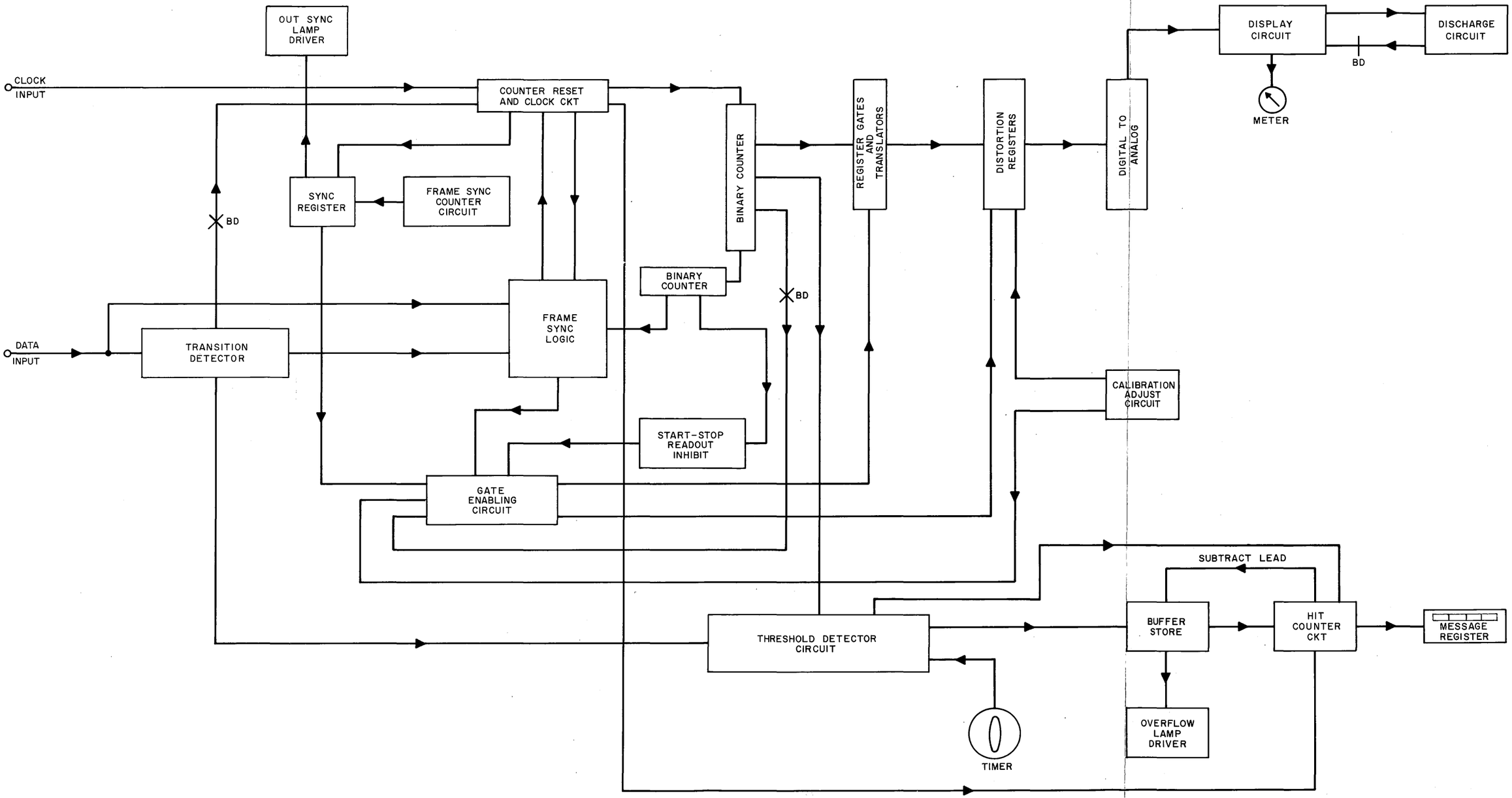


Fig. 17 — Distortion Measuring Circuit — Simplified Functional Schematic

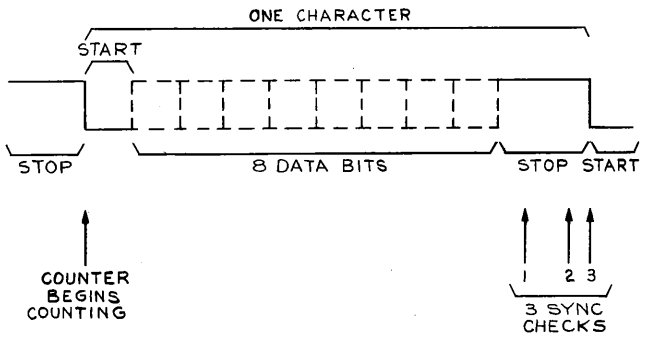


Fig. 18 — Checks Made by Sync Logic

CALIBRATION ADJUSTMENT

5.12 To adjust the calibration of the meter, operate the HI CAL-LO CAL switch to LO CAL. Adjust the LO CAL potentiometer until the meter reads 0. Move the switch to HI CAL and adjust HI CAL potentiometer so that meter reads 12. Again operate the switch to LO CAL and adjust potentiometer so that meter reads 1. Operate HI CAL-LO CAL switch to normal. This procedure adjusts the meter circuit to give the expected accuracy.

READING THE METER

5.13 In order to measure the magnitude of a distortion hit to the greatest degree of accuracy with the meter, the highest point reached by the needle must be read. The needle will reach a peak and fall back to a rest point momentarily before being discharged 1 to 3 seconds later. This rest point is not the distortion reading to be made.

6. CHANNEL SELECTOR (Fig. 19)

6.01 The channel selector permits high impedance monitoring of the B1 signals on the 4-wire facility. The 4-wire facility is connected through resistors in the MON jack to the high impedance input of the bridging amplifier which is followed by a receive channel filter for each of the six data channels and the supervisory channel (Fig. 20). These filters are of the same design as the B1 receive filters and permit selecting the signal from one channel without interference from others. The output from the filter corresponding to the desired channel is selected by the appropriate channel selector relay (CH1 to CH7). If data distortion measurements are to be made on either the data channels or the supervisory channel, relay TMC is operated.

6.02 If transmission, noise, or frequency offset measurements are to be made on equipment mounted elsewhere in the 20A testboard, the relay TMC is not operated and the signal from the selected channel is connected through a pad and transformer back to the data test cord circuit. Since the loss of the filter may vary not only from channel to channel but for a given channel, the gain of the bridging amplifier is usually adjusted to the loss of each filter by contacts on the channel selector relays. The amplifier has three gain-adjusting resistors. Each resistor has an associated contact on each of the seven channel selector relays. By using all combinations of resistors, eight different gain settings are available. Thus by choosing the right resistor combination, the gain of an amplifier can be matched to the loss of a filter. By wiring the correct combination of resistors to each channel selector relay, the amplitude of the signal delivered to the meters can be closely matched to the 4-wire facility.

6.03 If data distortion is to be measured on one of the six data channels, the operated TMC relay connects the selected channel signal to the channel demodulator which performs the same function as, and is essentially identical to, the receive portion of the channel circuit in the B1 data terminal. It shifts the signal from the channel frequency to the F2 band so that the signal can be demodulated by the FSK demodulator. The channel demodulator consists of a pad, a switch-type demodulator, another pad, a low-pass filter, and an amplifier. The carrier frequencies for the demodulator are obtained from the B1 carrier supply. There is one oscillator frequency for each channel, and the appropriate one is connected to the channel demodulator by a channel selector relay. Just as in the B1 terminal, there are three different low-pass filters: one for channel 1, one for channel 2, and one for all other channels. The correct filter is chosen by the channel selector relays.

6.04 If the supervisory signal is to be examined (distortion measured or E lead states monitored), the operated TMC relay connects the signal from the supervisory filter directly to the super-

visory demodulator. The 3820-cps signal needed by the supervisory demultiplexer is connected through contacts on the CH7 relay and the isolation transformer to the supervisory demultiplexer.

7. SUPERVISORY DEMODULATOR-DEMULTIPLEXER DEMODULATOR

7.01 The purpose of the demodulator (CP61 and CP63) is to convert an FSK signal, shifting between 315 cps and 385 cps, transmitting a 95.5-bps data train, into an equivalent baseband pulse train. The 315 cps is demodulated as 0.2 volt output, while 385 cps is demodulated as +5.2 volt output. The transmission is through a narrow-band filter shown in Fig. 21 which has a nominal half power bandwidth of 150 cps centered around 350 cps. The end to end transmission characteristic including both send and receive filters has a nominal halfpower bandwidth of approximately 135 cps.

7.02 The demodulator consists of a sensitive limiter, a discriminator, and a slicer. The limiter accepts signals as high as +10 dbm and continues to provide full limiting for signals as low as −60 dbm (at the limiter input). The travis-type discriminator provides an output proportional to frequency between 315 and 385 cps. The slicer or squaring circuit switches abruptly between high and low states as the discriminator output crosses through a preset threshold. The BIAS control on CP63 is the control which sets this threshold (normally close to the ac zero value of the discriminator output). The demodulator is shown in block form in Fig. 22. A typical dis-

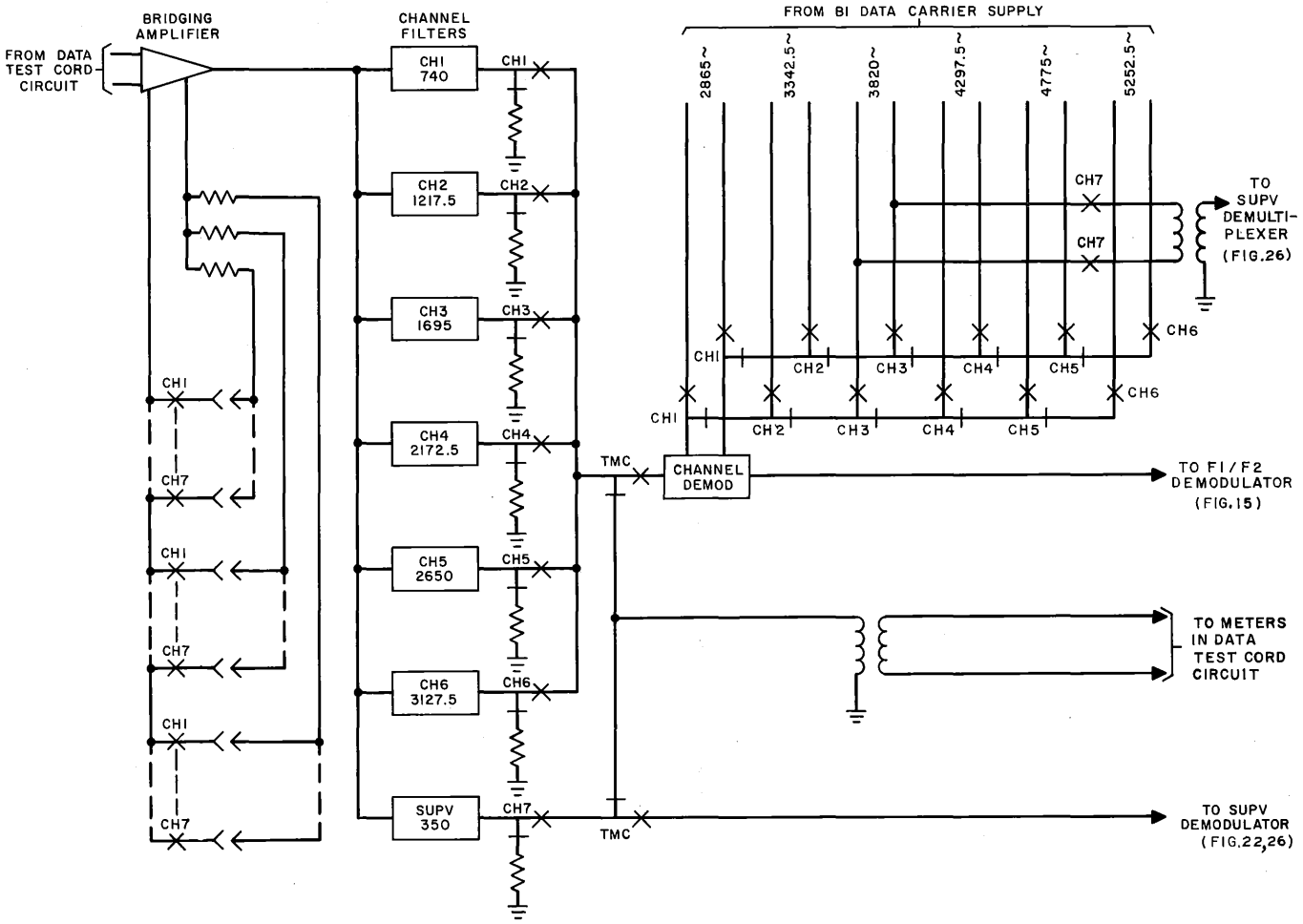


Fig. 19 — Channel Selector — Simplified Functional Schematic

criminator frequency versus response curve is shown in Fig. 23 and the typical output wave form and the corresponding slicer output are shown in Fig. 24.

7.03 If noise is present at significant levels along with the signal being monitored, the discriminator output, with several supervision frames superimposed, is as in Fig. 25. The corresponding slicer output is also shown.

7.04 Since the noise admitted to the receiver is of varying amplitude and in varying phase relation to the FSK signal, it affects, in a random manner, the time position of the zero crossings of the received wave that are presented to the discriminator. These time changes in the zero crossings in turn affect the discriminator's response, producing perturbrations in the discriminator output. The slicer, which follows the perturbations of the discriminator at the threshold crossings, distorts the pulse lengths. It is clear that if the positions of all positive going transitions are superimposed and we observe the pulse lengths until the negative going transitions occur, the noise will cause the pulse length not to be a contant, but to vary from pulse to pulse. We would expect that a tabulation of all pulse lengths, assuming that all pulses were the same length when transmitted, over a period of time would show that pulses nearer the transmitted value occur more frequently than those deviating greatly from the transmitted value. However, in a few cases this deviation from the transmitted value can be so severe as to cause a sampling error in the supervisory data train or loss of synchronism. The effects of such errors are discussed under the demultiplexer; however, a deviation of 50 per cent of the pulse length in the negative going pulse edge is sufficient to cause an error and may be taken as an "ideal" error criterion. Since such a deviation is not frequently encountered, we may predict how often such deviations do occur by observing deviations of a smaller magnitude which occur more frequently and predict the relative occurence of those of large magnitude. For this reason, the binary wave train, at the output of the demodulator is made available to the distortion measuring circuit where the penetrations of the various preset thresholds may be counted in a timed period.

7.05 There are two other contributions to pulse length distortion which affect supervisory error rates, although the exact effect of the combination of this distortion with distortion due to noise is not simple addition. These sources are modulator or residual distortion and facility distortion. Facility distortion consists of two components, amplitude and phase; phase distortion is generally given in terms of envelope delay distortion. Both modulator distortion and facility distortion are constrained in the case of the supervisory signal and are of smaller magnitude than the peaks of distortion introduced by noise. Distortion due to noise is not necessarily constrained to values below 50 per cent.

7.06 In order for distortion measurements to be made on the supervisory signal, a high input impedance, low output impedance inverting stage is provided to drive the distortion measuring circuit at either the local or a distant position. This inverting stage bridges the demodulator's binary output (lead (BI) without appreciable loading. The actual load on lead BI is provided by the demultiplexer.

DEMULTIPLEXER

7.07 The demultiplexer, shown in Fig. 26 and 27, operates on the demodulated data train obtaining synchronism and then, once synchronized with the distant terminals, it sequentially gates samples of the data train into registers known as the E lead memory. The registers change state corresponding to presence of samples on the SET lead or on the RESET lead. The sequential gating, the data sampling, and the frame timing are all derived from a 3820-cps square wave which is in turn derived from a sinusoidal 3820-cps wave provided through the channel selector circuit from a remote B1 data carrier terminal carrier supply circuit. The synchronism state of the demultiplexer is presented to the 20A attendant by means of the SYN lamp with lamp-on denoting synchronism. The six E lead states are presented by six lamps (SPV DEMULT) with the lamp on corresponding to on-hook. These lamps are located in the jack field which is easily seen from the 20A attendant position.

7.08 The data train transmitted by a B1 data carrier terminal consists of S1 and S2 bits,

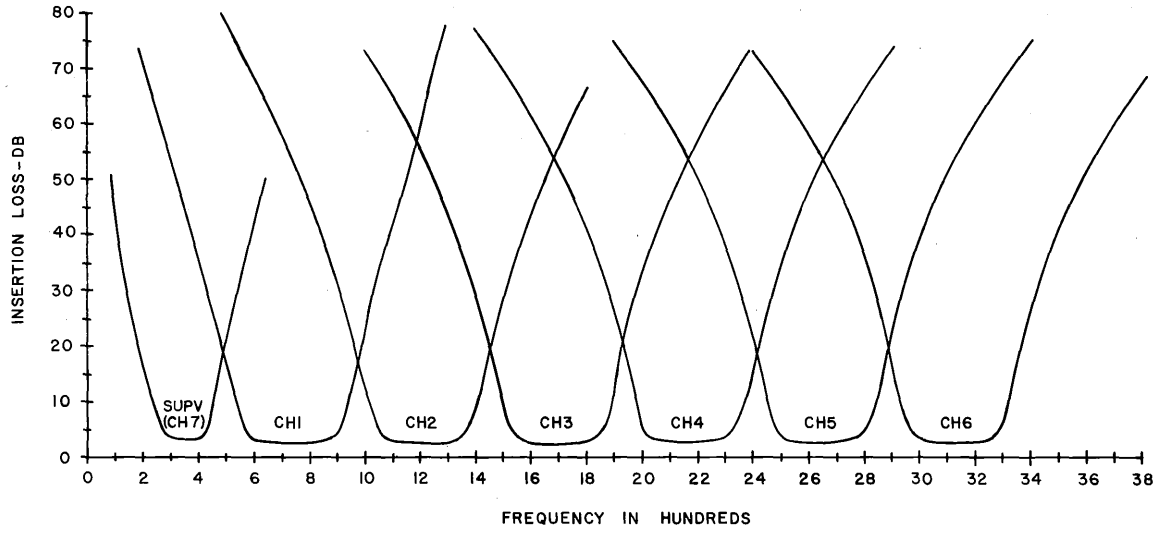


Fig. 20 — Channel Receive Filter

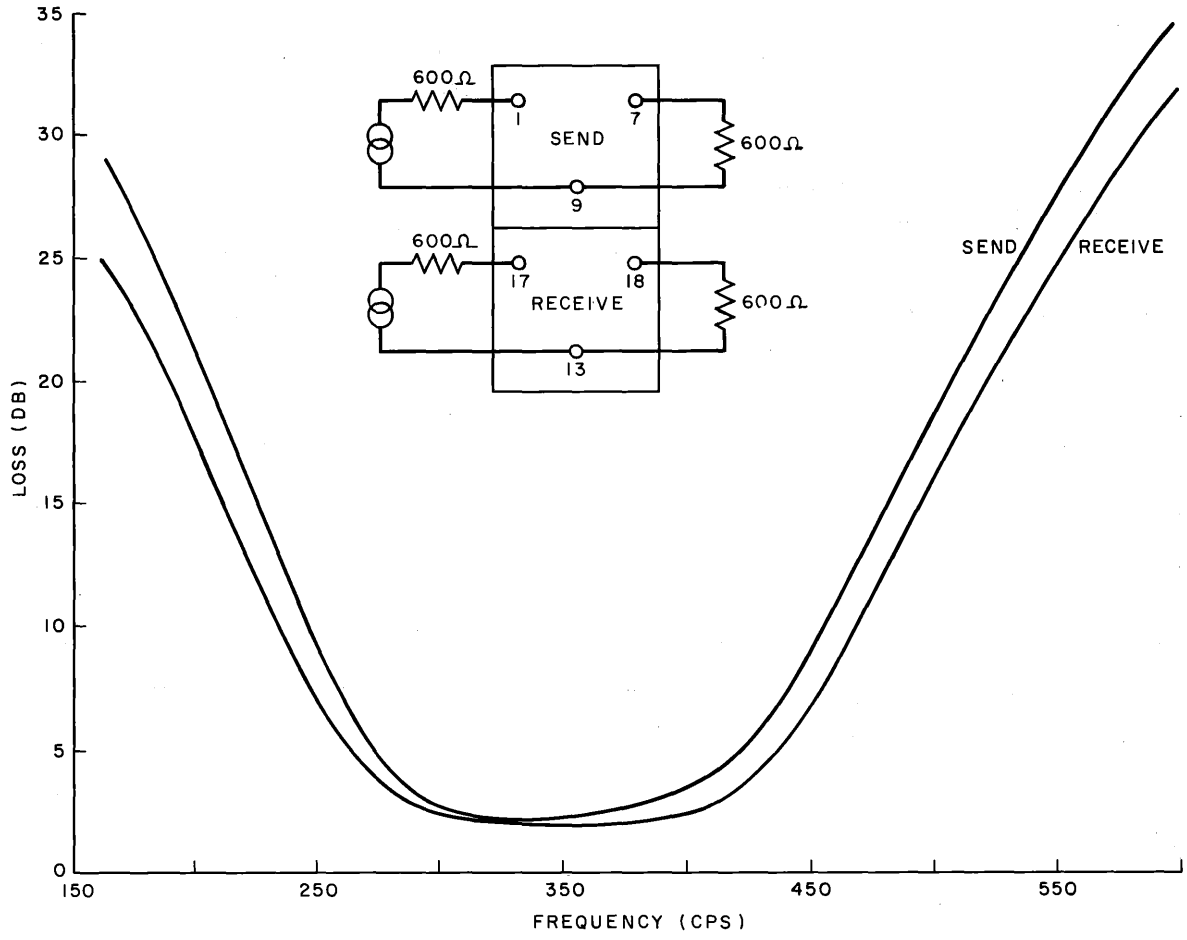


Fig. 21 — Loss-Frequency Characteristic of Supervisory Channel Filter

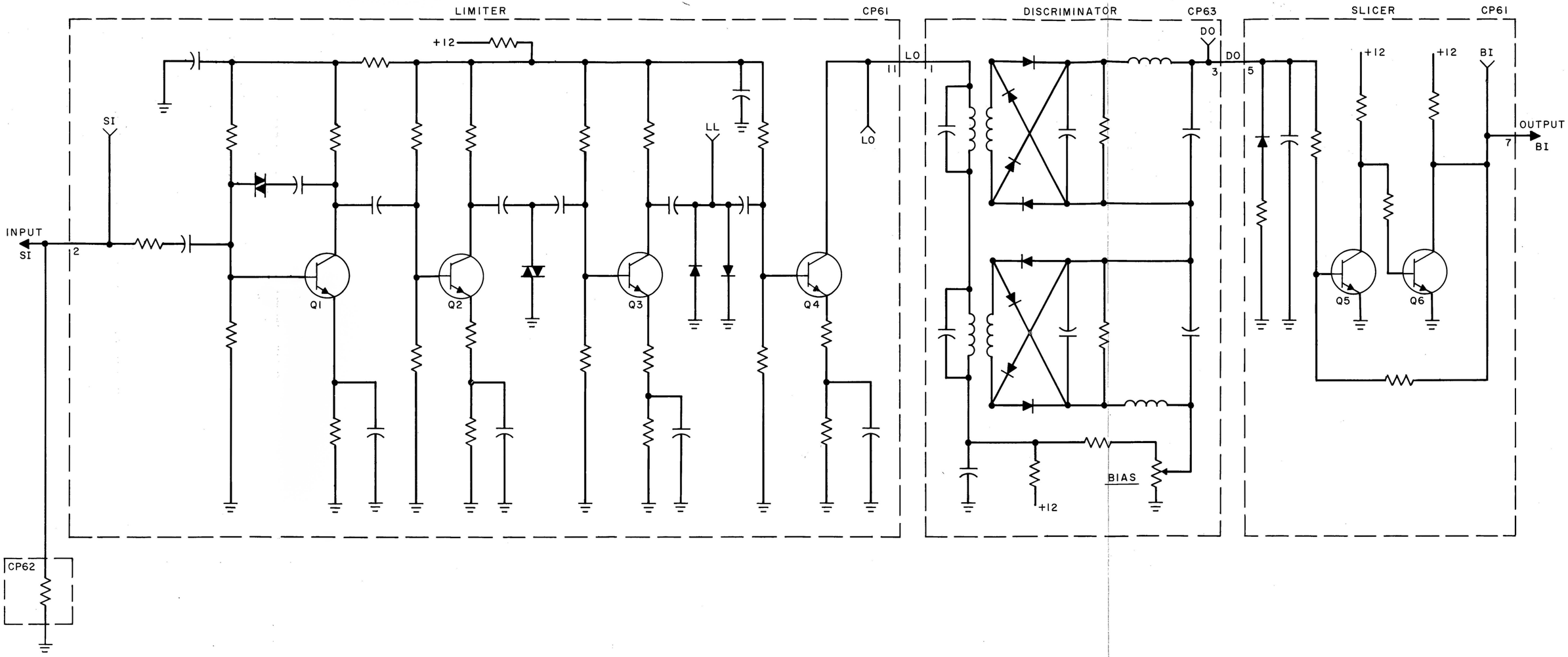


Fig. 22 — Supervisory Demodulator

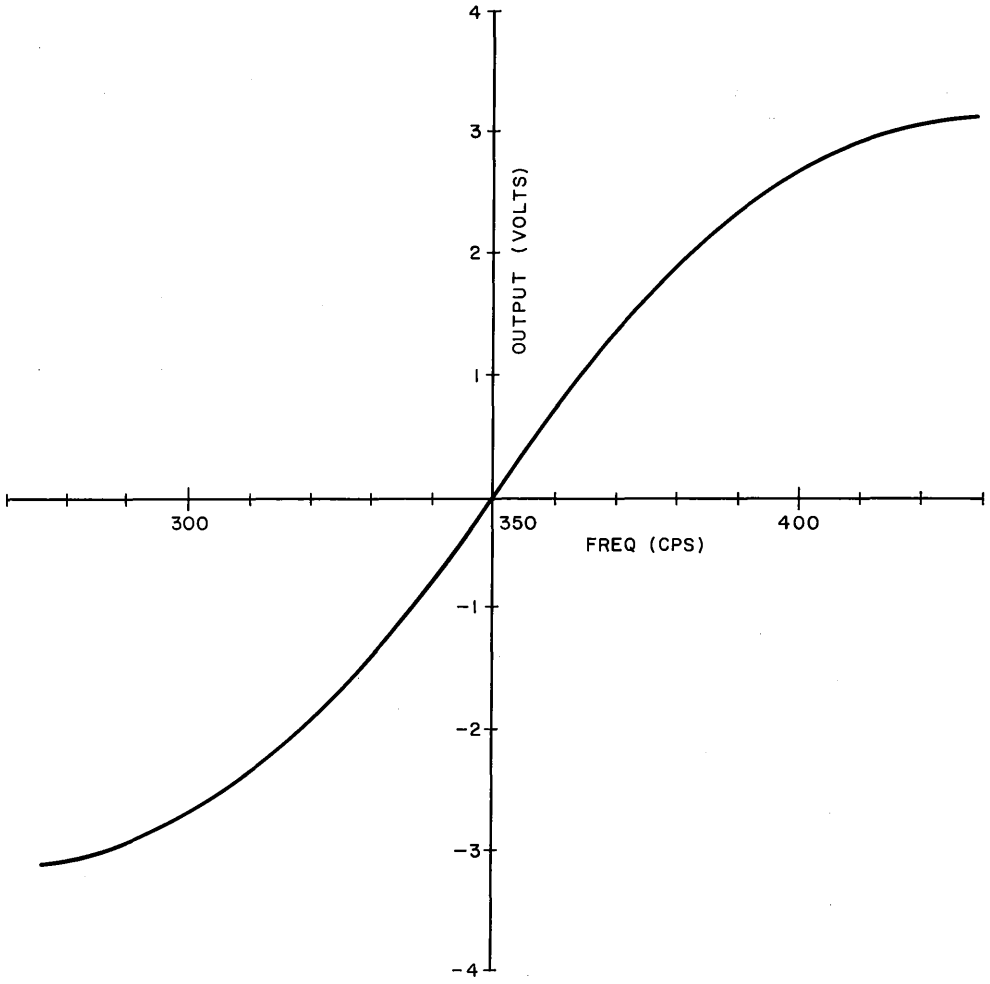


Fig. 23 — Typical Discriminator Response for the Supervisory Demodulator

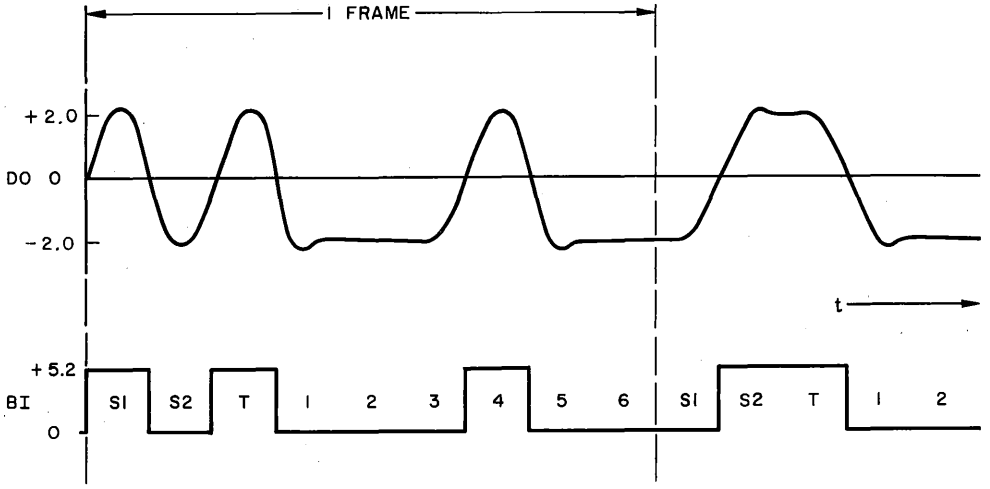


Fig. 24 — Discriminator Output and Corresponding Slicer Output Showing Synchronization Bits, S1 and S2, the Trouble Bit, and the Fourth Trunk Monitored in the Off-Hook State

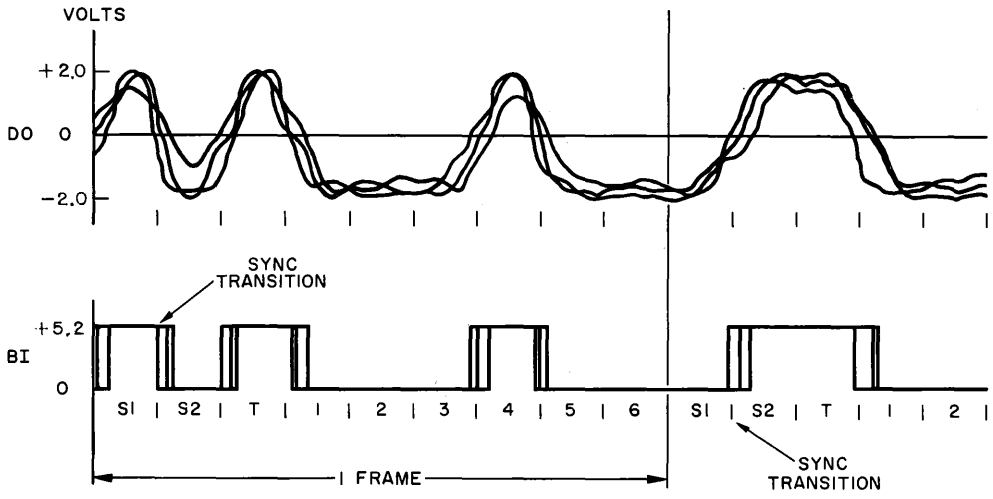


Fig. 25—Discriminator and Slicer Output Wave Forms as They Might Appear with High Noise Levels and Corresponding High Distortion

a "trouble" bit, and six bits which correspond to trunk state samples. The S1 and S2 bits are transmitted in alternate states in repeating frames, ie, at the beginning of frame A, S1 is high and S2 is low; at the beginning of frame B, S1 is low and S2 is high; the cycle then repeats. The trouble bit denotes the trouble status of the transmitting terminal, and, when indicating trouble, it constitutes a command to the distant terminal to make busy the six trunk circuits associated with that terminal. The six trunk state samples are low for on-hook and high for off-hook. A typical data train and sync recovery sequence may be found in Fig. 28.

7.09 The demultiplexer makes a decision as to whether synchronism exists between itself and the distant terminal once per frame. (A single frame is defined as S1, S2, trouble bit, and six bits for six trunk samples.) This decision is based on the S1 to S2 transition. Since the S1 and S2 bits alternate every frame, a negative going S1 to S2 transition in the previous frame must be followed by a positive going transition in the current frame and a negative transition in the next frame, and so on. In the circuit, the T monopulser generates the sync aperture pulse which corresponds to opening a time slot window (called T) to examine the transition direction between S1 to S2. If the direction agrees with the sync transition memory (H flip flop), the in-sync decision is made and the clock memory (G flip-flop) is reset to start the clock and hold the sync status memory (K flip-flop) in the in-sync state. The end of the clock period will initiate another test of synchronism. When the clock is started, it initiates a narrow sample pulse through the bit sample pulse generator, occuring in the expected center of each trunk lead sample.

7.10 If the expected direction of transition does not occur, an out-of-sync decision is made and the sync-status memory (K flip-flop) is set to the out-of-sync state immediately. At this point, the clock memory and the sync-status memory are such that the sync recovery sampling gates are opened and data train transition samples are applied directly to the sync transition memory. Upon the appearance of a transition of either direction, the sync transition memory is set or reset accordingly and the clock memory is reset to start the clock. With the clock started, the sync recovery sampling gates are closed. The clock times through eight bits, then starts the P monopulser which generates the aperture preparation pulse. This pulse in turn blocks the sync recovery sampling gates, changes the state of the sync transition memory, and starts the T monopulser generating the sync aperture pulse. If a transition arrives during the aperture pulse agreeing with state of the sync transition memory, an in-sync decision will be made; if no proper pulse arrives, the out-

of-sync decision reinitiates the process just described. In this way, out-of-sync causes the testing of transitions to move through the entire frame, transition by transition, until a decision can be made that synchronism exists. One synchronism is established, the sync status memory is reset to the in-sync state. Since the out-of-sync state has inhibited the sampled data train, no improper trunk state information has been entered into the E lead memory. When synchronism is recovered, the sampled data is presented to the E lead memory and the memory changes freely in accordance with the distant terminal trunk state samples.

7.11 A dotting signal, alternate high and low bits, can simulate sync since the uneven number of bits per frame (nine) results in alternate transition directions at the expected sync transition time. However, the similarity to a valid demultiplexer data train ends at this point since alternate frames will reverse all of the trunk state samples. For this reason, transmission of the dotting signal to a B1 data terminal that is not removed from service should not be attempted.

7.12 The foregoing discussion shows the importance of the precise location of sync transitions, but the discussion of the demodulator in 7.03 through 7.05 has pointed out that perturbations may exist in all transitions including the S1 to S2 transition. Sufficient perturbation of the S1 to S2 transition will result in the transition falling outside of the sync-aperture and an apparent loss of synchronism. It can be seen that two successive transitions displaced oppositely by 25 per cent of a bit from their normal location will be sufficient to produce a loss of synchronism. This amount of distortion would correspond to a reading of 50 per cent distortion on the 906A meter. In actual pratice, loss of synchronism may be somewhat more easily introduced. Manufacturing tolerances, power supply variation, and aging effects may change the periods of the P and T monopulsers of the B1 data carrier terminal sufficiently to reduce the 50 per cent ideally allowable distortion to 30 per cent. For this reason, special P and T monopulsers, which produce the sync-aperture have been used in the 906A demultiplexer. These monopulsers are more tightly controlled and are initially designed to agree with the worst expected distortion sensitivity in the B1 data carrier terminal supervisory signaling circuit. If the 906A demultiplexer can synchronize on a distant terminal multiplexer signal, a properly operating B1 data carrier terminal should also be able to acquire synchronization.

7.13 The synchronism state of the demultiplexer may be monitored by the distortion threshold counter in addition to being observed on the SYN lamp. This counter enables the 20A toll testboard attendant to obtain sync loss counts in a timed interval too extended for visual monitoring.

8. CALIBRATOR CIRCUIT (Fig. 29)

8.01 The distortion calibrator is capable of distorting certain bits in the quasi-random sequence from the signal generator of the 906A. The amount of distortion is controlled by the setting of the DIST potentiometer. Rotation in a clockwise direction increases the amount of distortion.

8.02 The impedance presented by the two buffer inverters (8-1 and 8-6) is high and will not load down any of the leads on the signal generator. If the TST key is off, the two OR gates (8-5 and 8-11) will be off and present a high impedance on the outputs to the rest of the signal generator. If the MDM-SG key is in the MDM position, the output of the demodulator goes through buffer inverter 8-12 to the DMS in the normal manner. In order to calibrate the distortion measuring circuit, the OFF-TST key and the MDM-SG key must be operated to TST and SG.

METHOD OF OPERATION

8.03 *Single Hit Every Complete Sequence (693 bits) of the Signal Generator (Fig. 30a):* With the MULT-SGL-BIAS key in the SGL position and the CONT-INT key in the INT position, a positive pulse on the EIN lead at the same time as a positive pulse on the STRT lead (this coincidence occurs only once per 693 bits) causes AND gate 8-2 to operate by means of the two buffer inverters (8-1 and 8-6) causing the flip-flop on CP8 to set. The zero side output of the flip-flop through OR gate 8-5 clamps the DM lead to ground. During the start pulse, the DM lead is normally at ground; however, when the pulse on STRT lead goes to ground, AND gate 8-2 turns on, causing a positive transition at the output of

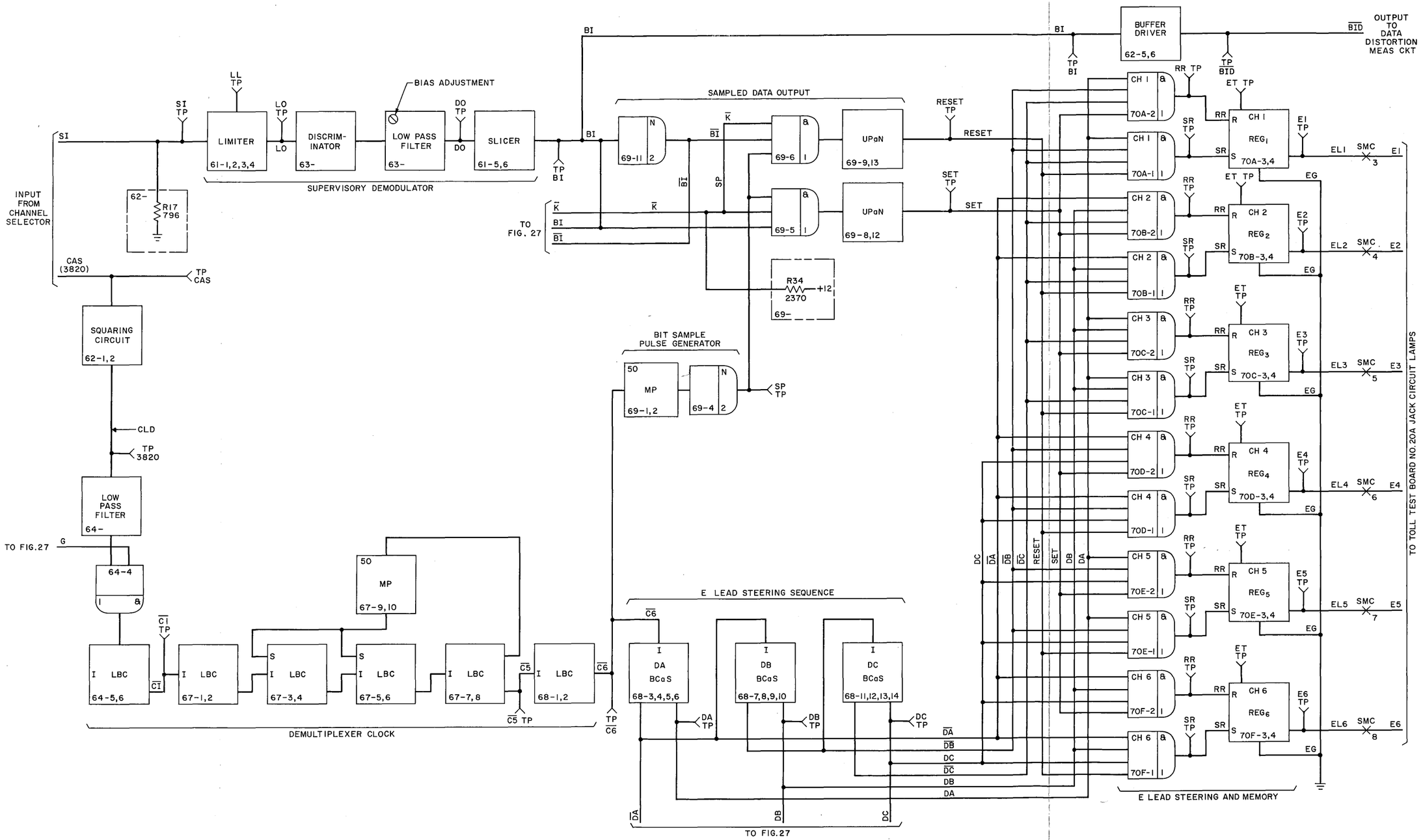


Fig. 26 — Supervisory Demodulator-Demultiplexer — Functional Schematic (Part 1)

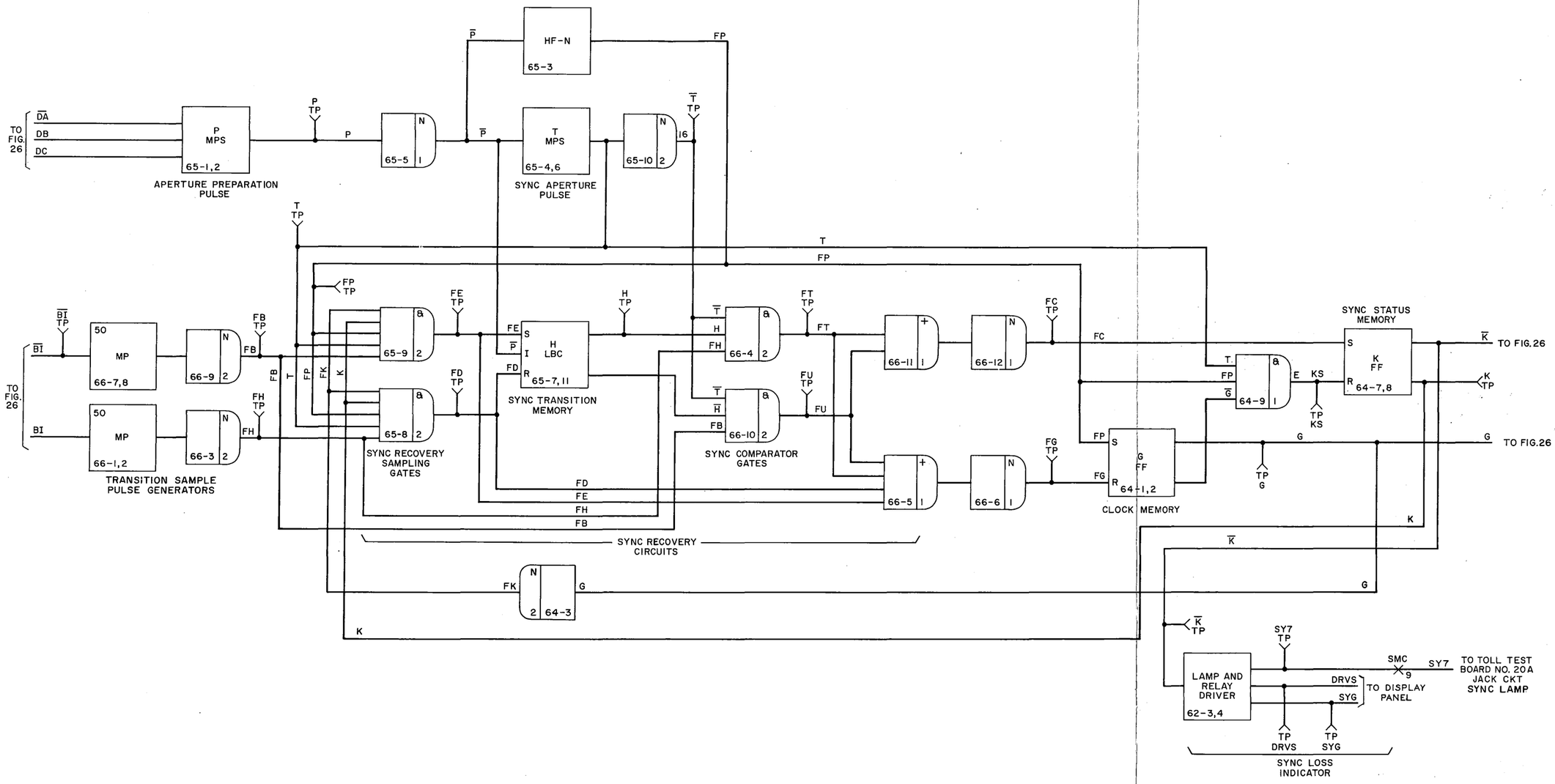


Fig. 27 — Supervisory Demodulator-Demultiplexer — Functional Schematic (Part 2)

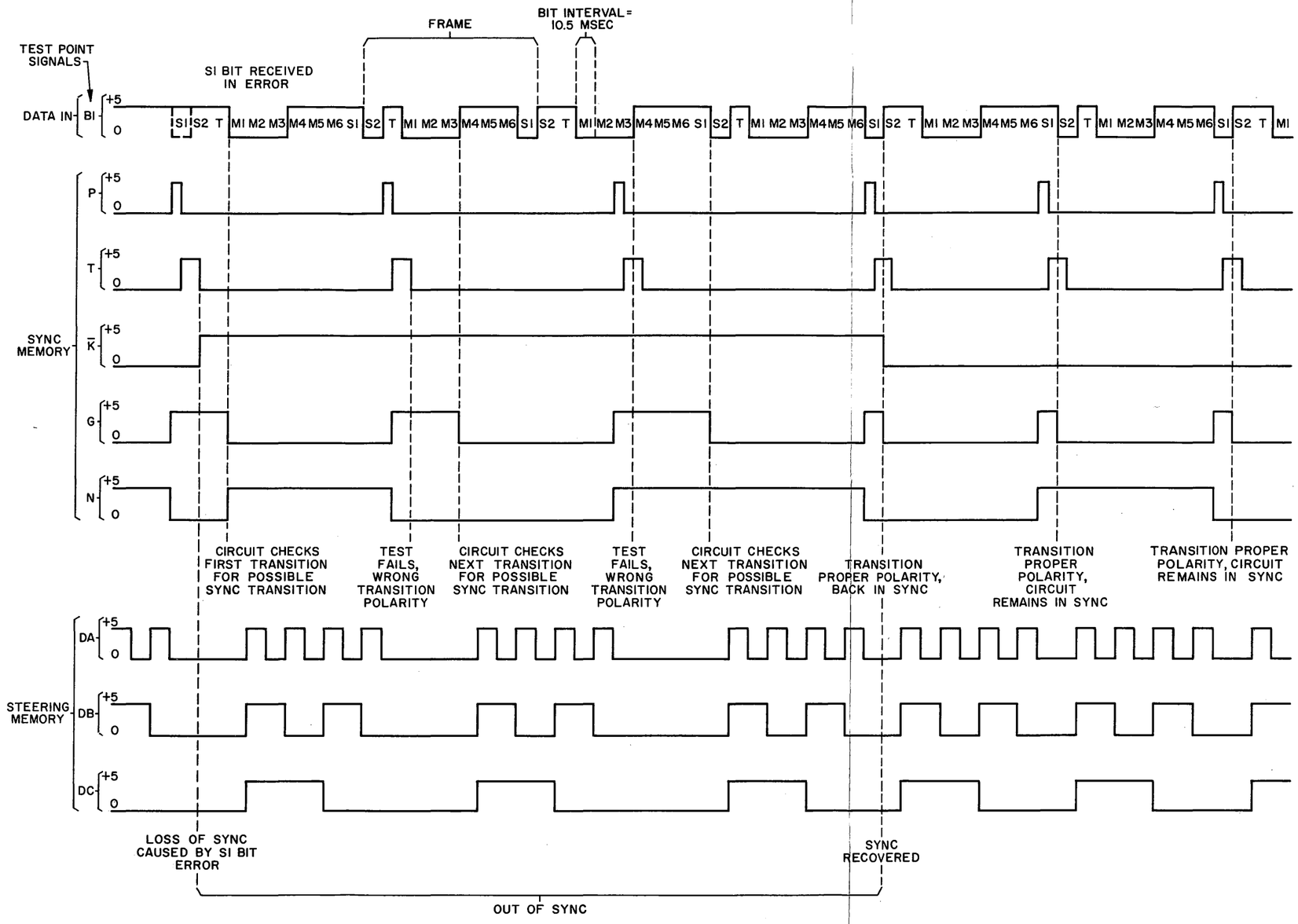


Fig. 28 — Supervisory Demultiplexer Sequence Diagram

inverter 8-13 which, in turn, turns on the variable width monopulser (MPF) which takes over the function of clamping the DM lead to ground. Delay through monopulser 8-9, 10 resets the flip-flop, but this action is sufficiently delayed so that OR gate 8-5 remains turned on because of the overlap of the monopulser output and the output of the zero side of the flip-flop. When the MPF monopulser resets, the ground on DM is removed and because the character following the coincidence of the pulses on EIN and STRT has a one in the first bit position, a delayed positive transition occurs causing a hit of distortion on the DM lead.

8.04 *Burst of Five Hits Every 693 Bits (Fig. 30b):* With the CONT-INT key in the INT position and the MULT-SGL-BIAS key in the MULT position, a positive pulse on EIN and STP acts in the way described above to set the flip-flop and clamp SS and STRT to ground, both these leads being at ground at this time. When the STP goes to ground, MPF fires and unclamping action on DM and SS takes place late, as described above. At this time STRT wants to go positive, and, therefore, a delayed start transition is produced. The amount of delay is variable since the length of the pulse from MPF may be controlled. Five transitions occur in the following character before the next start pulse and these are indicated as five hits of distortion, as distortion is measured from the start pulse of each character.

8.05 *Continuous Hits:* If the CONT-INT key is returned to CONT, the action described above takes place on every start pulse causing every transition to be distorted.

8.06 *Bias:* With the MULT-SGL-BIAS key in the BIAS position and the GEN MODE switch on the 20A toll testboard set to DOT, a square wave is produced by the signal generator on the SQ lead and positive transition causes the flip-flop on CP8 to set, causing clamp action on the DM lead (already at ground). The negative transition on SQ unclamps DM late, as described above, causing a variable amount of bias distortion to be introduced into the dotting signal.

8.07 *Procedure for Measuring Narrow Pulses in Conjunction with the 908A Logic Circuit Test Set:* In maintaining the 906A, there are times when it is necessary to detect pulses of shorter duration than is normally possible with the 908A logic circuit test set. In these cases, the MPF monopulser can be used to stretch the pulses so they are long enough to be detected by the 908A. This is done as follows:

(a) *Positive Pulses*

(1) Ground TP 5 in N CP8.

(2) Ground TP 4 FF CP8.

(3) Operate key FREQ-OFF-TST on calibrator panel to FREQ.

(4) Connect signal to be measured on TP 6 MP+ CP8.

(5) Connect input of 908A test circuit to D1 TP 5 on calibrator panel.

(b) *Negative Pulses*

(1) Ground TP 2 G2 CP8.

(2) Ground TP 4 FF CP8.

(3) Operate key FREQ-OFF-TST on calibrator panel to FREQ.

(4) Connect signals to be measured on TP 7 MP— CP8.

(5) Connect input of 908A test circuit to D1 TP 5 on calibrator panel.

9. POWER SUPPLY

9.01 The 12-volt dc power supply required for the electronic circuits is furnished by a dc converter J87294A, List 2. The description of this circuit is covered in CD-81608-01.

10. RELATED BPS, SDs, CDs

20A TOLL TESTBOARD

- General Description and Operating Principles—314-016-160.
- Directions on How to Use the 20A Testboard—314-016-560.
- Data Test Cord Circuit—CD- and SD-56528-01.
- Jack Circuit—CD- and SD-56526-01.

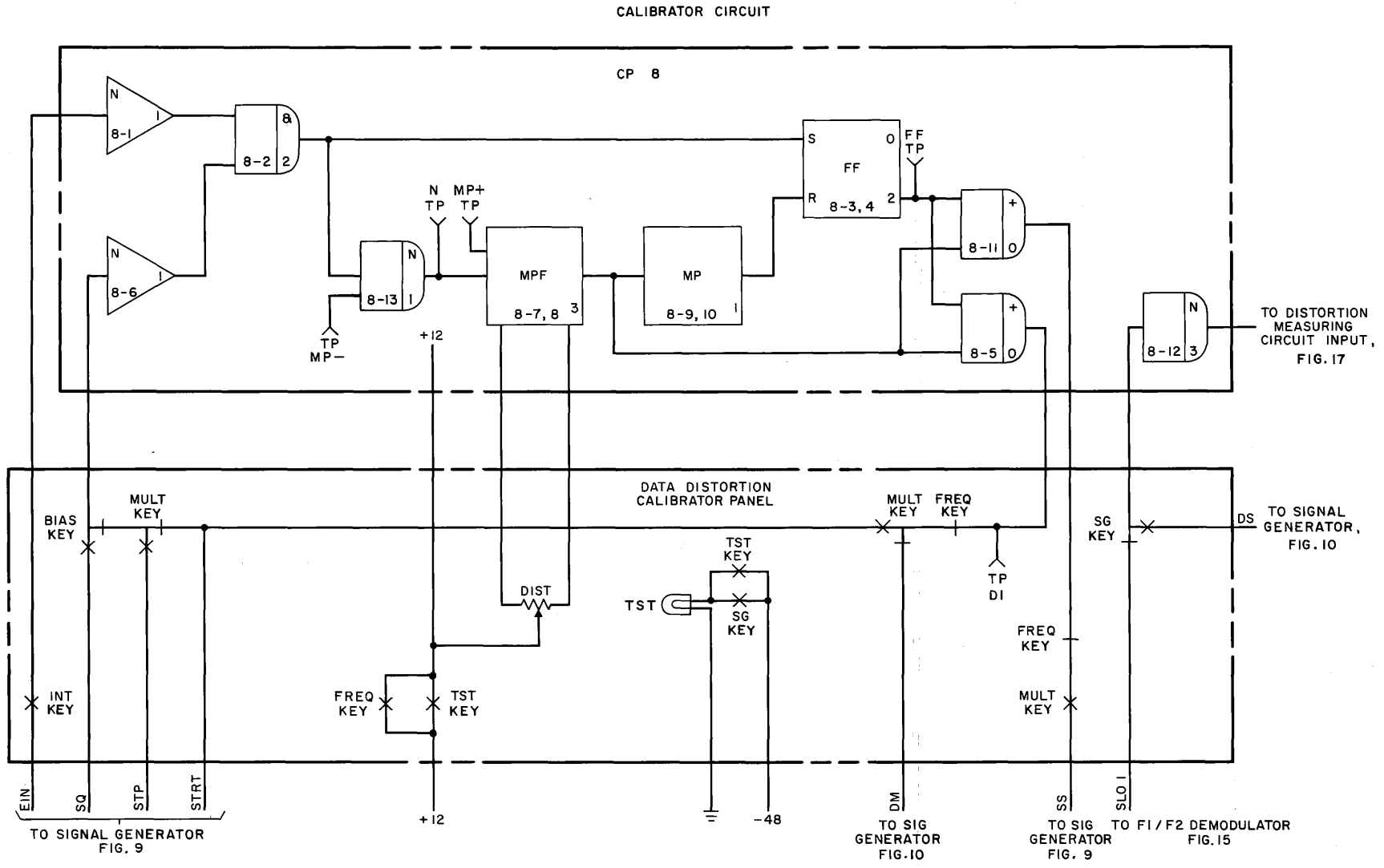


Fig. 29 — Calibrator — Simplified Functional Schematic

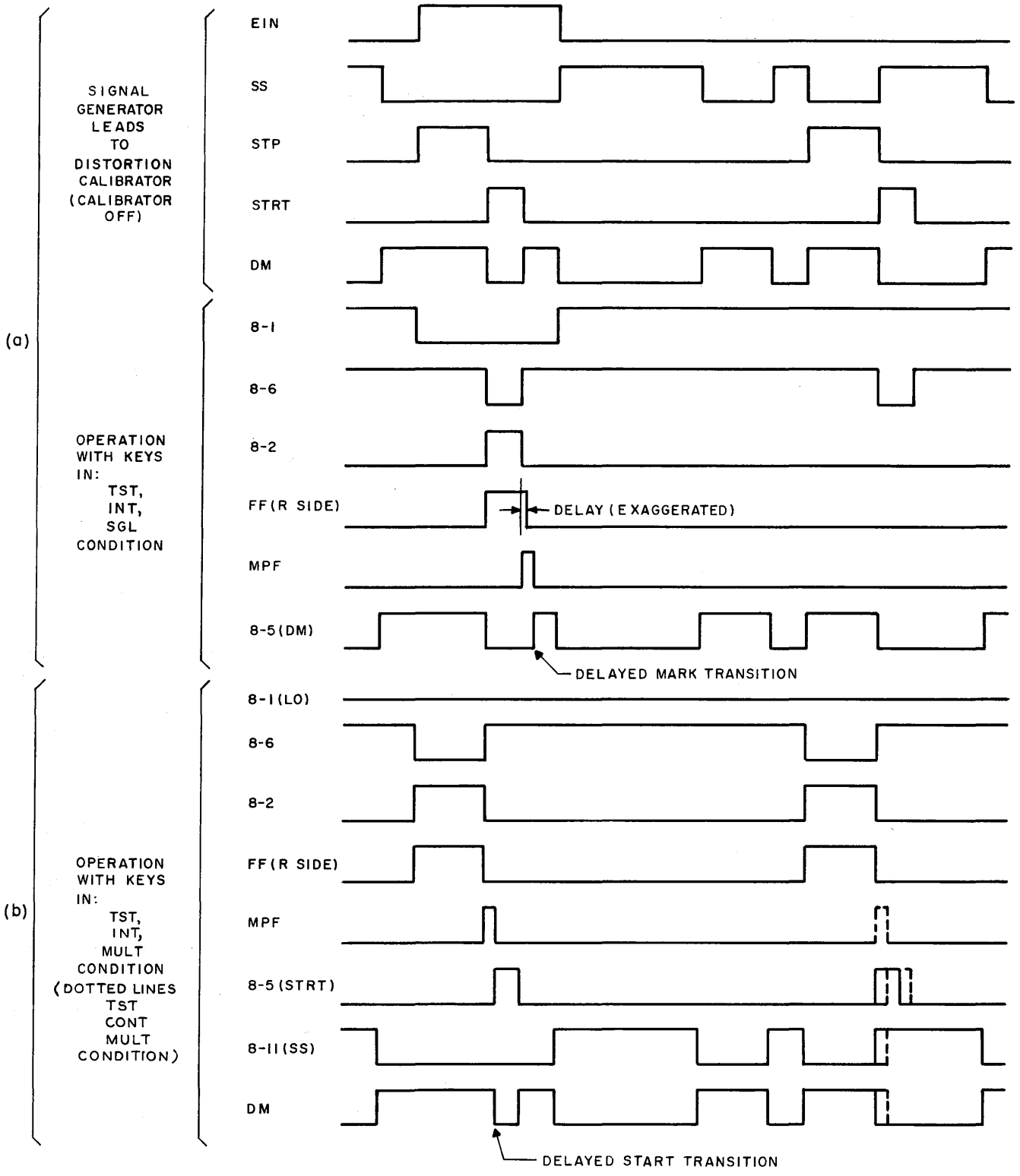


Fig. 30 — Calibrator Sequence Diagram

B1 DATA CARRIER TERMINAL

- General Description and Operating Principles—314-016-150.
- Application Schematic—CD- and SD-73020-01.

906A DATA DISTORTION TEST CIRCUIT, CD- and SD-73022-01

- Performance Requirements—AA638.222.
- Tests, Inspection, Alignment—107-302-500.
- Equipment Design Requirements—AA282.823.