

## 912A WIDEBAND DATA TEST SET

### DESCRIPTION AND OPERATION

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#### 1. GENERAL

**1.01** This section provides a description of the 912A wideband data test set (WDTS). Typical operation and test arrangements are illustrated. However, for detailed instructions on testing a particular type of wideband data set or station, refer to the test section covering the data set or data station. This section also contains instructions for testing and maintaining the 912A WDTS.

**1.02** This section is reissued to add information concerning compatibility between the J79912AC interface unit and the 500A-L1/5 data service unit. Due to extensive changes, arrows ordinarily used to indicate changes have been omitted.

**1.03** The 912A WDTS is designed to test wideband data stations or sets which operate in the range of 9 to 2000 kbps. A maximum of ten self-contained speeds may be installed in the test set, but only five are initially provided. These give bit rates of 19.2, 40.8, 50.0, 230.4, and 250.0 kbps. The five remaining speeds will be made available on an optional basis as future wideband data set developments require.

**1.04** The 912A WDTS determines error rates, tests various interface functions of a wideband data set or station, makes margin tests of received nonsynchronous data, and tests low-speed data sets 404B which may be associated with a wideband data station.

**1.05** At present, three plug-in interface units are available for use with the 912A WDTS. These are described below:

- (a) The J79912AA interface unit provides access to the unbalanced type interface clock, data and control signals of data sets 301- and 303-type. In addition, access to Electronic Industries Association (EIA) data signals associated with the low-speed data set interface (when provided) and balanced data signals of certain codes of

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data sets 303-type provided with the balanced customer interface is available.

(b) The J79912AB interface unit provides cable connections for five types of data sets 301 and 303. This unit is normally used in rack-mounted 912A WDTSs.

(c) The J79912AC interface unit provides access to the high-speed balanced clock and data signals and to the unbalanced EIA control signals associated with data set 306 and the 500A-L1/5 data service unit. This interface unit is used only with a portable 912A WDTS.

**Note:** J79912AC interface units manufactured before 1973 were not compatible with the 500A-L1/5 (56 kbps) data service units. Compatibility was provided by a class A wiring change (see SD-73047-01, Note 307).

**1.06** The 912A WDTS requires approximately 60 watts of 117-volt, 60-Hz ac power. It will operate in a temperature range of 40 to 120°F in a relative humidity of 20 to 95 percent.

### 2. PHYSICAL DESCRIPTION

**2.01** The 912A WDTS is composed of three major units: the transmitter, the receiver, and a plug-in interface unit. Interface cables are supplied with each interface unit.

**2.02** The 912A WDTS is designed to be either portable or rack-mounted. It is a light gray unit with dark decaled markings and is enclosed in a light gray luggage-type case sized as shown in Fig. 1. The test set weighs approximately 45 pounds and is provided with handles for portability. Brackets are available to permit mounting of the test set in a 23-inch bay.

**2.03** The front cover may be removed by depressing the two latches and lifting the cover forward. When the 912A WDTS is rack-mounted, the front cover is removed.

**2.04** Components making up the 912A WDTS are shown in Fig. 2 and the front panel in Fig. 3.

**2.05** The front panel (Fig. 2) is hinged at the top to permit access to circuit fuses and spare fuses during maintenance.

**2.06** The cable storage panel (Fig. 2) contains the POWER switch, POWER lamp, storage space for the two cables, and the power cord and power jack.

**2.07** The printed circuit board locations are shown in Fig. 4. Printed boards CP 18, 19, and 20 as shown are part of the J79912AA interface unit.

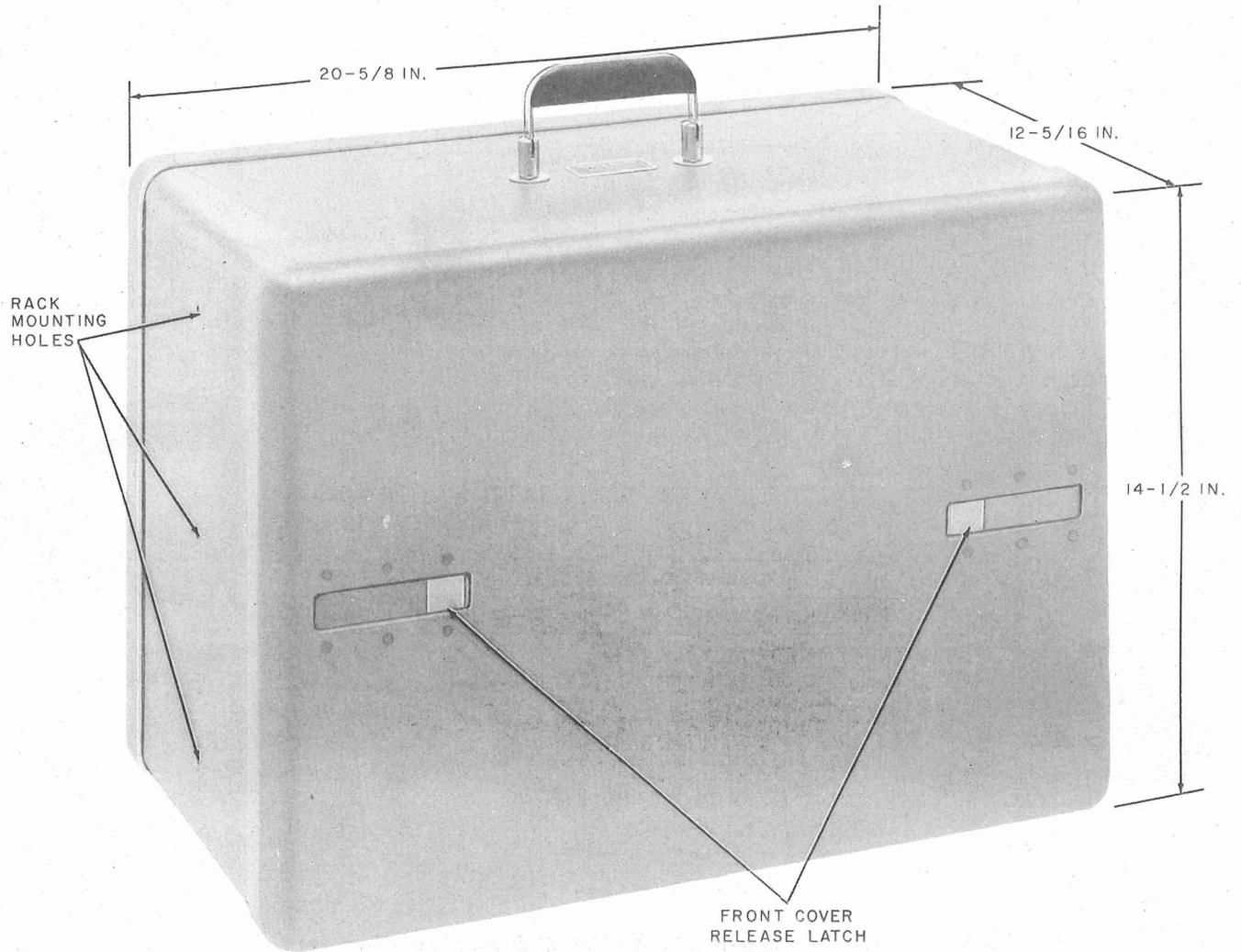


Fig. 1—912A Wideband Data Test Set, Front View

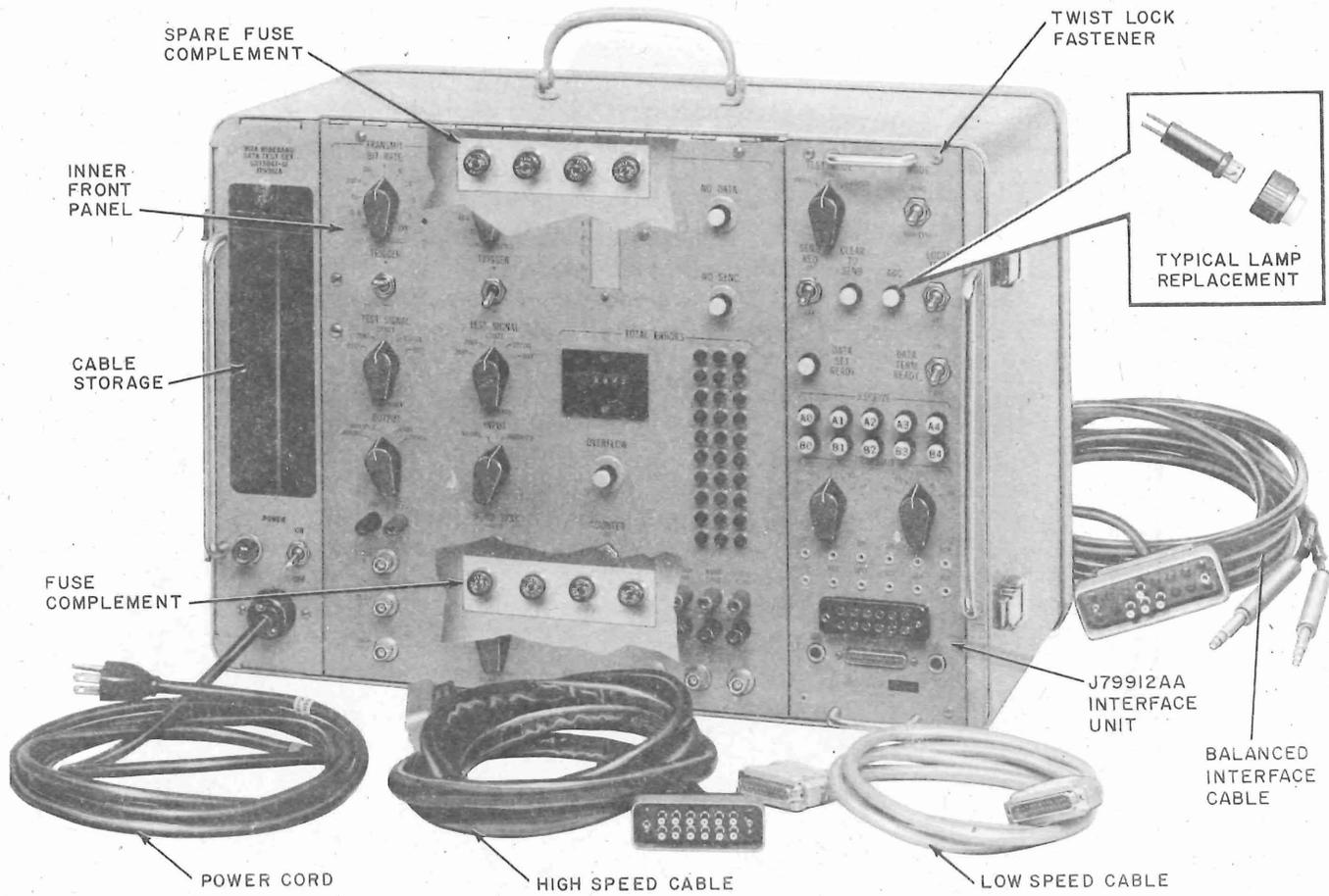


Fig. 2—Components of 912A Wideband Data Test Set

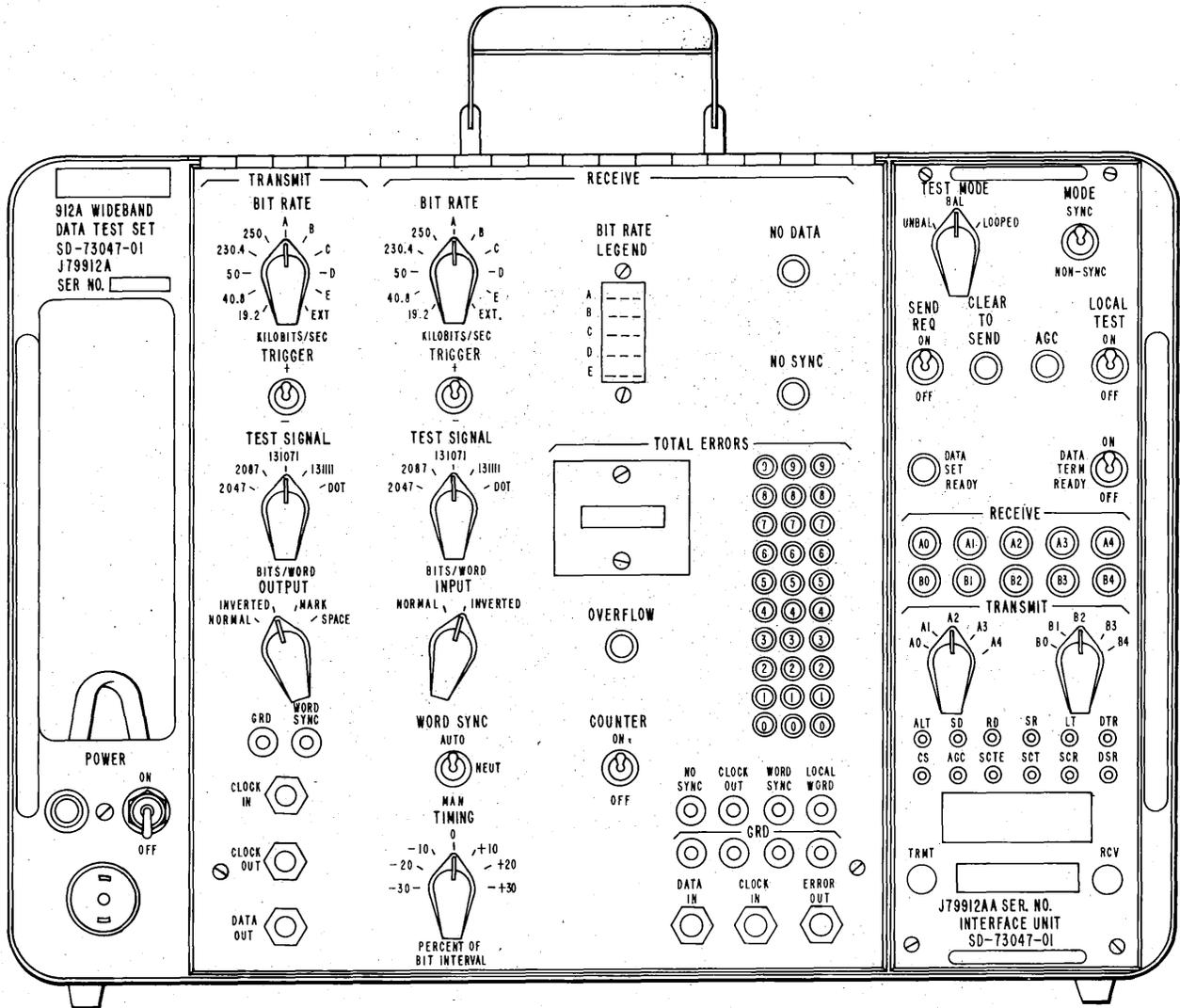
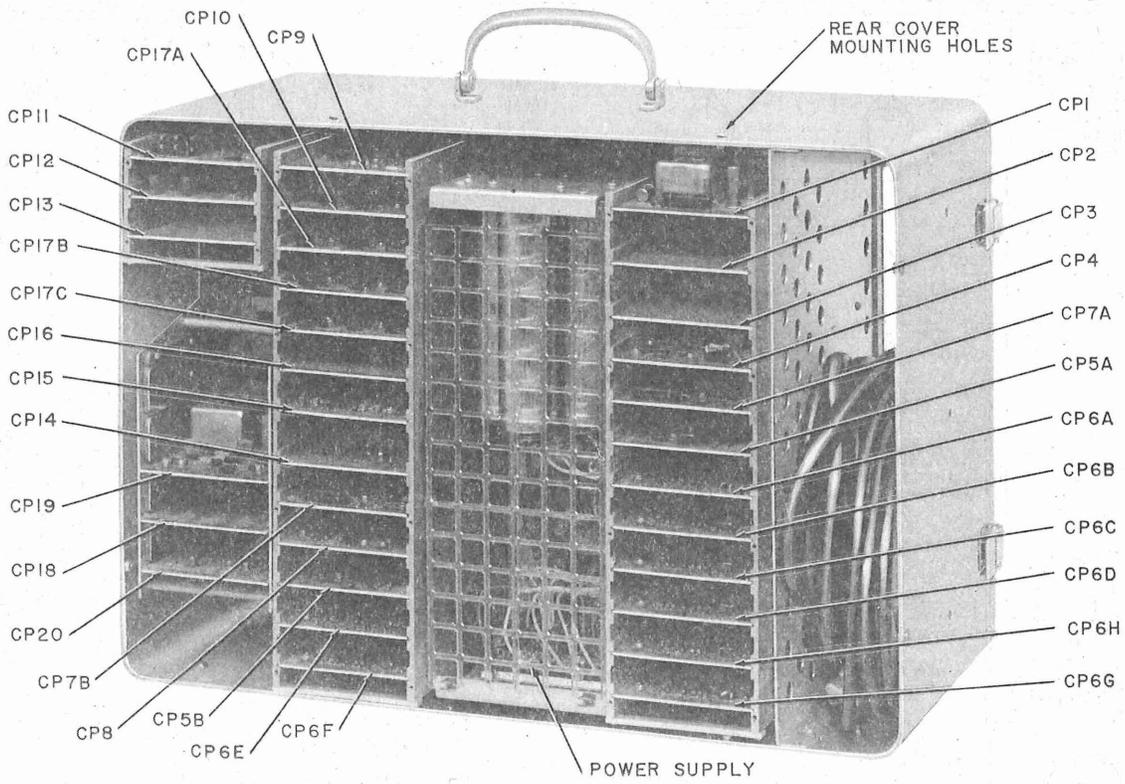


Fig. 3—912A Wideband Data Test Set With J79912AA Interface Unit, Front Cover Removed



**Fig. 4—912A Wideband Data Test Set, Printed Circuit Board Complement**

### 3. FUNCTIONAL DESCRIPTION

#### General

**3.01** A station may be tested using the 912A WDTS on a local basis (looped), or a system may be tested on an end-to-end basis. In either case, the 912A WDTS simulates a business machine by generating test signals and sending them through the circuits of a wideband data set or station. Fig. 5 is a basic block diagram of the 912A WDTS operating in the looped state. The output signals from the data set under test are then compared with an internally generated test signal. A comparator circuit within the 912A WDTS detects differences (errors) between the received and test signal, and the number of errors are displayed on a 7-decade error counter. The 912A WDTS is also capable of signal margin evaluation.

#### Transmitter

**3.02** The basic test signal (data out) generated by the transmitter test signal generator (Fig. 6) is a periodic pseudo-random pulse sequence of 2047 or 131071 bits. These two test signals may be altered by adding 40 bits (all "ones") into the data stream to provide sequences of 2087 and 131111 bits. There is also a dotting signal generated by the transmitter which gives a total of five available pulsed test signals. The test signal generator may be timed by a self-contained crystal oscillator (transmit clock circuit), or externally timed by a clock signal from the data set under test. The 912A WDTS accepts a total of ten crystals with associated networks, but only five crystals are initially supplied. The bit rates for the supplied crystals are 19.2, 40.8, 50.0, 230.4, and 250.0 kbps. The five remaining bit rates allow for future development. The OUTPUT switch allows selection of a NORMAL or INVERTED test signal. There is also a steady MARK or a steady SPACE test signal available.

**3.03** The controls and indicators of the 912A WDTS transmitter are identified in Fig. 7 and described in Table A.

#### Receiver

**3.04** The receiver contains a bit sync recovery circuit, a test signal generator, a comparator (error detector), an error-counting circuit, a word sync circuit, a test signal sync detector, and a data detector. The test signal generator circuit generates a periodic pseudo-random test signal identical to that generated in the transmitter. The comparator circuit detects differences between the test signal received from the data set under test with the receiver test signal. Errors detected by the comparator are recorded by the 7-decade error counter. The first three decades constitute a high-speed electronic counter capable of counting errors at a 2-megabit rate. The last four decades constitute a mechanical counter. Combination of the two counters allows for isolated 1000-bit error bursts. Should errors occur at a rate exceeding the capability of the counter, the OVERFLOW lamp is illuminated. The bit sync recovery circuit and the test signal synchronization circuit provide proper phasing of the test signal with respect to the received test signal. The receiver has means for manual or automatic test signal synchronization. The test signal sync detector circuit illuminates the NO SYNC lamp whenever the two test signals are out of phase. The data detector circuit illuminates the NO DATA lamp whenever there is no data being received from the data set under test.

**3.05** Received data signal margins may be evaluated by displacement of the bit-sampling pulses to time slots either earlier or later than the average center of the bits in the nonsynchronous mode of data set operation. This feature, under control of the TIMING switch, provides an evaluation of the data in displacement increments of 10 percent from -30 to +30 percent of a bit interval.

**3.06** The controls and indicators of the 912A WDTS receiver are identified in Fig. 8 and described in Table B.

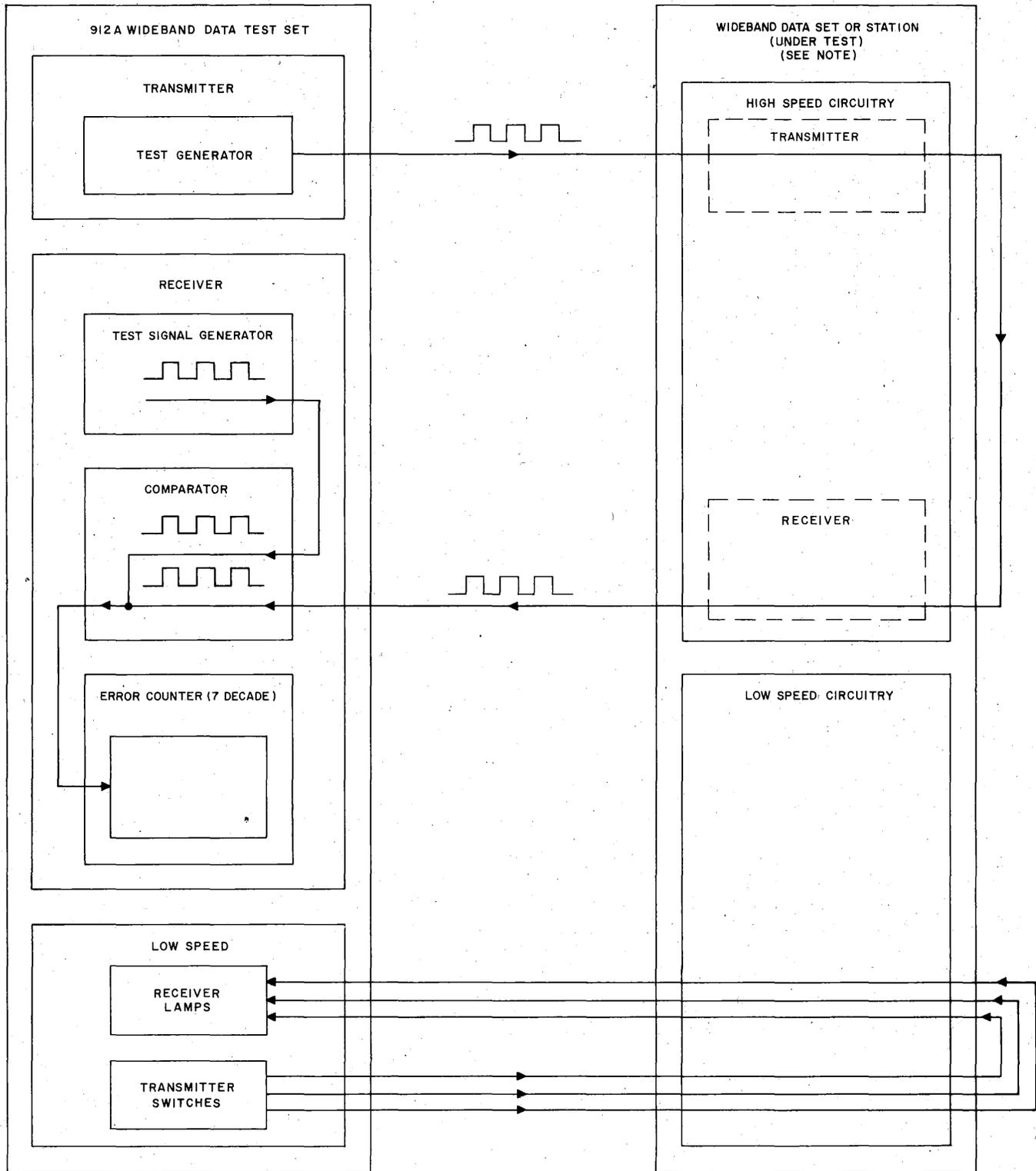


Fig. 5—912A Wideband Data Test Set, Operational Block Diagram

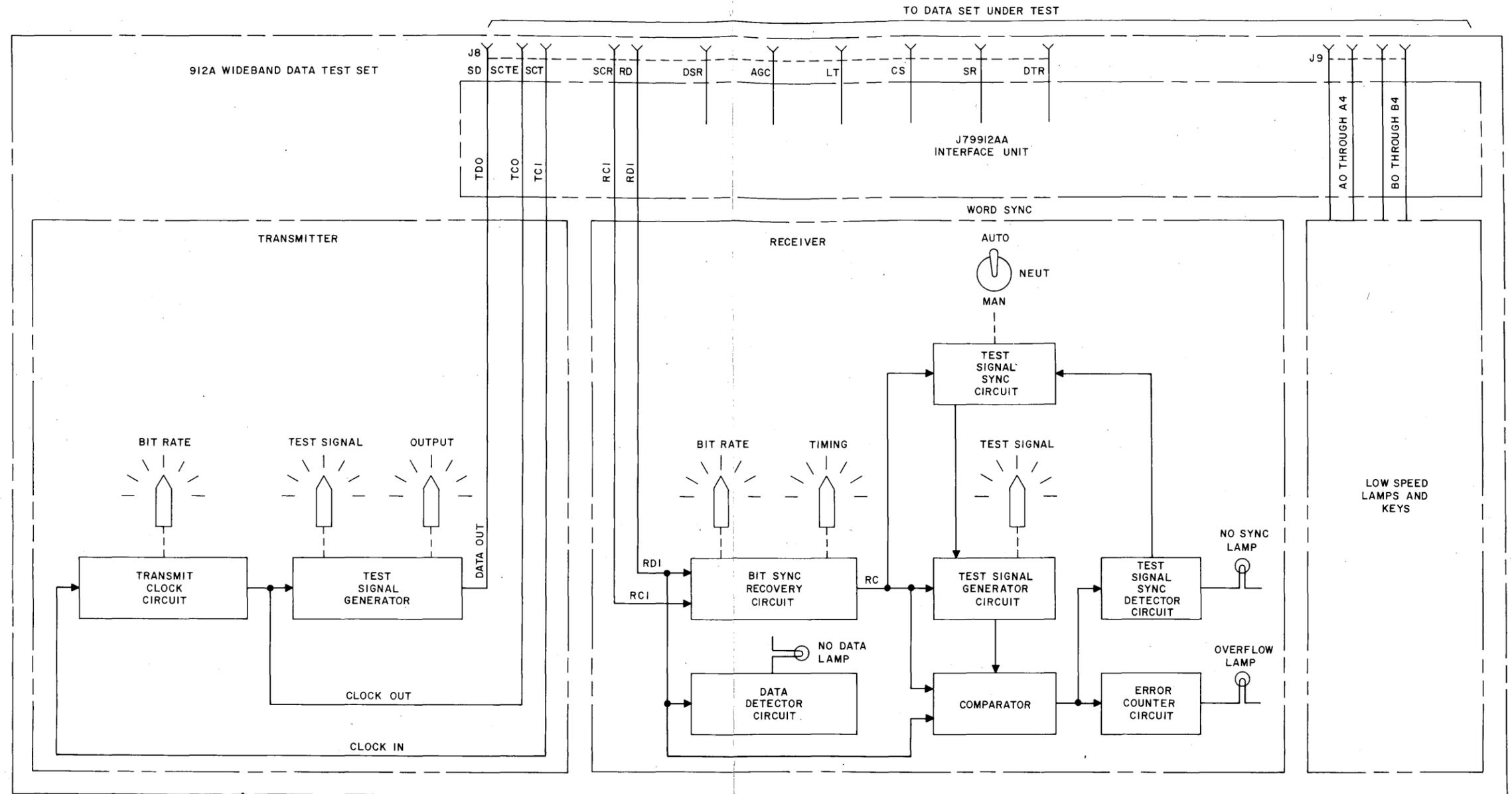


Fig. 6—912A Wideband Data Test Set, Functional Block Diagram

**J79912AA Interface Unit**

**3.07** The J79912AA interface unit is an optional plug-in unit which provides means for connecting the 912A WDTS to a data set and for control of various data set functions.

**3.08** Connections to all the high-speed terminals of the data set under test are made through a multiple-pin coaxial connector which accommodates inputs and outputs for data sets operating in either the synchronous or nonsynchronous mode. The high-speed portion contains cable-terminating and cable-driving circuitry. There are test points in the form of pin jacks for monitoring signals of the high-speed signal leads.

**3.09** Connection to the low-speed circuitry is made through a standard 25-pin connector which conforms to EIA Standard RS-232-A. The low-speed control circuits permit tests of the data set (DS) 404B associated with the 303-type wideband data station. The interface unit drives the low-speed parallel data transmitter of the DS 404B. In response to signals from the transmitter, the data set receiver sends signals to the 912A WDTS. These response signals drive the indicator lamps of the interface unit which display the state of the receiver channels during a test. Jacks which supply line battery current are used when making loop-around tests of the voice coordination channel.

**3.10** Controls and indicators of the J79912AA interface unit are identified in Fig. 9 and described in Table C.

**3.11** A high-speed cable (ED-73242-20, Group 1) and a low-speed cable (ED-73243-20, Group 1) are provided for direct connection to the data set under test. In addition, a balanced interface cable (ED-73248-20, Group 2) is provided for testing the following:

- Wideband regenerative repeater J70174-type when side A and side B are equipped for balanced ac type line signals (test performed from the wideband service bay)
- Data auxiliary set 824A-type
- Data set 303-type equipped for balanced or unbalanced customer line signals (test performed from the wideband test bay).

**J79912AB Interface Unit**

**3.12** The J79912AB interface unit provides many of the functions of the high-speed portion of the J79912AA interface unit and is intended for use in the rack-mounted version of the 912A WDTS. Usually, a rack-mounted 912A WDTS is used in a wideband data test bay where an auxiliary interface unit is used to convert the balanced data set signals to be compatible with the unbalanced signal requirements of the data test set.

**3.13** The J79912AB interface unit may connect to a maximum of five data sets 301- or 303-type. The high-speed operation is permitted through five interface connectors at the rear of the unit. The individual connectors are selected by a switch on the front panel of the interface unit. For synchronous operation, straps on TS101 must be removed.

**3.14** Controls and indicators of the J79912AB interface unit are identified in Fig. 10 and described in Table D.

**J79912AC Interface Unit**

**3.15** The J79912AC interface unit is used only with the portable data test set when testing synchronous data set 306A-type and the 500A-L1/5 data service unit.



*Option W must be installed in the data test set for the test set to perform satisfactorily because of the high bit rate (1.344 mbps) associated with the 306A. Option W may be ordered as field modification kit J79912 List 46 for those WDTSs not originally equipped.*

**3.16** All connections between the data set and the interface unit are made with a balanced double-ended cable, CA201. This cable connects to the 34-pin connector, J201, on the front of the interface.

**3.17** All wideband interface signals are balanced dc signals, and the unbalanced control signals meet EIA Standard RS-232-C format. The unit provides pin jacks for monitoring these signals.

**3.18** Controls and indicators of the J79912AC are identified in Fig. 11 and described in Table E.

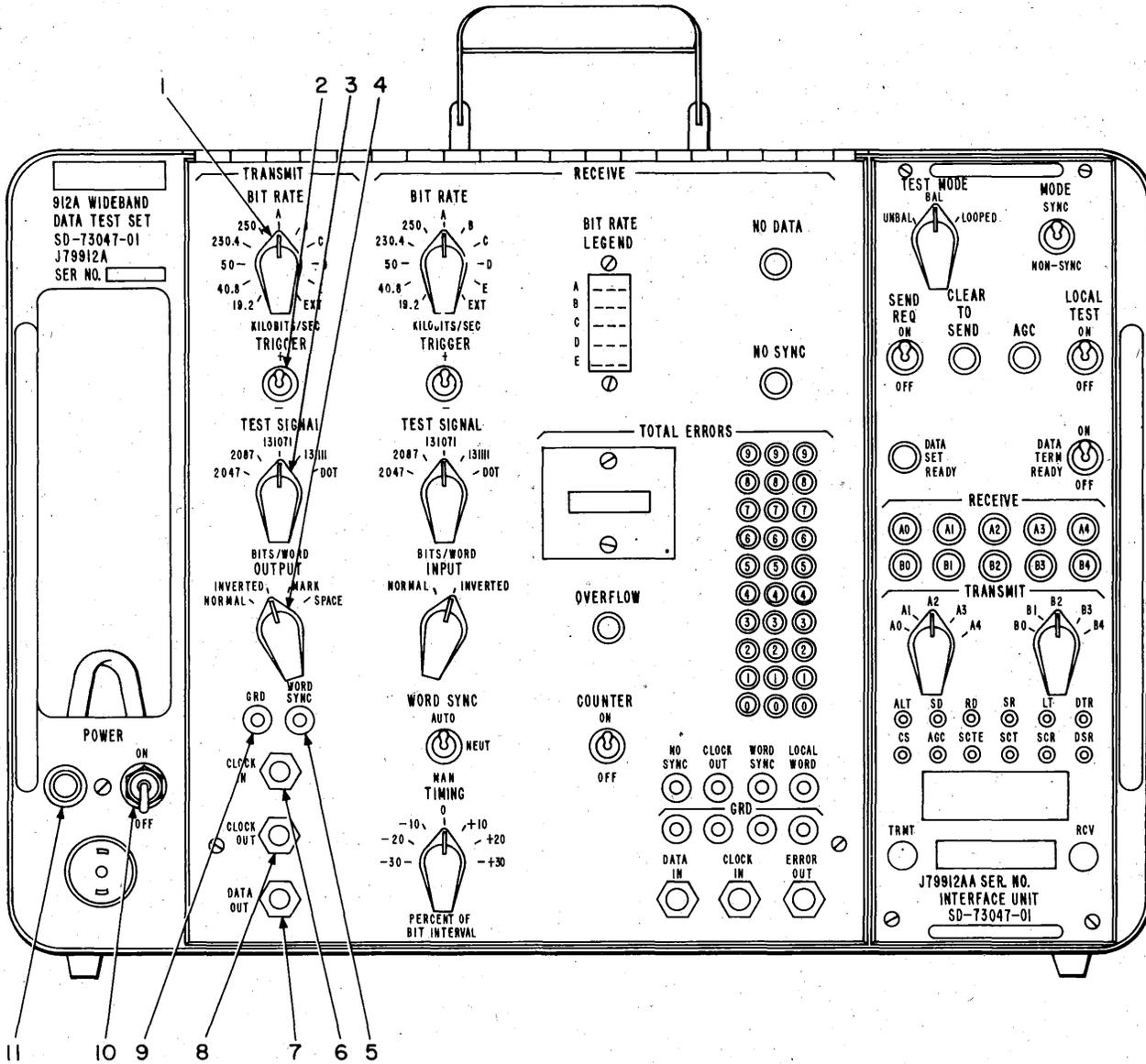


Fig. 7—Controls and Indicators Related to Transmit Portion of the 912A Wideband Data Test Set

TABLE A  
 CONTROLS AND INDICATORS RELATED TO TRANSMIT PORTION OF 912A  
 WIDEBAND DATA TEST SET

KEY TO FIGURE 7	CONTROL OR INDICATOR	TYPE	FUNCTION
1	BIT RATE	Switch, Rotary	Selects one of the five internally controlled clock rates or the external clock signal from the data set. The A through E positions are for future use.
2	TRIGGER	Switch, Toggle	Determines the polarity of the clock pulse transitions which will trigger the word generator.
3	TEST SIGNAL	Switch, Rotary	Selects the length of the transmit test signal generated by the 912A WDTS.
4	OUTPUT	Switch, Rotary	Selects the polarity of the output test signal from the 912A WDTS, or selects a steady mark or a steady space output. The test signal is applied to the DATA OUT connector (7) and the SD lead of the high-speed connector.
5	WORD SYNC	Test Point	A triggering pulse is present at this test point for synchronizing an oscilloscope for viewing a test signal.
6	CLOCK IN	Coaxial Connector	This connector provides a means for applying an external clock input.
7	DATA OUT	Coaxial Connector	This connector provides a means whereby the output data of the 912A WDTS can drive external equipment.
8	CLOCK OUT	Coaxial Connector	This connector provides a clock output for driving external equipment.
9	GRD	Test Point	This terminal provides a means for applying transmitter ground to external equipment.
10	POWER	Switch, Toggle	When operated to ON, applies power to the 912A WDTS.
11	POWER	Lamp	When lighted, indicates that power is applied to the 912A WDTS.

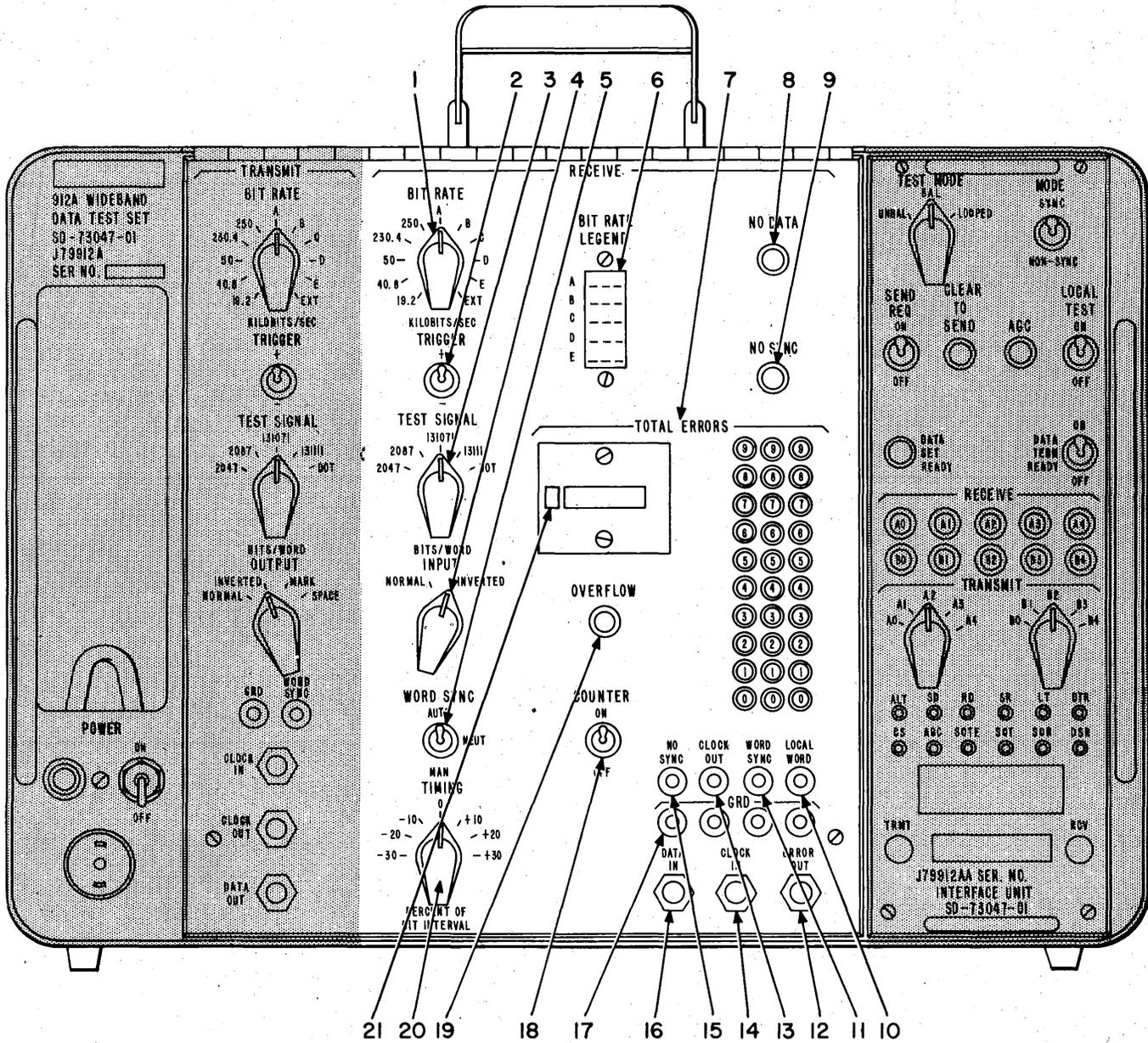


Fig. 8—Controls and Indicators Related to Receive Portion of the 912A Wideband Data Test Set

TABLE B

CONTROLS AND INDICATORS RELATED TO RECEIVE PORTION OF 912A  
WIDEBAND DATA TEST SET

KEY TO FIGURE 8	CONTROL OR INDICATOR	TYPE	FUNCTION
1	BIT RATE	Switch, Rotary	Selects one of the five internally controlled clock rates or the external clock signal from the data set. The A through E positions are for future use.
2	TRIGGER	Switch, Toggle	When the BIT RATE switch is set to EXT, the TRIGGER switch provides a means of selecting the polarity of clock trigger.
3	TEST SIGNAL	Switch, Rotary	Selects the length of the receiver test signal that is to be compared with the test signal from the data set.
4	INPUT	Switch, Rotary	This switch conditions the incoming signal to a normal or inverted condition for comparison with the 912A WDTS generated test signal.
5	WORD SYNC	Switch, Toggle (3-Position Spring-Loaded From MAN)	When set to AUTO, automatically synchronizes and maintains synchronization of the 912A WDTS with the received signal. When operated to MAN, synchronizes the 912A WDTS with the received test signal. Must be operated to MAN each time synchronization is lost when not in the AUTO mode. Once synchronization is established, the switch can be set to the NEUT position.
6	BIT RATE LEGEND	Placard	This is a window provided to list the future speeds for the BIT RATE switch.
7	TOTAL ERRORS	Counters	Counters record total errors.
8	NO DATA	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that no data is received.
9	NO SYNC	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that the received test signal and the locally generated test signal are not in synchronization.
10	LOCAL WORD	Test Point	Provides a means of monitoring the test signal generated by the 912A WDTS.
11	WORD SYNC	Test Point	Provides a positive pulse corresponding to the beginning of the test signal generated by the receiver part of the 912A WDTS.
12	ERROR OUT	Coaxial Connector	Provides a connection for an external counter.
13	CLOCK OUT	Test Point	Provides a means of monitoring the 912A WDTS receiver clock output.

TABLE B (Cont)

CONTROLS AND INDICATORS RELATED TO RECEIVE PORTION OF 912A  
WIDEBAND DATA TEST SET

KEY TO FIGURE 8	CONTROL OR INDICATOR	TYPE	FUNCTION
14	CLOCK IN	Coaxial Connector	Provides a means of connecting an external receiver clock input.
15	NO SYNC	Test Point	Provides a positive voltage when the received test signal and the local test signal are out of synchronization.
16	DATA IN	Coaxial Connector	Provides a means of connecting high-speed data from a source other than the data set under test.
17	GRD	Test Point (Four)	Provides a ground return for test points 10, 11, 13, and 15.
18	COUNTER	Toggle Switch	When set to ON, enables the 7-decade counter.
19	OVERFLOW	Screw-On Type Lens and Plug-In Lamp	When lighted, it indicates that the error rate has exceeded the counting rate of the counter.
20	TIMING	Switch, Rotary	The received test signal margins may be evaluated by the setting of this switch which displaces bit-sampling pulses to time slots either earlier or later than the average center of the bits.
21	Reset	Pushbutton on Counter	When depressed, resets the counters.

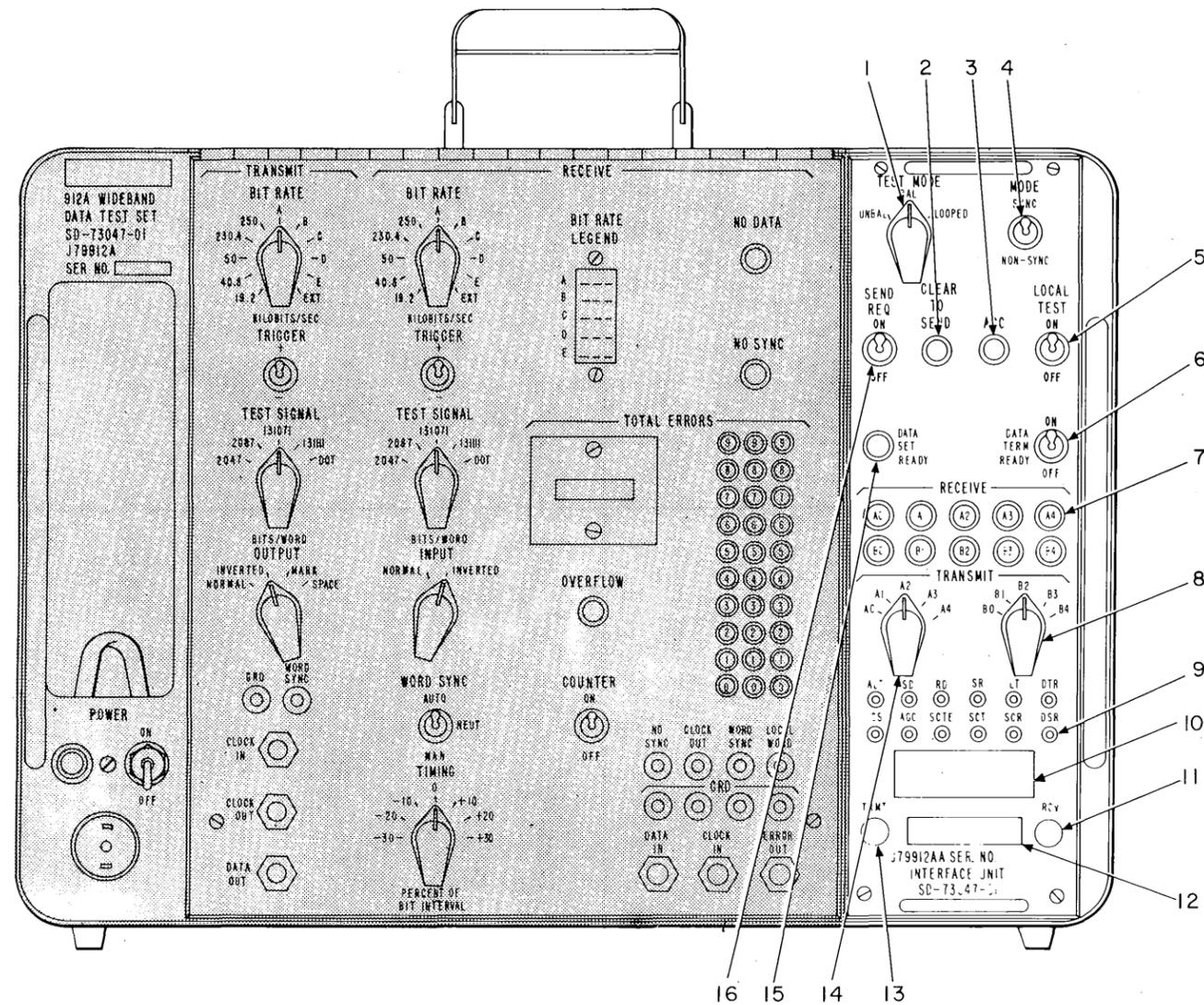


Fig. 9—Controls and Indicators Related to the J79912AA Interface Unit of the 912A Wideband Data Test Set

TABLE C

CONTROLS AND INDICATORS RELATED TO THE J79912AA INTERFACE UNIT OF THE 912A WIDEBAND DATA TEST SET

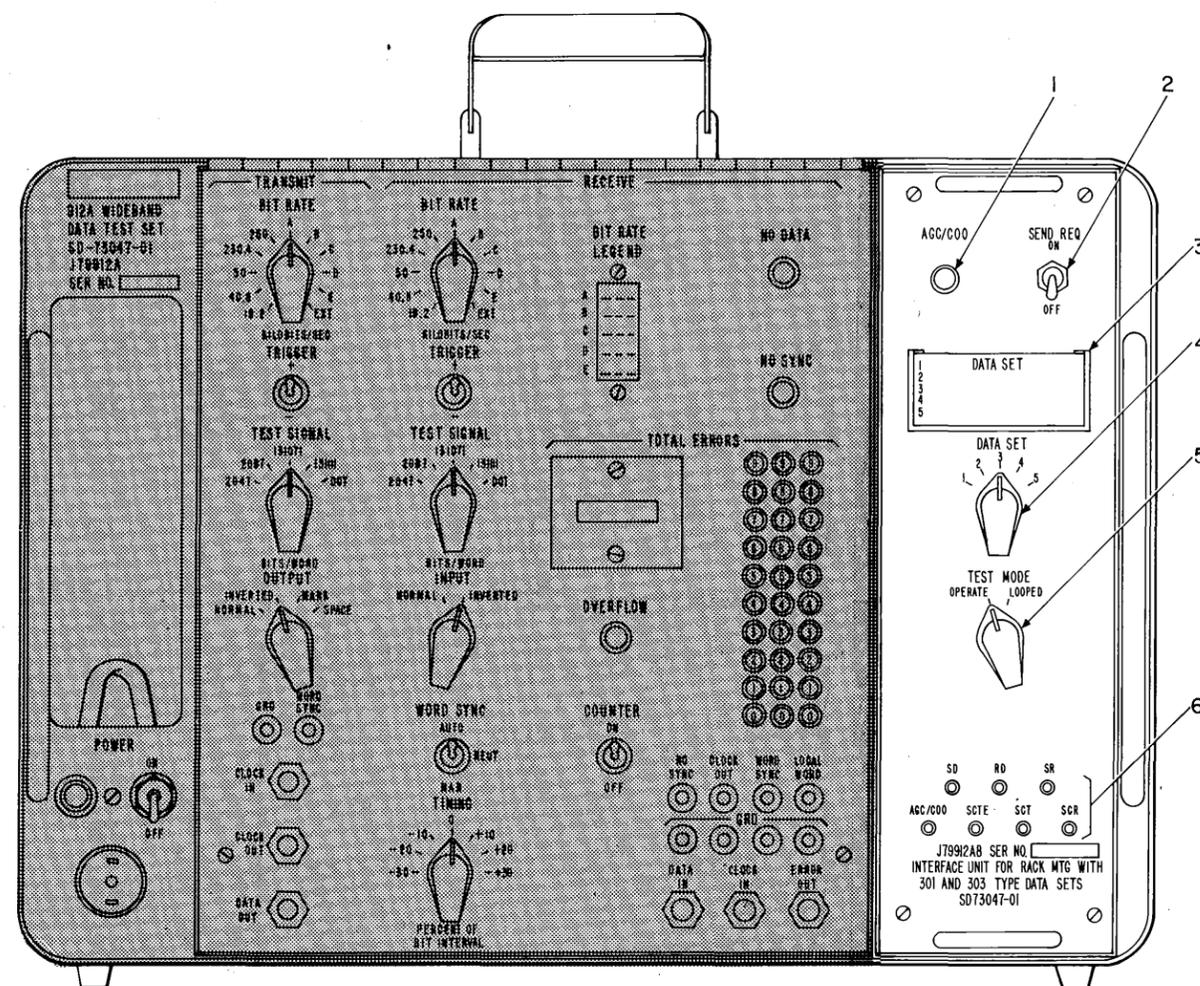
KEY TO FIGURE 9	CONTROL OR INDICATOR	TYPE	FUNCTION
1	TEST MODE	Switch, Rotary	When set to UNBAL, permits testing of data sets with unbalanced interface. When set to BAL, permits testing of data sets with a balanced interface. When set to LOOPED, permits testing of the 912A WDTS.

TABLE C (Cont)  
CONTROLS AND INDICATORS RELATED TO THE J79912AA INTERFACE UNIT OF THE 912A WIDEBAND DATA TEST SET

KEY TO FIGURE 9	CONTROL OR INDICATOR	TYPE	FUNCTION
2	CLEAR TO SEND	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that the Clear-to-Send signal is received from the data set.
3	AGC	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that the data set is detecting received data.
4	MODE	Switch, Toggle	Conditions the data set under test for either synchronous or nonsynchronous operation.
5	LOCAL TEST	Switch, Toggle	When set to ON, causes the data set under test to switch to the local test mode.
6	DATA TERM READY	Switch, Toggle	When set to ON, applies the DTR signal to the wideband data set under test.
7	RECEIVE — Channel Lamps	Screw-On Type Lens and Plug-In Lamps	When lighted, indicate which voice coordination data signals are being received from the data set.
8	TRANSMIT — B Channel Switch	Switch, Rotary	Provides a means of simulating a signal to Data Set 404B on Channel B.
9	Test Points	TP6 — TP15, TP18, TP19	Provide a means for monitoring the wideband interface lead indicated by the name over the test point.
10	High-Speed Connector (J8)	12-Pin	Provides a means of connecting a wideband data set to the 912A WDTS.
11	RCV Jack	Connector	This jack, in conjunction with TRMT jack (13), provides for looping line battery.
12	Low-Speed Connector (J9)	25-Pin	Provides a means of connecting a voiceband data set to the 912A WDTS.
13	TRMT Jack	Connector	This jack, in conjunction with RCV jack (11), provides for looping line battery.
14	TRANSMIT — A Channel Switch	Switch, Rotary	Provides a means of simulating a signal to Data Set 404B on Channel A.
15	DATA SET READY	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that the wideband data set is ready to operate.
16	SEND REQ	Switch, Toggle	Provides a means of simulating the Send Request signal from the business machine.

TABLE D

CONTROLS AND INDICATORS RELATED TO THE J79912AB INTERFACE UNIT OF THE 912A WIDEBAND DATA TEST SET



KEY TO FIGURE 10	CONTROL OR INDICATOR	TYPE	FUNCTION
1	AGC/COO	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that the received test signal magnitude is within acceptable limits.
2	SEND REQ	Switch, Toggle	Provides a means of simulating the Send Request signal from the business machine.
3	DATA SET Designation Card	Placard	Lists and identifies the associated data sets in the 915 Wideband Data Test Bay (WDTB).
4	DATA SET Selector Switch	Rotary, 5-Position	Selects one of the associated data sets in the 915 WDTB.
5	TEST MODE Switch	Rotary, 2-Position	When set to OPERATE, permits testing of data sets. When set to LOOPED, permits self-testing of the 912A WDTS.
6	Test Points	TP101 — TP107	Provide a means for monitoring the wideband interface lead indicated by the name above the test point.

Fig. 10—Controls and Indicators Related to the J79912AB Interface Unit of the 912A Wideband Data Test Set

TABLE E

CONTROLS AND INDICATORS RELATED TO THE J79912AC INTERFACE UNIT OF THE 912A WIDEBAND DATA TEST SET

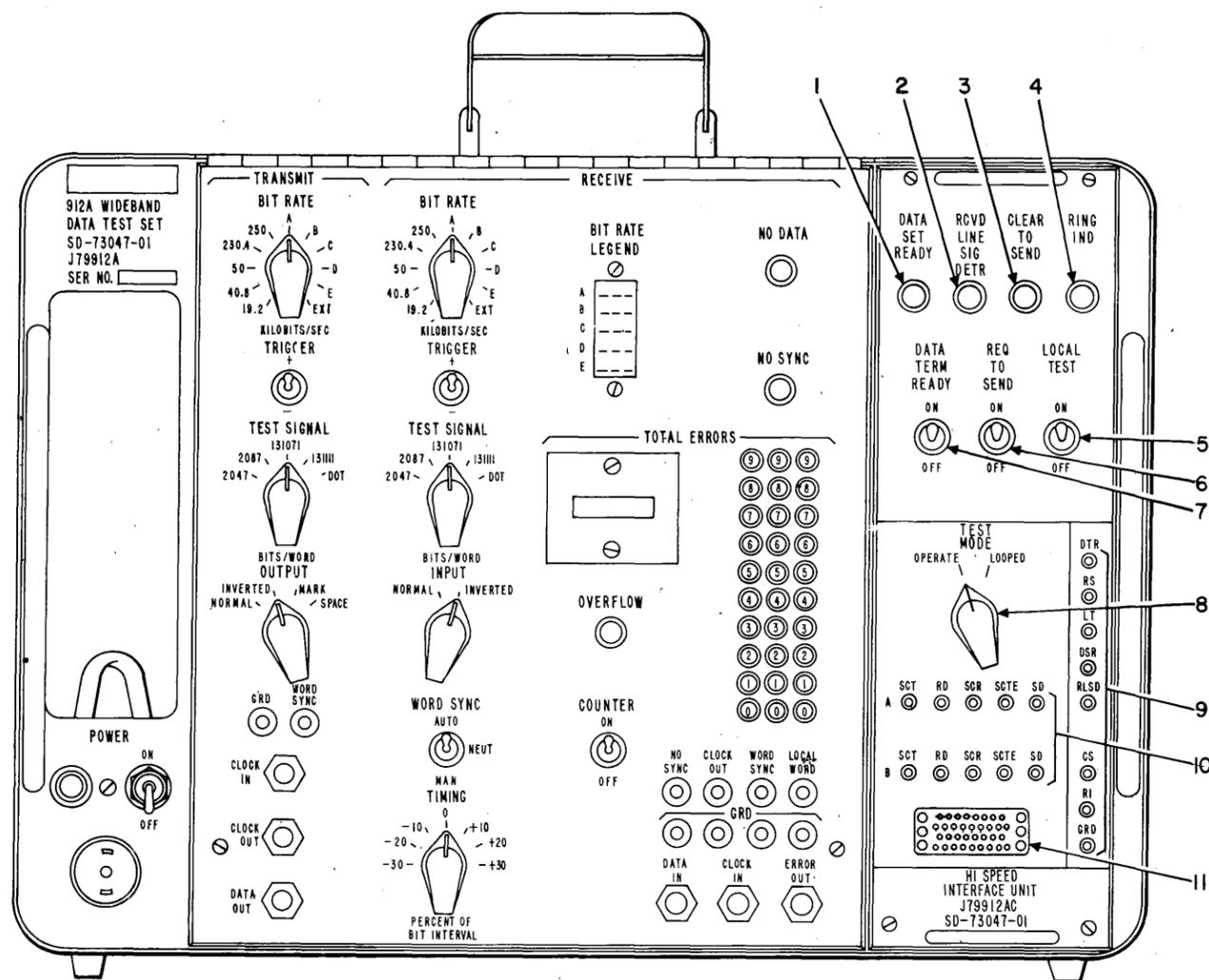


Fig. 11—Controls and Indicators Related to the J79912AC Interface Unit of the 912A Wideband Data Test Set

KEY TO FIGURE 11	CONTROL OR INDICATOR	TYPE	FUNCTION
1	DATA SET READY	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates the data set is capable of operating (not in a test mode) provided other control conditions are met; for example, to transmit data the Clear-to-Send signal must be ON.
2	RCVD LINE SIG DETR	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates the framing or data signals on the Receive Data lead are reliable.
3	CLEAR TO SEND	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates the data set is in a condition to permit the transmission of data or test signals in the local test mode.
4	RING IND	Screw-On Type Lens and Plug-In Lamp	When lighted, indicates that a ringing signal is being received.
5	LOCAL TEST	Switch, Toggle	When operated to ON, causes the data set to switch to the local test mode.
6	REQ TO SEND	Switch, Toggle	When operated to ON, provides a means of simulating the Request-to-Send signal from the business machine.
7	DATA TERM READY	Switch, Toggle	When operated to ON, provides a means of simulating the Data Terminal Ready signal from the business machine.
8	TEST MODE Switch	Rotary, 2-Position	When set to OPERATE, permits testing of data sets. When set to LOOPED, permits self-testing of the 912A WDTS.
9	Test Points	TP201 — TP207 TP218 is GRD	The pin jack test points provide a means of monitoring the EIA unbalanced control signal leads indicated by the name above the test point.
10	Test Points	TP208 — TP217	The pin jack test points provide a means for monitoring the balanced high-speed wideband interface lead indicated by the name above the test point.
11	J201 Connector	34-Pin	Provides a means of connecting a wideband data set or data service unit to the 912A WDTS.

### Power Supply

**3.19** The power supply is fused and converts 117-volt, 60-Hz ac power into three regulated dc outputs (+12V, -12V, and +6V) which are distributed to all parts of the test set.

### 4. OPERATION AND TYPICAL TESTS

**4.01** The 912A WDTS can be used to test a data system on an end-to-end basis as long as there is a compatible test set at the remote station. Figure 12 illustrates the basic connections for this type of test. The test set can also be used to test a wideband system from a single location by looping 4-wire lines. The loop-back connection can be made either at the remote station or local station. The test set can also be arranged for long-period unattended error rate tests. When used in conjunction with a digital counter and a digital recorder, it can check the performance of a data set or station over long periods of time.

**Note:** The 912A WDTS is compatible with another 912A WDTS or with the F56426 test set provided that the 2047- or 2087-bit word is used.

### End-to-End Synchronous Test

**4.02** This test is performed on an end-to-end basis as shown in Fig. 13. While only one direction of testing is shown, the test may be performed on a full-duplex basis.

**4.03** The transmitter test signal generator at station (A) is driven by the serial clock transmit (SCT) signal from the data set transmitter at station (A). In response, the 912A WDTS generates a test signal (data) which is applied to the data set transmitter at station (A). The data set transmits the signal via the telephone line to the data set receiver at station (B). At the receiver

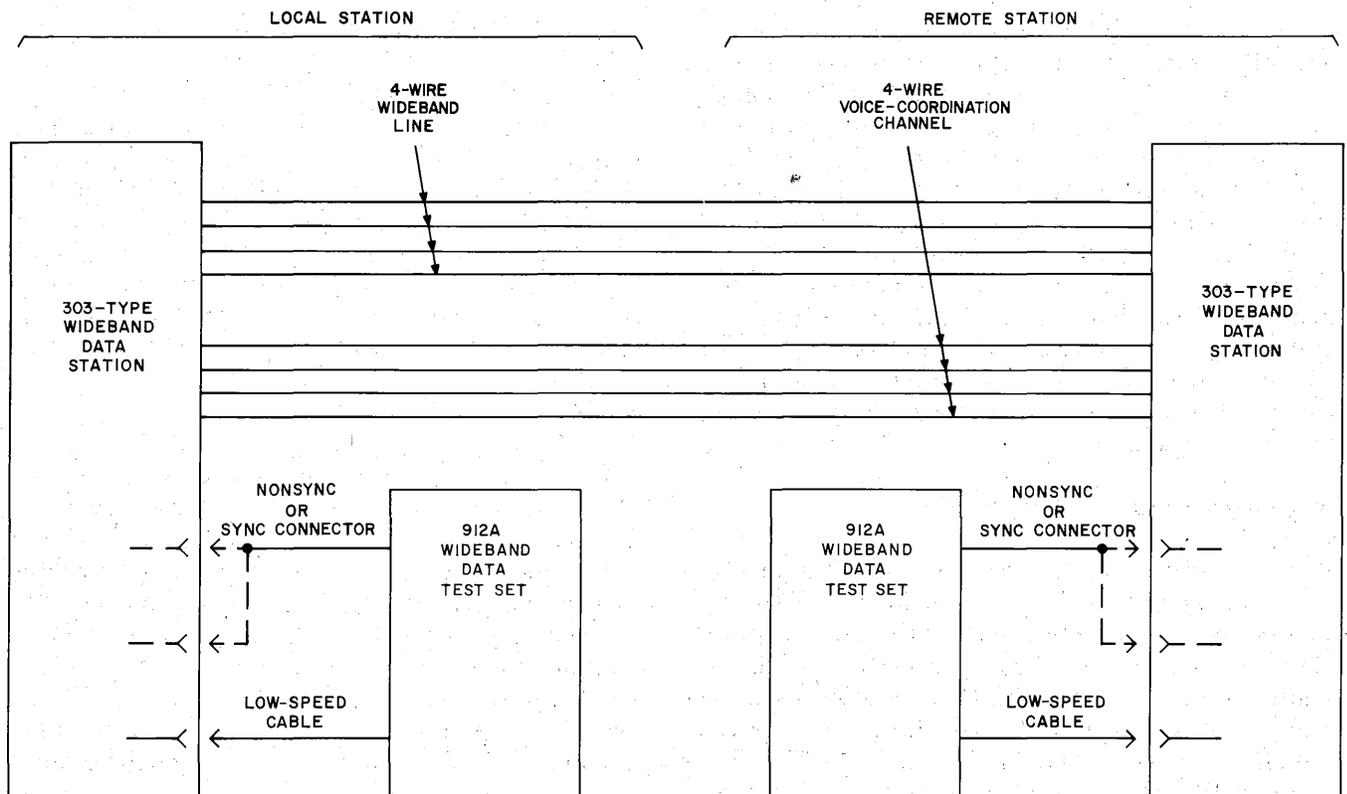


Fig. 12—Typical Connections for End-to-End Test Utilizing the 912A Wideband Data Test Set

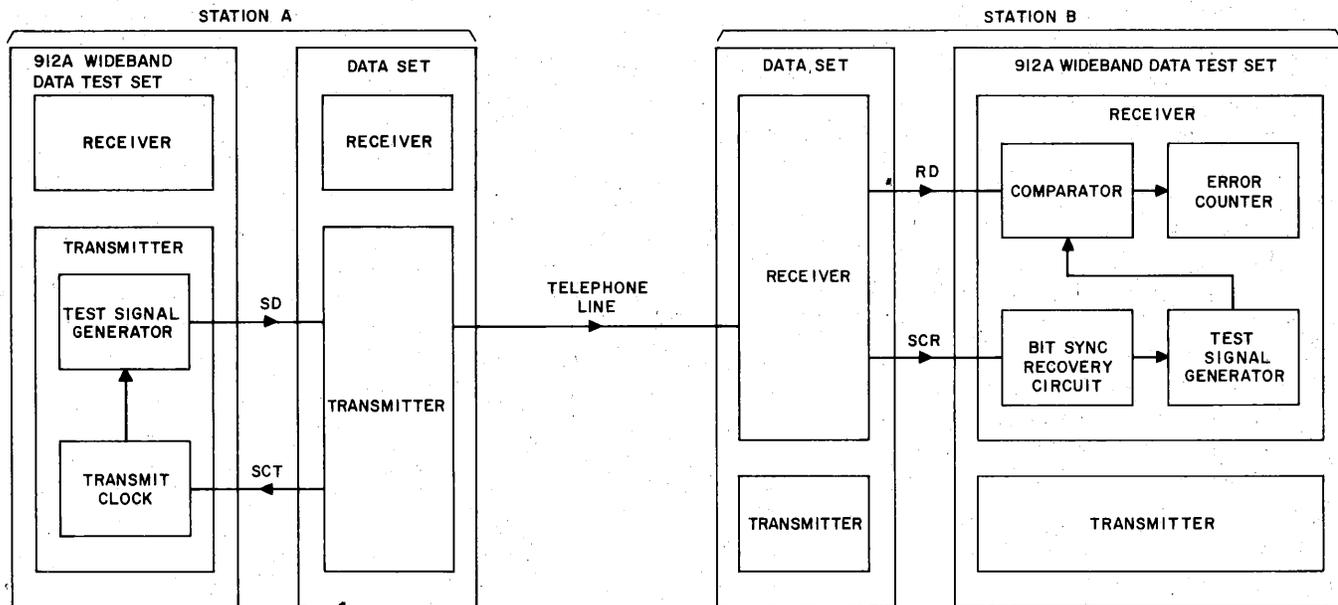


Fig. 13—End-to-End Synchronous Test, Functional Block Diagram

station (B), the data set receiver applies the receive data (RD) signal to the 912A WDTs receiver and also applies the serial clock receive (SCR) signal to the bit sync recovery circuit which drives the test signal generator and the comparator. The receive test signal generator at station (B) produces the test signal which is identical to the signal produced by the test signal generator of the 912A WDTs at station (A). Upon achieving proper phasing of the test signal from station (A) and station (B), the comparator performs a bit-by-bit comparison of the two test signals. Any errors contained in the received test signal are recorded by the error counter.

#### End-to-End Nonsynchronous Test

**4.04** Operation of the transmitting station (A), as shown in Fig. 14, is identical to the end-to-end synchronous test with the exception that the clock is supplied by a crystal oscillator contained in the 912A WDTs at station (A). At the receiver station (B), the data set receiver supplies the RD signal to the 912A WDTs. The 912A WDTs receive bit sync recovery circuit derives the clock signal from the incoming data (RD) and drives the receive test signal generator and comparator in the same manner as described in the end-to-end synchronous test.

#### Local Test of Data Set

**4.05** The 301B-type, 303-type, and 306A-type stations are equipped with a local looping feature which permits local tests of a station. Operation of the LOCAL TEST switch on the J79912AA interface unit causes the line side of the data set to be looped by a relay (Fig. 15). Synchronous and nonsynchronous stations may be tested as described in 4.02 through 4.04 while the stations are in the looped mode.

#### Margin Test

**4.06** When testing synchronous data sets or stations, the comparator samples each test signal bit at bit center. When testing nonsynchronous data sets or stations, in order to determine the margin of performance, the sampling point of the bit may be shifted by operation of the TIMING switch in 10 percent increments away from bit center to the left or right. Errors will result if a transition occurs later than it should and after sampling, or if a transition occurs earlier than it should and before sampling. A transition affected by instantaneous distortion might, therefore, cause the bit to be registered as an error. The error rate will increase for successively larger displacements of the sampling point from the bit center position.

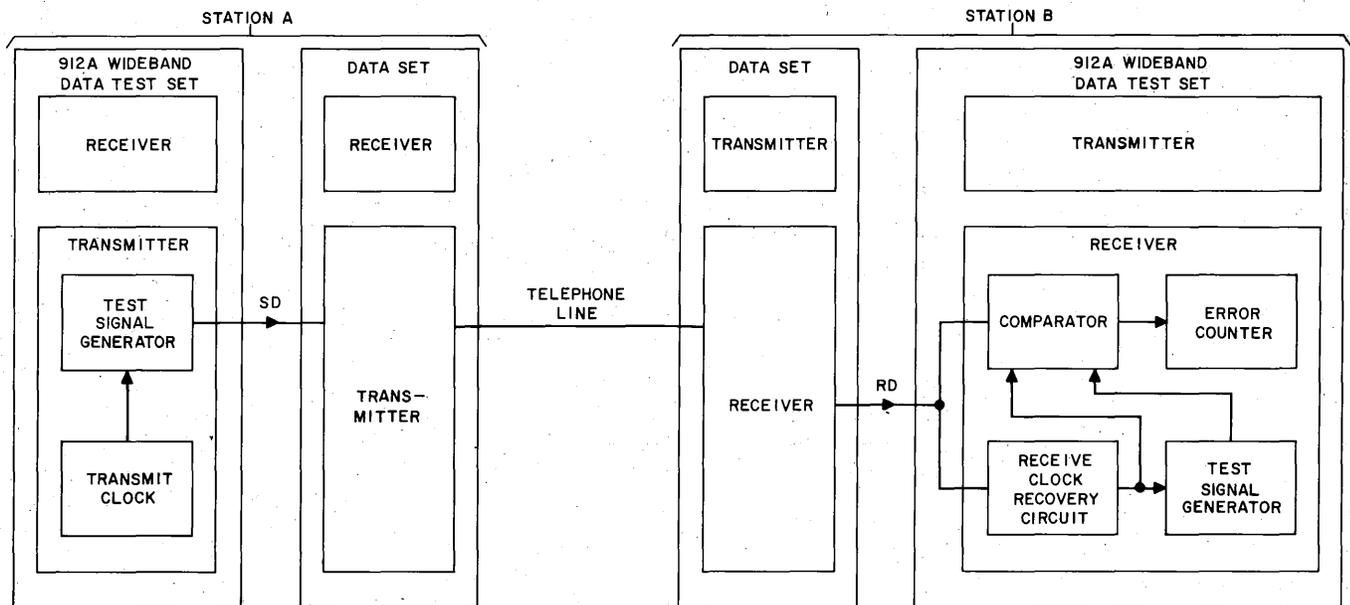


Fig. 14—End-to-End Nonsynchronous Test, Functional Block Diagram

**Note:** Limits for error rates will be specified by the sections describing the data sets or stations being tested.

#### Long-Term Unattended Error Rate Test

**4.07** Long-term error rate tests without the attendance of an operator can be performed by using an external (Hewlett-Packard 5245L or equivalent) counter and a digital recorder. The 912A WDTs is connected as shown in Fig. 16. With error pulses applied to the signal input and the counter gated at intervals appropriate to the bit rate of the data set under test, the counter records the errors per interval. The counter activates the digital recorder which provides a printed record of the error rate.

**Note:** The COUNTER switch on the 912A WDTs has no effect on the errors out signal and need not be turned ON while using the error-recording system.

## 5. MAINTENANCE

**5.01** No field maintenance is to be attempted on the 912A WDTs with the exception of replacing lamps and fuses as shown in Fig. 2 and readjusting the potentiometers controlling the bit sync multivibrators as described in 5.07.

**5.02** To gain access to panel associated circuits, fuses, and spare fuses which are located behind the panel, release the quarter-turn, twist-lock fasteners and pull the inner front panel forward from the bottom. The supporting bar, located behind the front panel, can be latched to hold up the panel.

#### Testing of the 912A WDTs

**5.03** The following test procedures for the 912A WDTs are primarily to verify that the set is performing within tolerances and are to be performed in sequence. If the 912A WDTs fails to meet the test requirements, return it to the nearest distributing house for repair.

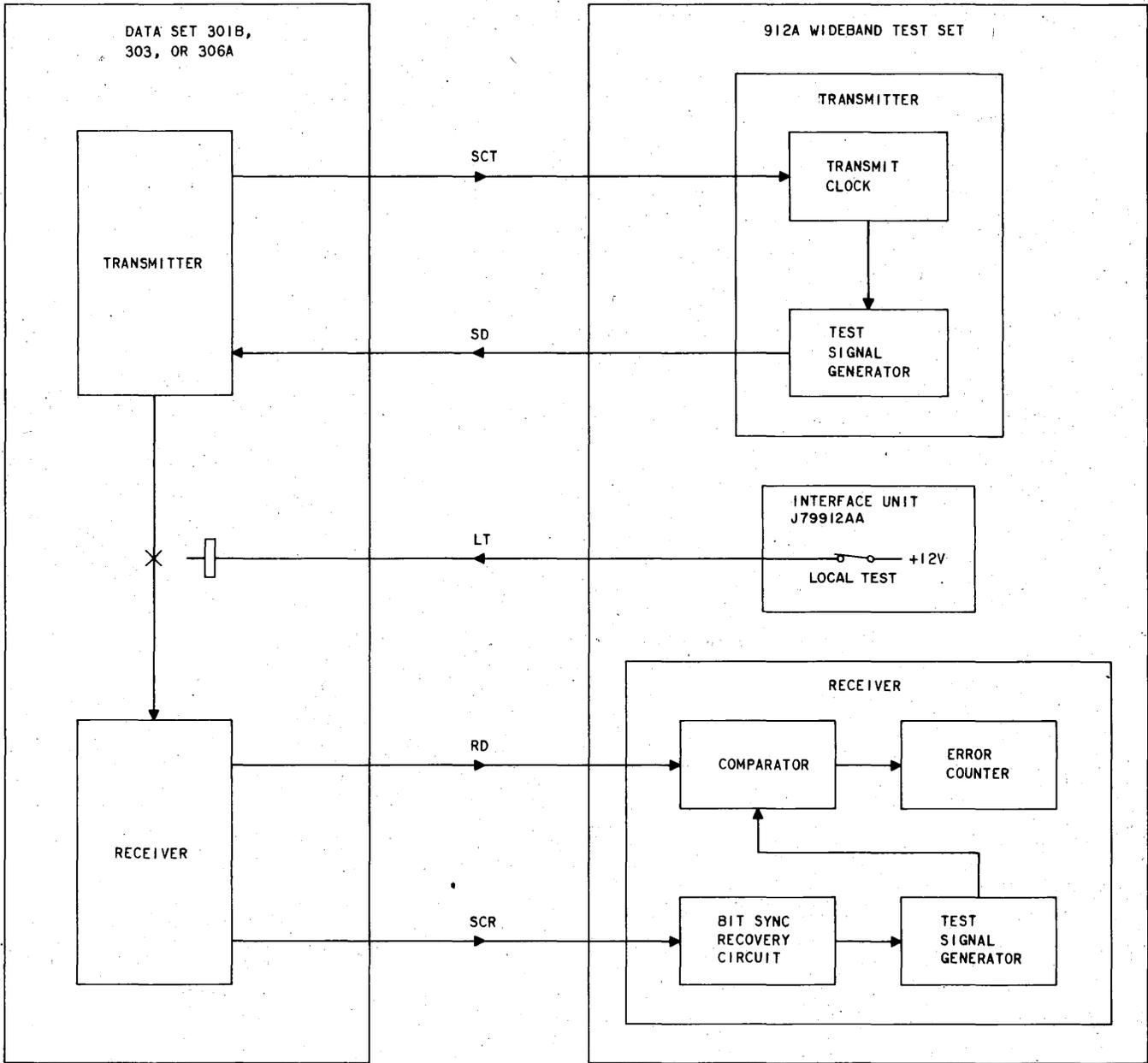
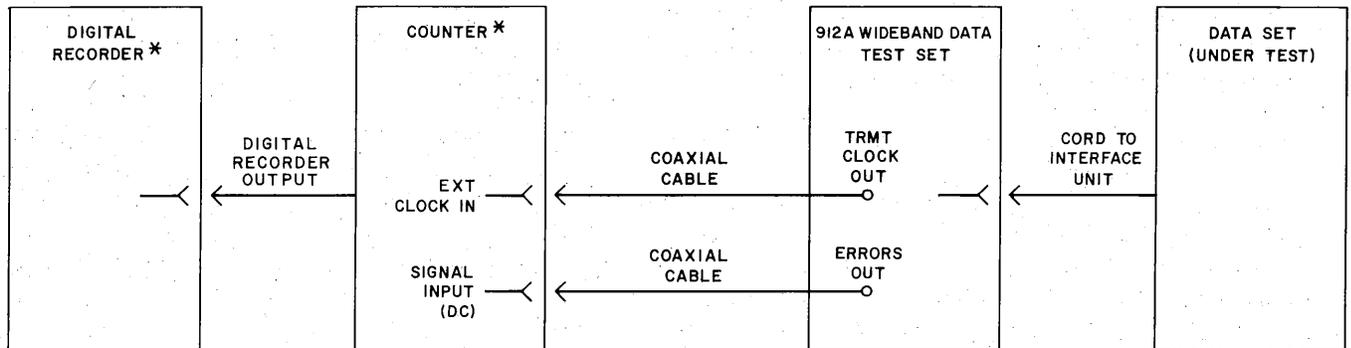


Fig. 15—Local Synchronous Test, Functional Block Diagram



\* THE COUNTER AND RECORDER ILLUSTRATED HERE ARE THE HEWLETT PACKARD 5245L AND HEWLETT PACKARD 562A, RESPECTIVELY. COUNTERS AND RECORDERS OTHER THAN THOSE SPECIFIED HERE MAY BE USED PROVIDED PROPER OPTIONS ARE SELECTED TO INSURE COMPATIBILITY BETWEEN UNITS.

Fig. 16—Connection Diagram for Unattended Error Rate Test

**5.04** When the interface unit TEST MODE switch is positioned to LOOPED, the transmitter test signal is applied to the receiver input making self-test of the 912A WDTS possible.

**5.05** Perform self-test as follows:

- (a) Connect the 912A WDTS power cord to a utility outlet.
- (b) Position the POWER switch to ON.
- (c) Position the TEST MODE switch to LOOPED.
- (d) Perform the steps in Table F.

**Note:** The self-test should be performed at each bit rate, with jack at each test signal, and with input/output normal and inverted. Insure that the transmit and receive BIT RATE switches, the transmit and receive TEST SIGNAL switches, and the transmit OUTPUT and receive INPUT switches are set to the same position.

#### Total Errors Counter Check

**5.06** Perform total errors counter check as follows:

- (a) Set the 912A WDTS switches according to Table G.

(b) After setting the switches according to Table G, the counter should read all zeros; the NO DATA, NO SYNC, and OVERFLOW lamps remain extinguished.

(c) Depress WORD SYNC switch to the manual position for approximately 1 minute. After releasing the WORD SYNC switch, the count should be divisible by 40 without a remainder.

#### Bit Sync Circuit Test and Adjustment

**5.07** The following procedure is to be at each bit rate. Insure that both the transmit and receive BIT RATE switches are set to the desired bit rate. In the event that readjustment is required, adjust the potentiometer corresponding to the bit rate being tested (Fig. 17).

**5.08** Perform bit sync circuit test and adjustment as follows:

- (a) Set controls of 912A WDTS according to Table H.
- (b) Position interface TEST MODE switch to LOOPED.
- (c) Connect channel 1 of Tektronix type 561A oscilloscope or equivalent to RECEIVE—DATA

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IN. Connect channel 2 of oscilloscope to RECEIVE—ERROR OUT and synchronize scope externally to TRANSMIT—CLOCK OUT (Fig. 18).

(d) Error pulses should be observed on channel 2 of oscilloscope.

(e) Adjust oscilloscope so that one bit interval (channel 1) corresponds to 10 cm on the horizontal scale. The time base of the oscilloscope must be adjusted by using its VARIABLE control. See Fig. 19 for an indication of the correct pattern.

(f) The error pulse (channel 2) should lie near the center of the time base scale. Adjust potentiometer R38 on CP 11 (Fig. 17) until the leading edge of the error pulse is centered as shown in Fig. 19.

(g) Set TIMING control to +10. Leading edge of pulse shall be  $1 \pm 0.15$  cm to right of center.

(h) Set TIMING control to +20. Leading edge of pulse shall be  $2 \pm 0.30$  cm to right of center.

(i) Set TIMING control to +30. Leading edge of pulse shall be  $3 \pm 0.45$  cm to right of center.

(j) Set TIMING control to -10. Leading edge of pulse shall be  $1 \pm 0.15$  cm to left of center.

(k) Set TIMING control to -20. Leading edge of pulse shall be  $2 \pm 0.30$  cm to left of center.

(l) Set TIMING control to -30. Leading edge of pulse shall be  $3 \pm 0.45$  cm to left of center.

(m) Reset TIMING control to 0.

(n) Repeat the above procedure for each bit rate provided in the 912A WDTS.

## 6. REFERENCES

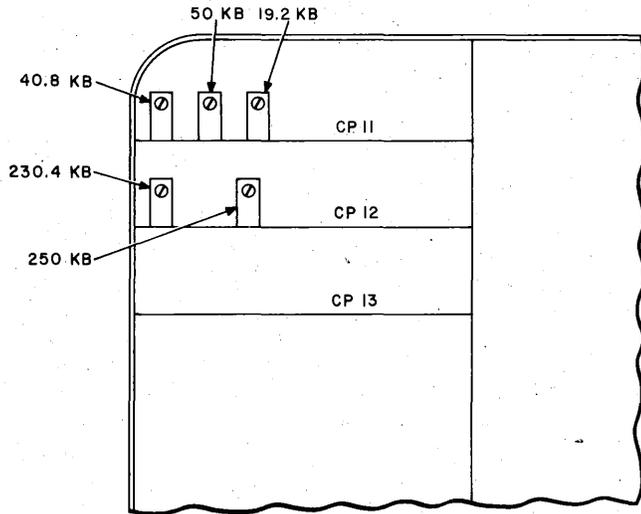
6.01 For detailed information on the 912A WDTS, refer to CD- and SD-73047.

**TABLE F**  
**912A WIDEBAND DATA TEST SET SELF-TESTING PROCEDURE**

TRANSMIT		RECEIVE		INDICATION
SWITCH	POSITION	SWITCH	POSITION	
(2) TRIGGER	Either	(18) COUNTER TRIGGER	OFF Either	NO DATA, NO SYNC, and OVERFLOW lamps extinguish and remain extinguished. The total error count should indicate all zeros.
(4) OUTPUT	NORMAL	INPUT	NORMAL	
(4) OUTPUT	MARK	(5) WORD SYNC (6) TIMING (7) COUNTER (8) Reset	AUTO 0 ON Momentarily Depress	
(10) OUTPUT	INVERTED	INPUT (11) Reset	INVERTED Momentarily Depress	NO DATA and NO SYNC lamps should light and remain lighted. The counter should count. <i>Note:</i> At bit rates over 19.2, the OVERFLOW lamp should light.  NO DATA, NO SYNC, and OVERFLOW lamps extinguish and remain extinguished. The total error count should indicate all zeros.

**TABLE G**  
**TEST SET SWITCH SETTINGS FOR**  
**TOTAL ERRORS COUNTER CHECK**

TRANSMIT		RECEIVE	
SWITCH	POSITION	SWITCH	POSITION
BIT RATE	250	BIT RATE	250
TRIGGER	Any	TRIGGER	Any
TEST SIGNAL	2087	TEST SIGNAL	2087
OUTPUT	NORMAL	INPUT	NORMAL
		COUNTER	ON
		WORD SYNC	AUTO
		Reset	Depress



**Fig. 17—Rear View of 912A Wideband Data Test Set Showing Bit Sync Potentiometers**

**TABLE H**  
**TEST SET CONTROL SETTINGS**

CONTROL	POSITION
TRMT-TEST SIGNAL	2047
OUTPUT	NORMAL
TRMT-TRIGGER	+
TIMING	0
RCV-WORD SYNC	NEUT
RCV-TEST SIGNAL	DOT
INPUT	NORMAL
RCV-TRIGGER	+
COUNTER	OFF

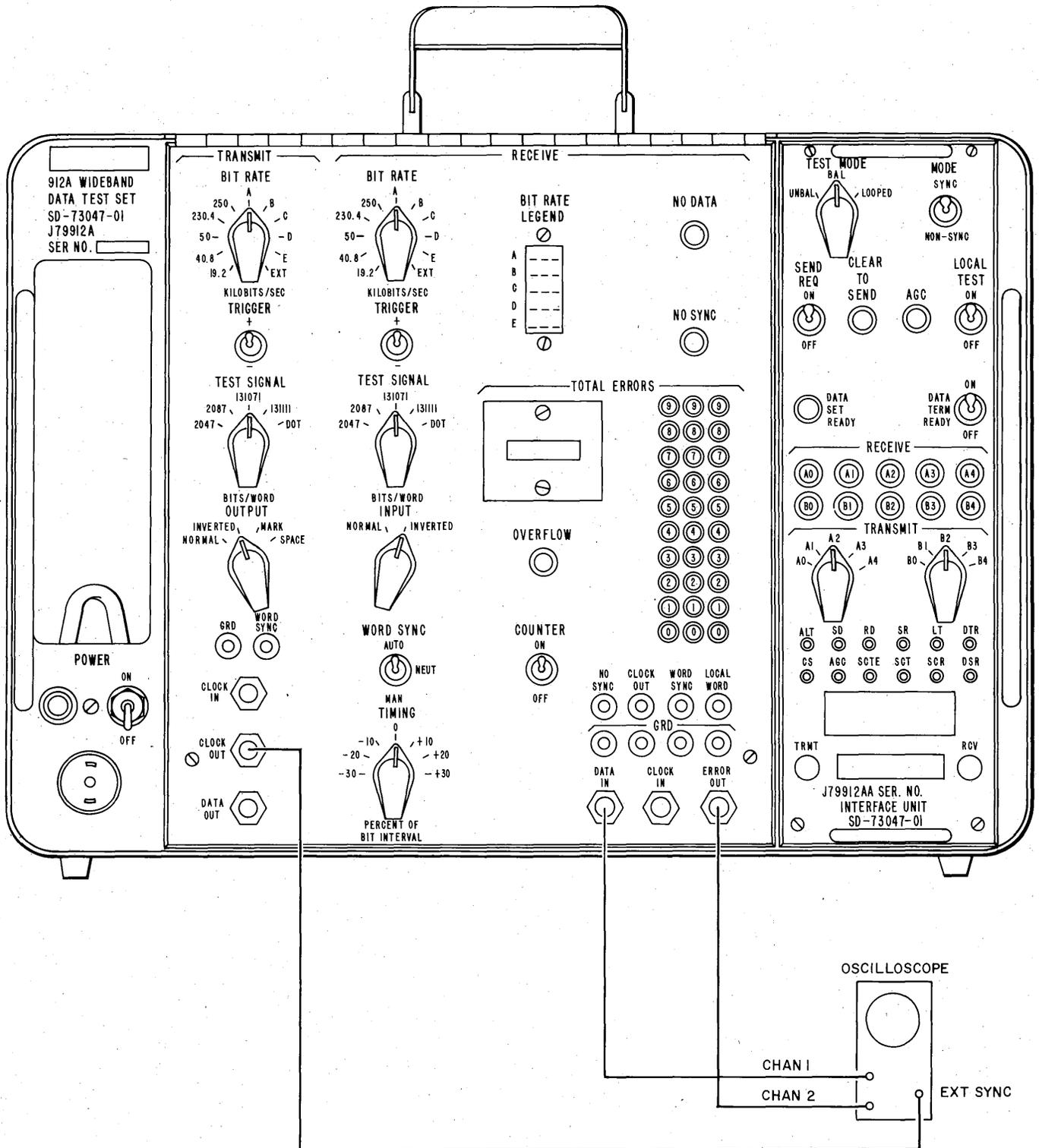


Fig. 18—Test Connections for Bit Sync Circuit

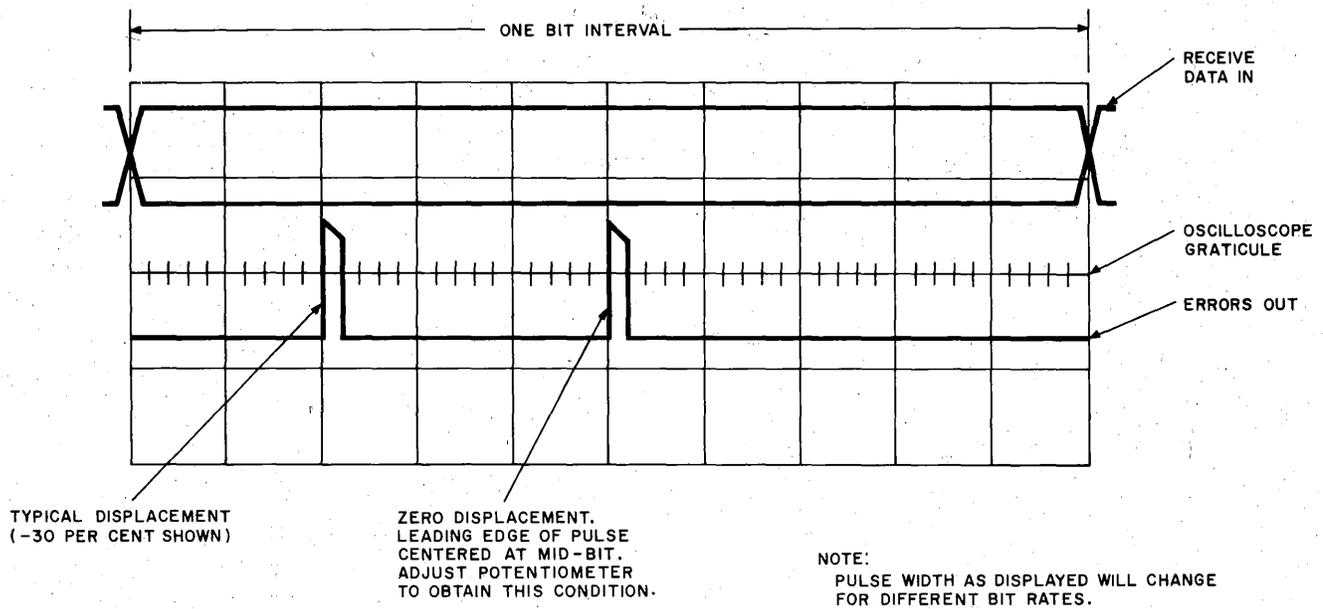


Fig. 19—Bit Sync Adjustment