921A DATA TEST SET
DESCRIPTION AND OPERATION

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1. GENERAL

1.01 This section provides a description and operation of the 921A data test set (DTS), hereafter referred to in this section as the DTS.

1.02 A third version of the DTS (Version 3) has been developed to provide increased testing capabilities for new data sets and services and to improve on the capabilities of Versions 1 and 2. This section has been reissued to incorporate these

changes and to explain the differences between the three versions. A Version 1 DTS can be converted to a Version 2 at a Western Electric repair center. Version 2 can be field-converted to Version 3 by installing a kit of parts available from WECo. The number of the kit is J79921A, L52. The list codes for Versions 1, 2, and 3 DTS are J79921A-L1, J79921A-L2, and J79921A-L3, respectively.

1.03 The DTS is a portable, general purpose data test set. It has been developed for use by craft personnel at the station location for preservice and maintenance testing of serial data services. End-to-end or station-to-serving test center tests of both synchronous data sets (201-, 208-, 209-type) and data service units (DSUs) (500 and 501), and nonsynchronous data sets (202-type) and 550 channel service units (CSUs) are possible. In addition, 212-type data sets can be tested with a Version 2 or 3 DTS. (A Version 1 DTS can perform certain tests on 212-type data sets.) Also, with Versions 2 and 3 the Transaction III Network Service (TNS) and DATAPHONE® Select-A-Station (DSAS) can be tested. Other data sets such as the 103- and 113-type may be tested provided they conform to one of the specified interfaces. Any data set may be tested provided it is interface compatible with the DTS.

1.04 Detailed test procedures for individual data sets or the particular data service, using the DTS, are found in the appropriate Bell System Practice (BSP).

1.05 The DTS provides the serial testing capabilities of the 914C DTS; replaces and/or is compatible with the 901, 902, and 903 DTS; is compatible with the 911 DTS and the 911NA DTS; and replaces the 912A wideband DTS for 56 kb/s testing on DATAPHONE digital service (DDS). Listed below are the major DTS features.

Versions 1 through 3

- Three plug-in interface modules (EIA RS-232-C, 550 CSU, and CCITT V.35) with Version 1, and a fourth [Transaction Network (TN)] with Versions 2 and 3.
- Flexibility in connecting to new data service interfaces.
- Switch control and pin access of up to 37 interface leads.
- Thirteen fixed and four assignable interface status indicators.
- Synchronous and asynchronous (start-stop) operation.
- Provides clock for synchronous data sets equipped with external clock option.
- Bit speeds of up to 56 kb/s.
- Full- or half-duplex operation.
- Bit error, block error, and block count measurements.
- Manual sync interrupt capability plus out-of-sync indication.
- Manual bit error injection.
- Controlled carrier start-up testing with 128 fixed or programmable bits.
- Bridging mode for on-line monitoring.
- Isochronous distortion measurement for DDS CSUs.
- DDS control code recognition and generation for CSUs.
- Parity error measurement.
- Start-stop distortion measurement for nonsynchronous data sets (receive only—Version 1; full duplex—Versions 2 and 3).
- Transmits FOX message (short FOX message for asynchronous data sets only—Version 1; standard FOX message for asynchronous or synchronous data sets—Versions 2 and 3).
- Autoranging digital multimeter.
- Autoranging frequency counter, autoranging interval timer, and event counter.
- Preset timer to control duration of tests.
- Generation of 1004- or 2713-Hz tones at 0 dBm level.

- Analog private line talk link capability.
- Audio line monitoring.
- Keyboard input and alphanumeric display output.
- Simplified operation due to test set prompting.
- Ability to interrupt a test while in progress.
- Self-testing capability with appropriate diagnostics.
- Ability to replace read only memory (ROM) in the field.
- Storage of cables and accessories in the "saddlebag."
- Externally accessible circuit breakers.
- Duplex receptacle on power cord.

Versions 2 and 3

- TN testing.
- DATAPHONE Select-a-Station testing.
- Programmable transmit message (up to 255 characters) for either synchronous or asynchronous operation.
- Display received message (up to 255 characters) for asynchronous operation.

Version 3 Only

- Full duplex programmable message test (all terminals).
- Stored messages for testing DATASPEED® 40/1, 40/2, and 40/3 and Model 43 terminals (asynchronous ASCII).
- Stored messages for testing DATASPEED 40/4 and 4540 (synchronous ASCII and EBCDIC with bisynchronous line protocol).

1.06 Many of the features have been realized through the use of a general purpose microcomputer which functions as a central controller and a signal processor. This microcomputer administers overall control, configures measurement equipment, and processes measurement data for the DTS. Through the use of 2-digit codes, it allows human interface via the keyboard and the alphanumeric display to be implemented with a minimum of switches and knobs. The use of a memory-based controller to direct the activities of the DTS measurement circuitry provides the flexibility needed to add new test features in the future.

1.07 By means of the adapters and cables provided, terminal equipment and/or data sets are plugged into the DTS for automatic testing. Access and disconnection of any of the interface leads is accomplished by jacks and switches located at the top of the front panel. Additional switches on the interface modules permit on-line monitoring (bridging) of the interface leads.

1.08 The DTS provides automatic self-testing of major functions at system reset. Other self-tests are provided which require operator initiation.

1.09 The DTS printed circuit packs (CPs) are as follows.

CP1—Microcomputer

CP2—Counter/timer, audio, and start-stop distortion

CP3—Multimeter and data buffers

CP4—Isochronous distortion and clock

CP5—Status indicators and cross-connect network

CP6—Pseudorandom word generator (Version 1 only)

CP7—EIA RS-232-C plug-in module

CP8—550 CSU plug-in module

CP9—CCITT V.35 plug-in module

CP10—LED indicators, interface lead switches, and jacks

CP11—Pseudorandom word generator and expanded memory (Versions 2 and 3—replaces Version 1 CP6)

CP12—Transaction Network plug-in module (Versions 2 and 3).

2. PHYSICAL DESCRIPTION

2.01 The DTS (Fig. 1) is entirely self-contained with all necessary accessories stored in the "saddlebag." The DTS may be used horizontally or in an upright position using two removable feet.

2.02 Figures 2, 3, and 4 show the cover and accessories contained therein. The cover is fitted with a molded plastic insert which facilitates the orderly placement of the interface cables, adapters, test leads, and loopback connectors. In addition, on the face of the insert are four tables as well as an operational flowchart. Tables A, B, and C provide 2-digit codes required for the keyboard interface. The added codes for Versions 2 and 3 are shown in brackets. The cover is hinged and may be removed for convenience or when the DTS is used in the upright position. The cover may be removed from its hinges by unlocking a cover stay latch located on the left side of the cover and sliding the cover to the right (Fig. 5).

2.03 A cable accessory case ("saddlebag") (Fig. 6) is provided with Version 3 of the DTS for storing cables. The case and mounting hardware may be ordered as J79921, List 51. If a velcro strip is mounted next to the handle, the accessory case can be ordered separately as part number 841-644-628.

Caution: Accessories should not be stored by laying them on top of the

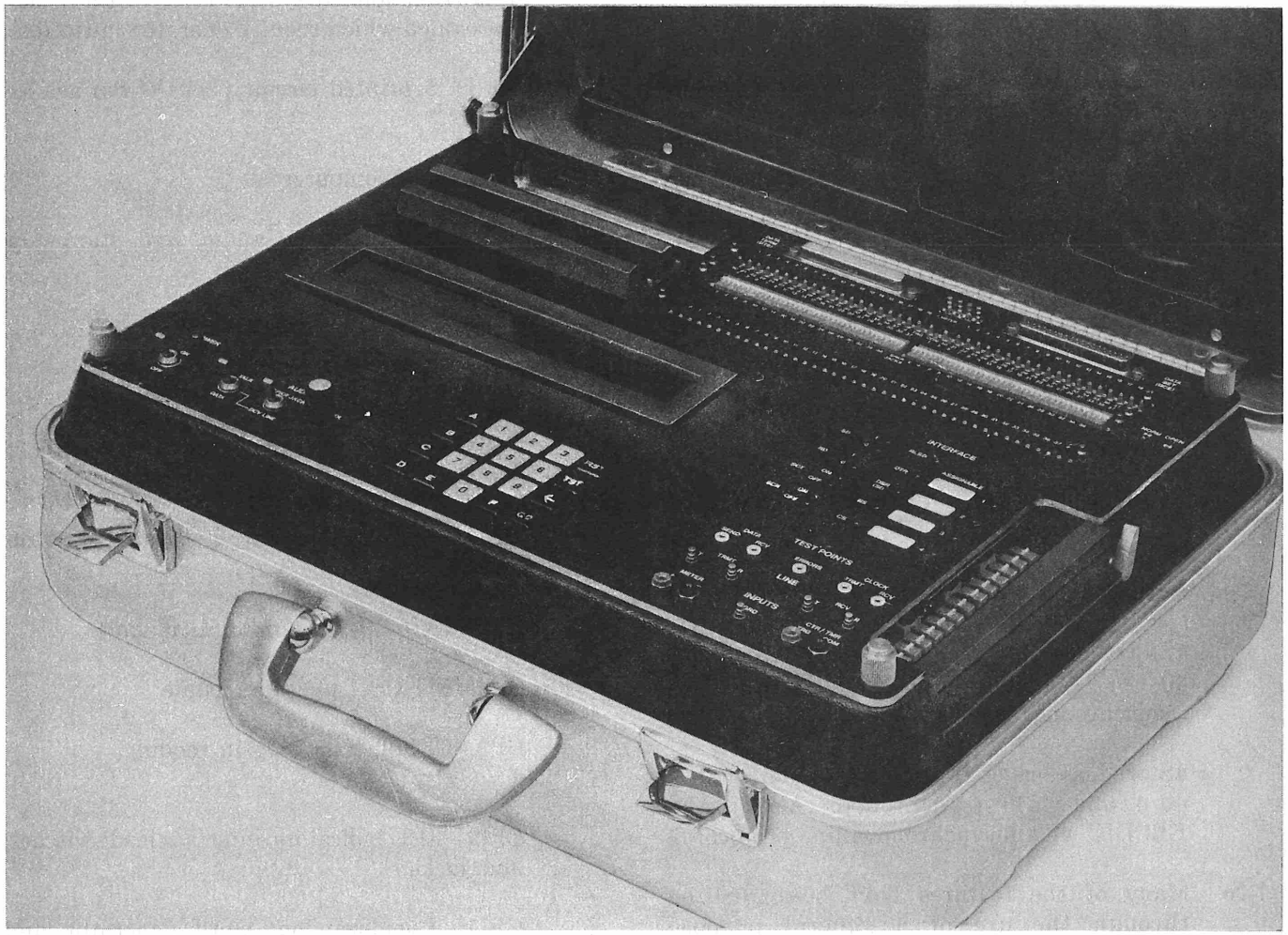


Fig. 1—DTS Front View—Cover Open

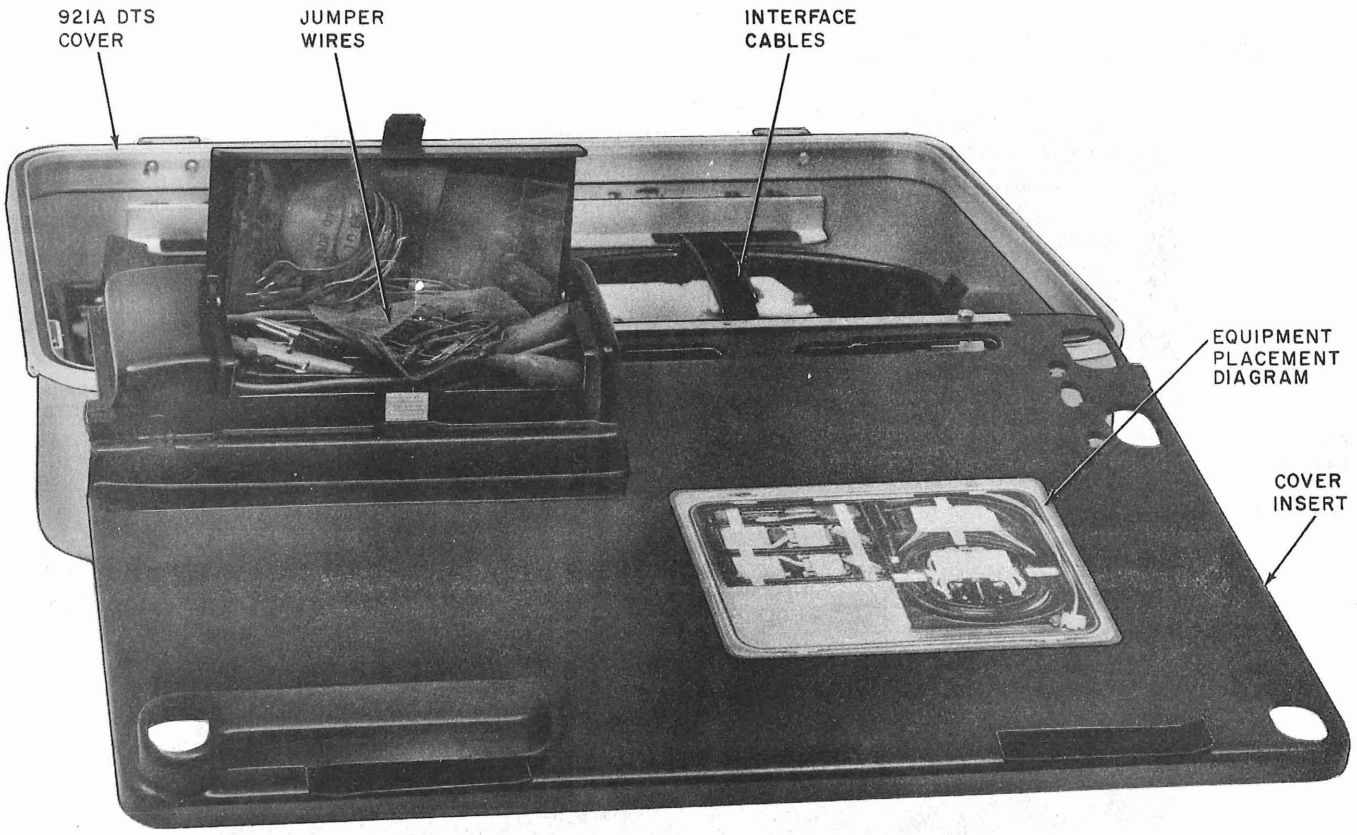


Fig. 2—DTS Cover—Insert Removed

front panel. Be sure all jumper wires are removed from pin jacks before closing cover. Closing the cover with any items on the front panel could cause the light emitting diodes (LEDs) to break.

2.04 In its carrying case, the DTS is approximately 18 inches wide, 13 inches high, 7 inches deep, and weighs approximately 33 pounds.

2.05 The DTS may be removed from the case by freeing four captive screws (one in each corner of the front panel) and lifting the front panel and chassis from the case. The section entitled 921A DTS—Maintenance (107-402-500), gives details of disassembly and troubleshooting procedures.

2.06 The DTS requires 117-volt, 60-Hz, 60-watt power for operation. Two power supplies provide the necessary operating voltages. One supply provides 250 volts for the alphanumeric display; the second provides +12, -12, and +5 volts for the test set circuits. A continuous duty fan is used to moderate the interior temperature of the DTS.

2.07 Three circuit breakers, located on the DTS left side (Fig. 7), are employed for protection of the circuits and components. The main circuit breaker detects surges on the line and, in conjunction with a thermostat, prevents damage due to high temperature conditions inside the DTS. The circuit breaker labeled 3 protects the +12, -12, +5 volt power supply, while the circuit breaker labeled 0.3 provides protection for the 250-volt display supply.

2.08 On the DTS left side, adjacent to the circuit breakers, are two terminals for the 1013-type handset, a load plug for the 117-volt power cord, and a 9-pin telephone interface connector.

2.09 The various controls and indictors located on the DTS are shown and listed in Fig. 8.

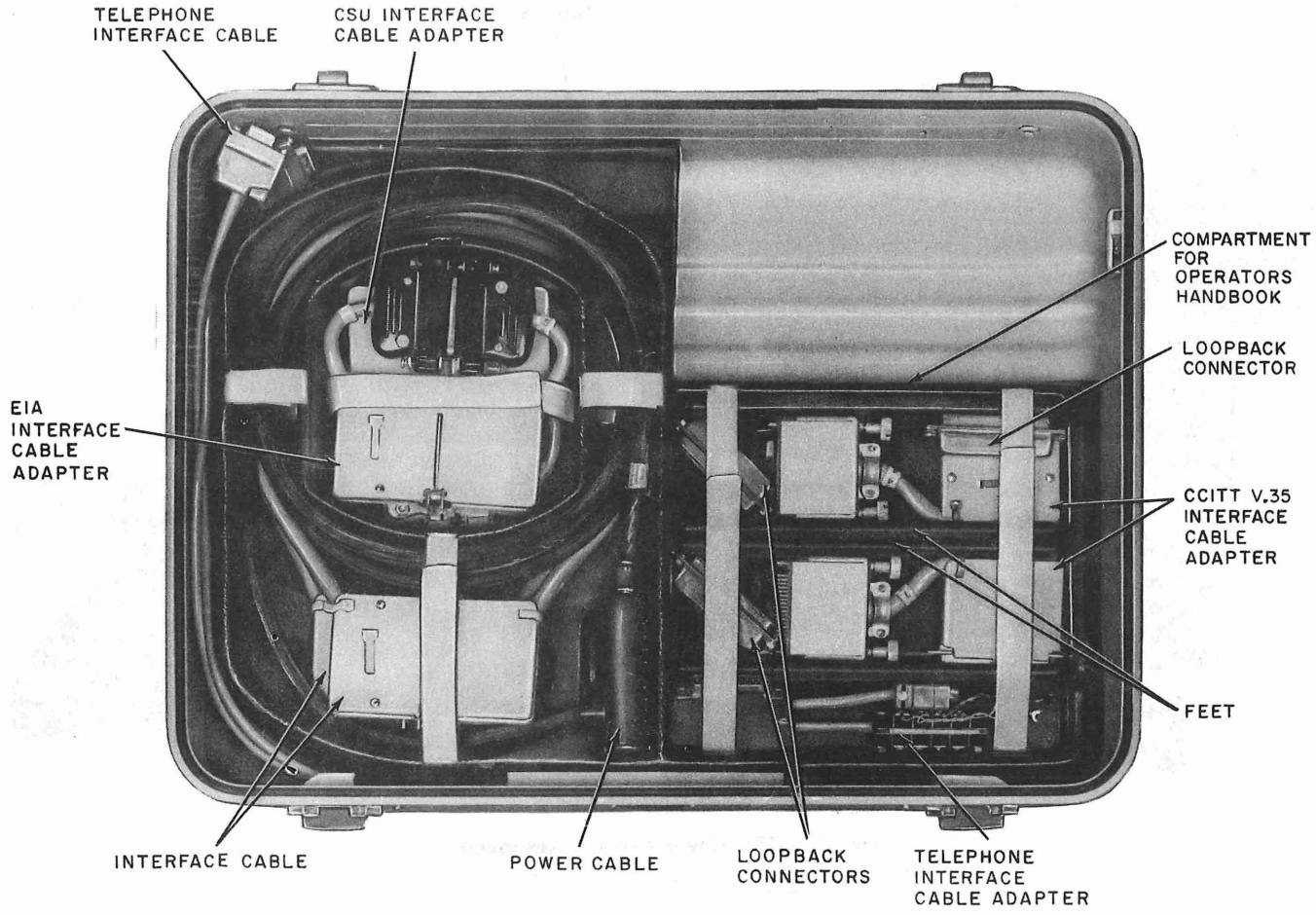


Fig. 3—DTS Cover Interior—Insert Removed

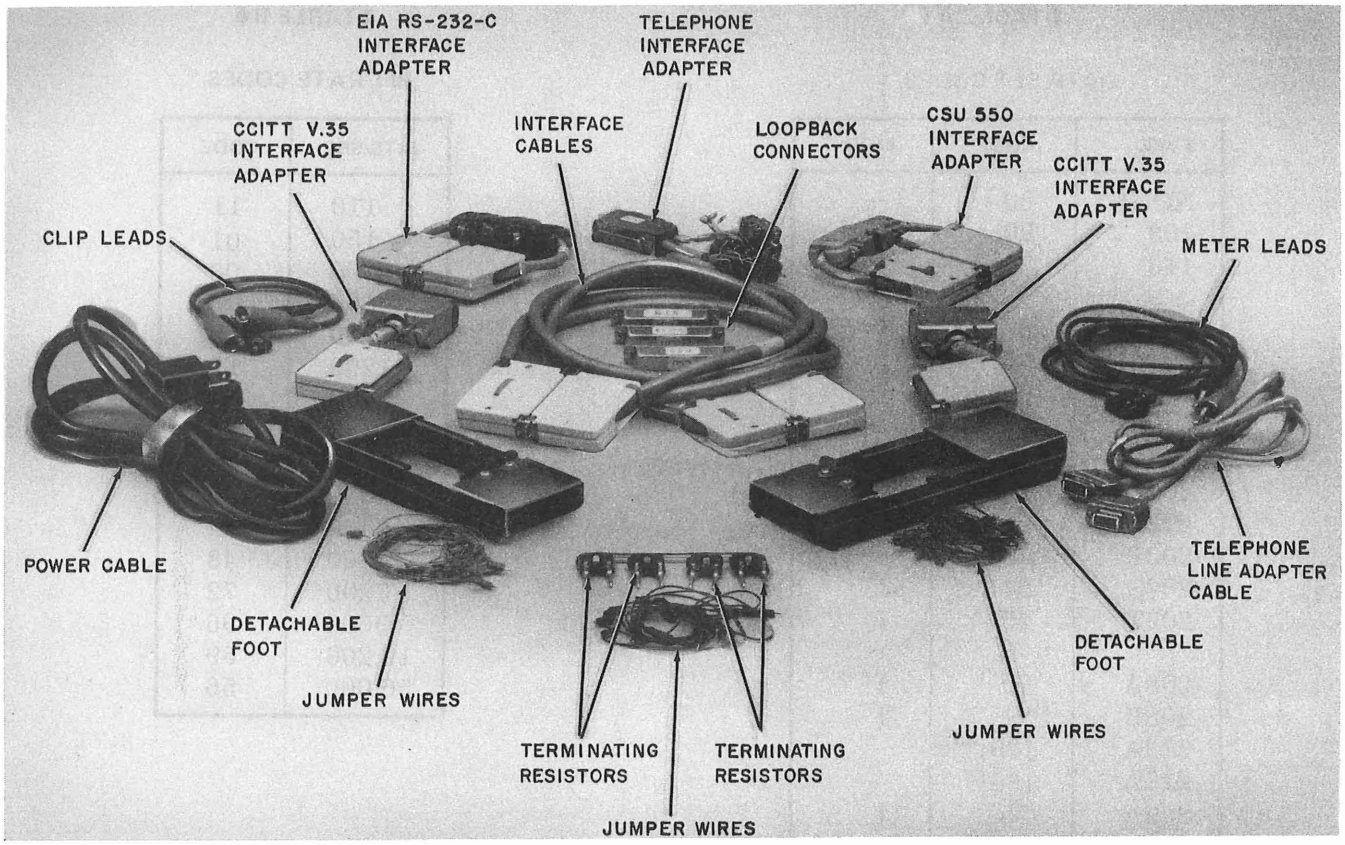


Fig. 4—DTS Accessories

◗TABLE A◖

DATA SET CODES

TYPE	CODE	MOD
NONE	00	—
103	20	I
113	20	I
201A	60	I
201B	61	I
201C	62	I
202C	20	I
202D	21	I
202E	22	I
202R	23	I
202S	24	I
202T	25	I
208A	70	I
208B	71	I
212A[3]	[36][5]	
212A[4]	[66][5]	
209A	75	I
500A[1]	80	I
500A[2]	81	III
501A[1]	85	I
501A[2]	86	III
550A	50	II
DSAS	[10][5]	I
TNS	[13][5]	IV
EXP	99	ANY

1: Subrate

2: 56 kb/sec

3: Asynchronous

4: Synchronous

5: Brackets [ ] denote Versions 2 and 3.

◗TABLE B◖

BIT RATE CODES

BITS/SEC	CODE
110	11
150	01
300	03
600	06
1000	10
1200	12
1400	14
1600	16
1800	18
2000	20
2400	24
4800	48
7200	72
9600	96
19,200	59
56,000	56

TABLE C

TEST CODES

NO.	CODE
	UTILITY DISPLAYS
00	Version Number
01	Data Set Code
02	Bit Rate Code
03	Test Codes—Selected
04	—Remaining
	UTILITY ROUTINES[4]
08	Set Message Display Time
09	Manufacturing Test Only
	GENERAL PURPOSE
10	Multimeter—Ohms
11	—AC Volts
12	—DC Volts
15	Event Counter—Internal[1]
16	—External
17	Frequency Counter—Internal[1]
18	—External (AC Coupled)
19	—External (DC Coupled)
20	Interval Timer—Internal (A or B First)[1]
21	—Internal (A First)[1]
22	—External (TRG Input Only)
	LINE OPERATIONS
25	Talk Link
26	Transmit—1004 Hz
27	—2713 Hz
	INTERFACE OPERATIONS
29	Monitor SD (Defaults to RD if TEST SEQ Appears)
30	RS—CS Interval
31	RS—RLSD Interval
32	RS—SQD Interval
36	Control—RS (Assigns RS to S1)
37	—DTR (Assigns DTR to S2)
38	—S1—S4 (Must be Preassigned)[1]
39	Reverse Channel
40	Automatic Answer
	PROGRAMMABLE CLOCK
43	Free Run[2]—RCV & TRMT
44	Phase Locked[2]—RCV & TRMT
45	—RCV Only
46	Enable Automatic Settings

NO.	CODE
	ASSIGNABLE CONNECTIONS
47	Open
48	Assign (Overrides Automatic Connections)
	SEQUENCE GEN. & ERROR TESTS
50	Display RCV Characters—ASYNC[3]
51	Programmable Message—TRMT[3]
52	FOX Message—TRMT
53	TRMT Dot, Space, Mark and
54	RCV 2047, 511, or 63 Bit
55	FDX Pseudorandom Word
57	Parity—RCV
58	Full Duplex Programmable Message[4]
	DDS CODE
62	Zero Suppression—FDX
63	Idle—FDX
64	Out-of-Service—RCV
65	Not Ready—TRMT
	START-UP
67	Standard Message—Controlling
68	—Controlled
70	Programmable Message—Controlling
71	—Controlled
	DISTORTION
78	Isochronous—RCV
79	Start-Stop —RCV
	DATA SERVICES
80	DATAPHONE® Select-A-Station[3]
83	Transaction III Network[3]
	SELF-TESTS
94	Loopback Error Test
95	Multimeter Test
96	Keyboard, Display and LEDs
97	Interface Module and Cables
98	
99	Manufacturing Tests Only[3]

1: Precede by test 48.

2: Overrides automatic clock settings.

3: Versions 2 and 3.

4: Version 3 only.

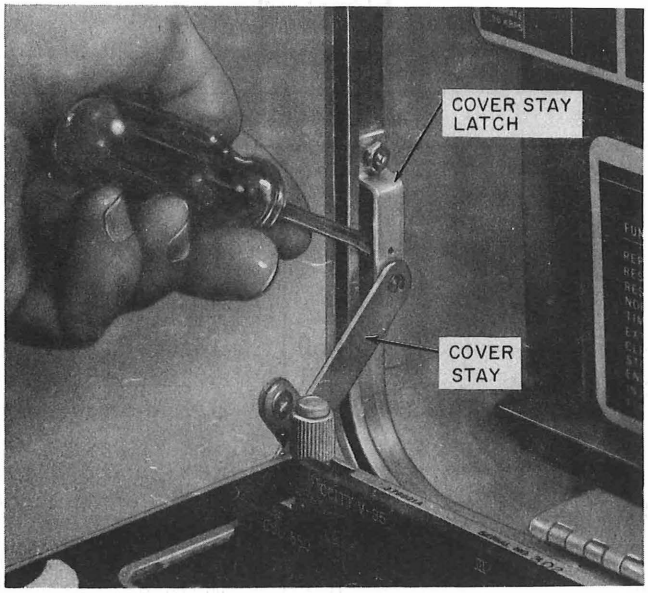


Fig. 5—DTS Cover Removal

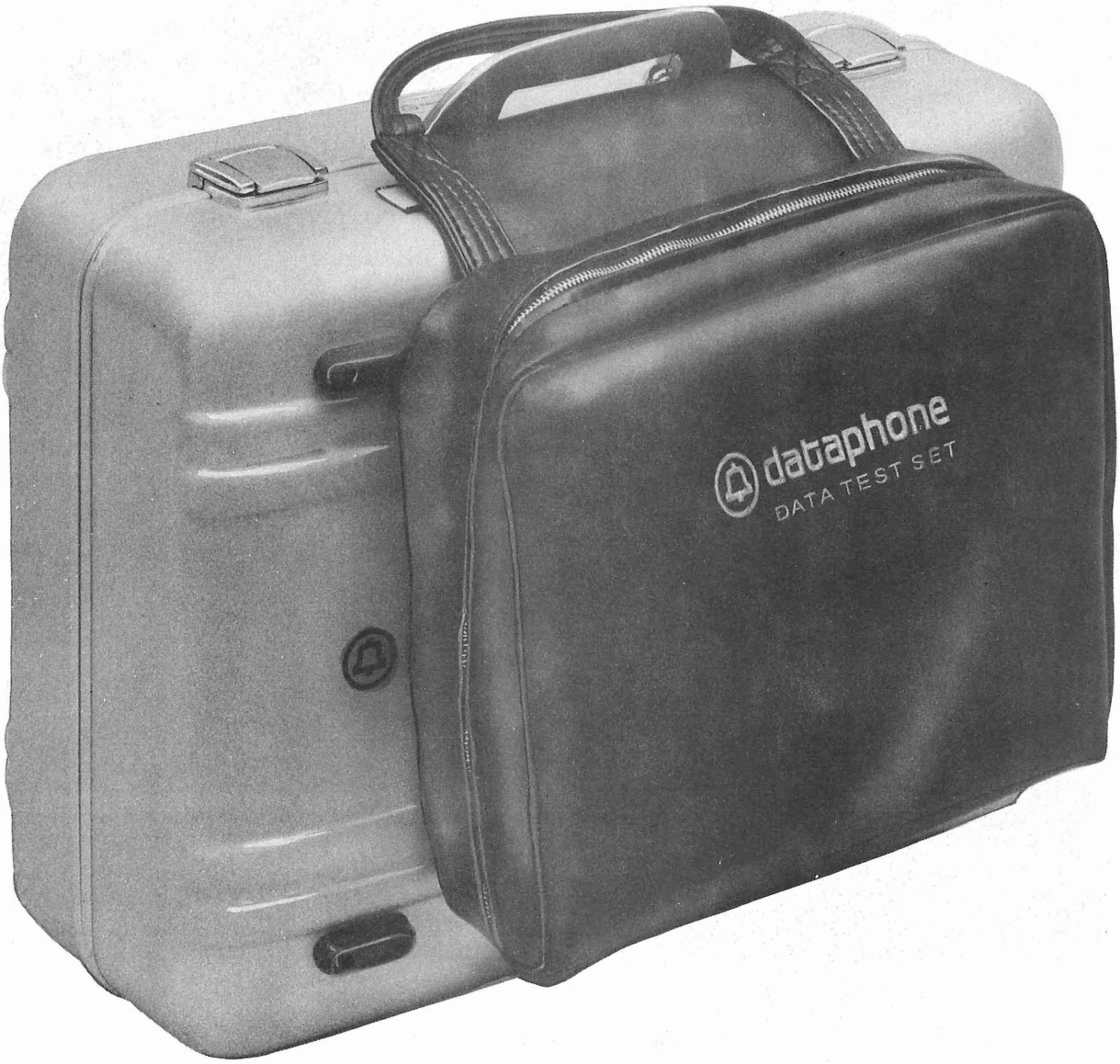


Fig. 6—Cable Accessory Case on DTS

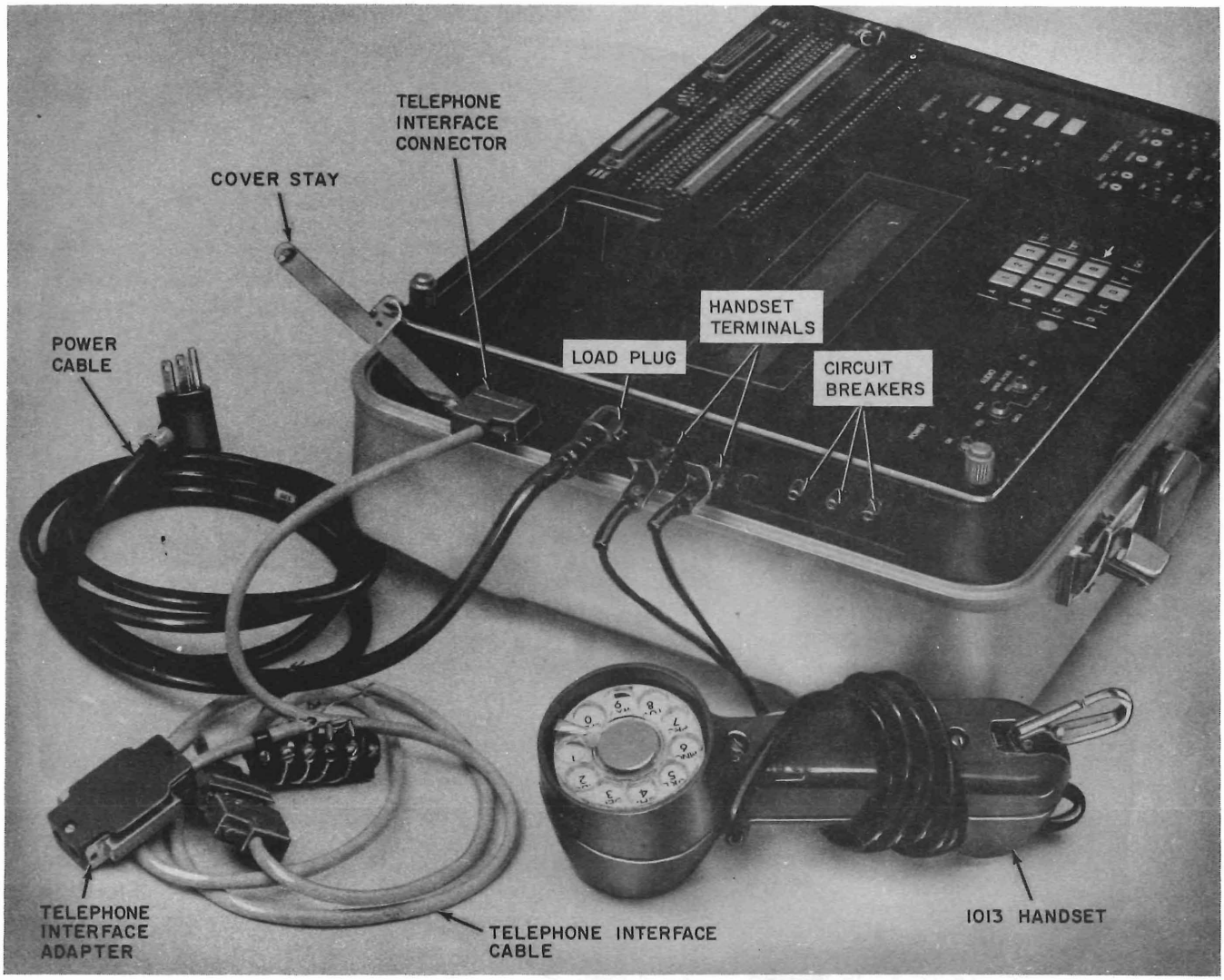


Fig. 7—DTS Left-Side View

3. FUNCTIONAL DESCRIPTION

3.01 This description is based on the DTS Functional Block Diagram, Fig. 9. Each of the four functional units will be discussed.

HUMAN INTERFACE

3.02 All information is entered into the DTS via the keyboard. The keyboard has ten numeric, six alpha, and four control keys. All requests are entered as 2-digit codes. These codes are listed in three tables: Data Set Codes, Table A; Bit Rate Codes, Table B; and Test Codes, Table C. The use of these tables is explained in the following paragraphs and similar tables are also included in the DTS cover.

3.03 Table A associates each data set type with an appropriate 2-digit code and an interface module number. Code 99 is reserved for synchronous experimental data sets, new synchronous data sets, or synchronous data sets other than those listed. The data set code conditions the DTS interface module and selects the appropriate interface LEDs. Additionally the data set code is used by the tests selected subsequently to program the DTS cross-connect and clock mode. Table B associates each available bit rate with an appropriate 2-digit code. Table C lists the 2-digit codes in numerical order and associates each with a test function. Part 4 provides a description of the individual tests.

3.04 The functions of control keys labeled RST, TST, ←, and GO, are described in Table D. The alpha keys (A, B, C, D, E, F) have special functions which may vary depending on the particular test. Table E shows their functions for each test. They are also used to input hexadecimal information required for tests which permit the programming of data characters. Editing and data display features have been added for two of the tests in Versions 2 and 3. The alpha and ← keys have additional

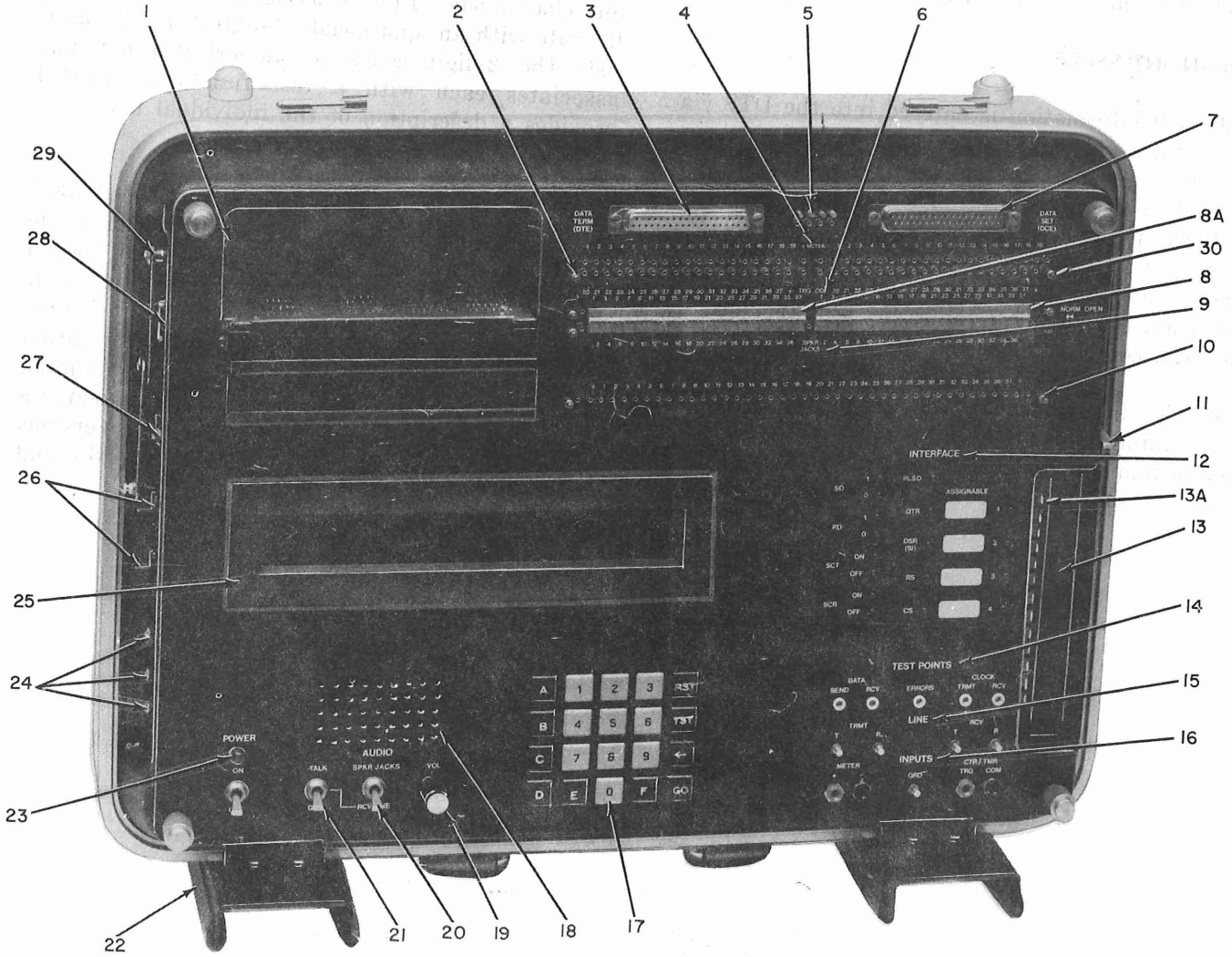


Fig. 8—DTS Controls and Indicators

LEGEND–921A CONTROLS AND INDICATORS

NO.	ITEM	DESCRIPTION
1	Module Storage Area	Provides for storage of up to four interface modules.
2	Interface Lead Jacks	Provide access to signals on DATA TERM (3) or DATA SET (7) connectors.
3	DATA TERM (DTE) Connector	A 37-pin connector used to interface customer terminal equipment.
4	METER +, — Jacks	Provide convenient input to multimeter from the interface lead jacks (2).
5	Auxiliary Post Jacks	Provide means to interconnect interface lead jacks (2) to other equipment.
6	TRG, COM Jacks	Provide convenient input to counter/timer from the interface lead jacks (2).
7	DATA SET (DCE) Connector	A 37-pin connector used to interface data set.
8	DCE Interface Lead Switches	Provide means for breaking connection of DCE individual interface signals.
8A	DTE Interface Lead Switches	Provide means for breaking connections of DTE individual interface signals.
9	SPKR Jacks	Provide access to the speaker.
10	Common Interface Lead Jacks	Provide access to signals at DTS side of lead switches (8).
11	Locking Lever	Secures interface module in module port.
12	INTERFACE LEDs	Monitor interface lead status.
13	Interface Module Port	Receives interface module.
13A	Interface Module Switches	Switches on interface module which are used to select either TERM or MON position.
14	TEST POINTS	Provide logic level signals of interface DATA (SEND AND RCV), CLOCK (TRMT AND RCV) and ERRORS (bit or block) for driving external devices.
15	LINE Terminals	Provide access to transmit (TRMT) and receive (RCV) tip (T) and ring (R) signals when used with telephone adapter and cable.

LEGEND–921A CONTROLS AND INDICATORS (Contd)

NO.	ITEM	DESCRIPTION
16	Jack INPUTS	Provide access to multimeter and counter/timer when using test probes.
17	Keyboard	Provides for the manual input of information.
18	Speaker	Provides audible monitoring.
19	VOL	Provides volume control for speaker.
20	SPKR JACKS/RCV LINE Switch	Connects speaker to SPKR JACKS (9) or receive T and R (15).
21	TALK/DATA Switch	Selects talk or data mode when telephone/adapter and cable are used.
22	Detachable Feet	Enable DTS to be used in upright position.
23	POWER	Main power lamp and switch.
24	Circuit Breakers	Provide protection of circuits and components.
25	Display	A 32-character alphanumeric gas discharge display.
26	Handset Terminals	Connecting terminals for use of telephone handset.
27	Load plug	For connecting 117 volt ac power cord.
28	Telephone Connector	A 9-pin telephone interface used with telephone adapter and cable.
29	Cover Stay	Allows DTS cover to be removed.
30	Auxiliary Spring Post Jacks	Provide means to secure components (resistors, etc.) and to interconnect with interface lead jacks (2).

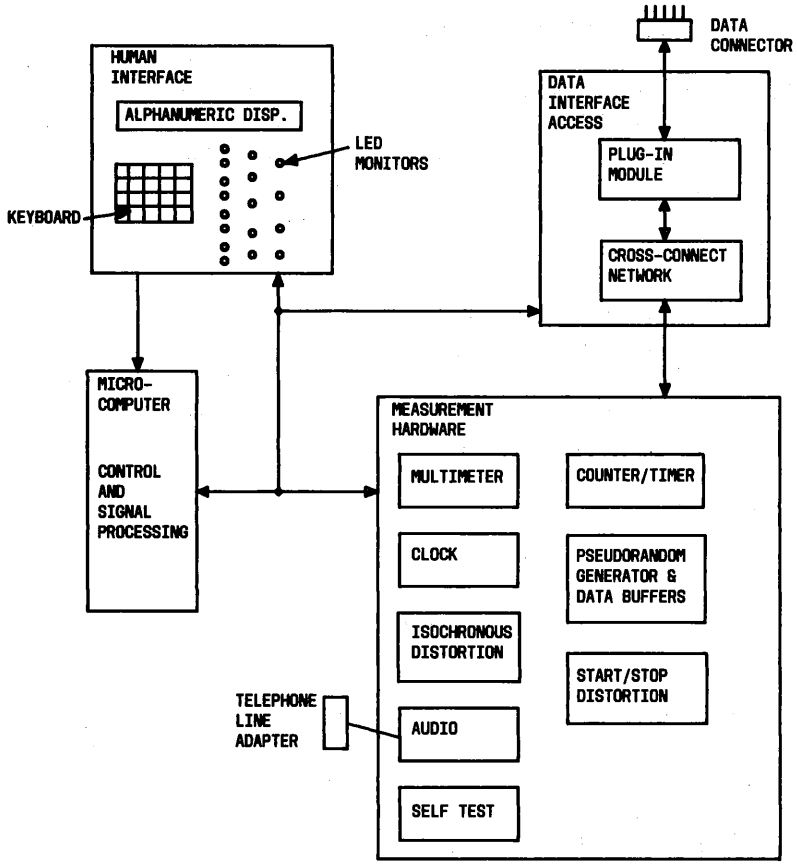


Fig. 9—DTS Functional Block Diagram

functions during the editing mode of a test as shown in Table F.

3.05 The 32-character alphanumeric display, along with 17 light emitting diodes (LEDs), provide test results and status information. Test descriptions and appropriate messages are presented in Part 4 of this section. Thirteen fixed LEDs give the state of indicated interface leads. Four LEDs are assignable by means of test code 48 (Part 4).

DATA INTERFACE ACCESS

3.06 Data sets to be tested are connected to the DTS via the DCE connector. The DTE connector is provided for data terminal access. The leads of these connectors link through the interface lead switches [Fig. 8 (8)] to the common interface lead jacks [Fig. 8 (10)]. With both the DCE and DTE interface lead switches in the normal position, the corresponding pairs of connectors (DCE and DTE) are interconnected.

3.07 Under some circumstances, a data set may be tested on an on-line basis, ie, with the terminal connected to the data set. In this case, connector DCE goes to the data set and connector DTE to the terminal. All the switches on the interface module must be in the MON position for this test.

3.08 By opening the respective DCE and DTE interface lead switches for individual interface leads, access to the data set or terminal may be obtained, breaking the connection between the data set and the customer interface (Fig. 10).

TABLE D

CONTROL KEYS

KEY	FUNCTIONS
RST	• Presents display of DTS version number at which time self tests are automatically performed. • DATA SET: message appears when self-test is successfully completed. • Cancels all information previously entered and reinitiates self-test.
TST	• Cancels all remaining tests. • Causes TEST SEQ: message to appear. • Allows operator to change test sequence without affecting data set and bit rate codes previously entered.
←	• Corrects mistakes. • Erases codes previously entered. • Shortens display time of messages.
GO	• Allows flow through operational flowchart. • Causes test sequence to begin. • Interrupts tests which do not self complete.

◗TABLE E◖

SPECIAL FUNCTION KEYS

FUNCTION	TEST CODE															
	15 16	20 21 22	30 31 32	[50][2]	[51][2]	52	53	54	55	57	58	67 68	70 71	78	79	94
Repeat Test		A	A	A	A	A		A	A		A	A	A		A[2]	A
Reset Counter	A															
Resync										A						
Normal Display														A		
Time Remaining								B	B						B[2]	B
Extended Display														B		
Clear Display								C	C	C		C	C	C	C	C
Stop Test[1]												D	D			
End Test[1]					D	D[2]		D	D						D[2]	D
Inject 8 Errors							E		E							E
Force Out-of-Sync							F		F							F
Edit Mode					←						←					
Enter Display Mode											C					
Restart											D					

1: After test is stopped, it may be resumed without affecting the display by pressing key A. However, when a test is ended it may not be resumed or continued.

2: Versions 2 and 3.

3.09 Three plug-in interface modules are provided in Version 1. A fourth (TNS) module is provided in Versions 2 and 3. The EIA RS-232-C interface module conforms to all RS-232-C electrical specifications and, in addition, provides pairs of drivers/terminators on some dual function leads. Table G shows which leads have drivers, which have terminators, and which have both. For those leads that have both drivers and terminators, the proper selection is made by the DTS according to the data set specified. Table ◗H◖ shows the correspondence between the data set code and the state of the dual function leads. The switches on the EIA interface module are used in the TERM position for normal (off-line) data set testing and must be in MON position for in-service (on-line) testing. For leads with drivers only, the MON position opens the connection to prevent loading

TABLE F

DATA DISPLAY AND EDIT KEYS*

FUNCTION	TEST CODE	
	50	51, 58
Display First Line	C	C
Display Last Line	E	E
Display Prior Line	B	B
Display Next Line	F	F
Delete Character		←
Delete Message		D
Character Location		0-9

* Versions 2 and 3.

during on-line testing. For those leads with terminators only, the MON position inserts a high impedance for monitoring.

Contacts on the interface boards must be kept as clean and free from contamination as possible to ensure continuity. Contacts may be cleaned with perchlorethylene or equivalent, as often as necessary.

3.10 The 550 CSU module conforms to Bell System standards only. It has one driver, one terminator, and one control lead. The switches on the CSU interface module function the same as those on the EIA module (paragraph 3.09).

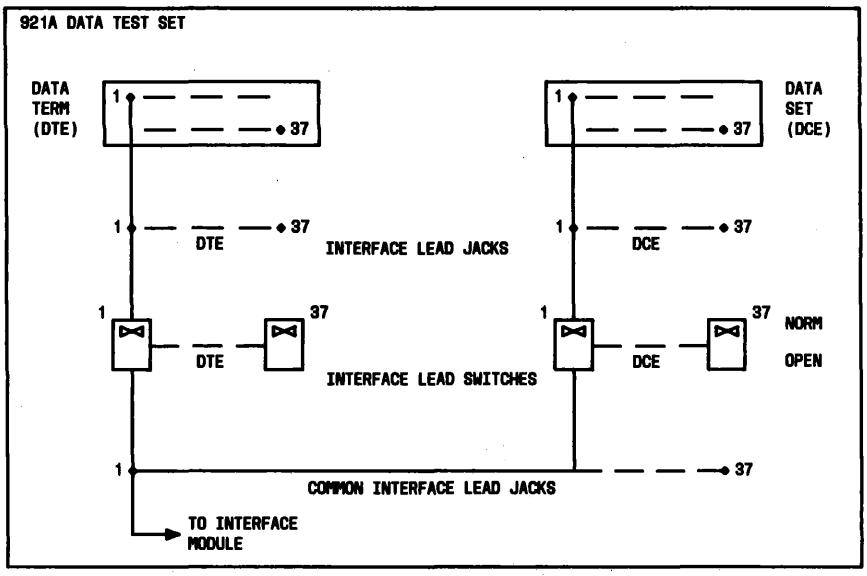


Fig. 10—DTE and DCE Interface Lead Switches and Jacks—Functional Schematic

3.11 The CCITT V.35 interface module conforms to CCITT V.28 (same as RS-232-C) except for data and clock signals which are balanced to allow higher speed operation. This module is used with 56 kb/s DSUs. The switches on the CCITT interface module function the same as those on the EIA module (paragraph 3.09).

3.12 The TNS interface module contains a complete frequency shift keyed (FSK) modem. This module is used to send and receive signals over TN facilities. It is internally connected to the tip and ring leads on the DTS 9-pin telephone connector. The data and control leads from the module do not appear on either the DCE or DTE connector. However, tip and ring do appear on these connectors.

Note: For pin assignments of each interface module, see Table G. For electrical specifications of the EIA RS-232-C, 550 CSU, and CCITT V.35 interface modules, see Table I.

3.13 Interface leads are connected to internal DTS test circuits via an electronic cross-connect

TABLE G

INTERFACE MODULE PIN ASSIGNMENTS

INTERFACE MODULE							
EIA RS-232-C (I)		550 CSU (II)		CCITT V .35 (III)		TNS (IV)	
PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
2	D	2	T	C	D		
3	T	3 }	T	D	T		
4	D	4 }		E	T		
5	T	5 }	D	F	T		
6	T	6 }		H	D		
8	T			J	T		
11	D/T			K	D		
12	T			P }	D		
13	T			S }			
14	D			R }	T		
15	T			T }			
16	T			V }	T		
17	T			X }			
18	D/T			Y }	T		
19	D			A }			
20	D			N	D		
21	D/T						
22	T						
23	D/T						
24	D						
25	D/O Vers 1						
25	D/T Vers 2 & 3						
						36	Ring
						37	Tip

D = Driver, T = Terminator, and O = Open

} = Both pins are associated with a single driver or terminator (balanced).

network. There is no external physical access to this network. For data set testing, all connections are made automatically by the DTS prior to performing a test (Table J); ◗for terminal testing, changes must be made in the jack field since the cross-connect cannot accommodate interfacing to terminals.◖ Each test requires different equipment configurations and some depend on the data set type. The DTS is preprogrammed to know these connections and to make them at the proper time. For special applications, different or additional connections may be made via keyboard commands (test codes 47 and 48). When used, these assignable connections allow the operator to have complete control over all cross-connections since they inhibit the DTS from using its preprogrammed repertoire. Not all inputs to the network may be routed to all outputs. Table K shows all allowable connections by a check at the appropriate cross-connect point.

3.14 The state of the primary interface leads is indicated by the front panel light emitting diodes (LEDs). The data LEDs (SD, RD) show the binary data states (binary 1 = Mark = negative

TABLE H

EIA RS-232-C DRIVER/TERMINATOR PAIR CONFIGURATION*

PIN	DATA SET CODE			
	20-25, 80, 85	60-62	70, 71, 75, 99	36, 66 VERSIONS 2 AND 3
11	D	T	T	T
18	T	T	T	D
21	T	D	T	D
23	T	T	T	D
25	D	O	O	T

* D=Driver, T=Terminator, O=Open

EIA voltage; binary 0 = Space = positive EIA voltage). The clock LEDs (SCT, SCR) show the ***on*** and ***off*** states of the clock signals. They should be ***off*** for those data sets that do not provide clock to the DTS and should be flickering when the data set clock is present. The control signal LEDs (RLSD, DTR, DSR, RS, CS) show the EIA ***on*** or ***off*** state of the appropriate lead.

3.15 The data and clock interface signals are available on the front panel at four test points labeled DATA (SEND, RCV) and CLOCK (TRMT, RCV). The TRMT AND RCV CLOCK and RCV DATA test points provide signals coming from the data set, whereas the SEND DATA test point provides signals originating in the DTS.

MEASUREMENT HARDWARE

3.16 The DTS clock is used when operating with nonsynchronous data sets. It also provides timing to synchronous data sets equipped with an external timing option when the EIA RS-232-C module is used. A clock signal, the frequency of which is determined by the bit-rate code entered, is present at pin 24 (SCTE). The clock is configured in three modes.

(1) Receive clock synchronized (phase-locked) to the incoming data and the transmit clock operating independently (free-running). This clock mode is used for synchronous tests (such as bit error tests) with nonsynchronous data sets (eg, 202-types).

(2) Start-stop, where the receive clock is enabled on a "start" bit and inhibited on a "stop" bit. This clock mode is used for nonsynchronous tests (such as parity tests) on nonsynchronous data sets.

(3) Both receive and transmit clocks synchronized (phase-locked) to the incoming data. This clock mode is used for tests performed on CSUs.

3.17 In the transmit direction, a hardware generator is used for dotting, marking, spacing, and all pseudorandom words. A transmit data buffer is used for sending out programmable data messages, DDS codes, and the FOX message. This data buffer is directly under control of the CS interface lead, except when testing CSUs. (Transmission does not begin until CS goes ***on***.)

3.18 In the receive direction, another data buffer is used for all receive data functions. The receive data buffer is under direct program control.

3.19 All errors measured by the DTS (bit, block, parity, and start-up) are available as pulses at the test point labeled ERRORS.

3.20 The isochronous distortion circuit gathers measurement data from the hardware counters and places it into the main memory. These counters contain time intervals (in percent of unit intervals) necessary to compute the isochronous distortion. The accuracy of the computation is +3 counts on all measurements and all bit rates. The actual computation is done by the program.

3.21 The start-stop circuit functions much like the isochronous distortion circuit, collecting time intervals (also in percent) in hardware counters and passing this information to the processor where it is interpreted and displayed. The maximum percentage error for recommended bit rates is +1 percent at ⧫110,⧫ 150, and 300 b/s, +3 percent at 600 and 1800 b/s, -1 percent at 1000 b/s, and -2 percent at 1200 b/s.

3.22 The counter/timer can be configured by the processor to perform four functions: interval timing, event counting, frequency, and count-down timing. The first three are selected by the operator using test codes 15 through 22 and 30 through 32.

TABLE I

INTERFACE MODULES ELECTRICAL SPECIFICATIONS

	EIA	CCITT	CSU
Unbalanced Driver	a. Signal output—Bipolar nonreturn to zero b. Output impedance—300 ohms minimum c. Output voltage—±10 volts nominal (load 3 kohm, 470pf) d. Rise and fall times—1 μs maximum (load 3 kohm, 470pf) e. Bit rates—Up to 20 kb/s	Same as EIA	
Unbalanced Terminator	a. Signal input—Bipolar nonreturn to zero b. Input impedance 3000 ohms to 7000 ohms c. Input signal (terminate or monitor mode) ±3 volts to ±30 volts d. Bit rates—Up to 20 kb/s	Same as EIA	Same as EIA
Balanced Driver		a. Signal output—Bipolar nonreturn to zero b. Differential output impedance—100 ohms c. Output voltage—1.1 volts ±20% peak-to-peak (terminated in 100 ohms) d. Rise and fall times—40 ns maximum (terminated in 100 ohms) e. Bit rate—56 kb/s	a. Signal output—Bipolar return to zero b. Output impedance—135 ohms c. Output voltage—Binary one: ±1.4 to 2.1 volts (terminated in 135 ohms). Binary zero: ±0.14 volt maximum d. Pulse width—50% ±2.5% of bit interval e. Rise and fall times—Not to exceed 5% of bit interval f. Bit rates—Up 56 kb/s
Balanced Terminator		a. Signal input—Bipolar nonreturn to zero b. Input impedance—100 ohms c. Input voltage—1.1volts peak-to-peak d. Rise and fall times—40 μs maximum e. Bit rate—56 kb/s	a. Signal input—Bipolar return to zero b. Input impedance—135 ohms c. Input voltage—Binary one: ± 1.05 volts minimum, Binary zero: ± 0.35 volt maximum d. Pulse width—45% to 90% of bit interval e. Rise and fall times—Not to exceed 5% of bit interval f. Bit rates—Up to 56 kb/s

◗TABLE J◖

CROSS-CONNECTIONS MADE BY 921A DTS

TEST CODE*	DATA SET	LEAD NAMES	LEAD CODES X-Y(Z) FROM TABLE K
30	ALL	RS-A, RS-S1, DTR-S2, CS-B	05-03, 05-09, 16-10, 06-04
31	ALL	RS-A, RS-S1, DTR-S2, RLSD-B	05-03, 05-09, 16-10, 08-04
32	ALL	RS-A, RS-S1, DTR-S2, SQD-B	05-03, 05-09, 16-10, 17-04
36	ALL	RS-S1	05-09
37	ALL	DTR-S2	16-10
39	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, SRLSD-L1	05-09, 16-10, 15-11, 10-05
40	ALL	RS-S1, DTR-S2, RI-L1, DSR-L2	05-09, 16-10, 18-05, 07-06
48	ALL	AS SPECIFIED BY OPERATOR	SEE TABLE K
50[1]	ASYNCHRONOUS	RD-RDB, DTR-S2, RLSD-L2, SCRA-SCRM	02-02, 16-10, 08-06, 22-14
51[1], 52	SYNCHRONOUS	RS-S1, CS-L1, DTR-S2, SD-SDB, SCR-SCRM	05-09, 06-05, 16-10, 01-01 (1), 03-14
51[1], 52	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, CS-L1, SD-SDB, SCRA-SCRM	05-09, 16-10, 15-11, 06-05, 01-01 (1), 22-14
51[1], 52	CSU	SD-SDB, SCRC-SCRM	01-01 (1), 27-14
52[2]	ASYNCHRONOUS	RS-S1, DTR-S2, CS-L1, SD-SDB, STC-SCTM, SCRA-SCRM	05-09, 16-10, 06-05, 01-01 (1), 22-14
53	SYNCHRONOUS	RS-S1, DTR-S2, RD-RDB, SD-SDP, STC-SCTM, SCR-SCRM	05-09, 16-10, 02-02, 01-01 (0), 03-14
54	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, RD-RDB, SD-SDP, SCT-SCTM, SCRA-SCRM	05-09, 16-10, 15-11, 02-02, 01-01 (0), 22-14
55	CSU	RD-RDB, SD-SDP, STC-SCTM, SCRC-SCRM	02-02, 01-01 (0), 27-14
57	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, CS-L1, SD-SDB, RD-RDB, STC-SCTM, SCRA-SCRM	05-09, 16-10, 15-11, 06-05, 01-01 (1), 02-02, 22-14

◗ TABLE J (Contd) ◖

CROSS-CONNECTIONS MADE BY 921A DTS

TEST CODE*	DATA SET	LEAD NAMES	LEAD CODES X-Y (Z) FROM TABLE K
58[3]	SYNCHRONOUS	RS-S1, CS-L1, DTR-S2, SD-SDB, SCR-SCRM, RLSD-L2	05-09, 06-05, 16-10, 01-01 (1), 03-14, 08-06
58[3]	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, CS-L1, SD-SDB, SCRA-SCRM, RLSD-L2	05-09, 16-10, 15-11, 06-05, 01-01 (1), 22-14, 08-06
62, 63, 64, 65	CSU	RD-RDB, SD-SDB, STC-SCTM, SCRC-SCRM	02-02 , 01-01 (1), 27-14
67, 68, 70, 71	SYNCHRONOUS	RS-S1, DTR-S2, RD-RDB, SD-SDB, STC-SCTM, SCR-SCTM, RLSDL-L1	05-09, 16-10, 02-02, 01-01 (1), 03-14, 08-05
78	CSU	RD-RDB, SRS-L1, SRS-S1	02-02, 09-05, 09-09
79	ASYNCHRONOUS	RS-S1, DTR-S2, SRS-S3, RD-RDB, SD-SDP, SCRA-SCRM, STC-SCTM	05-09, 16-10, 15-11, 02-02, 01-01 (0), 22-14

1: Versions 2 and 3.

2: Version 1.

3: Limited terminal testing.

* Tests not listed here do not affect cross-connections.

The count-down feature is used for timed tests such as bit errors or start-stop distortion. It is also used in timed transmissions during a start-up test. The interval timer has an accuracy of ±1 percent with a resolution of 10 μsec. The frequency counter has an accuracy of ±1 Hz between 0 and 10,000 Hz and ±10 Hz up to 65,535 Hz.

3.23 The audio circuit allows for the following.

- Establish an audio path on 4-wire private line (non-DDS).
- Transmit 1004- or 2713-Hz tone at 0 dBm over the telephone line.
- Monitor data or voice on a speaker.
- Access T and R for TNS test provided in Versions 2 and 3.

A telephone adapter and cables are provided with the DTS and must be used to obtain access to the line [central office (CO)] side of the data set (Fig. 11).

3.24 Two switches on the front panel control the line operations. During normal data set testing or when monitoring data on the speaker, the TALK/DATA switch must be in the DATA position and the SPKR JACKS/RCV LINE switch must be in the RCV LINE position. When the TALK/DATA switch is in the TALK position, it allows a 1013 handset to operate for voice communications provided test code 25 has been

entered. When it is in the TALK position, the switch allows an internal tone generator to transmit tones (1004 or 2713 Hz) on the line provided that test code 26 or 27 has been entered. When the SPKR JACKS/RCV LINE switch is in the SPKR JACKS position (regardless of the position of the other switch), the speaker-jacks are connected to the speaker to allow an external signal to be monitored (Fig. 12). A volume control is also provided for the speaker.

3.25 The multimeter can be configured by the processor as an ohmmeter or ac or dc voltmeter. The ranges are: 10 ohms to 1 megohm for the ohmmeter, -50 dBm to +10 dBm (referenced to 600 ohms) for the ac voltmeter, and ±94 mV to ±100 volts for the dc voltmeter. It is autoranging and has autopolarity for all functions. Terminating plugs of 135, 600, and 900 ohms are provided with the DTS. These plugs terminate the line for ac voltage measurements and are inserted into the METER ±jack inputs [Fig. 8 (16)].

3.26 Table L gives the electrical specifications for the measurement hardware.

MICROCOMPUTER

3.27 CP1 of the DTS is a general purpose microcomputer designed around an Intel 8080A (an 8-bit microprocessor integrated circuit). It contains 14K bytes of ROM used for program storage and 1K bytes of random access memory (RAM) used as buffer and scratch pad. It has interrupt facilities (keys RST, TST, and GO) and a direct memory access circuit for the isochronous distortion measurement. Versions 2 and 3 provide 32K bytes of additional ROM storage on CP11.

3.28 An input/output structure allows for passing data from the measurement hardware to the microcomputer and for the microcomputer to control and configure the measurement hardware. A separate crystal clock is used to drive the central processor unit (CPU) and the memory.

4. DESCRIPTION OF DTS OPERATION AND TESTS

DTS OPERATION

4.01 Paragraphs 4.02 through 4.18 describe the DTS set-up procedures and operation. A flowchart (Fig. 13) is used to explain overall DTS operation.

4.02 After the DTS is suitably connected for data set testing, insert the proper interface module and place the locking lever in the closed position. Place POWER switch in the ON position and press RST key.

> ***Caution: In Version 1, the locking lever must be placed in the open (horizontal) position; in Versions 2 and 3 the locking lever must be in the vertical position before attempting to remove module or damage to contacts will result.***

Disregard any characters or messages displayed prior to pressing RST. After pressing RST, the DTS version number (eg, 921A VERS #03) is displayed. At this time, the automatic self-tests are performed. (Refer to paragraph 4.11 if diagnostic messages are displayed.) Upon successful completion of the self-tests, the message DATA SET: appears. The appropriate 2-digit data set code (Table A) is entered at this time.

> ***Note 1:*** The back arrow (←) key can be used to delete or change a data set code before the GO key is pressed.

> ***Note 2:*** If no module is used or the wrong interface module is inserted into the DTS and the data set code is entered, the message WRONG INTERFACE appears on the display and is flashed twice.

> ***Note 3:*** If a data set code not listed in Table A is entered, the message NOT AVAILABLE appears on the display and is flashed twice.

4.03 Press the GO key after which the message BIT RATE: appears. The appropriate 2-digit code (Table B) is entered at this time.

> ***Note 1:*** The ← key can be used to delete or change a bit rate code before the GO key is pressed.

> ***Note 2:*** If a bit rate code not listed in Table B is entered, the message NOT AVAILABLE appears on the display and is flashed twice.

TABLE K

PROGRAMMABLE CROSS-CONNECTIONS (TEST CODE 48)

SIGNAL NAME	INTERFACE SIGNALS						LEAD NAME	INTERNAL FUNCTIONS															
	CCITT V.35		CSU	550	EIA RS-232-C			DATA			CTR/TMR INPUT		ASSIGNABLE LEDS				ASSIGNABLE SWITCHES				CLOCK	
								← SDP	← SDB	→ RDB	→ A	→ B	→ L1	→ L2	→ L3	→ L4	← S1	← S2	← S3	← S4	→ SCTM	→ SCRM
	DESIG	PIN	DESIG	PIN	DESIG	PIN	X \ Y	Z=0 01	Z=1 02		03	04	05	06	07	08	09	10	11	12	13	14
Send Data	SD	P,S	SD	5,6	SD	2	01	√	√		√	√										
Receive Data	RD	R,T	RD	3,4	RD	3	02			√	√	√	√	√	√	√						
Serial Clock Receive	SCR	V,X			SCR	17	03				√											√
Serial Clock Transmit	SCT	Y,a			SCT	15	04				√										√	
Request to Send	RS	C			RS	4	05				√	√					√	√	√	√		
Clear to Send	CS	D			CS	5	06				√	√	√	√	√	√						
Data Set Ready (Status Indicator)	DSR	E	SI	2	DSR	6	07				√	√	√	√	√	√						
Receive Line Signal Detect	RLSD	F			RLSD	8	08				√	√	√	√	√	√						
Equalizer Mode					QM	11	09	√	√		√	√	√	√	√	√	√	√	√	√		
Secondary Request to Send					SRS		09	√	√		√	√	√	√	√	√	√	√	√	√		
Supervisory Send Data					SSD		09	√	√		√	√	√	√	√	√	√	√	√	√		
Local Loop	LL	K			LL		09	√	√		√	√	√	√	√	√	√	√	√	√		
Supervisory Receive Data					SRD	12	10			√	√	√	√	√	√	√						
Secondary Receive Line Signal Detect					SRLSD		10			√	√	√	√	√	√	√						
Secondary Clear to Send					SCS	13	11				√	√	√	√	√	√						
New Sync					NS	14	12	√	√		√	√					√	√	√	√		
Secondary Send Data					SSD		12	√	√		√	√					√	√	√	√		
Secondary Receive Data					SRD	16	13			√	√	√	√	√	√	√						
Dibit Clock Transmit					DCT		13			√	√	√	√	√	√	√						
Dibit Clock Receive					DCR	18	14				√	√	√	√	√	√						
Secondary Request to Send					SRS	19	15				√	√					√	√	√	√		
Data Terminal Ready	DTR	H			DTR	20	16				√	√					√	√	√	√		
Signal Quality Detector					SQD	21	17					√	√	√	√	√	√	√	√	√		
Ready					RDY		17					√	√	√	√	√	√	√	√	√		
Ring Indicator	RI	J			RI	22	18					√	√	√	√	√						
Data Signal Rate Selector					DSRS	23	19				√		√	√	√	√	√	√	√	√		
Ring Indicator #2					RI2		19				√		√	√	√	√	√	√	√	√		
Serial Clock Transmit — External					SCTE	24	20				√											
Carrier Detector Reset					CDR	25	21				√						√	√	√	√		
In Service	IS	n			IS		21				√						√	√	√	√		
Analog Loopback/Make Busy					AL/MB		21				√						√	√	√	√		
Test Mode					TM		21				√						√	√	√	√		
Serial Clock Receive Asynchronous	INTERNAL SIGNALS				SCRA	22				√											√	
Serial Transmit Clock					STC	23				√											√	
Test Clock					TCLK	24			√	√	√	√	√	√	√	√						
Word Sync					WDS	25				√												
Extended Hundred Times Clock					EHND	26				√												
Serial Clock Receive CSU					SCRC	27																√

NOTE 1: ARROWS INDICATE SIGNAL FLOW
i.e. ← = TO DCE, → = FROM DCE.

NOTE 2: TEST CIRCUIT MNEMONICS MEAN THE FOLLOWING:

MNEMONIC	MEANING
SDP	PSEUDORANDOM SEND DATA
SDB	BUFFER SEND DATA
RDB	BUFFERED RCV DATA
A	CTR/TMR INPUT A
B	CTR/TMR INPUT B
L1-L4	ASSIGNABLE LEDS 1 THRU 4
S1-S4	ASSIGNABLE SWITCHES 1 THRU 4
SCTM	MULTIPLEXED TRMT CLOCK
SCRM	MULTIPLEXED RCV CLOCK

NOTE 3: CONNECTIONS TO SCTM AND SCRM ARE SPECIFIED IN PAIRS AS FOLLOWS:

03,14 → 04,13 23,13 → 22,14
04,13 → 03,14 24,13 → 27,14
22,14 → 23,13 27,14 → 23,13

NOTE 4: CONNECTIONS TO SDP, SDB AND RDB ARE SPECIFIED IN PAIRS AS FOLLOWS:

01,01(0) → 02,02
01,01(1) → 02,02
02,02 → 01,01(0)

NOTE 5: INTERNAL CONNECTION TO THE EVENT AND FREQUENCY COUNTERS IS MADE VIA CTR/TMR INPUT A.

NOTE 6: PROGRAMMABLE CROSS — CONNECTIONS OVERRIDE AUTOMATIC CONNECTIONS.

NOTE 7: PRIOR TO MAKING PROGRAMMABLE CONNECTIONS ALL PREVIOUS CONNECTIONS SHOULD BE OPENED USING TEST CODE 47.

NOTE 8: THE CORRELATION BETWEEN NUMBERS AND LETTERS ASSIGNED TO INTERFACE MODULE PINS IS AS FOLLOWS:

1 — A	10 — L	19 — W	28 — g
2 — B	11 — M	20 — X	29 — h
3 — C	12 — N	21 — Y	30 — i
4 — D	13 — P	22 — Z	31 — j
5 — E	14 — R	23 — a	32 — k
6 — F	15 — S	24 — b	33 — m
7 — H	16 — T	25 — c	34 — n
8 — J	17 — U	26 — d	
9 — K	18 — V	27 — f	

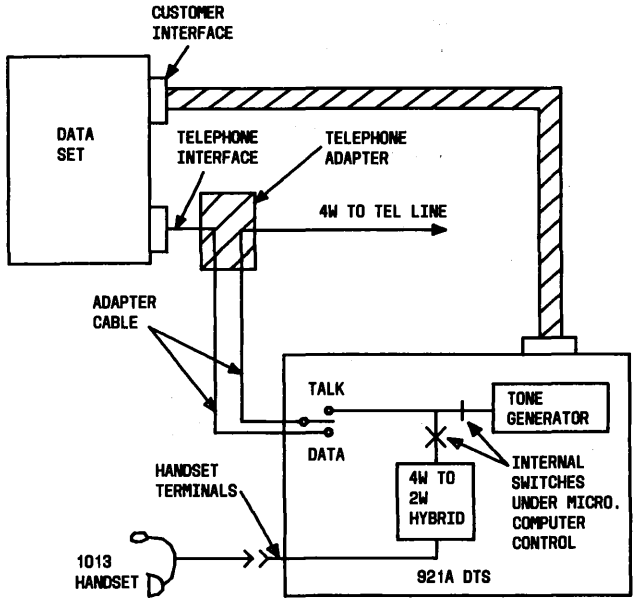


Fig. 11—TALK/DATA Switch—Functional Schematic

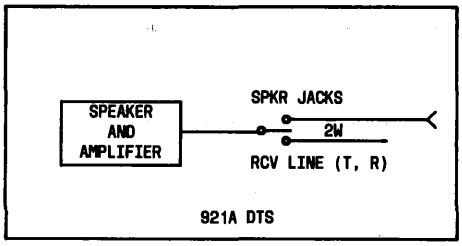


Fig. 12—SPKR JACKS/RCV LINE Switch

4.04 Press the GO key after which the message TEST SEQ: appears. At this time, the DTS will accept one or more 2-digit test codes (Table C).

> ***Note 1:*** The ← key can be used to delete the test codes entered one by one starting with the last code entered.
>
> ***Note 2:*** If a test code not listed in Table C is entered, the message NOT AVAILABLE appears on the display and is flashed twice after which a colon (:) is displayed indicating that additional test codes may be entered.

When the display is full, the DTS provides a new line indicated by : at which time additional test codes may be entered. Some test codes require additional information which must be entered after the test code. After inserting the test codes and necessary information, the GO key is pressed and the test sequence is initiated.

4.05 Some tests require further information which must be entered after the sequence begins but before the test has started. Messages displayed during each test are explained in the paragraphs that follow.

4.06 Each test is performed in the sequence entered. Those tests which self-complete are indicated by the TEST COMPLETE message and the next test is initiated automatically. Those tests which do not self-complete require the operator to press GO. The message TEST INTERRUPTED appears and the sequence continues.

4.07 Any test in progress may be interrupted by pressing the GO key. This causes the TEST INTERRUPTED message to appear after which testing resumes if additional tests have been entered. If the last, or only, test has been interrupted, the TEST SEQ: message appears.

4.08 Pressing the TST key at any time cancels all remaining tests and the TEST SEQ: message appears. This allows the operator to change the test sequence without affecting the data set or bit rate codes previously entered.

4.09 Pressing the RST key at any time cancels all the information previously entered, reinitiates the automatic self-test, and causes the DATA SET: message to appear.

4.10 In addition, the ← key shortens the display duration of timed messages. Table D summarizes the functions of the four control keys.

4.11 During the sequence of automatic self-tests performed at system reset (RST key pressed), the following diagnostic messages may appear:

Diagnostic Message

RAM TEST FAILED

ROM TEST FAILED F=PROCEED

ROM ORDER TEST FAILED F=PROCEED

921A VERS #XX* (XX is DTS version)

TABLE L

ELECTRICAL SPECIFICATION—MEASUREMENT HARDWARE

MULTIMETER SPECIFICATIONS	
OHMMETER	Input Range: 10 ohms to 1 megohm Accuracy: (±8% of input + 4 counts), 10 to 20 ohms; (±4% of input + 4 counts), 20 ohms to 1 megohm Maximum Input: ±50 Vdc
AC VOLT-METER	Frequency Range: 100 Hz to 10 kHz Input Range: 2.4 mV to 2.45V rms (−50 dBm to +10 dBm @600 ohms) Accuracy: −40 to +10 dBm (600 ohms) ±1 dBm −50 to −40 dBm (600 ohms) ±3 dBm Maximum Input: 110V rms
DC VOLT-METER	Input Range: ±94 mV to ±100 Vdc Accuracy: (±2% of input + 4 counts) Maximum Input: ±150 V
CLOCK SPECIFICATIONS	
BIT RATES	110, 150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, 2400, 4800, 7200, 9600, 19,200, 56,000
TRANSMIT CLOCK STABILITY	±25 Parts Per Million
COUNTER/TIMER SPECIFICATIONS	
CTR/TMR JACKS	Input Range: 24.5 mV rms (−30 dBm @600 ohms) to 110V rms Input Resistance: 40 kohms
FREQUENCY COUNTER	Range: DC to 65,535 Accuracy: ±1 Hz;$0 < f < 10{,}000$ Hz ±10 Hz;$10{,}000 < f < 65{,}530$ Hz
INTERVAL TIMER	Range: 10 μs to 99990 seconds Accuracy: ±1 count Resolution: 10 μs
EVENT COUNTER	Range: DC to 50 kb/s
AUDIO AND TONES SPECIFICATIONS	
SPKR JACKS	Input Range: 110V rms maximum Input Resistance: 20 kohms
1004 Hz TONE	0 dBm ± 1 dBm @600 ohms
2713 Hz TONE	0 dBm ± 1 dBm @600 ohms
ISOCHRONOUS DISTORTION	
	Accuracy of +3 counts on all measurements, all bit rates
START-STOP DISTORTION	
BIT RATES (b/s)	110 150 300 600 1000 1200 1400* 1600* 1800 2400* 4800*
MAX ERROR (percent)	+1 +1 +1 +3 −1 −2 +4 −5 +3 +7 +7
	*Start-stop distortion measurements not recommended at these rates.
OUTPUT TEST POINTS	
ERRORS RCV CLOCK TRMT CLOCK RCV DATA SEND DATA	Output Impedance: 1 kohm Output Voltage: 0.4V min to 4.5V max Output Drive Current: 8 mA max

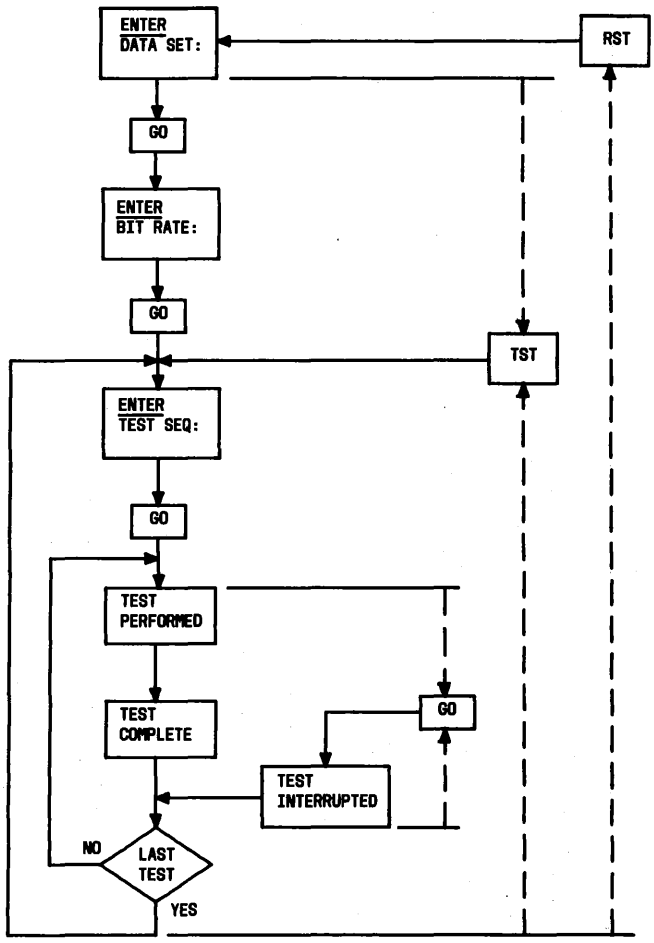


Fig. 13—Operational Flowchart

SW NET. TEST FAILED F=PROCEED

TIMER TEST FAILED F=PROCEED

CLOCK TEST FAILED F=PROCEED

ISO DIST TEST FAILED F=PROCEED

STRT-STP TEST FAILED F=PROCEED

BUFFER TEST FAILED F=PROCEED

921A VERS #XX (lockup condition, where XX is the particular DTS version number).

4.12 If the RAM test fails, the DTS cannot be used for any test.

4.13 If a ROM test fails, it could be indicative of the following problems:

- ROM missing from socket
- ROM improperly plugged in socket
- ROM defective.

(a) A ROM order test failure indicates the ROMs are not plugged into their proper IC sockets.

(b) See paragraph 4.21.

4.14 A switch network (cross-connect network) failure may be caused by one or more inaccessible paths through the network and may cause other functions such as clock, timer, and start-stop tests to fail as well.

4.15 Timer and clock failures are serious failures that could prevent most data set testing.

4.16 Isochronous distortion, start-stop circuit, or 921A VERS #XX lockup failures will not affect other functions.

4.17 A BUFFER failure affects most synchronous or asynchronous transmit and receive data functions.

4.18 Anytime an "F=PROCEED" failure message appears, pressing the F key allows the DTS to continue the self-tests after which the DTS may be used for those tests still operable. In case of a 921A VERS #XX lockup condition, pressing RST and TST keys simultaneously will bypass this failure. Refer to the section entitled 921A DTS—Maintenance (107-402-500) for detailed diagnostic information.

DESCRIPTION OF TESTS

4.19 Each available test is identified by a 2-digit code (Table C). The tests have been grouped according to their function into thirteen categories. Each test is described in detail in the following paragraphs in the order they appear in Table C.

Note: When performing tests that require cross-connections (Table J), the 921A automatically opens all paths previously set up through the cross-connect network and establishes the new connections. In a Version 1 DTS, this may result in a DDD call drop by data sets which

are particularly sensitive to interface lead DTR changes. To avoid this, jumper DTR high by using the data set +12 volts and the DTS interface jacks and switches. This situation is corrected in Versions 2 and 3.

A. Utility Displays

4.20 Utility displays are included as aids for the DTS operator. They provide assistance by displaying previously entered or displayed information. The information is displayed for approximately 7 seconds, and then the next test is executed.

Test Code 00—Version Number

4.21 The most recent version number will be displayed. The version number is determined by the set of ROMs within the DTS. Example: enter 00, press GO; for Version 1, the display will read 921A VERS #01.

> ***Note:*** If an asterisk (*) appears next to the version number, it indicates a compatibility problem with the set of ROMs. Either they are plugged in incorrectly, one or more ROMs are missing, or they are not all compatible with the version number displayed. If they are plugged in incorrectly or any are missing, the ROM self-test or ROM order test or both will fail.

Test Code 01—Data Set Code

4.22 This code is used to remind the operator which data set code, if any, was initially specified. Example: enter 01, press GO, and if a 202C data set were selected (code 20 from Table A), the display will read DATA SET: 20.

Test Code 02—Bit Rate Code

4.23 This code is used to remind the operator what bit rate, if any, was initially specified. Example: enter 02, press GO, and if 2400 b/s were specified (code 24 from Table B), the display will read BIT RATE: 24.

Test Code 03—Test Codes Selected

4.24 This displays all of the test codes selected (Table C) before or after entering 03. For those tests which have additional information entered at the time the test code was specified, such information is also displayed in parentheses next to the test code. Test code 03 may be entered anywhere in a string of test codes, but will only be acted upon after the DTS has sequentially performed all tests preceding it. Example: enter 00, 01, 02, 03, 47, press GO. After tests 00, 01, 02 are executed in sequence, test code 03 is executed by displaying :00 01 02 03 47.

Test Code 04—Test Codes Remaining

4.25 This displays all the test codes, if any, entered after test code 04. For those tests which have additional information entered at the time the test code was specified, such information is also displayed in parentheses next to the test code. Test code 04 may be entered anywhere in a string of test codes, but will only be acted upon after the DTS has sequentially performed all tests preceding it. The most useful way of employing test code 04 is to alternate 04 with a sequence of test codes such as :00 04 01 04 02 04 47. In this example, after test code 00 is executed the display will show :01 04 02 04 47. After test code 01 is executed the display will show :02 04 47 as the remaining tests, etc. This is used as an aid to remind the operator as to what step in a sequence the DTS has progressed.

B. Utility Routines

Test Code 08—Set Message Display Time Versions 2 and 3

4.26 This test allows the DTS operator to select the time duration for the display of timed messages. If test code 08 is not used, timed messages will be displayed for 2.3 seconds. When 08 is entered the message :08 MESSAGE DELAY = ?.? SECONDS is displayed. The operator then enters two digits which will determine the time duration (0.0 to 9.9 seconds) of displayed messages during subsequent tests. This test is most useful to an experienced DTS operator who wants to shorten the time duration of displayed messages.

> ***Example:*** After 08 is entered and the above message is displayed, the operator presses 12. This causes the display time of subsequent messages to be set to 1.2 seconds.

C. General Purpose

4.27 These functions may be performed with or without a data set connected to the DTS. The multimeter functions (ohms, ac volts, dc volts) may be performed only on leads connected to the METER +,- input jacks [Fig. 8 (4), (16)].

4.28 If multimeter measurements for particular interface signals are required, jumper wires (located in the DTS cover) are connected between the interface lead jacks [Fig. 8 (2), (10)] and the METER +,- jacks [Fig. 8 (4)].

4.29 If multimeter measurements for external equipment are required, leads are connected from the external equipment to the METER +,- terminals [Fig. 8 (16)].

Test Code 10—Multimeter—Ohms

4.30 This is an autoranging ohmmeter. Resistance readings are in the range from 10 ohms to 1 megohm.

> ***Note:*** The resistance to be measured must be floating with respect to ground.

To select the ohmmeter, enter test code 10 and press GO. A resistance greater than 1 megohm or an open circuit will result in an OVER 1 MEGOHM display. A resistance under 10 ohms will result in an UNDER 10 OHMS display. Other readings are displayed either in OHMS or KOHMS, as appropriate. VOLTAGE ON LEADS will be displayed if this condition exists. To terminate measurement, press GO.

> ***Note:*** When measuring a capacitive load (such as an open circuited line pair) greater than 0.01 μf, the display may indicate VOLTAGE ON LEADS or some random reading.

Test Code 11—Multimeter—AC Volts

4.31 Autoranging ac voltage readings can be made in the range from 2.4 mV to 2.45V. A signal level (in dBm) is also displayed along with the ac readings and is calculated based on operator specified terminations (135, 600, or 900 ohms). For the 600-ohm case, the range is -50 to +10 dBm. Terminating resistors of 135, 600, and 900 ohms are provided for terminating the line. They are inserted in the METER +,- jacks [Fig. 8 (16)]. A high-impedance termination may also be specified, resulting in an ac volt reading without the dBm portion. To select the ac voltmeter, enter test code 11 and press GO. The display reads :11 R = ? 1=135 6=600 9=900 0=N, with N (none) representing no termination. Select the appropriate impedance for the equipment under test (also ensure that the DTS is terminated accordingly) and press GO. Readings greater than 2.45 Vac will result in a message OVER 2.45 VAC. Reading less than 2.4 mV ac will result in a message UNDER 2.4 MV AC. To terminate measurement, press GO.

Test Code 12—Multimeter—DC Volts

4.32 The dc voltmeter is autoranging and has autopolarity. Dc voltage readings are in the range from 94 mV to 100V. To select the dc voltmeter, enter test code 12 and press GO. Readings greater than 100 Vdc will result in a message OVER 100 VDC. Readings less than 94 mV dc will result in the message UNDER 94 MV DC. To terminate voltmeter measurement, press GO.

> ***Note:*** When measuring a dc voltage, a fast change in this voltage (less than 10 ms) to the opposite polarity may cause the display to lock up to the previous reading. This only occurs when the magnitudes of the two levels are approximately the same. If lockup occurs, manually open and then close one of the meter inputs to restore the display.

Test Code 15—Event Counter—Internal

4.33 The event counter counts events up to a 50-kHz rate on selected interface leads. The interface signals are routed through the programmable cross-connect network to the counter/timer circuit. Positive- or negative-going transitions (with reference to EIA signal ground) may be specified. The selection of the particular lead for internal event counting is made via the programmable cross-connect network (test code 48) (Table K). The signal to be examined must be routed to input A of the CTR/TMR. To do this, bring the DTS to the TEST SEQ: display. Enter test code 47 (opens all connections), 48, and 15. The prompting message : 15 TRG=? (0-NEG,1=POS) will appear. Enter 1 if positive-going transitions are to be counted, or 0 for negative-going transitions, and press GO. Test code 48 requests the necessary cross-connections

(X=?? Y=??). Use Table K to select the code corresponding to the desired signal under column X. For example, CS corresponds to code 06. Enter 06 for the value of X and enter 03 (counter input A) for the value of Y. Press GO to start event counting. Event counts are displayed from 0000 to 9999. A count greater than 9999 will result in an overflow (OVF) message while the counting continues. To clear the display and restart the counter, press A. To terminate the counter, press GO.

Test Code 16—Event Counter—External

4.34 An externally provided signal is applied across the trigger (TRG) and common (COM) inputs of the CTR/TMR [Fig. 8 (6), (16)]. Events are recorded for signal frequencies up to 50 kHz and for signal levels down to -30 dBm (referenced to 600 ohms). To allow counting of events at a slow rate, a dc coupled mode is automatically selected by the DTS. Therefore, an event will only be counted when the signal on the TRG input swings through the reference level of the COM input. Enter test code 16 and the prompting message :16 TRG=? (0=NEG,1=POS) appears. Enter 1 if positive-going transistions (on the TRG input) are to be counted, or 0 for negative-going transitions. Press GO to start event counting. To clear the display and restart the counter, press A. To terminate the count, press GO.

Test Code 17—Frequency Counter—Internal

4.35 This measures and displays the frequency of internal signals up to 65 kHz. The signals are routed to the frequency counter through the programmable cross-connect network. The selection of the particular lead for internal frequency counting is made via the programmable cross-connect network (test code 48) using Table K. The signal to be examined must be routed to the counter/timer input A. To do this, enter 47 48 17 and press GO. Test code 48 will request the necessary cross-connections (X=?? Y=??). Select the code corresponding to the desired signal under Column X of Table K; for example, SCT corresponds to code 04. Enter 03 (timer input A) for Y. Now press GO to start measuring frequency. The display will appear as FREQ=XXXX HZ if the frequency of the signal is less than 10,000 Hz. If the frequency is greater than 10,000 Hz, the display will show FREQ = XX.XX KHZ. The test is terminated by pressing GO.

Test Code 18—Frequency Counter—External (AC Coupled)

4.36 The signal to be measured is applied to the CTR/TMR jack inputs. The frequency counter will measure signal frequencies up to 65 kHz and signal levels down to -30 dBm (referenced to 600 ohms). Enter test code 18 and press GO to start measuring frequency. To terminate the test, press GO.

Test Code 19—Frequency Counter—External (DC Coupled)

4.37 The signal to be measured is applied to the CTR/TMR jack inputs. The frequency counter will measure signal frequencies up to 65 kHz and signal levels down to -30 dBm (referenced to 600 ohms). For counting to occur, the signal on the TRG input must swing through the reference level of COM input. Enter test code 19 and press GO to start measuring frequency. To terminate the test, press GO.

Test Code 20—Interval Timer—Internal (A or B First)

4.38 This provides for measurement of elapsed time between two signal occurrences and pulse width of a single signal appearing on an interface lead (Fig. 14). For period measurements on a single interface lead, refer to test code 21. Time intervals from 0.01 ms to 99,990 seconds (27 hours, 46 minutes) may be measured. Signals appearing on interface leads may be selected for measurement and are routed to the timer inputs A and B via the programmable cross-connect network (test code 48 and Table K).

> ***Note:*** Interval measurements cannot be performed when the DTS is in the monitor mode if one of the interface leads is a driver.

When measuring the interval between two signals, one signal must be routed to timer input A and the other to timer input B. In the "A or B First" mode, the timer will start when the preselected signal first appears on either A or B, regardless of which occurs first. An indication of which signal occurred first, and the results, is given on the display after the second transition occurs. If the second transition does not occur, the result portion of the display remains blank. Selection of the transition sense is made immediately after entering

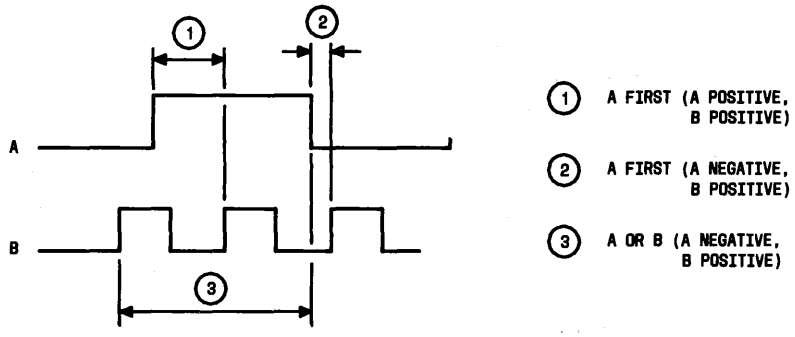


Fig. 14—Example of Internal Interval Timer

test code 20. The DTS displays the message : 20 A=? B=? (0=NEG,1=POS). Specifying, for example, A=1 B=1 will cause the timer to start on the positive transition of the first signal occurrence and stop on the positive transition of the other signal. Repeating the measurement is done by pressing A. The test is terminated by pressing GO.

> ***Example:*** Measure the time interval between CS and RLSD (assume the DTS is bridged on line). Enter 47 48 20 47. The message :20 A=? B=? (0=NEG, 1=POS) will appear. Enter 11 to make A=1 B=1. Press GO. Test 47 self-completes after which test 48 requests the necessary cross-connections X=?? Y=??. Using Table K, Column X, select and enter code 06 for CS. Using row Y, select and enter 03 for timer input A. When the question marks (??) reappear, enter 08 for X (RLSD) and 04 for Y (timer input B). Press GO. Test 48 is interrupted and test 20 begins. After CS goes ***on***, the timer monitors for RLSD to go ***on*** and then displays the results. If these conditions do not occur, the result portion of the display remains blank. To terminate, press GO. Test 47 self-completes.

Test Code 21—Interval Timer—Internal (A First)

4.39 This test accomplishes the same function as test code 20 and provides for measurement of elapsed time between two signal occurrences and period or pulse width of a single signal appearing on an interface lead (Fig. 14).

> ***Note:*** Interval measurements cannot be performed when the DTS is in the monitor mode if one of the interface leads is a driver.

When measuring the interval between two signals, one signal must be routed to timer input A and the other to timer input B. When measuring the period or pulse width of a single signal, such signal must be routed to both timer inputs A and B. In the "A First" mode, the timer starts only when the first transition occurs on the lead connected to input A. The results become available after the transition on input B occurs. If the B transition does not occur, the result portion of the display remains blank. Selection of the transition sense is made immediately after entering test code 21. The DTS displays the message : 21 A=? B=? (0=NEG,1=POS). Specifying, for example, A=1 B=1 will cause the timer to start on the positive transition of signal A and stop on the positive transition of signal B. Repeating the measurement is done by pressing A. The test is terminated by pressing GO.

> ***Example:*** To determine the turnaround time in a polled network, measure the interval when CS goes ***off*** until RLSD goes ***on***. The DTS must be bridged on line. Enter 47 48 21 47. The message :21 A=? B=? (0=NEG, 1=POS) will appear. Enter 0 1 to make A=0 B=1. Press GO. Test 47 self-completes after which test 48 requests the necessary cross-connection X=?? Y=??. Using Table K, Column X, select and enter code 06 for CS. Using row Y, select and enter 03 for timer input A. When the question marks (??) reappear, enter 08 for X (RLSD) and 04 for Y (timer input B). Press GO. Test 48 is interrupted and 21 begins. After CS goes

off, the timer monitors for RLSD to go *on* and then displays the results. If these conditions do not occur, the result portion of the display remains blank. To terminate, press GO. Test 47 self-completes.

Test Code 22—Interval Timer—External

4.40 In external mode, only the period or pulse width of a single signal can be measured (Fig. 15). The signal must be applied to the CTR/TMR jack input (TRG and COM). For triggering to occur, the signal on the TRG input must swing through the reference level of the COM input. Positive- or negative-going transitions may be selected to control the timing cycle. The sense of transitions that trigger and stop the timer are selected with respect to the TRG input and specified immediately after code 22 is entered. The prompting message : 22 TRG=? STP=? (0=NEG,1=POS) appears. Press GO to start. The result portion of the display remains blank until two transitions occur. The measurement may be repeated by pressing A. The test is terminated by pressing GO.

Example: To measure the pulse width of a signal, trigger the timer on the positive transition and stop it on the negative transition (TRG=1 STP=0). To measure the signal period, trigger on positive and stop on positive transition (TRG=1 STP=1).

D. Line Operations

4.41 These functions are independent of the data set under test. They allow for transmission and detection of signals directly on the line side of the data set. Access to T and R terminals is obtained with the telephone adapter and cables provided. The TALK/DATA switch must be in the TALK position for all line operations.

Test Code 25—Talk Link

4.42 This allows communication with the far end on 4-wire private line (non-DDS) facilities only. The telephone line adapter cable (Fig. 3 and 4) is connected to the 9-pin telephone connector on the left side of the DTS. One side of the telephone line adapter is plugged into the 25-pin line connector, the other side is plugged into the data set (Fig. 11). The telephone line adapter is also provided with spade lugs and terminals.

4.43 Set the TALK/DATA switch to the TALK position. This breaks the T and R connection to the data set and routes T and R to the DTS (Fig. 11). Set SPKR-JACKS/RCV LINE switch to the RCV LINE position. This places the speaker inputs across the receiver line T and R (Fig. 12). Connect 1013 telephone handset to the handset terminals [Fig. 8 (26)].

Note: The 921A will not operate if the handset terminals are shorted to each other or to the case.

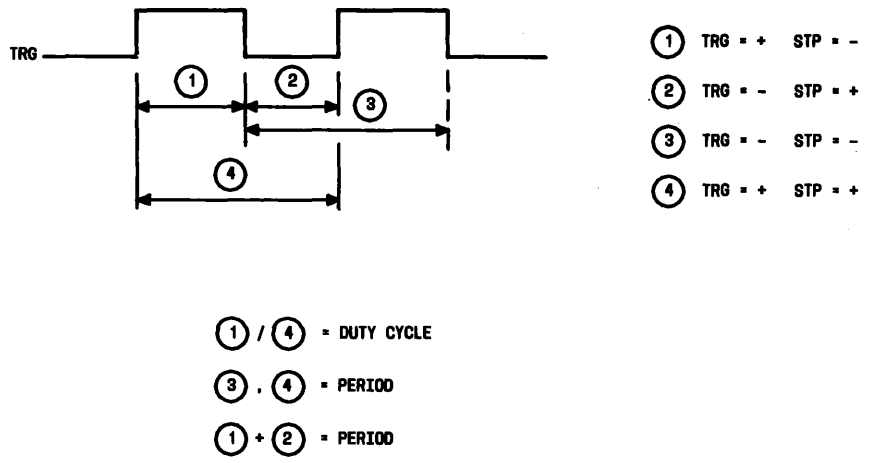


Fig. 15—Example of External Interval Timer

Set the MON/TALK switch of the 1013 handset in the TALK position. Enter test code 25 and press GO. The message TEST COMPLETE will appear indicating internal DTS connections are made and voice communication is established. Received audio will be heard on both the 1013 handset and DTS speaker.

Test Code 26—Transmit 1004 Hz

4.44 This tone is available for performing line loss measurements between the DTS location and the far end. It is transmitted at 0 dBm ±1 dBm. The telephone line adapter cable (Fig. 3 and 4) is connected to the 9-pin telephone connector on the left side of the DTS. One side of the adapter is plugged into the 25-pin line connector, and the other side is plugged into the data set.

4.45 Set the TALK/DATA switch to the TALK position. This breaks the T and R connection to the data set and routes T and R to the DTS (Fig. 11). Set the SPKR-JACKS/RCV LINE switch to the RCV LINE position. This places the speaker inputs across the receive line T and R (Fig. 12). Enter test code 26 and press GO. The message TEST COMPLETE will appear indicating completion of internal DTS setup. The DTS continues to transmit the tone. For a quick audio check, connect the TRMT T and R to the SPKR JACKS by means of jumper wires, move the SPKR-JACKS/RCV LINE switch to SPKR JACKS, and adjust the volume control until the tone is audible on the DTS speaker. Now place the switch back to RCV LINE.

4.46 An application of test code 26 for testing a line circuit with a loopback DAS is given in paragraph 5.02.

Test Code 27—Transmit 2713 Hz

4.47 The 2713 Hz is used to loop back the far-end data auxiliary set (DAS) 829 so that line loss or bit error measurements can be performed. This tone is also transmitted at 0 dBm ±1 dBm. The telephone line adapter cable (Fig. 3 and 4) is connected to the 9-pin telephone connector on the left side of the DTS. One side of the adapter is plugged into the 25-pin line connector, the other side is plugged into the data set.

4.48 Set the TALK/DATA switch to the TALK position. This breaks the T and R connection to the data set and routes T and R to the DTS (Fig. 11). Set the SPKR-JACKS/RCV LINE switch to the RCV LINE position. This places the speaker inputs across the receive line T and R (Fig. 12). Enter test code 27 and press GO. The message TEST COMPLETE will appear indicating completion of internal DTS setup. The DTS continues to transmit the tone on the TRMT T and R terminals. For a quick audio check, connect the TRMT T and R to the SPKR JACKS by means of jumper wires. Set the switch to SPKR JACKS and adjust the volume control until the tone is audible on the DTS speaker. Set the switch back to RCV LINE position.

> ***Note 1:*** By means of jumper wires located in the cover, it is possible to measure the level of the transmitted (or received) signal by patching the TRMT (or RCV) T and R terminals to the METER terminals and using test code 11 (ac voltmeter).
>
> ***Note 2:*** By means of jumper wires located in the cover, it is possible to measure the frequency of the transmitted (or received) signal by patching the TRMT (or RCV) T and R terminals to the CTR/TMR jacks and using test code 18 (frequency counter, external).

4.49 With test code 27 inserted and AUDIO switches in TALK and SPKR JACKS positions, the 2713 Hz is transmitted to the remote DAS. Test codes 26 and 27 may be inserted whenever the DTS is conditioned for TEST SEQ:.

4.50 Applications of test code 27 for testing a line circuit with a loopback DAS is given in paragraphs 5.02 and 5.03.

E. Interface Operations

4.51 The interface operations allow a number of measurements and operations to be performed on interface leads, particularly control signals. This group also includes two functional tests: the reverse channel and automatic answer tests.

Test Code 29—Monitor SD

4.52 In normal operation and whenever TEST SEQ: message appears, the DTS is automatically set up to receive on the RD lead and to transmit on the SD lead. Test code 29, when selected, causes the DTS to receive data on the SD lead. This is useful when the DTS is bridged on-line

and required to look toward the terminal instead of the data set.

> ***Note:*** When the DTS is bridged on-line, all interface module switches should be placed in the MON position.

In Version 1, when test code 29 is entered, the message 29 ? (0=RD, 1=SD) appears. At this time 1 is entered to permit SD to be monitored. Press GO and when the TEST COMPLETE message appears, the DTS is in the monitor SD mode. In Versions 2 and 3 when test code 29 is entered, no other message appears. Other tests which will be performed are then entered. Test code 29 causes the DTS to receive data on the SD lead throughout subsequent tests.

4.53 If the DTS is in the monitor SD mode, it is possible to return to normal (monitor RD). In Version 1, when test code 29 is entered and 0 is selected the DTS will go into the monitor RD mode. In Version 1 or 2 when the TEST SEQ: message appears, the SD and RD leads return to normal. Applications of test code 29 for start-up and isochronous distortion monitoring are given in paragraphs 5.05 and 5.09, respectively.

Test Code 30—RS-CS Interval

4.54 This test measures the interval between the time the request-to-send (RS) lead is turned ***on*** and the clear-to-send lead responds. When test code 30 is entered and the GO key is pressed, the DTS automatically connects RS and CS to the interval timer, turns RS ***on*** and displays the results RS-CS=XXXX MSEC as soon as CS goes ***on***. If CS does not go ***on***, the result portion of the display will remain blank. To make another measurement, press A. The RS lead is turned ***off*** for 1 second, then turned ***on*** again. To terminate the test, press GO.

Test Code 31—RS-RLSD Interval

4.55 This test measures the interval between the time the RS lead is turned ***on*** and the RLSD lead responds. When test code 31 is entered and the GO key pressed, the DTS automatically connects RS and RLSD to the interval timer, turns RS ***on***, and displays the results RS-RLSD=XXXX MSEC as soon as RLSD goes ***on***. If RLSD does not go ***on***, the result portion of the display will remain blank. To make another measurement, press A. The RS lead is turned ***off*** for 1 second, and then turned ***on*** again. To terminate the test, press GO.

Test Code 32—RS-SQD Interval

4.56 This test measures the interval between the time the RS lead is turned ***on*** and the signal-quality detector (SQD, EIA pin 21) lead responds. When test code 32 is entered and the GO key pressed, the DTS automatically connects RS and SQD to the interval timer, turns RS ***on***, and displays the results RS-SQD=XXXX MSEC as soon as SQD goes ***on***. If SQD does not go ***on***, the result portion of the display will remain blank. To make another measurement, press A. The RS lead is turned ***off*** for 1 second, then turned ***on*** again. To terminate the test, press GO.

Test Code 36—Control RS

4.57 This test allows for control of the RS lead. Lead RS may be turned ***on*** or ***off*** by keyboard selection. When test code 36 is entered, the DTS displays the message : 36 RS=? (0 or 1). Enter 1 if RS is to be turned ***on***. Enter 0 if RS is to be turned ***off***. The DTS automatically connects RS to S1 (assignable switch 1) which it then controls as requested. This test is self-completing. The status of RS may be observed on the appropriate interface LED. In Versions 2 and 3, the RS lead is turned ***off*** regardless of its previous state when the DTS returns to the TEST SEQ: message.

Test Code 37—Control DTR

4.58 This test allows for control of the data terminal ready (DTR) lead. Lead DTR may be turned ***on*** or ***off*** by keyboard selection. When test code 37 is entered, the DTS displays the message : 37 DTR=? (0 or 1). Enter 1 if DTR is to be turned ***on***. Enter 0 if DTR is to be turned ***off***. The DTS automatically connects DTR to S2 (assignable switch 2) which it then controls as requested. This test is self-completing. The status of DTR may be observed on the appropriate interface LED.

Test Code 38—Control S1-S4

4.59 This allows the keyboard keys 1, 2, 3, and 4 to function as toggle switches. Key 1 is S1, key 2 is S2, key 3 is S3, and key 4 is S4. Every time one of these keys is pressed, the

corresponding switch is toggled. After entering test code 38 and pressing GO, the DTS displays the current status of these four assignable switches; for example, S1=ON S2=OFF S3=OFF S4=OFF. When a key is pressed (1 through 4), the corresponding switch changes state and its new state is displayed. To make this function effective, these switches must be assigned to control signals. This assignment is made by using test code 48 in conjunction with Table K. To interrupt or terminate this test, press GO. If test codes 36 and 37 are used in sequence, then S1 and S2 should not be assigned. In Versions 2 and 3, when the DTS returns to the TEST SEQ: message, S1 is turned ***off*** regardless of its previous state.

Test Code 39—Reverse Channel

4.60 This is a functional test that exercises the reverse channel option available in some data sets. Both the receive and transmit reverse channel capabilities can be tested. This test must be done in conjunction with a data test center. First, the data test center transmits a reverse channel tone to the data set which acknowledges receipt by turning ***on*** the SRLSD interface lead. This is recognized by the DTS which then turns SRS ***on***, causing the data set to transmit the reverse channel tone back to the data test center where it may be detected. To start the test, enter test code 39 and press GO.

4.61 The DTS will be waiting for SRLSD to go ***on***, indicating that the data set is receiving a reverse channel tone. The message SRLSD IS ON or SRLSD IS OFF is displayed, as appropriate. When the message SRS IS ON appears, pin 19 is high, and the data set should be sending the reverse channel tone toward the data test center. The DTS will remain in this mode until the GO key is pressed.

Test Code 40—Automatic Answer Test

4.62 This is a functional test that exercises the automatic answer option available in some switched network data sets. The test is performed automatically with no user intervention required except for call setup. Test results appear on the display as either TEST PASSED or TEST FAILED.

4.63 At the data set under test, prepare the DTS by entering test code 40 and pressing GO. The display will read WAITING FOR RI. At this time the ring indicator (RI) interface lead of the data set is ***off*** and the DTS is waiting for RI to go ***on*** in response to the detection of ringing by the data set.

4.64 Call the data set under test. When the data set detects ringing, RI goes ***on*** and the DTS indicates RINGING on the display. At this time the state of the RI lead may be observed on assignable LED 1.

4.65 After three or four rings are detected, ◗DTR◖ is turned ***on***. Thirteen seconds later (6.8 seconds later for 212-type data sets), the DTS checks to see whether the data set responded by turning DSR ***on***, at which time the DTS indicates ANSWERED on the display. LED 2 will go ***on*** when DSR goes ***on***.

4.66 After DSR goes ***on***, the DTS turns RS ***on***, thereby allowing the caller to verify that the data set has automatically answered and is in the data mode. The data set turns CS ***on*** in response to RS going ***on***.

4.67 Seven seconds after the display indicates ANSWERED (2.5 seconds after for 212-type data sets), DTR is turned ***off***. After 1 second, the DTS then checks to see whether the data set turns DSR ***off***. At this time CS and LED 2 also go ***off*** and RS remains ***on***.

4.68 The successful completion of paragraphs 4.63 through 4.67 will be indicated by the TEST PASSED message, otherwise the DTS will indicate TEST FAILED. This test is self-terminating in a Version 1 DTS and the DTS indicates TEST COMPLETE when the cycle is ended. For Versions 2 and 3 DTS, if the test fails, the message TEST FAILED will remain on the display until the GO key is pressed.

4.69 This test can fail in two modes: either the data set does not respond to DTR on by turning DSR ***on***, or the data set does not respond to DTR ***off*** by turning DSR ***off***. Either failure can be observed on the interface LEDs.

F. Programmable Clock

4.70 Normally, for tests which require the use of the internal DTS clock, such as nonsynchronous data sets or CSUs, both the bit rate and the clock-operating mode are automatically set by the

DTS. To override the automatic clock settings, test codes 43, 44, and 45 are provided. These test codes allow the operator to have exclusive control over the clock. When testing synchronous data sets with Version 1 sets, the internal clock should be programmed using test code 43 to provide clock to the data sets optioned for external timing. For Versions 2 and 3, test code 43 is not required for data sets with this option. The use of test code 43, 44, or 45 prohibits all test programs from changing any clock settings. Test code 46 must be used when the action taken by 43, 44, or 45 is to be cancelled.

Test Code 43—Free Run—RCV and TRMT

4.71 This allows the transmit clock and the receive clock to operate in a free-run mode, independent of incoming data. This clock mode is used with Version 1 sets when operating with a synchronous data set optioned for external clock or for performing special tests. For Versions 2 and 3, test code 43 is not required for data sets having an external clock option.

4.72 To make use of this mode, enter test code 43 and press GO. The message BIT RATE: will appear. Enter the 2-digit code (Table B) corresponding to the desired speed. Take no further action until the message TEST COMPLETE is displayed.

> ***Note:*** When using the EIA RS-232-C module, clock is available on pin 24 (SCTE) and no special cross-connections are required.

Test Code 44—Phase-Locked—RCV and TRMT

4.73 This allows both the transmit and receive clocks to operate synchronized (phase-locked) to incoming data. This clock mode is normally used for CSU operation. For those tests on CSUs already programmed in the DTS, the clock settings are automatic. Test code 44 should only be used when performing special tests.

> ***Note:*** In addition to setting up the clock mode, the clock signals SCRC and STC must be connected to SCRM and SCTM, respectively. Use test code 48 and Table K. To make use of this mode, enter test code 44 and press GO. The message BIT RATE: will appear. Enter the 2-digit code (Table B) corresponding to the desired speed. Take no further action until the message TEST COMPLETE is displayed.

Test Code 45—Phase-Locked—RCV Only

4.74 This allows the receive clock to operate synchronized to the incoming data while the transmit clock is allowed to free run. This clock mode is normally used for synchronous tests (such as bit error tests) on nonsynchronous data sets (eg, 202-types). For such tests which are already programmed in the DTS, the clock settings are automatic. Test code 45 should only be used when performing special tests.

> ***Note 1:*** In addition to setting up the clock mode, the clock signals SCRA and STC must be connected to SCRM and SCTM, respectively. Use test code 48 and Table K. To make use of this mode, enter test code 45 and press GO. The prompting message TRANSMITTER=? 1=921 2=914 3=903 will appear. This information is necessary for setting up the pull-in range of the receiver phase-locked clock. The appropriate key (1, 2, or 3) must be pressed according to the far-end transmitter test set. If only one DTS is used in a loopback mode, enter 1. The message BIT RATE: will appear next. Enter the 2-digit code (Table B) corresponding to the desired speed. Take no further action until the message TEST COMPLETE is displayed.
>
> ***Note 2:*** Some tests performed with a 903 or 914 as the transmitter ***may*** not operate as a result of a narrow receiver pull-in range setting in the 921A. In the case of the 914, specify the transmitter as 3=903 in order to set up a wider receiver pull-in range. If the test still cannot be performed, the transmitter frequency of the 914 is beyond the widest setting of receiver pull-in range. Versions 2 and 3 of the DTS extend the receiver pull-in range.

Test Code 46—Enable Automatic Clock Settings

4.75 The use of test codes 43, 44, and 45 prohibit succeeding tests from setting up the clock. Test code 46 is provided to cancel this action and allows the DTS to make the usual automatic clock

settings. ▶Enter test code 46 and press GO. The message TEST COMPLETE is displayed.◀

G. Assignable Connections

4.76 This feature allows the operator to have control of the internal cross-connect network in order to bring selected interface signals to the measurement hardware and to the LED status indicators.

Test Code 47—Open

4.77 This opens all existing connections in the cross-connect network. Test code 47 is used in conjunction with test code 48 described in paragraph 4.78. This test is self-completing.

Test Code 48—Assign

4.78 The use of test code 48 allows connection of interface signals to be made to DTS internal functions for special applications. This test overrides any automatic connections which are set up by the DTS. When used, test code 48 prevents all succeeding tests from setting up their prescribed cross-connections. All previous connections are unaffected. Subsequent tests require that connections be made manually. In order to avoid this condition, test code 47 should follow the test code entered after 48. As a result, all manually entered cross-connections are opened, thus permitting subsequent tests to automatically set the required cross-connections. In order to assign cross-connections, enter test code 48, and then press GO. The message SW CONN: X=?? Y=?? appears. Table K lists all valid cross-connections. The table is constructed so interface and internal DTS signals are represented by X, while the internal DTS functions are represented by Y. Cross-connections are entered as pairs of 2-digit codes which replace the ?? in the display. Once the pair of codes is entered, the cross-connection is made and the codes entered disappear leaving the original message with ?? in place of the codes. For certain cross-connections, a third single-digit code represented by Z (also in Table K) is required. The display message indicates when to enter Z by the following type of message SW CONN: X=01 Y=01 Z=?. If an invalid cross-connection is attempted, the message will read NOT AVAILABLE and flash two times. Once all required cross-connections have been made, the GO key is pressed so that the next test may be performed. For special applications or new data sets, when one or more cross-connections are required in addition to the preset connections, use test code 48. In this case, assign the prescribed connections according to Table J, then any additional connections may be added. If the connections are not assigned according to Table J, the test may not work.

> ***Note 1:*** The 921A will recognize test code 48 by the entry of at least one valid X, Y pair.
>
> ***Note 2:*** When setting up connections involving RD-RDB (02-02), SD-SDP(01-01(0)), and SD-SDB (01-01-(1)), the RD-RDB connection should be made first.
>
> ***Note 3:*** For Versions 2 and 3 DTS, if test code 48 is used, the following message will be displayed between subsequent tests: CROSS CONNECTIONS MANUALLY SET.

H. Sequence Generator and Error Tests

4.79 These functions are provided for both synchronous and nonsynchronous data sets. The error tests (Dot, Space, Mark, and pseudorandom 2047-, 511-, 63-bit words) can be performed on all data sets, including DSUs and CSUs. In Version 1 DTS the transmit FOX message and parity tests are included for nonsynchronous data sets only. In Versions 2 and 3, the FOX message may be transmitted in either synchronous or asynchronous format.

Test Code 50—Display RCV Characters (Async)

Versions 2 and 3

4.80 This test will display up to 255 received characters after a selectable sequence of synchronizing characters have been received. The synchronizing characters can be any sequence of expected characters (five maximum) in the received message. The test will function only for asynchronous transmission with a character format consisting of one start bit, eight data bits (including parity), and one or more stop bits. Each received character is displayed as two hex digits. Tables M and N give conversions from hex to ASCII and EBCDIC.

4.81 To display received characters, enter test code 50 and press GO. The message NO.

♦TABLE M♦

CHARACTER TO HEX CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC		
CHAR.	BINARY	HEX	CHAR.	BINARY	HEX	CHAR.	BINARY	HEX
A	01 000 001	41	A	11 000 001	C1	A	11 000 001	C1
B	01 000 010	42	B	11 000 010	C2	B	11 000 010	C2
C	11 000 011	C3	C	01 000 011	43	C	11 000 011	C3
D	01 000 100	44	D	11 000 100	C4	D	11 000 100	C4
E	11 000 101	C5	E	01 000 101	45	E	11 000 101	C5
F	11 000 110	C6	F	01 000 110	46	F	11 000 110	C6
G	01 000 111	47	G	11 000 111	C7	G	11 000 111	C7
H	01 001 000	48	H	11 001 000	C8	H	11 001 000	C8
I	11 001 001	C9	I	01 001 001	49	I	11 001 001	C9
J	11 001 010	CA	J	01 001 010	4A	J	11 010 001	D1
K	01 001 011	4B	K	11 001 011	CB	K	11 010 010	D2
L	11 001 100	CC	L	01 001 100	4C	L	11 010 011	D3
M	01 001 101	4D	M	11 001 101	CD	M	11 010 100	D4
N	01 001 110	4E	N	11 001 110	CE	N	11 010 101	D5
O	11 001 111	CF	O	01 001 111	4F	O	11 010 110	D6
P	01 010 000	50	P	11 010 000	D0	P	11 010 111	D7
Q	11 010 001	D1	Q	01 010 001	51	Q	11 011 000	D8
R	11 010 010	D2	R	01 010 010	52	R	11 011 001	D9
S	01 010 011	53	S	11 010 011	D3	S	11 100 010	E2
T	11 010 100	D4	T	01 010 100	54	T	11 100 011	E3
U	01 010 101	55	U	11 010 101	D5	U	11 100 100	E4
V	01 010 110	56	V	11 010 110	D6	V	11 100 101	E5
W	11 010 111	D7	W	01 010 111	57	W	11 100 110	E6
X	11 011 000	D8	X	11 011 000	58	X	11 100 111	E7
Y	01 011 001	59	Y	11 011 001	D9	Y	11 101 000	E8
Z	01 011 010	5A	Z	11 011 010	DA	Z	11 101 001	E9
a	11 100 001	E1	a	01 100 001	61	a	10 000 001	81
b	11 100 010	E2	b	01 100 010	62	b	10 000 010	82
c	01 100 011	63	c	11 100 011	E3	c	10 000 011	83
d	11 100 100	E4	d	01 100 100	64	d	10 000 100	84
e	01 100 101	65	e	11 100 101	E5	e	10 000 101	85
f	01 100 110	66	f	11 100 110	E6	f	10 000 110	86
g	11 100 111	E7	g	01 100 111	67	g	10 000 111	87
h	11 101 000	E8	h	01 101 000	68	h	10 001 000	88
i	01 101 001	69	i	11 101 001	E9	i	10 001 001	89
j	01 101 010	6A	j	11 101 010	EA	j	10 010 001	91
k	11 101 011	EB	k	01 101 011	6B	k	10 010 010	92
l	01 101 100	6C	l	11 101 100	EC	l	10 010 011	93
m	11 101 101	ED	m	01 101 101	6D	m	10 010 100	94
n	11 101 110	EE	n	01 101 110	6E	n	10 010 101	95
o	01 101 111	6F	o	11 101 111	EF	o	10 010 110	96
p	11 110 000	F0	p	01 110 000	70	p	10 010 111	97
q	01 110 001	71	q	11 110 001	F1	q	10 011 000	98
r	01 110 010	72	r	11 110 010	F2	r	10 011 001	99

♦TABLE M (Contd)♦

CHARACTER TO HEX CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC		
CHAR.	BINARY	HEX	CHAR.	BINARY	HEX	CHAR.	BINARY	HEX
s	11 110 011	F3	s	01 110 011	73	s	10 100 010	A2
t	01 110 100	74	t	11 110 100	F4	t	10 100 011	A3
u	11 110 101	F5	u	01 110 101	75	u	10 100 100	A4
v	11 110 110	F6	v	01 110 110	76	v	10 100 101	A5
w	01 110 111	77	w	11 110 111	F7	w	10 100 110	A6
x	01 111 000	78	x	11 111 000	F8	x	10 100 111	A7
y	11 111 001	F9	y	01 111 001	79	y	10 101 000	A8
z	11 111 010	FA	z	01 111 010	7A	z	10 101 001	A9
0	00 110 000	30	0	10 110 000	B0	0	11 110 000	F0
1	10 110 001	B1	1	00 110 001	31	1	11 110 001	F1
2	10 110 010	B2	2	00 110 010	32	2	11 110 010	F2
3	00 110 011	33	3	10 110 011	B3	3	11 110 011	F3
4	10 110 100	B4	4	00 110 100	34	4	11 110 100	F4
5	00 110 101	35	5	10 110 101	B5	5	11 110 101	F5
6	00 110 110	36	6	10 110 110	B6	6	11 110 110	F6
7	10 110 111	B7	7	00 110 111	37	7	11 110 111	F7
8	10 111 000	B8	8	00 111 000	38	8	11 111 000	F8
9	00 111 001	39	9	10 111 001	B9	9	11 111 001	F9
SP	10 100 000	A0	SP	00 100 000	20	SP	01 000 000	40
!	00 100 001	21	!	10 100 001	A1	!	01 011 010	5A
”	00 100 010	22	”	10 100 010	A2	”	01 111 111	7F
#	10 100 011	A3	#	00 100 011	23	#	01 111 011	7B
$	00 100 100	24	$	10 100 100	A4	$	01 011 011	5B
%	10 100 101	A5	%	00 100 101	25	%	01 101 100	6C
&	10 100 110	A6	&	00 100 110	26	&	01 010 000	50
’	00 100 111	27	’	10 100 111	A7	’	01 111 101	7D
(	00 101 000	28	(	10 101 000	A8	(	01 001 101	4D
)	10 101 001	A9	)	00 101 001	29	)	01 011 101	5D
*	10 101 010	AA	*	00 101 010	2A	*	01 011 100	5C
+	00 101 011	2B	+	10 101 011	AB	+	01 001 110	4E
,	10 101 100	AC	,	00 101 100	2C	,	01 101 011	6B
-	00 101 101	2D	-	10 101 101	AD	-	01 100 000	60
.	00 101 110	2E	.	10 101 110	AE	.	01 001 011	4B
/	10 101 111	AF	/	00 101 111	2F	/	01 100 001	61
:	00 111 010	3A	:	10 111 010	BA	:	01 111 010	7A
;	10 111 011	BB	;	00 111 011	3B	;	01 011 110	5E
<	00 111 100	3C	<	10 111 100	BC	<	01 001 100	4C
=	10 111 101	BD	=	00 111 101	3D	=	01 111 110	7E
>	10 111 110	BE	>	00 111 110	3E	>	01 101 110	6E
?	00 111 111	3F	?	10 111 111	BF	?	01 101 111	6F
@	11 000 000	C0	@	01 000 000	40	@	01 111 100	7C
[	11 011 011	DB	[	01 011 011	5B			
\	01 011 100	5C	\	11 011 100	DC	\	11 100 000	E0
]	11 011 101	DD	]	01 011 101	5D			

♦TABLE M (Contd)♦

CHARACTER TO HEX CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC		
CHAR.	BINARY	HEX	CHAR.	BINARY	HEX	CHAR.	BINARY	HEX
∧	11 011 110	DE	∧	01 011 110	5E			
—	01 011 111	5F	—	11 011 111	DF	—	01 101 101	6D
`	01 100 000	60	`	11 100 000	E0	`	01 111 001	79
{	01 111 011	7B	{	11 111 011	FB	{	11 000 000	C0
¦	11 111 100	FC	¦	01 111 100	7C	¦	01 101 010	6A
}	01 111 101	7D	}	11 111 101	FD	}	11 010 000	D0
~	01 111 101	7E	~	11 111 110	FE	~	10 100 001	A1
						¢	01 001 010	4A
						¬	01 011 111	5F
						¦	01 001 111	4F
ACK	00 000 110	06	ACK	10 000 110	86	ACK	00 101 110	2E
BEL	10 000 111	87	BEL	00 000 111	07	BEL	00 101 111	2F
BS	10 001 000	88	BS	00 001 000	08	BS	00 010 110	16
						BYP	00 100 100	24
CAN	00 011 000	18	CAN	10 011 000	98	CAN	00 011 000	18
						CC	00 011 010	1A
CR	10 001 101	8D	CR	00 001 101	0D	CR	00 001 101	0D
DC1	00 010 001	11	DC1	10 001 001	91	DC1	00 010 001	11
DC2	00 010 010	12	DC2	10 010 010	92	DC2	00 010 010	12
DC3	10 010 011	93	DC3	00 010 011	13	DC3	00 010 011	13
DC4	00 010 100	14	DC4	10 010 100	94	DC4	00 011 100	3C
DEL	11 111 111	FF	DEL	01 111 111	7F	DEL	00 000 111	07
DLE	10 010 000	90	DLE	00 010 000	10	DLE	00 010 000	10
						DS	00 100 000	20
EM	10 011 001	99	EM	00 011 001	19	EM	00 011 001	19
ENQ	00 000 101	05	ENQ	10 000 101	85	ENQ	00 101 101	2D
						EOB	00 100 110	26
EOT	10 000 100	84	EOT	00 000 100	04	EOT	00 110 111	37
ESC	00 011 011	1B	ESC	10 011 011	9B	ESC	00 100 111	27
ETB	00 010 111	17	ETB	10 010 111	97	ETB	00 100 110	26
ETX	00 000 011	03	ETX	10 000 011	83	ETX	00 000 011	03
FF	00 001 100	OC	FF	10 001 100	8C	FF	00 001 100	OC
FS	10 011 100	9C	FS	00 011 100	1C	FS	00 100 010	22
GS	00 011 101	1D	GS	10 011 101	9D			
HT	00 001 001	09	HT	10 001 001	89	HT	00 000 101	05
						IFS	00 011 100	1C
						IGS	00 011 101	1D
						IL	00 010 111	17
						IRS	00 011 110	1E
						IUS	00 011 111	1F
						LC	00 000 110	06
LF	00 001 010	0A	LF	10 001 010	8A	LF	00 100 101	25

▶TABLE M (Contd)◀

CHARACTER TO HEX CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

EVEN PARITY ASCII			ODD PARITY ASCII			EBCDIC		
CHAR.	BINARY	HEX	CHAR.	BINARY	HEX	CHAR.	BINARY	HEX
NAK	10 010 101	95	NAK	00 010 101	15	NAK	00 111 101	3D
						NL	00 010 101	15
NUL	00 000 000	00	NUL	10 000 000	80	NUL	00 000 000	00
						PF	00 000 100	04
						PN	00 110 100	34
						PRE	00 100 111	27
						RES	00 010 100	14
						RLF	00 001 001	09
RS	00 011 110	1E	RS	10 011 110	9E	RS	00 110 101	35
SI	00 001 111	0F	SI	10 001 111	8F	SI	00 001 111	0F
						SM	00 101 010	2A
						SMM	00 001 010	0A
SO	10 001 110	8E	SO	00 001 110	0E	SO	00 001 110	0E
SOH	10 000 001	81	SOH	00 000 001	01	SOH	00 000 001	01
						SOS	00 100 001	21
STX	10 000 010	82	STX	00 000 010	02	STX	00 000 010	02
SUB	10 011 010	9A	SUB	00 011 010	1A	SUB	00 111 111	3F
SYN	10 010 110	96	SYN	00 010 110	16	SYN	00 110 010	32
						UC	00 110 110	36
US	10 011 111	9F	US	00 111 111	1F			
VT	10 001 011	8B	VT	00 001 011	0B	VT	00 001 011	0B

OF SYNC CHARS = ? 0-5 will appear. If one through five sync characters are selected then the message ENTER X SYNC CHAR ?? ?? ... ?? is displayed, where X is the selected number of sync characters. (The number of ?? pairs corresponds to the selected number X.) The operator then enters the desired sync characters as two hex digits each. Each hex digit replaces one of the ? on the display. If 0 sync characters are selected then the previous message will not appear.

4.82 ▶Next, the message NO. OF LOG CHARS = ??? MAX = 255 will appear.◀ (The number of log characters includes the sync characters.) After a number from 001 to 255 has been selected, the test begins and the message WAITING FOR SYNC is displayed. When sync is detected, the message SYNC DETECTED appears. After the selected number of characters have been received, the first line of characters (ten maximum) will be displayed along with line number 00; for example, 00: D1 55 C9 C3 4B A0 42 D2 CF D7. Note that 00: designates the first line; 01: the second line, etc.

4.83 The operator may now look at any line of ten characters within the received message by using the B, C, E and F keys. The first two digits always specify the line number currently displayed. The function of these keys is as follows.

B key—display previous line of characters

C key—display first line of characters

E key—display last line of characters

F key—display next line of characters.

Pressing the A key will repeat the test (including selection of sync characters). To terminate the test, press GO.

◆TABLE N◆

HEX TO CHARACTER CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX	HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX
00	NUL	NUL		00	28		(		28
01	SOH		SOH	01	29			)	29
02	STX		STX	02	2A	SM		*	2A
03	ETX	ETX		03	2B		+		2B
04	PF		EOT	04	2C			,	2C
05	HT	ENQ		05	2D	ENQ	—		2D
06	LC	ACK		06	2E	ACK	.		2E
07	DEL		BEL	07	2F	BEL		/	2F
08			BS	08	30		0		30
09	RLF	HT		09	31			1	31
0A	SMM	LF		0A	32	SYN		2	32
0B	VT		VT	0B	33		3		33
0C	FF	FF		0C	34	PN		4	34
0D	CR		CR	0D	35	RS	5		35
0E	SO		SO	0E	36	UC	6		36
0F	SI	SI		0F	37	EOT		7	37
10	DLE		DLE	10	38			8	38
11	DC1	DC1		11	39		9		39
12	DC2	DC2		12	3A		:		3A
13	DC3		DC3	13	3B			;	3B
14	RES	DC4		14	3C	DC4	<		3C
15	NL		NAK	15	3D	NAK		=	3D
16	BS		SYN	16	3E			>	3E
17	IL	ETB		17	3F	SUB	?		3F
18	CAN	CAN		18	40	SP		@	40
19	EM		EM	19	41		A		41
1A	CC		SUB	1A	42		B		42
1B		ESC		1B	43			C	43
1C	IFS		FS	1C	44		D		44
1D	IGS	GS		1D	45			E	45
1E	IRS	RS		1E	46			F	46
1F	IUS		US	1F	47		G		47
20	DS		SP	20	48		H		48
21	SOS	!		21	49			I	49
22	FS	"		22	4A	¢		J	4A
23			#	23	4B	•	K		4B
24	BYP	$		24	4C	<		L	4C
25	LF		%	25	4D	(	M		4D
26	EOB/ETB		&	26	4E	+	N		4E
27	ESC/PRE	'		27	4F	|		O	4F

♦TABLE N (Contd)♦

HEX TO CHARACTER CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX	HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX
50	&	P		50	78		x		78
51			Q	51	79	\		y	79
52			R	52	7A	:		z	7A
53		S		53	7B	#	{		7B
54			T	54	7C	@		¦	7C
55		U		55	7D	'	}		7D
56		V		56	7E	=	~		7E
57			W	57	7F	"		DEL	7F
58			X	58	80			NUL	80
59		Y		59	81	a	SOH		81
5A	!	Z		5A	82	b	STX		82
5B	$		[	5B	83	c		ETX	83
5C	*	\	\	5C	84	d	EOT		84
5D	)		]	5D	85	e		ENQ	85
5E	;		Λ	5E	86	f		ACK	86
5F	¬	—		5F	87	g	BEL		87
60	-	\		60	88	h	BS		88
61	/		a	61	89	i		HT	89
62			b	62	8A			LF	8A
63		c		63	8B		VT		8B
64			d	64	8C			FF	8C
65		e		65	8D		CR		8D
66		f		66	8E		SO		8E
67			g	67	8F			SI	8F
68			h	68	90		DLE		90
69		i		69	91	j		DC1	91
6A	¦	j		6A	92	k		DC2	92
6B	,		k	6B	93	l	DC3		93
6C	%	l		6C	94	m		DC4	94
6D	—		m	6D	95	n	NAK		95
6E	>		n	6E	96	o	SYN		96
6F	?	o		6F	97	p		ETB	97
70			p	70	98	q		CAN	98
71		q		71	99	r	EM		99
72		r		72	9A		SUB		9A
73			s	73	9B			ESC	9B
74		t		74	9C		FS		9C
75			u	75	9D			GS	9D
76			v	76	9E			RS	9E
77		w		77	9F		US		9F

♦TABLE N (Contd)♦

HEX TO CHARACTER CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX	HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX
A0		SP		A0	C8	H		H	C8
A1	~		!	A1	C9	I	I		C9
A2	s		"	A2	CA		J		CA
A3	t	#		A3	CB			K	CB
A4	u		$	A4	CC		L		CC
A5	v	%		A5	CD			M	CD
A6	w	&		A6	CE			N	CE
A7	x		'	A7	CF		O		CF
A8	y		(	A8	D0	}		P	D0
A9	z	)		A9	D1	J	Q		D1
AA		*		AA	D2	K	R		D2
AB			+	AB	D3	L		S	D3
AC		,		AC	D4	M	T		D4
AD			—	AD	D5	N		U	D5
AE			.	AE	D6	O		V	D6
AF		/		AF	D7	P	W		D7
B0			0	B0	D8	Q	X		D8
B1		1		B1	D9	R		Y	D9
B2		2		B2	DA			Z	DA
B3			3	B3	DB		[		DB
B4		4		B4	DC			\	DC
B5			5	B5	DD		]		DD
B6			6	B6	DE		\		DE
B7		7		B7	DF			—	DF
B8		8		B8	E0	\		\	E0
B9			9	B9	E1		a		E1
BA			:	BA	E2	S	b		E2
BB		:		BB	E3	T		c	E3
BC			<	BC	E4	U	d		E4
BD		=		BD	E5	V		e	E5
BE		>		BE	E6	W		f	E6
BF			?	BF	E7	X	g		E7
C0	{	@		C0	E8	Y	h		E8
C1	A		A	C1	E9	Z		i	E9
C2	B		B	C2	EA			j	EA
C3	C	C		C3	EB		k		EB
C4	D		D	C4	EC			l	EC
C5	E	E		C5	ED		m		ED
C6	F	F		C6	EE		n		EE
C7	G		G	C7	EF			o	EF

♦TABLE N (Contd)♦

HEX TO CHARACTER CONVERSION FOR EVEN PARITY ASCII, ODD PARITY ASCII, AND EBCDIC CODES

HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX	HEX	EBCDIC	EVEN PARITY ASCII	ODD PARITY ASCII	HEX
F0	0	p		F0	F8	8		x	F8
F1	1		q	F1	F9	9	y		F9
F2	2		r	F2	FA		z	·	FA
F3	3	s		F3	FB			{	FB
F4	4		t	F4	FC		¦		FC
F5	5	u		F5	FD			}	FD
F6	6	v		F6	FE			~	FE
F7	7		w	F7	FF		DEL		FF

Note: If sync has been detected and the number of received characters is less than the number of specified logged characters, then the message SYNC DETECTED will remain. Only when the number of received characters equals or exceeds the specified number of logged characters will the first line of received characters be displayed.

Test Code 51—Programmable Message (TRMT)

Versions 2 and 3

4.84 This test provides for transmitting a user programmed message in either synchronous or asynchronous format. The transmission format is determined by the data set code previously entered. Any message length from 1 to 255 characters can be selected. Each character to be transmitted is entered as two hex digits from the keyboard. Tables M and N give conversion from ASCII and EBCDIC characters to hex digits.

4.85 After all of the characters have been entered, the message is transmitted with all characters back-to-back (no gaps) in either of two modes: manual or continuous. In the continuous mode, RS is kept ***on*** at all times and the messages are sent out one after another as long as CS is ***on***. In the manual mode, RS is turned ***on***, one message is transmitted after CS goes ***on***, and then RS is turned ***off***.

4.86 An editing feature is provided to allow the user to scan, change, and delete characters while they are being entered. The editing mode may be reentered at any time during or after message transmission. The edit mode is described in paragraph 4.90.

4.87 To enter characters and transmit a programmable message enter test code 51 and press GO. If a 212-type data set was selected for asynchronous operation at 1200 bps, the message BITS/CHAR=? (0=NINE 1=TEN) is displayed. Otherwise the message SELECT 0001 to 0255 CHARACTERS will be displayed, followed by ???? CHARACTERS IN MESSAGE. After the user enters the desired number of characters, the display 00:?? ?? ... ?? appears. Each pair of question marks indicate a location for two hex digits (eight data bits) to be entered from the keyboard. For asynchronous transmission, the DTS adds one start and one stop-bit per character. For nine bits per character operation, the most significant (eight) bit is not transmitted.

4.88 The locations for the characters on each line are referred to as locations 0 through 9. The 00: indicates the first line of the message. The user can now begin entering the hex digits from the keyboard. Each time a digit is entered a question mark is replaced by the digit entered. For example, if the user presses 5 and then C, the first pair of question marks will be replaced with 5C. The next pair of digits entered will replace the next pair of question marks and so on.

4.89 If the number of characters selected is greater than ten, then after the tenth hex pair has been entered, the display will be 01:?? ?? ... ?? where 01 indicates the second line of the message. The user can continue entering hex digits until the number of characters entered is equal to the specified number of characters in the message. By pressing the ← key, the user can enter the edit mode, described in paragraphs 4.90 and 4.91, to change previously entered characters. After the last character in the message has been entered, the message TRMT=? (1=MAN 2=CONT) appears. The user then selects the mode by entering either a 1 for manual, or a 2 for continuous transmission. The next message to be displayed is PRESS A TO START OR ← TO EDIT. If the A key is pressed, RS goes ***on***, and the message will be transmitted after CS goes ***on***. (If a CSU is being tested, the DTS does not look for a CS ***on*** indication before sending the message.) The display will read SENDING MESSAGE while the message is being transmitted. Transmission may be stopped at any time by pressing the D key. This causes RS to go ***off*** and the message PRESS A TO START OR ← TO EDIT will be displayed. The user can then send the message again or enter the edit mode.

4.90 The edit mode can be entered by pressing the ← key to allow scanning, changing, or deleting characters in the message. After the ← key is pressed, the display XX:YY*YY*...*YY will appear, where YY represents previously entered hex digits and XX represents the line number in the message. The * marks are an indication to the user that the DTS is now in the edit mode. Table F shows the function of the B, C, D, E, F, and ← keys while in the edit mode. As an example, suppose that the 25th character (corresponding to location 4 on line 02) contains hex digits 8B and is to be changed to digits 9C. In order to change this character, line number 02 must be found by using the appropriate B, C, E, and F keys. When line 02 is found, the display will indicate:

02:YY*YY*YY*YY*8B*YY*YY*YY*YY*YY,

where the fifth pair of digits is the 8B which is to be changed. Next the user presses the 4 key since the digits 8B are in location four on the line. The display will now show two question marks in location four on the line. The user now presses 9 and then C which replace the two question marks in location four. Next, the user should press the ← key to exit the edit mode. The display will now be TRMT=? (1=MAN 2=CONT) as previously described.

4.91 The editing mode can also be used during the initial entry of characters before the total number of characters has been reached. Hence, if a mistake is recognized at any time during entry of characters, the ← key will allow the user to correct the mistake by going to the edit mode. Characters can be deleted one at a time within a message while in the edit mode. As an example of this, suppose the seventh character (location 6) contains the hex digits AB which are to be deleted. After entering the edit mode and finding line 00, the display will be:

00:YY*YY*YY*YY*YY*YY*AB*ZZ*YY*YY,

where AB is the character (location 6) to be deleted, ZZ is the next character, and YY represents the other characters on the line. The user now presses 6 causing the AB to be replaced by ??. Next, the ← key is pressed which deletes the two question marks, moves the ZZ characters over to where the ?? was previously located and moves the YY pairs left one position. The hex digits in the extreme right position on the line are replaced by the hex digits in the extreme left position on the next line and so on until the rest of the message has moved one position to the left. Additional characters can also be deleted in a similar fashion.

Note: Whenever characters are deleted from a message, additional characters must be inserted at the end of a message such that the total characters in the message are equal to the number of characters selected by the user at the beginning of the test.

4.92 When entering a message, if the mistakes in the entered characters are too numerous to correct, the entire message can be eliminated by pressing the D key. The display will show SELECT 0001 to 0255 CHARACTERS which is the beginning of the test as described above.

Test Code 52—FOX Message (TRMT)

Version 1 Only

4.93 This test provides for transmitting a start-stop formatted ASCII message through a nonsynchronous data set.

4.94 The message can be transmitted to another 921A located at the far end, a 911NA DTS, a DATASPEED® 40 terminal, or any device which is capable of receiving start-stop formatted messages as described in paragraphs 4.95 and 4.96. The message is 31 printable characters (THE QUICK BROWN FOX JUMPED OVER), preceded by four nonprinting characters (DEL, CR, LF, DEL), and followed by a space and a DEL character. Each character consists of 7-bit ASCII code, even parity bit, one start and one stop bit. The message is transmitted with all characters back-to-back (no gaps) in two modes, manual or continuous.

4.95 In the continuous mode, RS is kept ***on*** at all times and the messages are sent out one after another provided that CS is ***on***. In the manual, or one-shot mode, RS is turned ***on***, the data set responds with CS going ***on***, one message is transmitted, and then RS is turned ***off***.

4.96 To transmit the FOX message, enter test code 52 and press GO. The message TRMT: 1=MAN 2=CONT will be displayed. Select 1 for the manual mode or 2 for the continuous mode. For the continuous mode, the DTS displays PRESS A TO START after which it displays SENDING ASCII MESSAGE while transmitting. For the manual mode, the DTS displays PRESS A TO START and will transmit one message each time A is pressed. In the manual mode, the display SENDING ASCII MESSAGE appears only briefly, while the DTS is transmitting. To stop transmission, press GO.

Test Code 52—Fox Message (TRMT)

Versions 2 and 3

4.97 This test provides for transmitting a message in either synchronous or asynchronous format. The message can be transmitted to another 921A or any other device which is capable of receiving the formatted messages as described in paragraph 4.98. The message contains 73 printable ASCII characters (The Quick Brown Fox Jumped Over A Lazy Dog's Back 1234567890 Testing 0123) and is preceded by four nonprinting characters (DEL, CR, LF, DEL). Two SYN characters (hex digits 16) precede the message in synchronous transmission.

4.98 The format (synchronous or asynchronous) is determined by the DTS according to the type of data set being tested. In asynchronous transmission each character consists of a 7-bit ASCII code, parity bit, one start and one stop bit for a total of ten bits. Even or odd parity may be selected by the user. Also if a 212-type data set is being tested at 1200 bps asynchronous, the user may select a 9-bit character length in which case the parity bit is deleted from each character. The message is transmitted with all characters back-to-back (no gaps) in two modes, manual or continuous.

4.99 In the continuous mode, RS is kept ***on*** at all times and the messages are sent out one after the other after CS is ***on***. In the manual, or one-shot mode, RS is turned ***on*** and after the data set responds by turning CS ***on***, one message is transmitted and then RS is turned ***off***.

4.100 To transmit the FOX message, enter test code 52 and press GO. If a 212 data set arranged for 1200-bps asynchronous operation is being tested, the message BITS/CHAR=? (0=NINE 1=TEN) will be displayed. Otherwise, the message PARITY=? (0=EVEN, 1=ODD) is displayed. After the parity has been selected by the user, the message TRMT=? (1=MAN 2=CONT) is displayed. After selecting the transmit mode, the message PRESS A TO START appears. When the A key is pressed, RS is turned ***on*** and the message will be transmitted after CS goes ***on***. During the interval between RS ***on*** and CS ***on***, the message CS MUST BE ON TO TRANSMIT is displayed. After CS goes ***on*** the display SENDING MESSAGE appears while the message is being transmitted.

4.101 In the manual mode, the display PRESS A TO START will appear after the FOX message has been transmitted. The operator may then press the A key to send the message again. To terminate the test, press GO.

4.102 In the continuous mode, the display SENDING MESSAGE will remain indefinitely after the A key has been pressed. The operator may stop sending the message at any time by pressing the D key. This causes RS to go ***off*** and the display PRESS A TO START appears. The test may be resumed by pressing the A key. To terminate the test, press GO.

4.103 If a CSU is being tested, the message will be transmitted as soon as RS goes ***on***, since a CSU does not have a CS lead.

Dot, Space, Mark and 2047-, 511-, or 63-Bit Pseudorandom Word Error Test

4.104 The transmit only (test code 53) or receive only (test code 54) tests require a DTS and a craft person at the remote station. The full-duplex (test code 55) test can be performed with or without a DTS at the remote station. If the remote data set is placed in the loopback mode, the test can be performed entirely from the near station.

4.105 The DTS can generate and record bit or block errors on the following six patterns: 63-, 511-, or 2047-bit pseudorandom word, or marking, spacing, and dotting.

4.106 Since the three pseudorandom word patterns are compatible with those generated by other Bell System DTSs, the 921A DTS may be used with another 921A DTS or any compatible DTS to perform pseudorandom error tests.

4.107 Any of the six error tests may be performed in a half-duplex, transmit-only mode (test code 53), half-duplex, receive-only mode (test code 54), or full-duplex mode (test code 55). The DTS also provides the capability for ending the test automatically after a selectable period of time. In addition to recording bit errors, or blocks received and blocks received in error, a record is kept of the number of sync losses occurring during the test. When the DTS determines that it has lost word synchronization, it automatically attempts to regain sync.

4.108 The error test also allows the transmitting station to manually inject eight errors into the data stream or manually force an out-of-sync (OSYN) condition. When a bit error test is performed with a 202-type data set, the DTS is programmed to automatically condition its receiver to phase lock to the incoming data.

Test Code 53—Transmit—Dot, Space, Mark and 2047-, 511-, or 63-Bit Pseudorandom Word Test

4.109 Enter test code 53 and press GO. Display reads SELECT ERROR TEST, briefly, followed by D=DT 0=SP 1=MK 2=2047 5=511 6=63 which indicates that a selection must be made of the pattern to be transmitted.

4.110 Selecting the indicated keys causes the following displays.

Key D, DOTTING BIT ERROR TEST

Key 0, SPACING BIT ERROR TEST

Key 1, MARKING BIT ERROR TEST

Key 2, 2047 BIT ERROR TEST

Key 5, 511 BIT ERROR TEST

Key 6, 63 BIT ERROR TEST.

4.111 When the key is pressed, the appropriate bit pattern is transmitted and the display remains unchanged for the duration of the test.

4.112 Key E may be used to manually inject eight error bits while key F may be used to force an OSYN condition into the transmitted data stream.

> ***Note:*** Key F does not force an out-of-sync condition when the marking or spacing pattern is being transmitted.

Test Code 54—Receive—Dot, Space, Mark, and 2047-, 511-, or 63-Bit Pseudorandom Word Test

4.113 Enter test code 54 and press GO. If a non-synchronous data set (for example, 202-type) code has been entered, the display will read TRANSMITTER=? 1=921 2=914 3=903. The type of far-end transmitter must now be entered by pressing the appropriate key. This information is necessary for setting the pull-in range of the receiver phase-locked clock. The display will now indicate SELECT ERROR TEST briefly and D=DT 0=SP 1=MK 2=2047 5=511 6=63 which indicates a selection is to be made. If a data set code other than 202 has been entered, SELECT ERROR TEST would appear immediately after entering test code 54 and pressing GO.

> ***Note 1:*** Some tests performed with a 903 or 914 as the transmitter may not operate as a result of a narrow receiver pull-in range

setting in the 921A. In the case of the 914, specify the transmitter as 3=903 in order to set up a wider receiver pull-in range. If the test still cannot be performed, the transmitter frequency of the 914 is beyond the widest setting of the receiver pull-in range. Versions 2 and 3 of the DTS extend the receiver pull-in range.

Note 2: If operating at 56 kb/s, the 63- and 511-bit pseudorandom word patterns cannot be used. The display shows D=DT 0=SP 1=MK 2=2047.

4.114 Selecting the indicated keys causes the following displays.

Key D, DOTTING BIT ERROR TEST

Key 0, SPACING BIT ERROR TEST

Key 1, MARKING BIT ERROR TEST

Key 2, 2047 BIT ERROR TEST

Key 5, 511 BIT ERROR TEST

Key 6, 63 BIT ERROR TEST.

4.115 Pressing one of the keys initiates the appropriate bit pattern and causes the display to read 1=BIT ERRORS 2=BLOCK ERRORS, indicating a selection must be made whether bit or block errors will be recorded.

4.116 If bit errors are to be recorded, key 1 is pressed and the display indicates ???? SECONDS. Go to paragraph 4.120 if key 1 is pressed.

4.117 If block errors are to be recorded, key 2 is pressed and the display indicates ???? BITS IN A BLOCK. The number of bits is entered via the keyboard. This number must be greater than or equal to 1024 and less than or equal to 59992. A number outside this range causes the following momentary display SELECT BETWEEN 1024 & 59992.

4.118 The number of bits entered should be a multiple of eight. If not entered as a multiple of eight, the number is rounded off and displayed.

4.119 After the number of bits in a block is entered, the display indicates ???? SECONDS.

4.120 The duration of the test is now entered and may be from 0001 to 9998 seconds. Selecting 9999 results in an untimed test which will run indefinitely.

4.121 The test starts immediately after the time interval is entered. If bit errors have been selected, the display indicates 0000 BITS IN ERROR and records bits in error. If block errors have been selected, the display indicates BLK RCVD=0000 ERR=0000 and records blocks received and blocks in error. A block in error is recorded when one or more bits in the block are in error. In either case, the display will indicate an OSYN or overflow (OVF) condition if it exists during the test.

Note 1: A sync loss will be registered when more than 255 bits in a 1024-bit group are in error.

Note 2: Bit error tests performed on DDS are usually specified in terms of error-free seconds. To determine error-free seconds, first select the block length (in bits) to correspond to 1 second; for example, specify the block length as 2400 bits for 2.4 kb/s operation. Then subtract the error blocks (ERR) from the blocks received (BLK RCVD) to obtain the error-free seconds.

4.122 If the duration of the test has been specified, the test will automatically terminate at the end of the specified interval. This is indicated by the DTS cycling through a series of three messages. For a bit error test, the messages are TEST COMPLETE, XXXXX SYNC LOSSES, XXXX BITS IN ERROR. For a block error test, the three messages are TEST COMPLETE, XXXXX SYNC LOSSES, BLK RCVD=XXXX ERR=XXXX. In either case, the second message indicates the number of sync losses that occurred during the test. The third message is the final result of the test.

4.123 Special function keys A, B, C, and D provide additional control of the error test (Table E).

(a) Pressing key A at any time during the test or when a test has terminated clears the display and reinitiates the test. All information previously entered is used (bit pattern, bit or

block errors, bits in a block, and length of test) and does not have to be specified again.

(b) Pressing key B anytime during a timed test displays the time remaining in the test.

(c) Pressing key C clears the display.

(d) Pressing key D during a test terminates the test and displays test results. The test may be reinitialized by pressing key A.

4.124 For every error (bit or block) recorded by the DTS, an output pulse will appear at the front panel test point labeled ERRORS.

> ***Note:*** When an OSYN condition has occurred, the number of output pulses appearing at the test point may be less than the number of errors indicated on the display.

Test Code 55—Full Duplex—Dot, Space, Mark, and 2047-, 511-, or 63-Bit Pseudorandom Word Test

4.125 Enter test code 55 and press GO. If a nonsynchronous data set (for example, 202-type) code has been inputted, the display will read TRANSMITTER=? 1=921 2=914 3=903. The type of far-end transmitter must now be inputted by pressing the appropriate key. This information is necessary for setting the pull-in range of the receiver phase-locked clock. The display will now indicate SELECT ERROR TEST briefly and D=DT 0=SP 1=MK 2=2047 5=511 6=63 which indicates a selection is to be made. If a data set code other than 202 had been entered, SELECT ERROR TEST would appear immediately after entering test code 55 and pressing GO.

> ***Note 1:*** Some tests performed with a 903 or 914 as the transmitter ***may*** not operate as a result of a narrow receiver pull-in range in the 921A. In the case of the 914, specify the transmitter as 3=903 in order to set up a wider receiver pull-in range. If the test still cannot be performed, the transmitter frequency of the 914 is beyond the widest setting of receiver pull-in range. Versions 2 and 3 of the DTS extend the receiver pull-in range.
>
> ***Note 2:*** If operating at 56 kb/s, the 63- and 511-bit pseudorandom word patterns cannot be used. The display will show D=DT 0=SP 1=MK 2=2047.

4.126 Selecting the indicated keys causes the following displays.

Key D, DOTTING BIT ERROR TEST

Key 0, SPACING BIT ERROR TEST

Key 1, MARKING BIT ERROR TEST

Key 2, 2047 BIT ERROR TEST

Key 5, 511 BIT ERROR TEST

Key 6, 63 BIT ERROR TEST.

Pressing one of the keys initiates the appropriate bit pattern and causes the display to read 1=BIT ERRORS 2=BLOCK ERRORS, indicating a selection must be made whether bit or block errors will be recorded.

4.127 If bit errors are to be recorded, key 1 is pressed and the display indicates ???? SECONDS. Go to paragraph 4.131 if key 1 is pressed.

4.128 If block errors are to be recorded, key 2 is pressed and the display indicates ????? BITS IN A BLOCK. The number of bits is entered via the keyboard. This number must be greater than or equal to 1024 and less than or equal to 59992. A number outside this range causes the following momentary display SELECT BETWEEN 1024 & 59992.

4.129 The number of bits entered should be a multiple of eight. If not entered as a multiple of eight, the number is rounded off and displayed.

4.130 After the number of bits in a block is entered the display indicates ???? SECONDS.

4.131 The duration of the test is now entered and may be from 0001 to 9998 seconds. Selecting 9999 results in an untimed test which will run indefinitely.

4.132 The test starts immediately after the time interval is entered. If bit errors have been selected, the display indicates 0000 BITS IN ERROR

and records bits in error. If block errors have been selected, the display indicates BLK RCVD=0000 ERR=0000 and records blocks received and blocks in error. A block error is recorded when one or more bits in the block are in error. In either case, the display will indicate an OSYN or OVF condition if it exists during the test.

Note 1: A sync loss will be registered when more than 255 bits in a 1024-bit group are in error.

Note 2: Bit error tests performed on the DDS are usually specified in terms of error-free seconds. To determine error-free seconds, first select the block length (in bits) to correspond to 1 second. For example, specify the block length as 2400 bits for 2.4 kb/s operation. Then subtract the error blocks (ERR) from the blocks received (BLK RCVD) to obtain the error-free seconds.

4.133 If the duration of the test has been specified, the test will automatically terminate at the end of the specified interval. This is indicated by the DTS cycling through a series of three messages. For a bit error test, the messages are TEST COMPLETE, XXXXX SYNC LOSSES, XXXX BITS IN ERROR. For a block error test, the three messages are TEST COMPLETE, XXXXX SYNC LOSSES, BLK RCVD=XXXX ERR=XXXX. In either case, the second message indicates the number of sync losses that occurs during the test. The third message is the final result of the test.

4.134 Special function keys A, B, C, D, E, and F provide additional control of the error test (Table E).

(a) Pressing key A at any time during the test or when a test has terminated clears the display and reinitiates the test. All information previously entered is used (bit pattern, bit or block errors, bits in a block, and length of test) and does not have to be specified again.

(b) Pressing key B anytime during a timed test displays the time remaining in the test.

(c) Pressing key C clears the display.

(d) Pressing key D during a test terminates the test and displays test results. The test may be reinitialized by pressing key A.

(e) Each time key E is pressed during a test, eight errors are injected into the transmitted data stream.

(f) Pressing key F forces an OSYN condition to be generated in the transmitted data stream.

Note: Key F does not force an OSYN condition when the marking or spacing pattern is being transmitted.

4.135 For every error (bit or block) recorded by the DTS, an output pulse will appear at the front panel test point labeled ERRORS.

Note: When an OSYN condition has occurred, the number of output pulses appearing at the test point may be less than the number of errors indicated on the display.

4.136 An application of test code 55 for testing a line circuit with a loopback DAS is given in paragraph 5.03.

Test Code 57—Parity

4.137 Both even and odd parity errors may be counted by using test code 57. The received data signal must be in ASCII format (seven information bits plus one parity bit) with one start bit and one or more stop bits. End-to-end tests may be performed with another 921A, a 911NA DTS, a DATASPEED 40 terminal, or any device which transmits the properly formatted signal.

4.138 To initiate the test, enter test code 57. The DTS will display the prompting message : 57 ? (0=EVEN 1=ODD). Enter 0 if parity to be measured is even; enter 1 if odd. Press GO after selecting parity. To start the test, press key A after the DTS displays PRESS A TO START. The message PARITY ERRORS=00 will appear whether or not data is being received.

4.139 To ensure that data is being received by the DTS, visually check the RD LEDs. This measurement is not timed and will be performed indefinitely until the operator interrupts it. The OVF indicator will appear on the display after 99 counts while the counter will continue to function.

4.140 During the test, key C may be pressed to clear the parity error count. In the event

that sync is lost (rapid overflow of parity errors), press key A to resynchronize. The test may be interrupted or terminated by pressing GO.

4.141 For every parity error recorded by the DTS, an output pulse will appear on the front panel test point labeled ERRORS.

▶*Test Code 58—Full Duplex Programmable Message Test*◀

4.142 ▶This test transmits a user programmable message and simultaneously receives an incoming message that can begin with a user programmable sequence of characters. Data terminals, either local or remote, can be tested using test code 58 (see paragraph 4.145). The transmission format, synchronous or asynchronous, is determined by the data set code previously entered into the test set. If testing a terminal on a stand alone (local) basis, the data set code that is entered at the beginning of the testing session should be compatible with the characteristics of the terminal. The transmitted message length may be 1 to 255 characters and the received message may contain a maximum of 255 characters. For the user programmable message, each character to be transmitted is entered as two hex digits from the keyboard. Any one of the 17 standard messages is entered automatically, with prompting for special parameters as required. Tables M and N give conversion from ASCII and EBCDIC characters to hex digits, which may be useful if entering a user programmable message. When using a synchronous format, the particular sync character expected in the incoming receive data and the number of contiguous sync characters expected, are entered from the keyboard. In addition, for synchronous or asynchronous format, the sequence of characters which determine the beginning of the incoming message, called trap characters, may be zero to 20 characters in length and are also entered from the keyboard.

> ***Note:*** Test code 58 identifies three types of characters which are defined as follows.

Sync character(s) — Several identical characters at the beginning of a synchronous message used to determine character boundaries in the message.

Trap character(s) — Up to 20 characters in a receive message used to mark the beginning of the data to be stored in the receive buffer.

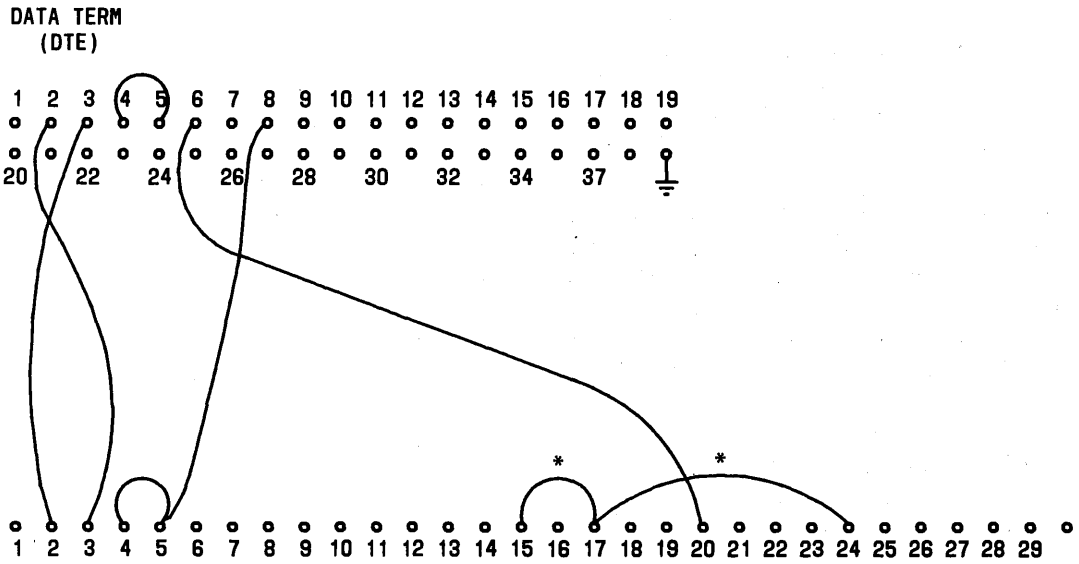
Log Character(s) — Up to 255 characters stored in the receive buffer following the trap characters but not including the trap characters.◀

4.143 ▶After all the transmit characters, receive sync character and number, and receive trap characters have been entered, request-to-send (RS) is turned ***on,*** the message is transmitted when clear-to-send (CS) goes ***on,*** and at the end of the message, RS is turned ***off.*** Simultaneously, a search for the receive sync character(s) is begun on the incoming data if the synchronous format is used. If an asynchronous format is used, the sync character search is omitted. After the sync character is detected, when the format is synchronous, or beginning immediately when the format is asynchronous, incoming data is searched to obtain a match with the trap sequence assuming zero trap was not selected. Once trap is detected, or if zero trap was selected, the next 255 incoming characters including trap characters are stored in a receive buffer for later display. All the characters after the trap characters are called log characters.◀

4.144 ▶An editing feature is provided to allow the user to scan, change, and delete characters while they are being entered. The editing mode may be reentered at any time during or after message transmission. The edit mode is described in paragraph 4.150.◀

4.145 ▶To use the full duplex programmable message test, enter test code 58 in response to TEST SEQ:, and press GO. The message CHANGE JACK FIELD IF LOCAL TEST is displayed. If testing directly into a data terminal, rearrange the jack field according to Fig. 16. If a 212-type data set was selected for asynchronous operation at 1200 b/s, the message TST CODE 58 REQUIRES 10 BIT CHAR is displayed. (See DS 212 Section 592-034-100.) If 9-bit characters are in use, the proper options must be changed to 10-bit characters for test code 58 to work properly on a DS 212.◀

4.146 ▶The message 1=PROGRAMMABLE 2=STANDARD MSG will now appear. Assume that 1 is pressed so that a user programmable message can be entered. The message SELECT 0001 to 0255 CHARACTERS will be displayed, followed by ???? CHARACTERS IN MESSAGE. After the user enters the desired number of transmit characters, the display 00:?? ?? ... ?? appears. Each pair of question marks indicates a location for two hex digits (eight data bits each) to be entered from



CAUTION: DO NOT CLOSE COVER WITH JUMPER WIRES INSERTED IN PIN JACKS

NOTES:
1. OPEN ALL SLIDE SWITCHES TO THE DTE EXCEPT 1 AND 7.
2. PLACE JUMPER WIRES AS INDICATED ABOVE.
3. IF TESTING A SYNCHRONOUS TERMINAL, SUCH AS A 40/4, ALSO CLOSE SLIDE SWITCHES 15 AND 17.
4. JUMPER WIRES MARKED WITH * MUST BE IN PLACE FOR SYNCHRONOUS TERMINALS.

Fig. 16—Jumper Wire Connections

the keyboard. For asynchronous transmission, the DTS adds one start and one stop bit per character.

4.147 The locations for the 10 characters on each line are referred to as locations 0 through 9. The 00: indicates the first line of the message. The user can now begin entering the hex digits from the keyboard. Each time a digit is entered a question mark is replaced by the digit entered. For example, if the user presses 5 and then C, the first pair of question marks will be replaced with 5C. In the case of even parity ASCII (Table N), that would be the backslash character. The next pair of digits entered will replace the next pair of question marks and so on.

4.148 If the number of characters selected is greater than ten, then after the tenth hex pair has been entered, the display will be 01:?? ?? ... ?? where 01 indicates the second line of the message. The user can continue entering hex digits until the number of characters entered is equal to the number specified for the message. By pressing the ← key, the user can enter the edit mode, described in paragraph 4.150 to change previously entered characters. After the last character in the message has been entered, the message A TO CONTINUE OR ← TO EDIT TRMT appears.

4.149 Returning to the message 1= PROGRAMMABLE 2=STANDARD MSG, and assuming that 2 is entered on the keyboard, the message STANDARD MSG NUMBER=?? (01-17) is displayed. The user enters two digits via the keyboard to select one of 17 possible standard messages. Table O lists the 17 messages, indicating the terminal(s) that each message is designed to test and giving the extra parameters required to complete a message. Messages 01 to 03 are used

to test EBCDIC DATASPEED 40/4 terminals, or equivalent. Messages 04 to 06 are used to test ASCII DATASPEED 40/4 terminals, or equivalent. Messages 07 to 17 are used to test DATASPEED 40/1, 40/2, or 40/3 terminals, or equivalent. Messages 01, 02, 04, 05, and 12 have extra parameters which cause the DTS to display special prompting messages as indicated in Table O. After any extra parameters have been entered the program proceeds along a common line regardless of whether the transmit message was entered manually by the user or automatically by use of the standard message. The message A TO CONTINUE OR ← TO EDIT TRMT appears.◀

4.150 ▶The edit mode can be entered by pressing the ← key to allow scanning, changing, or deleting characters in a message. After the ← key is pressed, the display XX:YY*YY*...*YY will appear, where YY represents previously entered hex digits and XX represents the line number in the message. The * is an indication to the user that the DTS is now in the edit mode. Table F shows the function of the B, C, D, E, F, and ← keys while in the edit mode. As an example, suppose that the 25th character (corresponding to location 4 on line 02) contains hex digits 8B and is to be changed to digits 9C. In order to change this character, line number 02 must be found by using the appropriate B, C, E, and F keys. When line 02 is found, the display will indicate:

02:YY*YY*YY*YY*8B*YY*YY*YY*YY*YY,

where the fifth pair of digits is the 8B which is to be changed. Next, the user presses the 4 key since the digits 8B are in location four on the line. The display will now show two question marks in location four on the line. The user now presses 9 and then C which replace the two question marks in location four. Next, the user should press the ← key to exit the edit mode. The display will return to the above message, A TO CONTINUE OR ← TO EDIT TRMT.◀

4.151 ▶If the A key is pressed and the format is synchronous, the message SYNC CHAR=?? # OF CHAR=? (1-3) appears. The expected receive sync character is entered from the keyboard along with the number (1, 2, or 3) of sync characters required to determine sync. For the asynchronous format, the above message does not appear.◀

4.152 ▶Assuming that this is the first time through the program (this is not a reedit), or, if zero trap characters were selected the last time through the program, the message SELECT 0000 TO 0020 TRAP CHAR will be displayed, followed by ???? TRAP CHARACTERS. If the user enters from 0001 to 0020, the display 00:?? ?? ... ?? appears. The operation at this point is the same as for the transmit character entry explained in paragraphs 4.146 through 4.148. After the last trap character has been entered, the message A TO START OR ← TO EDIT TRAP appears. On the other hand, if receive trap characters were previously entered (this is a reedit), only the last message A TO START OR ← TO EDIT TRAP appears.◀

4.153 ▶Consider again the message ???? TRAP CHARACTERS. When 0000 is entered, the message NO TRAP CHARACTERS ARE ENTERED appears followed by PRESS A TO START.◀

4.154 ▶To edit trap characters, proceed as indicated in paragraph 4.150 except that the message displayed after exit from the edit mode is A TO START OR ← TO EDIT TRAP.◀

4.155 ▶When the A key is pressed, RS goes ***on,*** and the transmit message will be transmitted when CS goes ***on***. (If a CSU is in use, the DTS does not look for a CS ***on*** indication before sending the message.) Simultaneously, the following messages will appear, although they may last for extremely short intervals and not be visible on the display.◀

4.156 ▶With a synchronous format, the message WAITING FOR SYNC appears until sync is detected. This message does not appear with an asynchronous format. If at least one trap character was entered, the message WAITING FOR TRAP appears. The waiting messages will remain on the display indefinitely while searching for the sync or trap characters, respectively. In order to terminate either search, the D key is pressed causing the message ← TO REEDIT, A TO RETRMT, D TO RESTART to appear. One of three functions can be performed from this point. The first function is to reedit the user programmable message or to reenter another standard message. If a user programmable message had been entered,

TABLE O

STANDARD MESSAGES

MESSAGE NUMBER	TERMINAL	TEST	PROMPTING MESSAGE
01	40/4	EBCDIC Selection	SSA=?? ??, DA=?? ??
02	40/4	EBCDIC Polling	SPA=?? ??
03	40/4	EBCDIC Printer AMZZ	
04	40/4	ASCII Selection	SSA=?? ??, DA=?? ??
05	40/4	ASCII Polling	SPA=?? ??
06	40/4	ASCII Printer AMZZ	
07	40/1,/2,/3	Full ASCII	
08	40/1,/2,/3	132 Column Lines	
09	40/1,/2,/3	Edit (Part 1)	
10	40/1,/2,/3	Edit (Part 2)	
11	40/1,/2,/3	Tabs	
12	40/3	Fox	FDX INT=??, ETX OR EOT=??
13	40/1,/2,/3	Options	
14	40/1,/2,/3	RO	
15	40/1,/2,/3	Special Options (Part 1)	
16	40/1,/2,/3	Special Options (Part 2)	
17	40/1,/2,/3	Printer AMZZ	

and ← is pressed, the program returns to the point in the program indicated by the message A TO CONTINUE OR ← TO EDIT TRMT. Alternately, if a standard message was entered and ← is pressed, the program returns to the point in the program indicated by the message STANDARD MSG NUMBER=?? (01-17). The second function is to retransmit the user programmable message or the standard message. If A is pressed, the transmit/receive operation is repeated and the program returns to the point in the program where A was pressed to start (paragraph 4.155). The third function is to restart the test by entering all new data. If D is pressed, the program returns to the point in the program indicated by the message 1=PROGRAMMABLE 2=STANDARD MSG (paragraph 4.146).

4.157 Assume that the sync character (if synchronous) and the trap sequence (if not zero trap) are detected. If ten or less trap characters were selected, line 00 : will be displayed with tildes between hex pairs. For example, assuming 6 trap characters, the display would be 00:XX~XX~XX~XX~XX~XX. If 11 to 20 trap characters were selected, line 01: will be displayed with tildes between hex pairs. For example, assuming 13 trap characters, the display would be 01:XX~XX~XX, displaying the last 3 received trap characters. After approximately 1 second, and each second thereafter, the display would be updated to include any received log characters up to a maximum of 255 trap plus log characters. In the example, after 1 second, if 13 trap plus 122

log characters are received, the display would be 13:XX~XX~XX~XX~XX. When the trap plus log characters equal 255, the receive buffer is filled, and the first line is displayed without tildes, that is, 00:XX XX XX XX XX XX XX XX XX XX. If less than 255 trap plus log characters are received, the display update will change only with further input data and the display will show the latest update with tildes. To manually terminate the accumulation of log characters, the C key is pressed causing the first line to be displayed without tildes, as previously stated. Note that the number of characters stored in the receive buffer is something less than 255.◀

4.158 ▶On the other hand, assume that the sync character(s) (if synchronous) has been detected but there are zero trap characters. The display will indicate 00 : and update immediately after the reception of each of the first five or ten characters. (Five characters for speeds above 4800 b/s and ten characters for speeds less than or equal to 4800 b/s). There is no 1 second update interval for the first five or ten log characters. After the first five or ten log characters are received, the operation is identical to that for nonzero trap characters as explained in paragraph 4.157.◀

4.159 ▶With the tildes omitted from the display, the received data can be scrolled. The operator can look at any line of ten characters within the received message by using the B, C, E, and F keys. The first two digits specify the line number currently displayed. The function of these keys is as follows.

Key B, display previous line of characters

Key C, display first line of characters

Key E, display last line of characters

key F, display next line of characters.◀

4.160 ▶After scrolling, further action can be taken by pressing the A, D, or ← keys. The action is the same as described in paragraph 4.156.

Key A, repeat the transmit/receive operation

Key ←, reedit the transmit message or reenter a standard message, reenter sync characters, and reedit the trap sequence as required

Key D, restart the test by entering all new data.◀

4.161 ▶The editing mode can also be used during the initial entry of characters before the total number of characters has been reached. This is true for the entry of transmit or trap characters. Hence, if a mistake is recognized at any time during entry of characters, the ← key allows the user to correct the mistake by going to the edit mode. Characters can be deleted one at a time within a message while in the edit mode. As an example, suppose the seventh character (location 6) contains the hex digits AB which are to be deleted. After entering the edit mode and finding line 00, the display will be:

00:YY*YY*YY*YY*YY*YY*AB*22*YY*YY,

where AB is the character (location 6) to be deleted, 22 is the next character, and YY represents the other characters on the line. The user now presses 6 causing the AB to be replaced by ??. Next, the ← key is pressed deleting the two question marks, moving the 22 over to where the ?? was located, and shifting all following characters one position left. The hex digits in the extreme right position on the line are replaced by the hex digits in the extreme left position on the next line and so on until the rest of the message has moved one position to the left. Additional characters can also be deleted in a similar fashion.

Note: Whenever characters are deleted from a message, additional characters must be inserted at the end of a message such that the total number of characters in the message are equal to the number of characters selected by the user at the beginning of the test. The character FF (all ones) may be used as a fill character.◀

4.162 ▶When entering a message, if the mistakes in the entered characters are too numerous to correct conveniently, the entire message can be eliminated by pressing the D key while in the edit mode. If the D key is pressed, while editing a user programmable message, the display will show SELECT 0001 TO 0255 CHARACTERS, followed by ???? CHARACTERS IN MESSAGE. If the D key is pressed while editing a standard message,

the display will show 1=PROGRAMMABLE 2=STANDARD MSG. If the D key is pressed while editing trap characters, the display will show SELECT 0000 TO 0020 TRAP CHAR. The program will jump to the step given in paragraph 4.146 for the programmable or standard message and to the step given in paragraph 4.152 for trap character entry.◀

4.163 ▶Figure 17 is a flowchart of test code 58 indicating the displayed messages that the user would encounter while stepping through the program. Test code 58 will operate to 7200 bps for asychronous data and 9600 bps for synchronous data.◀

I. DDS Codes

4.164 These tests are performed only when a CSU is provided in DDS. The DTS can transmit and receive control codes to CSUs using bipolar violation format at all DDS speeds (2.4, 4.8, 9.6 and 56 kb/s).

Test Code 62—Zero Suppression

4.165 This is a full-duplex test during which the DTS is continuously sending a zero suppression code. At the same time, the DTS examines the received bipolar violation pattern expecting to receive the zero suppression code back. To initiate this test, enter test code 62, then press GO. The display reads ZERO: ENTERED=XX DROPPED=XX, indicating how may times (up to 99) the zero suppression mode was entered and how many times it was dropped. To enter the mode, three consecutive zero suppression bytes must be received. To drop out, two different consecutive bytes must be received.

4.166 If the DTS entered the mode one more time than dropped, it means that it is currently receiving the proper codes; for example, ZERO : ENTERED=01 DROPPED=00. If the number of times dropped equals the number of times entered, it means that the DTS is not currently receiving the proper code; for example, ZERO: ENTERED=01 DROPPED=01. The test is terminated by pressing GO.

Test Code 63—Idle

4.167 This is a full-duplex test during which the DTS is continuously sending the idle code. At the same time, the DTS examines the received bipolar violation pattern expecting to receive the idle code back. To initiate this test, enter test code 63, then press GO. The display reads, IDLE: ENTERED=XX DROPPED=XX, indicating how many times (up to 99) the idle mode was entered and how many times dropped. To enter the idle mode, three consecutive idle mode bytes must be received. To drop out of idle mode, two different consecutive bytes must be received.

4.168 If the DTS entered the mode one more time than dropped, it means that it is currently receiving the proper codes; for example, IDLE : ENTERED=02 DROPPED=01. If the number of times dropped equals the number of times entered, it means that the DTS is not currently receiving the proper code; for example, IDLE: ENTERED=02 DROPPED=02. The test is terminated by pressing GO.

Test Code 64—Out of Service

4.169 This is a receive-only function. The DTS does not transmit; it detects the out-of-service (OOS) code. To initiate the test, enter test code 64 and press GO. The display reads, OOS: ENTERED=XX DROPPED=XX, indicating how many times (up to 99) the OOS mode was entered and how many times dropped. To enter the mode, three consecutive OOS bytes must be received. To drop out of OOS mode, two different consecutive bytes must be received.

4.170 If the DTS entered the mode one more time than dropped, it means that it is currently receiving the proper codes; for example, OOS: ENTERED=03 DROPPED=02. If the number of times dropped equals the number of times entered, it means that the DTS is not currently receiving the proper code; for example, OOS: ENTERED=03 DROPPED=03. The test is terminated by pressing GO.

Test Code 65—Not Ready

4.171 This is a transmit-only function used on the switched DDS. The DTS continuously transmits the NOT READY (CSA) bipolar violation code toward the network until interrupted by the GO key.

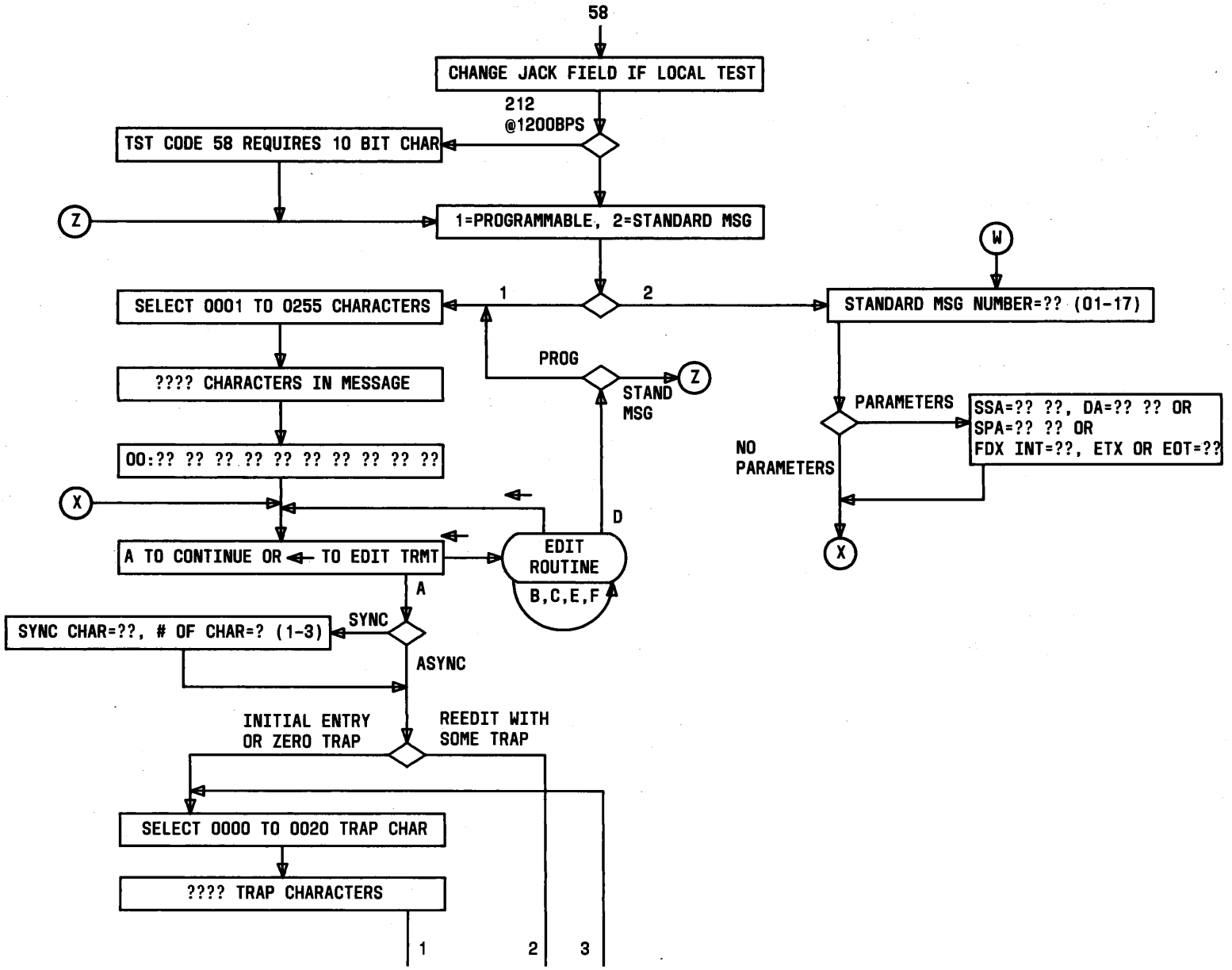


Fig. 17—Flowchart of Test Code 58 (Sheet 1 of 2)

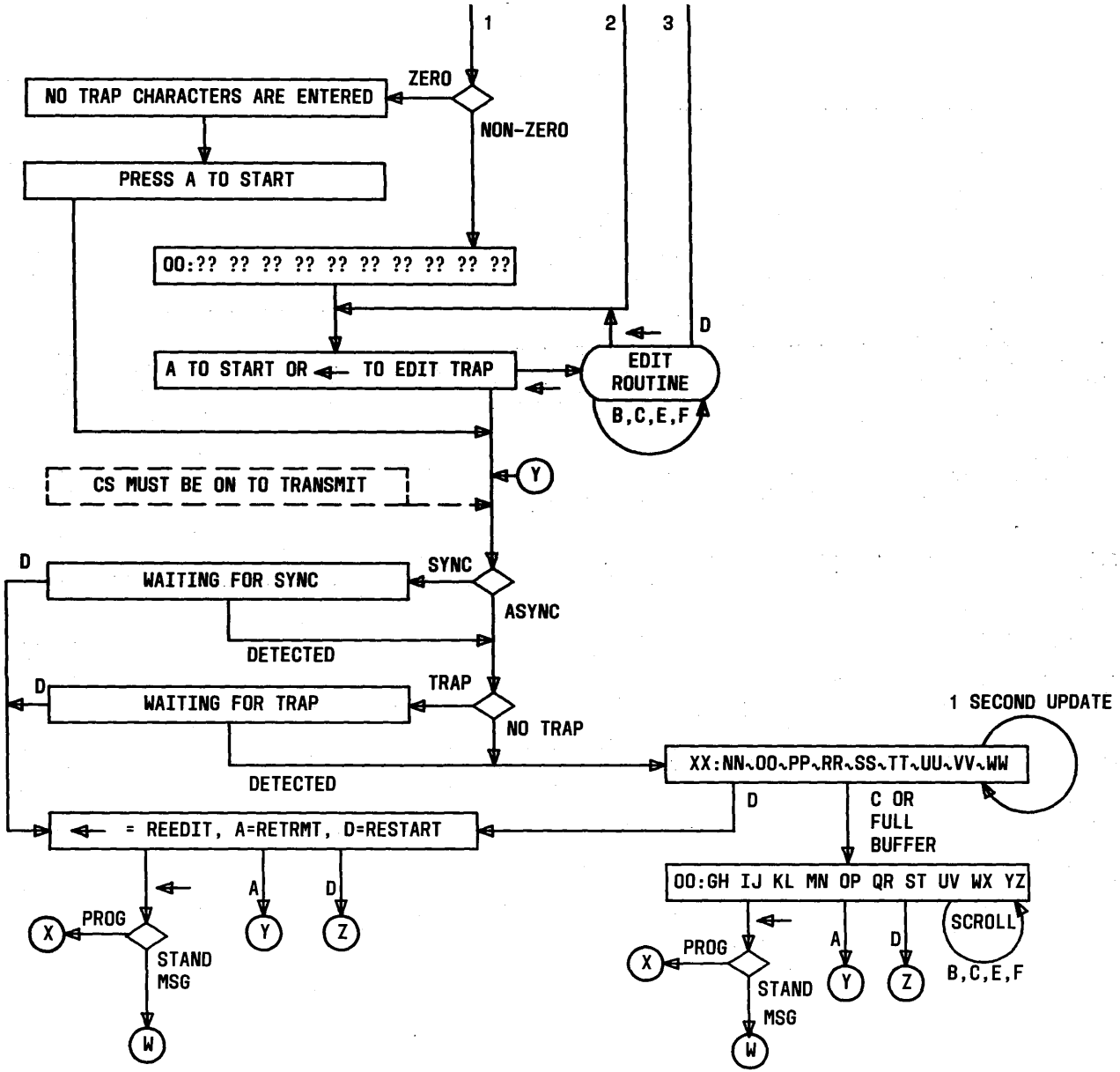


Fig. 17—Flowchart of Test Code 58 (Sheet 2 of 2)

J. Start-Up Tests

4.172 The start-up tests measure the error performance of a data channel in the transient state. The tests are intended primarily for polling networks where short bursts of data are frequently transmitted. A start-up test typically measures the error performance of a data channel during a short time interval immediately after a data set indicates the channel is ready for data transmission.

> ***Note 1:*** The start-up tests are intended to be used on data channels which use a synchronous-type data set.
>
> ***Note 2:*** Certain options may be required for a specific data set. See the appropriate data set BSP for more information about options for the start-up test.

4.173 During an end-to-end start-up test, a DTS at one location sends a short message (128 bits) to a second location. The DTS at the second location records whether the block it receives contains any errors. If the test is a 2-way test, the DTS at the second location then sends a short message back to the first location. The DTS at the first location records whether the block received contains any errors. This sequence may be repeated under either manual control or automatic control. The start-up test may also be performed with data sets that have been looped back.

4.174 The 128-bit message may be either the standard message of the DTS or an operator-defined (programmable) message keyed into the test set just prior to performing the test. The standard message of the DTS (in ASCII) is SYN SYN SOH 123 STX START-UP ETX. The programmable message must be encoded into a hexadecimal format before being inputted to the test set. Hexadecimal conversions are given in Table M.

> ***Note:*** The last two characters cannot both be programmed as hexadecimal FF.

4.175 The programmable message can be used when performing a start-up test with the customer's far-end terminal. In addition, the DTS may be used to monitor a 128-bit message transmitted between customer terminals.

4.176 During an end-to-end start-up test, the DTS at one location is the controlling station and the DTS at the other location is the controlled station (Fig. 18). If both stations operate switched carrier, then either station may be specified as controlling or controlled station (as in DDD operation). If one station operates continuous carrier (RS continuously ***on***) and the other station operates switched carrier, then the continuous carrier station must be specified as controlling and the switched carrier station must be specified as controlled (as in a multipoint polling network).

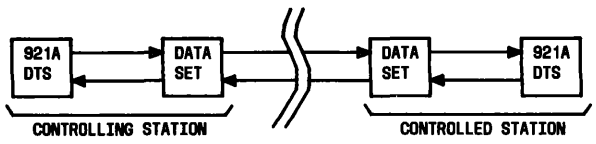


Fig. 18—Start-Up Test Configuration

4.177 The controlling station initiates, and can reinitiate, the test (it controls the test by determining when a message is to be sent), and the controlled station responds only when it receives signals from the controlling station. The DTS at the controlling station uses test code 67 for the standard message and test code 70 for the programmable message. The DTS at the controlled station uses test code 68 for the standard message and test code 71 for the programmable message.

4.178 Three types of start-up tests can be performed:

(1) One-Way

(2) Inquiry Response Switched Carrier (IR SW)

(3) Inquiry Response Continuous Carrier (IR CONT).

This type of test is selected after the appropriate test code is entered and the GO key is pressed.

4.179 In all tests except for the Controlling Station (IR-CONT), the data sets must be optioned for switched carrier operation. In the IR-CONT test, only the controlling station may be optioned for RS continuously ***on.*** See paragraph 4.176 for

a definition of controlling stations and controlled stations.

4.180 Keys A, C, and D provide the functions shown in Table E for the above three types of start-up tests. Key A starts or reinitiates the start-up test selected; key C clears the display; and key D stops the test but does not clear the display. The same test may be resumed by pressing key A.

4.181 During the start-up test, the DTS stores all of the data it receives and then attempts to gain character synchronization by examining the data stored most recently (data sent last). This allows the DTS to gain character synchronization even if the first few characters in the received message have start-up errors. This is explained in detail in paragraph 4.182.

4.182 Once all of the received data have been stored, they are examined in order to gain character synchronization. This is done by first examining the last 16 bits (two characters) received and comparing them to the last 16 bits of the expected message. If a match is not found, the search is repeated starting one bit earlier. Thus, the net effect is to search backward through the received data until a match is found to the last 16 bits of the expected message. In this method of search, the last two characters of the expected message are the synchronization characters. Once the match is found, character synchronization has been achieved. The advantage of this type of search is that start-up errors in the first few characters of the message do not prevent the achievement of character synchronization by the DTS.

One-Way Test

4.183 In the one-way test, the controlling station transmits a message and the controlled station receives the message.

4.184 One cycle of the one-way test is described as follows. The DTS at the controlling station initiates the test by turning RS ***on***. When the data set responds by turning CS ***on***, the 128-bit message is transmitted, RS is turned ***off***, and the controlling station updates the display. The DTS at the controlled station stores all data received while RLSD is ***on***. When RLSD is turned ***off***, the DTS examines the stored data for the 128-bit message and then updates the display.

Test Code 67—Standard Message, Controlling — One-Way Test

4.185 Enter test code 67 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of the three types of start-up tests is to be selected. For the one-way test, press key 1 and the display indicates TRMT: 1=MAN 2=TIMED.

4.186 At this time, a selection must be made whether the test is to be performed in a manual or automatic timed mode. Pressing key 1 conditions the DTS to initiate the cycle described in paragraph 4.184 each time key A is pressed. Pressing key 2 conditions the DTS to initiate the cycle described in paragraph 4.814 once every second. Pressing either key 1 or 2 causes the display to read PRESS A TO START.

> ***Note:*** Before pressing key A to initiate transmission, the controlled station must be initialized and waiting to receive data. See paragraphs 4.190 and 4.191.

4.187 Pressing key A displays BLK TRMT=XXXX *XXXX. The controlling station then initiates one cycle of the test by turning RS ***on***. As soon as the data set responds by turning CS ***on***, the controlling station sends the 128-bit message and then turns RS ***off***.

4.188 The display for the controlling station indicates the number of blocks of data it transmits (BLK TRMT=XXXX) and the number of blocks it unsuccessfully attempts to transmit (*XXXX).

4.189 Every time the controlling station turns RS ***on*** to transmit a block of data, it must receive an ***on*** condition from the data set on the CS lead to indicate the channel is ready for data transmission. Since a block of data is sent out as soon as CS goes ***on***, the counter indicating the block transmitted (BLK TRMT=XXXX) is progressed when CS goes ***on***. When CS does not go ***on*** in response to RS, the block of data is not transmitted and the counter is not progressed. However, since the controlling station waits for CS to go ***on*** until a new cycle is initiated (either manually or timed), the counter indicating the

number of unsuccessful attempts (*XXXX) to transmit a block of data is not progressed until a new cycle is initiated.

Test Code 68—Standard Message, Controlled—One-Way Test

4.190 Enter test code 68 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of the three types of start-up tests is to be selected. For a one-way test, press key 1 and the display should indicate PRESS A TO START. If RLSD is ***on***, the display indicates RLSD MUST BE OFF TO START. When RLSD goes ***off***, the display indicates PRESS A TO START.

4.191 After PRESS A TO START is displayed, press A to prepare the controlled station to receive data. The message BLK RCVD=XXXX ERR=XXXX *XXXX is displayed.

4.192 The controlled station then waits for RLSD to turn ***on***. When RLSD turns ***on***, the DTS starts placing data into its memory buffer. All data received while RLSD is ***on*** is stored in the memory buffer. As soon as RLSD turns ***off***, the stored data are examined to determine if the 128-bit sequence has been received without errors. The display is then updated to indicate that a block has been received (BLK RCVD=XXXX). The block error counter is also updated if the block contained an error (ERR=XXXX). For every error recorded by the DTS an output pulse will appear on the front panel test point labeled ERRORS. Improper operation causes the trouble counter (*XXXX) to be progressed.

4.193 The trouble counter (*XXXX) is progressed whenever the capacity of the memory buffer used to store received data is exceeded. This buffer can store 4000 bits. If the trouble counter is progressed, the BLK RCVD and ERR counters do not progress.

Test Code 70—Programmable Message, Controlling—One-Way Test

4.194 Enter test code 70 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of start-up tests is to be selected. For the one-way test, press key 1 and display indicates ENTER HEX CHARS followed by ???.....???.

4.195 At this time, the programmable message is entered by the 16 alphanumeric keys. The 128-bit message is partitioned into sixteen 8-bit characters. The characters must be encoded hexadecimally (Table P). Each 8-bit character (two hexadecimal digits) is inputted by pressing two of the keys. The 8-bit character entered first (first two hexadecimal digits) will be transmitted first and will be followed by the remaining 15 characters in the order of entry. After all 32 hexadecimal digits have been entered, the message TRMT: 1=MAN 2=TIMED appears.

TABLE P

HEXADECIMAL TO BINARY, OCTAL, AND DECIMAL CONVERSION

HEX	BINARY	OCTAL	DECIMAL
0	0000	00	0
1	0001	01	1
2	0010	02	2
3	0011	03	3
4	0100	04	4
5	0101	05	5
6	0110	06	6
7	0111	07	7
8	1000	10	8
9	1001	11	9
A	1010	12	10
B	1011	13	11
C	1100	14	12
D	1101	15	13
E	1110	16	14
F	1111	17	15

4.196 Perform steps indicated in paragraphs 4.186 through 4.189.

Test Code 71—Programmable Message, Controlled—One-Way Test

4.197 Enter test code 71 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of start-up tests is to be selected. For the one-way test, press key 1 and display indicates ENTER HEX CHARS followed by ???.....???.

4.198 At this time the programmable message (same message that is to be inputted at the controlling station) is entered by the 16 alphanumeric keys as described for test code 70. After all 32 hexadecimal digits have been entered, the display should indicate PRESS A TO START. If RLSD is ***on***, the display indicates RLSD MUST BE OFF TO START. When RLSD goes ***off***, the display indicates PRESS A TO START.

4.199 Perform steps indicated in paragraphs 4.191 through 4.193.

4.200 An application of test code 71 for on-line start-up monitoring is given in paragraphs 5.04, 5.05, and 5.06.

Inquiry Response, Switched Carrier Test (IR SW)

4.201 The IR SW test is a 2-way test. Both controlling and controlled stations transmit the same 128-bit message to each other. This test simulates data communication on the DDD network since the carrier operates on a switched basis in both directions. One cycle of the IR SW test is described in paragraph 4.202.

4.202 The controlling station DTS initiates the test by turning RS ***on***. When the controlling station DTS receives an ***on*** condition from the data set CS lead, the 128-bit message is transmitted, RS is turned ***off***, and the controlling station waits for RLSD to go ***on***. At the controlled station, all data is stored while RLSD is ***on***. When RLSD is turned ***off***, the DTS examines the stored data for the 128-bit message and updates the display. The controlled station then turns RS ***on***, transmits the 128-bit message when CS is turned ***on*** by the data set and then turns RS ***off***. The controlling station then stores all data received while RLSD is ***on***, examines the stored data for the 128-bit message, and updates the display.

Test Code 67—Standard Message, Controlling—Inquiry Response Switched Carrier Test

4.203 Enter code 67 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these three types of tests is to be selected. For an IR SW test, press key 2 and display indicates TRMT: 1=MAN 2=TIMED 3=SW CARR.

4.204 At this time, a selection must be made whether the test is to be performed in a manual, automatic timed or automatic switched carrier mode. Pressing key 1 conditions the DTS to initiate the cycle described in paragraph 4.202 each time key A is depressed. Pressing key 2 conditions the DTS to initiate the cycle described in paragraph 4.202 once each second. Pressing key 3 conditions the DTS to initiate the cycle described in paragraph 4.202 each time RLSD goes from ***on*** to ***off***. This mode (SW CARR) allows the cycle to be repeated at a much faster rate than once every second. When key 1, 2, or 3 is pressed, the display indicates PRESS A TO START.

> ***Note 1:*** In the switched carrier mode, a possible lockup condition exists where both stations are waiting for RLSD to change state in order to transmit a message. As long as nothing disturbs the system and one station turns RS ***on*** while the other waits for RLSD to go ***on*** there is no lockup. However, if (due to noise or some other disturbance) one of the stations misses the change of state of the RLSD lead, then both stations would end up waiting for an ***off***-to-***on*** transition on the RLSD leads. The two stations would remain in this locked-up state (neither station transmitting a message) until the test cycle is manually reinitiated (by pressing key A) at the controlling station. This lockup condition cannot occur in the automatic timed mode because the controlling station reinitiates the test once every second regardless of conditions at the interface leads.
>
> ***Note 2:*** Before pressing key A to initiate transmission, the controlled station must be initialized and waiting to receive data. See paragraphs 4.209 and 4.210.

4.205 Pressing key A displays BLK RCD=XXXX ERR=XXXX *XXXX. The controlling station then initiates the test by turning RS ***on***. When the data set responds, CS goes ***on***, the DTS sends the 128-bit message and turns RS ***off***. It then waits for RLSD to turn ***on***. After the controlled station has received a block of data, it sends the 128-bit message back to the controlling station. At that time, the RLSD lead at the controlling station turns ***on***.

4.206 When RLSD turns ***on***, the controlling station DTS starts placing data into its memory

buffer which stores all of the data received while RLSD is ***on***. As soon as RLSD goes ***off***, the stored data are examined to determine if the 128-bit sequence has been received without errors. The display is then updated to indicate that a block has been received (BLK RCVD=XXXX). The block error counter is also updated if the block contained an error (ERR=XXXX). For every error recorded by the DTS, an output pulse will appear on the front panel test point labeled ERRORS. Improper operation causes the trouble counter (*XXXX) to be progressed.

4.207 The trouble counter is progressed when one of the following conditions exists. The 4000-bit memory buffer which stores received data overflows; a new cycle of the test is initiated (manually or on a timed basis) and the controlling station has not detected its RLSD lead go ***on***; a new cycle of the test is initiated (manually or on a timed basis) and the controlling station has detected its RLSD lead go ***on*** but not ***off***. If the trouble counter is progressed, the BLK RCVD or ERR counters do not progress.

4.208 An application of test code 67 (IR SW) for loopback testing a data set is given in paragraphs 5.07 and 5.08.

Test Code 68—Standard Message, Controlled—Inquiry Response Switched Carrier Test

4.209 Enter test code 68 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of the three types of tests is to be selected. For IR SW test, press key 2 and the display should indicate PRESS A TO START. However, if RLSD is ***on***, the display indicates RLSD MUST BE OFF TO START. When RLSD goes ***off***, the display indicates PRESS A TO START.

4.210 After the PRESS A TO START message is displayed, the controlled station is prepared to receive data by pressing key A. At this time BLK RCVD=XXXX ERR=XXXX *XXXX is displayed.

4.211 The controlled station then waits for RLSD to go ***on***. When RLSD goes ***on***, it starts inputting data to its memory buffer and stores all data received while RLSD is ***on***. As soon as RLSD goes ***off***, the stored data are examined to determine if the 128-bit sequence has been received without errors. The display is then updated to indicate that a block has been received (BLK RCVD=XXXX). The block error counter is also updated if the block contained an error (ERR=XXXX). Improper operation causes the trouble counter (*XXXX) to be progressed.

4.212 The trouble counter (*XXXX) is progressed whenever the 4000-bit capacity of the memory buffer used to store received data is exceeded. If the trouble counter is progressed, the BLK RCVD and ERR counters do not progress.

4.213 After the controlled station updates its counters, it responds to the 128-bit inquiry message by turning RS ***on***, waiting for the data set to respond by turning CS ***on***, and sending the same 128-bit message back to the controlling station. It then turns RS ***off*** and waits for RLSD to go ***on*** which indicates another message from the controlling station.

4.214 At the controlled station the cycle described in paragraphs 4.211 and 4.213 is repeated each time the controlling station transmits another block of data.

Test Code 70—Programmable Message, Controlling—Inquiry Response Switched Carrier Test

4.215 Enter test code 70 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of tests is to be selected. For the IR SW test, press key 2 and display indicates ENTER HEX CHARS followed by ???....???.

4.216 At this time, the programmable message is entered by the 16 alphanumeric keys. The 128-bit message is partitioned into sixteen 8-bit characters. The characters must be encoded hexadecimally (Table P). Each 8-bit character (two hexadecimal digits) is inputted by pressing two keys. The 8-bit character entered first (first two hexadecimal digits) will be transmitted first and will be followed by the remaining 15 characters in the order of entry. After all 32 hexadecimal digits have been entered, the message TRMT: 1=MAN 2=TIMED 3=SW CARR appears.

4.217 Perform the steps indicated in paragraphs 4.204 through 4.207.

4.218 An application of test code 700 (IR SW) for loopback testing a data set is given in paragraphs 5.07 and 5.08.

Test Code 71—Programmable Message, Controlled—Inquiry Response Switched Carrier Test

4.219 Enter test code 71 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of tests is to be selected. For the IR SW test, press key 2 and display indicates ENTER HEX CHARS followed by ???....???.

4.220 At this time the programmed message (same message that is to be inputted at the controlling station) is entered by the 16 alphanumeric keys as described in paragraph 4.216. After the 32 hexadecimal numbers have been entered, the display should indicate PRESS A TO START. If RLSD is ***on***, the display indicates RLSD MUST BE OFF TO START. When RLSD goes ***off***, the display indicates PRESS A TO START.

4.221 Perform steps indicated in paragraphs 4.210 through 4.213.

Inquiry Response, Continuous Carrier Test (IR CONT)

4.222 The IR-CONT is a 2-way test. Both the controlling and controlled stations transmit the same 128-bit message to each other. This test simulates the data communication on one circuit of a private line polled network since the carrier is continuously ***on*** in one direction and switched in the other. One cycle of the IR CONT test is described in paragraph 4.223.

4.223 RS is ***on*** continuously at the controlling station. The controlling station holds SD in the marking condition prior to initiating the test. To initiate a test, the controlling station sends its 128-bit message, returns SD to the marking condition, and then waits for RLSD to go ***on***. The controlled station starts storing data at the first mark-to-space transition of RD. All data received for 300 ms immediately following the first transition are stored. At the end of this time, the stored data are examined for the 128-bit message and the controlled station updates the display. The controlled station turns RS ***on***, transmits the 128-bit message when CS lead is turned ***on***, and then turns RS ***off***. The controlling station stores all data received while RLSD is ***on***, examines the stored data for the 128-bit message, and then updates the display.

Test Code 67—Standard Message, Controlling—Inquiry Response Continuous Carrier

4.224 Enter test code 67 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these three types of tests is to be selected. For an IR CONT test, press key 3 and the display indicates TRMT: 1=MAN 2=TIMED 3=SW CARR. The RS lead will go ***on*** at this time and stay ***on*** for the duration of the test.

4.225 At this time, a selection must be made whether the test is to be performed in manual, automatic timed, or automatic switched carrier mode. Pressing key 1 conditions the DTS to initiate the cycle described in paragraph 4.223 each time key A is pressed. Pressing key 2 conditions the DTS to initiate the cycle once each second. Pressing key 3 conditions the DTS to initiate the cycle each time it detects the RLSD lead go from ***on*** to ***off***. The switched carrier mode allows the cycle to be repeated at a much faster rate than once each second. When key 1, 2, or 3 is pressed, the display PRESS A TO START appears.

> ***Note 1:*** In the switched carrier mode, a possible lockup condition exists where the controlling station is waiting for RLSD to change state in order to transmit a message, and the controlled station is waiting for a mark-to-space transition in order to transmit a message. As long as nothing disturbs the system and the controlling station sends a message while the controlled station is looking for a mark-to-space transition and the controlled station turns RS ***on*** while the controlling station waits for RLSD to go ***on***, there is no lockup. However, if (due to noise or some other disturbance) this cycle is interrupted, then both stations could end up waiting for the other station to initiate a transmission. The two stations would remain in this locked-up state (neither station transmitting a message) until the cycle is manually reinitiated by pressing key A at the controlling station. This lockup condition could not occur in the automatic-timed mode because the controlling

station reinitiates the test once every second, regardless of conditions at the interface leads.

Note 2: Before pressing key A to initiate transmission, the controlled station must be initialized and waiting to receive data as described in paragraphs 4.229 and 4.230.

4.226 Pressing key A displays BLK RCVD=XXXX ERR=XXXX *XXXX. The controlling station then initiates the test by sending the 128-bit message and waits for RLSD to go ***on***. After the controlled station has received a block of data it, in turn, sends the 128-bit message back to the controlling station. RLSD at the controlling station goes ***on***.

4.227 When the controlling station detects RLSD on, it starts inputting data into its memory buffer. It stores all of the data received while RLSD is ***on***. As soon as RLSD goes ***off***, the stored data are examined to determine if the 128-bit sequence has been received without errors. The display is then updated to indicate that a block has been received (BLK RCVD=XXXX). The block error counter is also updated if the block contained an error (ERR=XXXX). For every error recorded by the DTS, an output pulse will appear on the front panel test point labeled ERRORS. Improper operation causes the trouble counter (*XXXX) to be progressed.

4.228 The trouble counter is progressed when one of the following conditions exists: the 4000-bit memory buffer, which stores received data, overflows; a new cycle of the test is initiated (manually or on a timed basis) and the controlling station has not detected RLSD go ***on***; or a new cycle of the test is initiated (manually or on a timed basis) and the controlling station has detected RLSD go ***on*** but not ***off***. If the trouble counter is progressed, the BLK RCVD or ERR counters do not progress.

Test Code 68—Standard Message, Controlled—Inquiry Response Continuous Carrier

4.229 Enter test cost 68 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of the three types of tests is to be selected. For an IR CONT test, press key 3 and display will indicate PRESS A TO START. If RD is 0 (space), the display will indicate RD MUST BE 1 TO START. When RD goes from 0 to 1 (space to mark), the display indicates PRESS A TO START. After the PRESS A TO START message is displayed, the controlled station is prepared to receive data by pressing key A. At this time the display will show BLK RCVD=XXXX ERR=XXXX *XXXX.

4.230 The controlled station waits for RD to go from mark to space. The first mark-to-space transition at the controlled station causes the DTS to begin storing data. All data received for 300 ms immediately following the first transition are stored. At the end of this time, the stored data are examined to determine if the 128-bit message has been received without error. The display in the DTS is then updated to indicate that a block has been received (BLK RCVD=XXXX). The block error counter is also updated if the block contained an error (ERR=XXXX). For every error recorded by the DTS, an output pulse will appear at the front panel test point labeled ERRORS. Improper operation causes the trouble counter (*XXXX) to be progressed.

4.231 The trouble counter (*XXXX) is progressed whenever the 4000-bit capacity of the memory buffer used to store received data is exceeded. If the trouble counter is progressed, the BLK RCVD and ERR counters do not progress.

4.232 After the controlled station updates its counters, it responds to the 128-bit inquiry message by turning RS ***on***, waiting for the data set to respond with CS going ***on***, and then sending the same 128-bit message back to the controlling station. It then turns RS ***off*** and waits for a mark-to-space transition on RD as an indication of another message from the controlling station.

4.233 At the controlled station, the cycle described in paragraphs 4.230 and 4.231 is repeated each time the controlling station transmits another block of data.

Test Code 70—Programmable Message, Controlling—Inquiry Response Continuous Carrier

4.234 Enter test code 70 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of start-up tests is to be selected. For the inquiry response continuous (IR CONT) test, press key 3 and the

display indicates ENTER HEX CHARS followed by ???.....???. At this time, RS goes ***on*** and stays ***on*** for the duration of the test.

4.235 The programmable message is now entered by the 16 alphanumeric keys. The 128-bit message is partitioned into sixteen 8-bit characters. The characters must be encoded hexadecimally (Table P). Each 8-bit character (two hexadecimal digits) is inputted by pressing two keys. The 8-bit character entered first (first two hexadecimal digits) will be transmitted first and will be followed by the remaining 15 characters in the order of entry. After all 32 hexadecimal digits have been entered, the message TRMT: 1=MAN 2=TIMED 3=SW CARR appears.

4.236 Perform steps indicated in paragraphs 4.225 through 4.228.

Test Code 71—Programmable Message, Controlled—Inquiry Response Continuous Carrier

4.237 Enter test code 71 and press GO. Display shows 1=ONE WAY 2=IR SW 3=IR CONT, indicating that one of these types of tests is to be selected. For the inquiry response continuous (IR CONT) test, press key 3 and display indicates ENTER HEX CHARS followed by ???....???.

4.238 At this time the programmed message (same message that is to be inputted at the controlling station) is entered by the 16 alphanumeric keys as described in paragraph 4.235. After all 32 hexadecimal digits have been entered, the display should indicate PRESS A TO START. If RD is 0 (space), the display indicates RD MUST BE 1 TO START. When RD goes from 0 to 1 (space to mark), the display indicates PRESS A TO START.

4.239 After A is pressed, operation proceeds as indicated in paragraphs 4.230 through 4.233.

K. Distortion Tests

Test Code 78—Isochronous Distortion

4.240 This measurement is required at CSU locations. It provides a measure of timing jitter associated with the customer receive or transmit data signal. Isochronous distortion tests can be made at all DDS speeds (2.4, 4.8, 9.6 and 56 kb/s) and can only be performed on CSUs.

4.241 To initiate the test, enter test code 78 and press GO. Until enough data is gathered for the first measurement, the message ISO DIS LE= % PULSE= % is displayed. When the first measurement becomes available, the blanks are filled in and LE (leading edge) may change to TE (trailing edge).

> ***Note:*** The interval between measurements or display updates may be as long as 20 seconds. To indicate that the test is in progress, assignable LED 1 will be flashing.

4.242 The first measurement (ISO DIS LE=XX%) gives the isochronous distortion in terms of percentage of data bit width. It also identifies whether LE or TE is associated with the greater distortion for the present measurement sample. The second measurement (PULSE=XX%) gives the median pulse width of the data pulses.

> ***Note:*** An * may appear as the first character in the above message. This is a result of receiving, during one measurement interval, 25 or more pulses classified by the DTS as invalid and discarded from the measurement. Such invalid pulses of 1000 or more will result in the display EXCESS DP (where DP means discarded pulses).

4.243 The ISO DIS LE=XX% PULSE=XX% is called the normal display. Another display, referred to as the extended display, is available by pressing B on the keyboard (Table E). Allow a time delay of one measurement interval (up to 20 seconds) for the extended display to appear. The extended display provides further information concerning the nature of the distortion. For example, there may be many discarded pulses as a result of impulse noise, yet the isochronous distortion reading may be low. The extended display is LE=XX% TE=XX% MAX=XX% DP=XXXXX. Both LE and TE distortions are displayed for the most recent measurement and, in addition, a maximum isochronous distortion reading computed over the entire test period is displayed. The counter DP=XXXXX shows the number of discarded pulses during the most recent measurement. To return to the normal display, press A. To clear the results of either the normal or extended

display, press key C. To terminate the test, press GO.

4.244 An application of test code 78 for monitoring the isochronous distortion of the transmit data signal is given in paragraph 5.09.

Test Code 79—Start-Stop Distortion

Version 1 Only

4.245 This is a signal distortion measurement made on the received data signal for asynchronous, start-stop systems. The transmitter can be another 921A, a 911NA DTS, a DATASPEED 40 terminal or any device which transmits the start-stop formatted data. Three measurements are simultaneously performed on the received data signal:

- Peak percent gross distortion
- Count of hits that equals or exceeds a threshold
- Average bias distortion.

4.246 The peak percent distortion is the largest amount of distortion (from 1 to 50 percent) encountered throughout the entire test interval. "Hits" are those distortion values which equal or exceed a specified threshold. The hit threshold is specified by the user after test code 79 is entered. The threshold can range from 0 to 49%.

4.247 The average bias distortion is computed and displayed every 256 data transitions. These measurements are usually done on an end-to-end basis. The far-end may be transmitting the FOX message (test code 52) or any other start-stop formatted characters consisting of eight bits plus one start and one or more stop bits.

> ***Note:*** The RS lead is not affected by this test. Therefore, if the DTS is expected to operate in a receive-only mode, RS must be turned ***off*** (test code 36) prior to execution of test code 79.

4.248 To initiate a start-stop distortion test, enter test code 79. The prompting message : 79 HITS OVER ??% appears. Enter a number (threshold) from 00 to 49. A hit is registered whenever the distortion equals or exceeds the specified threshold number. This should be a number consistent with the maximum distortion objective set for a particular data set. Press GO. Now the display will show ???? SECONDS. Enter the time duration (in seconds) for running this test. At the end of the specified interval, the test will terminate automatically. The DTS will cycle through two messages: TEST COMPLETE and PEAK=XX% HITS=XX/XX AVG BIAS=XX%. For an untimed test, enter 9999 for the time duration. The test is now started and the results are displayed as follows: PEAK=XX% HITS=XX/TH AVG BIAS=XX%. PEAK represents the peak gross distortion (00%-50%), HITS is the number of hits (00 to 99 or OV if greater than 99) exceeding the specified threshold (shown as XX/XX) and AVG BIAS is the average bias distortion (00%-50%). In the display, HITS=XX/XX, the first pair of numbers defines the number of hits equal or exceeding the hit threshold, while the second pair defines the selected hit threshold. During the test, the display may be cleared by pressing key C. To terminate the test, press GO.

4.249 Test code 79 may be operated full duplex. See paragraph 5.10.

Versions 2 and 3

4.250 This test is similar to the start-stop distortion test for Version 1 with the added capability of performing in a full-duplex mode. Also, when testing 212-type data sets operating asynchronously at 1200 bps, a choice of nine or ten bits per character (includes one start and one stop bit) operation is available to the operator.

4.251 This is a signal distortion measurement made on the received data signal for asynchronous (start-stop) systems. The transmitter can be the same 921A, another 921A, a 911NA DTS, a DATASPEED 40 terminal or any device which transmits start-stop formatted data. Three measurements are simultaneously performed on the received signal:

- Peak percent gross distortion
- Count of hits exceeding a threshold
- Average bias distortion.

4.252 The peak percent distortion is the largest amount of distortion (from 1 to 50 percent) encountered throughout the entire test interval.

"Hits" are those distortion values which exceed a specified threshold. Such threshold (between 0 and 49 percent) is specified by the operator.

4.253 The average bias distortion is computed and displayed every 256 data transitions. These measurements are usually done on an end-to-end basis. The far-end may be transmitting the FOX message (test code 52) or any other start-stop formatted characters consisting of eight bits plus one start, and one or more stop bits. (This can be seven bits plus one start, and one or more stop bits for 212-type data sets.)

4.254 To initiate a start-stop distortion test, enter test code 79 and press GO. The message MODE=? (1=RCV 2=RCV & TRMT) appears. If 1 is pressed for receive only operation, RS is turned ***off***. If 2 is pressed for full-duplex operation, then test code 79 must be preceded by either test code 51 or 52. If 51 (Programmable Message-TRMT) is selected, then the programmed message will be transmitted continuously during the test. If 52 (FOX Message-TRMT) is selected, then the FOX message will be transmitted continuously during the test. RS is turned ***on*** only during the full-duplex test. (See paragraph 5.11 for full duplex operation.)

> ***Note:*** If a 212-type data set, operating asynchronously at 1200 bps is being tested, the mode display above will be preceded by BITS/CHAR=? (0=NINE 1=TEN). If this test is preceded by test code 51, ensure that the BITS/CHAR selection is compatible.

After the mode is chosen, the display will show HITS OVER??% (MAX=49%). Enter a number (threshold) from 00 to 49 above which any distortion count will be considered a hit. This should be a number consistent with the maximum distortion objective set for a particular data set. After the hit threshold has been selected, the display will show ???? SECONDS. Enter the time duration (in seconds) for running this test. At the end of the specified interval, the test will terminate automatically. The DTS will cycle through two messages: TEST COMPLETE and PEAK=XX% HITS=XX/XX AVG BIAS=XX%. For an untimed test, enter 9999 for the time duration. The test is now started and the results are displayed as follows: PEAK=XX% HITS=XX/XX AVG BIAS=XX%. PEAK represents the peak gross distortion (00%-50%), HITS is the number of hits (00 to 99 or OV if greater than 99) exceeding the specified threshold (shown as XX/XX) and AVG BIAS is the average bias distortion (00%-50%). In the display, HITS=XX/XX, the first pair of numbers defines the number of hits exceeding the threshold, while the second pair defines the selected bit threshold.

4.255 During the test, A, B, C, and D keys may be used to perform the following functions:

A key—pressing the A key clears the display, resets the time duration for the test, and restarts the test. In addition, for the full-duplex mode, transmission is stopped (RS ***off***) and then restarted (RS ***on***).

B key—pressing the B key causes the display to show the number of seconds remaining in the test.

C key—pressing the C key clears the distortion readings on the display.

> ***Note:*** In some cases erroneous readings may occur immediately after the test is started. If this happens, the C key should be pressed to clear the erroneous readings.

D key—pressing the D key terminates the test. The DTS cycles through the two messages previously described. The test may be restarted again by pressing the A key.

The GO key can be used to terminate the test at any time in order to advance to the next test selected by the user.

L. Data Services Tests

Test Code 80—DATAPHONE Select-a-Station (DSAS)

Versions 2 and 3

4.256 This test, using the EIA RS-232-C interface module, provides the capability to test the data station selector (DSS) via the selector control unit (SCU) located at the customer master station. Two DSS services are offered, sequential and addressable. Tests for the sequential offering are divided into those for automatic step DSS and controlled step DSS.

4.257 For an automatic step DSS three tests are provided: frame tone, cycle time, and a reset option test. For a controlled step DSS, three tests are provided: step to frame tone, number of ports per cycle, and step to a specific port. For an addressable DSS two series of tests are provided: addressing ports and sending control tone.

4.258 Refer to the section entitled Data Station Selector-J70180AA-TOP (598-083-106), for details of DSAS testing.

Test Code 83—Transaction III Network Testing

Versions 2 and 3

4.259 This test provides for testing the Transaction III Network at a polled terminal location. Six tests have been incorporated into Versions 2 and 3 DTS. Five of the tests are performed with the DTS replacing the customer owned and maintained (COAM) terminal, and the sixth is performed with the DTS bridging accross tip and ring with the COAM connected. Test 1 measures the poll characteristics including poll duration and access time. Test 2 tests the digital protocol by examining a series of reflected messages from TN. Test 3 measures the received signal power of a reflected message by using the multimeter within the DTS. Test 4 measures the mark and space frequencies of two messages reflected back by TN. Test 5 measures peak distortion, average bias distortion, and the number of times the distortion exceeds a threshold specified by the operator. Test 6 monitors received characters from TN by bridging across tip and ring of a COAM terminal.

4.260 Refer to the appropriate 590-series of TOP documents to TN test procedures.

M. Self-Tests

4.261 In addition to the automatic self-tests,, which are performed whenever the RST key is pressed, there are four manual self-tests. These manual tests are performed whenever a malfunction is suspected in one of the following major portions of the test set: the transmit/receive bit error test circuitry, multimeter, keyboard, display, LEDS or interface modules, and cables. These functions could not be included in the self-tests performed automatically at system reset since they require operator assistance.

Test Code 94—Loopback Error Test

4.262 This is identical to test 55, a full-duplex bit or block error test as selected by the operator. It is performed entirely internal to the DTS. The transmit data is automatically connected to the received data through the programmable cross-connect network and before the interface circuitry. Eight-bit errors or out-of-sync should be injected and must be recorded on the display if the DTS is operating properly. See test 55 for details of operation.

Test Code 95—Multimeter

4.263 A test is performed by the DTS on all three functions of the multimeter (ohmmeter, ac voltmeter, dc voltmeter). Enter test code 95 and press GO. The prompting message OPEN METER INPUT, PRESS A will appear. Ensure that there is nothing connected to either one of the two meter inputs and press A. While the DTS sequences through the test steps, the display reads TEST IN PROGRESS. In a Version 1 DTS, this is followed by either TEST PASSED or TEST FAILED message and then a TEST COMPLETE. In a Version 2 or 3 DTS, TEST COMPLETE is displayed if the test passes. If the test fails, the message MULT. TEST FAILED F=PROCEED remains displayed.

4.264 A multimeter failure normally does not prohibit the DTS from being used for other functions.

Test Code 96—Keyboard, Display, and LEDs

4.265 This tests each of the keys on the keyboard, each position of the display, and each LED on the front panel. Enter test code 96 and press GO. Observe that all 17 LEDs are lighted while the message PRESS 0 THRU 9, A THRU F appears on the display. Any LEDs that remain in the ***off*** state are defective. Press keys 0123456789ABCDEF in this exact order. Observe that each position in the display contains the most recently pressed key designation.

> ***Note:*** A deviation from the above order will cause the keyboard test to fail.

4.266 If all the above keys are functional, the message PRESS ← will follow. Press the ← key and observe the display for either a TEST PASSED or TEST FAILED indication followed by TEST COMPLETE.

Test Code 97—Interface Module and Cables

4.267 This test checks the interface module inserted in the interface module port and the cables connected to the DCE connector. A loopback connector (available in the cover) which corresponds to the interface being tested, must be used. There are three different loopback connectors provided, one for each interface module. The TNS module (Versions 2 and 3) can also be tested but does not require a loopback connector. The loopback connector may be inserted directly into the DCE connector, in which case only the interface module is tested. The loopback connector may also terminate the free end of one or more cables attached to the DCE connector. In this case, both the interface module and the cables are tested simultaneously. This last case allows testing of cables between the data set and the subscriber's equipment.

4.268 To initiate the test, insert the interface module under test and insure that the proper loopback connector is attached. Enter test code 97 and press GO. The DTS will identify the interface under test with either one of the following messages: RS-232-C INTERFACE BEING TESTED, V.35 INTERFACE BEING TESTED, 550 INTERFACE BEING TESTED, and in Versions 2 and 3, TN INTERFACE BEING TESTED. In Version 1, the DTS will proceed to test the appropriate interface and cables, indicate either TEST PASSED or TEST FAILED and then TEST COMPLETE. In Versions 2 and 3 DTS, TEST COMPLETE is displayed if the test passes. If the test fails, the message INTF. TEST FAILED F=PROCEED remains displayed. In either version, if no interface is inserted, a failure message will appear.

> ***Note 1:*** Insure that all interface module switches are in the TERM position except for CCITT switch Y/A which should be in the MON position.
>
> ***Note 2:*** In Version 1, test code 97 alters the internal clock settings of the 921A. If used during the course of data set testing, reenter the bit rate code by pressing the RST key. In Versions 2 and 3, the interval clock settings are restored, and resetting is not necessary.

4.269 In case of failure, the test should be repeated without the cables in an attempt to isolate the fault to either the cables or the interface module.

4.270 Another test of the EIA RS-232-C interface and cables is possible which provides some degree of fault isolation. Insert the EIA loopback connector at the cable end or at the DCE connector. Condition the DTS for data set code 20, any desired bit rate, and test code 55 (bit error test). When test code 55 prompting messages are displayed, enter 1 for TRANSMITTER=1, 2 for 2047 BIT ERROR TEST, 1 for BIT ERRORS, and 9999 for 9999 SECONDS. At this time, the DTS is transmitting the 2047-bit pattern and receiving the same pattern through the loopback connector. Because data set code 20 was selected, the DTS receiver is phase-locked to the transmitted data. If functioning properly, the display indicates 0000 BIT ERRORS; the SD and RD LEDs indicate data present; and the RLSD, DTR, DSR, RS, and CS LEDs are all ***on***. Press key E to inject 8-bit errors. Press key F to force an out-of-sync condition.

4.271 ▶A limited test of the SD, RD, RS, and CS leads can be made using test code 58. With nothing connected to the DCE and DTE connectors, use jumper wires to connect pins 2 to 3 and 4 to 5. If a synchronous data set is selected, interconnect pins 15, 17, and 24. Enter test code 58 and observe that whatever was transmitted will be received subject to the parameters selected for test code 58.◀

5. APPLICATIONS OF TESTS

5.01 This section provides application examples which extend the basic use of the tests described in Part 4.

A. Loopback Line Tests

5.02 Loopback loss measurements are performed with test codes 26 (1004 Hz), 27 (2713 Hz), and 11 (ac voltmeter). Access T and R terminals with the telephone adapter cables. Insure that the TALK/DATA switch is in the TALK position and that receive T and R are properly terminated

with one of the terminator plugs. Enter test code 27 and transmit the 2713-Hz signal for at least 5 seconds. This loops back the far-end DAS. Enter test code 26 and transmit the 1004-Hz signal. Enter test code 11 and measure the receive line signal on the RCV T and R terminals. After testing is completed, restore the circuit by transmitting the 2713-Hz signal.

> ***Note:*** To assure that the circuit is restored, enter test code 26 and retransmit the 1004-Hz signal. Use test codes 18 (frequency counter) and 11 (ac voltmeter) to verify the absence of 1004-Hz loopback signal.

5.03 Loopback bit error measurements are performed with test codes 27 (2713 Hz) and 55 (bit error test). Connect the DTS to the data set via the data set connector and the telephone connector. Set the TALK/DATA switch to the TALK position. Enter test code 27 and transmit the 2713-Hz signal for at least 5 seconds. This loops back the far-end DAS. Set the switch to the DATA position. Enter test code 55 and proceed to perform the bit error test. After testing is completed, restore the circuit by setting the switch in TALK position and transmitting the 2713-Hz signal.

> ***Note:*** To assure that the circuit is restored, enter test code 26 and transmit the 1004-Hz signal. Use test codes 18 (frequency counter) and 11 (ac voltmeter) to verify the absence of 1004-Hz loopback signal.

B. Start-Up Monitoring Test

5.04 The one-way test of test code 71 may be used for on-line start-up monitoring of either the receive or transmit data. To use the monitor mode, insure that the interface module switches are in the MON position. In the receive direction, enter test code 71 and press GO. Select the one-way test by pressing 1. Specify the expected 16 characters to be monitored by means of the alphanumeric keys and Table M. Press A when the display indicates PRESS A TO START. Operation then proceeds as in paragraph 4.197.

5.05 In the transmit direction, it is necessary to open the RLSD and SCR interface lead switches (both toward the DCE and DTE [Fig. 8 (8)]. Using jumper wires, patch the RS and SCT interface lead jacks [Fig. 8 (2)] to the RLSD and SCR common interface lead jacks [Fig. 8 (10)], respectively. In Version 1, when the test sequence message is displayed, enter 29 so that the message 29 ? (0=RD, 1=SD) appears. At this time, 1 is entered to permit SD to be monitored. Enter 71 and the display will indicate 29 1 (0=RD, 1=SD) 71 for 3 seconds then : . In Version 2, when the TEST SEQ: message is displayed, enter 29 79 and the display will read TEST SEQ: 29 79. Press GO and when the TEST COMPLETE message appears, the DTS is in the monitor SD mode. Select the one-way test by pressing 1. Specify the expected 16 characters to be monitored by means of the alphanumeric keys and Table M. Press A when the display indicates PRESS A TO START. Operation then proceeds as in paragraph 4.197.

5.06 The use of start-up monitoring in trouble location is given by the example in Fig. 19. The initial 16 characters (SYN through J) are programmed first and transmissions of the message (SYN through EOT) are monitored and recorded. The message must be no longer than 500 characters (see paragraph 4.198). If no errors are displayed, the DTS is programmed for the next 16 characters (K through Z). This process of programming successive 16-character blocks is continued until the complete message is verified.

C. Loopback Start-Up Test

5.07 The start-up test may be used for testing data sets that are in either an analog or digital loopback mode. One method of performing a loopback start-up test follows.

5.08 Enter test code 67 or 70 and press key 2 (IR SW). If test code 70 has been entered, the selection of the programmable message is now made as described in paragraph 4.216 and the normal or timed transmit mode is selected. The test is begun by pressing key A. The display will indicate the number of blocks received, the number of blocks in error, and the number of trouble blocks.

> ***Note:*** When testing some data sets in digital loopback, pad characters (marking) are required at the beginning of the programmable message to avoid invalid error indications. This is necessary because the data set may drop the first few characters as a result of the RS-CS turnaround time.

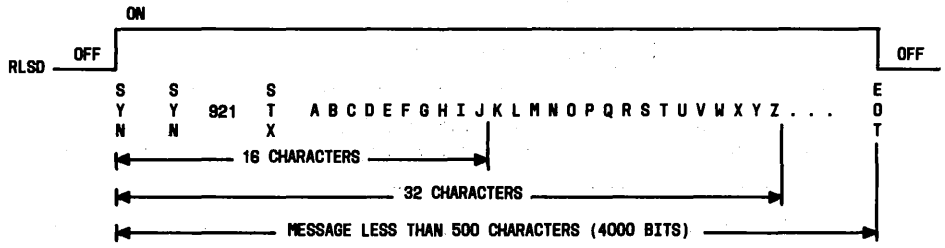


Fig. 19—Example of Start-Up Line Monitoring

D. Isochronous Distortion Monitoring Test

5.09 To monitor (on-line) the isochronous distortion of a transmit data signal, place the CSU module switches in the MON position. In Version 1, when the TEST SEQ: message is displayed, enter 29 and the message 29 ? (0=RD, 1=SD) appears. At this time, enter 1 to permit SD to be monitored. Enter 78 and the display will indicate 29 1 (0=RD, 1=SD) 78. In Version 2, when the TEST SEQ: message is displayed, enter 29 78. The display will read TEST SEQ: 29 78. Press GO and when the TEST COMPLETE message appears, the DTS is in the monitor SD mode. Press GO to measure the isochronous distortion.

E. Full Duplex Start-Stop Distortion Test

Version 1 Only

5.10 Test code 79 is normally used in the receive-only mode. However, the DTS may be conditioned to operate full-duplex (for example when the near-end data set is in analog loopback) by performing the following steps.

(1) Run test 53 (transmit only) and select a dotting pattern. Press GO. The DTS will keep RS ***on*** and continue to transmit the dotting pattern even after the message TEST INTERRUPTED appears.

(2) Now run test 79 as explained in paragraph 4.245 but do not turn RS ***off.***

Versions 2 and 3

5.11 To perform a full-duplex start-stop distortion test using a Version 2 or 3 DTS, the procedure is as follows.

(1) Perform test 51 or 52 to send either a programmable or FOX message. Follow the steps as given in the test procedure for either 51 or 52 until the message PRESS A TO START appears. It is not necessary to press the A key. Instead, press GO and the message TEST INTERRUPTED will appear momentarily.

Note: If the A key was pressed, then the message would be transmitted until the GO key was pressed. If the A key was not pressed, ensure that the CS LED is ***on*** when running test code 79.

(2) Now run test 79 as explained in the test procedure beginning with paragraph 4.250.

F. ▶Preprogrammed Terminal Test◀

▶Version 3 Only◀

5.12 ▶When access to a remote Data Test Center is not available for installation testing, the preprogrammed terminal tests of the 921A DTS (Test Code 58) may be substituted. For DATASPEED 40/4, message 01 (EBCDIC) or 04 (ASCII) should be sent to test the station's response to selection. If correct, this will place a test message on the screen. The response to selection will be captured by the 921A and may be checked for correctness. (Responses to succeeding transmissions will not be copied.) Next, clear the screen, type a few characters, enter a bid, and send message 02 (EBCDIC) or 05 (ASCII) twice quickly. This will cause the S/R key to flash and the screen to clear. The initial response to polling may also be checked. If a printer is present at the station, it should be checked using the AMZZ message, 03 (EBCDIC) or 06 (ASCII). (This message tests for slight maladjustment of the printer not detectable with the usual self-test.)◀

◗ TABLE Q ◖

MODIFIED TEST MESSAGES

APPLICATION	NAME OF TEST	921A TEST CODE 58 MESSAGE NO.	REMARKS
40/1, 40/2, 40/3, Int ROP	Full ASCII	07	Each line sent once instead of twice — send message twice to equal test in service manual. Message requires editing (as given in service manual) in some cases.
40/1, 40/2, 40/3, Int ROP	132 Column Lines	08	
40/1, 40/2, 40/3	Edit	09, 10	Message has been split — send 09 followed by 10 to equal test in service manual.
Int ROP	Tabs	11	
40/3	40/3 Fox	12	Not in service manual in this form — replaces several tests in service manual.
40/1, 40/2, 40/3, Int ROP	Options	13	
40/1, 40/2, 40/3, Int ROP	RO	14	
Int ROP	Special Options	15, 16	Message 15 must be sent three times with minor editing the second and third times and Message 16 must be sent once to equal the test in the service manual.
40/1, 40/2, 40/3, Int ROP	Printer AMZZ	17	Not in service manual at present, but should be used by all printers to verify adjustment.

5.13 ▶For DATASPEED 40/1, 40/2, and 40/3, testing may be done using the sequence in the appropriate service manual: 325-059 (40/1), 325-058 (40/2), 325-062 (40/3), or 325-064 (integrated ROP for 40/1, 40/2, or 40/3). The messages required by these service manuals to be sent from a remote Data Test Center are stored in the 921A DTS with some modifications, as listed in Table Q. Consequently, the results of each test (except for these modifications) will be exactly as shown in the appropriate service manual.◀

6. REFERENCES

6.01 Additional information concerning the DTS may be obtained from the following sources.

SECTION	TITLE
107-402-500	921A Data Test Set—Maintenance
502-323-402	5000A Transaction III Terminal Set
592-027-501	208A-Type Transmitter-Receiver —Test Procedures Using 921A Data Test Set
592-028-501	202S Transmitter-Receiver—Test Procedures Using 921A Data Test Set
592-029-501	201C-L1Transmitter-Receiver—Test Procedures Using 921A Data Test Set
592-030-501	208B-Type Transmitter-Receiver —Test Procedures Using 921A Data Test Set
592-031-501	202T Transmitter-Receiver—Test Procedures Using 921A Data Test Set
592-032-501	209A-L1 Transmitter-Receiver—Test Procedures Using 921A Data Test Set
592-034-501	212A Transmitter-Receiver—Test Procedures Using 921A Data Test Set
595-100-500	550A-Type Channel Service Unit —Test Procedures
595-200-500	500A-Type Data Service Unit—Test Procedures