PROGRAMMABLE SCANNER/DISTRIBUTOR SD-94844-01

DESCRIPTION

AUTOMATIC TROUBLE ANALYSIS (ATA)

CONTENTS PAGE

1. GENERAL

1.01 This section provides a description of the programmable scanner/distributor (PSD).

1.02 This section is reissued for the following reasons:

(a) To change title

(b) To add description of PSD circuit packs.

1.03 The PSD may be used in applications which require the observance and control of electromechanical circuits and the communication of information to external devices.

1.04 The PSD (Fig. 1) consists of a programmable controller (procon), a scanner/distributor, I/O ports, interface circuits, a random access memory (RAM), a control and display panel, and a power converter. The controls and indicators of the PSD are shown in Figure 2.

1.05 The procon directs the data flow and also has the ability to operate on the data which is being received, stored, or transmitted.

1.06 Data concerning the operation of the office is gathered via the scanner, which converts the state of office relays into a form which is usable by the PSD. The distributor provides access to the office by converting binary information from the PSD into a series of relay opens and closures.

1.07 Communication between the PSD and external devices is via one or more I/O ports. These ports may be connected to dedicated private line or dial up data links or devices such as teleprinters.

1.08 The RAM is used for temporary storage of data between collection and transmission or for scratch memory during arithmetic or logical operations.

1.09 Data transfers between the controller and other parts of the PSD pass through the bus interface. This interface also contains a binary counter, usable as a real-time clock, and error-detection circuitry. This error detection circuitry functions primarily as a check on the sanity of the controller.

1.10 The control panel contains error indicators and switches for exerting control over the operation of the PSD.

1.11 The power converter provides the logic voltages for the PSD.

2. UNIT DESCRIPTION

A. Physical

2.01 The PSD consists of a procon unit, a 16-row by 16-bit scanner matrix and a 4-row by 16-bit signal distributor matrix or a 16-row by 10-bit scanner matrix and a 4-row by 6-bit signal distributor matrix, a RAM, I/O ports, a power converter, and a control and display panel. The PSD with a combined scanner/distributor requires

approximately 14 inches of mounting space on a standard relay rack; the PSD with separate scanner and distributor requires approximately 18 inches of mounting space.

B. Functional

2.02 The procon is a micro-controller containing a read-only memory encoded with a unique, application-oriented program. This unit directs all functions of the PSD via 16-bit unidirectional input and output buses.

2.03 The basic connections for the circuit packs and procon for the PSD for No. 5 Crossbar are shown in Figure 3. The circuit packs shown are the interface controller (ICNT), two bus interfaces (BI0, BI1), RAM0, the trouble buffer interface (TBI), three data channel interfaces (I/O 0, I/O 1, I/O 2), the bus extender (BEX), the scan/distribute controller (S/D CONT), ten scan matrices (SM00 through SM09), and three signal distribute matrices (DM0, DM1, DM2).

Data Bus

2.04 Data is transferred between the procon and the various subunits of the PSD via the 16-lead data bus (Fig. 3). The information sent on procon output bus leads $\overline{0OB(0\text{-}15)}$ drives the PSD bus leads DB(00-15)0 (Fig. 4). The data bus drivers on the BI circuit packs are enabled by $\overline{ENB}$ being at a low level. The bus leads DB(00-07)0 are transmitted to I/O 0, I/O 1, I/O 2, RAM0, and BEX circuit packs (Fig. 5). The TBI circuit pack receives only bus leads DB(00-04)0. The BEX also receives the remaining bus leads DB(08-15)0. The BEX then transmits these bus leads as leads D(0-15)to the combined scanner and signal distributor matrix (Fig. 6). Each scanner matrix circuit pack (A1068) receives one of these bus leads (D0-D9), and each signal distributor matrix circuit pack (A1074) receives three of these bus leads (D0-D6). A more detailed functional schematic of the I/O, RAM0, BEX, and TBI circuit packs is shown in Figures 7 through 10.

2.05 Each A1074 circuit pack contains eight signal distributor points organized as two bits of four words. The two low order addresses are decoded into four clock signals which select a unique word out of the four.

2.06 The A1074 circuit packs place data from the PSD data bus onto the appropriate row of signal distribute points selected by the address present on the PSD address bus.

2.07 The A1068 circuit packs transmit data from a row of scan points to the procon. The scan points are selected by a row address present on the PSD address bus.

2.08 The address register, the real-time clock, and the PSD data bus gate data into the procon via input bus leads IB(0-15). When lead RDDB is at a high level, the PSD data bus is gated onto the input bus. A high level on lead RDAR gates the contents of the address register onto the input bus. A high level on lead RDRT gates the contents of the real-time clock onto the input bus.

2.09 When the PSD data bus is being gated to the input bus, lead $\overline{ENB}$ is driven to a high level. This prevents the data bus drivers on the BI circuit packs from controlling the bus and allows the bus to be driven by one of the functional subunits.

Control Bus

2.10 The control leads from the procon are received by the ICNT circuit pack (Fig. 3) which derives various clock and gating signals. These leads are buffered by the ICNT circuit pack to drive the PSD control bus.

2.11 The source select leads, $\overline{0S0}$, $\overline{0S1}$, and $\overline{0S2}$, drive control leads DI00, DI10, and DI20, respectively (Fig. 4). The device select leads, NI0-NI3, are buffered to control bus leads DS(0-3)1. The ICNT circuit pack gates the control bus leads DI(1-2)0 and DS(0-3)1 to the I/O, TBI, and BEX circuit packs (Fig. 5). The TBI and BEX circuit packs do not receive the lead DI20. The ICNT circuit pack also gates lead DI00 to the RAM0 circuit pack.

2.12 Destination select leads, $\overline{0D0}$ and $\overline{0D1}$, drive control bus leads DO00 and DO10 through gates which are enabled by a high level on the procon clock lead TCLK. A control bus lead is driven low by a combination of a high level on lead TCLK and a low level on the appropriate destination select lead. The ICNT circuit pack gates lead DO10 to the I/O, TBI, and BEX circuit

packs. The ICNT circuit pack also gates lead DO00 to the RAM0 circuit pack.

Address Register

2.13 The 16-bit address register (Fig. 4) is divided into two 8-bit bytes, each byte is on the BI circuit pack. The control signals necessary for writing and reading of the address register are received, decoded, and transmitted to the BI circuit packs from the ICNT circuit pack.

2.14 When writing into the address register, the procon places the complement of the data on its output bus leads $\overline{0OB(0\text{-}15)}$ and causes a low going pulse on lead 0D2. This causes a high going pulse on leads LDARLO and LDARHI. The data on $\overline{0OB(0\text{-}15)}$ is gated into the address register on the rising edge of these pulses and latched on the falling edge. The outputs of the address register drive the leads of the PSD address bus leads A(00-11)0 through the open buffer circuits. The BI circuit packs transmit the leads A(00-11)0 to the RAM0 circuit pack (Fig. 5). The BI circuit packs also transmit eight of these leads (A00-A07)0 to the BEX circuit pack. The BEX then transmits these address bus leads as leads A(1-8) to the S/D controller circuit pack (Fig. 6). The S/D controller circuit pack gates four address bus leads AD(1-4), to the scanner matrix circuit packs. The other address bus leads are decoded into clock signals and sent to the signal distributor matrix circuit packs. A more detailed schematic of the S/D controller circuit pack is shown in Figure 11.

2.15 The lower byte of the address register can be written without affecting the upper byte. This is accomplished by a low going pulse on lead $\overline{0D3}$, which results in a high going pulse on lead LDARLO. The pulse on lead LDARLO causes the data on leads 0OB(0-7) to be latched into the lower bytes of the address register.

2.16 The contents of the address register are read by the procon which causes a low going pulse on lead $\overline{0S2}$. This pulse causes a high going pulse on lead RDAR and a low going pulse on lead RDDB. The high level on lead RDAR causes the contents of the address register to be gated onto the procon input bus leads IB(0-15). The low level on lead RDDB blocks the data path from the PSD data bus to the procon input bus.

Random Access Memory

2.17 The PSD buffer storage is provided by one or more RAM circuit packs (Fig. 5), each containing 1024 words of memory. Each word is capable of storing 8 bits of data plus a parity bit. Individual words are addressed via leads A(00-11)0 of the PSD address bus with leads A100 and A110 used as a board select address. A set of backplane straps determines the state of leads A100 and A110 to which an individual RAM circuit pack responds.

2.18 The PSD provides storage for up to 2048 sixteen-bit words. This is accomplished by providing four RAM circuit packs. One pair of RAM circuit packs is connected to the low order leads DB(00-07)0 and low order parity lead DBPLO of the data bus. The other pair is connected to the high order leads DB(08-15)0 and the high order parity lead DBPHI of the data bus.

2.19 Data is written into a memory word when the procon places information on its output bus leads 0OB(0-15) while generating a low going pulse on lead $\overline{0D0}$ (Fig. 4). This causes a low going pulse on lead DO00 of the PSD control bus. Leads 0OB(0-15) are gated to the PSD data bus. The state of leads DB(00-15)0 and 0OB(0-15) is the same during this operation. When the memory receives a low going pulse on lead DO00, it will store the data on leads DB(00-15)0, DBPLO, and DBPHI of the word specified by the address bus.

2.20 Information is read from the memory when the procon generates a low going pulse on lead $\overline{0S0}$. This results in a low going pulse on the DI00 which causes the memory to place data from the addressed memory location on the PSD data bus. The high level on lead RDDB causes data present on the data bus to be inverted and gated onto the procon input bus.

2.21 The address verification circuitry of ICNT circuit pack checks the validity of memory read or write operations. A falling edge on lead $\overline{0S0}$ or $\overline{0D0}$ arms this circuitry. A low level on lead AVO disarms it. If the circuitry remains armed at the falling edge of the clock signal on lead TCLK when lead T0 raises to a high level, an error condition is indicated.

Scanner/Distributor

2.22 The scanner matrix and signal distributor matrix circuit packs (Fig. 6) are connected to the PSD data, control, and address buses by the BEX circuit pack. The BEX circuit pack (Fig. 5) provides termination and buffering for all bus leads and translates the PSD control bus signals into the control signals required by the scanner and distributor circuits. The address register is loaded with the address of the desired row before the scan or distribute operation. The leads of the PSD address bus are used to drive the address leads of the S/D controller bus. The address to which a row of scan or distribute points will respond is determined by a set of backplane straps.

2.23 Data on the procon output bus buffers the PSD data bus leads DB(00-15)0. The BEX buffers the PSD data bus to the scanner/distributor data bus leads D(0-15). No inversion exists in the data path from the procon output bus to the scanner/distributor bus.

Real-Time Clock

2.24 A 16-bit binary counter is provided with the PSD for use as a real-time clock (Fig. 4). The counter is presettable and readable. It counts at a rate determined by the frequency of the clock signal on the TCLK lead. During normal operation, the counter increments on the rising edge of a clock signal on the CLKRT lead.

2.25 An overflow of the counter is indicated by a high level on leads CTH1 and OVST. When lead OVST is at a high level, an overflow flag is set on the falling edge of the signal on lead TCLK. The setting of the flag is indicated by lead T1 being driven to a high level.

I/O Channels

2.26 The data port of the I/O circuit packs contains received data, transmitted data, readable status, and writable registers. Input data is read by the received data register. Data collected by the PSD to be transmitted over the data link to external devices is placed in the transmitted data register. The operating mode of the data port is indicated by the readable status register. The transmitted data format is controlled by the writable register.

2.27 Data is written to the transmit data register of an I/O circuit pack when the data is placed on the low 8 bits of the procon output bus and a low going pulse is generated on lead $\overline{0D1}$ while lead NI0 is at a high level.

2.28 Data which has been entered into the transmit register is transmitted serially from the data port on lead _BA. The detailed format of data transmission is determined by a select switch on the I/O circuit pack control register.

2.29 Serial information is received by the data port on lead _BB. This data is converted from serial to parallel form and placed in the received data register by the data port. The contents of this register are gated onto the PSD data bus by the data port when a low going pulse is generated on lead $\overline{0S1}$ while lead NI0 is at a high level.

2.30 Format checking of received data is performed by the I/O circuit pack. The result of this checking is in the data port status register. The contents of this register are gated to the PSD data bus when lead $\overline{0S1}$ is pulsed low while lead NI0 is at a low level. The status register also contains bits which indicate whether a character can be read from the received data register and whether a new character can be loaded into the transmit data register.

2.31 Leads _CA, _CD, and _SCA are controlled by the writable control register of the I/O circuit pack. This register controls the transmitted data format.

Control and Trouble Indication

2.32 Indication and control of the operational status of the PSD is provided by switches and light-emitting diodes (LEDs) located on the control and display panel. A more detailed functional schematic of the TBI circuit pack and the control and display panel is shown in Figure 10.

2.33 The status of the CONTROL 1, 2, 3, and 4 switches are delivered to the TBI circuit pack on leads TC(0-3) (Fig. 5). A raised switch allows the appropriate lead to be at a high level. A lowered switch grounds the associated lead. A low going pulse on lead $\overline{0S1}$ of the procon causes a high level on leads TC(0-3). The high level is gated onto the low order leads DB(00-03)0 of the

PSD data bus. At the same time, the data bus leads are gated to the procon input bus.

2.34 CONTROL 1, 2, 3, and 4 LEDs are driven by the buffered outputs of a 4-bit latch on the TBI circuit pack. This latch is loaded from the four low order leads of the PSD data bus when a low going pulse is generated on lead $\overline{0D1}$ while leads NI(0-3) are at a low level. A LED is turned on when its associated latch is loaded from a low level data bus lead.

2.35 The latch which drives the S/D, MEM, and I/O LEDs is loaded when lead $\overline{0D1}$ is pulsed low while lead NI0 is at a high level and leads NI(1-3) are at a low level. These LEDs reflect the status of the latch bits which are loaded from data bus leads DB(00-02)0. An additional two latch bits, connected to leads DB030 and DB040 of the data bus will be loaded.

2.36 A low level on the appropriate data bus lead results in lead $\overline{AE}$ or $\overline{BE}$ being latched at a low level. This results in the operation of mercury relay contacts on the relay/regulator circuit pack (Fig. 10). A low level on lead $\overline{AE}$ causes a contact pair closure which establishes continuity between leads TBLAA and TBLAB. A low level on lead $\overline{BE}$ causes a contact pair closure which establishes continuity between leads TBLBA and TBLBB.

2.37 The TEST switch on the control and display panel functions as a lamp test. When the TEST switch is depressed, a low level on lead $\overline{LT}$ causes all the LEDs to be operated.

2.38 When the INIT switch is depressed, a low level on lead $\overline{RST}$ and a high level on lead RST is caused. This causes a low going pulse on lead $\overline{RESET}$. The pulse will be of approximately 35 microseconds duration.

2.39 The EX switch is tied directly to lead T3 (Fig. 4). When EX switch is depressed, the pulse on lead T3 is at a high level.

Power and Fusing

2.40 The PSD obtains power from a standard -48V battery. A power converter transforms the battery into the +5V required by the logic circuitry and ±16V required by the I/O circuit packs. The ±16V is regulated by the relay/regulator circuit pack. The output of the relay/regulator circuit pack is ±12V which is tied directly to the I/O circuit packs.

2.41 All voltage supply leads are fused. The input battery is tied to the scan units through fuse SPB and to the power converter through fuse PF (Fig. 12). The +5V output of the power converter is connected to the procon and the control and display panel through fuses C0 and CD0. Power is applied to the scanner and signal distribution matrix circuit packs through fuse SD0 while the REF fuse supplies +5V as a reference voltage to the regulators on the relay/regulator circuit pack. PD0 and PD1 fuses supply current at +5V to the remainder of the logic circuitry.

2.42 The failure of a fuse supplying a positive voltage results in lead FAP being raised to approximately +5V. The failure of a fuse supplying a negative voltage results in lead FAM being raised to approximately -5V. Either of these conditions operates the fuse alarm relay on the relay/regulator circuit pack which causes a contact closure to establish continuity between leads TBLAA and TBLBB.

2.43 The power converter is operated by the PWR switch on the control and display panel. Failures in the power converter are indicated by the lighting of an LED on the power converter and by the closure of an alarm relay within the power converter. This closure is indicated by the establishment of continuity between leads TBLAA and TBLAB.

Terminal Numbering

2.44 The wiring side terminal numbering for the various connectors is shown in Figure 13.

3. DATA PORTS

3.01 The transmission and reception of data is via I/O data ports (maximum of 4), each functioning as one end of an asynchronous serial data link.

3.02 The connection between the data port and external device is a standard EIA interface. This allows the data port to be used with most of the existing types of low or medium speed asynchronous serial modems. A connector for each data port is provided on the PSD for connection to the appropriate device. This device must be

located within 50 feet of the PSD. Data transmission rate is either 300 or 1200 baud, determined by a backplane strap on the PSD.

4. CONTROLS AND INDICATORS

4.01 Controls and indicators are provided on the control and display panel (Fig. 2). Their functions are described below:

(a) The FA (fuse alarm) LED is lighted when a PSD fuse fails. It is also lighted when the FA lamp on the power converter is lighted to indicate excessive or low voltage or excessive output current.

(b) The CONT (controller) LED is lighted when the procon fails an instruction word parity check or sanity time time-out.

(c) The S/D (scanner/distributor), I/O (input/output), MEM (memory), and CONTROL LEDs are lighted under program control.

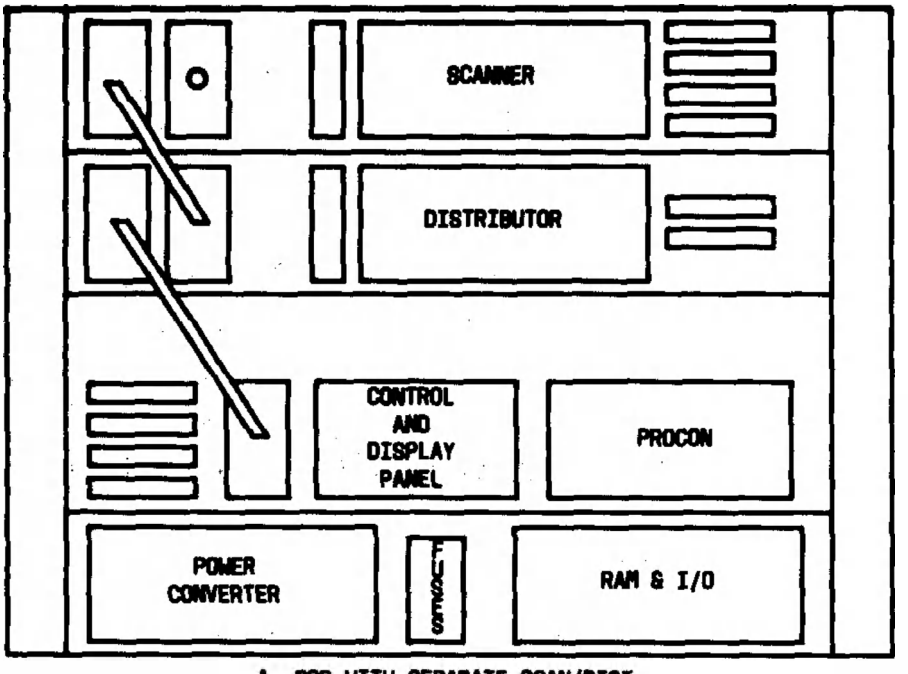
(d) The PWR switch applies -48 volt office battery to the power converter.

(e) The TEST switch illuminates all lamps on the control panel.

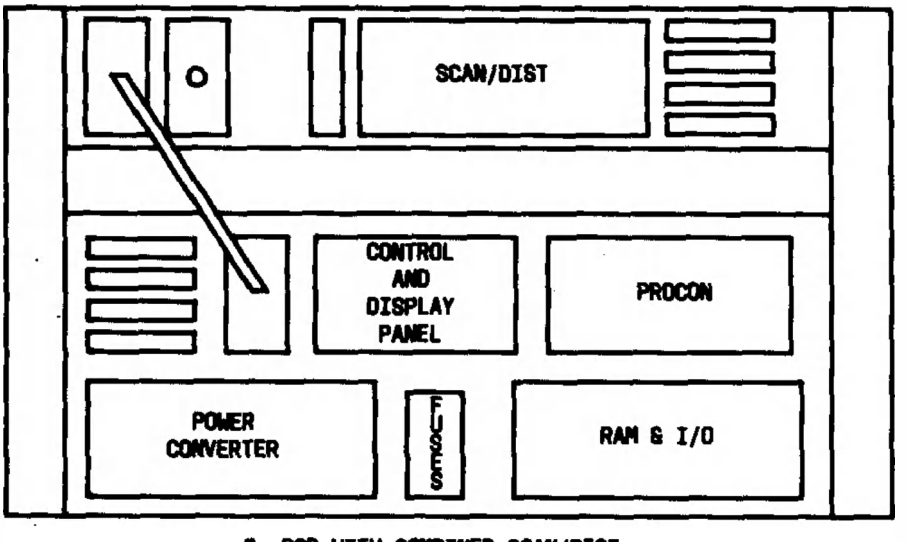
(f) The INIT (initialize) switch causes the program to be restarted at instruction zero.

(g) The EX (execute) switch causes the PSD to run tasks as defined by the application program.

(h) The CONTROL switches are used to define the tasks to be run when the EX switch is depressed.



A. PSD WITH SEPARATE SCAN/DIST



B. PSD WITH COMBINED SCAN/DIST

Fig. 1—Programmable Scanner/Distributor (PSD)

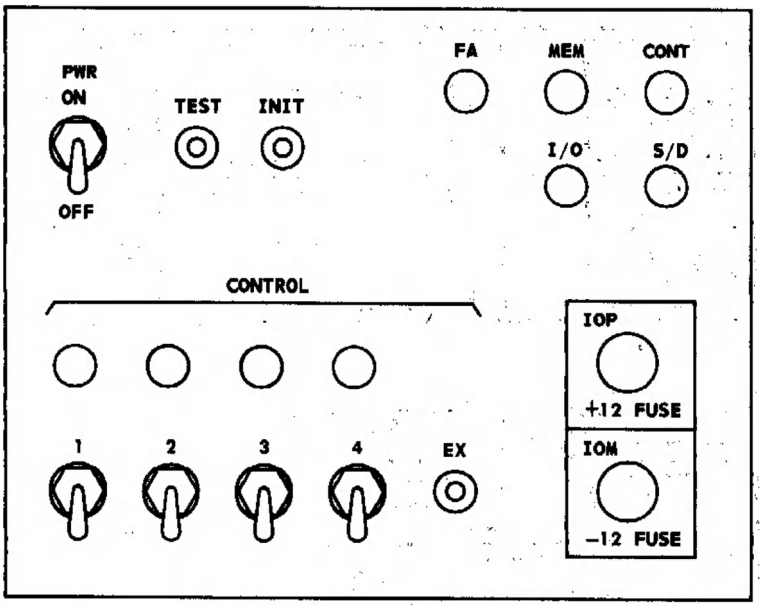


Fig. 2—PSD Control and Display Panel

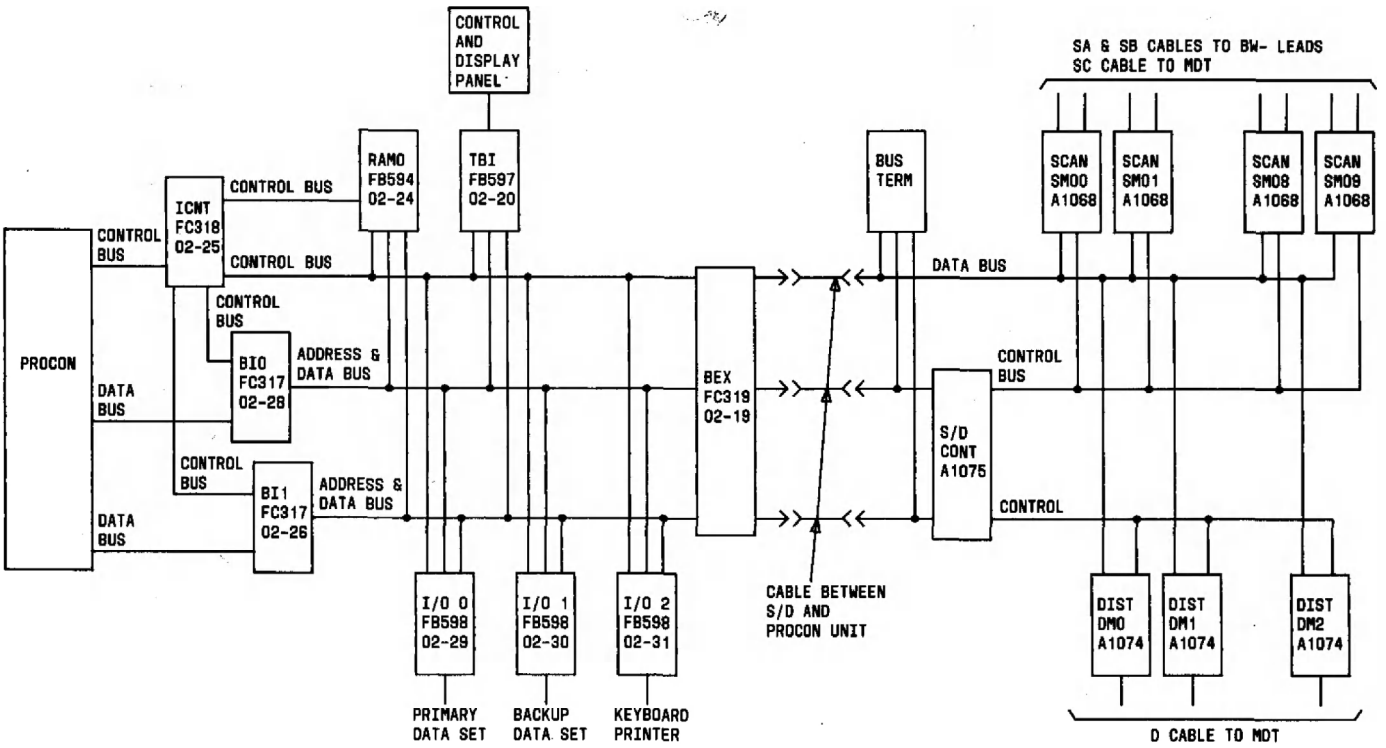


Fig. 3—PSD Circuit Pack and PROCON Interconnections

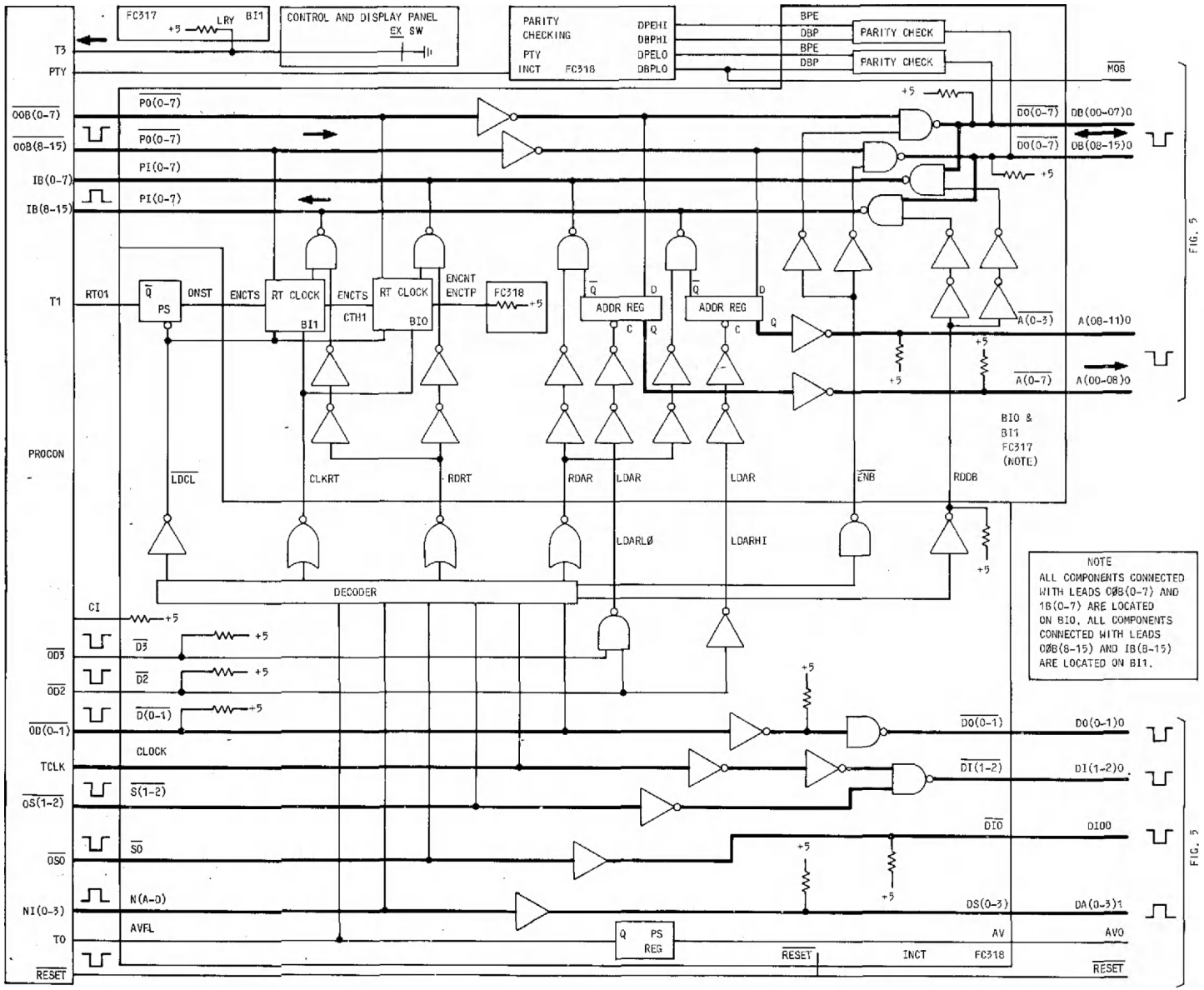


Fig. 4—PROCON, ICNT, BI0, and BI1 Functional Schematic

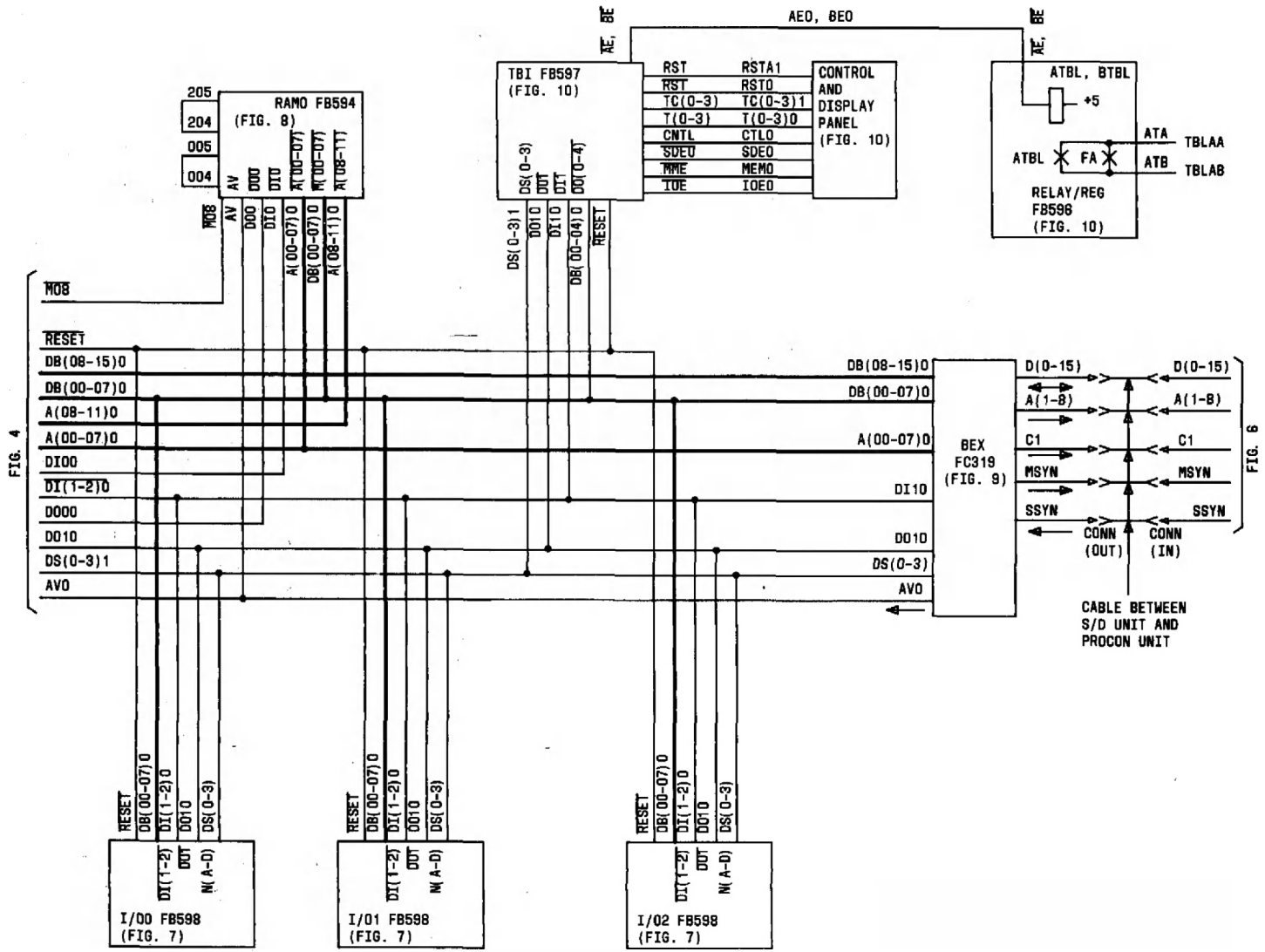


Fig. 5—Bus Layout Showing Interconnections of Circuit Packs RAMO, I/O (0-2) and BEX

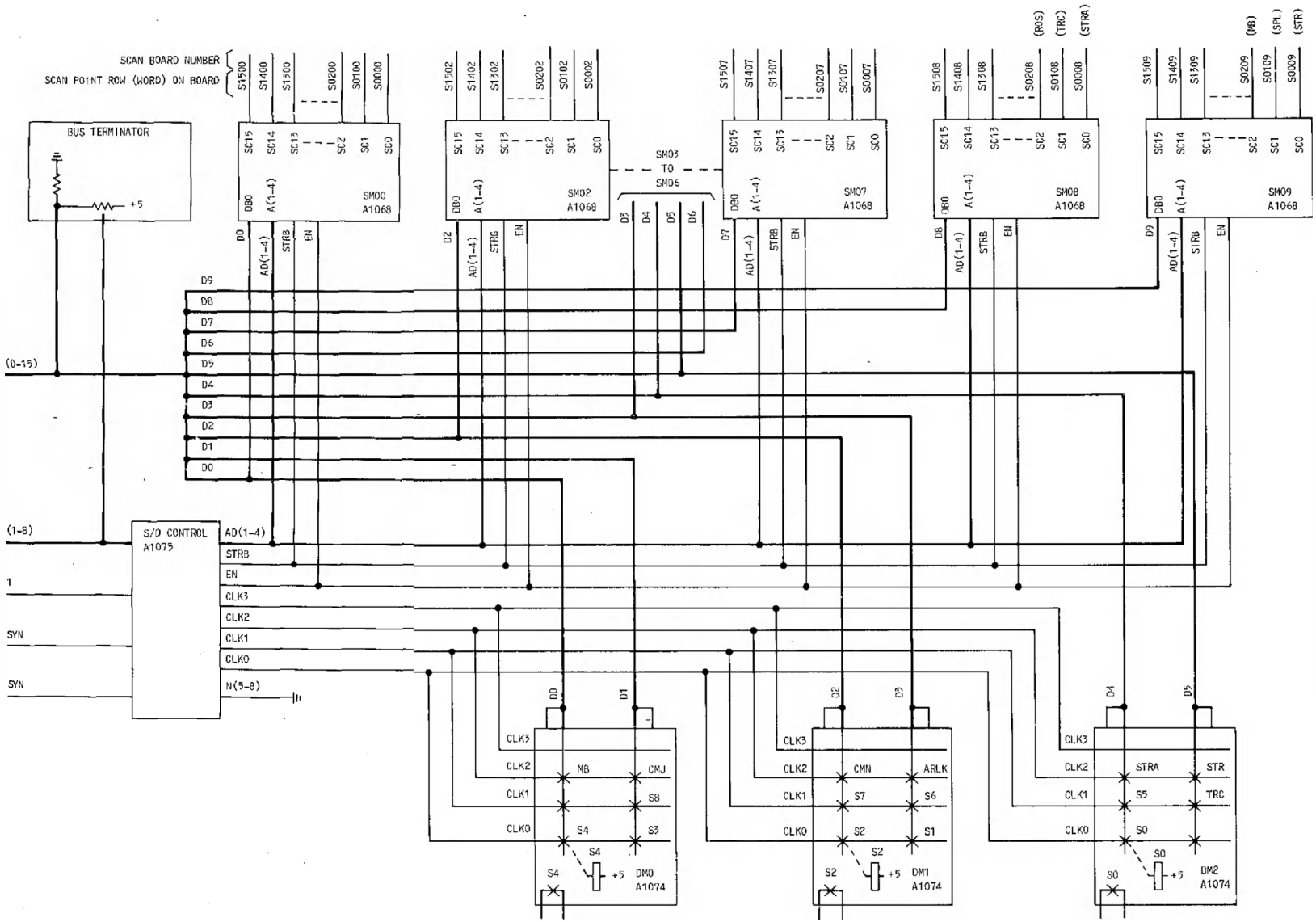
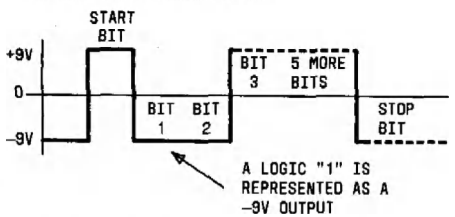


Fig. 6—Combined Scanner/Distributor Showing Functional Lead Connections to Circuit Packs S/D Controller, Scan (0-9), and Distribute (0-2)

NOTES:
1. I/O0 - NBO & NCO CONNECT TO GROUND,
   I/01 - NCO CONNECTS TO GROUND,
   I/02 - NBO CONNECTS TO GROUND
2. LOGIC "1" IS <0.8V,
   LOGIC "0" IS >2.4V
3. CLOCK PULSING - 60 MICROSECOND NEGATIVE GOING PULSE AT 4.8 KHZ REPETITION RATE
4. A TYPICAL CHARACTER TRANSMITTED ON LEAD BA IS SHOWN BELOW:



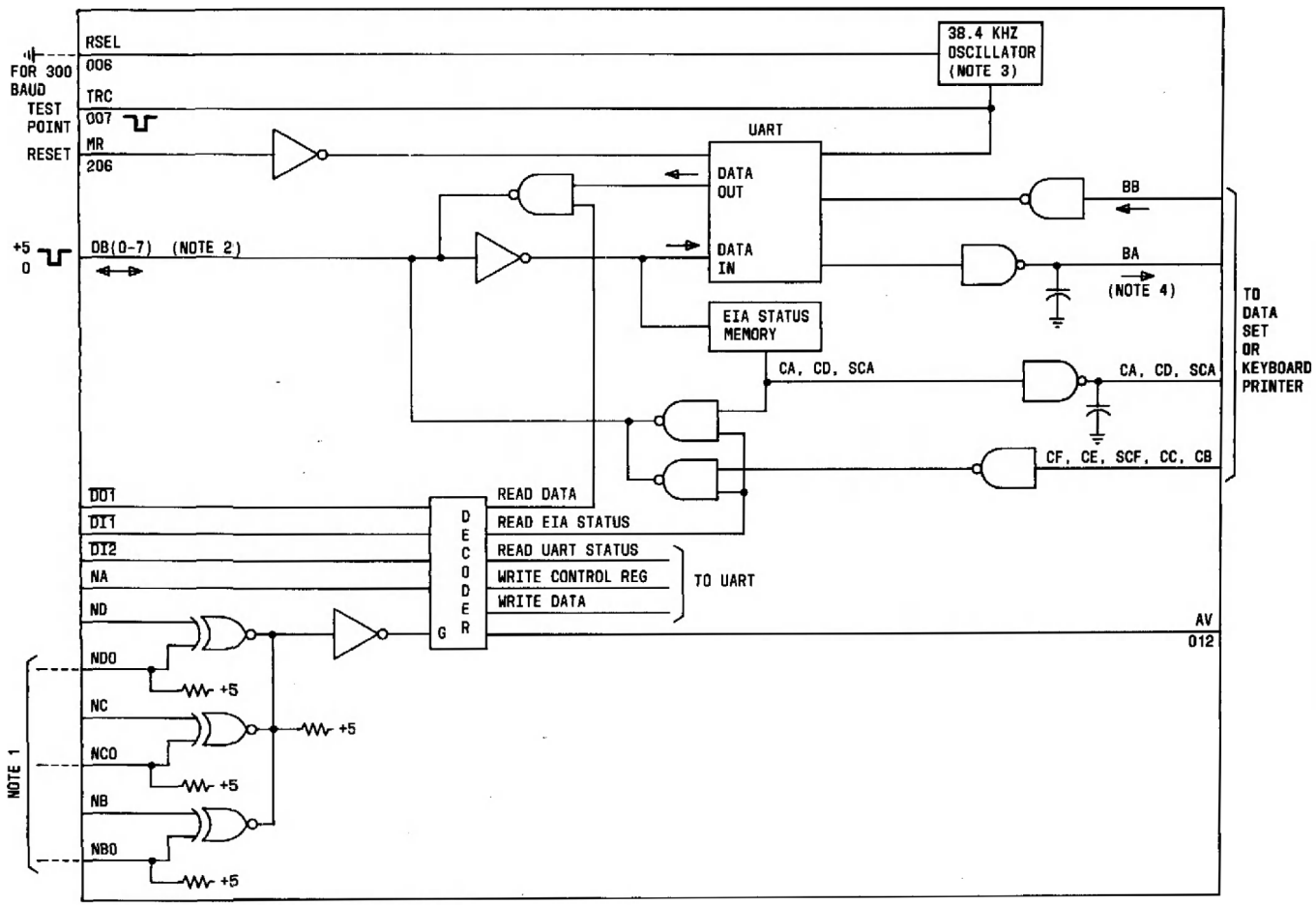
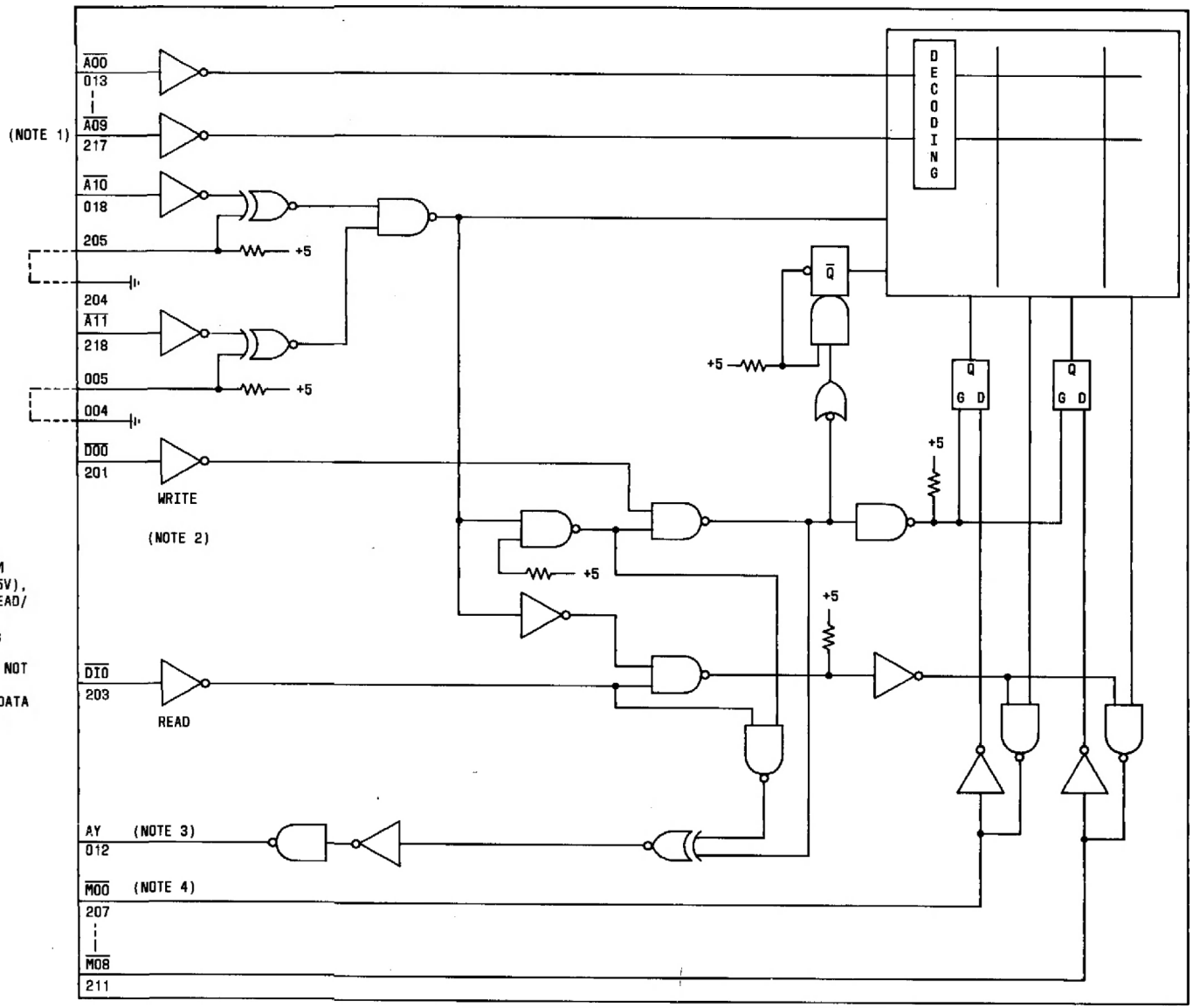


Fig. 7—I/O Port Circuit Pack (FC598)



NOTES:

1. LEADS $\overline{A00}$ TO $\overline{A09}$ SELECT WHICH RAM WORD (1 OUT OF 1024) (1=GRD, 0=+5V), LEADS $\overline{A10}$ AND $\overline{A11}$ ARE HIGH FOR READ/WRITE FUNCTION
2. TO WRITE, LEAD $\overline{D00}$ IS PULSED LOW; TO READ, LEAD $\overline{DI0}$ IS PULSED LOW
3. LEAD AV IS PULSED LOW IF ONE BUT NOT BOTH $\overline{D00}/\overline{DI0}$ GOES LOW
4. LEADS M00 TO M07 CARRY I/O WORD DATA (1=GRD, 0=+5V), LEAD M08 IS EVEN PARITY

Fig. 8—RAMO Circuit Pack (FB594)

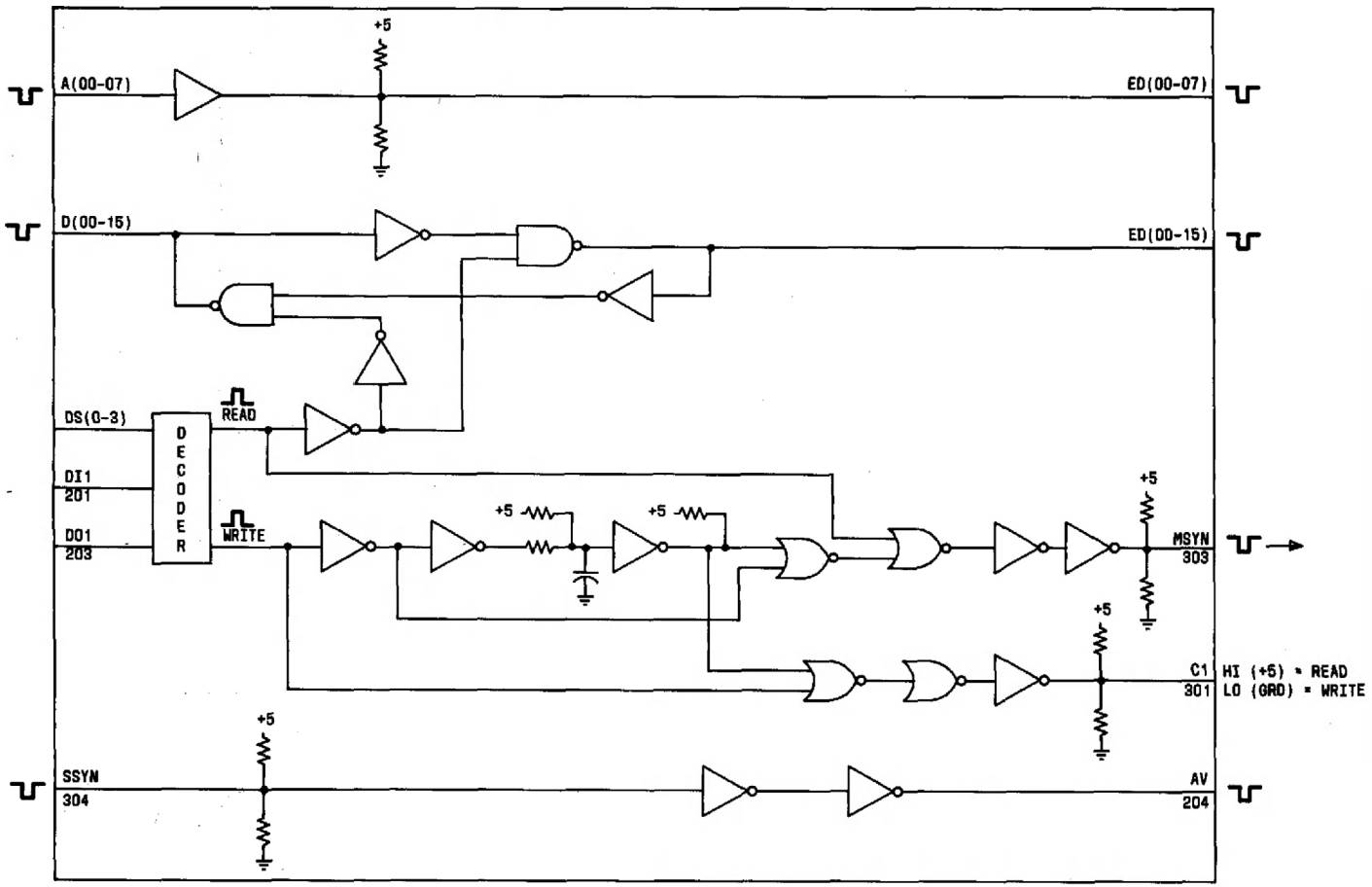


Fig. 9—BEX Circuit Pack (FC319)

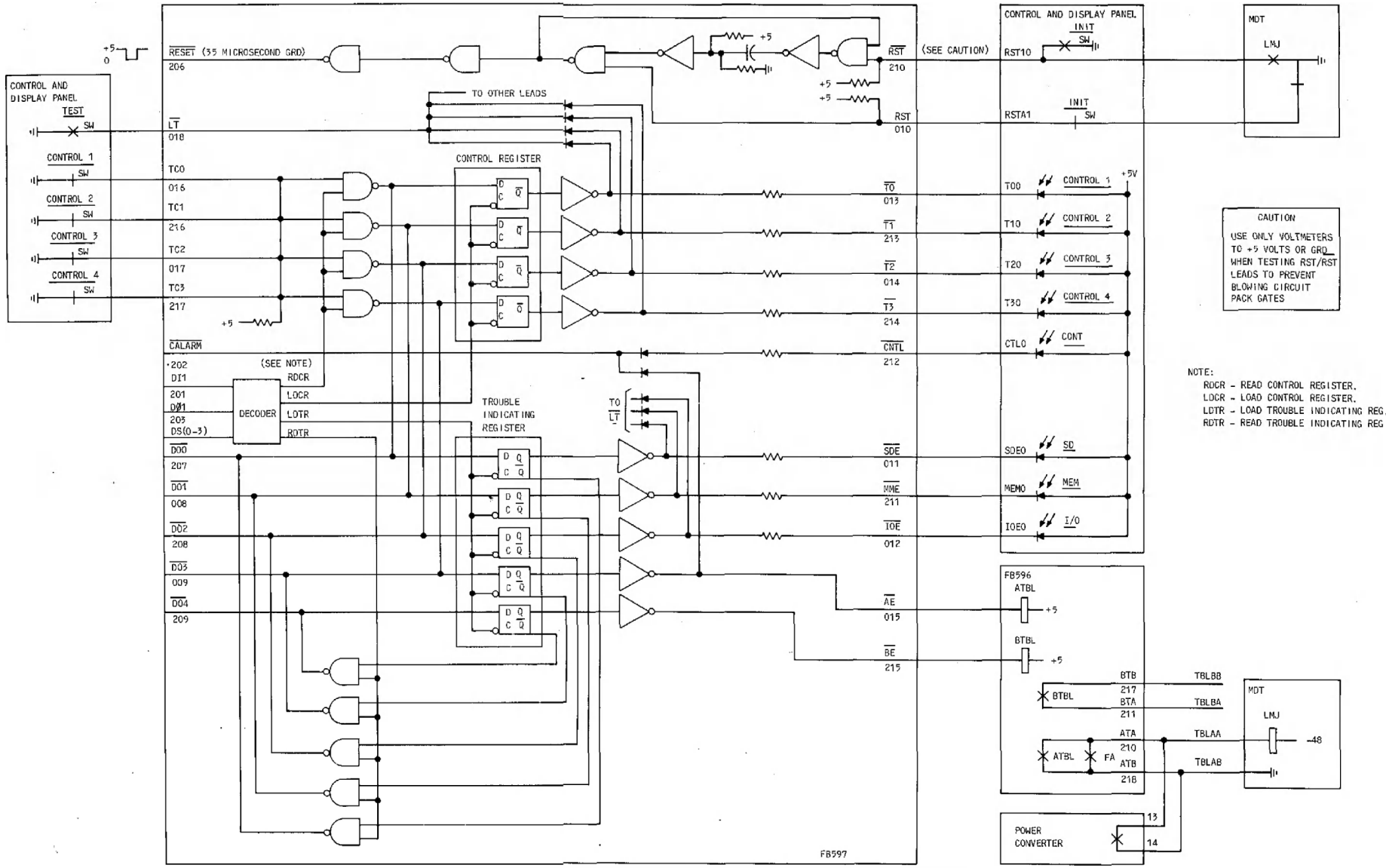


Fig. 10—TBI Circuit Pack (FB597) and Control and Display Panel

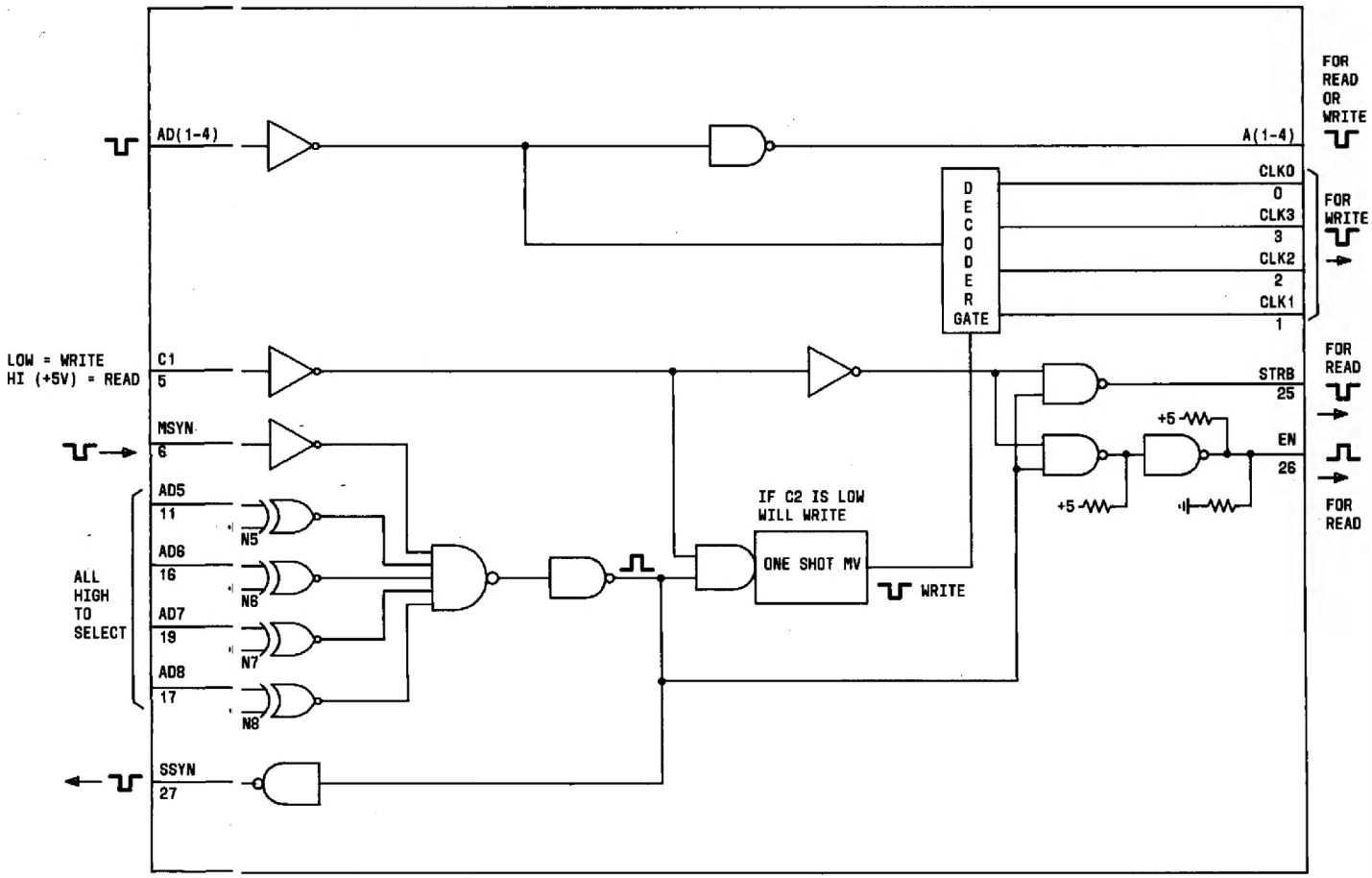


Fig. 11—S/D Controller Circuit Pack (A1075)

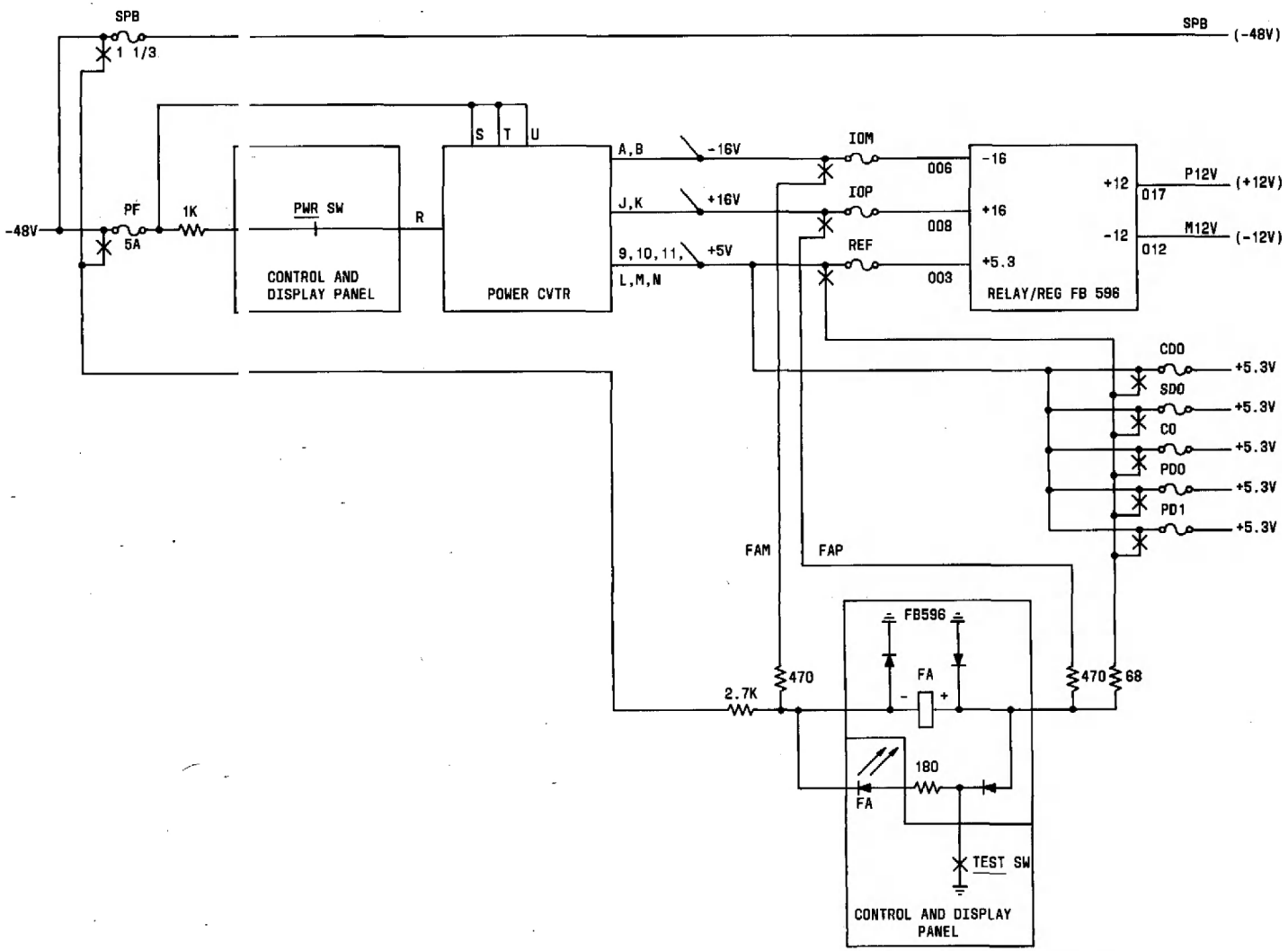


Fig. 12—Power Supply, Voltage Regulator, Control and Display Panel, and Fusing Part of Relay/Regulator Circuit Pack (FB596)

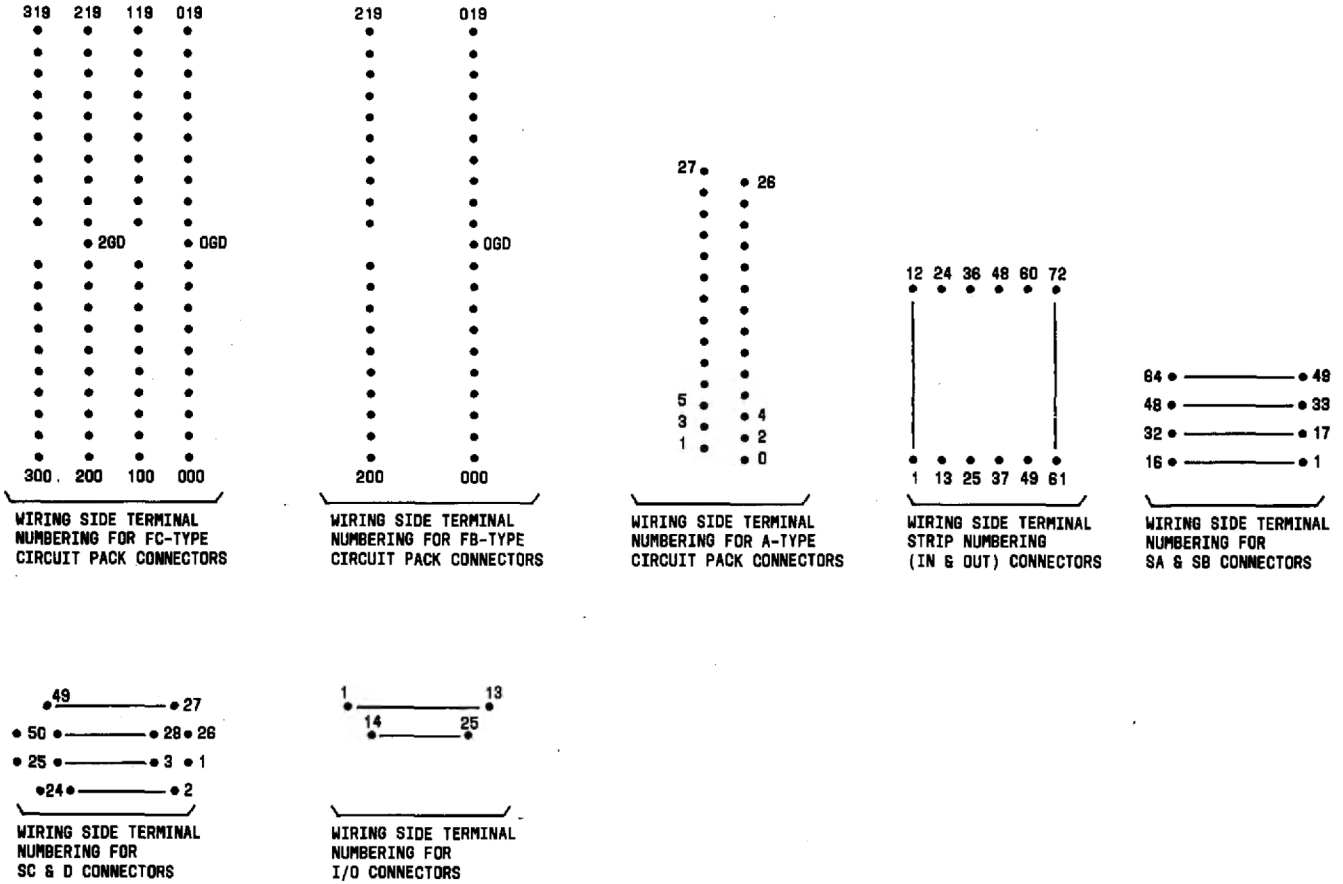


Fig. 13—Wiring Side Terminal Numbering for the Various Connectors