

**PROGRAMMABLE SCANNER DISTRIBUTOR
TROUBLE LOCATING PROCEDURES
AUTOMATIC TROUBLE ANALYSIS**

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4. TROUBLE ANALYSIS	2	1. GENERAL	
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B. Selecting Memory Option	2	1.02 This section is reissued for the following reasons:	
C. I/O Cross-Connects	2	(1) To change the title	
D. Faulty Circuit Pack Selection	2	(2) To add DTU discrete test functions.	
E. Circuit Pack Replacement	3	This reissue does not affect the Equipment Test List.	
F. Scan/Dist Cross-Connect Application	3	2. APPARATUS	
G. Procon Replacement	3	2.01 Diagnostic Test Unit (DTU) J99379C. Cross-connect plugs and cables are furnished with the DTU.	
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NOTICE

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3.02 Block the LMJ relay nonoperated for No. 5 crossbar or the LMJA relay nonoperated for No. 1 crossbar before performing trouble clearing procedures. Remove blocking tool after trouble is cleared.

3.03 Perform the procedures in Fig. 1. When a trouble locating number (TLN) is obtained on the DTU display, replace circuit packs per Tables B and C. Replace circuit packs sequentially, one at a time, and repeat the procedure after each replacement until the trouble is cleared. If the replaced circuit pack does not clear the trouble, reinsert the original prior to another replacement.

3.04 If circuit pack replacement does not clear the trouble, additional information is given in Table D to aid in locating faulty connector pins, wiring, etc. In addition to Table D, detailed testing information is given in Part 5.

3.05 The procedure for clearing a fuse alarm is shown in Fig. 2.

4. TROUBLE ANALYSIS

A. Inserting and Removing DTU

4.01 PSD diagnostics are performed with the DTU (Fig. 4).

4.02 Remove power from PSD and loosen four procon mounting screws and remove retainer strip (Fig. 3).

Caution: Loosen screws only enough to remove retainer strip.

Remove circuit pack PSU1 at location 06 and insert DTU left-hand circuit pack into location 04. The two circuit packs of the DTU will, therefore, be inserted one on each side of the right-hand DMU circuit pack in the procon. The DTU should be inserted very carefully and seated firmly in the procon.

4.03 When testing is completed, carefully remove the DTU, replace circuit pack PSU1 in location 06, replace retainer strip and tighten mounting screws, remove cross-connect plugs, and replace office cables on input/output (I/O) and scan/distribute connectors.

B. Selecting Memory Option

4.04 Set switches per Table A for memory option.

C. I/O Cross-Connects

4.05 Remove all keyboard printer and data set cables from the I/O connectors (note cabling locations so they can be replaced correctly). Place cross-connect plugs on each I/O connector.

D. Faulty Circuit Pack Selection

4.06 Table B contains a brief list of trouble numbers. As a further aid to trouble isolation, Table D contains a detailed trouble list. The trouble number that appears in the display when the display switch is in the TLN position is found under TLN in the table. In general, several faults will have the same TLN. When the display switch is set to the DATA position, the second number of the total trouble number appears in the display. This number is matched with the number under the DATA column in that group which has all the same TLNs. If there is more than one matching number, the procedure is repeated with the display switch in the ADDR and then the AUX position. If this procedure produces a direct match of a total trouble number that points to a single circuit pack, then that circuit pack should be replaced. If this procedure results in the determination of an area of the table that is close to the number in the DTU display, the circuit packs indicated for those numbers should be noted. The circuit pack that appears most often for these close numbers should be selected for initial replacement. The case also exists where a direct match in trouble numbers indicates more than one circuit pack. The circuit pack appearing most often in the REASON FOR FAILURE column should be replaced first.

4.07 An X in the digit position of a listed number is a "don't care" condition. These are considered to match any data in the corresponding digit position of the TLN.

4.08 Examples using Table D are given in (a) through (c).

(a) Direct match

Total TLN = 22 2000 0 177771

This number points to FC317 at 02-26.

(b) Close numbers

Total TLN = 47 177603 0 177771

A close number, 47 177602 0 177771, appears in the table. That number in addition to several other close numbers points to FC317 at 02-28. Note also that the number 47 XXX 0 177771 is a direct match. This points to FC318 at 02-25.

(c) Direct match with multiple packs

Total TLN = 201 0 3777 37

Circuit packs 02-20, 02-25, and 02-19 are listed for this number. The pack at 02-20 has the most entries in the REASON FOR FAILURE column and should be replaced first.

4.09 The 100001 TLN indicates that a fault was detected during the scan/distribute test. The unit that failed is the one that contains the cross-connect. Only numbers that are listed for the type of unit being tested should be initially considered. For example, if a combined unit has the cross-connect applied to it, numbers that indicate equipment locations CU-16 to CU-32 (combined unit) are valid. If a separate unit is being tested, the numbers with equipment locations SU-16 to SU-32 (scan unit) or DU-16 to DU-32 (distribute unit) are valid.

4.10 Trouble number 32 indicates that a PSD data bus is being held at ground. The DATA register indicates which lead is being held. A 1 in the bit position indicates the corresponding failing data bus bit. See Table D, note 6.

E. Circuit Pack Replacement

4.11 Before replacing a circuit pack, set the PWR switch on the PSD control panel to OFF. After replacing the circuit pack, set the PWR switch to ON, and momentarily operate the RESET switch on the DTU.

F. Scan/Dist Cross-Connect Application

4.12 For a combined scan/distribute unit, cross-connects are connected to the SA, SB, SC, and D connectors (Fig. 3). Connect ground clip of cable assembly to mounting plate. After the diagnostic is run, the cross-connect is moved to the next unit to be tested.

4.13 For separate units, the cross-connect is attached to the SA, SB, SC, and SD connectors on the scan unit to be tested and to the DA and DB connectors on the distribute unit. After the diagnostic is run, the cross-connects are moved to another set of scan/distribute units. If the application contains more scan units than distribute units, the cables can be left on the distribute connectors of one unit while the other end of the cross-connect cable is moved to test all the scan units. The same procedure is used in reverse if the application contains more distribute units than scan units. If there is a question as to whether the fault is in a scan unit or a distribute unit, cross-connecting with different units can help to isolate the fault.

G. Procon Replacement

4.14 To replace the procon, note the location of the plugs on the backplane of the procon, then remove them by carefully pulling straight out. Do not bend the attached cables excessively.

4.15 Loosen the four mounting screws at the front of the procon (Fig. 3) and lift the unit from the PSD. Insert the replacement procon in the PSD, and tighten the four mounting screws.

4.16 Carefully align the plugs with the backplane pins and connect the plugs. Connector information is given in SD-94844-01.

4.17 Perform procedures outlined in Fig. 1.

5. DETAILED TROUBLE ANALYSIS**A. Transient or Intermittent Failures**

5.01 Continuous execution of the diagnostic program can be performed to acquire information on a transient fault. In this mode the diagnostic program cycles until an error is encountered and then displays the trouble number and supporting fault information.

5.02 The diagnostic and routine exercise functions are given in Table F.

5.03 To run a diagnostic program continuously and stop on errors, select the diagnostic routine to be run (Table F), set the ERROR STOP switch on the DTU up, set the CONT XEQ switch up, and set the display switch to TLN. If trouble number 40000 or 100000 is displayed, the PSD is

not failing. When a number other than 40000 or 100000 is displayed, set the CONT XEQ switch to OFF (down), set the ERROR STOP switch to OFF (down), and momentarily operate XEQ switch once. Refer to Table B to determine faulty circuit pack. Several attempts may be required to obtain a valid trouble number.

5.04 It might be helpful to stimulate a failure while the diagnostic routine is cycling. For example, if the PSD fails when power is removed from an adjacent frame, remove power from that frame at this time. In another situation, the failure might be stimulated by pressing lightly on the PSD circuit packs.

B. Detailed Testing Using the DTU

5.05 Three levels of software are provided in the DTU. The first is a PSD diagnostic program that tests the PSD hardware, including the bus circuits, data ports, and scan/distribute circuit packs. The output of the diagnostic program is a trouble number and supporting fault information that is used in conjunction with Tables B, C, and D. The second level of testing is provided by routine exercise functions. These functions provide a test sequence for a specific portion of the PSD circuitry. For example, a read-write test of all equipped Random Access Memory (RAM) is provided with a user-supplied data word. The third and most detailed level of testing allows the user to select a particular procon peripheral unit and send (or display) information to (or from) that device. The execution of this sequence can be in a single cycle or continuous mode. The continuous mode supports oscilloscope tracing for fault location.

C. DTU Switch Functions

5.06 The functions of the various controls are given below:

- (a) **PROG SELECT Lever-Wheel Switch:** Selects the maintenance functions to be performed.
- (b) **DATA Lever-Wheel Switch:** Supplies data to the maintenance routines.
- (c) **HI/LO Data Switch:** Allows the data switches to be used for the HI or LO 8 bits of the 16-bit data or address field.

- (d) **RESET:** When pushed up, resets the procon and PSD and restarts the supervisory routine.
- (e) **XEQ:** Initiates the execution of the selected maintenance function.
- (f) **I/O Switches:** Informs the diagnostic program that a particular data port is equipped and should be tested.
- (g) **RAM Switches:** Used to select the RAM option used in PSD application under test.
- (h) **CONT XEQ:** When up, this switch allows a single instruction or maintenance routine to be continuously executed.
- (i) **ERROR STOP:** Stops execution of certain maintenance routines when an error is encountered.
- (j) **Display Switch:** Used to select the information that is displayed in the six-segment LED displays as follows:

TLN	Trouble Locating Number—This number is used to enter the trouble locating tables.
DATA	Used for data in routine exercise functions and supporting information in the tables.
ADDR	Used as an address in routine exercise functions and supporting information in the tables.
AUX	Used as auxiliary information in routine exercise functions and supporting information in the tables.

- (k) **TEST Switch:** Used to light the AV and PTY lamps.

D. DTU Display Functions

5.07 This is a display used for displaying TLN, DATA, ADDR, and AUX registers.

AV and PTY lamps: Address verify and parity failure indicators.

E. Diagnostic Routines

5.08 The PSD diagnostic routines are detailed below. The general use of these routines is outlined in Part 3.

Program**Select****Code - Data****Function**

0-000	PSD Diagnostic (PSDDG) without manual action sections and without scan/distribute test. Data port tests are run only if appropriate equipped I/O switches are up (requires cross-connect if up).
0-001	PSDDG as in 0-000 but with manual action sections (PSD front panel test).
0-002	PSDDG as in 0-000 but with scan/distribute section. Requires scan/distribute cross-connections.
0-004	PSDDG all sections.

0-013

Routine exercise. Write all equipped RAM addresses. Data written is in DATA register. Stop on address verifies failure if ERROR STOP switch is up.

0-014

Routine exercise. Write and read all equipped RAM addresses. Data written and read is in DATA register. If ERROR STOP switch is up, stop on data, parity, or address verifies failure. On error, the ADDR register has failing address and the AUX register has failing data bits.

0-016

Routine exercise. Scan/distribute exercise. Clear registers with 0-010 prior to running. Stop on error is valid. If TLN equals 0 after routine is completed, then no errors were detected. If TLN does not equal 0 after routine is completed, then errors were encountered. (See TLN trouble number 100001 for fault information, Table C).

0-017

Routine exercise. I/O port exercise. Requires that the data port to be tested have a cross-connect applied to its EIA connector and have its equipped I/O switch up. DATA register has test data to be used (see paragraph 5.14).

F. Routine Exercise Functions

5.09 Routine exercise functions are designed to test a specific functional area within the PSD. The available routines are listed below. These routines can be continuously repeated by setting the CONT XEQ switch up.

Program**Select****Code - Data****Function**

0-010	Clears the display registers (TLN, ADDR, DATA, and AUX) and PSD trouble indicators.
0-012	Routine exercise. Read all equipped RAM addresses. Compare RAM data with data in DATA register. Stop on data, parity, or address verifies failures if ERROR STOP switch is up. On error, the ADDR register has failing address, and the AUX register has failing data bits.

1-nnn

RDRAM - Read the RAM into the AUX register. The data switches, nnn, supply the LO address byte and override the LO byte of the ADDR register. The ADDR register is then used as the address for the read.

2-nnn

LDADDR - Load the ADDR register (HI/LO). The data switches, nnn, contain the HI or LO data byte. The ADDR register contains the information sent to the PSD address register. To verify the address was received accurately, the AUX register contains a read of the PSD address register.

3-nnn LDDATA - Load the DATA register (HI/LO). The data switches, nnn, contain the HI or LO data byte. This function does not test or exercise PSD circuitry but is used to load data for the other exercises (0-012, 0-013, 0-014, 0-017, 4-nnn, and 5-nnn).

0, 1 or 2

nn = device select code, 00-17.

4-nnn WRTRAM - Write the RAM. The DATA register has the write data, and the ADDR register has the RAM address. The data switches, nnn, supply the LO address byte and override the LO byte of the ADDR register.

G. Discrete Test Functions

5.10 A detailed control over the PSD circuits is provided by the Data To Peripheral (DTOP) and Peripheral To Display (PTOD) functions. These functions allow a particular device to be accessed and data sent to or received from that device.

5.11 The purpose of this feature is to provide a continuous execution of a single operation to allow oscilloscope fault location.

The program codes and data formats for these functions are as follows:

Program Select

Code - Data

Function

5-dnn DTOP - Data To Peripheral. Data is sent from the DATA register to the peripheral device dnn where:

d = destination select field

0, 1, 2, or 3

nn = device select code, 00-17

6-snn PTOD - Peripheral To Display. The selected peripheral device snn is accessed and the information received is displayed in the AUX register:

s = source select field

The device selection codes for the PSD circuits are shown in Table G.

5.12 The test functions of the devices in the PSD are shown in Table H. These devices can be read or written as follows:

(1) Read Control Register—The read control register contains the state of the four control switches (CONTROL 1 through CONTROL 4) on the PSD control panel.

(2) Write Control Register—The write control register consists of four CONTROL LEDS. These LEDS are lighted (written) to indicate trouble information.

(3) Read and Write Trouble Indicator Register—The trouble indicating register consists of three LEDS (S/D, MEM, and I/O) and a trouble indicating relay. The LEDS are lighted (written) to indicate trouble in the scanner/distributor, memory, and I/O ports. The relay is used to sound a major office alarm. The trouble indicating register is read to determine the current setting for those LEDS and relays.

(4) Read and Write Real Time Clock—The real time clock is used to time certain events.

(5) Read and Write Address Registers—The address register is used to identify the word to be accessed when doing scan, distribute, or memory operations.

(6) Read and Write Random Access Memory—RAM is used as a scratch pad memory to store information such as the current maintenance data transmitter (MDT) mode (punch and transmit express and nonexpress). To read or write a word, the address register is loaded with the address of the word, the data to be written is put on the data bus, and the device selection code for writing RAM is activated. When reading RAM, the address register is loaded with the RAM word address, the read RAM access code is activated, and the word is read from RAM and gated onto the data bus to the precon.

(7) Write Distributor Word—The distribute points are operated or released by loading the address register with the distribute row (word) number (1 out of 4). The bit or bits to be accessed in the word (n out of 6) are placed on the data bus and the write distribute point access code is activated.

(8) Read Scan Word—The scan points are read by loading the address registers with the scan row (word) to be accessed. The read scan point access code is activated and the scan word is put on the data bus to the procon.¶

H. External Scan Tests

5.13 The DTU is also helpful if it is determined that a scan or distribute problem (see paragraph 5.15) is external to the PSD. For example, assume that a particular scan point is always in error with the applications program, but the PSD diagnostic passes. Using the DTU, the address of the scan row that contains the error is entered (PROG SELECT = 02, DATA switches = row address). To perform a scan operation of the selected row with the PSD, the PTOD function is used. From Table G, it is determined that for a scan, the source select is S1, and the device select is NO3. Using this information, the complete code to perform the scan is 6-103. The scan information will be displayed in the AUX display after XEQ is depressed. With the office scan/distribute connectors in place and the CONT XEQ switch up, the display will be updated as the scan leads change and efforts to change the state of the faulty scan point can be monitored.

5.14 ¶The N₁ leads in Table G represent the NI(0-3) leads from the procon, the N(A-D) leads at the interface controller circuit pack, or the DS(0-3) on the control bus. These leads are shown in binary format. The binary "1" indicates a high on the NI(0-3) leads from the procon.¶

I. External Distribute Tests

5.15 If the trouble is suspected to be a distribute but in circuitry external to the PSD, a test can be performed on the distribute point that is not responding. In this case, the distribute row is entered in the ADDR register (code = 2-*nnn* HI/LO), the distribute point data is entered in the DATA register (code = 3-*nnn* HI/LO) and the distribute is performed with destination D1 and device select N04 (code = 5-104). While executing this command, the office points being controlled can be monitored for the correct response.

J. I/O Port Routine Exercise

5.16 The I/O ports are tested by looping the output back on the input of the port. This looping is accomplished with a cross-connect plug that is attached at the I/O connector. The maintenance routines are informed that a particular data port should be tested when its associated I/O switch is up. A reset followed by an execute, with the PROG SELECT switch set to 0 and the DATA switches set to 017, automatically sequences the I/O port test outlined in the following paragraphs. Effective use of the following information requires a working knowledge of the data channel interface (FB598) circuit.

5.17 The first test sequence checks the capability of the data port to respond to procon commands as follows:

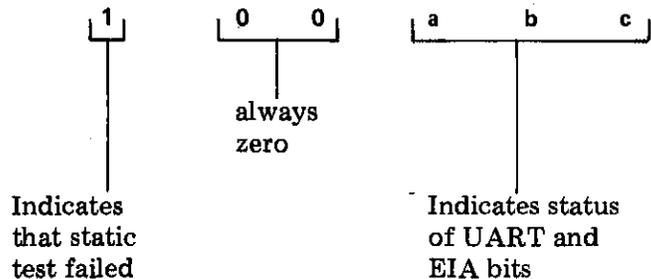
- (a) Read Data Port status should initially be in the reset condition. Verify normal reset conditions.
- (b) Read Data Port EIA status and verify reset condition.
- (c) Write Data Port status and verify EIA status written.

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This concludes the static test. A failure is indicated by a nonzero TLN. The AUX register contains the record of the failure. To determine which UART and/or EIA status bits are at the "1" state, an octal to binary conversion must first be made for each of the least three significant octal digits in the display. The following list provides octal-binary conversion:

OCTAL NUMBER	BINARY EQUIVALENT
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

5.18 The AUX register contains the static test failure as follows:



5.19 To determine the status of the UART and/or EIA bits:

- (1) Convert digits a, b, and c in paragraph 5.18 to binary per listing in paragraph 5.17.

- (2) Apply binary equivalents to the following table to determine status of UART and EIA bits:

(a)			(b)			(c)			UART Status
DR	TRE	THRE	OE	FE	PE	CA	CD	CF	EIA Status
SCA	SCF	CC	CB	CE	CF	CD	CA	CF	EIA Status

Example 1: AUX register indicates 100320. The binary equivalent of octal 320 is (a) 011, (b) 010, (c) 000. The UART or EIA bits at the "1" state are: UART = TRE, EIA = SCA, SCF, and CB.

Example 2: AUX register indicates 100236. The binary equivalent of octal 236 is (a) 010, (b) 011, (c) 110. The UART or EIA bits at the "1" state would be: UART = TRE, THRE, OE and FE, EIA = SCA, CB, CE, CF and CD.

Note: The test does not discriminate between the UART status and the EIA status for the "b" and "c" digits.

If the above static tests pass, the dynamic test is executed.

5.20 For the dynamic test, send/receive data is looped around through cross-connects on the I/O port. The following sequence is executed four times:

- (1) Pass 1 - 8 bit data, two stop bits, even parity
 Pass 2 - 7 bit data, one stop bit, even parity
 Pass 3 - 6 bit data, two stop bits, odd parity
 Pass 4 - 5 bit data, one stop bit, odd parity
- (2) Send data.
- (3) Verify TRE and THRE sequencing (AUX register is 6544 or 6454 if sequencing fails).
- (4) Send data complement.
- (5) Verify DR gets set with no error indicators set (OE, PE, and FE = 0).

- (6) Read data.
- (7) If 8-bit data, check data for errors.
- (8) Read data complement and check if 8-bit data.

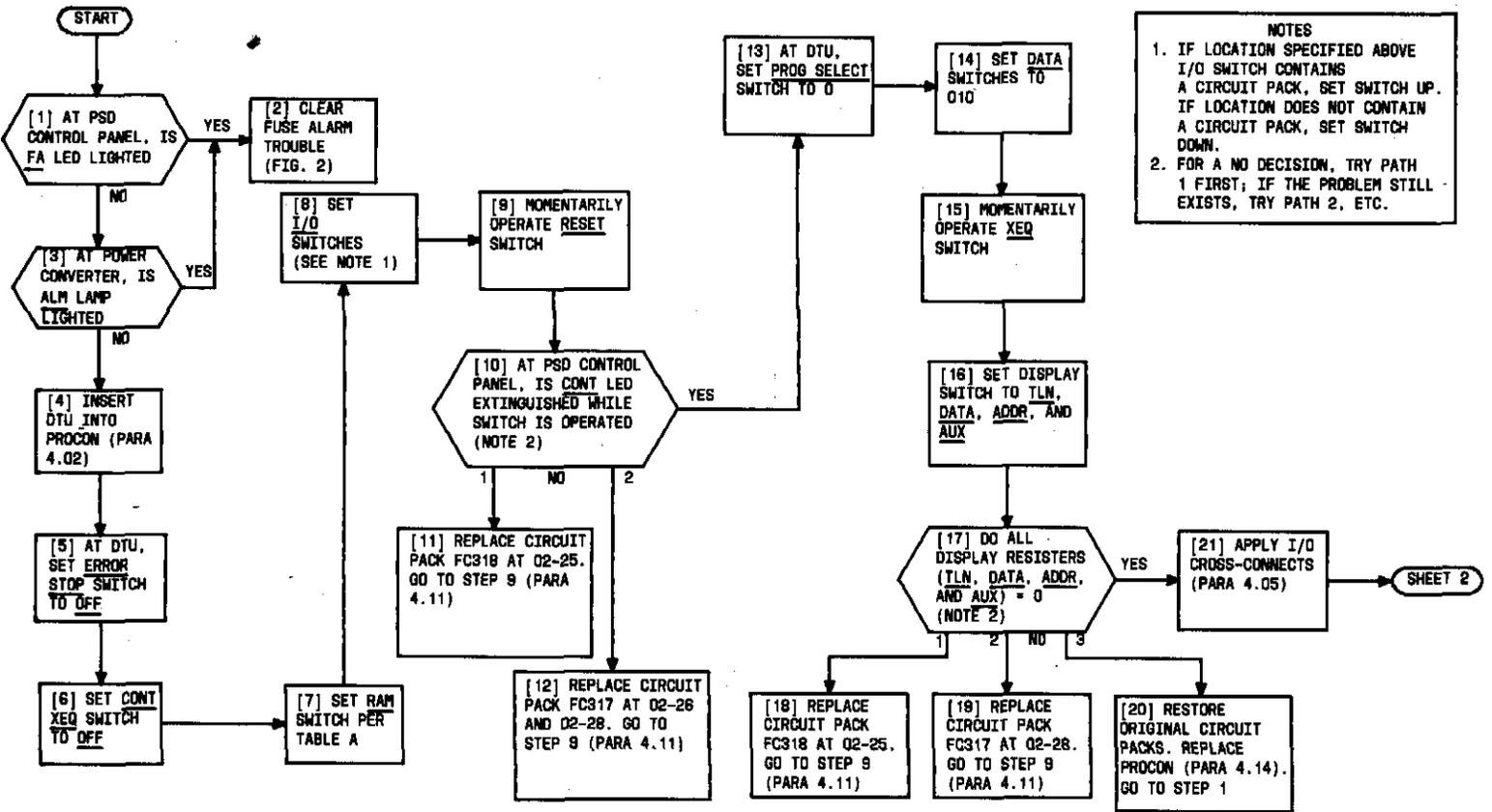
K. Scan/Distribute Cross-Connect

5.21 A distribute can be initiated with the information in paragraph 5.05. The result can be observed using a scan with the scan/distribute cross-connect applied. The cross-connect assignments are given in Table E. **Example:** A distribute of address 004 to address 002 will cause ones to

appear in bit positions 2 and 8 of scan rows 8, 9, 10, and 11 when these rows are subsequently scanned.

5.22 To perform a directed distribute, set the ADDR register to the distribute row address, set the DATA register to distribute data, set PGM SELECT switch to 5, and set DATA switches to 104.

5.23 To perform a directed scan, set the ADDR register to the scan row address, set PROG SELECT switch to 6, and set DATA switches to 103. The scan result is displayed in the AUX register.



NOTES

1. IF LOCATION SPECIFIED ABOVE I/O SWITCH CONTAINS A CIRCUIT PACK, SET SWITCH UP. IF LOCATION DOES NOT CONTAIN A CIRCUIT PACK, SET SWITCH DOWN.
2. FOR A NO DECISION, TRY PATH 1 FIRST; IF THE PROBLEM STILL EXISTS, TRY PATH 2, ETC.

Fig. 1—Clear PSD Trouble (Sheet 1 of 4)

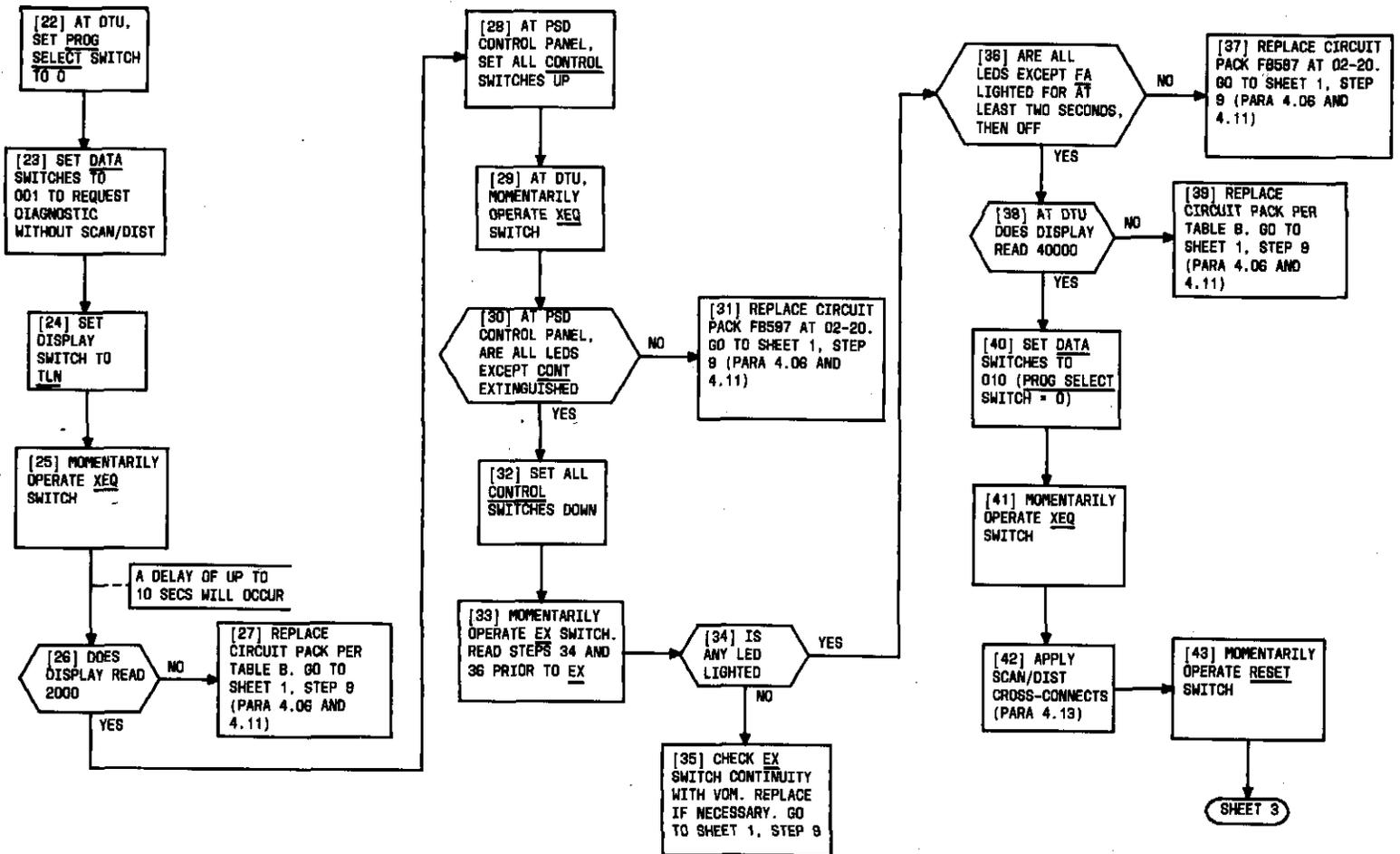


Fig. 1—Clear PSD Trouble (Sheet 2 of 4)

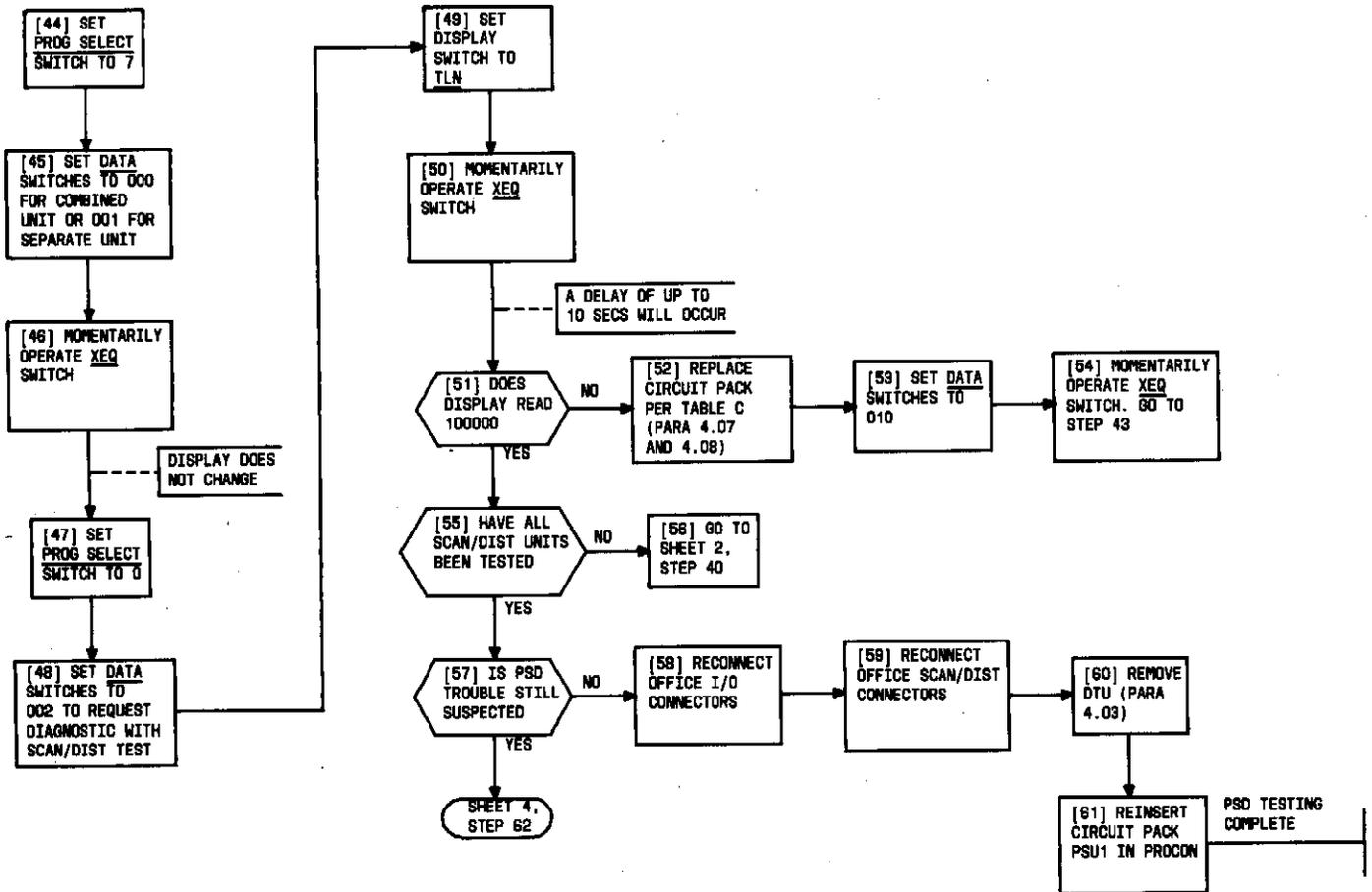


Fig. 1—Clear PSD Trouble (Sheet 3 of 4)

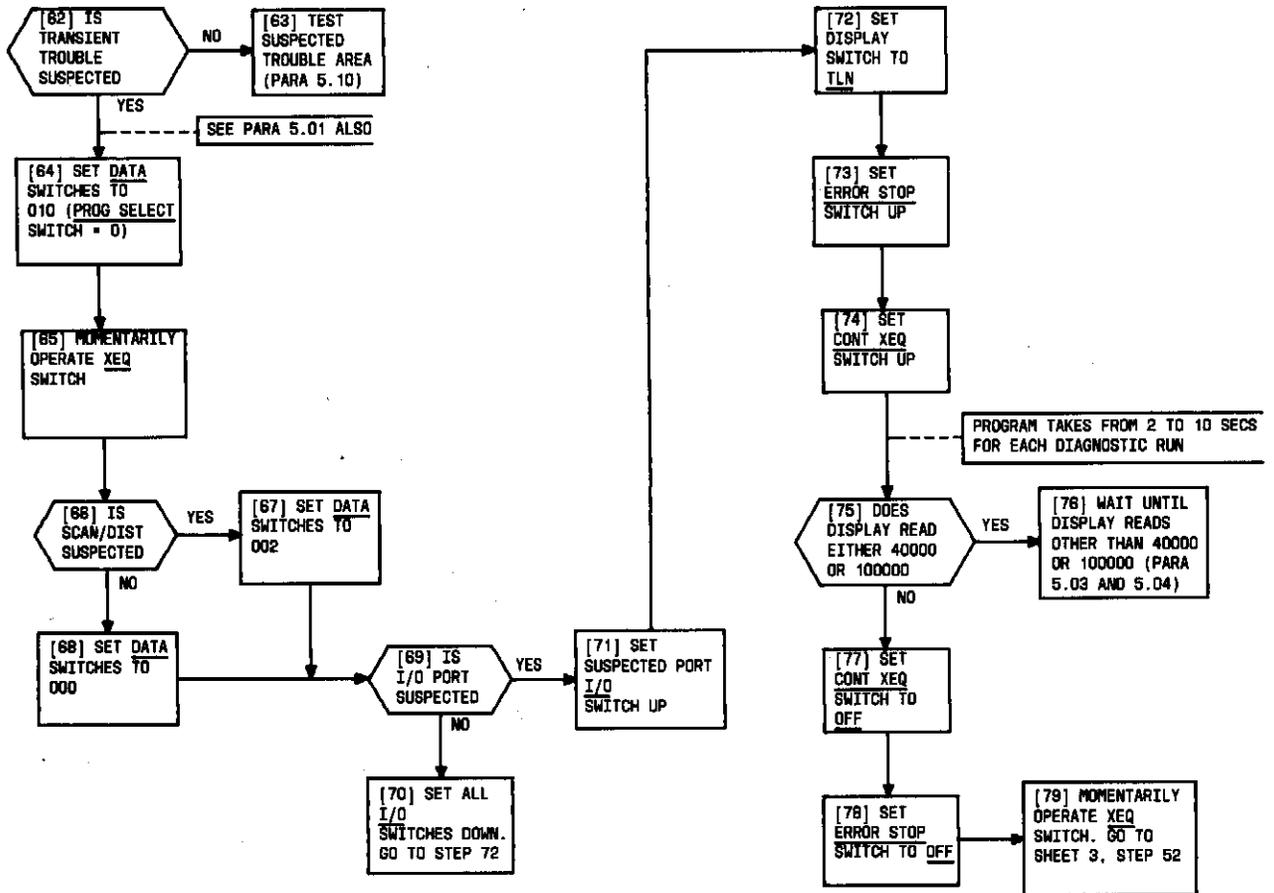
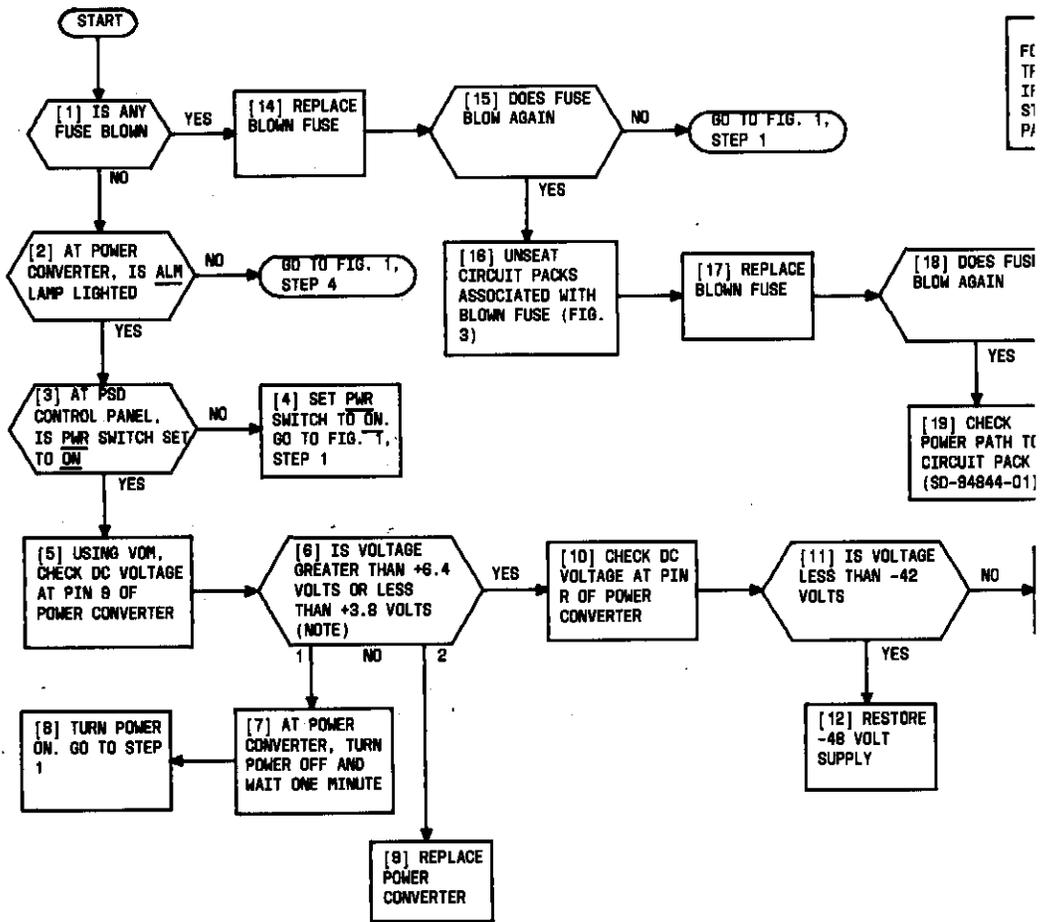


Fig. 1—Clear PSD Trouble (Sheet 4 of 4)



FC
TF
IF
SF
PF

NOTE
FOR A NO DECISION,
TRY PATH 1 FIRST;
IF THE PROBLEM
STILL EXISTS, TRY
PATH 2.

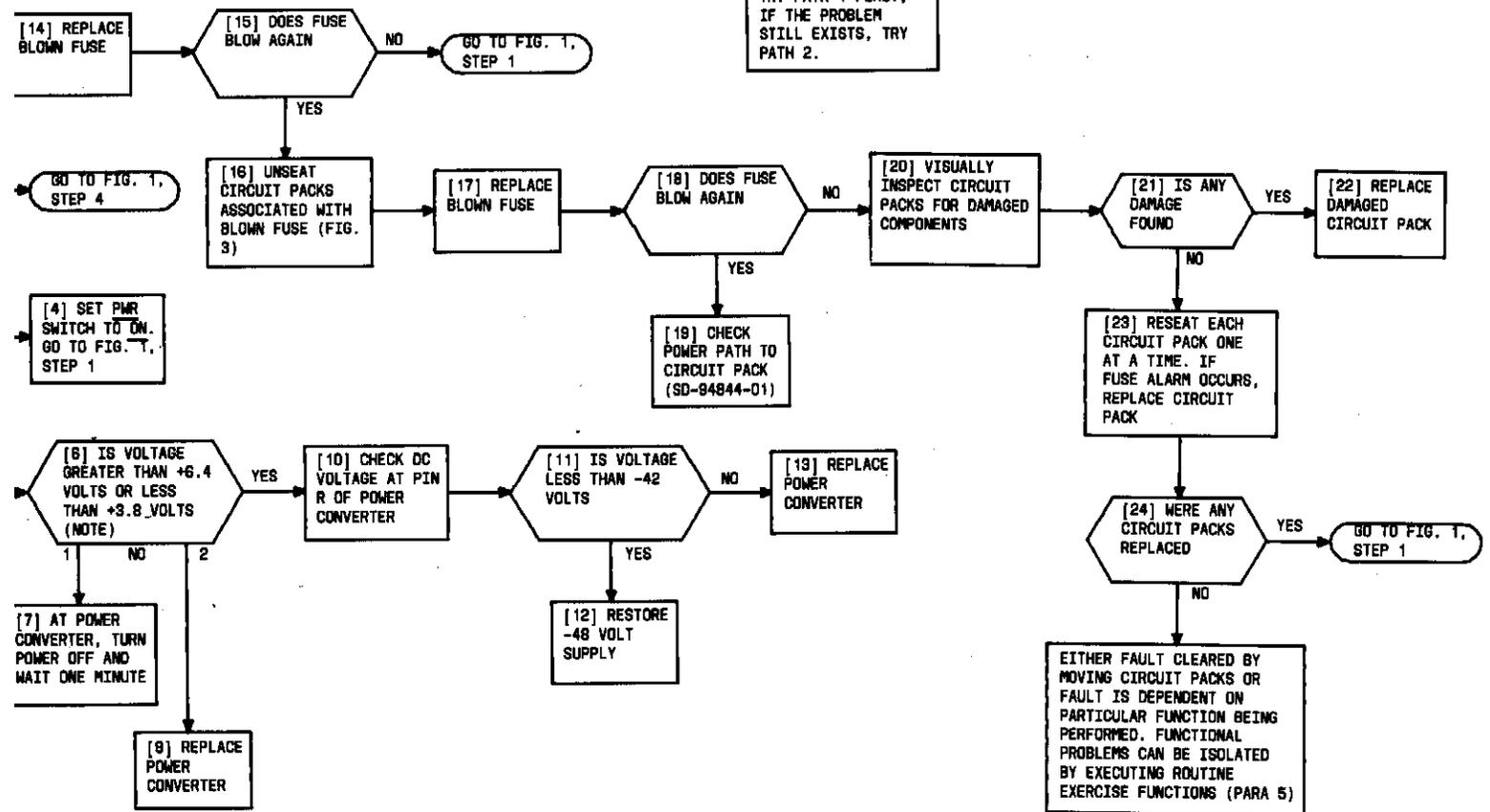


Fig. 2—Clear Fuse Alarm

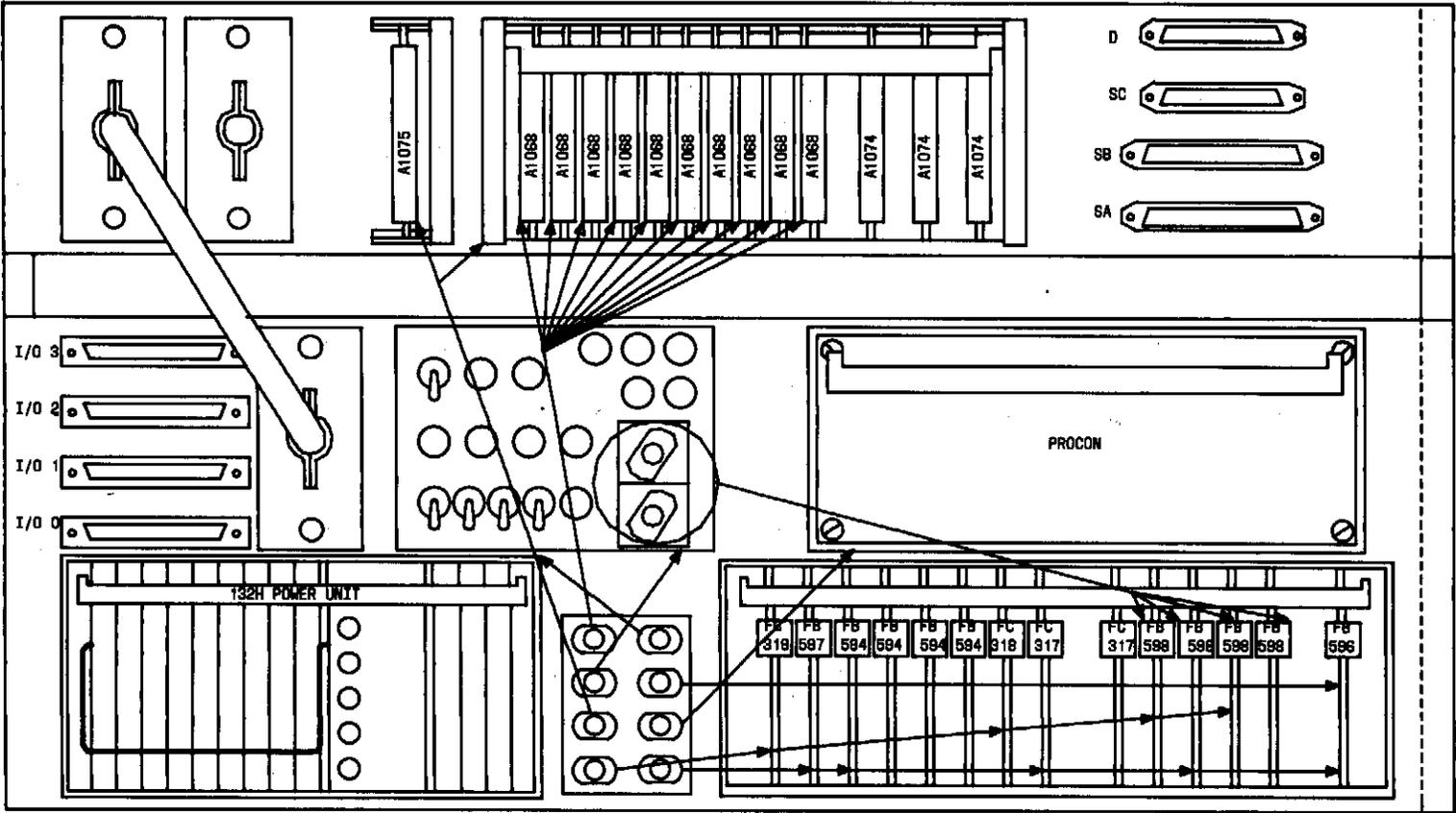


Fig. 3—Fuse Assignment Diagram

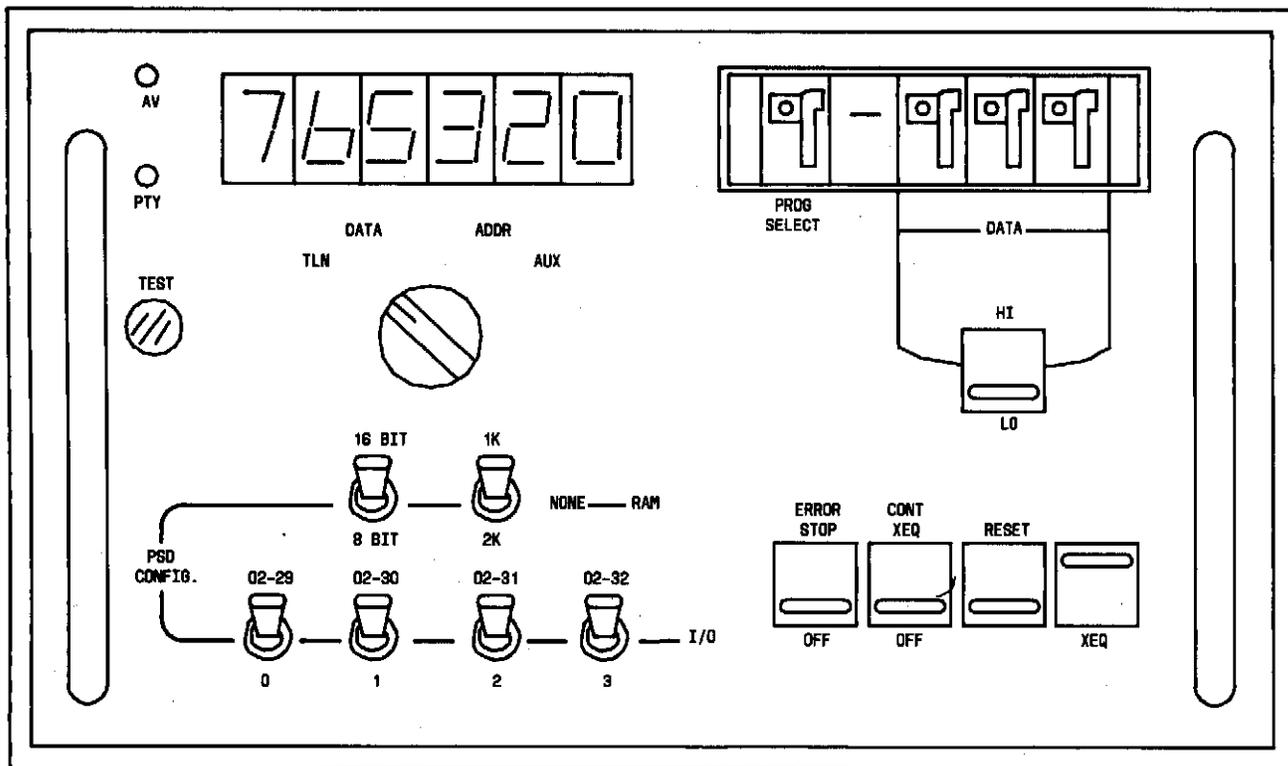


Fig. 4—DTU Control Panel

TABLE A
RAM SWITCH SETTINGS

FB594 CIRCUIT PACK LOCATION*				SET RAM SWITCHES TO
02-21	02-22	02-23	02-24	
X	X	X	X	2K-16 BIT
	X	—	X	2K-8 BIT
—	—	X	X	1K-16 BIT
—	—	—	X	1K-8 BIT
—	—	—	—	NONE

* X denotes an equipped location.

TABLE B
TROUBLE NUMBERS

TLN DISPLAY	REPLACE CIRCUIT PACK (SEE NOTE)		TLN DISPLAY	REPLACE CIRCUIT PACK (SEE NOTE)	
	CP LOCATION	CP CODE		CP LOCATION	CP CODE
11	02-25	FC318	216	02-25	FC318
11	02-26	FC317	216	02-22	FB594
12	02-26	FC317	227	02-25	FC318
12	02-25	FC318	401	02-25	FC318
14	02-25	FC318	416	02-22	FB594
16	02-26	FC317	426	02-24	FB594
22	02-26	FC317	426	02-25	FC318
26	02-28	FC317	427	02-25	FC318
26	02-25	FC318	1001	02-25	FC318
27	02-25	FC318	1001	02-22	FB594
32	02-21	FB594	1001	02-19	FC319
32	02-22	FB594	2001	02-20	FB597
32	02-19	FC319	2001	Control Switch	
32	02-20	FB597	4002	02-29	FB598
32	02-25	FC318	4002	02-25	FC318
32	02-32	FB598	4002	02-19	FC319
32	02-28	FC317	4002	02-34	FB596
36	02-28	FC317	10002	02-30	FB598
37	02-25	FC318	10002	02-34	FB596
44	02-28	FC317	10002	02-19	FC319
46	02-28	FC317	20002	02-31	FB598
46	02-25	FC318	20002	02-32	FB598
47	02-26	FC317	20002	02-34	FB596
47	02-28	FC317	20002	02-19	FC319
47	02-25	FC318	40000	All tests pass (without scan/ dist test)	
66	02-26	FC317		02-32	FB598
101	02-25	FC318	40002	02-22	FB594
106	02-25	FC318	40002	02-34	FB596
106	02-22	FB594	40002	02-19	FC319
106	02-24	FB594	40002	All tests pass	
156	02-24	FB594	100000	See Table C	
201	02-20	FB597	100001		
201	02-25	FC318			
201	02-32	FB598			
201	02-19	FC319			
206	02-21	FB594			
212	02-23	FB594			
212	02-24	FB594			
212	02-22	FB594			
212	02-28	FC317			
212	02-26	FC317			
212	02-25	FC318			

Note: Circuit packs are located in the I/O, interface, and RAM unit.

TABLE C
TROUBLE NUMBER 100001

COMBINED SCAN/DIST					
AUX DISPLAY	REPLACE CIRCUIT PACK (SEE NOTES)		AUX DISPLAY	REPLACE CIRCUIT PACK (SEE NOTES)	
	CP LOCATION	CP CODE		CP LOCATION	CP CODE
0	02-19	FC319	1010	CU-30	A1074
0	CU-16	A1075	1010	CU-20	A1068
1	CU-16	A1075	1376	CU-16	A1075
2	CU-18	A1068	1400	Check cross-connect	
4	CU-19	A1068	1414	CU-30	A1074
4	02-28	FC317	1777	CU-16	A1075
4	02-19	FC319	1777	02-19	FC319
10	CU-20	A1068	2000	02-19	FC319
17	Check cross-connect		4000	02-19	FC319
20	02-19	FC319	10000	02-19	FC319
20	CU-21	A1068	20000	02-19	FC319
20	CU-32	A1074	40000	02-19	FC319
40	CU-22	A1068	100000	02-19	FC319
40	CU-32	A1074	176000	See Table F, code 7-nnn and Fig. 1, Steps 44, 45, and 46	
40	02-19	FC319			
60	CU-32	A1074	SEPARATE SCAN/DIST		
100	CU-23	A1068	0	02-19	FC319
100	CU-16	A1075	0	SU-16	A1070
100	02-19	FC319	1	SU-17	A1068
100	02-22	FB594	1	DU-18	A1074
100	02-25	FC318	2	SU-18	A1068
101	CU-28	A1074	2	DU-18	A1074
101	CU-17	A1068	2	DU-18	A1074
101	02-19	FC319	3	DU-18	A1074
200	CU-24	A1068	4	SU-19	A1068
200	02-19	FC319	4	DU-20	A1074
202	CU-28	A1074	4	SU-16	A1070
202	CU-18	A1068	4	02-19	FC319
202	02-19	FC319	4	02-28	FC317
303	CU-28	A1074	4	SU-20	A1068
360	Check cross-connect		10	DU-20	A1074
400	CU-25	A1068	10	SU-16	A1070
400	02-19	FC319	10	DU-16	A1071
400	02-26	FC317	10	DU-20	A1074
404	CU-30	A1074	14	02-19	FC319
404	CU-19	A1068	20	02-22	FB594
404	02-19	FC319	20	SU-21	A1068
500	CU-16	A1075	20	DU-22	A1074
500	02-19	FC319	20	SU-16	A1070
577	CU-16	A1075	20	DU-16	A1071
1000	CU-26	A1068	20	DU-16	A1071
1000	02-19	FC319	34	SU-22	A1068
1000	02-26	FC317	40		

TABLE C (Contd)
TROUBLE NUMBER 100001

SEPARATE SCAN/DIST					
AUX DISPLAY	REPLACE CIRCUIT PACK (SEE NOTES)		AUX DISPLAY	REPLACE CIRCUIT PACK (SEE NOTES)	
	CP LOCATION	CP CODE		CP LOCATION	CP CODE
40	DU-22	A1074	20000	SU-30	A1068
40	02-19	FC319	20000	DU-30	A1074
60	DU-22	A1074	20000	02-19	FC319
60	SU-16	A1070	30000	DU-30	A1074
60	DU-16	A1071	40000	SU-31	A1068
77	DU-16	A1071	40000	DU-32	A1074
100	02-19	FC319	40000	02-19	FC319
100	SU-23	A1068	100000	SU-32	A1068
100	DU-24	A1074	100000	DU-32	A1074
100	02-25	FC318	100000	02-19	FC319
101	02-19	FC319	100010	SU-32	A1070
120	02-19	FC319	140000	DU-32	A1074
200	02-19	FC319	177000	DU-16	A1071
200	SU-24	A1068	177777	DU-16	A1071
200	DU-24	A1074			
202	02-19	FC319			
300	DU-24	A1074			
400	02-19	FC319			
400	02-26	FC317			
400	SU-25	A1068			
400	DU-26	A1074			
500	02-19	FC319			
1000	02-19	FC319			
1000	02-26	FC317			
1000	SU-26	A1068			
1000	DU-26	A1074			
1400	DU-26	A1074			
1777	02-19	FC319			
2000	SU-27	A1068			
2000	DU-28	A1074			
2000	02-19	FC319			
4000	SU-28	A1068			
4000	DU-28	A1074			
4000	02-19	FC319			
6000	DU-28	A1074			
10000	SU-29	A1068			
10000	DU-30	A1074			
10000		FC319			

Note 1: Circuit packs designated CU- _ are located in the scan/distribute matrix.

Note 2: Circuit packs designated 02- _ are located in the I/O, interface, and RAM unit.

Note 3: Circuit packs designated SU- _ are located in the scanner matrix.

Note 4: Circuit packs designated DU- _ are located in the distributor matrix.

TABLE D

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
11	0	0	177771	02-25	FC318	0-007 or 0-204. RTOV not getting reset.
11	0	0	177777	02-25	FC318	G-007. RTOV not getting set.
11	0	0	177777	02-26	FC317	G-300
12	400	0	0			G-317
12	1000	0	0			G-314
12	2000	0	0			G-218
12	4000	0	0			G-217
12	10000	0	0			G-307
12	20000	0	0			G-207
12	40000	0	0			G-308
12	100000	0	0	02-26	FC317	G-208
12	177400	0	0	02-25	FC318	0-012
14	XXX	0	0	02-25	FC318	Peripheral decoding.
16	XXX	0	0	02-26	FC317	Failed loop thru pack. DATA display is failing bits.
16	400	0	0			0-217 or 0-317
16	1000	0	0			0-314
16	2000	0	0			0-218
16	20000	0	0			0-207
16	10000	0	0			0-307
16	40000	0	0			0-308
16	100000	0	0			0-208
16	177400	0	0			Pack out
22	XXX000	0	17777X			Real time clock. DATA display is failing bits.
22	XXX400	0	17777X			Real time clock. DATA display is failing bits.
22	400	0	177771			IC3-G-14
22	1000	0	177771			IC3-G-13
22	2000	0	177771			IC3-G-12
22	4000	0	177771			IC3-G-11
22	170000	0	177777			IC3-G-15
22	177400	0	177771	02-26		0-016 or G-016
26	XXX	0	0	02-28		Address register. DATA display is failing bits.
26	1	0	0			IC10-G-16, 1
26	2	0	0			IC10-G-14, 15
26	4	0	0			IC10-G-10, 11
26	10	0	0			IC10-G-8, 9
26	17	0	0			IC15-G-4
26	20	0	0			IC11-G-10, 11
26	40	0	0			IC11-G-8, 9
26	100	0	0			IC11-G-14, 15
26	200	0	0			IC11-G-1, 16
26	360	0	0			IC15-G-2
26	377	0	0			IC13-G-7, IC15-0-15, IC15-G-15, 0-101, or G-101
26	3X8	28	3X8	02-28	FC317	G-309 or 0-309

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
26	377	0	0	02-25	FC318	0-115 or G-115
27	XXX	0	0			Address register gating.
27	177XX7	20	177XX0			0-018
27	177777	0	0			G-316, 0-216, 0-015, G-015, 0-206, 0-306
32	0	0	0	02-25	FC318	0-004, 0-016, G-016
32	1	0	0	02-32	FB598	G-207
32	1	0	0	02-22	FB594	G-207
32	1	0	0	02-20	FB597	G-207
32	1	0	0	02-19	FC319	G-005
32	2	0	0	02-22	FB594	G-008
32	2	0	0	02-20	FB597	G-008
32	4	0	0	02-22	FB594	G-208
32	4	0	0	02-20	FB597	G-208
32	4	0	0	02-19	FC319	G-006
32	10	0	0	02-22	FB594	G-009
32	10	0	0	02-20	FB597	G-208
32	10	0	0	02-19	FC319	G-206
32	20	0	0	02-22	FB594	G-209
32	20	0	0	02-20	FB597	G-209
32	20	0	0	02-19	FC319	G-007
32	40	0	0	02-25	FC318	G-006
32	40	0	0	02-22	FB594	G-010
32	40	0	0	02-19	FC319	G-207
32	100	0	0	02-22	FB594	G-210
32	100	0	0	02-19	FC319	G-008
32	200	0	0	02-22	FB594	G-011
32	200	0	0	02-19	FC319	G-208
32	377	0	0	02-28	FC317	IC13-G-6
32	400	0	0	02-21	FB594	G-207
32	400	0	0	02-19	FC319	G-009
32	1000	0	0	02-21	FB594	G-008
32	1000	0	0	02-19	FC319	G-209
32	2000	0	0	02-21	FB594	G-208
32	2000	0	0	02-19	FC319	G-010
32	4000	0	0	02-21	FB594	G-009
32	4000	0	0	02-19	FC319	G-210
32	10000	0	0	02-21	FB594	G-209
32	10000	0	0	02-19	FC319	G-011
32	20000	0	0	02-21	FB594	G-010
32	20000	0	0	02-19	FC319	G-211
32	40000	0	0	02-21	FB594	G-210
32	40000	0	0	02-19	FC319	G-012
32	100000	0	0	02-21	FB594	G-011
32	100000	0	0	02-19	FC319	G-212
32	177777	0	0	02-25	FC318	G-216

See para. 4.10

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
36	XXX	0	0	02-28	FC317	Failed loop thru pack. DATA display is failing bits.
36	377	0	0	02-28	FC317	Pack out
37	XXX	0	0	02-25	FC318	DATA display is failing bits.
37	177777	0	0	02-25	FC318	0-205 or G-205
44	XXX	XXX	XXX	02-28	FC317	DATA display is failing bits.
46	XXX	0	177771	02-28	FC317	Real time clock. DATA display is failing bits.
46	1	0	177771	02-28	FC317	IC3-G-7, 10, 14
46	1	0	177771	02-25	FC318	0-010, G-005, G-300
46	2	0	177771	02-28	FC317	IC3-G-13
46	4	0	177771			IC3-G-12
46	7	0	177771			G-104
46	10	0	177771			IC3-G-11
46	110	0	177771			0-104
46	202	0	177771			0-002
46	377	0	177771	02-28	FC317	IC3-G-1, IC13-G-10
47	XXX	0	177771	02-25	FC318	Real time clock gating
47	XXX001	0	177771	02-26	FC317	G-104
47	XXX401	0	177771	02-26	FC317	G-104
47	177602	0	177771	02-28	FC317	Shorted address leads
47	177760	0	177777	02-28	FC317	IC16-G-7, 10
47	177777	0	177771	02-25	FC318	G-018, IC13-G-3
66	400	0	0	02-26	FC317	G-008, IC12-G-11
66	1000	0	0			G-009, IC12-G-9, 10
66	2000	0	0			G-109, IC12-G-9
66	4000	0	0			G-108, IC12-G-10
66	10000	0	0			G-206, IC12-G-12
66	20000	0	0			G-006, IC12-G-2
66	40000	0	0			G-106, IC12-G-13
66	100000	0	0	02-26	FC317	G-105, IC12-G-1
101	0	X777	377	02-25	FC318	0-114 or G-114
106	0	3777	0	02-22	FB594	G-211
106	0	3777	0	02-25	FC318	0-207, G-207, 0-215
106	0	3777	0	02-24	FB594	Pack out
106	0	3777	377	02-25	FC318	0-111, 0-108, 0-203
106	0	3777	10000	02-25	FC318	G-111, 0-305, G-305
156	20	0	0	02-24	FB594	DATA display is failing bits.
201	0	X777	XXX	02-20	FB597	Trouble register failed. AUX display is failing bits.
201	0	X777	0			IC3-G-8
201	0	X777	1			0-207, IC8-G-1
201	0	X777	2			0-008, IC8-G-7
201	0	X777	4			0-208, IC8-G-15
201	0	X777	10			0-009, IC8-G-9, or power fusing
201	0	X777	20			0-209, or power fusing
201	0	X777	37	02-20	FB597	0-G-201, 0-G-002, 0-G-003, 0-G-004, 0-G-203

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
201	0	X777	37	02:25	FC318	IC15-G-14
201	0	X777	37	02-19	FC319	G-001, G-203
201	0	1777	37	02-32	FB598	G-203
201	0	X777	40	02-25	FC318	0-013, 0-006, IC4-G-15, IC12-G-1, 2, 6
201	0	X777	40			Trouble register failed. AUX display is failing bits.
201	0	X777	77	02-25	FC318	0-304
201	0	1777	37	02-32	FB598	G-001, G-203
201	0	3777	37	02-25	FC318	0-002, 0-003, G-001, 0-201
206	0	3777	0	02-22	FB594	0-012
206	400	3777	0	02-21		0-207
206	1000	3777	0			0-008
206	2000	3777	0			0-208
206	4000	3777	0			0-009
206	10000	3777	0			0-209
206	20000	3777	0			0-010
206	40000	3777	0			0-210
206	100000	3777	0			0-011
206	177400	3777	0	02-21	FB594	
212	0	X777	0	02-25	FC318	IC14-G-14
212	0	1777	0	02-25	FC318	0-G-207, 0-215
212	0	3777	0	02-22	FB594	G-218
212	210	1777	0	02-24	FB594	Pack out
212	0000XX	X777	0	02-28	FC317	Open in bidirection bus. DATA display is failing bits.
212	0001XX	X777	0			Open in bidirection bus. DATA display is failing bits.
212	0002XX	X777	0	02-28	FC317	Open in bidirection bus. DATA display is failing bits.
212	XXX000	X777	0	02-23	FB594	RAM trouble. DATA display is failing bits.
212	XXX000	X777	0	02-26	FC317	Open in bidirection bus. DATA display is failing bits.
212	XXX400	X777	0	02-23	FB594	RAM trouble. DATA display is failing bits.
212	4000	X777	0			IC13-G-6
212	1000	X777	0			IC18-G-2
212	1000	1777	0			0-008
212	2000	X777	0			IC18-G-12
212	2000	1777	0			0-208
212	10000	X777	0			IC13-G-10
212	10000	1777	0			0-009
212	20000	X777	0			IC13-G-12
212	20000	1777	0	02-23	FB594	0-010

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
212	40000	X777	0	02-23	FB594	IC13-G-4
212	40000	1777	0			0-210
212	100000	X777	0			IC13-G-2
212	100000	1777	0			0-011
212	177400	1777	0	02-23	FB594	0-005 or pack out
216	377	3777	0	02-25	FC318	0-G-108
216	377	3777	0	02-22	FB594	G-018
227	50021	3777	0	02-25	FC318	0-G-305
401	0	X777	1			Sanity timer failed to reset.
401	0	X777	2			Sanity time too short (less than 70 msec).
401	0	X777	3	02-25	FC318	Sanity time too long (more than 110 msec).
416	1	3777	0	02-22	FB594	0-207
416	2	3777	0			0-008
416	4	3777	0			0-208
416	10	3777	0			0-009, IC13-G-6
416	20	3777	0			0-209, IC13-G-10
416	40	3777	0			0-010, IC13-G-12
416	100	3777	0			0-210, IC13-G-4
416	200	3777	0			0-011, IC13-G-2
416	377	3777	0	02-22		0-G-005, 0-018, 0-201, 0-203
426	2	3777	0	02-24		0-008
426	4	3777	0			0-208
426	10	3777	0			0-009
426	20	3777	0			0-209
426	40	3777	0			0-010
426	100	3777	0			0-210
426	200	3777	0	02-24	FB594	0-011
426	377	1777	0	02-25	FC318	0-G-108
426	377	3777	0	02-24	FB594	0-G-005, 0-201, 0-203, or pack out
427	50021	1777	0	02-25	FC318	0-G-305
427	177777	1777	0			0-G-108
1001	0	0	2			0-G-108
1001	0	X777	1	02-25	FC318	Address verify passed on bad RAM-read, G-318.
1001	0	X777	1	02-19	FC319	G-204
1001	0	X777	2	02-25	FC318	Address verify passed on bad RAM-write.
1001	0	X777	3			Address verify passed on bad scan.
1001	0	X777	4	02-25	FC318	Address verify passed on bad distribute.
1001	0	3777	1	02-22	FB594	G-012, 0-218
2000	XXX	XXX	XXX			See Fig. 1, Step 26.

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
20002	125	4	6454	02-19	FC319	G-004
20002	125	4	6544	02-31	FB598	Oscillator trouble.
20002	125	X777	100177	02-34	FB596	Pack out
40000	XXX	XXX	XXX	All tests pass (without scan/dist test).		
40002	125	XXX	100174	02-32	FB598	No cross-connect on I/O port 3.
40002	125	1	100004			0-216
40002	125	1	100020			0-015
40002	125	1	100024			0-G-017, G-015, G-216
40002	125	1	100040			0-013
40002	125	1	100050			0-G-215, G-013
40002	125	1	100070			G-201
40002	125	1	100377	02-32	FB598	0-203
40002	125	4	1	02-22	FB594	0-207
40002	125	4	6454	02-32	FB598	0-001 or pack out
40002	125	4	6454	02-19	FC319	G-004
40002	125	4	6544	02-32	FB598	Oscillator trouble
40002	125	X777	100177	02-34	FB596	Pack out
100000	XXX	XXX	XXX	All tests pass		
100001	0	0	100	02-19	FC319	0-004, 0-G-201, 0-203, G-301, G-316 (CU)
100001	0	0	100	02-19	FC319	0-001, 0-002, 0-G-003, 0-303 (CU)
100001	0	0	100	02-25	FC318	G-002, G-003
100001	0	0	100	02-22	FB594	G-015, G-016, G-215, G-216 (CU)
100001	0	0	20	02-22	FB594	G-015, G-016, G-215, G-216 (SU)
100001	0	0	20	SU-16	A1070	0-005, 0-008, or cross-connect
100001	0	0	20	DU-16	A1071	0-000, 0-001, 0-007
100001	0	0	34	DU-16	A1071	0-020, 0-021, 0-022, 0-023
100001	0	0	60	SU-16	A1070	0-004, 0-006, 0-009
100001	0	0	60	DU-16	A1071	0-005, 0-006, 0-008, 0-009, 0-010
100001	0	0	100	CU-16	A1075	0-005, 0-006
100001	0	0	500	02-19	FC319	0-316
100001	0	0	500	CU-16	A1075	0-011, 0-016, 0-017, 0-019
100001	0	0	500	02-19	FC319	0-G-015, 0-G-215, 0-G-016, 0-G-216 (CU)
100001	0	0	120			0-G-015, 0-G-016, 0-G-215, 0-G-216 (SU-DU)
100001	0	0	20	02-19	FC319	0-G-004, 0-G-201, 0-203, G-301, G-316, G-003, 0-001, 0-002, 0-303 (SU-DU)
100001	1	0	1	CU-17	A1068	0-011, 012, 013, 014, 015, 016, 017, 018, 020, 021, 022, 023, 024, 025, 026, 027
100001	1	0	1	SU-17		
100001	1	0	2	CU-18	A1068	0-011, 012, 013, 014, 015, 016, 017, 018, 020, 021, 022, 023, 024, 025, 026, 027

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
100001	1	0	2	SU-18	A1068	0-011, 012, 013, 014, 015, 016, 017, 018, 020, 021, 022, 023, 024, 025, 026, 027
100001	1	0	4	CU-19		
100001	1	0	4	SU-19		
100001	1	0	10	CU-20		
100001	1	0	10	SU-20		
100001	1	0	20	CU-21		
100001	1	0	20	SU-21		
100001	1	0	40	CU-22		
100001	1	0	40	SU-22		
100001	1	0	100	CU-23		
100001	1	0	100	SU-23		
100001	1	0	200	CU-24		
100001	1	0	200	SU-24		
100001	1	0	400	CU-25		
100001	1	0	400	SU-25		
100001	1	0	1000	CU-26		
100001	1	0	1000	SU-26		
100001	1	0	2000	SU-27		
100001	1	0	4000	SU-28		
100001	1	0	10000	SU-29		
100001	1	0	20000	SU-30		
100001	1	0	40000	SU-31		
100001	1	0	100000	SU-32		0-011, 012, 013, 014, 015, 016, 017, 018, 020, 021, 022, 023, 024, 025, 026, 027
100001	4	0	1	CU-17		0-000, 007, 009, or pack out
100001	4	0	1	SU-17	A1068	0-000, 004, 007, 009
100001	4	0	1	DU-18	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	2	CU-18	A1068	0-000, 007, 009, or pack out
100001	4	0	2	DU-18	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	3	DU-18	A1074	0-004, 006, 007, 008, 009, or pack out
100001	4	0	4	02-28	FC317	0-G-005
100001	4	0	4	CU-19	A1068	0-000, 007, 009, or pack out
100001	4	0	4	SU-16	A1070	0-023, 026
100001	4	0	4	CU-16	A1075	0-000, 002, 003, 004, 007, 024
100001	4	0	4	DU-20	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	4	02-19	FC319	0-109 (SU-DU)
100001	4	0	10	CU-20	A1068	0-000, 007, 009, or pack out
100001	4	0	10	DU-16	A1071	0-018
100001	4	0	10	SU-16	A1070	0-014, 027

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
100001	4	0	10	CU-16	A1075	0-008, 009, 021
100001	4	0	10	DU-20	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	14			0-004, 006, 007, 008, 009, or pack out
100001	4	0	17	DU-20	A1074	Check cross-connect (CU).
100001	4	0	20	02-19	FC319	0-107
100001	4	0	20	CU-21	A1068	0-000, 007, 009, or pack out
100001	4	0	20	CU-32	A1074	0-012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	20	DU-22	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	40	02-19	FC319	0-G-307
100001	4	0	40	CU-22	A1068	0-000, 007, 009, or pack out
100001	4	0	40	CU-32	A1074	0-013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	40	DU-22		0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	60	CU-32		0-006, 007, 008, 009, or pack out
100001	4	0	60	DU-22	A1074	0-004, 006, 007, 008, 009, or pack out
		0	77	DU-16	A1071	0-002
100001	4	0	100	02-19	FC319	0-108
100001	4	0	100	CU-23	A1068	0-000, 007, 009, or pack out
100001	4	0	100	DU-24	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	101	02-19	FC319	0-105
100001	4	0	101	CU-28	A1074	0-012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	200	02-19	FC319	0-G-308
100001	4	0	200	CU-24	A1068	0-000, 007, 009, or pack out
100001	4	0	200	DU-24	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	202	02-19	FC319	0-305
100001	4	0	202	CU-28	A1074	0-013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	300	DU-24		0-004, 006, 007, 008, 009, or pack out
100001	4	0	303	CU-28		0-006, 007, 008, 009, or pack out
100001	4	0	360	CU-28	A1074	Check cross-connect (CU).
100001	4	0	400	02-19	FC319	0-109
100001	4	0	400	02-26	FC317	0-008
100001	4	0	400	CU-25	A1068	0-000, 007, 009, or pack out
100001	4	0	400	DU-26	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)
TLN	DATA	ADDR	AUX			
100001	4	0	404	02-19	FC319	0-106 (CU)
100001	4	0	404	CU-30	A1074	0-012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	1000	DU-26	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	1000	02-19	FC319	0-G-309
100001	4	0	1000	02-26	FC317	0-009
100001	4	0	1000	CU-26	A1068	0-000, 007, 009, or pack out
100001	4	0	1010	CU-30	A1074	0-013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	1400	DU-26		0-004, 006, 007, 008, 009, or pack out
100001	4	0	1414	CU-30		0-006, 007, 008, 009, or pack out
100001	4	0	2000	DU-28	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	2000	02-19	FC319	0-010
100001	4	0	4000	DU-28	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	4000	02-19	FC319	0-210
100001	4	0	6000	DU-28	A1074	0-004, 006, 007, 008, 009, or pack out
100001	4	0	10000	DU-30	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	10000	02-19	FC319	0-011
100001	4	0	20000	DU-30	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	20000	02-19	FC319	0-211
100001	4	0	30000	DU-30	A1074	0-004, 006, 007, 008, 009, or pack out
100001	4	0	40000	DU-32	A1074	0-000, 012, 015, 016, 019, 020, 023, 024, 027
100001	4	0	40000	02-19	FC319	0-012
100001	4	0	100000	DU-32	A1074	0-002, 013, 014, 017, 018, 021, 022, 025, 026
100001	4	0	100000	02-19	FC319	0-212
100001	4	0	100010	SU-16	A1070	0-002
100001	4	0	140000	DU-32	A1074	0-004, 006, 007, 008, 009 or pack out
100001	4	0	176000			See Table F, code 7-nnn and Fig. 1, Steps 44, 45, and 46
100001	200	0	4	02-19	FC319	Scan dist address error.
100001	400	0	0	02-19	FC319	0-G-304, 0-013, 0-G-213, 0-G-313, 0-G-014, 0-204, G-113, 0-G-214
100001	400	0	0	CU-16	A1075	0-027
100001	400	0	0	SU-16	A1070	0-018
100001	5170	XXX	177			Control panel fuse.

TABLE D (Contd)

DETAILED TROUBLE NUMBER INFORMATION (SEE NOTES)

DISPLAY SWITCH SETTING				CP LOCATION	CP CODE	REASON FOR FAILURE (SEE NOTES 5&6)	
TLN	DATA	ADDR	AUX				
100001	5170	1	XXXXXX	DU-16	A1071	Pack out	
100001	5170	1	XX000	SU-16	A1070	0-003, 017, 019, or pack out	
100001	5170	1	1	CU-17	A1068	0-004, 0-008	
100001	5170	1	2	CU-18		0-004, 0-008	
100001	5170	1	4	CU-19		0-004, 008	
100001	5170	1	10	CU-20		0-004, 008	
100001	5170	1	20	CU-21		0-008	
100001	5170	1	40	CU-22		0-008	
100001	5170	1	100	CU-23		A1068	0-008
100001	5170	1	100	02-19		FC319	G-105 (CU)
100001	5170	1	101	CU-17		A1068	0-008
100001	5170	1	200	CU-24		A1068	0-008
100001	5170	1	200	02-19		FC319	G-305 (CU)
100001	5170	1	202	CU-18	A1068	0-008	
100001	5170	1	400	02-19	FC319	G-106 (CU)	
100001	5170	1	400	CU-25	A1068	0-008	
100001	5170	1	404	CU-19	A1068	0-008	
100001	5170	1	577	CU-16	A1075	Pack out	
100001	5170	1	1000	02-19	FC319	G-306 (CU)	
100001	5170	1	1000	CU-26	A1068	0-008	
100001	5170	1	1010	CU-20	A1068	0-008	
100001	5170	1	1376	CU-16	A1075	0-012, 025, 026	
100001	5170	1	1777	CU-16	A1075	0-001	
100001	5170	1	1777	02-19	FC319	0-301, 0-113, G-313	
100001	5170	1	177700	DU-16	A1071	0-003	
100001	5170	1	177777	DU-16	A1071	0-004, 019	

TABLE D (Contd)

Note 1: Circuit packs designated 02-__ are located in the I/O, interface, and RAM unit.

Note 2: Circuit packs designated CU-__ are located in the combined scan/dist matrix.

Note 3: Circuit packs designated SU-__ are located in the scanner matrix.

Note 4: Circuit packs designated DU-__ are located in the distributor matrix.

Note 5: The following codes are used under "reason for failure":

- (a) 0-nnn — Open on pack pin nnn caused trouble number.
- (b) G-nnn — Ground on pack pin nnn caused trouble number.
- (c) ICaa-0-nn — IC number aa, open on pin nn.
- (d) ICaa-G-nn — IC number aa, ground on pin nn.
- (e) O-G-nnn — Open or ground on pin nnn caused trouble number.

Note 6: The DTU display is an octal notation. Each octal digit corresponds to three binary bits as follows:

OCTAL	BINARY
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

						BINARY BIT POSITION
15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0	
1	7	7	7	7	7	OCTAL REPRESENTATION OF ALL 1's IN BINARY WORD

An octal 100 in the display indicates that bit 6 is a 1. An octal 30 indicates that bits 3 and 4 are both ones.

TABLE E
SCAN/DIST CROSS-CONNECTS

	CONNECT DIST ROW	TO SCAN ROW	CONNECT DIST BIT	TO SCAN BIT
COMBINED UNIT	0	0, 1, 2, 3	0	0, 6
	1	4, 5, 6, 7	1	1, 7
	2	8, 9, 10, 11	2	2, 8
	3	12, 13, 14, 15	3	3, 9
			4	4
			5	5
SEPARATE UNITS	0	0, 1, 2, 3	0	0
	1	4, 5, 6, 7		
	2	8, 9, 10, 11		
	3	12, 13, 14, 15		
			15	15

TABLE F

DTU PROGRAM SELECT CODES

PROGRAM SELECT - DATA	FUNCTION
0-000	PSD Diagnostic (PSDDG) W/O Manual Action
0-001	PSDDG with Manual Action Section
0-002	PSDDG with Scan/Dist Section
0-004	PSDDG All Sections
0-010	Clear the DTU Display and PSD Trouble Register
0-012	REF 0 - Read All RAM Addresses
0-013	REF 1 - Write All RAM Addresses
0-014	REF 2 - Write/Read All RAM Addresses
0-016	REF 3 - SCAN/DIST Exercise
0-017	REF 4 - I/O Port Exercise
1-nnn	RDRAM - Read RAM, nnn is LO Address Bits
2-nnn	LDADDR - Load ADDR Register HI/LO
3-nnn	LDDATA - Load DATA Register HI/LO
4-nnn	WRTRAM - Write RAM, nnn is LO Address Bits
5-dnn	DTOP - DATA TO PERIPHERAL dnn
6-snn	PTOD - PERIPHERAL, snn, TO DISPLAY
7-nnn	OPTSD - Set Scan Distribute Option nnn = 000 Combined Unit nnn = 001 Separate Unit

TABLE G

DEVICE SELECTION CODES

ND NC NB NA		SOURCE SELECT			DESTINATION SELECT				
		S0	S1	S2	D0	D1	D2	D3	
0000	N00	↑	RD CNTL REG			↑	WT CNTL REG	↑	
0001	N01		RD TBL IND REG				WT TBL IND REG		
0010	N02		RD R.T. CLK	RD ADDR REG			WT R.T. CLOCK		
0011	N03		SCAN				RESET SANITY TIMER		
0100	N04						DIST		
0101	N05	READ RAM	RD LO DIAG			WRITE RAM	LO DIAG DISPLAY		
0110	N06		RD MISC DIAG				CLR PTY & AV		
0111	N07		RD HI DIAG				HI DIAG DISPLAY		
1000	N10		RD DPO UART STATUS	RD DPO EIA STATUS				WT DPO STATUS	
1001	N11		RD DPO DATA				WT DPO DATA		
1010	N12		RD DP1 UART STATUS	RD DP1 EIA STATUS			WT DP1 STATUS		

LOAD ADDRESS REGISTER

LOAD ADDRESS REGISTER (LOW 8 BITS)

TABLE G (Contd)

DEVICE SELECTION CODES

ND NC NB NA		SOURCE SELECT			DESTINATION SELECT			
		S0	S1	S2	D0	D1	D2	D3
1011	N13	↑ READ RAM ↓	RD DP1 DATA		↑ WRITE RAM ↓	WT DP1 DATA	↑ LOAD ADDRESS REGISTER ↓	↑ LOAD ADDRESS REGISTER (LOW 8 BITS) ↓
1100	N14		RD DP2 UART STATUS	RD DP2 EIA STATUS		WT DP2 STATUS		
1101	N15		RD DP2 DATA			WT DP2 DATA		
1110	N16		RD DP3 UART STATUS	RD DP3 EIA STATUS		WT DP3 STATUS		
1111	N17		RD DP3 DATA			WT DP3 DATA		

TABLE H

DTU DISCRETE TEST FUNCTIONS

TEST FUNCTIONS*	DISCRETE STEPS	HI/LO	PROG SELECT-DATA	SWITCH								
Read Control Register	<ol style="list-style-type: none"> 1. Read contents of control register to the auxiliary register display. 2. Interpret auxiliary display results (must do octal conversion). <p>BITS 7 6 5 4 3 2 1 0</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td><td></td><td></td><td></td><td>SW 4</td><td>SW 3</td><td>SW 2</td><td>SW 1</td> </tr> </table>					SW 4	SW 3	SW 2	SW 1		6-100	XEQ/CONT XEQ
				SW 4	SW 3	SW 2	SW 1					
Write Control Register	<ol style="list-style-type: none"> 1. Write data to data register (must do octal conversion to determine nnn setting). <p>BITS 7 6 5 4 3 2 1 0</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td><td></td><td></td><td></td><td>LED 4</td><td>LED 3</td><td>LED 2</td><td>LED 1</td> </tr> </table>					LED 4	LED 3	LED 2	LED 1	LO HI	3- <i>nnn</i> 3-000	XEQ XEQ
				LED 4	LED 3	LED 2	LED 1					
Write Trouble Indicating Register	<ol style="list-style-type: none"> 1. Write data to data register (must do octal conversion to determine nnn setting). <p>BITS 7 6 5 4 3 2 1 0</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td><td></td><td>CONT</td><td>TBLB</td><td>TBLA</td><td>I/O</td><td>MEM</td><td>S/D</td> </tr> </table>			CONT	TBLB	TBLA	I/O	MEM	S/D	LO HI	5-100 3- <i>nnn</i> 3-000	XEQ/CONT XEQ XEQ XEQ
		CONT	TBLB	TBLA	I/O	MEM	S/D					
Read Trouble Indicating Register	<ol style="list-style-type: none"> 2. Write data in data register to the trouble indicating register. 1. Read contents of trouble indicating register to the auxiliary display. 2. Interpret auxiliary display results (must do octal conversion). <p>BITS 7 6 5 4 3 2 1 0</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td><td></td><td>CONT</td><td>TBLB</td><td>TBLA</td><td>I/O</td><td>MEM</td><td>S/D</td> </tr> </table>			CONT	TBLB	TBLA	I/O	MEM	S/D		5-101 6-101	XEQ/CONT XEQ XEQ/CONT XEQ
		CONT	TBLB	TBLA	I/O	MEM	S/D					
Write Real-Time Clock	<ol style="list-style-type: none"> 1. Write data to data register (both high and low 8 bits). 2. Write data in data register to the real-time clock. 	LO HI	3- <i>nnn</i> 3- <i>nnn</i> 5-102	XEQ XEQ XEQ/CONT XEQ								

TABLE H (Contd)

DTU DISCRETE TEST FUNCTIONS

TEST FUNCTIONS*	DISCRETE STEPS	HI/LO	PROG SELECT-DATA	SWITCH
Read Real-Time Clock	<ol style="list-style-type: none"> 1. Read real-time clock to the auxiliary register display. 2. Auxiliary display should display clock information. 		6-102	XEQ/CONT XEQ
Write Address Register	Write data to the address register. The data switches contain the address (also see Routine Exercise 2-nnn).		6-102	XEQ/CONT XEQ
Read Address Register	Read contents of address register to the auxiliary register (also see Routing Exercise 2-nnn).			
Write RAM Word	1. Write data word to be stored in RAM into data register.		3-nnn	XEQ
	2. Write high order 8 bits of the RAM word address into the address register.	HI	2-nnn	XEQ
	3. Write data from data register into RAM. The low order 8 bits of the RAM word address is set on the data switches.		4-nnn	XEQ/CONT XEQ
Read RAM Word	1. Write high order 8 bits of the RAM word address into the address register.	HI	2-nnn	XEQ
	<ol style="list-style-type: none"> 2. Read the RAM word into the auxiliary display. The low order 8 bits of the word address is set on the data switches. <p><i>Example:</i> The RAM word addresses are in octal. Read contents of RAM word 1762 into the auxiliary register display.</p> $1762 = \underbrace{011}_{\text{High order address}} \underbrace{11110010}_{\text{Low order address}}$ <p style="margin-left: 100px;"> $\underbrace{\quad\quad\quad 3 \quad 6 \quad 2 \quad\quad\quad}$ Low order address </p> <p style="margin-left: 100px;">3</p>		1-nnn	XEQ

TABLE H (Contd)

DTU DISCRETE TEST FUNCTIONS

TEST FUNCTIONS*	DISCRETE STEPS	HI/LO	PROG SELECT-DATA	SWITCH																																			
Write Distribute Word	1. Load high 8 bits into address register.	HI	2-003	XEQ																																			
	2. Read RAM to auxiliary display.		1-362	XEQ																																			
	1. Load address register with distributor row (word) to be written.	HI LO	2-000 2-00n	XEQ XEQ																																			
	<p>BITS 7 6 5 4 3 2 1 0</p> <table border="1"> <tr> <td>ROW 3</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>ROW 2</td> <td></td> <td></td> <td>STR</td> <td>STRA</td> <td>ARLK</td> <td>CMN</td> <td>CMJ</td> <td>MB</td> </tr> <tr> <td>ROW 1</td> <td></td> <td></td> <td>TRC</td> <td>S5</td> <td>S6</td> <td>S7</td> <td>S8</td> <td></td> </tr> <tr> <td>ROW 0</td> <td></td> <td></td> <td></td> <td>S0</td> <td>S1</td> <td>S2</td> <td>S3</td> <td>S4</td> </tr> </table>				ROW 3									ROW 2			STR	STRA	ARLK	CMN	CMJ	MB	ROW 1			TRC	S5	S6	S7	S8		ROW 0				S0	S1	S2	S3
ROW 3																																							
ROW 2			STR	STRA	ARLK	CMN	CMJ	MB																															
ROW 1			TRC	S5	S6	S7	S8																																
ROW 0				S0	S1	S2	S3	S4																															
	<p><i>Note:</i> This table is only used for No. 5 Crossbar MDT SD-28111-01. Consult appropriate SDs for other applications.</p> <p>2. Load data register with bits corresponding to distribute points to be set or operated.</p> <p><i>Example:</i> To set CMJ and ARLK, the data would be 012 and the address would be 002.</p> <p>3. Write data to distribute points with a DTOP instruction.</p> <p><i>Note:</i> To reset points the data word must contain zero for that bit.</p>		3-nnn 5-104	XEQ XEQ/CONT XEQ																																			
Read Scan Word	1. Load address register with scan row which is to be read.	HI LO	2-000 2-nnn	XEQ XEQ																																			

TABLE H (Contd)

DTU DISCRETE TEST FUNCTIONS

TEST FUNCTIONS*	DISCRETE STEPS					HI/LO		PROG SELECT-DATA		SWITCH	
	9	8	7	6	5	4	3	2	1	0	
BITS											
ROW 17			116	117	118	119					
ROW 16			108	109	110	111	112	113	114	115	
ROW 15			100	101	102	103	104	105	106	107	
ROW 14			92	93	94	95	96	97	98	99	
ROW 13			86	87	88	89	BWX 2	BWX 3	90	91	
ROW 12			78	79	80	81	82	83	84	85	
ROW 11			70	71	72	73	74	75	76	77	
ROW 10			62	63	64	65	66	67	68	69	
ROW 7			54	55	56	57	58	59	60	61	
ROW 6			46	47	48	49	50	51	52	53	
ROW 5			38	39	40	41	42	43	44	45	
ROW 4			30	31	32	33	34	35	36	37	
ROW 3			24	25	26	27	28	29	BWX 0	BWX 1	
ROW 2	MB	ROS	16	17	18	19	20	21	22	23	
ROW 1	SPL	TRC	08	09	10	11	12	13	14	15	
ROW 0	STR	STRAI 1	BW 00	01	02	03	04	05	06	07	

Note: This table is only used for No. 5 Crossbar MDT SD-28111-01. Consult appropriate SDs for other applications.

TABLE H (Contd)

DTU DISCRETE TEST FUNCTIONS

TEST FUNCTIONS*	DISCRETE STEPS	HI/LO	PROG SELECT-DATA	SWITCH
	2. Read the scan word into the auxiliary with a PTOD instruction. 3. Interpret display to determine which scan points are grounded. <i>Example:</i> Determine if BW95 scan point is grounded. 1. Load row number into address register. 2. Read word into display. 3. Interpret results — assume auxiliary display = 142. The display 142 indicates BW98, BW94, and BW93 have grounds at row 14.		6-103 2-014 6-103	XEQ/CONT XEQ XEQ XEQ

* Before performing each test function, insure that CONT XEQ switch is OFF.