EADAS TRAFFIC DATA CONVERTER (ETDC) SD-3B213-01
CONNECTION VERIFICATION TESTS
USING ETDC INPUT PULSER SD-3B221-01
ENGINEERING AND ADMINISTRATIVE DATA ACQUISITION SYSTEM (EADAS)

1. GENERAL

1.01 This section describes a method of performing connection verification tests of the input leads to the EADAS traffic data converter (ETDC) SD-3B213-01.

1.02 This section is reissued to include information on the high-resolution 10-second usage card and to generally update this section. Revision arrows are used to emphasize the more significant changes. Equipment Test Lists are not affected.

1.03 The tests covered are:

1.04 Tests A, B, and C must be coordinated with traffic personnel at the EADAS central unit and should be performed during periods of light traffic.

1.05 Tests A and B require the aid of an assistant.

1.06 The Local Frame Line Circuit, SD-96379-01, or Switchmans Talking Line Circuit, SD-32021-01 (step-by-step offices), is used when performing tests that are outlined in Tests A and B. One head telephone set is connected to the talking line circuit at the equipment location associated with the particular ETDC input lead(s) to be tested. At the ETDC, another headset is also connected to the talking line circuit.

1.07 Local instructions should be followed for recording and reporting any traffic register operations caused by performing this test.

Caution: Before the tests in this section are performed, it is important that consideration be given to the data which is blocked while the ETDC inputs are being tested. The data for the entire 30-minute data collection interval at the EADAS central unit is considered lost because of the interruption of normal data.

1.08 Refer to Section 190-510-212 for method of performing local tests of the EADAS TDC at the ETDC location.

1.09 Refer to Section 190-510-211 for method of performing remote tests of the EADAS TDC at the EADAS central unit.

1.10 The ETDC is arranged to accommodate 32 input cards, each of which has 32 input leads giving a maximum capacity of 1024 inputs. Input card No. 31 is dedicated to handle discrete events; therefore, only 989 (addresses 0 and 1 reserved for buffer overflow and parity errors and an additional input reserved for ETDC cycle count) inputs can be used for data collection and calculations. Table A shows the input cards (circuit packs) which are associated with the ETDC input leads.

1.11 There are basically ▶six◀ different types of input cards:

(1) ***Peg Count Card***—Causes a unique binary data word (address) to be generated once and only once for each time one input lead receives a peg count indication.

(2) ***Scaled Peg Count Card***—Causes a unique address to be generated once for each time one input lead receives 10 peg count indications.

(3) ***Usage Card***—Causes a unique address to be generated for each time one input lead is scanned (100 seconds) and found busy.

(4) ***Discrete Card***—Causes a unique address to be generated for each time one input lead is scanned (approximately 10 seconds) and found busy.

(5) ***Multiscan Usage Card***—Causes a unique address to be generated for each time one input lead is scanned (1.8 seconds) and found busy. (Option YF permits an input lead to be scanned every 1.0 second and option YG permits an input lead to be scanned every 3.6 seconds.)

(6) ▶***High Resolution 10-Second Usage Card***—Provides highly accurate sampling for short holding time circuits on an individual basis. This card contains circuitry for scanning at a 20 ms rate for 32 inputs. When an individual input reaches a total of 500 in storage (equivalent to 10 seconds), an output is provided to the ETDC encoder.◀

1.12 The input leads to the ETDC directly correspond to a register number and are listed in Table B. Associated with each input lead number is the ETDC terminal location and a corresponding 10-bit word which is unique to the associated input. The leftmost five bits represent the input card number (block) and the rightmost five bits represent one of 32 input leads.

1.13 The EADAS input pulser generates 10 pulses on the input lead to be verified. Ten pulses are received at the ETDC and displayed on the LED readouts on the ETDC input verification test set.

Caution: Before connecting the input pulser to the lead to be verified, check to make sure the VT switch on ETDC is in TST position for off-line testing (Test A).

1.14 When an input to the ETDC is being verified, the SEL/CONT switch on the input pulser should be set to SEL, SEL/10X switch to 10X, and the CLR/START switch is momentarily operated to CLR and then placed in the START position. This pulses the input lead ten times. For each time the input lead is pulsed (nonscaled inputs), an indication is received at the ETDC and converted into an address which is unique to the associated input. The binary word address is then displayed on the ETDC input verification test set. For each time the START switch is operated at the input pulser, ten addresses are generated and received at the ETDC input verification test set. The first address transmitted appears on the FIRST WORD lamps and the last address transmitted appears on the LATEST WORD lamps. The FIRST WORD and LATEST WORD lamps corresponding to addresses with a ***one*** are lighted. The NO. WORDS counter registers 10 counts for each time the START switch is operated (nonscaled inputs). For scaled inputs, the NO. WORDS counter registers one count for each time the START switch is operated. The NO. WORDS counter registers the number of words encoded by the ETDC, while the NO. MATCHES counter registers the number of words encoded that match the address set on the REGISTER thumbwheel switches.

1.15 Normal office traffic can cause counts on the lead under test to be lost in the test mode. If input being verified fails, the test should be completed.

2. APPARATUS

2.01 EADAS input pulser, SD-3B221-01, equipped with testing cords.

2.02 52-type head telephone set, two required.

2.03 ETDC input verification test set, SD-3B236-01.

3. PREPARATION

STEP	ACTION	VERIFICATION
All Tests		
1	Connect the ETDC input verification test set to the TST connector.	
2	Connect the ETDC input verification test set power cord to the -48V supply.	
3	At ETDC input verification test set— Operate PWR switch to ON.	
4	Consult office records to obtain input card assignments of ETDC.	
5	Verify that ETDC is properly equipped with input cards.	
Tests A and B		
6	At ETDC— Connect headset to TEL or SP jack of frame line talk circuit. ***Note:*** It may be necessary to operate frame line key(s) to connect one floor to another floor.	
7	Consult office records to obtain equipment location associated with input lead(s) to be verified.	
8	At equipment location associated with input lead(s) to be verified— Connect headset to TEL or SP jack of frame line talk circuit (see Note after Step 6).	
9	Connect input pulser test set GRD jack to frame ground.	
10	At input pulser test set— Connect power cord to 115-volt ac power outlet (see paragraph 1.13).	READY lamp lighted. ***Note:*** If READY lamp is not lighted, it is probably because test set is not in horizontal position.

STEP	ACTION	VERIFICATION
11	Set SEL/CONT switch to SEL.	
12	Set SEL/10X switch to 10X.	
13	At ETDC input verification test set— Set NORMAL/EXTENDED switch on input verification test card to NORMAL.	

4. METHOD

STEP	ACTION	VERIFICATION
A. Off-Line Connection Verification		
14	At ETDC— Operate VT switch to TST.	Lamp on CP 11 (AR643) lighted.
15	At ETDC input verification test set— Set REGISTER NUMBER thumbwheel switches to correspond with input lead number to be verified.	
16	Momentarily operate BIN RESET pushbutton.	FIRST WORD and LATEST WORD lamps extinguished.
17	Operate CLEAR/RUN switch to CLEAR and then to RUN.	NO. WORDS and NO. MATCHES counters extinguished.
18	At equipment location associated with input lead(s) being verified— Connect PULSE jack of input pulser test set to terminal associated with input lead to be verified.	
19	At input pulser test set— Operate +18/GRD switch to +18.	
Nonscaled Inputs		
20	Operate CLR/START switch to CLR.	
21	Operate CLR/START switch to START. ***Note:*** If the NO. WORDS counter indicates 10 but the NO. MATCHES counter indicates 0, the lead being verified is connected to the wrong input terminal. The address displayed on the FIRST WORD and LATEST WORD lamps is the ETDC input terminal to which the lead is actually connected. If both counters indicate 0, the lead is not connected to an equipped input. If the NO. MATCHES counter	At ETDC input verification test set— Input verification test card FIRST WORD and LATEST word lamps indicate address corresponding with input lead being tested (see paragraph 1.14 and Table B). NO. WORDS and NO. MATCHES counters each indicate approximately 10. ***Note:*** If the addresses on the input verification test card FIRST WORD and LATEST WORD are different, or if NO. MATCHES counter

STEP	ACTION	VERIFICATION
	indicates 10, but the NO. WORDS counter indicates more than 10, there is a cross between two or more inputs. Each additional 10 counts on the NO. WORDS counter indicates one more crossed input. The addresses which are displayed on the FIRST WORD and LATEST WORD lamps correspond to two of the crossed inputs. Refer to Table B to determine which input leads are crossed.	indicates more than 10, there is a cross between two or more inputs. The addresses which are displayed on the FIRST WORD and LATEST WORD lamps correspond to two of the crossed inputs. Compare these addresses with the correct input and, if necessary, repeat Steps 20 and 21 until correct input is displayed. Refer to Table B to determine which input leads are crossed.
22	Remove cord connection from terminal associated with input verified.	
23	Repeat Steps 15 through 21 for other nonscaled input leads to be verified.	
	Scaled Inputs	
24	Repeat Steps 14 through 19 for scaled inputs to be verified.	
25	At input pulser test set— Operate CLR/START switch to CLR.	
26	Operate CLR/START switch to START. ***Note:*** If the NO. WORDS counter indicates 1 but the NO. MATCHES counter indicates 0, the lead being verified is connected to the wrong input terminal. The address displayed on the FIRST WORD lamps is the ETDC input terminal to which the lead is actually connected. If both counters indicate 0, the lead is not connected to an equipped input. If the NO. MATCHES counter indicates 1, but the NO. WORDS counter indicates more than 1, there is a cross between two or more inputs. Each additional count on the NO. WORDS counter indicates one more crossed scaled input. Ten or more counts on the NO. WORDS counter indicates a cross to a nonscaled input. The addresses displayed on the FIRST WORD and LATEST WORD lamps correspond to two of the crossed inputs. Refer to Table B to determine which input leads are crossed.	At ETDC input verification test set— Input verification test card FIRST WORD lamp indicates address corresponding to input lead being verified. NO. WORDS and NO. MATCHES counters indicate 1.
27	At input pulser test set— Remove cord connection from input lead being verified.	
28	At ETDC input verification test set— Momentarily depress BIN RESET pushbutton.	Input verification test card FIRST WORD and LATEST WORD lamps extinguished.

STEP	ACTION	VERIFICATION
29	Operate CLEAR/RUN switch to CLEAR and then to RUN.	NO. WORDS and NO. MATCHES counters extinguished.
30	At equipment location associated with next scaled input lead to be verified— Connect test cord to input pulser PULSE jack and to input lead to be verified.	
31	Repeat Steps 24 through 30 for other scaled inputs to be verified.	
	Nonscaled and Scaled Inputs	
32	At input pulser test set— Remove all cords.	
33	At ETDC— Restore VT switch to normal.	Lamp on CP 11 (AR643) extinguished.
34	At ETDC input verification test set— Operate PWR switch to OFF.	
35	Remove power cord from -48V supply.	
36	Remove ETDC input verification test set from the TST connector.	
	B. On-Line Connection Verification From Associated Equipment	
	Note: This test should only be performed when verification of a small number of inputs is required.	
14	At ETDC input verification test set— Set REGISTER NUMBER thumbwheel switches of input verification test card to agree with input lead number to be verified.	
15	Operate CLEAR/RUN switch to CLEAR and then to RUN.	NO. MATCHES lamp extinguished. ***Note:*** A small number of matches may occur due to normal office data.
16	At input pulser test set— Operate CLR/START switch to CLR.	
17	Operate +18/GRD switch to GRD.	
18	Connect PULSE jack of input pulser test set to input lead to be verified.	

STEP	ACTION	VERIFICATION
	Nonscaled Inputs	
19	At input pulser test set— Operate CLR/START switch to START.	At ETDC input verification test set— Input verification test card NO. MATCHES counter indicates approximately 10. ***Note:*** Ignore all other lamps.
20	Repeat Steps 14 through 19 for other nonscaled input leads to be verified.	
	Scaled Inputs	
21	At input pulser test set— Operate CLR/START switch to CLR and then to START.	At ETDC input verification test set— Input verification test card NO. MATCHES counter indicates 1. ***Note 1:*** Due to normal traffic conditions it may be necessary to repeat Step 21 several times to receive verification. ***Note 2:*** Ignore all other lamps.
22	Repeat Steps 14 through 18 and Step 21 for other scaled inputs to be tested.	
	Nonscaled and Scaled Inputs	
23	At input pulser test set— Remove all cords.	
24	At ETDC— Operate CLEAR/RUN switch to CLEAR.	NO. WORDS and NO. MATCHES counters extinguished.
25	At ETDC input verification test set— Operate PWR switch to OFF.	
26	Remove power cord from -48V supply.	
27	Remove ETDC input verification test set from the TST connector.	
	C. On-Line Verification of ETDC Operation From ETDC	
6	At ETDC— Connect GRD jack of input pulser test set to frame ground.	

STEP	ACTION	VERIFICATION
7	At input pulser test set— Connect power cord to 115-volt ac power outlet.	READY lamp lighted. ***Note:*** Input pulser test set must be in horizontal position (switches upward); otherwise READY lamp may not light.
8	Set SEL/CONT switch to SEL.	
9	Set SEL/10X switch to 10X.	
10	Set +18/GRD switch to GRD.	
11	At ETDC input verification test set— Set NORMAL/EXTENDED switch to NORMAL.	
12	Set REGISTER NUMBER thumbwheel switches to correspond with input lead to be verified.	
13	Refer to Table B to obtain INNET terminal number corresponding to input lead to be verified.	
14	Connect input pulser PULSE jack to input terminal obtained in Step 13.	
15	At ETDC input verification test set— Momentarily depress BIN RESET pushbutton.	At ETDC input verification test set— Input verification test card FIRST WORD and LATEST WORD lamps extinguished.
16	Operate CLEAR/RUN switch to CLEAR and then to RUN.	NO. WORDS and NO. MATCHES counters extinguished.
	Nonscaled Inputs	
17	At input pulser test set— Operate CLR/START switch to CLR.	
18	Operate CLR/START switch to START.	At ETDC input verification test set— Input verification test card NO. MATCHES counter indicates approximately 10.
19	Remove cord connection from input terminal.	
20	Repeat Steps 12 through 18 for other nonscaled inputs to be verified.	
	Scaled Inputs	
21	At input pulser test set— Operate CLR/START switch to CLR.	

STEP	ACTION	VERIFICATION
22	Operate CLR/START switch to START.	At ETDC input verification test set— Input verification test card NO. MATCHES counter indicates 1. ***Note 1:*** Ignore all other lamps. ***Note 2:*** Due to normal traffic conditions, it may be necessary to repeat Steps 21 and 22 several times to receive verification.
23	Remove cord connection from input terminal.	
24	Repeat Steps 12 through 16 and 21 and 22 for other scaled inputs to be tested.	
	Nonscaled and Scaled Inputs	
25	At input pulser test set— Remove all cords.	
26	At ETDC input verification test set— Operate PWR switch to OFF.	
27	Remove power cord from -48V supply.	
28	Remove ETDC input verification test set from the TST connector.	

TABLE A

INPUT NO.'S	INPUT CARD NO.	INPUT NO.'S	INPUT CARD NO.
0-31	0	512-543	16
32-63	1	544-575	17
64-95	2	576-607	18
96-127	3	608-639	19
128-159	4	640-671	20
160-191	5	672-703	21
192-223	6	704-735	22
224-255	7	736-767	23
256-287	8	768-799	24
288-319	9	800-831	25
320-351	10	832-863	26
352-383	11	864-895	27
384-415	12	896-927	28
416-447	13	928-959	29
448-479	14	960-991	30
480-511	15	992-1023	31

TABLE B

Note: The INNET TERM columns of these tables are used for J options only. With G option the INNET TERM is the same as the REGISTER NO. See Fig. 1 for INNET terminal arrangement with G option.

REGISTER NO.	INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
0	0	000	Not used	
1		010	Not used	
2		020	000000	00010
3		030	00000	00011
4		040	00000	00100
5		050	00000	00101
6		060	00000	00110
7		070	00000	00111
8		080	00000	01000
9		090	00000	01001
10		100	00000	01010
11		110	00000	01011
12		120	00000	01100
13		130	00000	01101
14		140	00000	01110
15		150	00000	01111
16		001	00000	10000
17		011	00000	10001
18		021	00000	10010
19		031	00000	10011
20		041	00000	10100
21		051	00000	10101
22		061	00000	10110
23		071	00000	10111
24		081	00000	11000
25		081	00000	11000
26		101	00000	11010
27		111	00000	11011
28		121	00000	11100
29		131	00000	11101
30		141	00000	11110

REGISTER NO.	INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
31	0	151	00000	11111
32		002	00001	00000
33		012	00001	00001
34		022	00001	00010
35		032	00001	00011
36		042	00001	00100
37		052	00001	00101
38		062	00001	00110
39		072	00001	00111
40		082	00001	01000
41		092	00001	01001
42		102	00001	01010
43		112	00001	01011
44		122	00001	01100
45		132	00001	01101
46		142	00001	01110
47		152	00001	01111
48		003	00001	10000
49		013	00001	10001
50		023	00001	10010
51		033	00001	10011
52		043	00001	10100
53		053	00001	10101
54		063	00001	10110
55		073	00001	10111
56		083	00001	11000
57		093	00001	11001
58		103	00001	11010
59		113	00001	11011
60		123	00001	11100
61		133	00001	11101

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
62	0	126	00001	11110
63		153	00001	11111
64		005	00010	00000
65		015	00010	00001
66		025	00010	00010
67		035	00010	00011
68		045	00010	00100
69		055	00010	00101
70		065	00010	00110
71		075	00010	00111
72		085	00010	01000
73		095	00010	01001
74		105	00010	01010
75		115	00010	01011
76		125	00010	01100
77		135	00010	01101
78		145	00010	01110
79		155	00010	01111
80		006	00010	10000
81		016	00010	10001
82		026	00010	10010
83		036	00010	10011
84		046	00010	10100
85		056	00010	10101
86		066	00010	10110
87		076	00010	10111
88		086	00010	11000
89		096	00010	11001
90		106	00010	11010
91		116	00010	11011
92		126	00010	11100
93		136	00010	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
94	0	146	00010	11110
95		156	00010	11111
96		007	00011	00000
97		017	00011	00001
98		027	00011	00010
99		037	00011	00011
100		047	00011	00100
101		057	00011	00101
102		067	00011	00110
103		077	00011	00111
104		087	00011	01000
105		097	00011	01001
106		107	00011	01010
107		117	00011	01011
108		127	00011	01100
109		137	00011	01101
110		147	00011	01110
111		157	00011	01111
112	1	000	00011	10000
113		010	00011	10001
114		020	00011	10010
115		030	00011	10011
116		040	00011	10100
117		050	00011	10101
118		060	00011	10110
119		070	00011	10111
120		080	00011	11000
121		090	00011	11001
122		100	00011	11010
123		110	00011	11011
124		120	00011	11100
125		130	00011	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
126	1	140	00011	11110
127		150	00011	11111
128		001	00100	00000
129		011	00100	00001
130		021	00100	00010
131		031	00100	00011
132		041	00100	00100
133		051	00100	00101
134		061	00100	00110
135		071	00100	00111
136		081	00100	01000
137		091	00100	01001
138		101	00100	01010
139		111	00100	01011
140		121	00100	01100
141		131	00100	01101
142		141	00100	01110
143		151	00100	01111
144		002	00100	10000
145		012	00100	10001
146		022	00100	10010
147		032	00100	10011
148		042	00100	10100
149		052	00100	10101
150		062	00100	10110
151		072	00100	10111
152		082	00100	11000
153		092	00100	11001
154		102	00100	11010
155		112	00100	11011
156		122	00100	11100
157		132	00100	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
158	1	142	00100	11110
159		152	00100	11111
160		003	00101	00000
161		013	00101	00001
162		023	00101	00010
163		033	00101	00011
164		043	00101	00100
165		053	00101	00101
166		063	00101	00110
167		073	00101	00111
168		083	00101	01000
169		093	00101	01001
170		103	00101	01010
171		113	00101	01011
172		123	00101	01100
173		133	00101	01101
174		143	00101	01110
175		153	00101	01111
176		005	00101	10000
177		015	00101	10001
178		025	00101	10010
179		035	00101	10011
180		045	00101	10100
181		055	00101	10101
182		065	00101	10110
183		075	00101	10111
184		085	00101	11000
185		095	00101	11001
186		105	00101	11010
187		115	00101	11011
188		125	00101	11100
189		135	00101	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
190	1	145	00101	11110
191		155	00101	11111
192		006	00110	00000
193		016	00110	00001
194		026	00110	00010
195		036	00110	00011
196		046	00110	00100
197		056	00110	00101
198		066	00110	00110
199		076	00110	00111
200		086	00110	01000
201		096	00110	01001
202		106	00110	01010
203		116	00110	01011
204		126	00110	01100
205		136	00110	01101
206		146	00110	01110
207		156	00110	01111
208		007	00110	10000
209		017	00110	10001
210		027	00110	10010
211		037	00110	10011
212		047	00110	10100
213		057	00110	10101
214		067	00110	10110
215		077	00110	10111
216		087	00110	11000
217		097	00110	11001
218		107	00110	11010
219		117	00110	11011
220		127	00110	11100
221		137	00110	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
222	1	147	00110	11110
223		157	00110	11111
224	2	000	00111	00000
225		010	00111	00001
226		020	00111	00010
227		030	00111	00011
228		040	00111	00100
229		050	00111	00101
230		060	00111	00110
231		070	00111	00111
232		080	00111	01000
233		090	00111	01001
234		100	00111	01010
235		110	00111	01011
236		120	00111	01100
237		130	00111	01101
238		140	00111	01110
239		150	00111	01111
240		001	00111	10000
241		011	00111	10001
242		021	00111	10010
243		031	00111	10011
244		041	00111	10100
245		051	00111	10101
246		061	00111	10110
247		071	00111	10111
248		081	00111	11000
249		091	00111	11001
250		101	00111	11010
251		111	00111	11011
252		121	00111	11100
253		131	00111	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
254	2	141	00111	11110
255		151	00111	11111
256		022	01000	00000
257		012	01000	00001
258		022	01000	00010
259		032	01000	00011
260		042	01000	00100
261		052	01000	00101
262		062	01000	00110
263		072	01000	00111
264		082	01000	01000
265		092	01000	01001
266		102	01000	01010
267		112	01000	01011
268		122	01000	01100
269		132	01000	01101
270		142	01000	01110
271		152	01000	01111
272		003	01000	10000
273		013	01000	10001
274		023	01000	10010
275		033	01000	10011
276		043	01000	10100
277		053	01000	10101
278		063	01000	10110
279		073	01000	10111
280		083	01000	11000
281		093	01000	11001
282		103	01000	11010
283		113	01000	11011
284		123	01000	11100
285		133	01000	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
286	2	143	01000	11110
287		153	01000	11111
288		005	01001	00000
289		015	01001	00001
290		015	01001	00010
291		035	01001	00011
292		045	01001	00100
293		055	01001	00101
294		065	01001	00110
295		075	01001	00111
296		085	01001	01000
297		095	01001	01001
298		105	01001	01010
299		115	01001	01011
300		125	01001	01100
301		135	01001	01101
302		145	01001	01110
303		155	01001	01111
304		006	01001	10000
305		016	01001	10001
306		026	01001	10010
307		036	01001	10011
308		046	01001	10100
309		056	01001	10101
310		066	01001	10110
311		076	01001	10111
312		086	01001	11000
313		096	01001	11001
314		096	01001	11010
315		116	01001	11011
316		126	01001	11100
317		136	01001	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
318	2	146	01001	11110
319		156	01001	11111
320		007	01010	00000
321		017	01010	00001
322		027	01010	00010
323		037	01010	00011
324		047	01010	00100
325		057	01010	00101
326		067	01010	00110
327		077	01010	00111
328		087	01010	01000
329		097	01010	01001
330		107	01010	01010
331		117	01010	01011
332		127	01010	01100
333		137	01010	01101
334		147	01010	01110
335		157	01010	01111
336	3	000	01010	10000
337		010	01010	10001
338		020	01010	10010
339		030	01010	10011
340		040	01010	10100
341		050	01010	10101
342		060	01010	10110
343		070	01010	10111
344		080	01010	11000
345		090	01010	11001
346		100	01010	11010
347		110	01010	11011
348		120	01010	11100
349		130	01010	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
350	3	140	01010	11110
351		150	01010	11111
352		001	01011	00000
353		011	01011	00001
354		021	01011	00010
355		031	01011	00011
356		041	01011	00100
357		051	01011	00101
358		061	01011	00110
359		071	01011	00111
360		081	01011	01000
361		091	01011	01001
362		101	01011	01010
363		111	01011	01011
364		121	01011	01100
365		131	01011	01101
366		141	01011	01110
367		151	01011	01111
368		002	01011	10000
369		012	01011	10001
370		022	01011	10010
371		032	01011	10011
372		042	01011	10100
373		052	01011	10101
374		062	01011	10110
375		072	01011	10111
376		082	01011	11000
377		092	01011	11001
378		102	01011	11010
379		112	01011	11011
380		122	01011	11100
381		132	01011	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
382		142	01011	11110	414		145	01100	11110
383		152	01011	11111	415		155	01100	11111
384		003	01100	00000	416		006	01101	00000
385		013	01100	00001	417		016	01101	00001
386		023	01100	00010	418		026	01101	00010
387		033	01100	00011	419		036	01101	00011
388		043	01100	00100	420		046	01101	00100
389		053	01100	00101	421		056	01101	00101
390		063	01100	00110	422		066	01101	00110
391		073	01100	00111	423		076	01101	00111
392		083	01100	01000	424		086	01101	01000
393		093	01100	01001	425		096	01101	01001
394		103	01100	01010	426		106	01101	01010
395	3	113	01100	01011	427	3	116	01101	01011
396		123	01100	01100	428		126	01101	01100
397		133	01100	01101	429		136	01101	01101
398		143	01100	01110	430		146	01101	01110
399		153	01100	01111	431		156	01101	01111
400		005	01100	10000	432		007	01101	10000
401		015	01100	10001	433		017	01101	10001
402		025	01100	10010	434		027	01101	10010
403		035	01100	10011	435		037	01101	10011
404		045	01100	10100	436		047	01101	10100
405		055	01100	10101	437		057	01101	10101
406		065	01100	10110	438		067	01101	10110
407		075	01100	10111	439		077	01101	10111
408		085	01100	11000	440		087	01101	11000
409		095	01100	11001	441		097	01101	11001
410		105	01100	11010	442		107	01101	11010
411		115	01100	11011	443		117	01101	11011
412		125	01100	11100	444		127	01101	11100
413		135	01100	11101	445		137	01101	11101

* See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
446	3	147	01100	11110	478	4	141	01110	11110
447		157	01101	11111	479		151	01110	11111
448	4	000	01110	00000	480		002	01111	00000
449		010	01110	00001	481		012	01111	00001
450		020	01110	00010	482		022	01111	00010
451		030	01110	00011	483		032	01111	00011
452		040	01110	00100	484		042	01111	00100
453		050	01110	00101	485		052	01111	00101
454		060	01110	00110	486		062	01111	00110
455		070	01110	00111	487		072	01111	00111
456		080	01110	01000	488		082	01111	01000
457		090	01110	01001	489		092	01111	01001
458		100	01110	01010	490		102	01111	01010
459		110	01110	01011	491		112	01111	01011
460		120	01110	01100	492		122	01111	01100
461		130	01110	01101	493		132	01111	01101
462		140	01110	01110	494		142	01111	01110
463		150	01110	01111	495		152	01111	01111
464		001	01110	10000	496		003	01111	10000
465		011	01110	10001	497		013	01111	10001
466		021	01110	10010	498		023	01111	10010
467		031	01110	10011	499		033	01111	10011
468		041	01110	10100	500		043	01111	10100
469		051	01110	10101	501		053	01111	10101
470		061	01110	10110	502		063	01111	10110
471		071	01110	10111	503		073	01111	10111
472		081	01110	11000	504		083	01111	11000
473		091	01110	11001	505		093	01111	11001
474		010	01110	11010	506		103	01111	11010
475		111	01110	11011	507		113	01111	11011
476		121	01110	11100	508		123	01111	11100
477		131	01110	11101	509		133	01111	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
510	4	143	01111	11110
511		153	01111	11111
512		005	10000	00000
513		015	10000	00001
514		025	10000	00010
515		035	10000	00011
516		045	10000	00100
517		055	10000	00101
518		065	10000	00110
519		075	10000	00111
520		085	10000	01000
521		095	10000	01001
522		105	10000	01010
523		115	10000	01011
524		125	10000	01100
525		135	10000	01101
526		145	10000	01110
527		155	10000	01111
528		006	10000	10000
529		016	10000	10001
530		026	10000	10010
531		036	10000	10011
532		046	10000	10100
533		056	10000	10101
534		066	10000	10110
535		076	10000	10111
536		086	10000	11000
537		096	10000	11001
538		106	10000	11010
539		116	10000	11011
540		126	10000	11100
541		136	10000	11101
542	4	146	10000	11110
543		156	10000	11111
544		007	10001	00000
545		017	10001	00001
546		027	10001	00010
547		036	10001	00011
548		047	10001	00100
549		057	10001	00101
550		067	10001	00110
551		077	10001	00111
552		087	10001	01000
553		097	10001	01001
554		107	10001	01010
555		117	10001	01011
556		127	10001	01100
557		137	10001	01101
558		147	10001	01110
559		157	10001	01111
560	5	000	10001	10000
561		010	10001	10001
562		020	10001	10010
563		030	10001	10011
564		040	10001	10100
565		050	10001	10101
566		060	10001	10110
567		070	10001	10111
568		080	10001	11000
569		090	10001	11001
570		100	10001	11010
571		110	10001	11011
572		120	10001	11100
573		130	10001	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
574		140	10001	11110	606		142	10010	11110
575		150	10001	11111	607		152	10010	11111
576		001	10010	00000	608		003	10011	00000
577		011	10010	00001	609		013	10011	00001
578		021	10010	00010	610		023	10011	00010
579		031	10010	00011	611		033	10011	00011
580		041	10010	00100	612		043	10011	00100
581		051	10010	00101	613		053	10011	00101
582		061	10010	00110	614		063	10011	00110
583		071	10010	00111	615		073	10011	00111
584		081	10010	01000	616		083	10011	01000
585		091	10010	01001	617		093	10011	01001
586		101	10010	01010	618		103	10011	01010
587		111	10010	01011	619		113	10011	01011
588	5	121	10010	01100	620	5	123	10011	01100
589		131	10010	01101	621		133	10011	01101
590		141	10010	01110	622		143	10011	01110
591		151	10010	01111	623		153	10011	01111
592		002	10010	10000	624		005	10011	10000
593		012	10010	10001	625		015	10011	10001
594		022	10010	10010	626		025	10011	10010
595		032	10010	10011	627		035	10011	10011
596		042	10010	10100	628		045	10011	10100
597		052	10010	10101	629		055	10011	10101
598		062	10010	10110	630		065	10011	10110
599		072	10010	10111	631		075	10011	10111
600		082	10010	11000	632		085	10011	11000
601		092	10010	11001	633		095	10011	11001
602		102	10010	11010	634		105	10011	11010
603		112	10010	11011	635		115	10011	11011
604		122	10010	11100	636		125	10011	11100
605		132	10010	11101	637		135	10011	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
638		145	10011	11110	670	5	147	10100	11110
639		155	10011	11111	671		157	10100	11111
640		006	10100	00000	672		000	10101	00000
641		016	10100	00001	673		010	10101	00001
642		026	10100	00010	674		020	10101	00010
643		036	10100	00011	675		030	10101	00011
644		046	10100	00100	676		040	10101	00100
645		056	10100	00101	677		050	10101	00101
646		066	10100	00110	678		060	10101	00110
647		076	10100	00111	679		070	10101	00111
648		086	10100	01000	680		080	10101	01000
649		096	10100	01001	681		090	10101	01001
650		106	10100	01010	682		100	10101	01010
651	5	116	10100	01011	683		110	10101	01011
652		126	10100	01100	684		120	10101	01100
653		136	10100	01101	685		130	10101	01101
654		145	10100	01110	686	6	140	10101	01110
655		156	10100	01111	687		150	10101	01111
656		007	10100	10000	688		001	10101	10000
657		017	10100	10001	689		011	10101	10001
658		027	10100	10010	690		021	10101	10010
659		037	10100	10011	691		031	10101	10011
660		047	10100	10100	692		041	10101	10100
661		057	10100	10101	693		051	10101	10101
662		067	10100	10110	694		061	10101	10110
663		077	10100	10111	695		071	10101	10111
664		087	10100	11000	696		081	10101	11000
665		097	10100	11001	697		091	10101	11001
666		107	10100	11010	698		101	10101	11010
667		117	10100	11011	699		111	10101	11011
668		127	10100	11100	700		121	10101	11100
669		137	10100	11101	701		131	10101	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
702	6	141	10101	11110
703		151	10101	11111
704		002	10110	00000
705		012	10110	00001
706		022	10110	00010
707		032	10110	00011
708		042	10110	00100
709		052	10110	00101
710		062	10110	00110
711		072	10110	00111
712		082	10110	01000
713		092	10110	01001
714		102	10110	01010
715		112	10110	01011
716		122	10110	01100
717		132	10110	01101
718		142	10110	01110
719		152	10110	01111
720		003	10110	10000
721		013	10110	10001
722		023	10110	10010
723		033	10110	10011
724		043	10110	10100
725		053	10110	10101
726		063	10110	10110
727		073	10110	10111
728		033	10110	11000
729		093	10110	11001
730		103	10110	11010
731		113	10110	11011
732		123	10110	11100
733		133	10110	11101

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
734	6	143	10110	11110
735		153	10110	11111
736		005	10111	00000
737		015	10111	00001
738		075	10111	00010
739		035	10111	00011
740		045	10111	00100
741		055	10111	00101
742		065	10111	00110
743		075	10111	00111
744		085	10111	01000
745		095	10111	01001
746		105	10111	01010
747		115	10111	01011
748		125	10111	01100
749		135	10111	01101
750		145	10111	01110
751		155	10111	01111
752		006	10111	10000
753		016	10111	10001
754		026	10111	10010
755		036	10111	10011
756		046	10111	10100
757		056	10111	10101
758		066	10111	10110
759		076	10111	10111
760		086	10111	11000
761		096	10111	11001
762		106	10111	11010
763		116	10111	11011
764		126	10111	11100
765		136	10111	11101

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
766		146	10111	11110
767		156	10111	11111
768		007	11000	00000
769		017	11000	00001
770		027	11000	00010
771		037	11000	00011
772		047	11000	00100
773		057	11000	00101
774	6	067	11000	00110
775		077	11000	00111
776		087	11000	01000
777		097	11000	01001
778		107	11000	01010
779		117	11000	01011
780		127	11000	01100
781		137	11000	01101
782		147	11000	01110
783		157	11000	01111
784		000	11000	10000
785		010	11000	10001
786		020	11000	10010
787		030	11000	10011
788		040	11000	10100
789	7	050	11000	10101
790		060	11000	10110
791		070	11000	10111
792		080	11000	11000
793		090	11000	11001
794		100	11000	11010
795		110	11000	11011

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
796		120	11000	11100
797		130	11000	11101
798		140	11000	11110
799		150	11000	11111
800		001	11001	00000
801		011	11001	00001
802		021	11001	00010
803		031	11001	00011
804		041	11001	00100
805		051	11001	00101
806		061	11001	00110
807		071	11001	00111
808		081	11001	01000
809	7	091	11001	01001
810		101	11001	01010
811		111	11001	01011
812		121	11001	01100
813		131	11001	01101
814		141	11001	01110
815		151	11001	01111
816		002	11001	10000
817		012	11001	10001
818		022	11001	10010
819		032	11001	10011
820		042	11001	10100
821		052	11001	10101
822		062	11001	10110
823		072	11001	10111
824		082	11001	11000
825		092	11001	11001

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
826		102	11001	11010	858		105	11010	11010
827		112	11001	11011	859		115	11010	11011
828		122	11001	11100	860		125	11010	11100
829		132	11001	11101	861		135	11010	11101
830		142	11001	11110	862		145	11010	11110
831		152	11001	11111	863		155	11010	11111
832		003	11010	00000	864		006	11011	00000
833		013	11010	00001	865		016	11011	00001
834		023	11010	00010	866		026	11011	00010
835		033	11010	00011	867		036	11011	00011
836		043	11010	00100	868		046	11011	00100
837		053	11010	00101	869		056	11011	00101
838		063	11010	00110	870		066	11011	00110
839		073	11010	00111	871		076	11011	00111
840	7	083	11010	01000	872	7	086	11011	01000
841		093	11010	01001	873		096	11011	01001
842		103	11010	01010	874		106	11011	01010
843		113	11010	01011	875		116	11011	01011
844		123	11010	01100	876		126	11011	01100
845		133	11010	01101	877		136	11011	01101
846		143	11010	01110	878		146	11011	01110
847		153	11010	01111	879		156	11011	01111
848		005	11010	10000	880		007	11011	10000
849		015	11010	10001	881		017	11011	10001
850		025	11010	10010	882		027	11011	10010
851		035	11010	10011	883		037	11011	10011
852		045	11010	10100	884		047	11011	10100
853		055	11010	10101	885		057	11011	10101
854		065	11010	10110	886		067	11011	10110
855		075	11010	10111	887		077	11011	10111
856		085	11010	11000	888		087	11011	11000
857		095	11010	11001	889		097	11011	11001

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
890	7	107	11011	11010
891		117	11011	11011
892		127	11011	11100
893		137	11011	11101
894		147	11011	11110
895		157	11011	11111
896	8	000	11100	00000
897		010	11100	00001
898		020	11100	00010
899		030	11100	00011
900		040	11100	00100
901		050	11100	00101
902		060	11100	00110
903		070	11100	00111
904		080	11100	01000
905		090	11100	01001
906		100	11100	01010
907		110	11100	01011
908		120	11100	01100
909		130	11100	01101
910		140	11100	01110
911		150	11100	01111
912		001	11100	10000
913		001	11100	10001
914		021	11100	10010
915		031	11100	10011
916		041	11100	10100
917		051	11100	10101
918		061	11100	10110
919		971	11100	10111
920		081	11100	11000
921		091	11100	11001

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT
922	8	101	11100	11010
923		111	11100	11011
924		121	11100	11100
925		131	11100	11101
926		141	11100	11110
927		151	11100	11111
928		002	11101	00000
929		012	11101	00001
930		022	11101	00010
931		032	11101	00011
932		042	11101	00100
933		052	11101	00101
934		062	11101	00110
935		072	11101	00111
936		082	11101	01000
937		092	11101	01001
938		102	11101	01010
939		112	11101	01011
940		122	11101	01100
941		132	11101	01101
942		142	11101	01110
943		152	11101	01111
944		003	11101	10000
945		013	11101	10001
946		023	11101	10010
947		033	11101	10011
948		043	11101	10100
949		053	11101	10101
950		063	11101	10110
951		073	11101	10111
952		083	11101	11000
953		093	11101	11001

*See note on first sheet of Table B.

TABLE B (Contd)

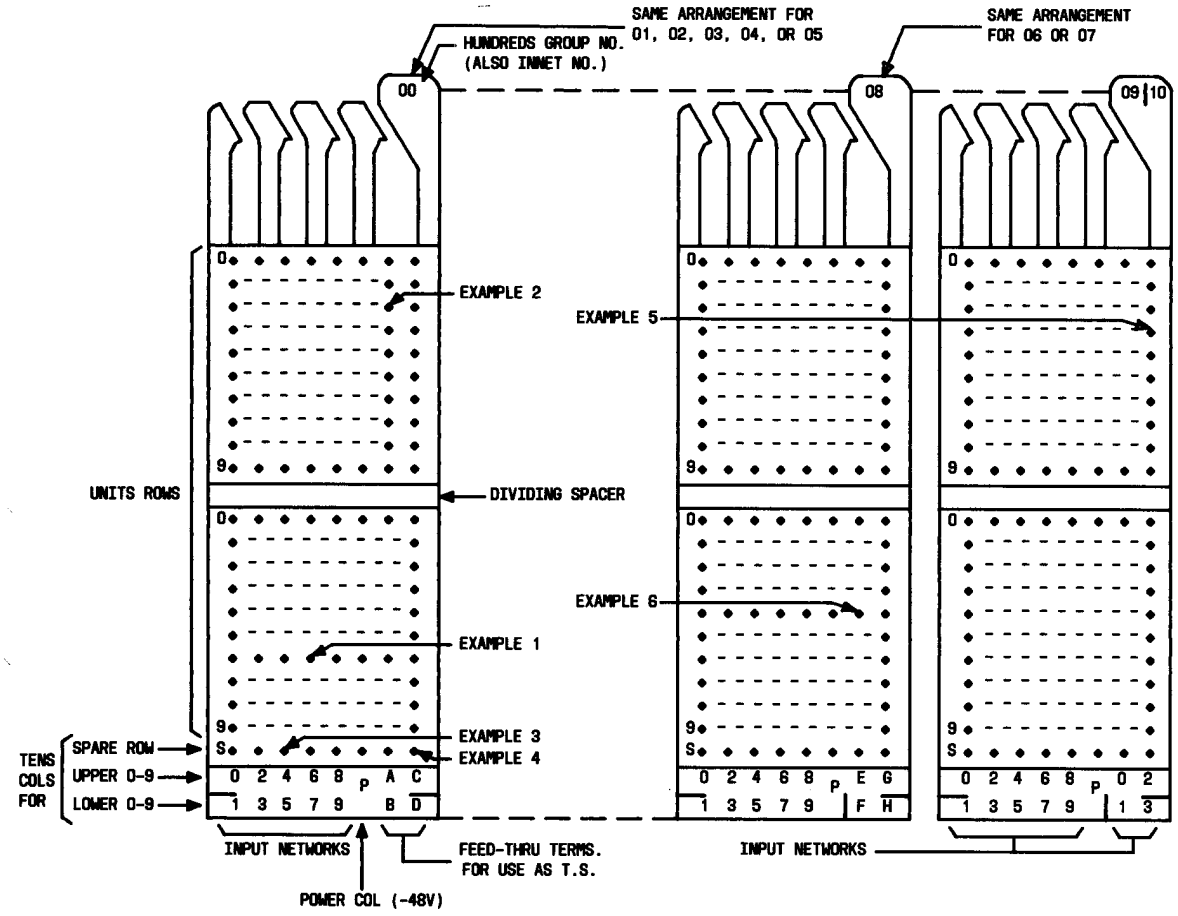
REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
954		103	11101	11010	986		106	11110	11010
955		113	11101	11011	987		116	11110	11011
956		123	11101	11100	988		126	11110	11100
957		133	11101	11101	989		136	11110	11101
958		143	11101	11110	990		146	11110	11110
959		153	11101	11111	991		156	11110	11111
960		005	11110	00000	992		007	11111	00000
961		015	11110	00001	993		017	11111	00001
962		025	11110	00010	994		027	11111	00010
963		035	11110	00011	995		037	11111	00011
964		045	11110	00100	996	8	047	11111	00100
965		055	11110	00101	997		057	11111	00101
966		065	11110	00110	998		067	11111	00110
967		075	11110	00111	999		077	11111	00111
968	8	085	11110	01000	1000		087	11111	01000
969		095	11110	01001	1001		097	11111	01001
970		105	11110	01010	1002		107	11111	01010
971		115	11110	01011	1003		117	11111	01011
972		125	11110	01100	1004		127	11111	01100
973		135	11110	01101	1005		137	11111	01101
974		145	11110	01110	1006		147	11111	01110
975		155	11110	01111	1007		157	11111	01111
976		006	11110	10000	1008		000	11111	10000
977		016	11110	10001	1009		010	11111	10001
978		026	11110	10010	1010		020	11111	10010
979		036	11110	10011	1011		001	11111	10011
980		046	11110	10100	1012		011	11111	10100
981		056	11110	10101	1013	9	021	11111	10101
982		066	11110	10110	1014		002	11111	10110
983		076	11110	10111	1015		012	11111	10111
984		086	11110	11000	1016		022	11111	11000
985		096	11110	11001	1017		003	11111	11001

*See note on first sheet of Table B.

TABLE B (Contd)

REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY		REGISTER NO.	*INNET		INPUT VERIFICATION TEST CARD DISPLAY	
	NO.	TERM	BLOCK	INPUT		NO.	TERM	BLOCK	INPUT
1018	9	013	11111	11010					
1019		023	11111	11011					
1020		005	11111	11100					
1021		015	11111	11101					
1022		025	11111	11110					
1023		006	11111	11111					

*See note on first sheet of Table B.



EXAMPLES:

1. INPUT NUMBER (P-) 0076
   HUNDREDS — UNITS, TENS
2. FEED-THRU TERM NO. 00A2
   HUNDREDS — UNITS, TENS
3. * SPARE INPUT 005S
   HUNDREDS — UNITS, TENS
4. FEED-THRU TERM 00DS
   HUNDREDS — UNITS, TENS
5. INPUT NO. 1023
6. INPUT NO. 08F4

NOTE;
THE TERMINALS ON THE INPUT NETWORKS (INNETS) ARE ARRANGED AND NUMBERED FOR THE G OPTION.

Fig. 1—Arrangement of Input Networks (INNETS) for the G Options