

TRANSACTION NETWORK
SYNCHRONOUS LINE ADAPTER FRAME J70179B
DESCRIPTION AND THEORY

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I. SLA Relay Panel	4	1.01 This section contains the physical and functional descriptions and theory of operation of the Transaction Network (TN) equipment used in the J70179B synchronous line adapter (SLA) frame. This equipment consists of the J70179BA SLA unit, J70179BB power plant, and J70179AM fuse panel. Also used in the SLA frame are the 46A1 data mounting and 829-type data auxiliary set (DAS); 42A1 data mounting and 201C data set (DS); 208A, and 209A DSs; and 48A1 data mounting and 500A-L1/2, -L1/3, and -L1/4 data service units (DSUs).	
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Note: The term "central processor unit" (CPU) as used in this section refers collectively to the 3A processor and all processor support equipment. The term "message switch" (MS) refers collectively to the CPU and the synchronous, asynchronous, and dial line adapter frames (SLA, ALA, and DLA, respectively).

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Also included in the message switch are the audio response (AR) and switch control and monitor (SCAM) frames.

1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 Figure 1 is a block diagram of the overall TN. Inquiry messages may originate from polled or dial-in stations and are transferred by the MS to a customer service center (CSC). Response messages are routed back to the inquiring station through the MS. The ALA serves as an interface and buffer between the CPU and the data station selector (DSS) or data station controller (DSC) used in polled service. The DLA serves as an interface and buffer between the CPU and 407 DS used in dial-in service. The interface to the data processing center is through an SLA and 200-type DSs or 500A-type DSUs.

1.04 The SLA enables the CPU to communicate with a CSC over high-speed synchronous data links. The SLA provides flexibility with regard to line protocols and transmission codes, while imposing minimal real-time demands on the CPU. It interfaces the parallel input/output subparallel channel (SPCH) of the CPU through the duplex bus selector (DBS). The SLA is capable of operating with data sets or in the digital data system (DDS) with DSUs at 2400, 4800, or 9600 bits per second (bps).

1.05 The SLA provides the following features:

- (a) Full or half-duplex synchronous communication for a single data link
- (b) Buffering of messages to and from the communications line
- (c) Special characters, whose receipt necessitates CPU intervention, can be detected and an interrupt generated
- (d) Interrupts can be generated at selected levels of buffer fill
- (e) CPU program control of character length, parity, interrupt generation, threshold interrupt control, synchronization, idle characters, and recognition of selected special characters.

2. PHYSICAL DESCRIPTION

2.01 A typical SLA frame bay arrangement is shown in Fig. 2. The frame is in Configuration A, which controls twelve 2400 bps lines. This frame arrangement accommodates equipment for 6 SLA units (12 SLAs) for a maximum of 12 channels. Other configurations are available according to the type of service required. These are as follows:

- (a) Configuration A—twelve 2400 bps analog channels
- (b) Configuration B—six 2400 and two 4800 or two 9600 bps analog channels
- (c) Configuration C—six 2400 bps analog channels and five 2400, 4800, or 9600 bps digital channels
- (d) Configuration D—six 4800 or 9600 bps analog channels
- (e) Configuration E—reserved for future use
- (f) Configuration F—ten 2400, 4800, or 9600 bps digital channels.

A. J70179BA SLA Unit

2.02 An SLA unit (Fig. 3) consists of two SLAs and two DBSs. The unit is 4 inches high, 10-1/2 inches deep, and 23-1/4 inches wide. It is mounted with 1008A mounting plates in 23-inch racks. A fully equipped SLA unit weighs 24 pounds. Each SLA consists of seven circuit packs, one each of FC343 through FC349. A description of the DBS is contained in Section 230-100-440.

2.03 The only options in the SLA are the address (option A), interrupt identification lead ID, and data set power monitor (option Z). The address is set by adjusting the 16-position switch on FC343 as shown in Table A. ID is set by connecting cable assembly ED-73627-ID, G1 from terminal 201 on FC348 to terminals on the parallel bus, as shown in Table A. The data set power monitor (option Z) defeats the check for data set power. It is installed when using DSUs by grounding lead 301 on FC349.

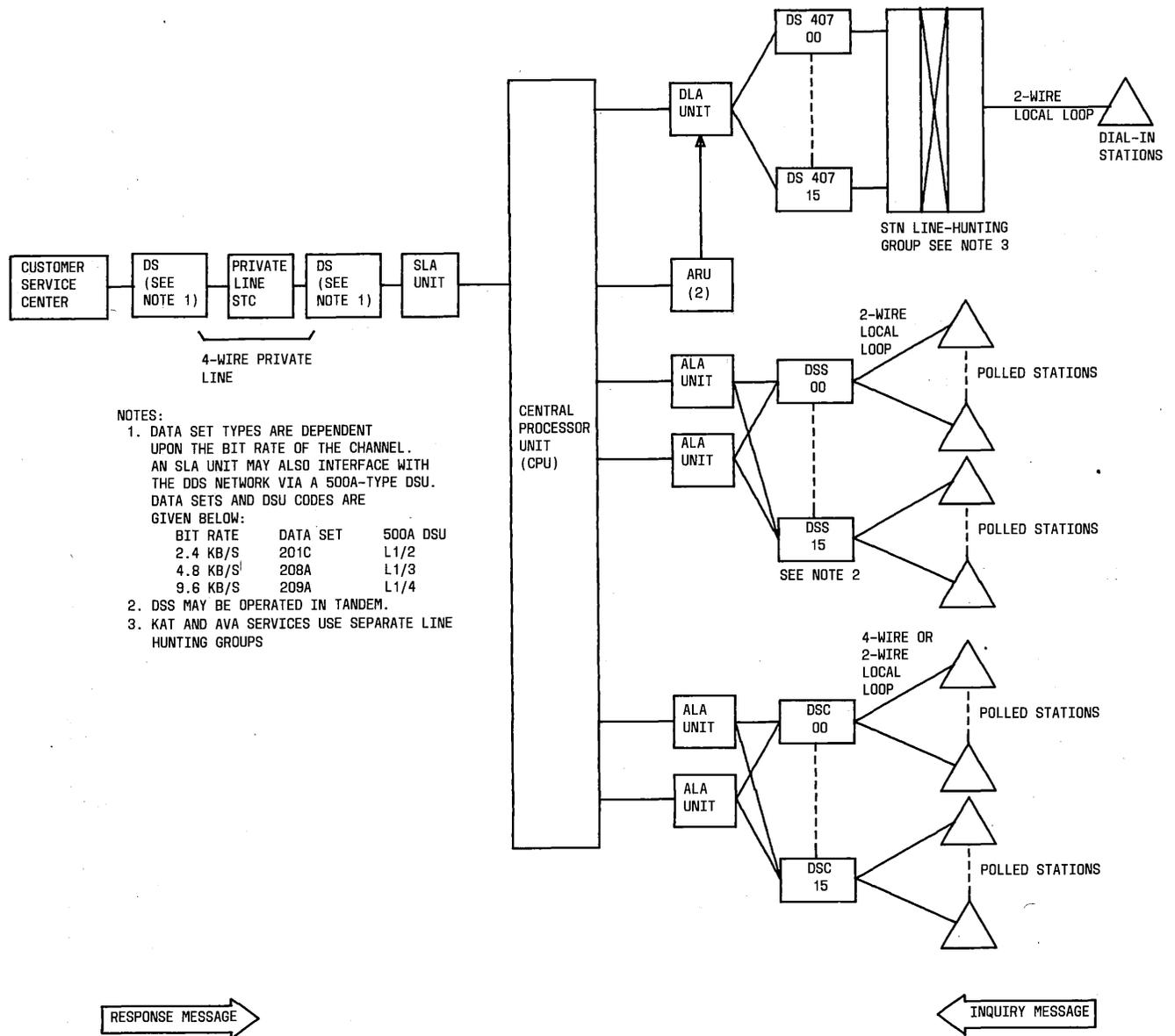


Fig. 1—Transaction Network—Block Diagram

B. 46A1 Data Mounting and 829-Type DAS

2.04 An SLA frame uses up to two 46A1 data mountings to house up to eight 829 DASs each. Power for the 829 DASs, 24 Vac, is supplied from transformers in the data mountings. Input power is supplied from the 117 Vac protected source.

C. 42A1 Data Mounting and 201C Data Set

2.05 An SLA frame uses up to two 42A1 data mountings to house up to six 201C DSs each. 201C DS transmits and receives synchronous, binary, serial data at a rate of 2400 bps. Power is supplied directly to the data set from the 117 Vac protected power source.

D. 208A and 209A Data Sets

2.06 An SLA frame uses up to six 208A or 209A DSs mounted with D-180556 mounting brackets. 208A and 209A DSs transmit and receive synchronous, binary, serial data at a rate of 4800 and 9600 bps, respectively. Power is supplied directly to the data sets from the 117 Vac protected power source.

E. 48A1 Data Mounting and 500A-Type DSU

2.07 An SLA frame uses up to two 48A1 data mountings which house up to five 500A-type DSUs each. 500A-L1/2, -L1/3, and -L1/4 DSUs transmit and receive bipolar digital data at a rate of 2400, 4800, and 9600 bps, respectively. Power is supplied directly to the DSUs from the 117 Vac protected power source.

F. J70179BB Power Panel

2.08 An SLA frame uses up to two J70179BB power panels which house up to six 131F power units each. The 131F power units receive power from the telephone company (telco) central office -48 Vdc battery and supply a regulated +5 Vdc to each SLA unit. Each SLA is supplied -12 Vdc from linear regulators mounted behind the 131F power units. The power panels are mounted with 1008A mounting plates.

G. J70179AM Fuse Panel

2.09 The fuse panel (Fig. 4) provides fusing for the -48 Vdc central office battery supply to the SLA frame. The fuse panel contains a diode isolation circuit which prevents faults on one -48V bus from being reflected into the second -48V bus and permits the 131F power units to operate from either or both -48V busses. A fuse alarm (FA) indicator lamp and an external alarm indication (contact closure) are also provided. Fuse assignments are as follows:

- (a) F1 through F6 to lower power shelf on frame (PU1 through PU6)
- (b) F7 through F12 to upper power shelf on frame (PU7 through PU12).

H. Interunit Wiring

2.10 There are five configurations of the SLA frame available. A typical example of interunit

signal cabling shown in Fig. 5 is Configuration B. Power cabling is shown in Fig. 6.

I. SLA Relay Panel

2.11 The SLA relay panel is located on the SCAM frame. The relay panel will switch a spare SLA, data set, and DBS combination into service when one fails. There is one spare SLA, data set, and DBS combination for each type of data set or DSU used in the central office. When using 200-type DSs, an analog loopback of the transmission facility, under control of the CPU, can be provided by the relay panel.

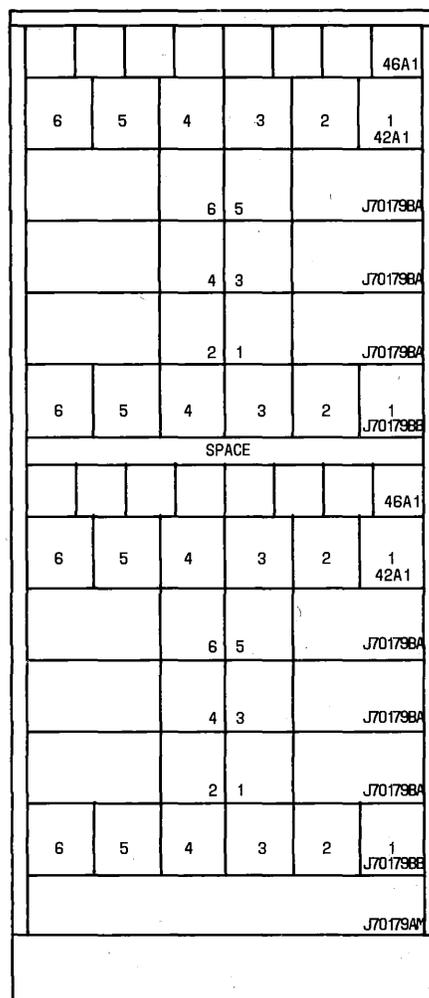


Fig. 2—SLA Frame—Configuration A

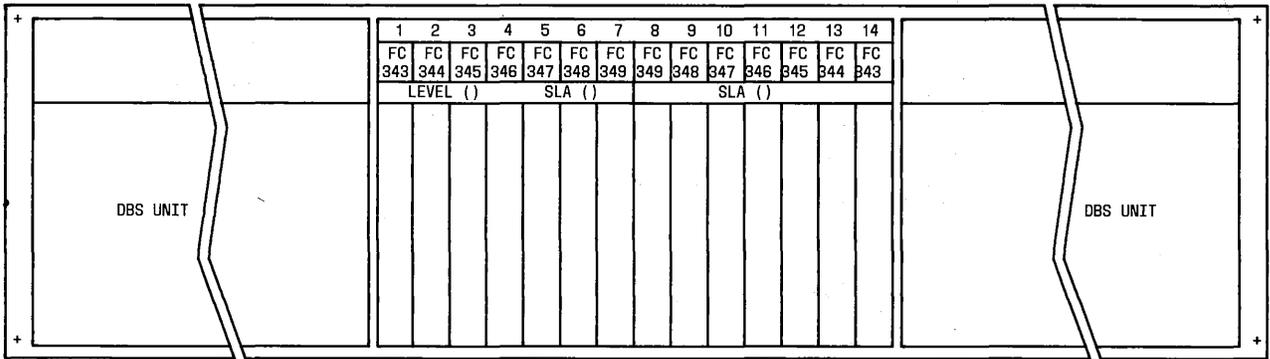


Fig. 3—Synchronous Line Adapter Unit

TABLE A

ADDRESS	SET ADDRESS SWITCH ON FC 343 TO (LOC 02-16 & 02-29)	FOR CKT A LOC 02-21 CONNECT TERM 201 TO LOC 02-20 TERMINAL	FOR CKT B LOC 02-24 CONNECT TERM 201 TO LOC 02-25 TERMINAL	DESIGNATION
00	0	202	202	INF000
01	1	203	203	INF010
02	2	303	303	INF020
03	3	204	204	INF030
04	4	304	304	INF040
05	5	305	305	INF050
06	6	206	206	INF060
07	7	306	306	INF070
08	8	002	002	INF080
09	9	003	003	INF090
10	10	103	103	INF100
11	11	004	004	INF110
12	12	104	104	INF120
13	13	006	006	INF130
14	14	105	105	INF140
15	15	106	106	INF150

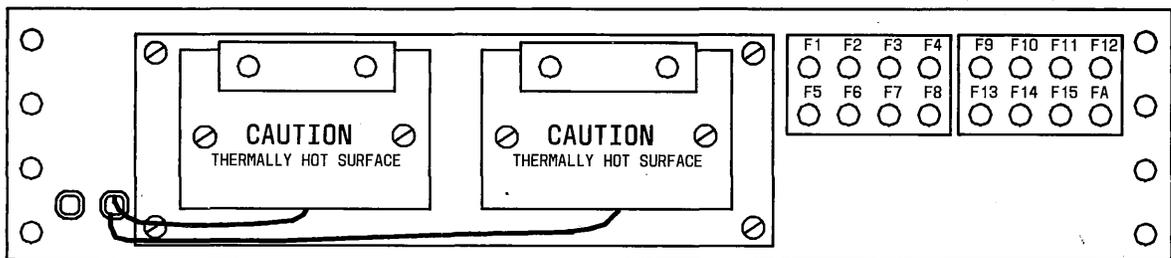
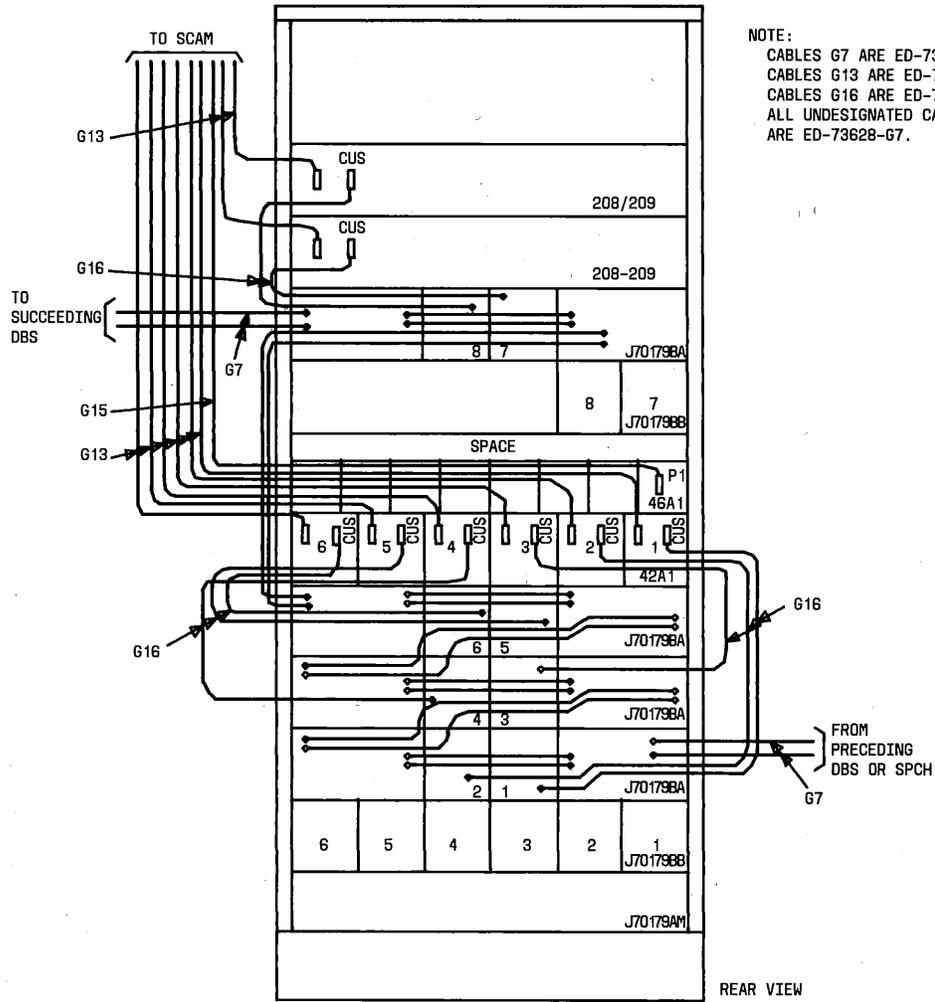


Fig. 4—Fuse Panel



NOTE:
 CABLES G7 ARE ED-73628-G7,
 CABLES G13 ARE ED-73628-G13,
 CABLES G16 ARE ED-73628-G16,
 ALL UNDESIGNATED CABLES
 ARE ED-73628-G7.

Fig. 5—SLA Frame—Configuration B—Signal Cabling

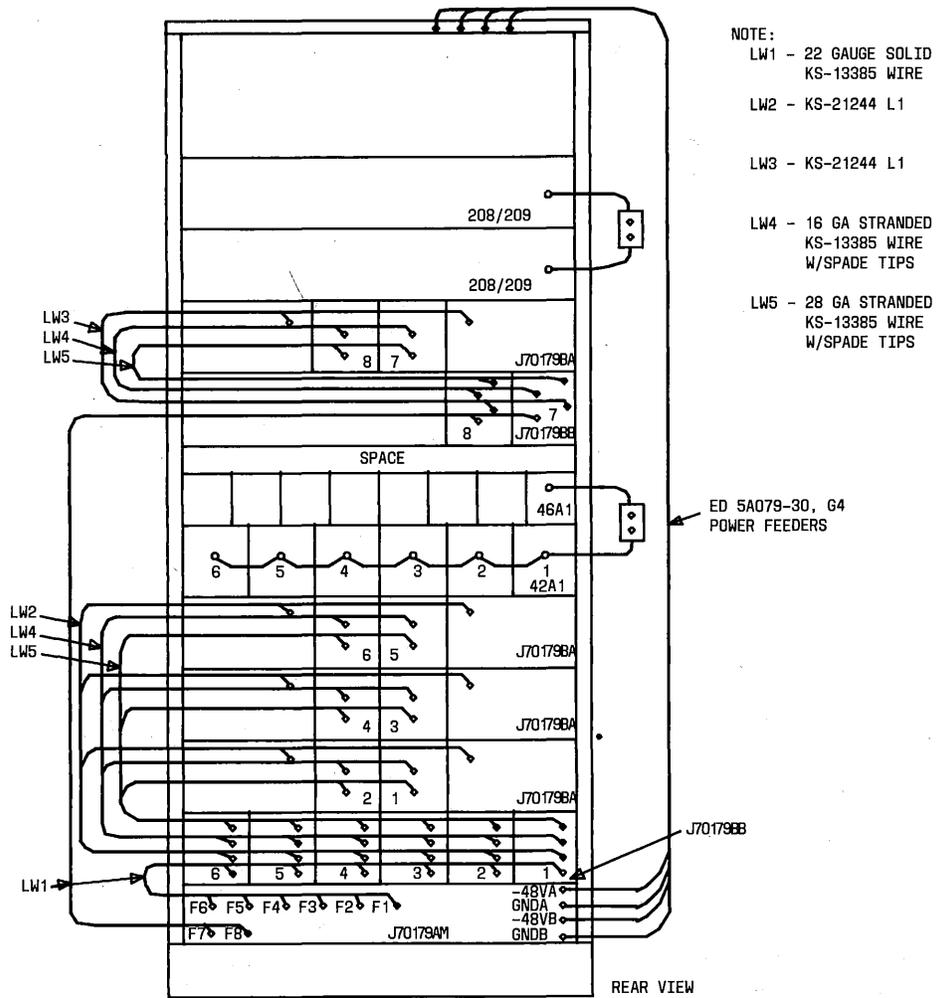


Fig. 6—SLA Frame—Configuration B—Power Cabling

3. FUNCTIONAL DESCRIPTION

A. Introduction

3.01 Figure 7 is a block diagram of a synchronous port to the CPU showing one SLA unit. The parallel bus from an SPCH can support up to 16 SLA units. The parallel bus is in a duplex (redundant) configuration, one bus from an SPCH is associated with CPU 0 and one bus from an SPCH is associated with CPU 1. In the standard message switch configuration, the DBS is connected to SPCH2 from both CPUs. The DBS connects the SLA unit to one of the busses under control of the CPU software. The duplex arrangement permits system operation to continue with a single CPU or bus failure. SLA units share the parallel

bus from SPCH2 with the ARV and SCAM, SLA's cannot share a bus with ALAs or DLAs.

3.02 A parallel bus consists of 36 leads; 6 address leads, 18 information leads, 6 control leads, 5 response leads, and 1 clock lead. The address, control, and clock leads carry signals from the CPU; the response leads carry signals to the CPU; and the information leads are bidirectional. The clock lead, one response lead, and one control lead are not used by the SLA.

3.03 The parallel bus uses transformer-coupled ac signals which are converted to transistor-transistor logic (TTL) level signals by the DBS. The active state (logic 1) of these signals at the output of the DBS is low (ground). Elsewhere

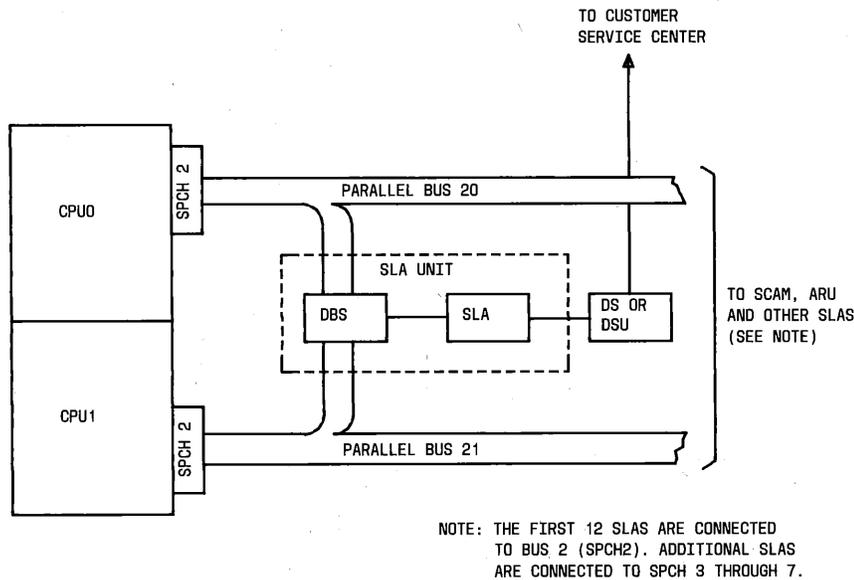


Fig. 7—SLA Synchronous Port

within the SLA unit, a logic 1 is high (positive voltage).

3.04 The 200-type data set transmits and receives phase shift keyed (PSK) data in conjunction with a data set at the data base location via 4-wire private line. The 201C, 208A, and 209A DSs operate in the duplex mode at 2400, 4800, and 9600 bps, respectively. The 500A-type DSUs transmit and receive bipolar digital data in conjunction with the 4-wire DDS to the data base. The 500A-L1/2, -L1/3, and -L1/4 DSUs provide service at 2400, 4800, and 9600 bps, respectively.

B. Interfaces

3.05 The interfaces between the parallel bus (via the DBS) and the SLA, and between the data set and the SLA are shown in Fig. 8. There are 6 address leads, 18 information leads, 5 command leads, and 4 response leads between the SLA and the CPU. Between the SLA and data set is the normal Electronic Industries Association (EIA) RS-232C interface.

3.06 The address of the SLA, to which the CPU sends data or commands, is transferred via the address (ADR) leads. ADR010 through ADR040 carry the binary address of the SLA. ADR000 is a "0" for normal address or a "1" for maintenance

address. ADR050 is the address parity bit (odd parity).

3.07 The bidirectional information (INF) leads are divided into two groups. The first eight leads, INF000 through INF070, are used for bidirectional transfer of data between the CPU and the SLA and to address the SLA internal registers from the CPU. Leads INF080 through INF150 are used for transfer of software data from the CPU to the SLA internal registers. The INF leads are also used to transfer the status of the SLA internal registers to the CPU. Direction of transfer and data transferred are selected by command signals from the CPU. Information parity low lead (INFPL0) and information parity high lead (INFPH0) are the parity bits for leads INF000 through INF070 and INF080 through INF150, respectively.

3.08 There are five command signals that may be sent by the CPU to the SLA. Two commands can be sent with either a normal address or a maintenance address. The command signals are as follows:

- (a) **Data Present (DP0) normal address:**
CPU requests the SLA transmit buffer to receive data from the information leads.

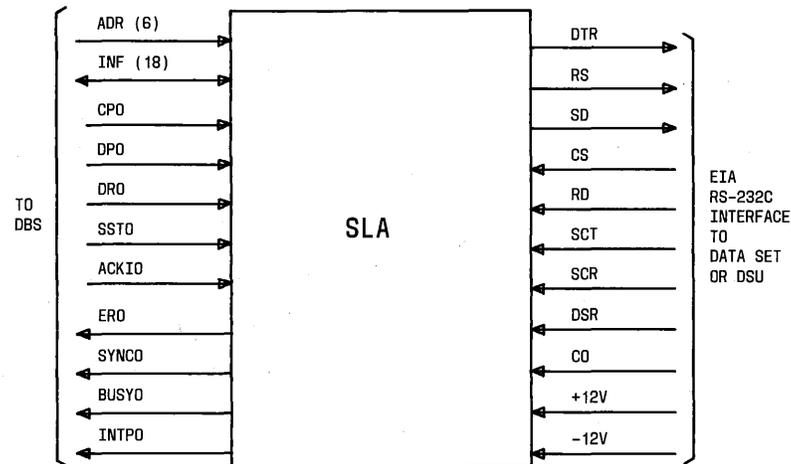


Fig. 8—SLA Interface Leads

(b) **Data Present (DPO) maintenance address:** CPU requests the SLA transfer register to receive data from the information leads.

(c) **Data Request (DRO) normal address:** Transfers one word from the SLA receive buffer onto leads INF000 through INF070. It also transfers the SLA receiver status onto leads INF080 through INF150. A "1" on lead:

- INF100 indicates overflow of receive buffer (over 64 characters in buffer)
- INF110 indicates loss of carrier from data set
- INF120 indicates a parity error on line from the CSC
- INF130 indicates receive hardware error
- INF150 indicates that the receive buffer is not empty
- INF080, INF090, and INF140 are not used.

(d) **Sense Status (SSTO) normal address:** Transfers the SLA address onto leads INF000 through INF050 from ADR000 through ADR050, and transfers SLA transmit buffer status onto leads INF080 through INF150. An SSTO command must be accepted and properly responded to by

the SLA regardless of its busy status. A "1" on lead:

- INF100 indicates transmit buffer underflow (buffer empties before message completed)
- INF130 indicates transmit hardware error
- INF150 indicates transmit buffer ready
- INF080, INF090, INF110, INF120, and INF140 are not used.

(e) **Sense Status (SSTO) maintenance address:** Transfers the character in the SLA transfer register onto leads INF000 through INF150.

(f) **Acknowledge Interrupt (ACKIO) no address:** Used to identify the SLA requesting interrupt. When ACKIO is issued, each SLA requesting interrupt sets a "1" on a predefined lead of INF000 through INF150. (See Table A.)

(g) **Command Present (CPD) normal address:** Requests SLA to receive a command via the information leads from the CPU. Transfers control information and parameters from the CPU to the SLA internal registers where they are retained for use during subsequent operations. The operation (OP) code field, on leads INF010 and INF020, define the

function to be performed by the SLA. The four functions are:

- OP = 00—initialize SLA
- OP = 01—clear selected buffer (receive, transmit, or both as determined by the state of INF080 and INF090)
- OP = 10—write SLA register. INF030 through INF070 contains the address of the register.
- OP = 11—read SLA register. INF030 through INF070 contains the address of the register.

Using this command, SLA parameters and special characters can be defined, receive and transmit operations can be initiated and continued, and detailed SLA and data set status information can be assembled for subsequent reading by the sense status (SST) command.

3.09 There are three response leads to the CPU used by the SLA as follows:

- (a) **ERO**—error condition detected by the SLA except lead CP0
- (b) **SYNCO**—After a command signal has been received, the SLA sets SYNCO to “1” to indicate that the command signal has been understood and data has been gated onto or from the information leads
- (c) **BUSYO**—same as SYNCO.

3.10 There is an interrupt lead to the CPU used by the SLA. This lead, if enabled, is used to notify the CPU if any of the following conditions occur:

- (a) Receive buffer counter equals or exceeds the preset threshold level
- (b) A special character was detected in the received data stream
- (c) The data set loss of carrier occurred
- (d) Transmit buffer counter equals or exceeds the preset threshold level

(e) The transmit buffer has underflowed.

3.11 The initialize periphery lead is not used by the SLA.

C. SLA Functional Description

3.12 A block diagram of the SLA is shown in Fig. 9. The SLA is broken down into functional blocks represented by circuit packs. The address leads, ADR000 through ADR050, from the CPU are connected to an address decoder on FC343. Also connected to FC343 are bidirectional leads, INF000 through INF070 and INFPL0, which carry the low-order information. The high-order information leads, INF080 through INF150 and INFPH0, and command leads are connected to FC344. The commands are decoded and distributed from FC344. Low-order information enters the bus interface circuit packs and is loaded into the transmit buffer on FC345. There, the parallel information is converted into serial data and transmitted to the data set via EIA drivers on FC349. The serial data is transmitted at a rate determined by the data set clock. When the transmit buffer is emptied to a preset level, an interrupt is sent to the CPU indicating the buffer will underflow if the remainder of the message is not sent from the CPU. The transmit interrupt circuit pack (FC346) checks the level of the transmit buffer and delivers the interrupt signal to the CPU.

3.13 The data set receive clock steps serial data, via lead RD, into the data set interface circuit pack (FC349). The data is converted to parallel form and enters the receive buffer on FC347. The receive interrupt circuit pack (FC348) delivers an interrupt signal to the CPU when a predetermined number of characters have been delivered to the receive buffer. The interrupt lead notifies the CPU to empty the receive buffer before it overflows. The parallel data is then sent to the CPU via the INF000 through the INF070 leads.

D. Bus Interface Low FC343

3.14 The bus interface low circuit pack (FC343) is shown functionally in Fig. 10. Address leads ADR00 through ADR050 carry the address to the circuit pack. The address decoder compares the incoming address to a 16-position switch, which was set at installation with the specific address of the SLA. If the address is correct, the command

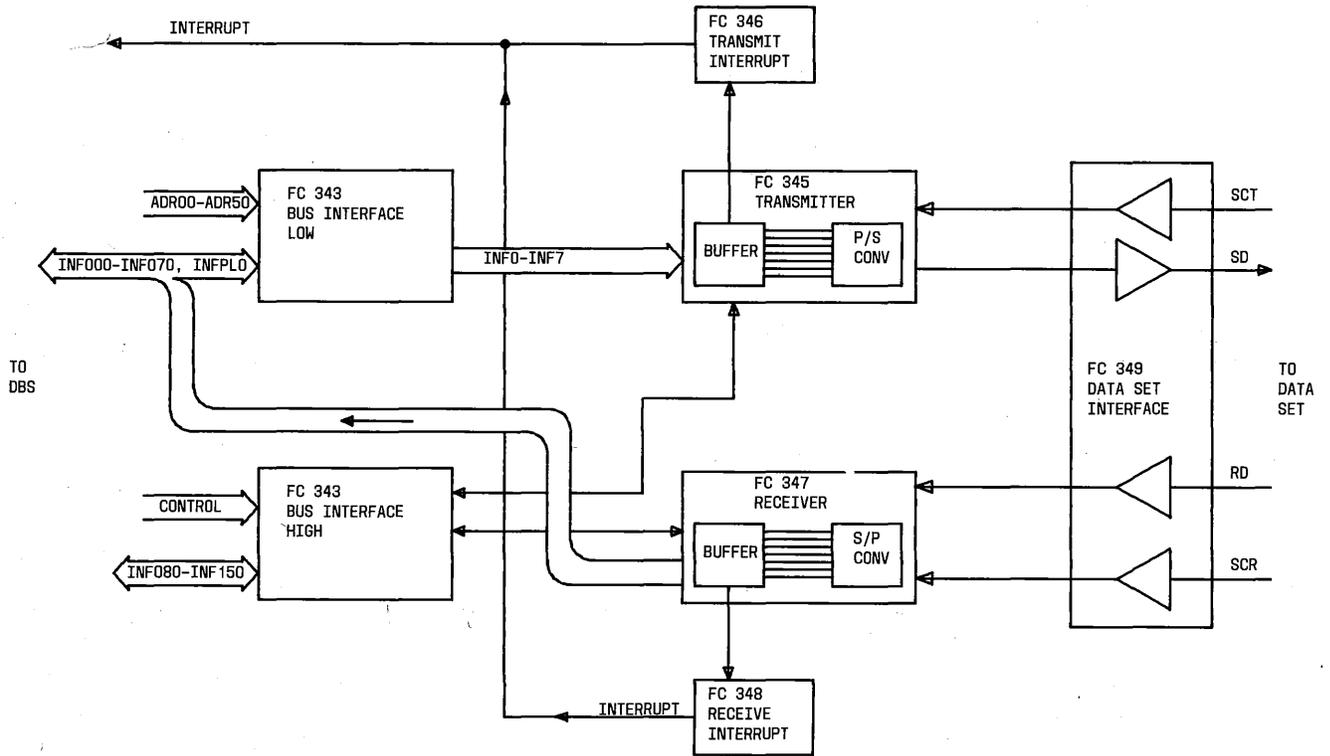


Fig. 9—SLA Block Diagram

decoder on FC344 and all bus terminators are enabled.

3.15 Low-order information leads (INF000 through INF070) and parity lead INFPL0 are connected to the bus terminators. From there the data is distributed to the SLA transmit buffer, transfer register, and command present (CP) decoder. The transfer register, upon command, transfers data from leads T0 through T7 and presents it to the bus drivers. From there the information can be returned to leads INF000 through INF070. The parity generator generates a parity bit (over INF000 through INF070). For outgoing data this bit is applied to the INFPL0 lead. For incoming data this bit is compared with the incoming parity bit (INFPL0) in the parity comparator. If they do not agree, an error signal is sent to the CPU. The SLA address can be looped back to the CPU on leads INF010 through INF050 via the address return upon SST command.

3.16 Leads T3 through T7 and send device command are connected to the CP decoder. When the CP decoder is enabled by command present, leads T3 through T7 contain the binary address of registers internal to the SLA. The CP decoder decodes the binary address and enables the addressed internal register.

E. Bus Interface High FC344

3.17 The bus interface high-circuit pack (FC344), shown functionally in Fig. 11, is similar to FC343. The bus terminators, parity generator, parity comparators, and transfer register are identical to those of FC343. The transfer register can transfer information from leads T8 through T15 to the bus drivers and transfer information on R8 through R15 from the program registers to the bus drivers. Information on leads T8 through T15 are transferred to the transfer register using the data present (DP) command along with the maintenance address of the SLA. Information from a specific internal register is presented to the transfer register by using the CP command to address it from the CP decoder on FC343 and using OP code 11. The information is then transferred to the bus drivers using maintenance address and SST command.

3.18 The command leads from the CPU are interfaced on FC344. They are connected to the multiple command detector and command

decoder. The multiple command detector will send an error indication on lead ERO to the CPU if more than one command is received at the same time or if a command is received while another command is being executed. The command decoder sends a "1" on lead SYNC0 to the CPU 250 ns after a command has been received. Then it decodes the command and distributes information to the appropriate circuits.

3.19 Three response leads to the CPU are controlled by the command decoder. A "1" is sent to the CPU on SYNC0 250 ns after a command is received. The BUSY0 lead is the same as SYNC0. The ERO lead carries an error indication to the CPU when a multiple command or parity error is detected. In the cost of CP commands, the meaning of ERO is reversed. Normally, every pulse on CP will cause a 1 on ERO. If an error is detected during CP, then ERO is held at 0.

3.20 The OP code decoder circuit decodes the OP code of the CP command and distributes the information to the appropriate circuits. OP code 00 (initialize SLA) puts a pulse on the CLEROL lead and clears all of the internal registers in the SLA. OP code 01 (clear transmit or receive, or both buffers) is the CLT or CREC lead. OP code 10 (write SLA register) is the RCOP1 and RCOP2 leads and it enables the addressed internal register to receive program information. Finally, OP code 11 (read SLA register) is the RC11 lead and it enables the transfer register to be loaded with the contents of the selected register.

F. Transmitter FC345

3.21 The transmitter circuit pack (FC345) is shown functionally in Fig. 12. Information is brought in on leads T0 through T7 to the transmit buffer. Parity lead PL1 and leads T8, T9, and T10 also enter the transmit buffer. The transmit buffer is a first-in/first-out (FIFO) device which can hold up to 64 characters, each 12 bits wide. Eight bits are used for data, the remaining four bits carry control information or are spare.

3.22 The output of the transmit buffer goes to the parallel-to-serial converter. This circuit converts the parallel data into serial form and sends it to the data set interface circuit pack (FC349) at the speed of the data set clock (lead SCT).

3.23 The monitor and error circuits check for parity errors and monitor the state of the transmit buffer. The circuit generates a parity bit from the output of the buffer and compares it with the parity bit which passed through the transmit buffer. If they do not agree, a transmit hardware error indication is sent to the CPU on lead INF130 during an SST command. The monitor circuit under SST command sends an indication on lead:

- (a) INF100 if the buffer underflows (buffer empties before message is completed)
- (b) INF130 transmit hardware error
- (c) INF150 if the buffer is ready to accept data.

3.24 There are two internal registers on FC345, indicated by the program store block. The register with address AD3 stores the word length of the characters in the transmit buffer. Words can be programmed to be 5, 6, 7, or 8 bits in length. When parity is selected, an even or odd parity bit is included in these lengths. The internal register with address AD9 stores the idle character. When the clear-to-send (CTS_X) lead is "on" from the data set, the data in the transmit buffer is transmitted from the parallel-to-serial converter to the data set. When the buffer is empty and CTS_X is "on", the idle character in AD9 is transmitted to the data set.

G. Transmit Interrupt FC346

3.25 The transmit interrupt circuit pack (FC346), shown functionally in Fig. 13, sends the interrupt signal to the CPU. High-order information leads T8 through T15 carry software information to the two internal registers with addresses AD8 and AD10. Internal register AD8 can be programmed to enable or disable the interrupt circuit. It also controls the request-to-send (RS) and data terminal ready (DTR) leads going to the data set. Program register AD10 stores the interrupt threshold level N, where $0 \leq N \leq 63$.

3.26 The counter circuit keeps track of the characters transmitted from the transmit buffer. The comparator circuit checks internal register AD10 and the counter circuit. When N or more characters have been read out of the buffer, a signal is sent to the interrupt circuit.

3.27 If an interrupt signal is received and the interrupt circuit is enabled, lead INTPO which goes to the CPU is enabled. The CPU will then enable lead ACKI (acknowledge interrupt) which is monitored by every SLA. The interrupting circuit then enables lead ID to identify itself to the CPU. Lead ID is wired to the DBS at installation. When the transmit buffer is emptied, lead FE (FIFO empty) is enabled and causes an interrupt if the interrupt circuit is enabled.

3.28 The readback circuit is similar to those already described. It can read data from the internal registers to leads R8 through R15. These leads go to the transfer register on FC344 and information is returned to the CPU upon an SST command.

H. Receiver FC347

3.29 The receive circuit pack (FC347), shown functionally in Fig. 14, is the inverse of the transmit circuit pack. Serial data from the data set via lead RD is converted to parallel data in the serial-to-parallel converter. The character length is the same as the transmit word length. This data is brought from internal register AD3 on FC345 via leads WL0 and WL1. Parity, if used, is checked on the incoming data stream.

3.30 The sync search circuit checks the serial data stream for a synchronization character signifying the start of message. When it is detected, data is then read into the receive buffer. Whether or not the synchronization character is transferred to the receive buffer is a software program option.

3.31 Leads RD0 through RD7 carry parallel information from the serial-to-parallel converter to the receive interrupt circuit pack (FC348) and to the receive buffer. The receive buffer is a FIFO which can hold up to 64 characters, each 12 bits wide. Eight bits are used for data, the remaining four bits carry control information or are spare. The data is stored in the buffer until the CPU empties it.

3.32 The FIFO control circuit allows the emptying of the receive buffer upon command from the CPU. It also signals the receive interrupt circuit pack when the buffer is empty (lead BE) and how many characters have been read out (lead CI). Whether or not parity is used in the incoming data stream, a parity bit is generated before and

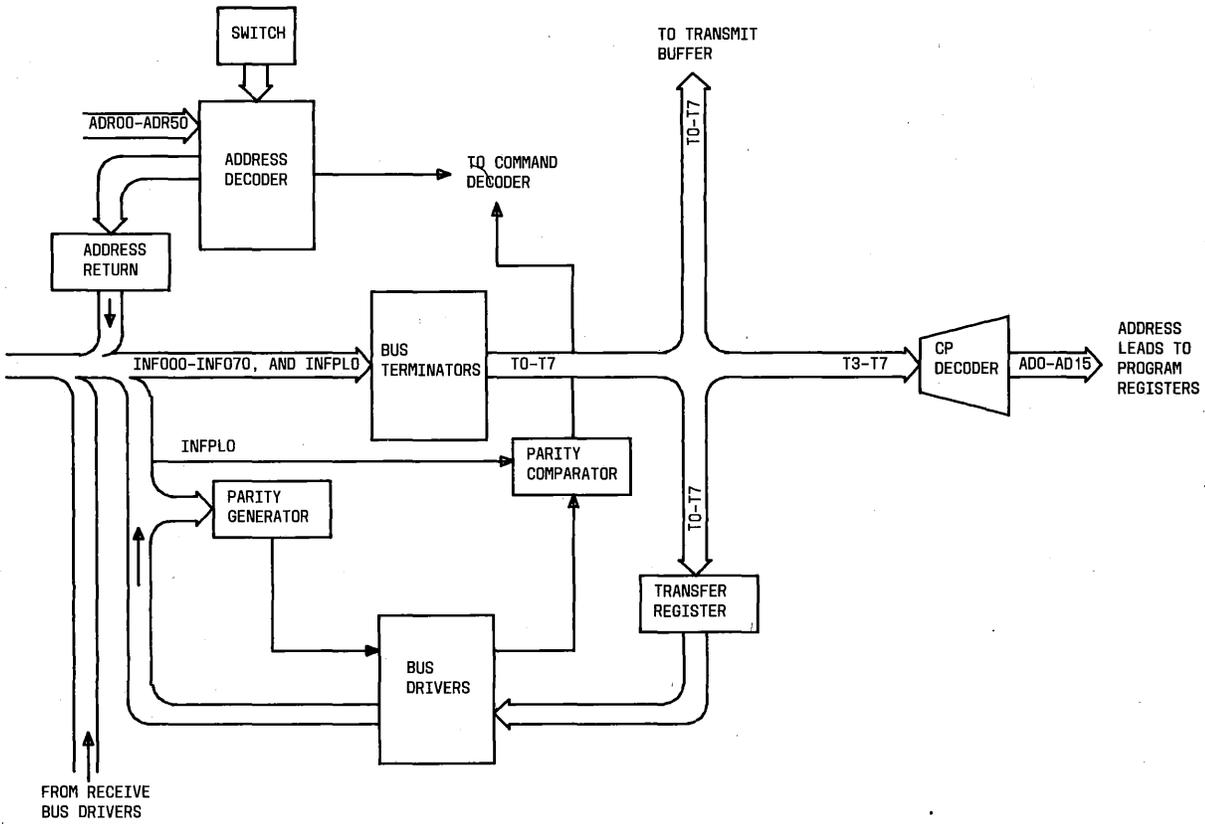


Fig. 10—Bus Interface Low

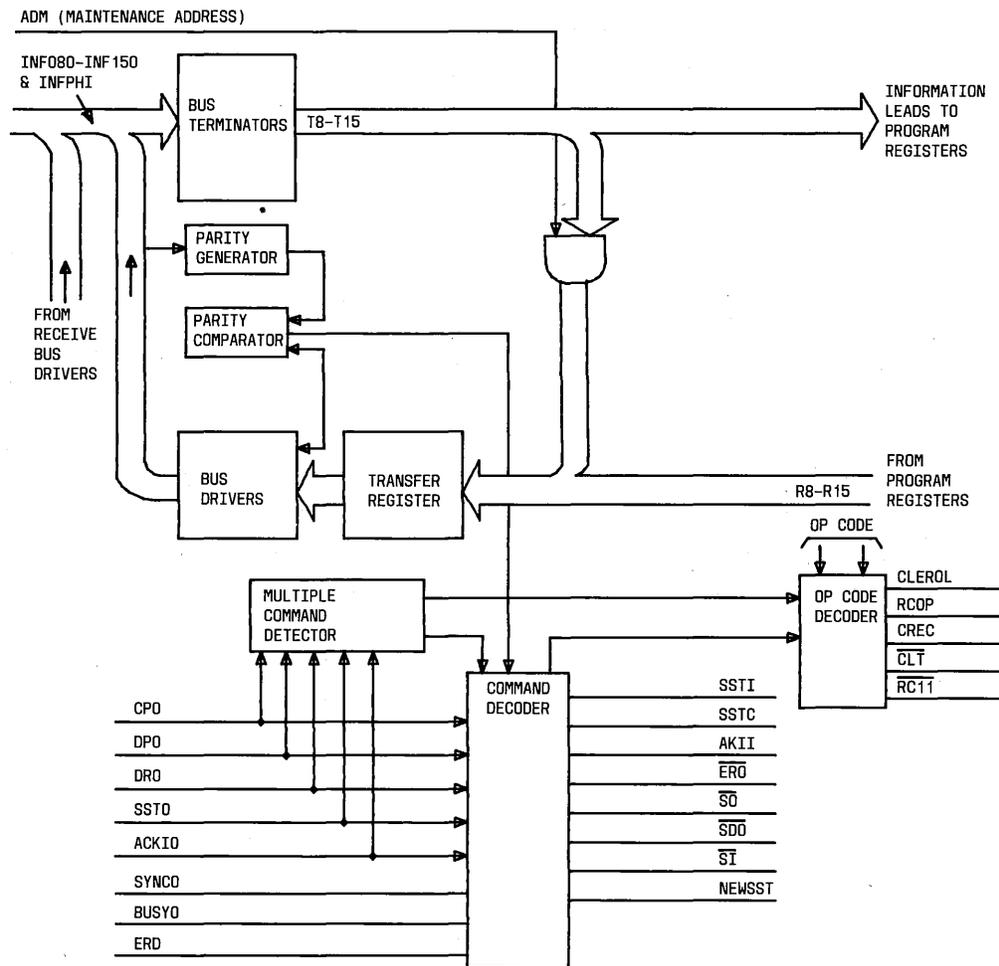


Fig. 11—Bus Interface High

after the data enters the receive buffer. These bits are compared and a receive hardware error indication is sent to the CPU if they do not agree.

3.33 The bus drivers present the information from the receive buffer and FIFO control directly to leads INF000 through INF150 which enter FC343 and FC344 from the DBS. Leads INF000 through INF070 contain data received from the data set receive data leads. When enabled, the status leads (INF100 through INF150) indicate the following:

- (a) INF100—overflow indication (buffer is full and one more character is received)
- (b) INF110—loss of carrier

- (c) INF120—parity error in serial data stream (only if parity is used)
- (d) INF130—receive hardware error (parity error in buffer)
- (e) INF150—data in receive buffer.

3.34 There are two internal registers on FC347 addressed by AD1 and AD2. Internal register AD1 stores the synchronization character which signifies the start of the message from the data set. Internal register AD2 signals the sync search circuit to start looking for a synchronization character and defines the write sync option.

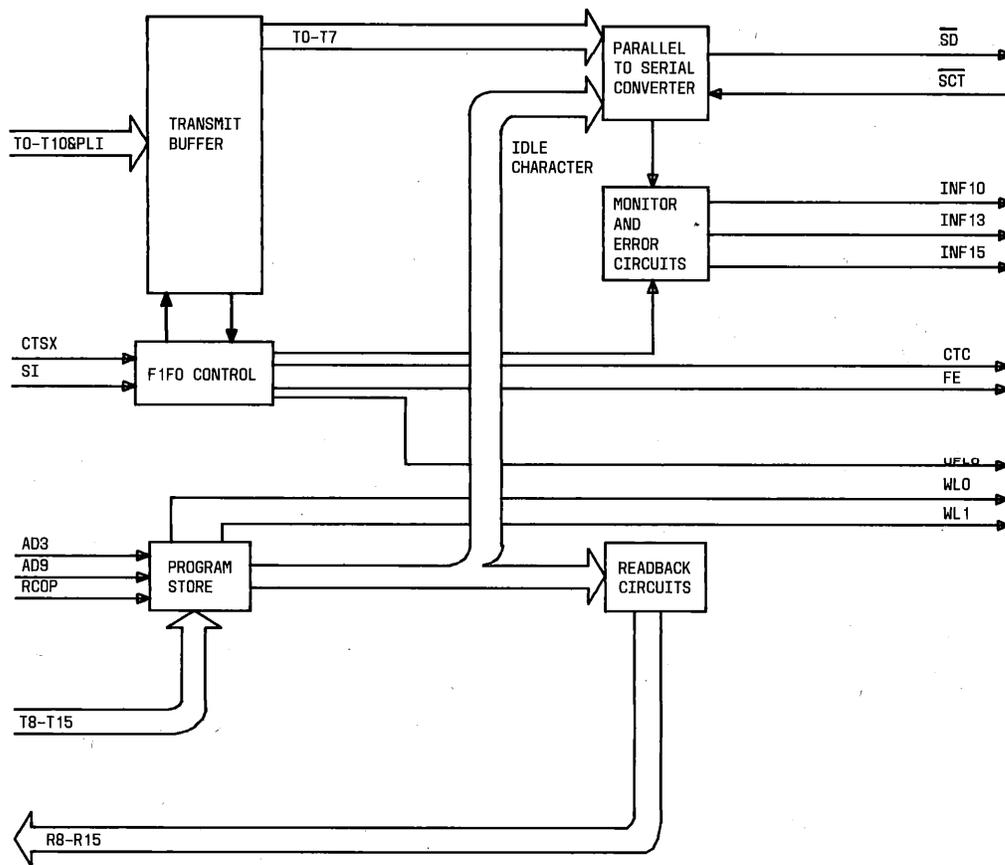


Fig. 12—Transmitter

I. Receive Interrupt FC348

3.35 The receive interrupt circuit pack (FC348), shown functionally in Fig. 15, is similar to the transmit interrupt circuit pack (FC346). High-order information leads T8 through T15 carry software information to the two internal registers (AD0 and AD2) represented by the program store block. Internal register AD0 enables the special character circuit and the receive interrupt circuit. Internal register AD2 stores the interrupt threshold level. AD2 contains bits that are used in the receiver and other bits that are used in the receive interrupt circuit.

3.36 The receive comparator and counter function the same as the transmit comparator and counter circuit. The counter, by monitoring the CI lead, determines how many characters have been written into the receive buffer. When this number equals or exceeds the threshold level, the

comparator enables the RCT lead connected to the interrupt circuit. The counter is reset by the BE lead to ensure that the counter reads 0 when the buffer is empty.

3.37 The receive interrupt circuit is similar to the transmit interrupt circuit. An interrupt can be generated if; the receive buffer equals or exceeds the threshold level, a special character has been detected, or loss of carrier from the data set occurs. The ACKI0, INTP0, and ID leads function the same as for the transmit buffer.

3.38 Leads RD0 through RD7 enter the special character recognition circuit from the serial-to-parallel converter on FC347. Also, internal registers AD4 and AD5 are in the special character recognition circuit. Internal register AD4 stores the special character while internal register AD5 erases the special character set in AD4. The purpose of the circuit is to generate an interrupt

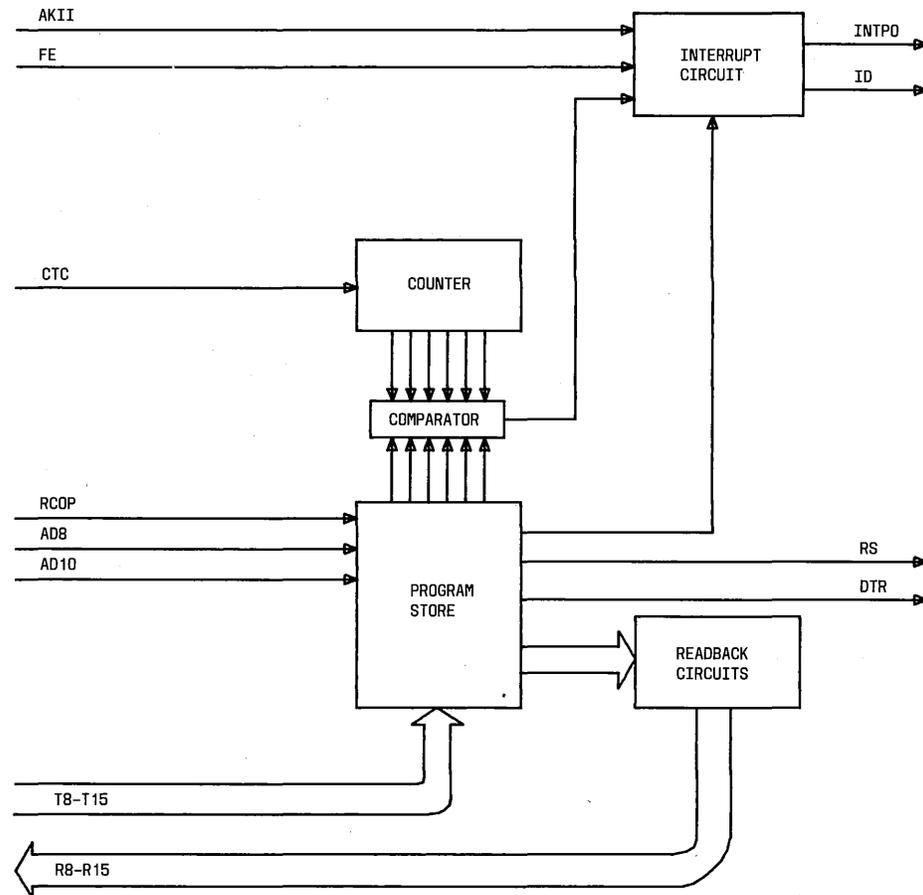


Fig. 13—Transmit Interrupt

signal when a programmed special character has been received from the data set. The read back circuits can transfer information from the program store to FC344.

J. Data Set Interface FC349

3.39 The data set EIA interface circuit pack (FC349) is shown functionally in Fig. 16. The EIA drivers and terminators connect the SLA to the EIA data set interface. Shown to the right of the EIA drivers and terminators are the EIA lead designations.

3.40 Data set control leads enter the FC349 circuit pack from the transmit interrupt circuit pack. The DTR command turns on data terminal ready to the data set. An RS command is a signal to the data set of the intent of the CPU to transmit data. The SLA begins transmitting the idle character

to the data set via lead SD. The data set responds to RS by enabling CTSX. SLA then transmits data to the data set via lead SD. Data is received from the data set via lead RD. While the SLA is receiving data from the data set, lead CAR is a "1" signifying that the data set is receiving a valid data signal from the line.

3.41 The logic interlock circuit monitors leads CTSX, RS, and FE. The logic interlock circuit maintains RS to the data set, even after RS is dropped from the CPU if the transmit buffer contains data. This circuit allows at least two idle characters to be transmitted after the buffer empties and then drops RS to the data set. The logic interlock also causes a 2-character delay in receiving CTSX from the data set.

3.42 The clock detectors monitor the data set transmit and receive clock leads. When

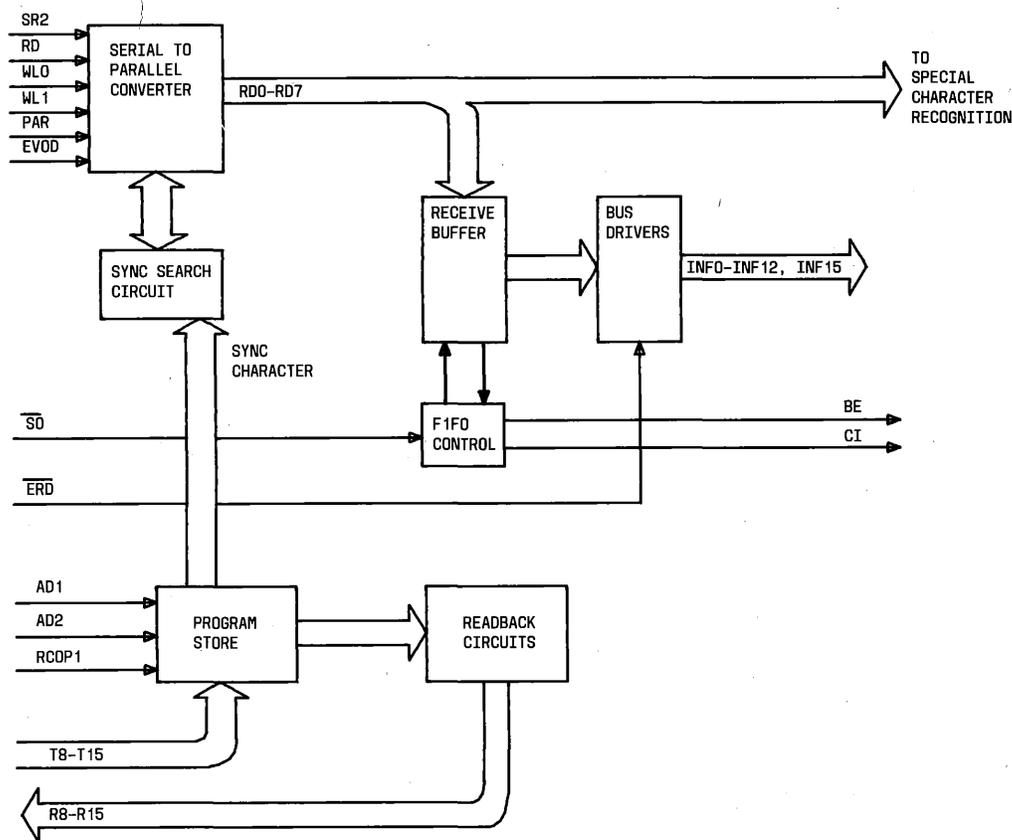


Fig. 14—Receiver

either clock stops, the clock detector presents this indication to gates R11 and R12 and can be read back to the CPU when internal register AD11 in the readback circuit is enabled. Internal register AD11 also monitors data set ready (DSR), carrier on (CO), clear-to-send (CS), and data set power from the data set. The readback circuits can transfer information from the program store to FC344.

3.43 The internal register AD12, represented by the program store, controls digital loopback. Under program control, data is looped back from the transmitter via lead SD, through the lower AND/OR gate combination, onto lead RD, and into the receiver. The transmitter timing is also looped back at this time from lead SCT, through the middle AND/OR gate combination onto lead SRI, and into the receiver.

3.44 The single step digital loopback mode is also possible. Using CP command with OP code

11 and internal register address AD12, the data set clock leads are disabled. Data can then be looped back in the manner described above, except that each OP code 11 command simulates one clock pulse. In this manner data can be manually stepped along through most of the SLA in order to locate trouble.

3.45 The +12T and -12T voltages from the data set are monitored in the readback circuits and an indication is sent to the CPU when these voltages change. However, when using DSUs, these voltages are not present at the interface. In order not to disrupt service, option Z must be installed by grounding lead 301 on the backplane of FC349.

K. Loopbacks

3.46 The loopbacks available in the SLA are shown in Fig. 17 and 18. All loopbacks, except for those in DAS and data set, are controlled by the CPU software. The 829 DAS loopbacks

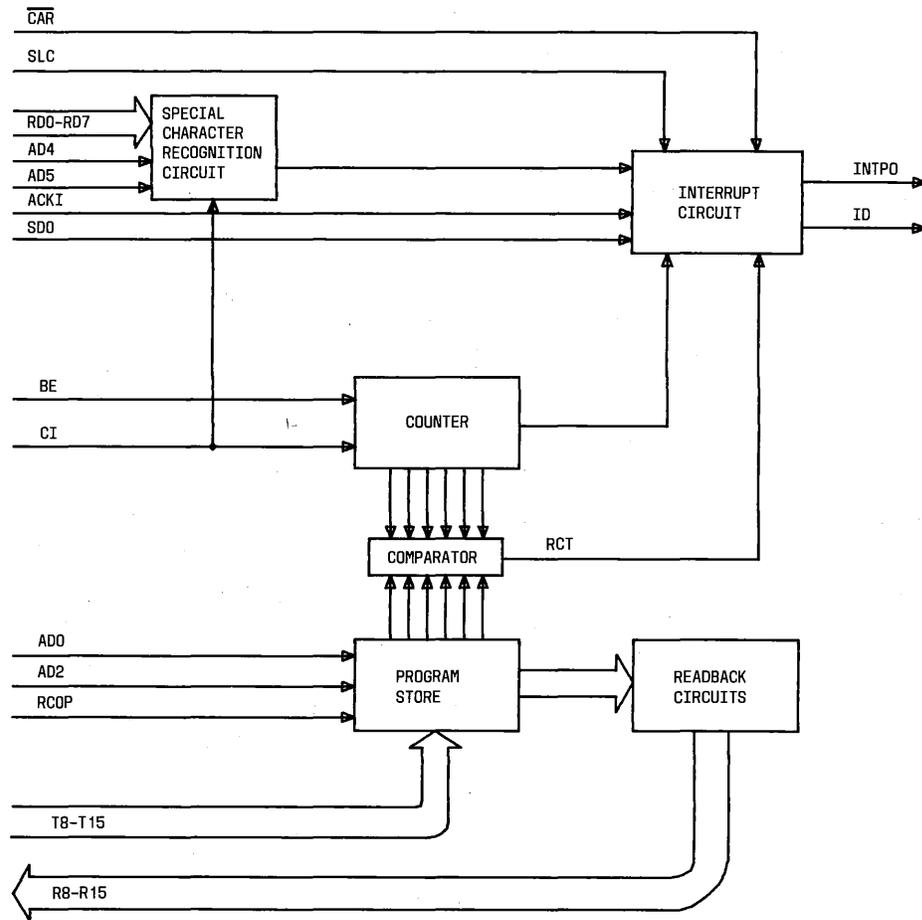


Fig. 15—Receive Interrupt

may be manually or remotely actuated by a 2713-Hz tone applied for 5 seconds on the receive pair. The loopback is released in the same manner. The data set loopback must be manually operated using the pushbuttons on the data set. The SCAM relay can be used to connect the data set transmit leads to receive leads for analog loopback.

L. SCAM Interface

3.47 The SCAM unit monitors a relay in each of the power units. These contacts close when the power unit senses an undervoltage condition or a power unit shutdown due to an overvoltage condition. Power unit failures are reported to the

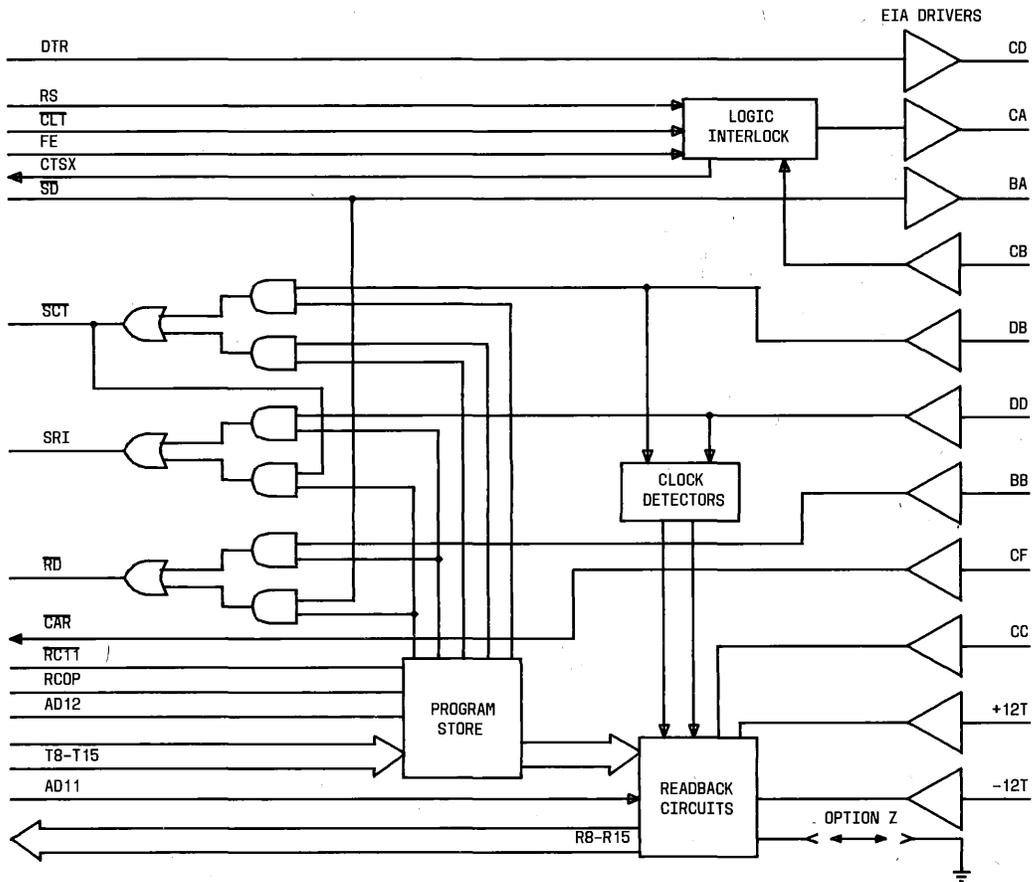


Fig. 16—Data Set Interface

CPU via the SCAM unit. The SCAM also connects a spare SLA, DBS, and DS or DSU combination when a failure occurs. There is one spare combination

for each type of DS or DSU used in the central office. The SCAM can also perform an analog loopback of the DS or DSU.

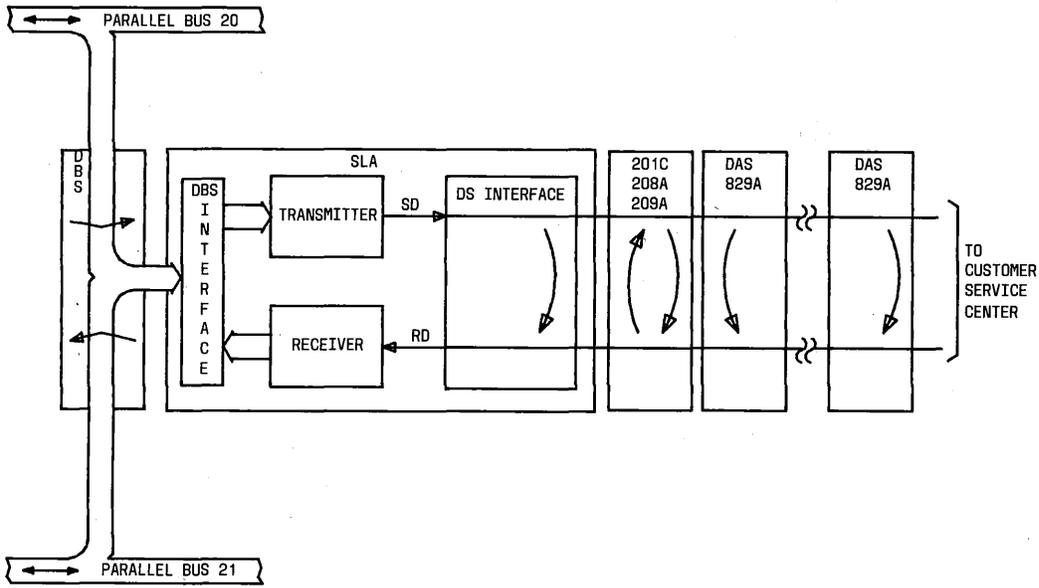


Fig. 17—Synchronous Port Loopbacks with Data Sets

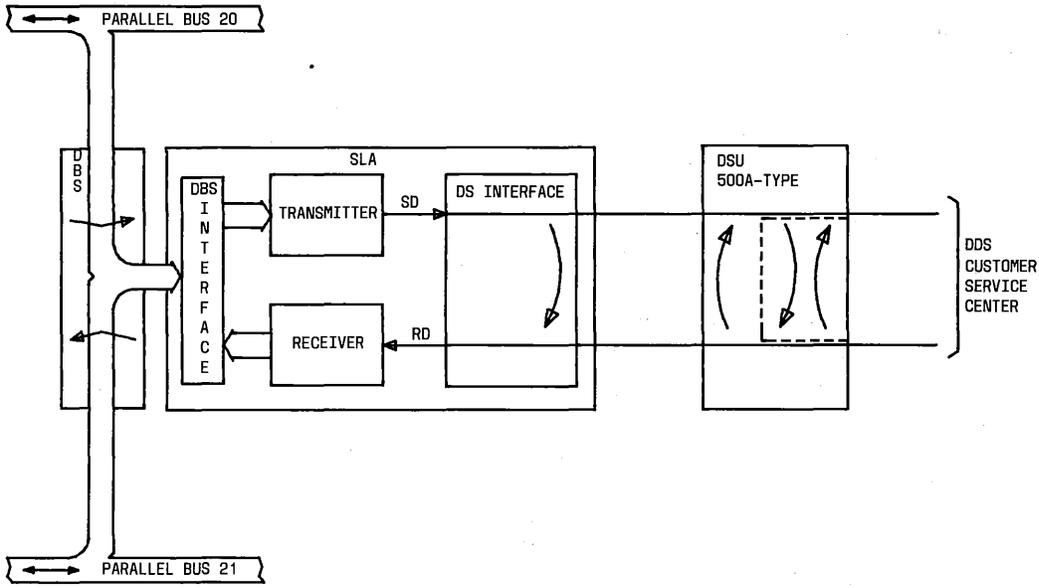


Fig. 18—Synchronous Port Loopbacks with Data Service Units

4. THEORY OF OPERATION

4.01 This part contains the theory of operation of the SLA. The information supplements the functional description contained in Part 3. The circuits described in order are:

- (a) FC343—SLA Address Decoder, I/O Logic for Bus Interface-Low, Command Address Decoder
- (b) FC344—I/O Logic for Bus Interface-High, Multiple Command Detector, Command Sampling Circuit
- (c) FC345—I/O Logic of Transmit Buffer
- (d) FC346—Transmit Interrupt Logic
- (e) FC347—Serial/Parallel Converter Logic, I/O Logic of Receive Buffer, Sync Search Circuit Logic
- (f) FC348—Special Character Recognition Logic, Receive Interrupt Logic
- (g) FC349—Logic Interlock Circuit, Digital Loopback Logic.

4.02 The circuits shown in the figures are not the exact schematics of the SLA, but have been simplified to facilitate explanation.

4.03 The SLA address logic is shown in Fig. 19. The 16-position switch is set at installation to the SLA address. The switch sets a "1" as ground and a "0" as positive. Gates DEC0 through DEC4 compare the address leads ADR00 through ADR50 with the SLA address set by the switch and enables lead ADB if they match. A matching maintenance address ("1" on lead ADR00) enables lead ADM. Parity is generated for the switch address by the parity generator. The switch address can be read back onto leads INF010 through INF050 when the SLA has been addressed, SST command has been sent, and address parity is ok.

4.04 The input/output logic for the bus interface low is shown in Fig. 20. Information on DBS leads INF000 through INF070 is in negative logic. If the SLA address and address parity are correct, gates IT0 through IT7 are enabled and pass data from leads INF000 through INF070 to

gates V0 through V7, the transmit buffer, and the command decoder.

4.05 When a valid maintenance address is detected, lead ADM is positive and enables gates V0 through V7 and data on leads T0 through T7 is passed through to the transfer register. A write data command with maintenance address enables the data to be written into the transfer register by putting a pulse on EWR. A command present (CP with OP=11) causes all "1s" to be written into the transfer register. Gates RV0 through RV7 invert the data so that all "1s" in the transfer register appear as all "0s" in inverted logic at the DBS.

4.06 An SST command with maintenance address enables lead E1 which enables gates ID0 through ID7. The data in the transfer register is now presented to the DBS.

4.07 Parity is generated from lead INF000 through INF070 by the parity generator and compared to the parity bit from the receive buffer (FP) in gate EG. Enabled receive data (ERD) lead transfers a "1" to lead INF130 if a parity error occurs. Gate PEL compares the generated parity bit to the parity bit on INFPL0 when a normal address (ADB) has been received. A "1" on lead PEL indicates correct parity. The parity generator output is placed on lead INFPL0 when enable parity out (lead EPO) is enabled.

4.08 The command address decoder (Fig. 21) enables one of sixteen registers (AD0 through AD15) to receive a CPU command. The inputs T3 through T6 are the internal register address and T7 must be "0" to enable the decoder. The flip-flop (FF) enables the command decode if a CP command is sent, parity is ok, and the normal address (ADB=1) is used. The decoder remains enabled until the SLA address (ADR00 through ADR50) is removed.

4.09 The input/output logic for the bus interface high is shown in Fig. 22. When the SLA address is detected, (ADB = 0) enables terminators T8 through T15 and inverts the negative logic on leads INF080 through INF150. Leads T8 through T15 go to internal registers and to gates M8 through M15. These gates are enabled by using the maintenance address, with no multiple command (MC) or parity error (MC = PER = 1). The data is inverted at these gates. Leads R8 through R15

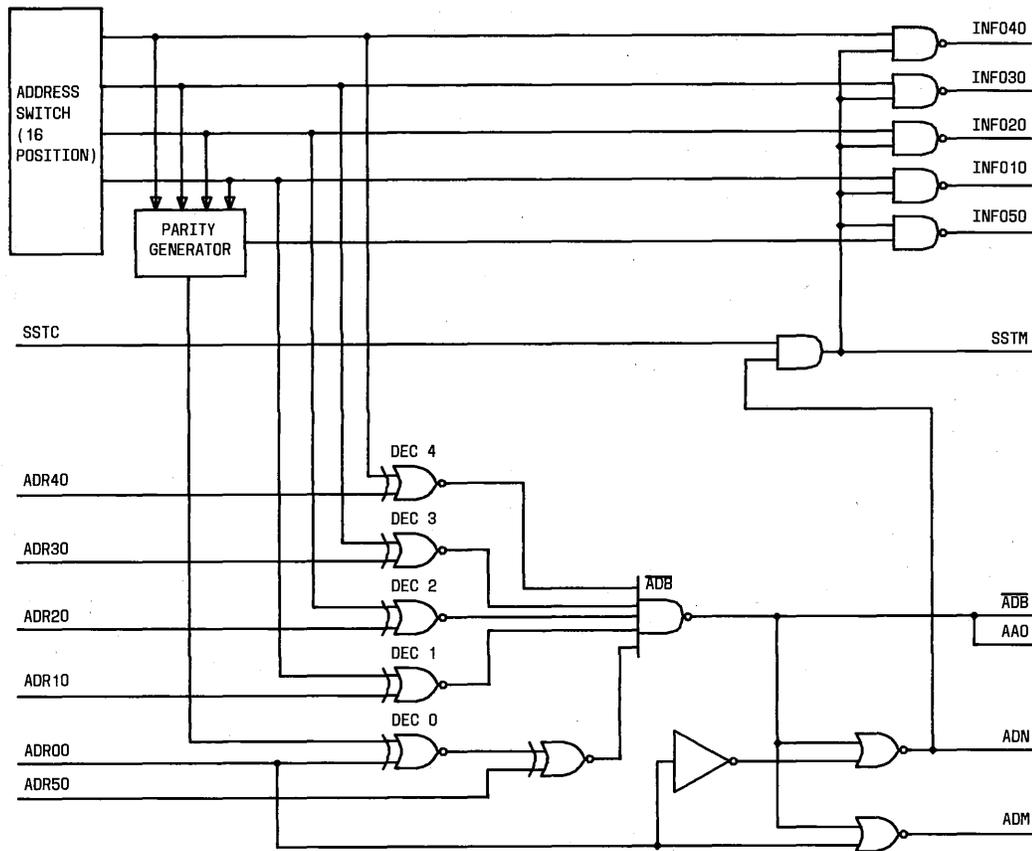


Fig. 19—SLA Address Circuit

from the readback circuits interface at the input to the transfer register. Data in either gates M8 through M15 or leads R8 through R15 can be transferred into the transfer register. If maintenance address is not used ($ADM = 0$), gates M8 through M15 are "off". Leads R8 through R15 are read into the transfer register when CP command and 11 OP-code are sent with ADB. When maintenance address is detected, gates M8 through M15 are enabled and entered into the transfer register if write data is "on" ($NEWRD = 1$). Data is inverted by gates RR8 through RR15 and presented to the bus drivers. When maintenance address is used ($AAO = 1$) with SST command, the bus drivers are enabled and present inverted data to DBS leads INF080 through INF150.

4.10 The parity generator generates parity for data received from leads INF080 through INF150. The parity comparator compares the generated parity bit with the parity bit received

(PEL) during a CP command or write data command. If they do not agree, an error lead is enabled.

4.11 The multiple command detector (Fig. 23) enables lead MC when one command is received. When more than one command is received, lead MC = 0.

4.12 All command leads are sampled with the leading edge of SYNC in D-type FFs. Figure 24 shows the timing sequence of the address, sync, commands, and error pulse. SYNC is returned to the CPU 250 nsec after the command is received. This eliminates errors due to short noise spikes on the line. MC lead must remain high to indicate no multiple command error. Parity error lead (PE) indicates an error received in the data.

4.13 The command sampling circuit is shown in Fig. 25. The command leads ACKI0, CP0, DP0, DR0, and SST0 are terminated and inverted

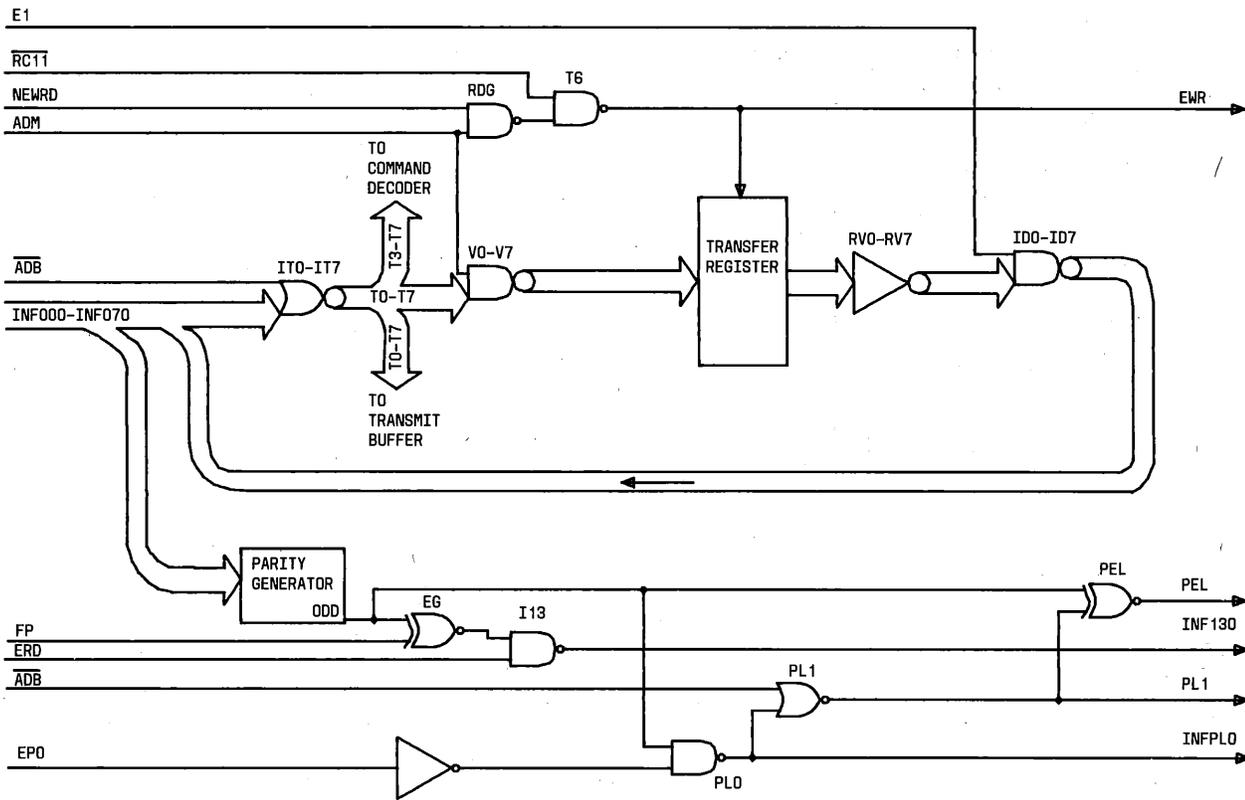


Fig. 20—Bus Interface Low

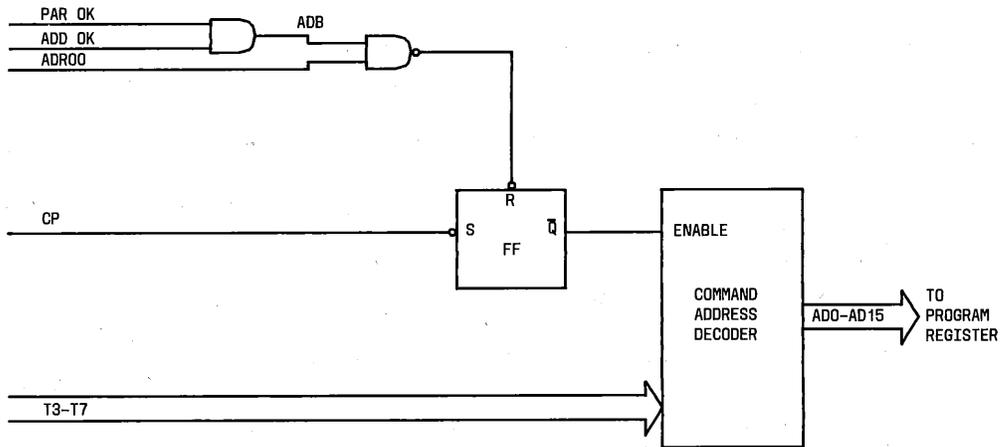


Fig. 21—Command Address Decoder

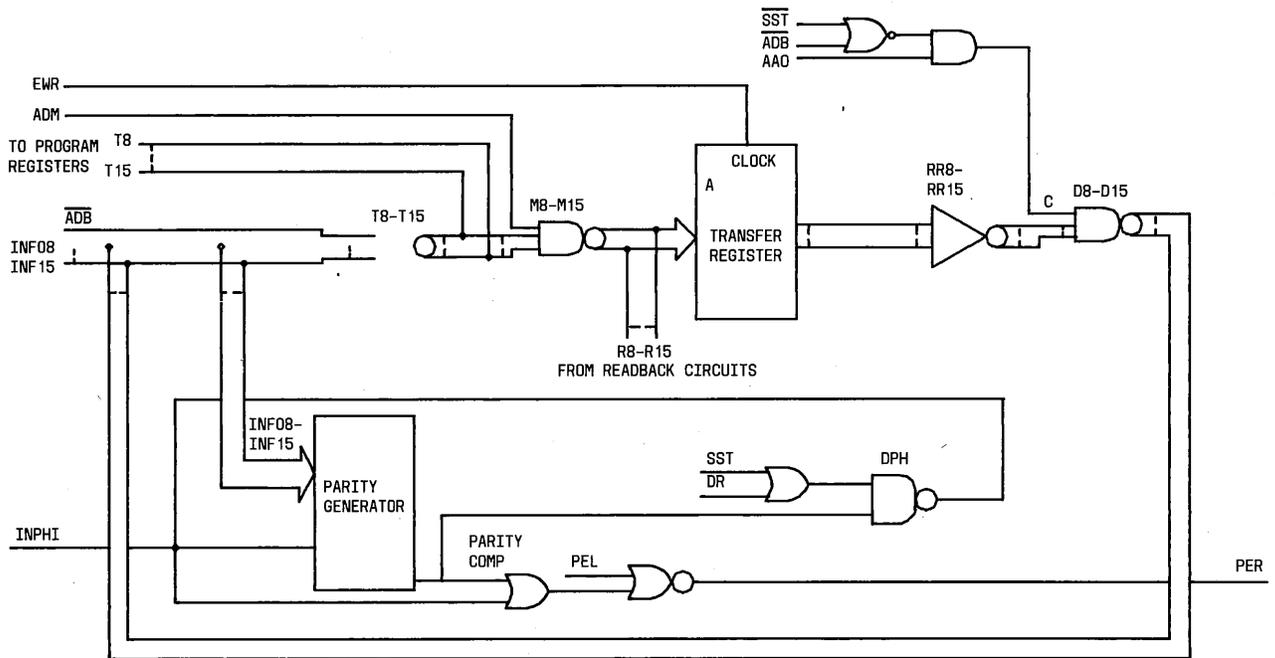


Fig. 22—Transfer Register

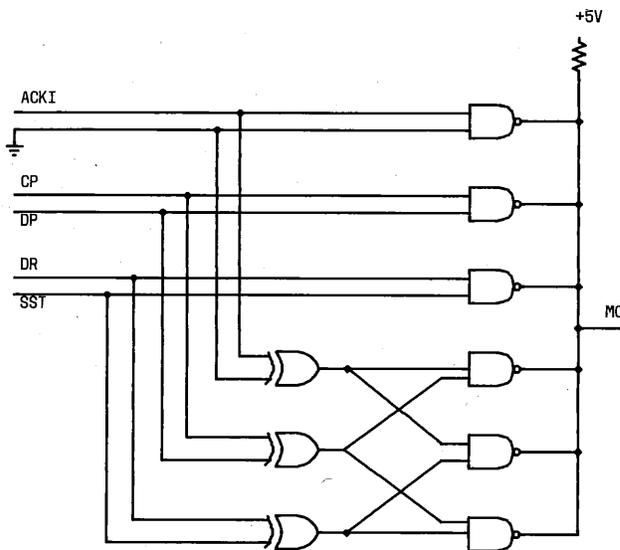


Fig. 23—Multiple Command Detector

by gates AKIR, CPR, DPR, DRP, and SSTR. The multiple command detector, sync generator, and set leads of the D-type FFs then receive the commands if the SLA address is correct. For

example, when a CP command is received CPR goes to the "1" state which removes the set conditions of the CPS FF. The output of CPG gate goes low if there is no parity error and normal address is received. A synchronizing pulse from the sync generator will toggle a "0" into the CPS flip-flop causing CPS lead to go low. When the CP command has expired CPR becomes a "0". Flip-flop CPS will go to a "1" since CPR is connected to the set lead. The other commands are treated in a similar manner. The rest of the logic simply distributes the OP code (leads INF01 and INF02) to the SLA registers via leads RC11, CLER0L, CREC, CLT, RCOP1 and RCOP2.

4.14 The transmit buffer logic is shown in Fig. 26. Parallel data enters the transmit buffer via leads T0 through T7 when the shift in (SI) lead has been pulsed. The buffer is a 64 word, 12 bit wide, FIFO register. Data is read out of the buffer when CTSX has been received from the data set and the shift-out lead has been pulsed. The shift-out pulse comes from the counter which monitors the data set transmit pulse. When the number of clock pulses equal the word character length, a shift-out pulse is generated by the counter. The word length is entered on leads T14 and T15

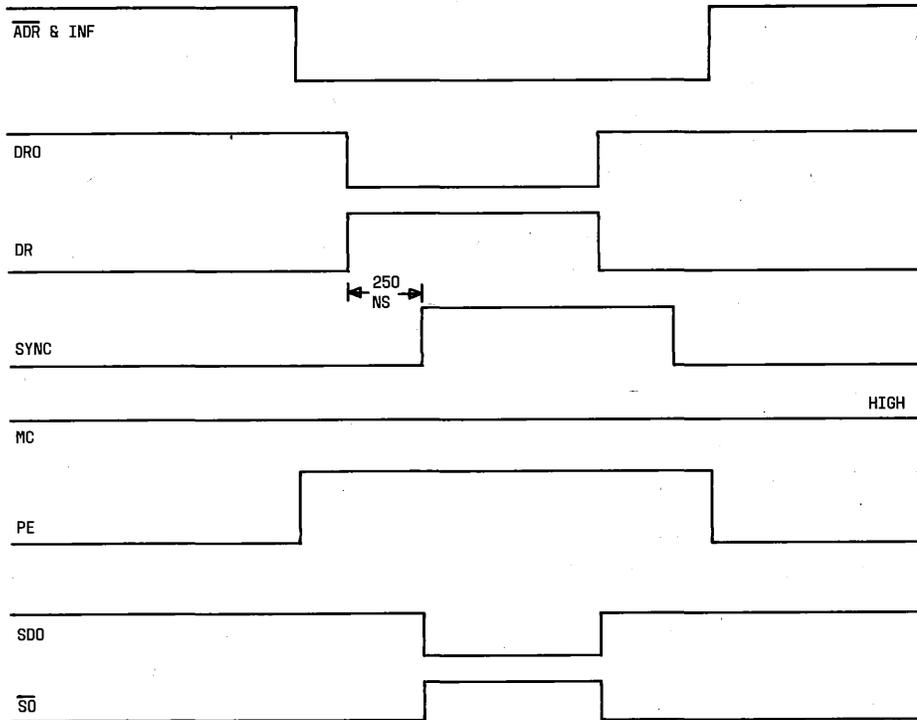


Fig. 24—Command Pulse Timing

when lead AD3 is enabled. The data from the FIFO enters the select gates which present the data to the parallel-to-serial converter. The select gates will transfer the idle character, from the idle character register, to the parallel-to-serial converter when the buffer empties. The idle character is written into the register via leads T8 through T15 when AD9 is enabled. Readout of idle character results when lead AD9 enables gates DR8 through DR15. The serial data is read out of the parallel-to-serial converter with the data set transmit pulses.

4.15 The parity insert circuit adds the parity bit and data is sent to the data set via lead SD. The parity error circuit generates parity for the data at the output of the buffer and compares it with the parity bit that was received from the FIFO. If the bits do not agree, a transmit hardware error indication is sent to the CPU on lead INF13 during the next SST command.

4.16 When the buffer empties, lead INF10 carries an underflow indication to the CPU. SST command enables readout of gates I10, I13, and I15 onto leads INF10, INF13, and INF15. Lead

AD3 enables gates DM12 through DM15 which causes read out of character word length and parity (even, odd, or no parity).

4.17 The transmit interrupt circuit is shown in Fig. 27. It generates an interrupt signal when the transmit buffer has read out a specified number of characters or if it underflows. The threshold register holds a 6-bit number, written in from leads T8 through T13, which specifies the interrupt level. The number is written in when lead AD10 and write command (RCOP) leads are enabled. It can be read out through gates R8 and R13 when lead AD10 is enabled and can be cleared by a pulse on CLEROL.

4.18 The counter accumulates the number of characters actually read out of the transmit buffer via lead CTC. The comparator enables the INTR flip-flop and clears the counter when the counter level equals or exceeds the threshold register level. Note that the buffer empty lead (FE) can also cause the counter to clear through gate RES. This ensures that the counter is in the "0" state when the buffer contains "0" characters. Gate INT will be enabled if INTR flip-flop and

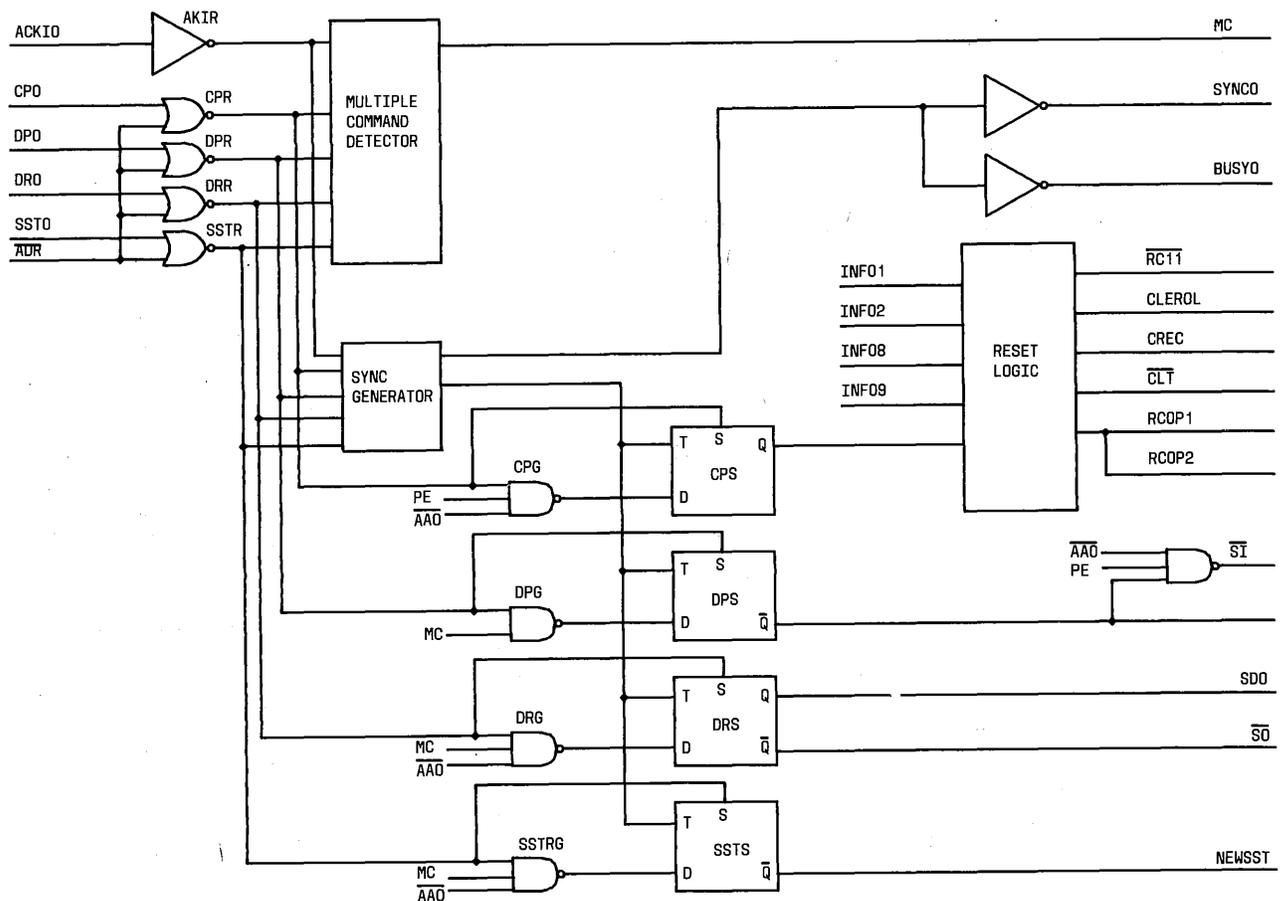


Fig. 25—Command Sampling Circuit

interrupt enable lead 15 from the command register are "on". This causes an interrupt to be sent to the CPU via lead INTPO. The transmit buffer underflow (UFLO) lead will also enable the INTR flip-flop which in turn enables the INTPO lead.

4.19 The command register (internal register addressed by AD8) receives commands via leads T12 through T15. Lead T12 enables request to send; lead T13 enables data terminal ready; lead T14 enables request for service; and lead T15 enables interrupt. This data is written in when lead AD8 is enabled. It can be read out via gates RC12 through RC15 when lead AD8 is enabled. Request-for-service (lead T14) and new-status-request (NEWSST) clear the INTR flip-flop and hence lead INTPO.

4.20 The serial-to-parallel converter logic is shown in Fig. 28. Serial data from the data set

enters the serial-to-parallel converter via lead RD. Data is clocked in using data set receive clock via lead SRC. Data leaves the converter in parallel form with a character length of 5, 6, 7, or 8 bits and goes to the special character circuit, sync search circuit, parity check, and receive buffer. The character length store (WLS) determines the character length via leads WL0 and WL1 and parity information via lead PAR. The WLS enables gates RD4 through RD7 depending upon character length.

4.21 The character clock and receive buffer are shown in Fig. 29. The character clock is produced by dividing the bit clock (lead SCR) by 5, 6, 7, or 8. Counter CTR produces a carry bit at count 15. Inputs WL0 and WL1 load the counter to a count of 8, 9, 10, or 11, during the next clock cycle after a carry has appeared on lead 15, for 8-, 7-, 6-, or 5-bit character lengths, respectively.

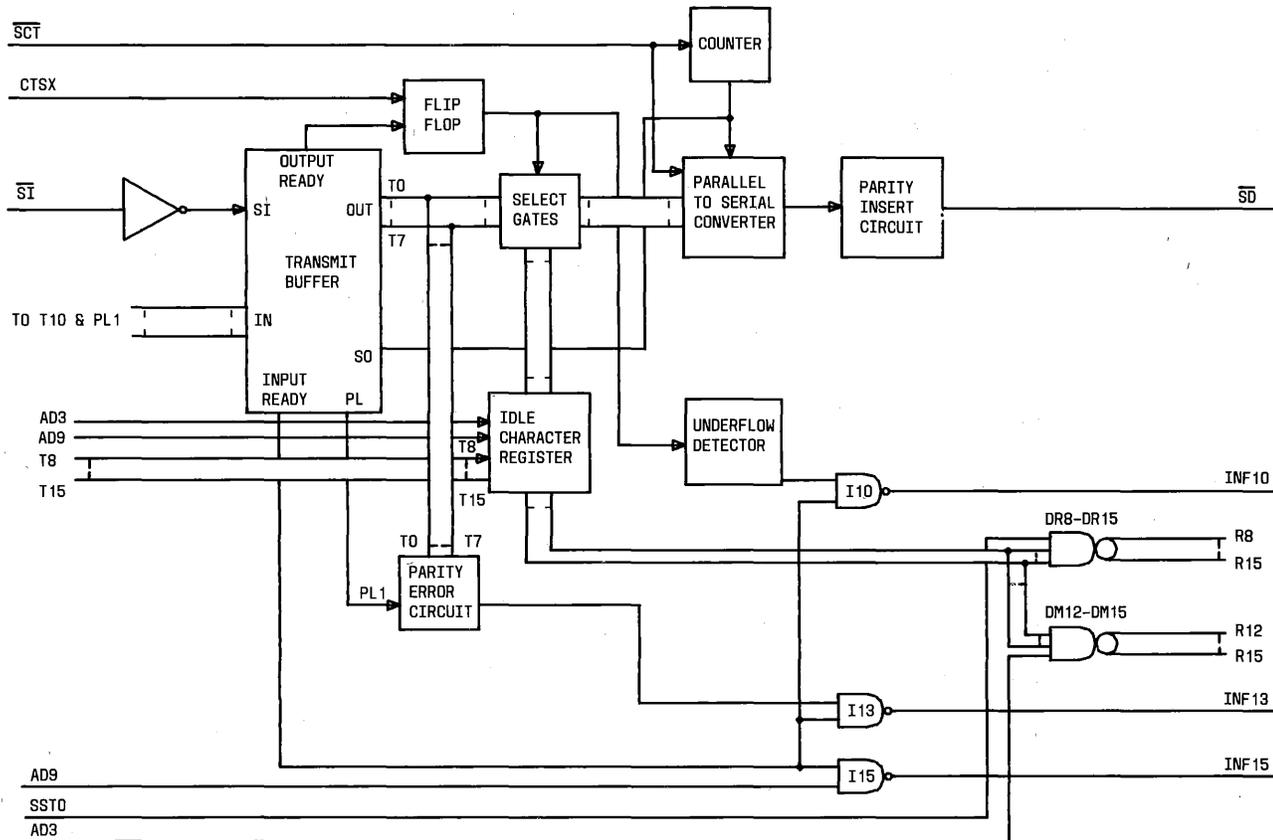


Fig. 26—Input/Output Logic of Transmit Buffer

Carry lead 15 also shifts data RD0 through RD7 into the receive buffer. The counter is also loaded when a synchronization character match is found ($MCH = 1$). When shift-out (SO) lead is pulsed from the command decoder, a new character is presented at the output of the buffer. The read gates are enabled by lead ERD.

4.22 The sync character store (Fig. 30) receives the synchronization character via leads T8 through T15 when AD1 is low and a positive pulse is on lead RCOP. The output goes to the sync match gates (M0 through M7) and the read-back circuits. Data from the serial-to-parallel converter is matched with the synchronization character at the sync match gates. If a synchronization character is detected, output MCH is a "1". The parity check circuit checks the incoming data for parity which is determined by lead EVOD. Lead EVOD is a "1" for even parity and a "0" for odd parity. A "1" on lead EVOUT indicates a parity error on the incoming data.

4.23 The special character recognition circuit is shown in Fig. 31. The heart of the special character recognition circuit is a 256-word random access memory (RAM) with each word 1-bit long. The special characters are written in when RCOP is enabled and leads AD4 or AD5 are enabled (made a "0"). An address, corresponding to the special character desired, is put on leads T8 through T15 and transferred to the input of the RAM which is loaded with a 1 when lead AD4 is enabled. A "0" is written into the RAM location designated by the special character address when lead AD5 is enabled. All 256 possible bit combinations must be defined as "1" (special character) or "0" (not special character). When data is being received from the data set, it is presented to the special character recognition circuit via leads RD0 through RD7 from the serial-to-parallel converter. When RCOP is not enabled, a "0" is read out of the RAM when a special character appears on leads RD0 through RD7. Gate SCI enables the lead to the interrupt circuit when a special character is

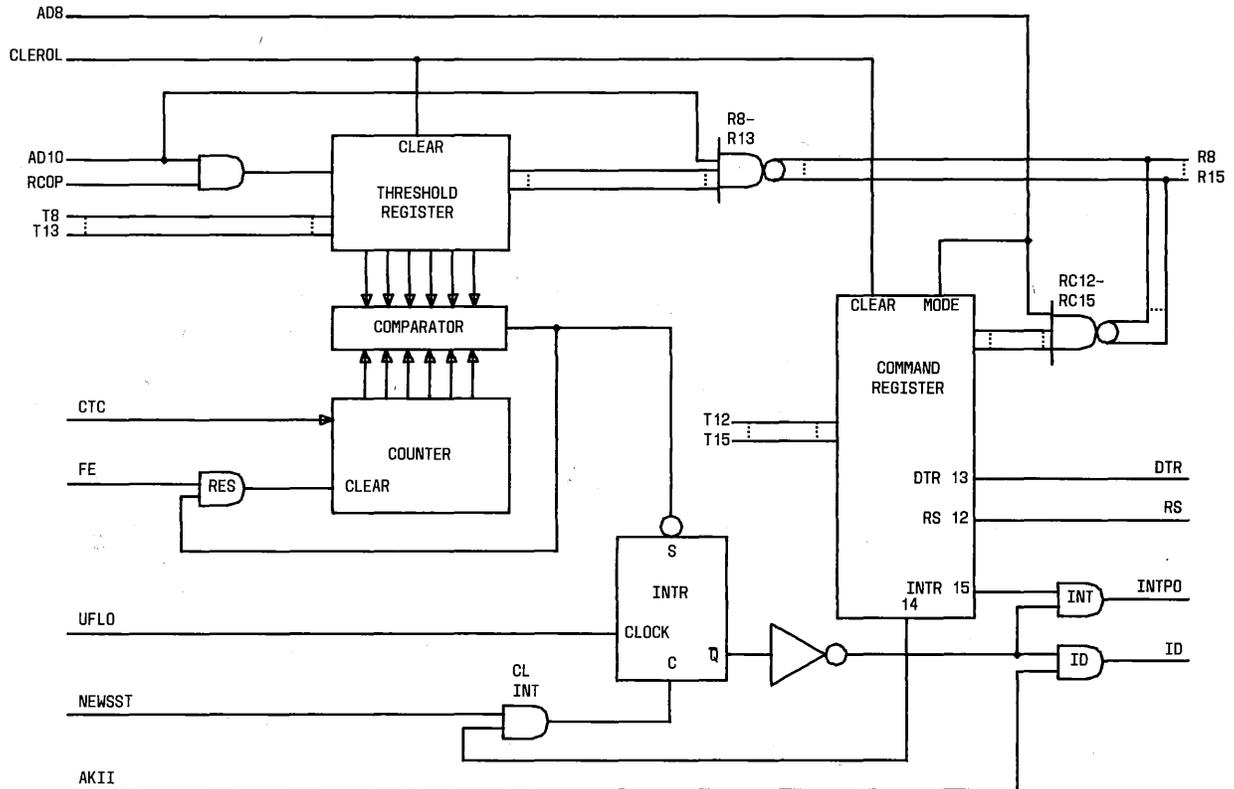


Fig. 27—Transmit Interrupt Circuit

present, neither AD4 nor AD5 are enabled, and a pulse appears on the counter lead (CI).

4.24 The receive interrupt circuit (Fig. 32) generates an interrupt signal when the receive buffer has received a specified number of characters, if loss of carrier from the data set occurs, or if a special character has been detected. The threshold register holds a 6-bit binary number which specifies the interrupt level. The number is written in when leads AD2 and write command (RCOP1) are enabled. It can be read out through gates R8 through R15 when lead AD2 is enabled. The register is preset to a count of 63 by a pulse on the CLEROL lead.

4.25 The counter accumulates the number of characters actually written into the receive buffer via lead CI. The comparator enables the INTR flip-flop and in turn clears the counter when the counter equals or exceeds the threshold register level. Note that the BE lead can also cause the counter to clear. With INTR flip-flop enabled, an interrupt signal is sent to the CPU if the interrupt

enable lead from the command register is "on". Special character detected and loss of carrier can also enable the INTR flip-flop.

4.26 The command register receives commands via leads T12, T13, and T15. Lead T12 enables special character interrupt; lead T13 enables clear interrupt; and lead T15 enables the interrupt output for all interrupt conditions. This data is written in when lead AD0 is enabled and read out via gates E13, Q13, and I13. The interrupt FF can be cleared when CREC (clear receive) is enabled, or SDO is enabled.

4.27 The logic interlock circuit is shown in Fig. 33. When request-to-send ($RS = 1$) is enabled, transmit buffer is not empty ($FE = 1$), and clear transmit buffer is "off" ($CLT = 1$), interface lead CA will turn "on" and data can be transmitted from the buffer to the data set. With each SPARE 2 pulse, one character is transmitted. RS can be dropped by the CPU but lead CA will be unaffected until the transmit buffer goes empty ($FE = 0$) and two SPARE 2 pulses have occurred.

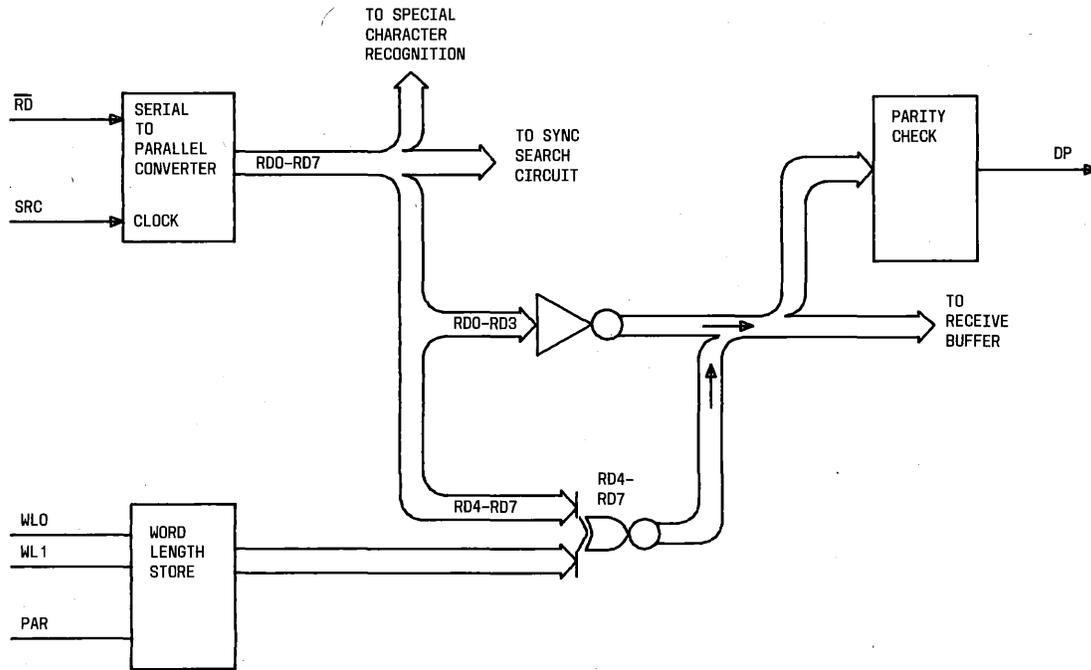


Fig. 28—Serial-to-Parallel Converter and Word Length Circuits

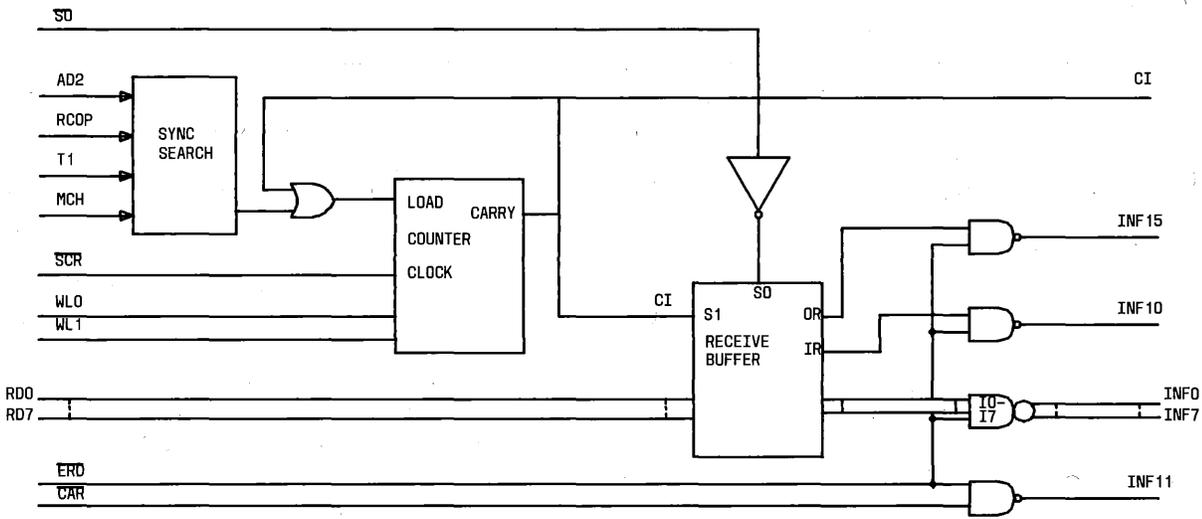


Fig. 29—Character Clock and Receive Buffer Logic

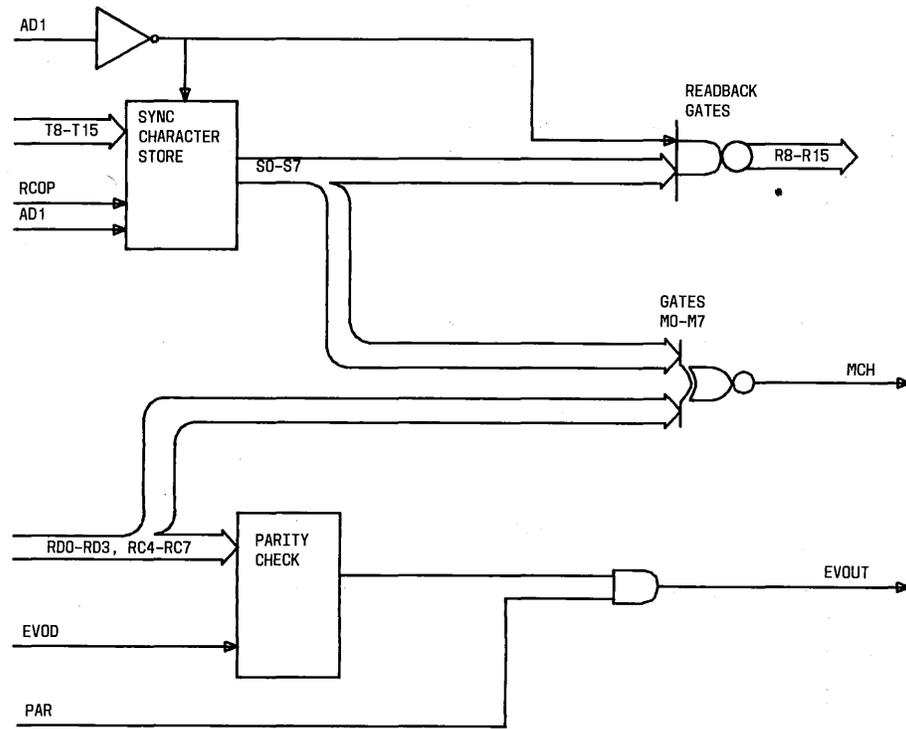


Fig. 30—Sync Search and Parity Check Circuits

The idle character is transmitted during these two pulses to ensure that the buffer is empty. Lead CA will then go low. Clear-to-send from the data

set (lead CB) also is delayed by two characters (two SPARE 2 pulses) before it reaches the CPU.

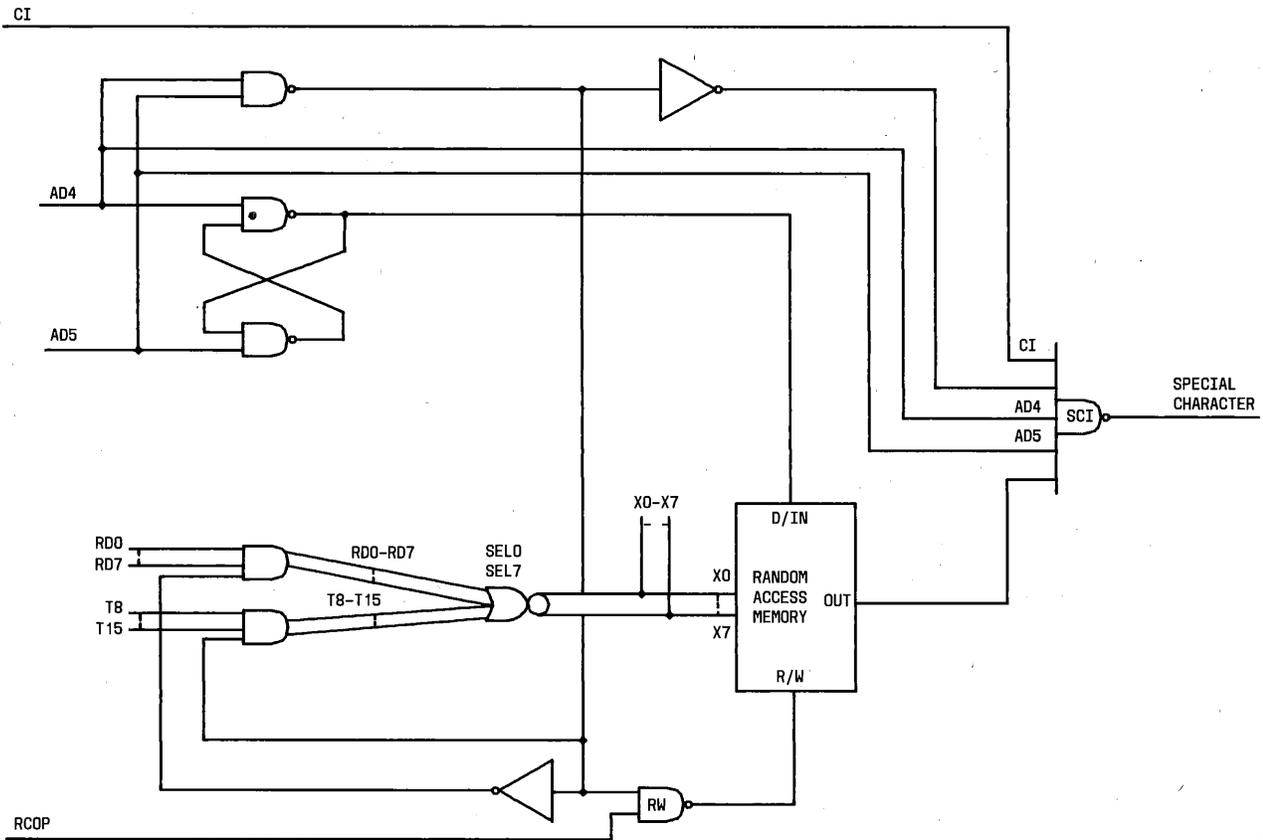


Fig. 31—Special Character Recognition Circuit

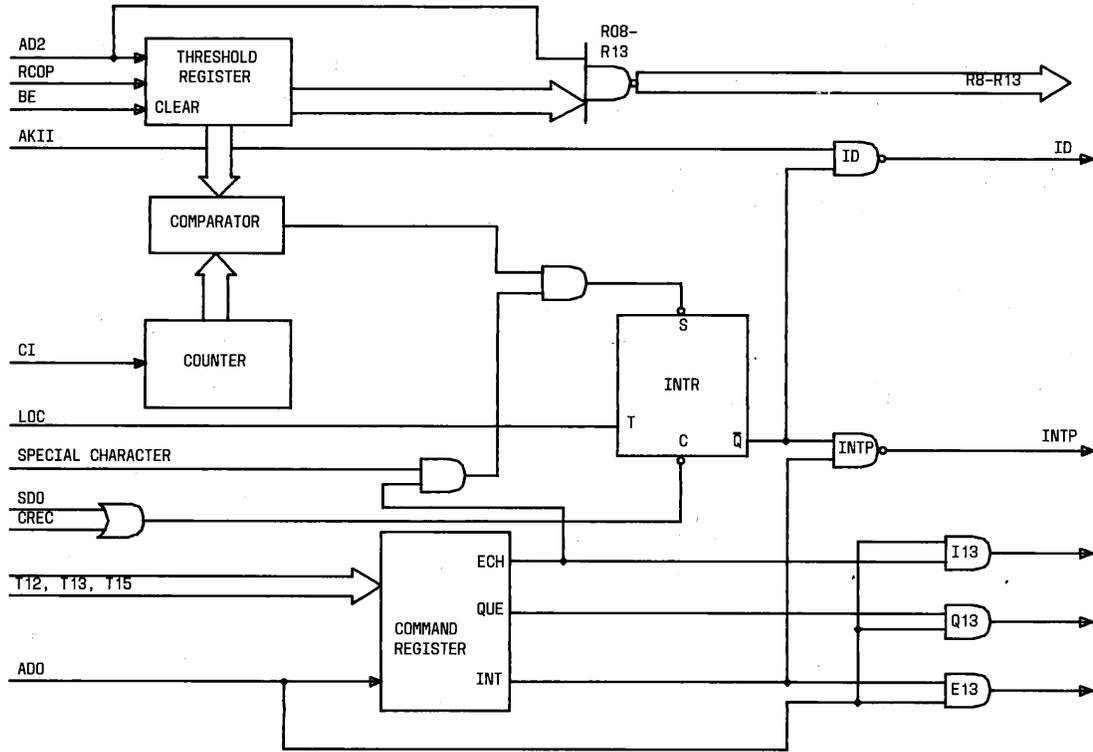


Fig. 32—Receive Interrupt

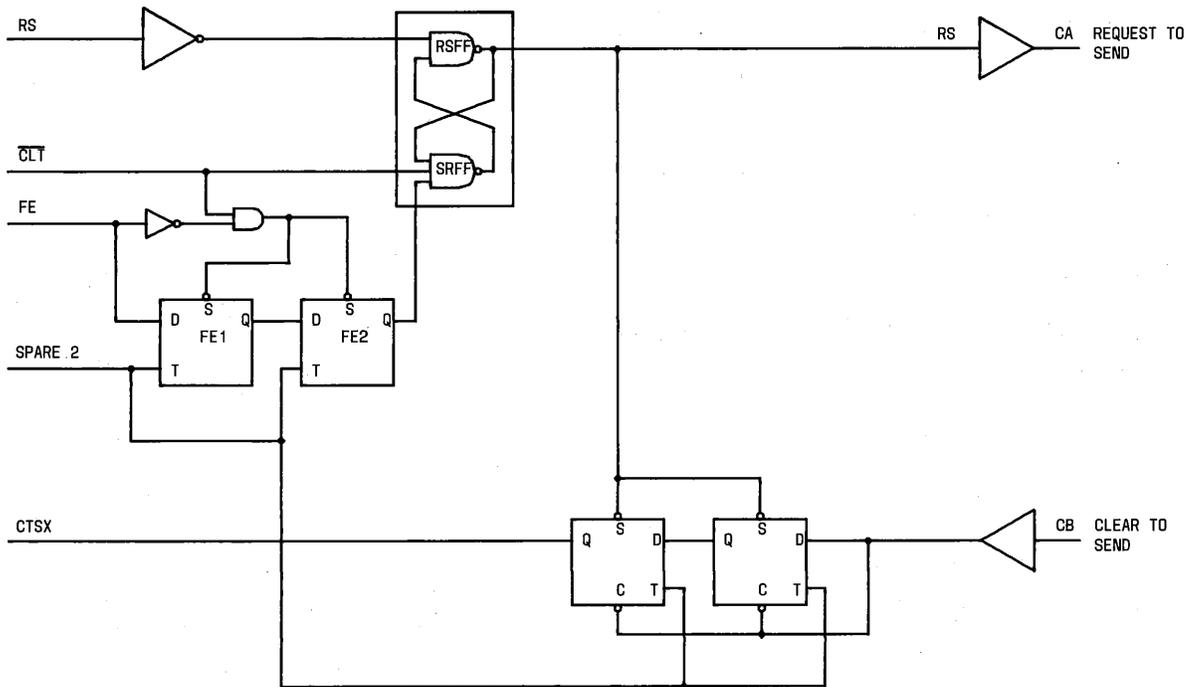


Fig. 33—Logic Interlock

4.28 The digital loopback circuit is shown in Fig. 34. Flip-flop DLB and DSS control digital loopback and single-step mode, respectively. A "0" on leads T14 and T15 result in normal operation. A "1" on lead T15 causes SD (send data lead) to be looped back on to RD (receive data lead) via gate SRD and SCT (transmitter timing lead) to be looped back onto SRC (receive timing lead) via

gate SRC. A "1" on lead T14 disconnects transmitter timing (DB) from SCT and enables the output of gate ESS onto SCT via gate STC. Gate ESS is enabled when lead T13 is "1", RC11 is "0", and AD12 is "0". When flip-flop DSS or DLB are enabled, SD is disconnected from lead BA via gate SDD.

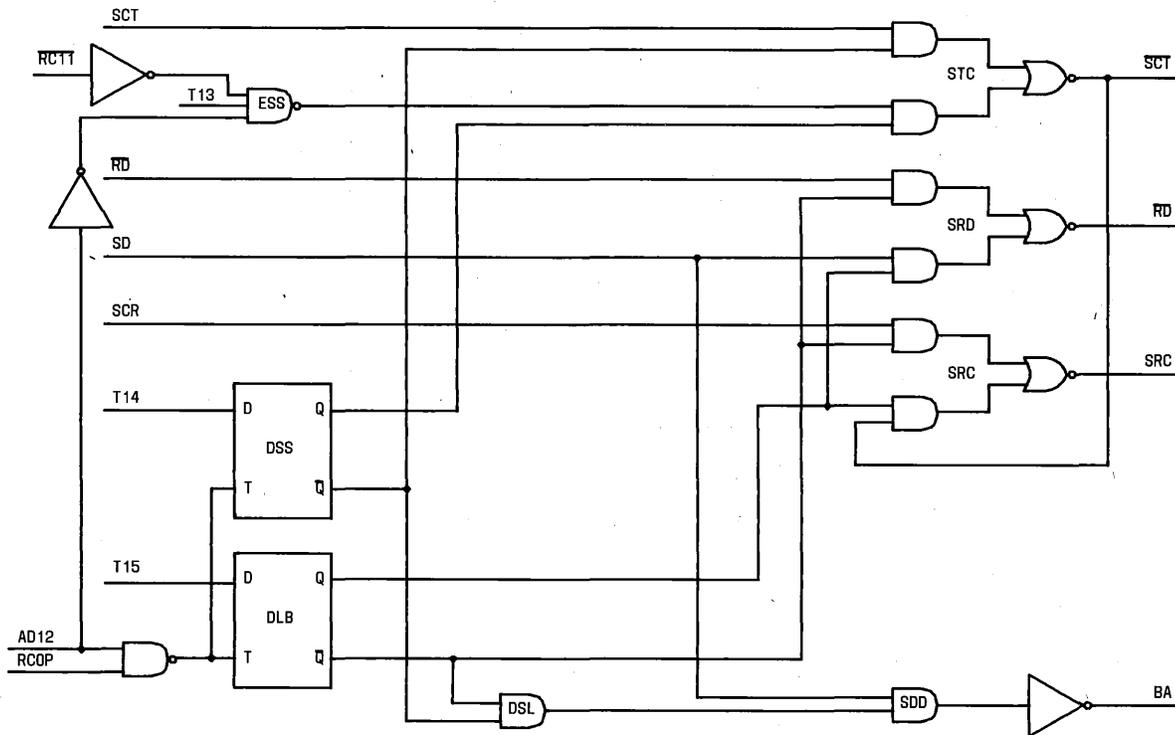


Fig. 34—Digital Loopback

5. REFERENCES

5.01 The following documents contain information pertaining to the SLA.

SD 73125-01	Transaction Network System— Power Distribution Circuit
SD 73124-01	Transaction Network System— Application Schematic Diagram

NUMBER	TITLE	SECTION	TITLE
CD & SD	Transaction Network—Synchronous Line Adapter Unit	230-100-440	Transaction Network—Duplex Bus Selector— Description
SD 73118-01	Transaction Network—Synchronous Line Adapter Circuit	230-100-001	Transaction Network—Overall System—Description
SD 73119-01	Transaction Network—Synchronous Line Adapter Frame	590-102-133	42A1-Type Data Mounting— Identification

SECTION	TITLE	CP	Command Present
590-102-136	46-Type Data Mounting— Identification	CPU	Central Processor Unit
590-102-139	48A-Type Data Mounting— Identification	CREC	Clear Receive Buffer
592-027-100	Data Set 208A-Type—Transmitter Receiver—Description	CSC	Customer Service Center
592-029-100	Data Set 201C-Type—Transmitter Receiver—Description	CTSX	Clear-to-Send
592-032-100	Data Set 209A-Type—Transmitter Receiver—Description	DAS	Data Auxiliary Set
595-200-100	Digital Data System—500A-Type DSU—Description and Operation	DBS	Duplex Bus Selector
598-082-100	Data Auxiliary Set 829-Type-Voice Band Private Line Channels— Description	DDS	Digital Data System
		DLA	Dial Line Adapter
		DLB	Digital Loopback
		DP	Data Present
		DR	Data Request
		DS	Data Set
		DSS	Single Step Mode
		DSU	Data Service Unit
		DTR	Data Terminal Ready
		EIA	Electronic Industries Association
		ER	Error Lead
		ERD	Enable Receive Data
		EVOD	Even or Odd Parity
		EVOUT	Incoming Parity Error
		FE	Transmit Buffer Empty
		FIFO	First-in/First-out
		ID	Interrupt Identification
		INF	Information Lead
		INFPH0	Parity High
		INFPL0	Parity Low

6. GLOSSARY OF ABBREVIATIONS/ACRONYMS

Note: Only the basic abbreviations and acronyms are listed in this part; lead and logic level suffixes are omitted as are logic negation symbols.

ACKI	Acknowledge Interrupt
AD	Internal Register Address
ADB	Address Detected
ADM	Maintenance Address
ADR	Address Leads
ALA	Asynchronous Line Adapter
BE	Receive Buffer Empty
BUSY	Busy Lead
CAR	Carrier
CI	Character Count
CLEROL	Clear All
CLT	Clear Transmit Buffer

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INTP	Interrupt	RS	Request-to-Send
I/O	Input/Output	SCAM	Switch Control and Monitor
Kbps	Kilobits per second	SCT	Transmit Clock
MC	Multiple Command	SD	Send Data
MCH	Sync Character Match	SI	Shift In
MS	Message Switch	SLA	Synchronous Line Adapter
NEWRD	DP (sampled)	SPARE 2	Clock Pulse
NEWSST	SST (sampled)	SPCH	Sub Parallel Channel
OP	Operation Code	SST	Sense Status
PER	Parity Error	SO	Shift Out
PU	Power Unit	SY	Sync
PSK	Phase Shift Keyed	SYNC	Sync Lead
RAM	Random Access Memory	TTL	Transistor-Transistor Logic
RCOP	Write Register	UFLO	Buffer Underflow
RC11	Read Register	WLS	Word Length Store
RD	Receive Data	WL0, WL1	Character Length