

**PDSP UNIVERSAL DATA LINK CONTROLLER
AND DATA LINK INTERFACE
SOFTWARE DESCRIPTION AND DIAGNOSTIC PROCEDURES
2-WIRE NO. 1 ELECTRONIC SWITCHING SYSTEM**

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NOTICE

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1.03 The universal data link controller (UDLC) provides the No. 1 Electronic Switching System (ESS) PDSP with a general purpose data communications channel capable of handling 16 DLI units independent of transmission protocol (Fig. 1). The UDLC accepts data and instructions from the PDSP and issues a sequence of commands to the appropriately selected DLI. The DLI acts as an interface between the data set operating at one end of a data link and the UDLC at the other end of the link.

1.04 When a data transaction is to take place, the PDSP first programs the UDLC to gain access to the required DLI and follows that instruction with the command defining the operation which is to be performed. The latter command triggers the microcontroller, which uses read only memory (ROM), containing DLI instruction sets required to execute the command.

1.05 For the enhanced private switched communications service (EPSCS) application, UDLC recovery has priority over the processor interface unit (PIU) recovery because, given a choice, it is preferable to lose communications with one switching machine while maintaining the data switching point in operation.

1.06 Abbreviations used in this section are:

ATP	All Tests Passed
CP	Command Present
DBS	Duplex Bus Selector
DLI	Data Link Interface
DP	Data Present
DR	Data Request

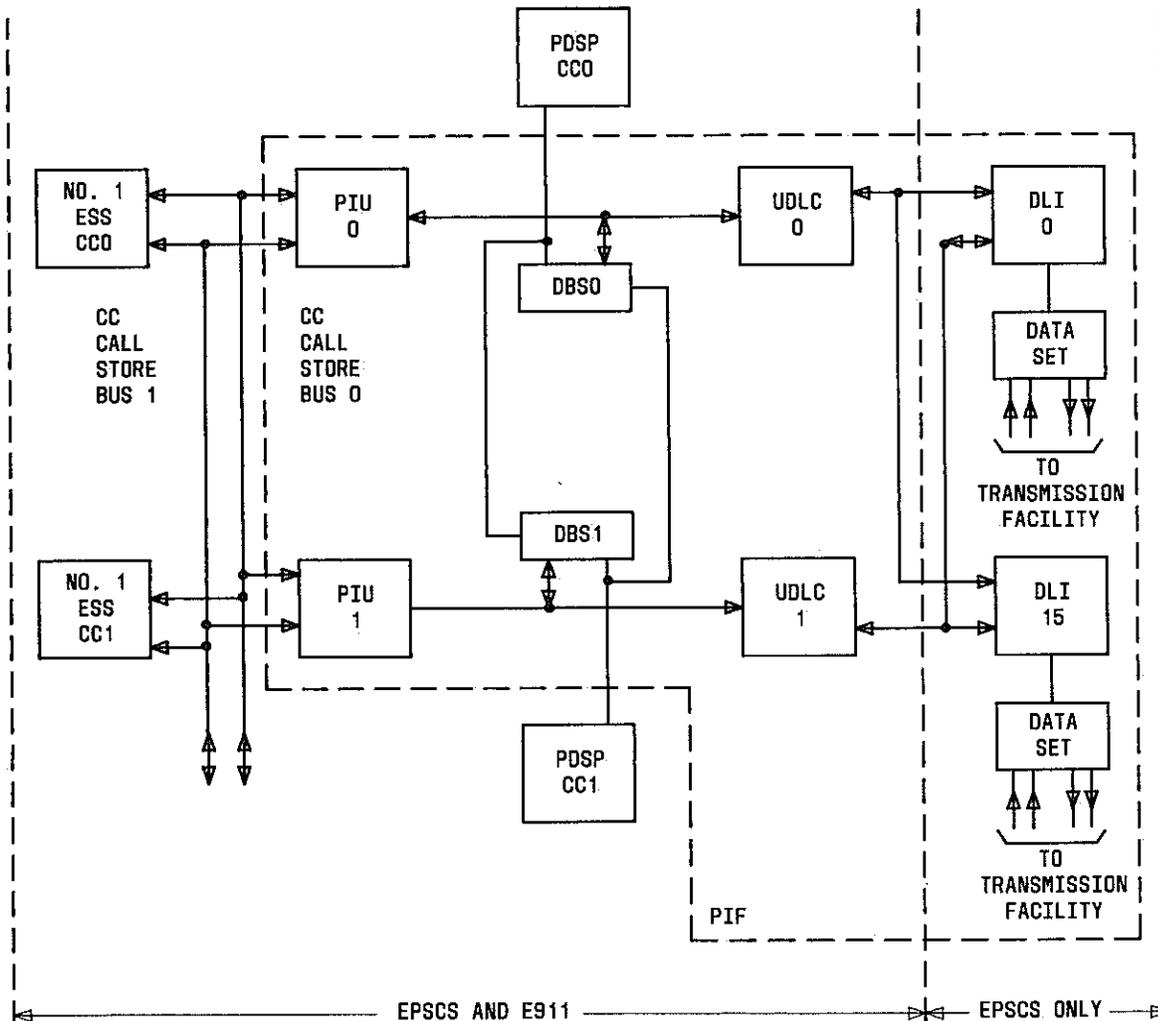


Fig. 1—No. 1 ESS-PDSP Configuration

DVCB	Device Control Block
EIA	Electronics Industry Association
EPSCS	Enhanced Private Switched Communications Service
ESS	Electronic Switching System
E911	Expanded 911 System
FIFO	First-In-First-Out
LCR	Line Control Register
PCH	Parallel Channel
PDSP	Peripheral Data Storage Processor
PIU	Processor Interface Unit
ROM	Read Only Memory
SC	Standby Controller
SPCH	Subparallel Channel
SST	Send Status
TLM	Trouble Locating Manual
UDLC	Universal Data Link Controller
USART	Universal Synchronous/Asynchronous Receiver and Transmitter

2. UDLC STRUCTURE

2.01 The UDLC is a ROM sequenced controller that connects to the PDSP via its subparallel channel. It receives command instructions and data from the PDSP and forwards the data along with the appropriate control to the designated data link. The UDLC interfaces with the PDSP subparallel channel via the duplex bus selector (DBS) which contains both cable drivers and receivers in addition to control circuits that respond to specific types of commands.

2.02 Control and data communications between the UDLC and the individual DLI units are accomplished over a dc bus complex. The bus structure can be divided into three subbuses: the

enable bus, the command and reply bus, and a multiplexed bidirectional data access bus.

A. Address Decoder

2.03 The address decoder circuit requires two unique addresses to identify data and commands intended specifically for the UDLC versus data transactions intended for a DLI unit.

B. Input Control Leads

2.04 Five control leads are employed to transmit commands from the PDSP to either the UDLC or a data link using a one out of five code. These leads are standard PDSP commands: command present (CP), data present (DP), data request (DR), and send status (SST). The definitions are as follows:

- (1) CP—When CP is set to one, it indicates to the selected device that a command is present on the information leads. The information leads contain a 15-bit coded command. Only the device with the proper address should respond to the command.
- (2) DP—When DP is set to one, it indicates to the selected device that data is present on the information leads.
- (3) DR—When DR is set to one, the selected device is requested to gate data onto the information leads.
- (4) SST—When SST is set to one, the selected device is requested to gate the contents of its status register onto the high ten bus information leads as well as its address code onto the low six bus information leads. An SST command must be accepted and properly responded to by the addressed device regardless of its busy status.

C. Response Leads

2.05 Three response leads are provided back to the PDSP. These leads are used to transmit information that is developing within the peripheral device selected. The leads are synchronization

(SYNC), busy (BUSY), and error (ER) and are defined as follows:

- (1) SYNC—After a control signal has been issued by the PDSP and properly received by the device, the device sets SYNC to one indicating that the control signal has been understood, all device check circuits have settled, and information has been gated onto or from the information leads. In case the device is not ready, the device should hold SYNC to zero until it has responded properly.
- (2) BUSY—The busy signal is used by the selected device to inform the processor of its readiness to respond immediately to a subsequent DP or DR control signal during block data transfer. The BUSY lead is asserted at the same time as SYNC.
- (3) ER—The error condition is set on or before the time that SYNC is set whenever the selected device has discovered an abnormal condition.

D. Select Register and Select Decoders

2.06 The select register and select decoders provide access to other internal registers, enable maintenance tests, stimulate errors, and select the set of ROMs.

E. Line Control Circuit

2.07 The line control circuit selects the DLI and provides a field from which DLI commands are generated. The line control circuit consists of a line control register (LCR) and a DLI enable decoder driven by the LCR. After programming the select register for access, the PDSP can write into the LCR by using a UDLC DP command. The line control register is composed of the enable address and the command field. The enable register is decoded by the DLI enable decoder and identifies which of 16 possible data links the enable decoder outputs is to be accessed. This circuit is duplicated and matched to prevent inadvertently enabling the incorrect DLI. The command field consists of four fixed command bits and seven programmable command bits that are defined as required according to the protocol or the DLI design.

F. Send Status Register

2.08 The send status (SST) register is used to trap errors in both the UDLC and the particular DLI that was being communicated with at the time the fault occurred.

G. DLI Activity Registers

2.09 The UDLC contains additional sets of registers used to indicate the general status of each DLI and whether any immediate action is being requested by a DLI. One bit in each of the 16-bit registers is assigned on a permanent basis to each DLI. These bits are asynchronously set and reset under the control of individual DLIs.

H. Multiplexer/Demultiplexer

2.10 The data bus structure employed between UDLC and DLI consists of a 9-bit data parallel bus. Each 16-bit word transmitted by the UDLC to the UDLC is divided into two 8-bit words and multiplexed out to the appropriate DLI. Similarly, two DLI words must be demultiplexed to form a complete data word. Parity accompanies the data bits. Data transmitted from the UDLC is checked by the DLI for proper received parity on each word. A positive acknowledgement reply must be generated back to the UDLC after receiving each word to indicate if parity has passed. If no positive reply is received, then either a parity failure or a device failure has occurred.

I. Microcontroller

2.11 A microcontroller that consists of a stand-alone ROM and a microprogram control circuit is used to control the repetitive processes of communicating with a DLI. The microcontroller assumes control whenever a DLI addressed command is detected by the UDLC.

3. DLI STRUCTURE

3.01 The data link interface is a wired logic circuit providing an interface unit compatible with data link control requirements on one end and the UDLC on the other. The DLI consists of an EIA interconnection, a universal synchronous/asynchronous receiver and transmitter (USART), and data buffering. The USART is a programmable microprocessor that performs the parallel-to-serial and serial-to-parallel conversions. The data buffering

includes a control and error checking circuit to guarantee the integrity of the data communicated between the UDLC and the DLI.

A. Bus Circuit

3.02 The DLI contains two bus circuits, 0 and 1, from the two respective UDLCs which permit communications from either controller. Each bus is divided into a 9-bit command field, four reply bits and a 9-bit bidirectional data access bus.

B. First-In-First-Out(FIFO) Registers

3.03 The DLI contains two FIFO registers. One FIFO is designated as the write or transmit FIFO and the other is designated as the read or receive FIFO. Each FIFO is 8 bits by 64 words. A read and write FIFO pointer circuit, comprised of two separate sets of up/down counters, is used to indicate the number of words contained within the FIFO registers. Both pointers can be interrogated by a single PDSP command.

C. Input Buffer and First Maintenance Loop Around

3.04 The input buffer is a single 8-bit register that is loaded with the data presently being written from the UDLC to the DLI. The data remains in the input buffer until overwritten by a new word. On normal write operations, the data word would also be loaded into the transmit FIFO register or the USART depending on the type of command. This facilitates the first level maintenance loop around. If the write command is identified as a first level maintenance loop around operation, the data is loaded into the input buffer only. By issuing a first level maintenance loop around read command, the data is read out of the input buffer onto the common internal DLI bus, parity is generated, and the data is returned to the PDSP. This permits testing of the bus between the UDLC and DLI, checks the bus receivers and driver, verifies proper parity operation and partially checks the DLI control circuit. Also, this test can be performed on an active DLI without interfering with normal data transmission.

4. UDLC/DLI PROGRAMS

4.01 The major UDLC/DLI programs are: administrative, data link driver, device handler, and fault recognition.

A. Administrative Program

4.02 The administrative program controls the switching from the active circuit to the standby circuit, the running of automatic UDLC diagnostics, the printing of hourly status reports and failure rate reports, all input/output messages pertaining to the UDLC, and the maintenance of the active unit and the UDLC pair state.

B. Data Link Driver

4.03 The data link driver program (DL01) is the input/output interface program which controls the data links using the UDLC/DLI hardware interface. It is a subroutine of the PDSP EOS program. The main tasks of the data link driver program are:

- To administer the DDCMP protocol
- To control the UDLC/DLI hardware
- To transfer messages to and from the higher level program (DSORT).

The data link driver program communicates to other PDSPs in the EPSCS data network, and to CNCC and CSACC computers through the data links. DDCMP is a message-oriented protocol which allows reliable data transmission in spite of occasional errors in transmission facilities or interfacing hardware. Message routing on the PDSP data network is done by the DSORT program which fills in the destination fields in message headers and outputs messages to the appropriate data link groups. The message types and message destinations are transparent to the data link driver program, which deals with one data link at a time and is indifferent to message content.

4.04 Outgoing messages are passed to the data link driver program from DSORT via the EOS WRITE macro. If the data link is not in the protocol "running" state (numbered data messages are being sent and received) or if the data link buffer is full, the message is rejected and the reason for rejection is reported to DSORT in the return code from the EOS WRITE macro. Otherwise, the new message is placed in queue in the data link buffer behind the other outstanding messages. A sequence number is assigned to the message when it is moved into the data link buffer from system memory. This message numbering is

another error check, because the receiving end rejects out of sequence messages. Each message is transmitted over the data link in its turn, but it is retained in the software buffer until an acknowledgment is received from the receiving end. When a negative acknowledgment from the receiving end indicates that a message was not transmitted correctly, all outstanding messages are retransmitted. Once the messages are placed in the data link driver buffer, DSORT cannot retrieve them. Incoming data messages which are received correctly by the data link driver program are immediately transmitted to DSORT. Incorrectly received messages are discarded and the sending PDSP is notified to retransmit the message.

4.05 The data link driver program consists of a base level and an interrupt level. The base level initializes the driver, processes WRITE commands, and responds to TTY commands directed to the data links. The WRITE command requires the driver to retrieve a message sent to it by DSORT through system memory, queue the message in the data link buffer, add a DDCMP header, assign a message number, and free system memory by setting a completion code.

4.06 The interrupt level is entered when a data link is to be polled. Also, error counts are kept for both the hardware operations and for DDCMP detected transmission errors. Whenever the frequency of errors exceeds a certain threshold, recovery action is initiated and TTY messages are generated. The timers necessary to detect these thresholds are administered at the interrupt level.

C. Device Handler

4.07 Each PDSP device has a device control block (DVCB) associated with it. This control block contains status information concerning the device. The UDLC device handler sets up this control block. The main difference between the UDLC as a device and other PDSP devices is that the UDLC has a controller 0 and a controller 1. At initialization, the device handler writes the DLI active controller address in each DLI control block. The UDLC device handler maintains the controller 0 address in its own device control block, keeps track of the active controller, and can determine the address of the active controller since it is algorithmically related to the controller 0 address.

4.08 Because the DLIs are accessed through the UDLC active controller, their addresses also have a controller 0 and controller 1 address.

D. Fault Recovery

4.09 Basically, the UDLC fault recovery scheme consists of the rapid removal from service of a faulty UDLC and its replacement with the duplicate standby UDLC. Once the faulty unit has been removed from service, it is automatically diagnosed under the initiation of UDLC fault recovery. The class of faults that may be identified by UDLC fault recovery are:

- Fault in subparallel channel (SPCH)
- Fault in DLI
- Fault in controller (CONTR)
- Multiple faults (MULT).

4.10 The multiple faults class indicates that a working configuration cannot be found. Each fault class will produce an output message in the following form:

```
REPORT UDLCP 0 CONTR a FAULT IN %b%bbb
```

a = 0 or 1

%b%bbb = CONTR, DLI, SPCH, or MULT

Additional data printed with this message will include the failing DLI number and the UDLC status register contents.

4.11 There are two remaining fault classifications:

- ERROR
- FAILURE.

The error classification indicates that a trouble has been detected by the DLI driver which cannot be reproduced by the fault recovery programs. Because of expected transient errors, no messages of the error classification are printed until a threshold is exceeded. This threshold is currently three per hour per DLI and is maintained as a total count and not on a per DLI basis. For example, an office with three DLIs will have no messages of the error classification printed until the tenth

message. All other message types will be printed at all times. If more than three troubles occur in a 10-second period, fault recovery is inhibited. When fault recovery is inhibited all faults are reported as failure faults. Fault recovery can be re-enabled manually by a TTY message or will be automatically re-enabled after the hourly reports. The message format for the error and failure fault classifications is:

```
REPORT UDLC 0 CONTR a 000000
```

a = 0 or 1

000000 = ERROR or FAILURE

The same additional failing data is provided with the message as is provided with the previous messages.

4.12 The automatic fault recovery responses for a failing UDLC are given priority over the fault recovery procedures of its associate PIU. The UDLC fault recovery software is permitted to make a request for a system configuration change which overrides the actions of the PIU maintenance software. PIU fault recovery is permitted to perform a system configuration change only if the UDLC maintenance software determines that no loss of UDLC operations will occur because of the configuration change. The override output message has the following form:

```
REPORT PIU 0 OVERRIDE CONF IS IN  
EFFECT ON CKT a
```

a = 0 or 1.

This message implies that UDLC fault recovery has forced a particular controller to be the active unit and has notified the PIU fault recovery program. In turn, PIU fault recovery has communicated a message to the No. 1 ESS, by way of an F-level interrupt, to reconfigure the PIU in accordance with UDLC fault recovery. If the No. 1 ESS is unable to perform the correct reconfiguration, the interface with the PDSP will be lost. A separate message will be output on the maintenance TTY which will describe the state of the interface between the No. 1 ESS and the PDSP.

UDLC Fault Recovery States

4.13 The UDLC fault recovery states are the normal state and the trouble state. The state of fault recovery may be determined by the output TTY messages which appear on the PDSP maintenance TTY. The normal state indicates that the interface between the No. 1 ESS and the PDSP is functioning properly. This means that one controller is active and functioning properly and the standby controller is available for switching. Fault recovery enters the trouble state when a fault has been detected in either the active or standby UDLC controller. Upon detection of a fault in a controller, fault recovery automatically runs a diagnostic. The UDLC remains in the trouble state if the diagnostic does not pass.

Inhibiting Fault Reporting

4.14 On the fourth occurrence of any fault type, in any 10-second period, fault recovery is automatically inhibited and the fault reporting mechanism is turned off. A report on the status of the system at this time may be requested with the input message

```
OP:UDLCP a,STATUS!
```

a = 0 (UDLCP unit number)

The system response would appear as:

```
OUTPUT STATUS UDLC a TROUBLE  
AUNIT b
```

```
RECOVERY INH REPORT OFF
```

4.15 The following TTY messages are generated automatically and generate major alarm indications.

```
REPORT UDLC a CONTR b ccccc  
EXCEEDS THRESHOLD
```

a = 0 (UDLCP unit number)

b = 0 or 1 (UDLCP controller number)

cccccc = Type of fault which has exceeded the threshold (DLI, CONTR, MULT, SPCH, ERROR, or FAILURE).

```
INH UDLC 0 RECOVERY
```

- 4.16 Fault recovery can also be inhibited manually using the input message

INH:UDLCP a,RECOVERY!

a = 0 (UDLCP unit number)

The printing of fault recovery reports may be manually inhibited with the message

STOP:UDLCP a,REPORT!

Fault recovery is automatically re-enabled every hour, the associated error counters are reset to zero, and the reporting mechanism is re-enabled to again activate the fault recovery procedures.

- 4.17 Fault recovery (but not fault reports) may be reactivated manually with the input message

ALW:UDLCP a,RECOVERY!

a = 0 (UDLCP unit number)

- 4.18 The following procedure is suggested to re-enable fault recovery and the printing of the associated reports:

- (1) Enable the report printing mechanism

REPT:UDLCP a,ØØbbb!

a = the pair number of the UDLC for which reports are requested.

ØØbbb = ALL—all messages are printed.

= FAULT—transmit error messages are not printed until the error threshold is exceeded.

- (2) Activate fault recovery

ALW:UDLCP a,RECOVERY!

- 4.19 If fault recovery is not manually activated, but the printing of errors is manually enabled, then the only error type sensed by the system is the failure classification. The system will print FAILURE message until the fourth occurrence of this error type when the printing of fault recovery reports will again be automatically inhibited by the system.

Fault Resolution

- 4.20 Figure 2 is a representation of the conditions that produce a sample of 17 possible faults. The UDLC loop around (UDLC-LA) test can be run on the active controller (AC) and the standby controller (SC). The DLI loop around (DLI-LA) test can also be run on both the active controller and the standby controller.

The DLI-LA test is run on the particular DLI that was reported as failing (FAIL) and is also run on the other DLI units. In the case of a control unit switch (CU SW), the P indicates a successful switch and the F indicates that the switch could not be accomplished.

- (1) **Case 1:** In this case, the active controller passed the UDLC-LA test and all DLI units passed the DLI-LA test. This situation is classified as a error fault type.

- (2) **Case 4:** The note indicates that the pair state has been classified as trouble. The loop around test on the active UDLC passed but the reported DLI unit failed the DLI-LA test. This situation is classified as a DLI fault type.

- (3) **Case 7:** The note indicates that the pair state for this case must be normal. The active UDLC failed the loop around test but the standby UDLC passed the test. Also, all DLI units passed the DLI-LA test with the standby controller. This situation is classified as a controller (CONTR) fault type. This case will result in an active unit switch and automatic diagnosis.

- (4) **Case 10:** Both the active and standby UDLC failed the loop around test. A PDSP control unit switch was successful. After the CU SW, the active UDLC passed the loop around test and the failing DLI passed the DLI loop around test. This situation is classified as a subparallel channel (SPCH) fault type. In this case, the CU diagnostics and associated PCH diagnostics should be run.

- (5) **Case 13:** Both the active and standby UDLCs failed the loop around and the control unit switch could not be accomplished. This situation is designated as a multiple (MULT) fault type. In this case, the CU diagnostics and associated PCH diagnostics should be run.

TEST RUN	CASE																
	1	2	3 ¹	4 ²	5 ¹	6 ¹	7 ¹	8 ³	9	10	11	12	13	14	15	16	17 ³
UDLC_LA AC	P	P	P	P	P	P	F	P	F	F	F	F	F	F	F	P	
DLI_LA AC	FAIL	P	P	F	F	F	-	F	-	-	-	-	-	-	-	F	
	OTHER	P	F	P	X	X	X	-	F	-	-	-	-	-	-	F	
UDLC_LA SC	-	-	P	-	P	F	P	P	P	F	F	F	F	F	F	P	
DLI_LA SC	FAIL	-	-	P	-	F	-	P	P	F	-	-	-	-	-	F	
	OTHER	-	-	X	-	X	-	P	X	X	-	-	-	-	-	F	
/ / / / / / / / / / / / / / / / / / / /																	
CU SW	-	-	-	-	-	-	-	-	-	P	P	P	F	P	P	P	
UDLC_LA AC	-	-	-	-	-	-	-	-	-	P	P	P	-	F	F	P	
DLI_LA AC	FAIL	-	-	-	-	-	-	-	-	P	F	F	-	-	-	F	
	OTHER	-	-	-	-	-	-	-	-	X	P	P	-	-	-	F	
UDLC_LA SC	-	-	-	-	-	-	-	-	-	-	-	P	-	P	F	P	
DLI_LA SC	FAIL	-	-	-	-	-	-	-	-	-	-	P	-	P	-	F	
	OTHER	-	-	-	-	-	-	-	-	-	-	X	-	X	-	F	
/ / / / / / / / / / / / / / / / / / / /																	
FAULT TYPE	E	E	E	D	D	D	C	C	C	S	S	S	M	M	M	M	
	R	R	R	L	L	L	O	O	O	P	P	P	U	U	U	U	
	R	R	R	I	I	I	N	N	N	C	C	C	L	L	L	L	
	R	R	R				T	T	T	H	H	H	T	T	T	T	
	R	R	R				R	R	R								

NOTES:

1. PAIR STATE MUST BE NORMAL
2. PAIR STATE IS TROUBLE
3. ALL DLIs FAIL (MORE THAN ONE DLI IS DEFINED IN THE SYSTEM)

P = TEST PASSED
 F = TEST FAILED
 X = DON'T CARE
 - = TEST NOT RUN
 FAIL = FAILING DLI

Fig. 2—Fault Resolution

5. UDLC/DLI DIAGNOSTICS

5.01 Six diagnostic messages are produced automatically when the No. 1 ESS requests the PIU and UDLC diagnostics to be executed. If each diagnostic does not produce an all tests passed (ATP), the diagnostics must be run manually from the maintenance TTY. The PIU must be run from the No. 1 ESS TTY, but the UDLC diagnostic may optionally be run from the PDSP TTY. The trouble locating manual (TLM) should be used to identify the cause of each diagnostic failure. No fault recovery state change occurs when the UDLC diagnostic is run manually from the PDSP side. Therefore, the fault recovery sequencer is left in

the trouble state. When the UDLC diagnostic finally produces an ATP message at the PDSP maintenance TTY, the PIU diagnostic should be initiated from the No. 1 ESS side. This execution of the PIU diagnostic will cause the fault recovery sequencer to be updated to the normal state after all of the PIU and UDLC tests are ATP. It may be determined that the fault recovery sequencer has entered the normal state by typing in the following message at the PDSP maintenance TTY:

OP:UDLCP a,STATUS!

where a = the unit number of the UDLC pair.

The system will respond with the following output message:

OUTPUT STATUS UDLC a NORMAL
AUNIT b

RECOVERY ccc REPORT ddddd

where a = the unit number of the UDLC pair

b = the active controller (0,1) in the UDLC pair

ccc = allow (ALW) or inhibit (INH)

dddd = ALL, OFF or FAULT.

5.02 When fault recovery is in the normal state, the UDLC has an associate PIU and the standby UDLC controller is fault-free. The standby UDLC controller has been previously diagnosed by the system and the diagnostic was found to produce an ATP result. However, if diagnosis of the UDLC standby controller is desired, it is necessary to first remove the standby controller:

RMV:UDLCP a,CONTR b;UCL!

where a = unit number of the UDLC pair

b = the number of the standby controller

The UDLC diagnostic (all tests) may then be requested on the controller that was removed:

DGN:UDLCP a,CONTR b;UCL!

To restore the controller to standby:

RST:UDLCP a,CONTR b;UCL!

5.03 Fault recovery enters the trouble state when a fault has been detected in either the active or standby UDLC controller. Upon the detection of the fault in a controller, fault recovery will then automatically run a diagnostic. The trouble state will be entered if the diagnostic does not pass. An STF message will be printed at the PDSP maintenance TTY.

5.04 Manual diagnostics can only be run if fault recovery is in the trouble state. If a manual

diagnostic request is typed into the system when fault recovery is not in the trouble state, the system will automatically place fault recovery in the trouble state.

5.05 The DLI driver program performs all the PDSP message handling that requires the UDLC and DLIs. When a fault occurs, the DLI driver program calls fault recovery as a subroutine. An output message is generated if the recovery programs can identify the fault.

A. UDLC/DLI Diagnostic Procedures

5.06 The following procedure may be used when UDLC/DLI problems occur:

- (1) Determine the UDLC and DLI numbers being used when the failure occurred.
- (2) If the UDLC to be tested is not out-of-service, remove it from service by typing:

RMV:UDLCP a,CONTR b!

where a = 0 or 1, the failing UDLC pair number

b = 0 or 1, the failing controller in pair a.

- (3) Request the UDLC diagnostic (all tests) by typing:

DGN:UDLCP a,CONTR b;UCL!

- (4) If all 11 tests pass, go to Step 6 to diagnose the DLI.

- (5) Correct any problems detected by the diagnostic and repeat this procedure beginning with Step 2.

Note: Removing a DLI from service will be customer-affecting and should be done only as a last resort.

- (6) If the DLI is not already out-of-service, remove it from service by typing:

RMV:DEVICE:DLI a!

where a = failing DLI number.

- (7) Request the DLI diagnostic (all tests) by typing:

DGN:DLI a,UCL!

- (8) Correct any problem detected and repeat Step 7 to insure that all problems were corrected.

- (9) To test the integrity of the circuits, place the system in the configuration that existed when the original fault occurred. Make the failing UDLC active by typing:

SW:UDLCP a,CONTR b!

where a = original failing UDLC pair number

b = original failing controller in pair a.

Leave the failing DLI out-of-service to allow it to be diagnosed.

- (10) Close the analog loop on the data set.
- (11) Request the DLI diagnostic test 3 for the analog loop test in the repeat mode of operation for a few minutes by typing:

DGN:DLI a,DELAY bb;RPT:3!

where a = DLI number

bb = additional delay needed to allow characters to be looped around before being checked (bb is the number of 0.1 msec increments desired).

B. UDLC Diagnostic Program Tests

5.07 The following tests are performed by the UDLC diagnostic program:

- (a) **Test 1:** Diagnosis of duplex bus selector (DBS).
- (b) **Test 2:** Verification of status register read order; verification of UDLC and DLI address decoders.

- (c) **Test 3:** Verification of command present (CP) order while sending UDLC reset command.

- (d) **Test 4:** Select register errors are *stimulated* and the error bits (9,10) are checked for each *stimulated* error.

- (e) **Test 5:** Verification of UDLC read command (DR).

- (f) **Test 6:** Verification of UDLC write command (DP).

- (g) **Test 7:** UDLC and DLI errors are *stimulated* and error bits (1,2,3,4,5,6) are checked for each *stimulated* error.

- (h) **Test 8:** Verification of UDLC parity checker.

- (i) **Test 9:** Verification of DLI write and read commands.

- (j) **Test 10:** Verification of information leads from PDSP to UDLC.

- (k) **Test 11:** Verification of the data access bus from UDLC to each active DLI.

C. UDLC Diagnostic Output Messages

5.08 The following information is contained in a UDLC diagnostic output message.

- A test number (from 1 to 11)
- A segment number (from 00 to 99)
- A trouble/error number (from 0 to 40)
- All 16 general PDSP registers at time of error.
- UDLC status (if available)
- Supplementary data.

Additional information is available in TLM 1A727-01.

D. DLI Diagnostic Program Tests

5.09 The following tests are performed when the DLI diagnostic program is executed.

- (a) **Test 1:** Verification of reset and DLI parity checker
- (b) **Test 2:** Verification of USART operations
- (c) **Test 3:** Verification of FIFO registers.

E. DLI Diagnostic Output Messages

5.10 The following information may be obtained from a DLI diagnostic output message.

- A test number (from 1 to 3)
- A segment number (from 00 to 99)
- A trouble/error number (from 0 to 9999)
- Values of all 16 general PDSP registers at time of error.

Additional information is available in TLM 1A726-01.

F. DBS Diagnostic

5.11 The duplex bus selector diagnostic turns off the DBS while it runs. Therefore, input/output failures would occur on an in-service unit whose DBS is being diagnosed. However, input/output interrupts will not address the associate of a unit under diagnosis since the maintenance programs

of both the PIU and the UDLC will force both associate units out-of-service when either is faulty.

6. UDLC/DLI MAINTENANCE

6.01 Any three faults in a 10-second period will cause fault recovery to be inhibited. When fault recovery is inhibited, none of the fault resolution tests are run. The fault classification of failure maintains a count of additional errors.

6.02 For the fault classification of error and for DLI, no action is required by the maintenance personnel except to observe the DLI in error and note any possible pattern. During the off hours, the DLI may be removed from service and then diagnostics may be run against it. The fault classification of CONTR causes an automatic switch of controllers and execution of diagnostics on the failing controller. The fault classification SPCH and MULT cause a switch of the control units and the controllers. Diagnostics are automatically executed on the failing controller. If desired, the maintenance personnel can execute the control unit diagnostic, the parallel channel diagnostic, and the duplex bus selector diagnostic.

7. DATA LINK RESTORAL PROCEDURE

7.01 The following flowchart is used for the data link restoral. See Fig. 3.4

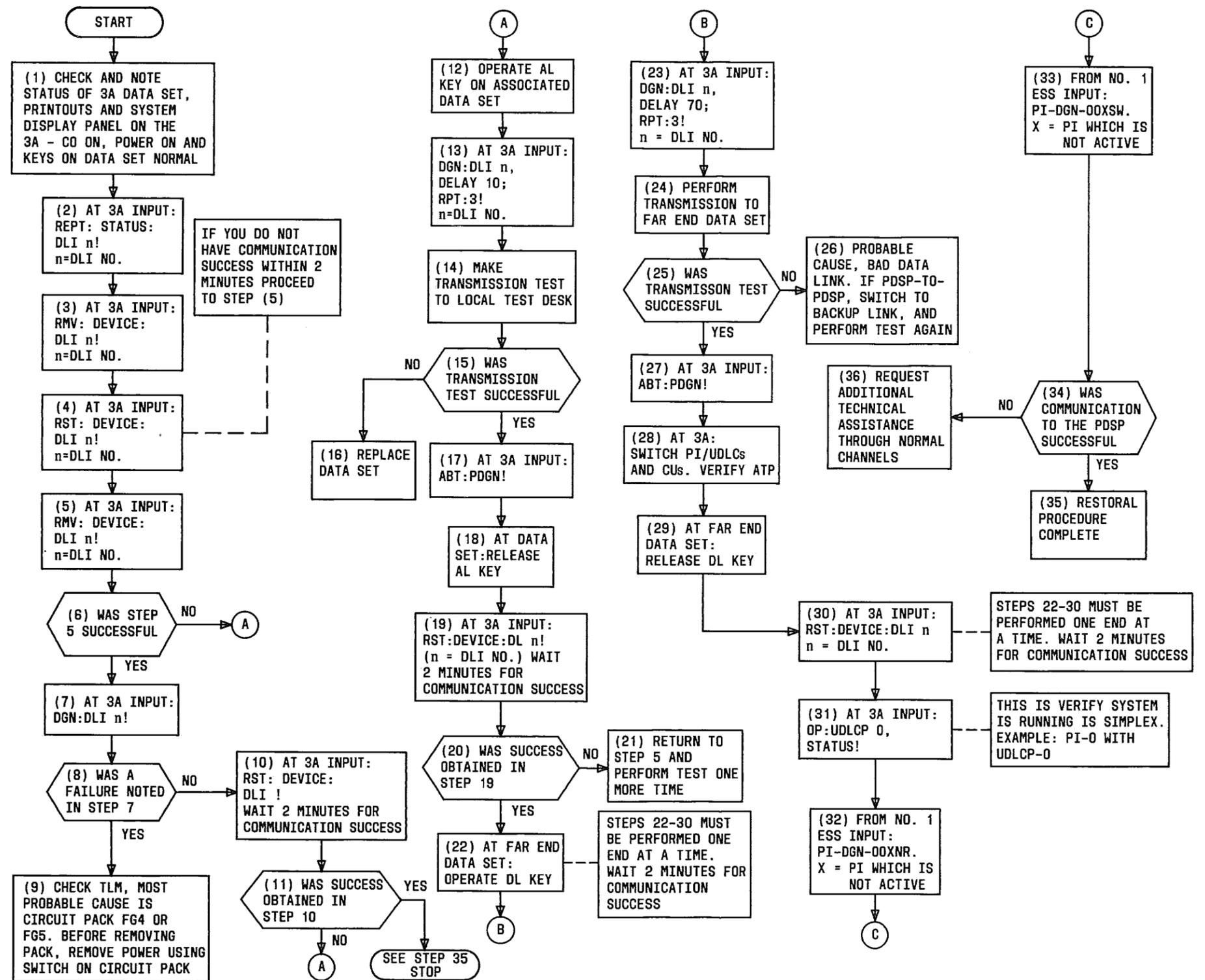


Fig. 3—Data Link Restoration Procedures