

## BUS SYSTEM TEST PROCEDURES

### 2-WIRE NO. 1 ELECTRONIC SWITCHING SYSTEM

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4. ABBREVIATIONS . . . . .	19	1. GENERAL	
		1.01 This section gives procedures for using the bus testing program (XBUS) auxiliary test program for the 2-Wire No. 1 Electronic Switching System (ESS). The program operates as a library program in program store (PS) module 05 of PS 0 (or module 15 of PS 1) and requires that the special library module be loaded as described in PA-1A500 or Section 231-147-301. The XBUS program is covered in PR-1A504. The scanner answer bus test is not covered in this section because it is allowed in auxiliary program Western Electric (APW) but not auxiliary program telephone company (APT) packages.	
<b>Figures</b>		1.02 This section is reissued to:	
1. Dual-Channel Scope Probes Connected Across a BTR to Reduce Noise on the Display . . . . .	3	(1) Update to PR-1A504, Issue 7	
2. Scope Displays for Bit 36 (Reset) and Bit 37 (FCG) . . . . .	6		
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- (2) Add:
  - (a) Enable pulse requirements
  - (b) Noise measurement requirements
  - (c) Notes and cautions
  - (d) A message for the 32K call store test.
- (3) Change:
  - (a) Scope procedures
  - (b) The CPD message.
- (4) Remove references to 6-program store offices
- (5) Make miscellaneous minor changes.

Since this is a general revision, arrows ordinarily used to indicate changes have been omitted.

**1.03** An initial test using program XBUS should be performed before the office is cut over. This test should be conducted on a per-frame basis. The program XBUS should also be performed periodically per the ETL. Conduct this periodic test at the bus terminating resistors (BTR). When growth occurs in an office, the program XBUS should be performed on the growth frames. The program XBUS may also be performed when trouble is suspected on a bus.

**1.04** The capabilities of program XBUS can be divided into two tests.

(1) **Peripheral Units Bus Test:** The peripheral units bus (PUB) test, which is run with the bus in an out-of-service (OS) condition, contains the three procedures described below. (Detailed procedures are in Part 3.)

(a) **Transposition and Polarity Test:** The transposition and polarity test provides the means to check the wiring on the PUB for both bit transposition and turnovers.

(b) **Enable Window Test:** The enable window test provides the means to verify that at a scanner frame, the coincidence of enable and bus data is sufficient to allow proper operation of the frame.

(c) **Noise Test:** The noise test insures that the crosstalk current on the bus is not increased as a result of adding a new frame.

### (2) Off-Line Testing

(a) **Call Store Bus Test:** The call store (CS) bus test can be used in the off-line mode to check bus connections during an office addition or to make a routine check of the CS bus system. Included in this test are the CS address, answer, and data bus tests.

(b) **Program Store Bus Test:** The PS bus test can be used in the off-line mode to make a routine check of the PS bus system. Included in this test are the PS address and answer bus tests.

**1.05** Abbreviations used in this section are listed in Part 4.

## 2. APPARATUS

**2.01** The apparatus required to perform the tasks in this section include:

- Auxiliary program J1A064AA List 2, 3, or 5 (See PA-1A500, Section 8)
- 453A-type Tektronic oscilloscope or equivalent
- P6021 ac current probe and amplifier
- KS-14510 L3 volt-ohmmeter
- Short section of coaxial cable.

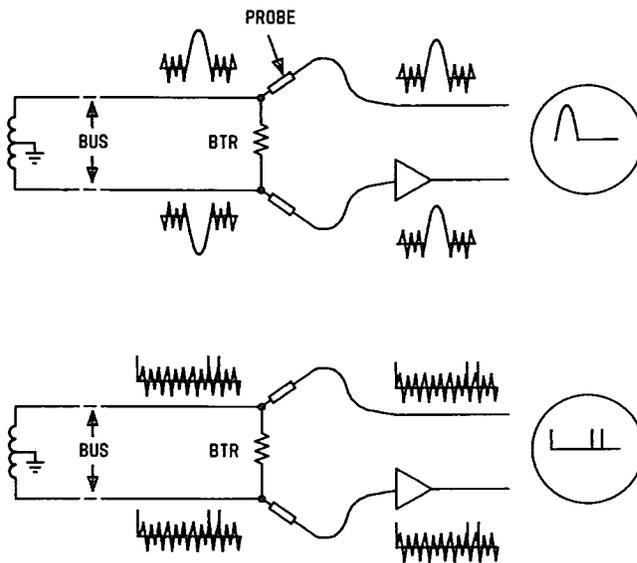
## 3. PROCEDURES FOR BUS TESTING PROGRAM (XBUS)

### PRELIMINARY PROCEDURE

**Caution:** The user should be familiar with Section 231-117-301 before using offline operation.

**3.01** The user must select the buses to be tested. Bus layouts are in the office base drawing T-xxxx-yy-388. (The x and y variables are the office base number and control group number.) The user also must locate the terminals on the buses where oscilloscope readings are to be taken.

**Note:** In some tests, bus pulse trains are narrow spikes on the oscilloscope display and may require increased intensity to be visible. To observe a single pulse in detail, the sweep may be expanded and the alternate connection method in Fig. 1 used. Both voltage probes of a dual-channel oscilloscope are connected across a bus terminating resistor (BTR). One channel is inverted so that the pulse amplitude is added and the noise is largely cancelled.



**Fig. 1—Dual-Channel Scope Probes Connected Across a BTR to Reduce Noise on the Display**

**3.02** PS module 05 must be loaded with the proper auxiliary program package; therefore, before running XBUS, perform the preliminary procedures in PA-1A500 or Section 231-147-301 for inserting an auxiliary test module, configuring auxiliary test programs into service, and using the LIB-EDIT- message.

#### PERIPHERAL UNITS BUS TEST

##### A. Transposition and Polarity Test

- (1) At the master control center (MCC), set the PUA switch (ie, BUS ISOLATION CONTROL switch for the peripheral unit address

buses) to the REQUEST position for the bus (0 or 1) to be tested.

System response should be

OK TO RMV PWR PBS

**Note:** For offices not having signal processors (SPs), skip step (2) and go to (3).

- (2) For offices having signal processors, perform the following steps on either the even central pulse distributor (CPD) if testing bus 0 or on the odd CPD if testing bus 1.

- (a) Depress the BUS DISTRIBUTION REQ INH key on the CPD.

System response should be an MA10 OK TO RMV PWR PBS message.

- (b) Depress the BUS DISTRIBUTION OFF key on the CPD. (This step removes the SP from the bus being tested.)

System response may be a possible SP06 message, an MA11 MAN. PWR RMV PBS message, and possible F-level interrupts.

- (c) Depress the BUS DISTRIBUTION REQ INH key on the CPD. (This step allows the program XBUS to have access to the PUB being tested.)

- (d) Repeat (a) through (c) for each additional even or odd CPD frame selected.

- (3) To start the program, type the following at the maintenance teletypewriter (TTY):

LIB-START-03 01 b 00.

b = 0 for testing bus 0

= 1 for testing bus 1

System response should be OK.

Lamp PD23 will light if the test is running.

The program will initiate pulses on each bus pair. The pulses form a binary number that is equivalent to the bus pair number.

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(4) To verify bus pairs 0 through 35 (address bits), perform the following steps:

(a) Attach a scope probe from channel A of a dual-trace oscilloscope to bit 0 of the bus being tested to obtain a trigger source.

(b) Set the scope time base to 20 microseconds per division.

(c) Line up the scope sync (bit 0 in Table A) with the eighth vertical grid mark counting from right to left.

(d) Use the channel B scope probe to check bits 1 through 35 in sequence while observing the scope display. Check both positive and negative terminals. Verify that the pulse at each terminal is of the correct polarity and shape and that each bit appears as the correct binary count. The binary weights correspond to the spaces between the vertical grid marks on the scope screen. For example, binary weight 1 is between the first and second vertical grid mark from the right, binary weight 2 is between the second and third mark, etc (Table A). Proper pulses verify that there are no transpositions, shorts, or opens on the bus being tested.

(5) To verify bits 36 (reset) and 37 (false cross and ground):

(a) Connect a scope probe from the channel A input to bit 37 on the bus.

(b) Connect a second probe from the channel B input to bit 36 on the bus.

(c) Place scope vertical mode switch to ADD.

(d) Observe that the scope display is as shown in Fig. 2(A). (Typical error-condition displays are shown in Fig. 3.)

(e) Place vertical mode switch to ALT.

(f) Observe that channel B displays bit 36 in relation to bit 37 (channel A) as shown in Fig. 2(E).

(6) To terminate the test at any time, type:

LIB-START-000000.

(7) To restore the bus to service:

(a) Depress the BUS DISTRIBUTION NOR key on the CPD.

(b) Return the PUA switch on the MCC to NORMAL.

(8) Repeat Steps 1 through 7 for each bus selected for testing.

**B. Enable Window Test**

**3.03** To verify that coincidence of the enable pulse and bus data at a scanner frame is sufficient for proper operation of the frame:

(1) At the MCC, set the PUA switch (ie, BUS ISOLATION CONTROL switch for the peripheral unit address buses) to the REQUEST position for the bus (0 or 1) to be tested.

System response should be

OK TO RMV PWR PBS

(2) Type:

LIB-START-03 02 b 01.

b = 0 for testing bus 0

= 1 for testing bus 1.

(3) Type:

LIB-DEC-uummm.

uu = Unit type of frame to be tested (decimal)

= 05 for master scanner

= 12 for line scanner

= 17 for junctor scanner

= 19 for universal trunk scanner

mmm = Member number of frame to be tested (decimal).

Lamp PD23 on the MCC will light while the test is running.

TABLE A

SCOPE DISPLAYS FOR PU BUS TESTS

PU BUS BIT	SCOPE SYNC ↓	BINARY WEIGHTS					
		32	16	8	4	2	1
Bit 0							
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
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34							
35							

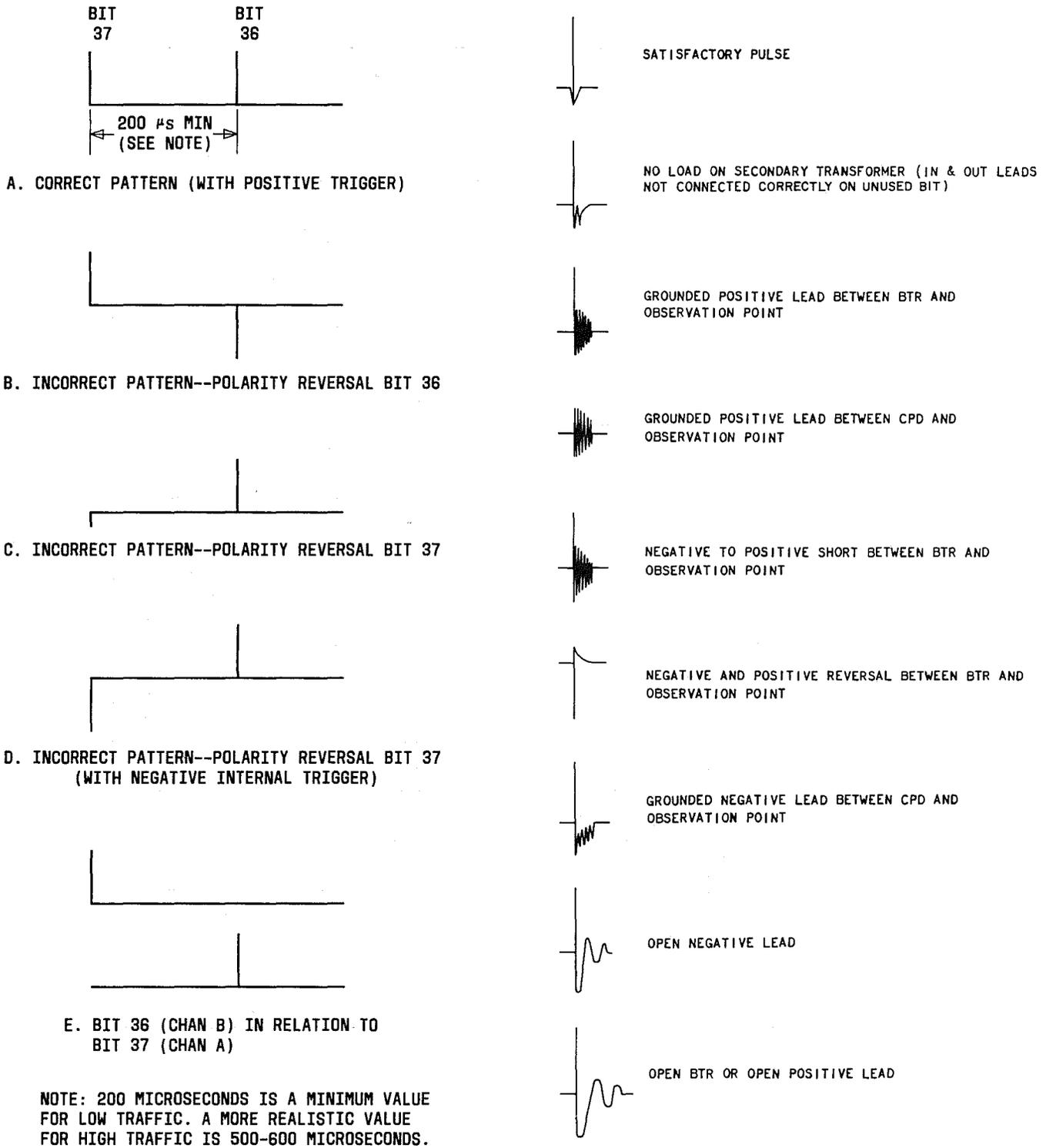


Fig. 3—Examples of Bus Terminal Conditions Observed at A Position Terminal

Fig. 2—Scope Displays for Bit 36 (Reset) and Bit 37 (FCG)

(4) Set up a dual trace oscilloscope as follows:

- (a) Set the time base for .5 microseconds per division.
- (b) Attach the scope probe of channel A to the output of the cable receiver pack for the EN00 enable if bus 0 is being tested or the EN11 enable if bus 1 is being tested. This supplies the trigger source. (The proper terminal is identified in Table B under the channel A column for the selected bus.)
- (c) Attach the scope probe of channel B to the output of the cable receiver pack for bit 0. (The proper terminal is identified in Table B under the channel B column for the selected bus.)

(5) Observe that the pulses on the scope display meet the following requirements (See Fig. 4):

- (a) The address pulse at the output of the cable receiver pack must have a duration between 0.25 and 0.75 microsecond.
- (b) At least 0.25 microsecond of the address pulse must be coincident with the enable window.
- (c) Address pulse rise and fall times are not critical as long as they do not exist in adjacent windows.

(6) To terminate the test at any time, type:

LIB-START-0000000.

(7) Return the PUA switch on the MCC to NORMAL to restore the bus to service.

(8) Repeat Steps (1) through (7) for each bus selected for testing.

### C. Noise Test

**3.04** To make noise measurements on the PUB:

- (1) At the MCC, set the PUA switch (ie, BUS ISOLATION CONTROL switch for the peripheral unit address buses) to the REQUEST position for the bus (0 or 1) to be tested.

System response should be

OK TO RMV PWR PBS

**Note:** For offices not having SPs, skip step (2) and go to (3).

(2) For offices having signal processors, perform the following steps on either the even CPD if testing bus 0 or on the odd CPD if testing bus 1.

(a) Depress the BUS DISTRIBUTION REQ INH key on the CPD.

System response should be an MA10 OK TO RMV PWR PBS message.

(b) Depress the BUS DISTRIBUTION OFF key on the CPD. (This step removes the SP from the bus being tested.)

System response may be a possible SP06 message, an MA11 MAN. PWR RMV PBS message, and possible F-level interrupts.

(c) Depress the BUS DISTRIBUTION REQ INH key on the CPD. (This step allows the program XBUS to have access to the PUB being tested.)

(d) Repeat (a) through (c) for each additional even or odd CPD frame selected.

(3) Type:

LIB-START-03 03 b 01.

b = 0 to test bus 0

= 1 to test bus 1.

(4) Type:

LIB-DEC-000xx.

xx = Bus bit number selected for test (decimal).

Lamp PD23 on the MCC will light while the program is running.

The program will send zero (no bits) on the selected bit to allow noise measurements to be made. All

TABLE B

## BUS AND CHANNEL IDENTIFICATION

EQUIPMENT SCANNER TYPE AND SD NUMBER	BUS 0						BUS 1					
	CHANNEL B INPUT PUA (0AD00)			CHANNEL A INPUT EN00			CHANNEL B INPUT PUA (1AD00)			CHANNEL A INPUT EN11		
	MOUNTING PLATE NO.	CKT PACK NO.	PIN NO.	MOUNTING PLATE NO.	CKT PACK NO.	PIN NO.	MOUNTING PLATE NO.	CKT PACK NO.	PIN NO.	MOUNTING PLATE NO.	CKT PACK NO.	PIN NO.
Master Scanners SD-1A209-01	32	18	3	34	36	1	32	26	3	34	38	21
Master Scanners SD-1A118-01	28	38	3	30	34	1	28	44	3	30	36	21
Line Scanners 2:1 LCR SD-1A111-01	132	18	3	134	36	1	132	32	3	134	38	21
Line Scanners 4:1 LCR SD-1A115-01	32	10	3	32	18	1	32	12	3	32	20	21
Junctor Scanners SD-1A214-01	32	18	3	34	36	1	32	26	3	34	38	21
Universal Trunk Scanners SD-1A215-01	32	18	3	34	36	1	32	26	3	34	38	21
Line Scanner 4:1 LCR Remreed SD-1A326-01	80	11	308	80	16	308	80	26	308	80	31	307
Line Scanner 2:1 LCR Remreed SD-1A332-01	80	11	308	80	16	308	80	26	308	80	31	307
Miniaturized Universal Trunk Frame SD-1A338-02	080	34	308	080	39	308	180	34	308	180	39	307
Combined Miscellaneous Trunk Frame SD-1A401-01	06	20	308	06	24	308	06	39	308	06	43	307
HILO Universal Trunk Frame SD-1A376-01	06	11	308	06	16	311	06	26	308	06	31	307
HILO Miscellaneous Trunk Frame SD-1A377-01	06	11	308	06	16	311	06	26	308	06	31	307

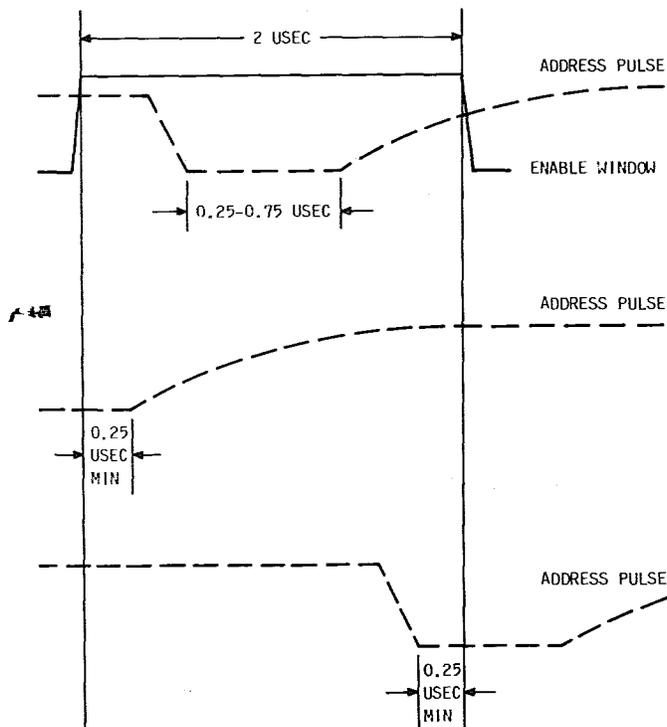


Fig. 4—Peripheral Units Bus Test Waveforms

ones are sent on each of the other bits of the bus.

- (5) Use an oscilloscope with a voltage probe to inspect the output of the receiver associated with the bus pair under test.
- (6) The scope should not display any pulses.

**Note:** If pulses exist at the output, excessive noise is indicated.

- (7) To terminate the test at any time, type:

LIB-START-0000000.

- (8) To test other bits, repeat steps 4 through 6 for each bus pair equipped.
- (9) To test another bus, repeat steps 1 through 8.

**Note:** The following steps are not required for the TELCO but may be used for more extensive analysis of failed noise tests in some

offices. The test uses installation handbook criteria and requires that a current probe be connected to bus pair appearances on:

- (a) BTRs (which may not be possible with some BTR hardware configurations)
  - (b) An ITE adapter used as an extender card to provide appearances. Adapter may not be available to the TELCO.
- (10) Set up a dual-trace oscilloscope as follows:
    - (a) Attach a scope probe from channel A to bit 0 of the bus being tested to obtain a trigger source.
    - (b) Set the scope time base to .2 microseconds per division.
    - (c) Line up the scope sync (bit 0) with the eighth vertical grid mark counting from right to left.
    - (d) Connect an ac current probe between the channel B input and the selected bus bit.

- (11) Observe the scope display. Figure 5 shows a normal bus bit and a typical noise pulse. The requirements for the noise pulse, as given in Installation Engineering Handbook 275A, Section 421.2, are as follows:

- If measurements are made at the last frame on the bus, the maximum positive pulse must not exceed 0.7 ma and the pulse width must not exceed 0.2 microsecond measured at the 50 percent point.
- If measurements are made at a frame other than the last frame on the bus, the allowable noise level will always be less than 0.7 ma. For each frame on the bus between the frame at which the measurement was made and the BTRs, subtract:
  - (a) 0.017 ma per frame for a nontwisted bus section.
  - (b) 0.011 ma per frame for a twisted bus section.

The pulse width requirement is 0.2 microsecond.

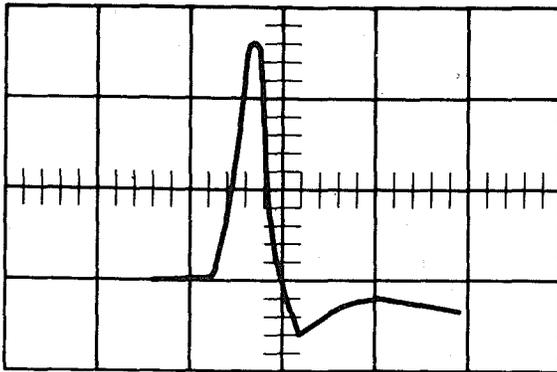
(12) To terminate the test at any time, type:

LIB-START-0000000.

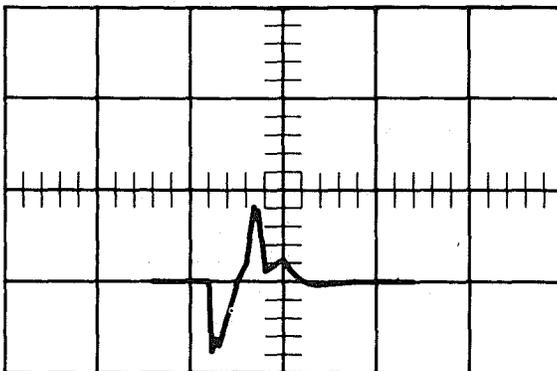
(13) To test other bits, repeat Steps (4), (10) and (11) for each bus pair equipped.

(14) To test another bus, repeat Steps (1) through (4), then (10) through (13) for each bus to be tested.

P.U. ADDRESS BUS CURRENT WAVESHAPES



TYPICAL NORMAL "ONE" BIT



TYPICAL NOISE "ZERO" BIT WHEN ALL OTHER BITS ARE "ONE" BITS

NOTE: THE ABOVE WAVESHAPES REPRESENT SCOPE DISPLAYS FOR 1 MILLIAMPERE PER MAJOR VERTICAL DIVISION AND 1 MICROSECOND PER MAJOR HORIZONTAL DIVISION.

Fig. 5—Normal Bus Bit and Typical Noise Pulse

OFF-LINE TESTING

**Caution 1:** The following tests are run in the off-line mode. They do not require the library control program

or any library input messages. The J1A064AA auxiliary program library must be in the PS that is to be taken off-line (PS 0 or PS 1).

**Caution 2:** Offline operation should be used during light traffic if possible since the system operates in simplex. A phase may be required to return to full duplex operation. The user should be familiar with Section 231-117-301 before using offline operation.

A. Call Store Bus Test

**Note:** If D level interrupts occur during the offline call store bus test, stop the offline CC (see paragraph 3.07).

CC-CS Bus Test

3.05 To check bus connections during an office addition or to make a routine check of the central control (CC) CS address, answer, and data buses, perform the following.

(1) Type one of the following:

(a) For offices with SPs, type

OFL-CONFIG-aabccd990.

(b) For offices without SPs, type

OFL-CONFIG-aabccd.

aa = Number of PS containing program library

b = PS bus (0 or 1)

cc = CS to be used off-line (either 00 or 01 except for answer bus test where CS can be CS0 through CS36.) In answer bus test, the CS selected must be on the fan-in being tested.

d = CS bus (0 or 1)

The system response should be PF followed by an 0L01 printout with information pertaining to the action performed.

**Note:** For offices with SPs, go to Step (3).

- (2) For offices without SPs, release the maintenance control (MAC) scratch by typing:

ØFL-MØDE-05.

System response should be ØK.

- (3) Type in:

ØFL-EXEC-060xxxxxxx00000000.

xxxxxxx = CCCSADD for address of CS address bus

= CCCSDAT for address of CS data bus (bus leads used for write orders for 8K call stores)

= CCCSDAT32 for address of CS data bus (bus leads used for write orders for 32K call stores)

= CCCSANS for address of CS answer bus (bus leads used for read orders).

**Note:** The absolute starting address for XBUS within the Mod 5 test program is found in PK-1A002-50x (x is for auxiliary test program being used). The relocatable address for routines CCCSADD, CCCSDAT, and CCCSANS are found in PR-1A504. To obtain the value of xxxxxxx, add the relocatable address for the appropriate routine to the absolute starting address of XBUS.

System response should be ØK.

- (4) To start the off-line CC and execute program loop, type in:

ØFL-MØDE-01.

System response should be ØK.

- (5) To set the ØL3 flip-flop so that maintenance orders will be sent on the bus, type:

T-CPD-W000017W.

System response should be ØK.

ØL3 is an offline control flip-flop in the CC. When it is set, the PS and CS bus selection is the same for maintenance and control orders as for normal orders. See CD-1A105-01, Buffer Bus System.

- (6) Scope the buses looking for the binary weighted bits shown in Table C for CC-CS address bus bits, Table D for CC-CS data bus bits, or Table E for CC-CS answer bus bits. Also note any error condition displayed on the scope (Fig. 3). Perform this check at each frame during initial installation and growth and at the BTR during periodic testing. When testing is completed on a bus, proceed to the next bus.

- (7) To stop the off-line CC, type in:

ØFL-MØDE-02

ØFL-EXEC-060xxxxxxx00000000.

xxxxxxx = Address of the next bus test.

System response should be ØK.

- (8) To restart the off-line CC, type in:

ØFL-MØDE-01.

System response should be ØK.

- (9) Repeat Steps 5 through 8 for final bus test.

- (10) When all tests have been run, the off-line mode must be cleared and the equipment restored before proceeding to the next bus (0 or 1). Type in:

ØFL-MØDE-02.

ØFL-MØDE-03.

System response should be ØK.

- (11) To terminate the off-line mode, type:

CS-RESTØRE-CSxx.

CS-RESTØRE-CBxx.

PS-RESTØRE-Syy.

CC-RESTØRE-.

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xx = Member number of unit being restored

yy = Number (00 through 11) used to specify PS to be returned to service.

System response should be PF followed by DR01.

(12) Repeat Steps 1 through 11 for other CS bus (0 or 1).

**SP-CS Bus Test**

**3.06** To check connections on the SP CS bus, perform the following.

(1) Type in:

ØFL-CØNFIG-aabccdeef.

aa = Number of PS containing program library

b = PS bus (0 or 1)

cc = CS to be used off-line

d = CS bus (0 or 1)

ee = SP to be used off-line

f = SP CS bus.

System response should be PF followed by ØL01.

(2) To release the MAC scratch, type in:

ØFL-MØDE-05.

System response should be ØK.

(3) Type in:

ØFL-EXEC-060xxxxxxx00000000.

xxxxxxx = SPCSADD for address of CS address bus

= SPCSDAT for address of CS data bus

= SPCSANS for address of CS answer bus.

**Note:** The absolute starting address for XBUS within the Mod 5 test program is found in PK-1A002-50x (x is for the auxiliary test program being used). The relocatable address for routines SPCSADD, SPCSDAT, and SPCSANS are found in PR-1A504. To obtain the value of xxxxxxx, add the relocatable address for the appropriate routine to the absolute starting address of XBUS.

System response should be ØK.

(4) To start the off-line CC and execute program loop, type in

ØFL-MØDE-01.

System response should be ØK.

(5) To set the ØL3 flip-flop so that maintenance orders will be sent on the bus, type:

T-CPD-W000017W.

T-CPD-000017.

System response should be ØK.

(6) Scope the buses at the BTR, looking for the binary weighted bits shown in Table F for SP-CS address bus bits, Table D for SP-CS data bus bits, or Table E for SP-CS answer bus bits as selected. Also note any error conditions displayed on the scope (Fig. 3). When testing is completed on a bus, proceed to the next bus.

**Note:** To verify SP address bus bits 15, 16, and 17 on the SP CS address bus, the flush flip-flop must be set.

(7) To stop the off-line CC, type in:

ØFL-MØDE-02.

System response should be ØK.

(8) Repeat Steps 5 through 7 for final bus test.

(9) When all tests have been run, the off-line mode must be cleared and the equipment restored before proceeding to the next bus (0 or 1). Type in:

ØFL-MØDE-02.

ØFL-MØDE-03.

PS-RESTØRE-Syy.

(10) To terminate the off-line mode, type in:

CC-RESTØRE-.

CS-RESTØRE-CSxx.

xx = Member number of unit being restored

CS-RESTØRE-CBxx.

yy = Number (00 through 11) used to specify  
PS to be returned to service.

CS-RESTØRE-ASxx.

System response should be PF followed by DR01.

CS-RESTØRE-ABxx.

(11) Repeat Steps 1 through 10 for other CS  
bus (0 or 1).

TABLE C

CC-CS ADDRESS BUS BITS

CC-CS ADDRESS BUS 0 BIT	SCOPE SYNC ↓	BINARY WEIGHTS					
		32	16	8	4	2	1
0A00							
0A01							
0A02							
0A03							
0A04							
0A05							
0A06							
0A07							
0A08							
0A09							
0A10							
0A11							
0A12							
0A13							
0A14							
0A15							
0A16							
0A17							
0A18 (R)							
0A19 (W)							
0A20 (G)							
0A21 (H)							
0A22 (C)							
0A23 (P)							
0AS1A (S00)							
0AS1B (S02)							
0AS2 (S08)							

Note: Table C can be used for bus 1 if the bit identifiers are changed as follows:

- 1A000
- .
- .
- .
- 1AS1A (S01)
- 1AS1B (S03)
- 1AS2 (S09)

TABLE D

CC-CS OR SP-CS DATA BUS BITS

CC-CS OR SP-CS DATA BUS 0 BIT	SCOPE SYNC ↓	BINARY WEIGHTS						
		32	16	8	4	2	1	
0D00								
0D01								
0D02								
0D03								
0D04								
0D05								
0D06								
0D07								
0D08								
0D09								
0D10								
0D11								
0D12								
0D13								
0D14								
0D15								
0D16								
0D17								
0D18								
0D19								
0D20								
0D21								
0D22								
0D23 (P)	WAVEFORM DEPENDS ON CS ADDRESS							
0DSA (S04)								
0DSB (S06)								

Note: Table D can be used for bus 1 if the bit identifiers are changed as follows:

- 1D00
- .
- .
- .
- 1DSA (S05)
- 1DSA (S07)

TABLE E

CC-CS OR SP-CS ANSWER BUS BITS

CC-CS OR SP-CS ANSWER BUS 0 BIT	SCOPE SYNC ↓	BINARY WEIGHTS					
		32	16	8	4	2	1
0CS00							
0CS01							
0CS02							
0CS03							
0CS04							
0CS05							
0CS06							
0CS07							
0CS08							
0CS09							
0CS10							
0CS11							
0CS12							
0CS13							
0CS14							
0CS15							
0CS16							
0CS17							
0CS18							
0CS19							
0CS20							
0CS21							
0CS22							
0CS23	WAVEFORM DEPENDS ON CS ADDRESS						
0CSSYN							
0CSASW							

Note: Table E can be used for bus 1 if the bit identifiers are changed as follows:

- 1CS00
- .
- .
- .
- 1CSASW

TABLE F

SP-CS ADDRESS BUS BITS

SP-CS ADDRESS BUS 0 BIT	SCOPE SYNC ↓	BINARY WEIGHTS						
		32	16	8	4	2	1	
0A00								
0A01								
0A02								
0A03								
0A04								
0A05								
0A06								
0A07								
0A08								
0A09								
0A10								
0A11								
0A12								
0A13								
0A14								
0A15								
0A16								
0A17								
0A18 (R)								
0A19 (W)								
0A20 (G)								
0A21 (H)								
0A22 (C)								
0A23 (P)								
0AS1A (S00)								
0AS1B (S02)								
0AS2 (S08)								

Note: Table F can be used for bus 1 if the bit identifiers are changed as follows:

- 1A00
- .
- .
- 1AS1A (S01)
- 1AS1B (S03)
- 1AS2 (S09)

Call Store Bus Test D Level Interrupts

Note: Do not use the procedure in the following paragraph unless the call store bus test caused D level interrupts.

3.07 If D level interrupts occur during an off-line call store bus test, the trouble may be a 32K call store with a defective off-line cable receiver circuit pack that is picking up signals from the on-line bus. Cable receivers for both BUS 0 and Bus 1 are on the same circuit pack. Normally, one set of receivers will receive only from the off-line bus and the other set will receive only from

the on-line bus. If the off-line bus receiver picks up signals from the on-line receiver, diagnosis is difficult because D level interrupts will appear to be caused by random call stores or by random locations in a call store. To isolate the call store with the circuit pack that is causing the D level interrupts.

- (1) Disconnect the **off-line** address and data CAB cables from all call stores on the off-line bus. See the following chart for cable assignments on a 32K call store.

	BUS 0	BUS 1
ADDRESS	CAB-04	CAB-05
DATA	CAB-06	CAB-07

**Caution: Do not disconnect the on-line bus.**

- (2) Restart the off-line bus test program that experienced the interrupts. D level interrupts should not occur.
- (3) When the off-line bus test completes, reconnect the address and data bus cables to the first call store on the bus. Restart the off-line test program. If no D level interrupts occur, continue connecting call stores and rerunning the test until D level interrupts recur.
- (4) Check the cable receiver circuit packs in the last call store that was connected before the D level interrupts recurred.

#### B. Program Store Bus Test

**Note:** The following tests are run in the off-line mode. They do not require the library control program or any library input messages. The J1A064AA auxiliary program library **must** be in the PS that is to be taken off-line (PS 0 or PS 1). Also, CS 0 **must** be the off-line CS. Because the J1A064AA program library must be loaded into either PS 0 or PS 1, the following will apply:

- (1) In offices where PS 0 and PS 1 are not in the same bus community, these tests can be used to test either community A (if the J1A064AA program library is in PS 1 or community B (if the J1A064AA program library is in PS 0).

- (2) In offices where PS 0 and PS 1 are in the same bus community, these tests can be used to test only that bus community which services both PS 0 and PS 1. The other bus community must be tested by other off-line methods.

**3.08** To check bus connections during an office addition or to make a routine check of the PS address and answer buses, perform the following.

- (1) Type one of the following:

- (a) For offices with an SP, type in:

ØFL-CØNFIG-aabccd990.

- (b) For offices without an SP, type in:

ØFL-CØNFIG-aabccd.

aa = Number of PS containing program library.

b = PS bus (0 or 1)

cc = CS to be used off-line (either 00 or 01)

d = CS bus (0 or 1).

The system response should be PF followed by an ØL01 printout with information pertaining to the action performed.

- (2) To release the MAC scratch, type in:

ØFL-MØDE-05.

System response should be ØK.

- (3) Type in:

ØFL-EXEC-060xxxxxxx00000000.

xxxxxxx = PSADD for address of PS address bus

= PSANSA for address of PS answer bus (community A)

= PSANSB for address of PS answer bus (community B).

**Note:** The absolute starting address for XBUS within the Mod 5 test program is found in PK-1A002-50x (x is for the auxiliary test program being used). The relocatable address for routines PSADD, PSANSA, and PSANSB is found in PR-1A504. To obtain the value of xxxxxxx, add the relocatable address for the appropriate routine to the absolute starting address of XBUS.

System response should be ØK.

**Note:** The J1A064AA program library must be in proper PS for test of each community, that is, the one taken off-line.

- (4) To start the off-line CC and execute program loop, type in:

ØFL-MØDE-01.

System response should be ØK.

- (5) To set the ØL3 flip-flop so that maintenance orders will be sent on the bus, type:

T-CPD-W000017W.

System response should be ØK.

- (6) Scope the buses, looking for the binary weighted bits shown in Table G for PS address bus bits or Table H for PS answer bus bits as selected. Also note any error conditions displayed on the scope (Fig. 3). When the test is completed on a bus (address or answer bus), proceed to the next bus.

- (7) To stop the off-line CC, type in:

ØFL-MØDE-02.

System response should be ØK.

- (8) When all tests have been run, the off-line mode must be cleared and the equipment restored before proceeding to the next bus (0 or 1). Type in

ØFL-MØDE-02.

ØFL-MØDE-03.

System response should be ØK.

- (9) To terminate the off-line mode, type in:

CS-RESTØRE-CSxx.

CS-RESTØRE-CBxx.

PS-RESTØRE-Syy.

CC-RESTØRE-.

xx = Member number of unit being restored

yy = Number (00 through 11) used to specify PS to be returned to service.

System response should be PF followed by DR01.

- (10) Repeat Steps 1 through 9 for the other PS bus (0 or 1).

#### END PROCEDURE

**3.09** Configure the MOD 5 containing XBUS out of service, remove the PS module, and replace it with the original PS module 05, using procedures outlined in PA-1A500 or Section 231-147-301.

#### 4. ABBREVIATIONS

**4.01** The following abbreviations are used in this section.

APT	Auxiliary Program Telephone Co.
APW	Auxiliary Program Western Electric
BTR	Bus Terminating Resistor
CC	Central Control
CPD	Central Pulse Distributor
CS	Call Store
ESS	Electronic Switching System
MAC	Maintenance Control
MCC	Master Control Center
OS	Out of Service
PS	Program Store

TABLE G

PS ADDRESS BUS BITS

PS ADDRESS BUS BIT	SCOPE SYNC ↓	BINARY WEIGHTS					
		32	16	8	4	2	1
A 00							
A 01							
A 02							
A 03							
A 04							
A 05							
A 06							
A 07							
A 08							
A 09							
A 10							
A 11							
A 12							
A 13							
A 14							
A 15							
E 16							
E 17							
E 18							
E 19							
E 20							
E 21							
CW 22							
CM 23							
GM 24							
HM 25							
SYN 26							

Note: Bits 20 and 21 may appear as all 1s in some offices.

TABLE H  
PS ANSWER BUS BITS

PS ANSWER BUS BIT	SCOPE SYNC ↓	BINARY WEIGHTS						NOTES
		32	16	8	4	2	1	
S 00								1. Since pairs SYN and ASW have the same scope display, momentarily short the positive and negative lead of the pair (SYN or ASW) at the first PS on the bus. This will cause the pulses on the pair to disappear while it is shorted and to reappear when the short is removed.
S 01								
S 02								
S 03								
S 04								
S 05								
S 06								
S 07								
S 08								
S 09								
S 10								
S 11								
S 12								
S 13								
S 14								
S 15								
S 16								
S 17								
S 18								
S 19								
S 20								
S 21								
S 22								
S 23								
S 24								
S 25								
S 26								
S 27								
S 28								
S 29								
S 30								
S 31								
S 32								
S 33								
S 34								
S 35								
S 36								
S 37								
S 38								
S 39								
S 40								
S 41								
S 42								
S 43								
ASW 44								
SYN 45								

**SECTION 231-148-301**

PUA	Peripheral Unit Address	TTY	Teletypewriter
PUB	Peripheral Unit Bus	XBUS	Bus Testing Program
SP	Signal Processor		