UNIVERSAL CONTROLLER TEST PROCEDURES
2-WIRE NO. 1 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 This section gives procedures for using the universal controller test program (XCON) auxiliary program (part of MOD 5 auxiliary program package APT 07) for the 2-wire No. 1 Electronic Switching System (ESS). The program operates as a library program in program store (PS) module 05 of PS 0 (or MOD 15 of PS1) and requires that the special library mod be loaded as described in Section 231-147-301 or PA-1A500. The XCON program is covered in PR-1A553. This section applies to APT 07, Issue 1 and later.

1.02 Whenever this section is reissued, the reasons for reissue will be listed here.

1.03 Abbreviations used in this section are explained in Part 8.

2. DESCRIPTION

GENERAL TEST PROCEDURE FORMAT

2.01 Unlike other auxiliary test programs, the XCON program request procedure can be varied to tailor test operation as desired. XCON uses a general test format where input messages can be added or deleted.

2.02 There are five input messages available for use with XCON:

(a) Normal

(b) Range

(c) Octal

(d) Long-Binary

(e) Function

These inputs can be used separately or in combinations.

2.03 The test format is made up of a minimum of two lines typed in the following order:

LIB-STA-31uublle.

LIB-DEC-nnfemc.

where

uu (Unit Type) = 05 for MS
= 06 for CPD
= 12 for LS
= 13 for LSF
= 14 for LJF
= 15 for TJF
= 16 for TSF
= 17 for JS
= 18 for JSD
= 19 for UTS
= 20 for USD
= 21 for SSD

b (technology) = 0 if frames are new style (remreed or other 1A types).

= 1 if frames are old style).

c (client number) = 0 if a team is running XCON on only one frame

= 1 if a team is running XCON on two different frames at the same time

= 2 if a team is running XCON on three different frames at the same time

= 3, 4, 5, 6, or 7.

Note: Teams 1-7 need an off-line call store. See program XCTR for the required message.

nn = Network number (0 through 15) for network and line scanner frame only.

f = Frame number (0 through 7) for network and line scanner frame only.

nnf = Frame number (0 through 127) for signal distributor scanner, and central pulse distributor frames only.

e (enable option) = 0 for normal test

= 1 for EN00 only (controller 0, bus 0, CPD 0)

= 2 for EN01 only (controller 0, bus 1, CPD 1)

= 3 for EN10 only (controller 1, bus 0, CPD 1).

= 4 for EN11 only (controller 1, bus 1, CPD 0).

Note: With forced enables, XCON can not test on the network or signal distributor diagnostic bus. Placing and testing controllers on the diagnostic bus requires more than one enable.

ll = number of input lines which will be used after LIB-STA-message (Table A).

m = Active modes (Table A).

TABLE A
VARIABLES ll AND m

DESIRED OPERATION	ll	m
NORMAL	01	0
OCTAL	03	4
LONG-BINARY	05	2
FUNCTION	03	1
OCTAL, LONG-BINARY	07	6
OCTAL, FUNCTION	05	5
LONG-BINARY, FUNCTION	07	3
OCTAL, LONG-BINARY, FUNCTION	09	7
RANGE, NORMAL	02	0
RANGE, OCTAL	04	4
RANGE, LONG-BINARY	06	2
RANGE, FUNCTION	04	1
RANGE, OCTAL, LONG-BINARY	08	6
RANGE, OCTAL, FUNCTION	06	5
RANGE, LONG-BINARY, FUNCTION	08	3
RANGE, OCTAL, LONG-BINARY, FUNCTION	10	7

A. Normal Test

2.04 The normal test is used to throughly test, one at a time, any type of peripheral unit controller in an ESS office. The normal test is requested by typing in the two lines of general test procedure (paragraph 2.03) with the variables

ll = 01,

e = 0, and

m = 0

Note: No additional input lines are necessary when using the normal test.

2.05 When a normal test is performed on a frame, XCON sends out orders to the frame, scans the frame scan points, and verifies that the frame is functioning normally. The orders come from tables and subroutines which have been designed to test the frame for proper operation.

2.06 Within the XCON program is a simulated duplicate of the frame under test. During a normal test, XCON simply compares the results of the real frame with the simulated frame to determine a malfunction. It is important to note, however, that sending an invalid order to the frame does not result in a failure. For example, if an order with a missing PU bus bit is sent to a good frame, the frame will reject the order because it is invalid. The simulator will also reject the invalid order because it is acting like a good frame. Thus, the simulator and the real frame results will match and there is no failure. By definition, a failure in XCON can only occur when the real frame and the simulator results mismatch.

B. Optional Test

2.07 Any type of controller can be tested and debugged using the normal test procedure. However, if there is a special need to try something out on a frame or to see how a specific circuit works, the optional input messages can be used.

2.08 Input options make it possible to take as much control of the frame testing as desired. It is also possible to learn frame operation by observing the results of orders sent to the frame by various input options. To determine what particular orders can be sent by a particular option, it will be necessary to observe the data layouts for that option. Because of XCON built-in safety features, it is not necessary to worry about damaging the frame in any way.

2.09 There are four optional input messages.

(1) Range

(2) Octal

(3) Long-binary

(4) Function.

Any combination of 2 or more of the four messages can be requested by:

(1) Typing in the two lines of the general test procedure (paragraph 2.03) with the variables ll, e, and m equal to the appropriate values given in paragraph 2.03 and in Table A.

(2) Typing in each line of input for each option (given in paragraph 2.10, 2.11, 2.15, and 2.19).

Range Option

2.10 The range option is used to sequentially test more than one frame of a given type. If this option is used, testing will begin on the frame listed in the first input LIB-DEC- line, and end on the frame listed in the LIB-DEC- line given for the range input. The test results for each frame will be automatically printed. The range input is:

LIB-DEC-nnf0rc.

nn = Network number (0 through 15) for network and line scan frame only

f = Frame number (0 through 7) for network and line scan frame only

nnf = Frame number (0 through 127)

for signal distributor scanner, and central pulse distributor frames only.

r = 0, program prints passing or failing status for each frame

= 1, program prints detailed analysis of the first failure found in each frame

= 2, program stops on failures to allow normal troubleshooting for each frame.

c (Client number) = 0 if a team is running XCON on only one frame

= 1 if a team is running XCON on two different frames at the same time

= 2 if a team is running XCON on three different frames at the same time

= 3, 4, 5, 6, or 7.

Octal Option

2.11 The octal option allows the maintenance personnel to override all or portions of the normal test orders which are sent to a frame. This will allow maintenance personnel to test any level of any frame or controller. For example, maintenance personnel testing a JSF could force the program to test only grid 1 of the frame. If all the tests pass on grid 1, then the teletypewriter will print out CATP (conditional all tests pass) at the end of the testing.

2.12 The octal input is made up of two lines:

LIB-OCT-oooooooc.

LIB-OCT-mmmmmmmmc.

oooooooo = Octal order

mmmmmmmm = Octal mask

c (client number) = 0 if a team is running XCON on only one frame

= 1 if a team is running XCON on two different frames at the same time.

= 2 if a team is running XCON on three different frames at the same time

= 3, 4, 5, 6, or 7.

To determine the octal order see the data layout (Fig. 1) for the particular frame or controller under test.

NOTE: Data layouts are given in binary bits. It is necessary to convert the octal order or mask to binary before using data layout.

```
-------------------------------------------------------------------------------
DATA LAYOUTS FOR OCTAL ORDERS:  TSF/JSF                    SD-1A327/SD-1A328
                                                                  Bit Numbers
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   OG OG)(OG      )(        )(   GR GR)(S0 S0 S0)(L0 L0 L0)(S1 S1 S1)(L1 L1 L1)
                                                              Bit Designations
TEST ORDERS:  QUARANTINE=14001000, TPA=14002000, RELEASE=14003000, STG=14004000.
OG(TSF)=ORDER TYPE:  1=CONNECT, 3=TEST
OG(JSF)=ORDER TYPE:  0=REMOVE NT, 1=CONNECT, 2=CONN W/FCG, 3=TEST,
5=CONN VER(LP ST), 6=OPERATE NT, 7=CONN VER (GD ST)
GR=GRID   S0=STAGE 0 SWITCH   L0=STAGE 0 LEVEL   S1=STAGE 1 SWITCH
L1=STAGE 1 LEVEL
FST:  0=IDLE, 1=TPAQ, 2=RESET, 3=QUAR, 4=ENABLED, 5=TPA, 6=FCG(JSF ONLY),
7=POWER OFF
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
DATA LAYOUTS FOR OCTAL ORDERS:  2:1 LSF                    SD-1A325
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   OG OG)(OG      )(      S1)(S1 L1 L1)(      BY)(CN CN CN)(S0    S0)(S0 L0 L0)

TEST ORDERS:  QUARANTINE=14010000, TPA=14020000, RELEASE=14030000, STG=14040054
OG=ORDER TYPE:  1=CONN CO OPEN, 2=FCG, 3=TEST, 4=HI & DRY, 5=CONN CO CLOSED,
7=RESTORE (CO).
S1=STAGE 1 SWITCH   L1= STAGE 1 LEVEL  BY=BAY   CN=CONCENTRATOR
S0=STAGE 0 SWITCH   L0=STAGE 0 LEVEL
FST:  0=IDLE, 1=TPAQ, 2=RESET, 3=QUAR, 4=ENABLED, 5=TPA, 6=UNUSED, 7=POWER OFF
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
DATA LAYOUTS FOR OCTAL ORDERS:  4:1 LSF                    SD-1A326
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   OG OG)(OG      )(      S1)(S1 L1 L1)(      BY)(CN CN CN)(S0 S0 L0)(L0 L0 L0)

TEST ORDERS:  QUARANTINE=14000000, TPA=14000030, RELEASE=14000020, STG=14040054
OG=ORDER TYPE:  1=CONN CO OPEN, 2=FCG, 3=TEST, 4=HI & DRY, 5=CONN CO CLOSED,
7=RESTORE (CO).
S1=STAGE 1 SWITCH   L1=STAGE 1 LEVEL   BY=BAY (BAY 2 OF 4:1 LSF IS BY=1)
CN=CONCENTRATOR
S0=STAGE 0 SWITCH   L0=STAGE 0 LEVEL
FST:  0=IDLE, 1=TPAQ, 2=RESET, 3=QUAR, 4=ENABLED, 5=TPA, 6=UNUSED, 7=POWER OFF
-------------------------------------------------------------------------------
```

Fig. 1—Data Layouts for Octal Orders (Sheet 1)

```
DATA LAYOUTS FOR OCTAL ORDERS:  JSD/USD                    SD-1A216/338
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(        )(        )(        )(   OR BY)(HM HM HM)(HM VF VF)(CK RY RY)

OR=OPERATE(0)/RELEASE(1)
BY=BAY
HM=HORIZONTAL MOUNTING PLATE (0000=HMP 1,1111=HMP 16)
VF=VERTICAL FILE
CK=CIRCUIT (0=MLR A,B,OR C;1=MLR D,E,OR F)
RY=RELAY CHOICE (00=MLR A OR D,01=MLR B OR E,10=MLR C OR F)
FST:  0=IDLE, 1=QUAR, 2=UNUSED, 3=TPAQ, 4=ENABLED, 5=UNUSED, 6=TPA, 7=POWER OFF
```

```
DATA LAYOUTS FOR OCTAL ORDERS:  SSD                        SD-1A216/402
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(        )(        )(        )(   OR HA)(QD QD RW)(RW RW RW)(RW FD FD)
OR=OPERATE(0)/RELEASE(1)
HA=HALF   QD=QUAD   RW=ROW   FD=FIELD
FST:  0=IDLE, 1=QUAR, 2=UNUSED, 3=TPAQ, 4=ENABLE, 5=UNUSED, 6=TPA, 7=POWER OFF
```

```
DATA LAYOUTS FOR OCTAL ORDERS:  LS/JS/UTS/MS          SD-1A332 111 326
                                                      115/209/215
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(        )(        )(        )(      MS)(MS MS LS)(LS LS   )(        )

MS=MOST SIGNIFICANT ROW SELECT BITS  LS=LEAST SIGNIFICANT ROW SELECT BITS.
FST (MASTER SCANNER ONLY):  0=POWER ON (OLD), 3=POWER ON (NEW), 7=POWER OFF
```

```
DATA LAYOUTS FOR OCTAL ORDERS:  CPD                                SD-1A109
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(    G  G)( G  R  R)( R  C  C)( C      )(    H   )(        )(        )(        )

G=GROUP  R=ROW  C=COLUMN  H=HALF
```

```
DATA LAYOUT FOR OCTAL ORDERS:  CPD
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(    G  G)( G  R  R)( R  C  C)( C  N  N)( N  N  H)( W  0  0)( 0  0  0)( 0  0  0)

G=GROUP, R=ROW, C=COLUMN, N=CPD, NUMBER (0-17), H=HALF(0-1), W=WRM1(=0 NO,=1,YES)
```

Fig. 1—Data Layouts for Octal Orders (Sheet 2)

Example 1

2.13 To force grid 1 when testing a junctor switching frame (JSF), operation explained in paragraph 2.10, type in lines 3 and 4 shown below after typing in the two lines of general format:

LINE 3:

LIB-OCT-00010000c.

LINE 4:

LIB-OCT-00030000c.

To understand how lines 3 and 4 above will force the program to test only grid 1, substitute the lines 3 and 4 into the JSF data layout (Fig. 2). Only bit 12 is set in the octal order to select grid (GR) 1 (bit 13 on and bit 12 off would select grid 2). By setting bits 12 add 13 of line 4, the program is forced to look at only bits 12 and 13 of the order. This will force the program to test the grid selected in the octal order (line 3).

For the order:

Line 3 input = ØØØ1ØØØØ (octal)

After converting to binary,

Bit 23 Bit 22 Bit 12 Bit 3 Bit 0

Line 3 = 000000000001000000000000

(bit 23 is excluded before substitution into data layout)

For the mask:

Line 4 input = 00030000 (octal)

After converting to binary,

Line 4 = 000000000011000000000000

Bit 23 Bit 22 Bit 12 Bit 3 Bit 0

(bit 23 is excluded before substitution into data layout)

Substituton of lines 3 and 4 into data layout gives:

```
-------------------------------------------------------------------------------
DATA LAYOUTS FOR OCTAL ORDERS:  TSF/JSF                    SD-1A327/SD-1A328
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   OG OG)(OG      )(        )(   GR GR)(S0 S0 S0)(L0 L0 L0)(S1 S1 S1)(L1 L1 L1)

┌LINE 3                                                                  ORDER┐
└( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  1)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)┘
┌( 0  0  0)( 0  0  0)( 0  0  0)( 0  1  1)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)┐
└LINE 4                                                                   MASK┘

TEST ORDERS:  QUARANTINE=14001000, TPA=14002000, RELEASE=14003000, STG=14004000.
OG(TSF)=ORDER TYPE:  1=CONNECT, 3=TEST
OG(JSF)=ORDER TYPE:  0=REMOVE NT, 1=CONNECT, 2=CONN W/FCG, 3=TEST,
5=CONN VER(LP ST), 6=OPERATE NT, 7=CONN VER(GD ST)

GR=GRID  S0=STAGE 0 SWITCH    L0=STAGE 0 LEVEL   S1=STAGE 1 SWITCH

L1=STAGE 1 LEVEL
FST:  0=IDLE, 1=TPAQ, 2=RESET, 3=QUAR, 4=ENABLED, 5=TPA, 6=FCG(JSF ONLY),
7=POWER OFF
-------------------------------------------------------------------------------
```

Fig. 2—Substitution Into JSF Data Layout

Example 2

2.14 A JSF is being tested and maintenance personnel want to force the program to test only switch 3 of the stage 1 switches in each grid of the frame.

Line 3:

LIB-OCT-00000030c.

Line 4:

LIB-OCT-00000070c.

Example 3

2.15 A JSF is being tested and maintenance personnel want to force the program to test only switch 3 of the stage 1 switches in grid 1 only.

LINE 3:

LIB-OCT-00010030

LINE 4:

LIB-OCT-0030070

Long Binary Option

2.16 The long binary option, like the octal option, allows maintenance personnel to override all or portions of the normal test orders which are sent to a frame. This will allow maintenance personnel to test any part of any frame or controller. Long binary overrides have a higher priority than octal overrides. Thus, if the same frame information in both octal and long binary options is specified, the long binary will dominate.

2.17 The long binary input is made up of four lines:

LINE 3:

LIB-OCT-llllllllc.

LINE 4:

LIB-OCT-mmmmmmmmc.

LINE 5:

LIB-OCT-llllllllc.

LINE 6:

LIB-OCT-mmmmmmmmc.

llllllll = Line 3 long binary order bits 0 through 22

through 22

llllllll = Line 5 long binary order bits 23 through 45

through 45

2.18 To determine the long-binary order or mask, see the data layout (Fig. 3) for the particular frame or controller under test.

Note: Data layouts are given in binary bits. It is necessary to convert the long-binary order or mask to binary before using data layout.

Example 1

2.19 A TSF is being tested and maintenance personnel want to run the normal test only on input levels 1, 2, 5, and 6.

LINE 3:

LIB-OCT-00000000c.

LINE 4:

LIB-OCT-00000011c.

LINE 5:

LIB-OCT-00000000c.

LINE 6:

LIB-OCT-00000000c.

2.20 To understand how input levels 1, 2, 5, and 6 were selected from the input lines 3 through 6, observe the TSF data layout (Fig. 3). Since certain levels are being selected, all others must be masked out. This is why only mask bits (not order bits) are set. Figure 4 shows the substitution of line 4 into the TSF data layout.

Note: Before LINE 4 can be substituted into the data layout, it must first be converted from octal to binary. Since line 4 represents mask bits 0 through 22, only data bit representation for those bits are required in Figure 4.

2.21 To understand how setting bit 0 and bit 3 will allow the test to run on input levels 1,2, 5, and 6, there must be an understanding of what program bits (Fig. 5) are normally set with a mask of all 0s (line 4 bits all set to 0).

2.22 Figure 5 shows the program bit layout with a mask of all zeros. Normally, each level that contains a 1 will be tested by the normal test program when the appropriate high order bit contains a 1. Therefore, each level 0 through 7 will be tested if the bits 0 through 3 and 16 and 17 are not set to 1s in the data layout.

```
-------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  TSF                    SD-1A327
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(      3H)(3H 2H 2H)(1H 1H 4L)(4L 4L 4L)(3L 3L 3L)(3L 2L 2L)(2L 2L 1L)(1L 1L 1L)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(         )(         )(         )(      6H)(6H 6L 6L)(6L 6L 5H)(5H 5L 5L)(4H 4H   )

H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP 1 = INPUT LEVEL
GROUP 2 = OUTPUT LEVEL (EVEN GRID), = OUTPUT SWITCH (ODD GRID)
GROUP 3 = INPUT SWITCH
GROUP 4 = OUTPUT SWITCH (EVEN GRID), = OUTPUT LEVEL (ODD GRID)
GROUP 5 = GRID
GROUP 6 = ORDER TYPE
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  TJF/LJF                SD-1A328
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(      3H)(3H 2H 2H)(1H 1H 4L)(4L 4L 4L)(3L 3L 3L)(3L 2L 2L)(2L 2L 1L)(1L 1L 1L)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(         )(         )(         )(      6H)(6H 6L 6L)(6L 6L 5H)(5H 5L 5L)(4H 4H   )

H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP 1 = INPUT LEVEL
GROUP 2 = OUTPUT LEVEL (EVEN GRID), = OUTPUT SWITCH (ODD GRID)
GROUP 3 = INPUT SWITCH
GROUP 4 = OUTPUT SWITCH (EVEN GRID), = OUTPUT LEVEL (ODD GRID)
GROUP 5 = GRID
GROUP 6 = ORDER TYPE
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  2:1 LSF                SD-1A325
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   3H 3H)(3H 3L 3L)(3L 3L 2H)(2H 2H 2H)(2L 2L 2L)(2L 1H 1H)(1H 1H 1L)(1L 1L 1L)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(         )(         )(         )(      6H)(6H 6L 6L)(6L 6L 5L)(5L       )(      3H)

H SUFFIX= HIGH ORDER 1-OUR-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP 1L = STAGE 0 LEVEL
GROUP 1H = CONCENTRATOR PAIR (0 OR 4, 1 OR 5, 2 OR 6, 3 OR 7)
GROUP 2L = STAGE 0 SWITCH PAIR (0 OR 4, 1 OR 5, 2 OR 6, 3 OR 7)
GROUP 2H = CONCENTRATOR & STAGE 0 SWITCH PAIR SELECT:
           (CON 4-7 & S0 0-3, CON 0-3 & S0 4-7, CON 4-7 & S0 0-3,
           CON 4-7 & S0 4-7)
GROUP 3L = STAGE 1 LEVEL
```

Fig. 3—Data Layouts for Long-Binary Orders (Sheet 1)

```
2:1 LSF DATA LAYOUT (Contd)

GROUP 3H = STAGE 1 SWITCH
GROUP 5  = HOME/MATE CONCENTRATOR SELECT
GROUP 6  = ORDER TYPE
--------------------------------------------------------------------------------

--------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  4:1 LSF              SD-1A326
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   3H 3H)(3H 3L 3L)(3L 3L 2H)(2H 2H 2H)(2L 2L 2L)(2L 1H 1H)(1H 1H 1L)(1L 1L 1L)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(        )(        )(        )(      6H)(6H 6L 6L)(6L 6L 5L)(5L 4L 4L)(4L 4L 3H)

H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP 1 = INPUT LEVEL
GROUP 2 = OUTPUT LEVEL
GROUP 3 = INPUT SWITCH HALF
GROUP 4 = CONCENTRATOR
GROUP 5 = HOME/MATE CONCENTRATOR SELECT
GROUP 6 = ORDER TYPE
--------------------------------------------------------------------------------

--------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  JSD/USD/SSD          SD-1A216/338/402
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   DL DL)(DL CL CL)(EL EL AL)(AL AL AL)(AL AL AL)(AL BL BL)(BL BL BL)(BL BL BL)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(        )(        )(        )(        )(        )(        )(   TL TL)(HL HL DL)

TEST ORDERS:  QUARANTINE=00000020(45-23),05200401(22-00)
                    TPA=00000020(45-23),11200401(22-00)
              RELEASE=00000020(45-23),21200401(22-00)
H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP A = 1/8 CONTACT SELECT
GROUP B = 1/8 CONTACT SELECT
GROUP C = 1/2 CONTACT SELECT
GROUP D = 1/4 CONTACT SELECT
GROUP E = OPERATE/RELEASE
GROUP H = BAY SELECT
GROUP T = ORDER TYPE
--------------------------------------------------------------------------------
```

Fig. 3—Data Layouts for Long-Binary Orders (Sheet 2)

```
-------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  LS/JS/UTS/MS          SD-1A332/111/326/115/
                                                            209/215
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(         )(   3L 2L)(2L 2L 2L)(2L 2L 2L)(2L 1L 1L)(1L 1L 1L)(1L 1L 1L)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(         )(         )(         )(         )(         )(         )(         )

H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP 1 = 1/8 ROW SELECT
GROUP 2 = 1/8 ROW SELECT
GROUP 3 = MAINTENANCE TEST ORDER BIT
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
DATA LAYOUTS FOR LONG-BINARY ORDERS:  CPD                   SD-1A109
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(         )( R  T  B)( B  B  B)( B  B  B)( B  A  A)( A  A  A)( A  A  A)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(         )(         )(       C)( C  C  C)( C  C  C)( C  C  C)( C  C  C)( C  C  C)

GROUP A=1/8 GROUP SELECT
GROUP B=1/8 ROW SELECT
GROUP C=1/16 COLUMN SELECT
      T=MAINTENANCE TEST ORDER BIT
      R=MAINTENANCE RESET BIT
-------------------------------------------------------------------------------
```

Fig. 3—Data Layouts for Long-Binary Orders (Sheet 3)

```
LINE 4 INPUT = 00000011      (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 4  =  000000000000000000001001
          /   \         |     |   \
       bit 23 bit 22 bit 10 bit 3 bit 0

(BIT 23 IS EXCLUDED BEFORE SUBSTITUTION INTO DATA LAYOUT  (BELOW)
```

```
DATA LAYOUTS FOR LONG-BINARY ORDERS:  TSF                    SD-1A327
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(      3H)(3H 2H 2H)(1H 1H 4L)(4L 4L 4L)(3L 3L 3L)(3L 2L 2L)(2L 2L 1L)(1L 1L 1L)
LINE 4
(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  1)( 0  0  1)
```

BIT 3 AND BIT 0 ARE BOTH LOW ORDER AND GROUP 1 BITS.

H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N GROUP BITS.

GROUP 1 = INPUT LEVEL

GROUP 2 = OUTPUT LEVEL (EVEN GRID), = OUTPUT SWITCH (ODD GRID)
GROUP 3 = INPUT SWITCH
GROUP 4 = OUTPUT SWITCH (EVEN GRID), = OUTPUT LEVEL (ODD GRID)
GROUP 5 = GRID
GROUP 6 = ORDER TYPE

Fig. 4—Substitution Into TSF Data Layout

2.23 Figure 6 shows the same program bit layout with a mask of bit 0 and bit 3 set in the data layout. In this case, levels 0 and 4 are masked out due to the set bit 0 in the data layout. Levels 3 and 7 are masked due to the set bit 3 in the data layout. As a result, only the levels which still contain an unmasked 1 in the program bit layout will be checked.

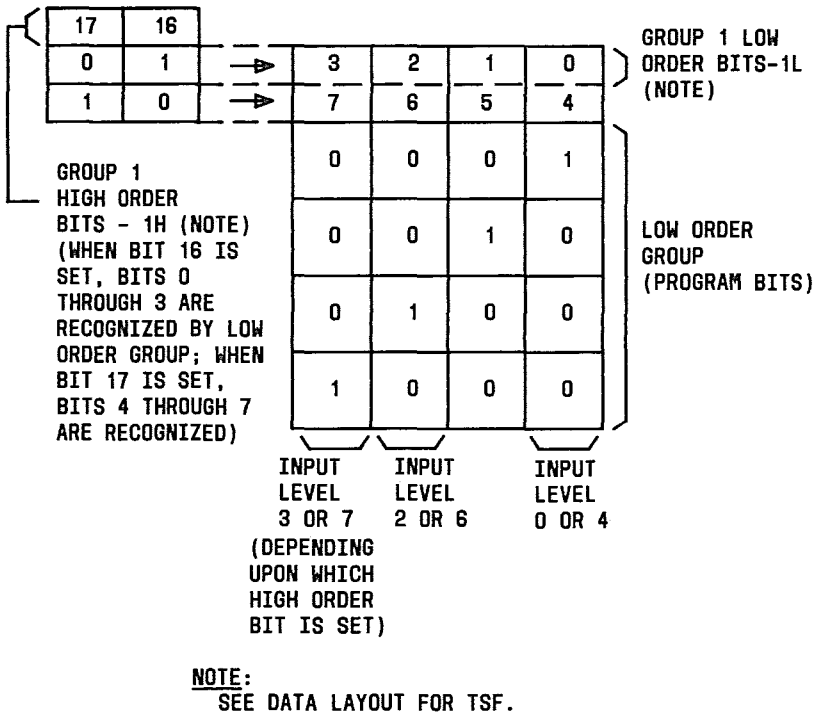


Fig. 5—Program Bit Layout (Mask of All Zeros)

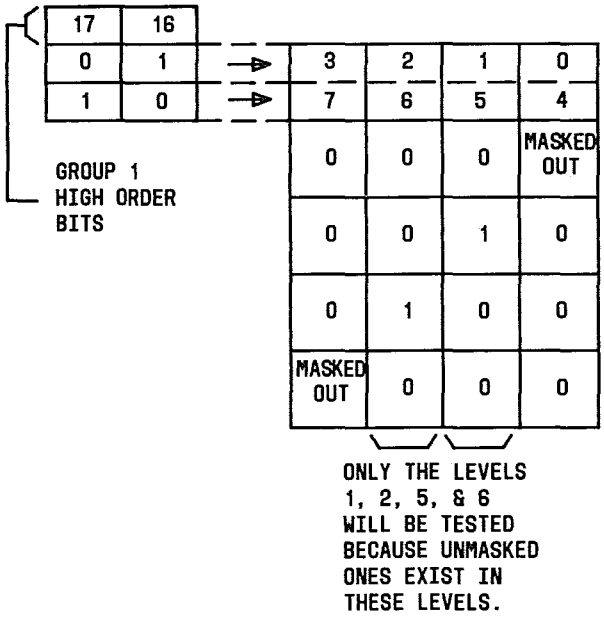


Fig. 6—Program Bit Layout (Mask of 0 and 3)

Example 2

2.24 Assume a supplementary signal distributor (SSD) is being tested and maintenance orders are to be inhibited.

LINE 3:

LIB-OCT-0000000c.

LINE 4:

LIB-OCT-00000000c.

LINE 5:

LIB-OCT-00000010c.

LINE 6:

LIB-OCT-00000030c.

2.25 To inhibit maintenance orders, set the order (00000010) in line 5 and the mask (00000030) in line 6. The binary mask (000000000000000000011000)

allows the program to see the order bits (00000000000000000001000) in line 5. Bit 27 in the order is 1 and bit 26 is 0. Bit 27, since it is set, forces a test using normal orders on the SSD frame. Bit 26, since it is 0, inhibits the maintenance orders.

2.26 To understand how maintenance orders are inhibited, substitute the input lines into the SSD data layout (Fig. 7). To inhibit maintenance orders, the normal orders have to be forced. This is why, in Fig. 7, bit 26 (normal orders bit) is set. By setting bits 26 and 27 of the mask (line 6), the program is forced to look at only bits 26 and 27 of the order (line 5). Bit 26 and bit 27 are the normal order and maintenance order bits, respectively.

```
LINE 5 INPUT = 00000010  (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 5 = 000000000000000000001000
          \                  /  \
       bit 46          bit 26  bit 23

(BIT 46 IS EXCLUDED)

LINE 6 INPUT = 00000030  (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 6 = 000000000000000000011000
                          /    \
                     bit 26  bit 23
```

SUBSTITUTION OF LINES 5 AND 6 INTO DATA LAYOUT FOR BITS 23 THROUGH 45 GIVES:

```
DATA LAYOUTS FOR LONG-BINARY ORDERS:  JSD/USD/SSD          SD-1A216/338/402
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(   DL DL)(DL CL CL)(EL EL AL)(AL AL AL)(AL AL AL)(AL BL BL)(BL BL BL)(BL BL BL)

(   45 44)(43 42 41)(40 39 38)(37 36 35)(34 33 32)(31 30 29)(28 27 26)(25 24 23)
(       )(       )(       )(       )(       )(       )(   TL TL)(HL HL DL)
[LINE 5                                                                ORDER]
[(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  1)( 0  0  0)]
[(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  1  1)( 0  0  0)]
[LINE 6                                                                MASK]
```

```
TEST ORDERS:  QUARANTINE=00000020(45-23),05200401(22-00)
                    TPA=00000020(45-20),11200401(22-00)
              RELEASE=00000020(45-23),21200401(22-00)
H SUFFIX= HIGH ORDER 1-OUT-OF-N GROUP BITS, L SUFFIX= LOW ORDER 1-OUT-OF-N
GROUP BITS.
GROUP A = 1/8 CONTACT SELECT
GROUP B = 1/8 CONTACT SELECT
GROUP C = 1/2 CONTACT SELECT
GROUP D = 1/4 CONTACT SELECT
GROUP E = OPERATE/RELEASE
GROUP H = BAY SELECT
GROUP T = ORDER TYPE (BIT 26 SET = NORMAL ORDERS; BIT 27 SET = MTCE ORDERS)
```

Fig. 7—Substitution Into SSD Data Layout

2.27 To summarize:

(a) Both normal orders and maintenance orders are masked in Line 6.

(b) The maintenance orders are inhibited so that the program is forced to test the frame using only normal orders (line 5).

Function Option

2.28 The function option allows maintenance personnel to override all or portions of the normal testing functions. Function overrides have a higher priority that long-binary and octal overrides. Thus, if similar frame information is specified in function, long binary, and octal, the function overrides will dominate. As in all XCON input options, the function order bits are only active where you set the mask bits to 1.

2.29 The function input is made up of two lines:

LINE 3:

LIB-OCT-ffffffffc

LINE 4:

LIB-OCT-mmmmmmmmc.

ffffffff = Function data

mmmmmmmm = Function mask.

2.30 To determine the function order or mask, see the data layout (Fig. 8) for the particular frame or controller under test.

Note: Data layouts are given in binary bits. It is necessary to convert the function order or mask to binary before using data layout.

```
DATA LAYOUTS FOR FUNCTION DATA:  TSF/JSF                    SD-1A327/SD-1A328
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-03, 01=PUB 04-07,02=PUB 08-11,03=PUB 12-15,04=PUB 16-17,
     05=PUB 18-19, 06=PUB 20-21,07=PUB 24-25,10=PUB 26-27,11=PUB 28-29,
     12=PUB 30-33, 13=PUB 34-35.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

```
DATA LAYOUTS FOR FUNCTION DATA:  2:1 LSF                    SD-1A325
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-03,01=PUB 04-07,02=PUB 08-11,03=PUB 12-15,04= PUB 16-19,
     05=PUB 20-23,06=PUB 28-29,07=PUB 30-33,10=PUB 34-35,
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

```
DATA LAYOUTS FOR FUNCTION DATA:  4:1 LSF                    SD-1A326
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-03,01=PUB 04-07,02=PUB 08-11,03=PUB 12-15,04=PUB 16-19,
     05=PUB 20-23,06=PUB 24-27,07=PUB 28-29,10=PUB 30-33,11=PUB 34-35.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

Fig. 8—Data Layout for Function Orders (Sheet 1)

```
DATA LAYOUTS FOR FUNCTION DATA:  JSD/USD/SSD                SD-1A216/338/402
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(CP CO BU)(EV HM  I)(         )(         )(         )( B     A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-07,01=PUB 08-15,02=PUB 18-19,03=PUB 20-23,04=PUB 16-17,
     05=PUB 24-25.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
I  = 0 TO SELECT ONLY SD BASIC CONTACTS,=1 TO SELECT ONLY SD EXTENDED CONTACTS
HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

```
DATA LAYOUTS FOR FUNCTION DATA:  LS/JS/UTS/MS       SD-1A332 111 326 115/209/215
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(CP CO BU)(EV      )(         )(         )(         )( B     A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-07,01=PUB 08-15.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

```
DATA LAYOUTS FOR FUNCTION DATA:  CPD                        SD-1A109
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(CP CO BU)(       )(         )(         )(         )( B  G  A)( A  A  A)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=CAB 00-07,01=CAB 08-15,02=CAB 16-31.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.
G  = 0 TO SELECT CPD NORMAL MODE,=1 TO SELECT CPD INHIBIT MODE.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

Fig. 8—Data Layout for Function Orders (Sheet 2)

Example 1

2.31 Assume that all less-than group checks are to be inhibited on a frame.

LINE 3:

LIB-OCT-00000040c

LINE 4:

LIB-OCT-00000040c

2.32 To inhibit less-than group checks, set the order (00000040) in line 3 and the mask (00000040) in line 4. The binary mask (0...0100000) allows the program to see the order bit (0...0100000) in line 3. Bit 5 in the order is 1. Since bit 5 is set, more-than group checks are forced, inhibiting less-than group checks.

2.33 To understand how less-than group checks are inhibited, substitute the input lines into any of the function option data layouts (Fig. 9). In order to inhibit less-than group checks, more-than group checks must be forced.

```
LINE 3 INPUT = 00000040   (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 3 = 000000000000000000100000
          \                  \   \
     bit 23                bit 5 bit 0
    (excluded)

LINE 4 INPUT = 00000040   (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 4 = 000000000000000000100000
          \                  \   \
     bit 23                bit 5 bit 0
    (excluded)
```

SUBSTITUTION OF LINES 3 AND 4 INTO DATA LAYOUT GIVES:

```
DATA LAYOUTS FOR FUNCTION DATA:  TSF/JSF                    SD-1A327/SD-1A328
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)
LINE 3                                                                    ORDER
(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 1  0  0)( 0  0  0)
(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 1  0  0)( 0  0  0)
LINE 4                                                                    MASK
```

A = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED.)
00=PUB 00-03,01=PUB 04-07,02=PUB 08-11,03=PUB 12-15,04=PUB 16-17,
05=PUB 18-19,06=PUB 20-21,07=PUB 24-25,10=PUB 26-27,11=PUB 28-29,
12=PUB 30-33,13=PUB 34-35.

B = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.

HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.

Fig. 9—Substitution Into Functional Option Data Layout for Example 1

2.34 This is why the order bit 5 is set in Figure 9. By setting bit 5 of the mask, the program is forced to look at the order bit 5. If the order bit 5 is set to 1, then more-than group checks are forced (inhibiting less-than group checks). If 5 is set to 0, then less-than group checks are forced (inhibiting more-than group checks).

Example 2

2.35 Assume that a less-than group check in PUB bits 4-7 is to be forced on a 4:1 line switch frame (LSF).

LINE 3:

LIB-OCT-00000001c.

LINE 4:

LIB-OCT-00000057c.

2.36 To understand how a less-than group check in PUB bits 04-07 is to be forced, substitute the input lines into the LSF data layout (Fig 10).

```
LINE 3 INPUT = 00000001    (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 3 = 000000000000000000000001
          /                 /    \
  bit 23 (excluded)    bit 5   bit 0

LINE 4 INPUT = 00000057    (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 4 = 000000000000000000101111
          /                 /    \
  bit 23 (excluded)    bit 5   bit 0

SUBSTITUTION INTO DATA LAYOUT GIVES:
```

```
DATA LAYOUTS FOR FUNCTION DATA:  2:1 LSF                    SD-1A325
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(        )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)
┌LINE 3                                                                 ORDER┐
└(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  1)┘
┌(    0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 1  0  1)( 1  1  1)┐
└LINE 4                                                                 MASK┘
```

A = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED)

00=PUB 00-03,01=PUB 04-07, 02=PUB 08-11,03=PUB 12-15,04=PUB 16-19,
05=PUB 20-23,06=PUB 28-29,07=PUB 30-33,10=PUB 34-35.

B = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP-CHECKS.

HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.
EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.
BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.
CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.

Fig. 10—Substitution Into LSF Data Layout

Example 3

2.37 Assume that mate orders are only going to be sent using PU BUS 0 (on any frame).

LINE 3:

LIB-OCT-00200000c.

LINE 4:

LIB-OCT-01200000c.

2.38 To understand how mate orders are going to be sent on PU BUS 0 only, substitute the input lines into any one of the function data layouts (Fig. 11).

```
LINE 3 INPUT = 00200000     (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 3 = 00000001000000000000000
          /                 /   \
  bit 23 (excluded)    bit 5   bit 0

LINE 4 INPUT = 01200000     (OCTAL)
AFTER CONVERTING TO BINARY,
LINE 4 = 00000101000000000000000
          /                 /   \
  bit 23 (excluded)    bit 5   bit 0

SUBSTITUTION INTO DATA LAYOUT GIVES:
```

```
DATA LAYOUTS FOR FUNCTION DATA:  TSF/JSF                    SD-1A327/SD-1A328
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(         )(CP CO BU)(EV HM   )(        )(        )(        )( B     A)( A  A  A)

(    0  0)( 0  0  0)( 0  1  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)
(    0  0)( 0  0  1)( 0  1  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)( 0  0  0)

A  = GROUP-CHECK SELECT INDEX (SELECTS PU BITS TO BE GROUP-CHECKED).
     00=PUB 00-03,01=PUB 04-07,02=PUB 08-11,03=PUB 12-15,04=PUB 16-17,
     05=PUB 18-19,06=PUB 20-21,07=PUB 24-25,10=PUB 26-27,12=PUB 30-33,
     13=PUB 34-35.
B  = 0 TO FORCE LESS-THAN GROUP-CHECKS,=1 TO FORCE MORE-THAN GROUP CHECKS.

HM = 0 TO SELECT ONLY HOME ORDERS,=1 TO SELECT MATE ORDERS.

EV = 0 TO SELECT ENABLE-VERIFY,=1 TO INHIBIT ENABLE-VERIFY.

BU = 0 TO SELECT BUS 0,=1 TO SELECT BUS 1.

CO = 0 TO SELECT CONTROLLER 0,=1 TO SELECT CONTROLLER 1.
CP = 0 TO SELECT EVEN CPD OF PAIR,=1 TO SELECT ODD CPD OF PAIR.
```

Fig. 11—Substitution Into Option Data Layout for Example 3

TROUBLESHOOTING OPTIONS

2.39 The troubleshooting options allow the user to take control of the program operation. One or more of these options can be typed in before the program has started testing, during testing, or after a failure has occurred. They can be typed with any input (normal or optional inputs) or any combination of inputs. Table B gives a list of all the troubleshooting options available for use with XCON.

Example 1

2.40 The test has not yet started and the following message is typed in:

LIB-STA-3116003c. Tests TSF 00.

LIB-SET-100c. Loop option.

LIB-DEC-00004c. Select octal option.

LIB-OCT-04005523c. Octal order.

LIB-OCT-37777777c. Octal mask.

The program will interpret this as a request to loop continuously on octal order 04005523.

Example 2

2.41 The test is running and the following troubleshooting option is typed:

LIB-SET-100c.

The program will interpret this as a request to stop the test and loop on the last order sent to the frame.

Example 3

2.42 The test has stopped on a failure and the following is typed:

LIB-SET-100c.

The program will interpret this as a request to loop on the failing order.

BUS TESTING

A. Bus Isolation

2.43 Bus testing normally should be done on the standby or inactive bus. This minimizes the chance of system problems and also provides a better scope trace since the bus being observed will be free of system activity.

2.44 The bus isolation procedure is covered in paragraph 5.01.

B. Peripheral Unit Address Bus Test

2.45 The peripheral unit address bus (PUAB) test sends a binary weighted pattern out on each bus lead (Fig. 12). The pattern, given in figure 12, originates in the active central control (CC) and is transmitted to all formats of the bus. The scope sync is obtained on PUAB bit 0.

C. Central Pulse Distributor Address Bus Test

2.46 The central pulse distributor (CPD) address bus test sends a binary weighted pattern out on each bus lead (Fig. 13). The pattern, given in figure 13, originates in the active CC and is transmitted to all fanouts of the CPD address bus. The scope sync is obtained on CPD address bus 0. Also, the selected CPD gets enabled so enable-window timing can be performed.

D. Peripheral Unit Reply Bus Test

2.47 The peripheral unit reply bus test sends a binary weighted pattern out on each bus lead. The pattern, Fig. 14, originates in the active CC and is transmitted on the PUAB to the CPD, then loops around into the scanner answer bus via the address bus loop-around circuit. It then returns to the CC. None of the scanner answer bus fan-ins are tested since they cannot be activated by program control. Only the main leg of the scanner answer bus from the CPD to the CC is used. Scope sync is obtained on C10 or C11 (group 0, row 5, column 6 or 7) of the CPD associated with the frame under test.

TABLE B

TROUBLESHOOTING OPTIONS

OPTION	EXPLANATION OF OPTION
LIB-SET-100c.	Loop continuously.
LIB-SET-101c.	Send order to frame, scan results and print.
LIB-SET-102c.	Scan frame and print results.
LIB-SET-103c.	Retest controller.
LIB-SET-104c.	Retest frame.
LIB-SET-105c.	Continue testing.
LIB-SET-106c.	Retry order (print PASSING, FAILING or INTERMITTENT).
LIB-SET-107c.	Perform detailed analysis and print.
LIB-SET-108c.	Suspend testing.
LIB-SET-109c.	Intermittent order trap. Loop continuously but stop and perform detailed analysis, if an intermittent failure occurs.
LIB-SET-110c.	Put controller on diagnostic bus (network or signal distribution frames), and set SIG flip-flop (network frames).
LIB-SET-111c.	Remove controller from diagnostic bus (network and signal distributor frames), and reset STG flip-flop (network frames).
LIB-SET-112c.	Intermittent order bypass. Continue testing, print all intermittent orders and stop only on hard faults.
LIB-SET-113c.	Print program status.
LIB-SET-114c.	Begin bipolar pulse testing. (See utility tests.)
LIB-SET-115c.	Alternately inhibit or restore enable-verify (F-level) from frame under test.
LIB-SET-116c.	Begin unipolar enable testing. (See utility tests.)
LIB-SET-117c.	Begin peripheral unit address bus testing. (See bus tests.)
LIB-SET-118c.	Begin central pulse distributor address bus testing. (See bus tests.)
LIB-SET-119c.	Begin peripheral unit reply bus testing. (See bus tests.)
LIB-SET-122c.	Abort test program.

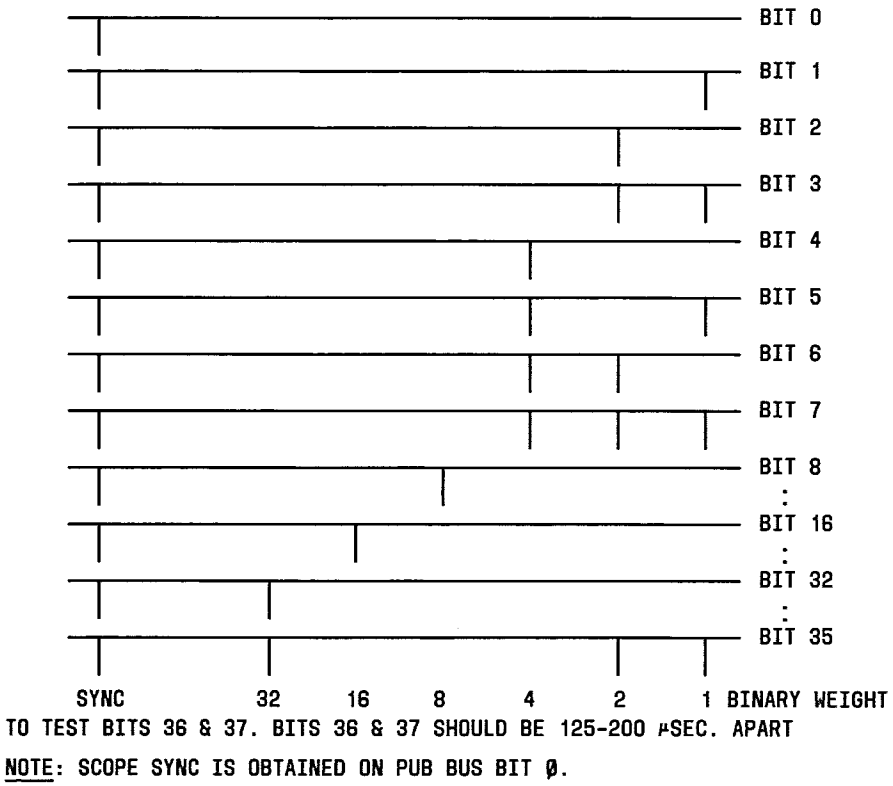


Fig. 12—PUB Binary Weight Pattern

UTILITY TESTS

A. Unipolar Enable Test

2.48 The unipolar enable test sends an enable pattern out on each enable lead (Fig. 15). The unipolar enable test is requested by typing in the two lines of general test procedure (paragraph 2) plus three additional lines of input. The unipolar enable CPD data layout is shown in Fig. 16.

B. Bipolar Pulse Test

2.49 The bipolar pulse test is designed to test CPD bipolar points. It sends a pulse pattern out on the P and N leads of a frame (Fig. 17). The bipolar pulse test is requested by typing in the two lines of general test procedure (paragraph 2), plus three additional lines of input.

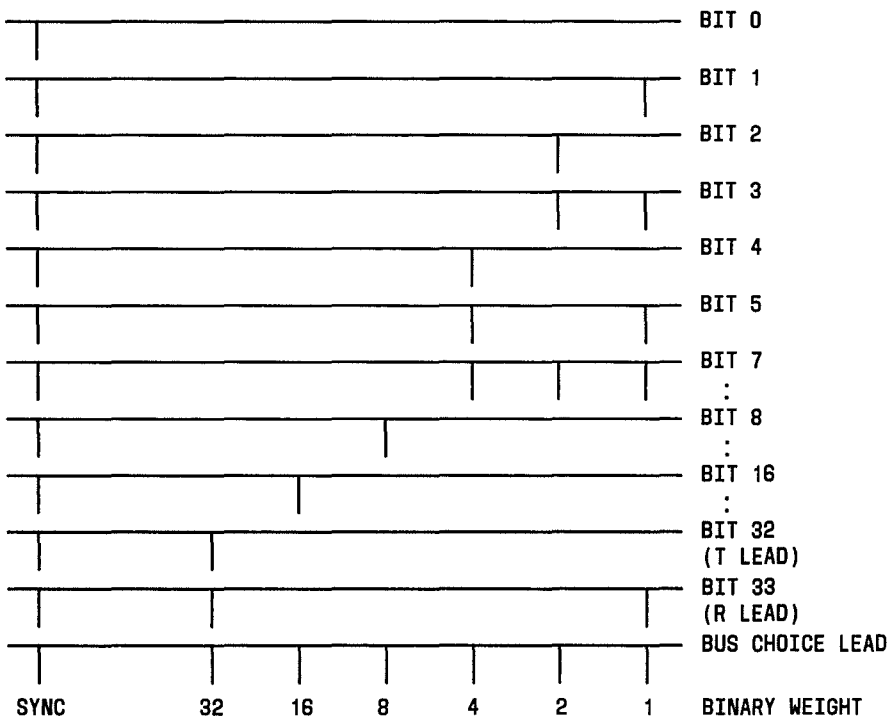
3. PRELIMINARY PROCEDURE

3.01 ***Loading and Configuring:*** Program store (PS) module 05 or 15 must be loaded with the proper auxiliary program package; therefore, before running XCON, perform the preliminary procedures in Section 231-147-301 or in PA-1A500 for inserting an auxiliary test module, configuring auxiliary test programs into service,and using the LIB-EDIT-message.

3.02 If the RC-UPDATE message has not already been typed in as part of the translation update (card writing) procedure, type in

RC-UPDATE-.

This consolidates the recent change area and insures that maximum size of the recent change auxiliary area available for use by XCON.



NOTE: SCOPE SYNC IS OBTAINED ON CPD ADDRESS BUS BIT 0.

Fig. 13—CPD Address Bus Binary Weight Pattern

4. CONTROLLER TEST PROCEDURE

Note: It is necessary to perform the preliminary procedure before performing the controller test procedure.

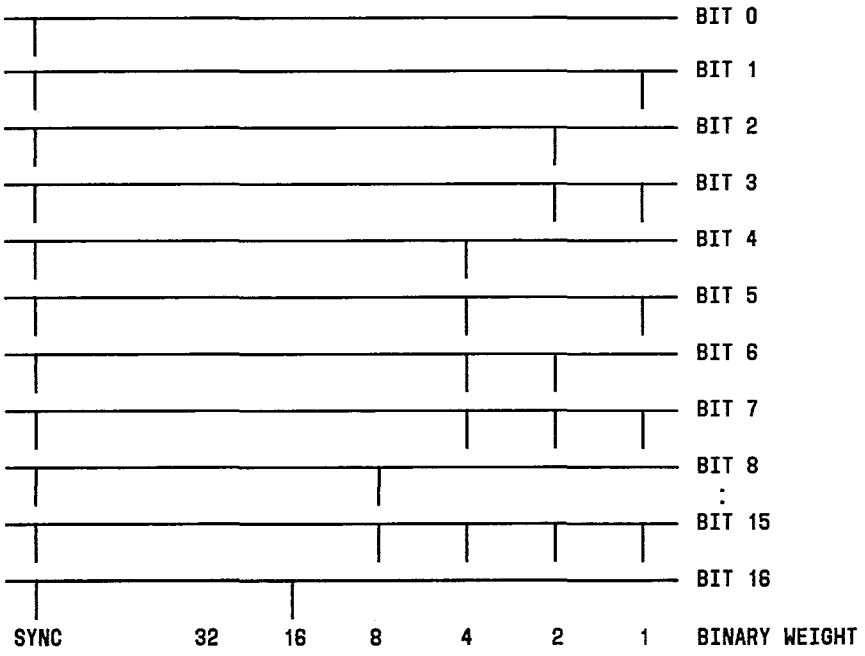
4.01 To test a frame using XCON, all that is ever needed is the normal test input. To perform the normal test, type

LIB-STA-31uub01c.

LIB-DEC-nnf00c.

uu (unit type) = 05 for MS
= 06 for CPD
= 12 for LS
= 13 for LSF
= 14 for LJF
= 15 for TJF
= 16 for TSF
= 17 for JS
= 18 for JSD
= 19 for UTS
= 20 for USD
= 21 for SSD

b (technology) = 0 if frames are new style (remreed or other 1A types)
= 1 if frames are old style.



NOTE: SCOPE SYNC IS OBTAINED ON C10 OR C11 (GROUP 0, ROW 5, COLUMN 6 OR 7) OR CPD ASSOCIATED WITH THE FRAME UNDER TEST.

Fig. 14—Peripheral Unit Reply Bus Binary Weight Pattern

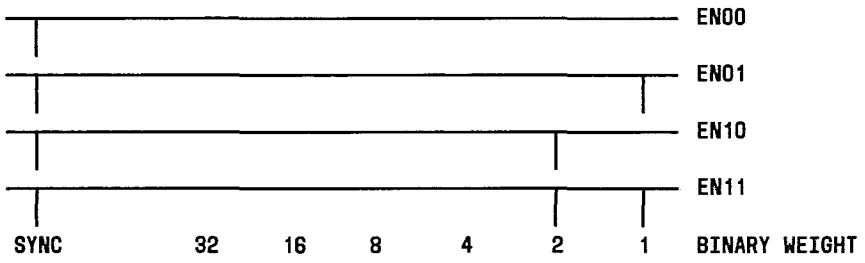


Fig. 15—Unipolar Enable Pattern

c (client number) = 0 if a team is running XCON on only one frame

= 1 if a team is running XCON on two different frames at the same time

= 2 if a team is running XCON on three different frames at the same time

= 3, 4, 5, 6, or 7

nn = Network number (0 through 15) for network and line scanner frame only

Number 16

```
-------------------------------------------------------------------------------
DATA LAYOUT FOR OCTAL ORDERS:  CPD
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(    G  G)( G  R  R)( R  C  C)( C  N  N)( N  N  H)( W  0  0)( 0  0  0)( 0  0  0)

G=GROUP, R=ROW, C=COLUMN, N=CPD NUMBER (0-17), H=HALF(0-1), W=WRMI (=0 NO, =1 YES)
-------------------------------------------------------------------------------
```

Fig. 16—Unipolar Enable CPD Data Layout

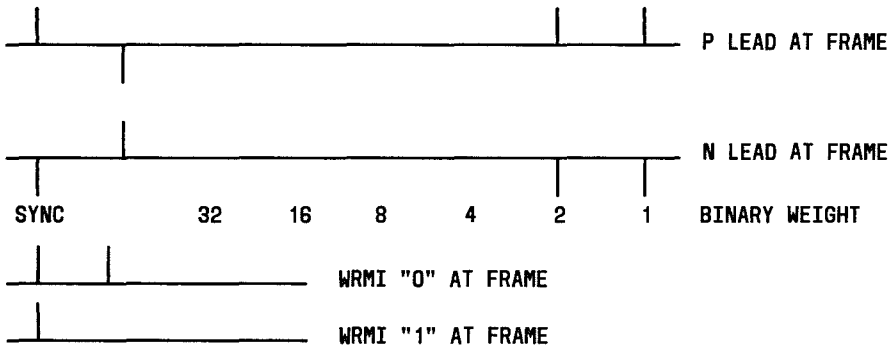


Fig. 17—Bipolar Pulse Test Pattern

f = Frame number (0 through 7) for network and line scanner frame only

nnf = Frame number (0 throuh 127) for signal distributor, scanner, and central pulse distributor frames only.

4.02 If the normal test on the chosen frame passes, the machine will print an all tests pass (ATP) message. If the frame fails to pass the normal test, maintenance personnel can use troubleshooting options to aid in finding the frame faults. Troubleshooting options may be typed in as LIB-SET- messages at any time before or during a normal test. They may also be inputted along with the two normal test input lines given in paragraph 4.01. A detailed explanation and list of troubleshooting options is covered in paragraph 2.39 through 2.42 of the description.

4.03 It may also be desirable for some special reason to use input options. For example, input options are capable of testing several frames of the same type simultaneously. Also, they can be used as a troubleshooting aid. Paragraph 2.07

through 2.38 of the description cover the various input options available for use.

5. BUS TEST PROCEDURE

Bus Isolation Procedure

5.01 The bus isolation procedure should be performed before any bus is tested. To isolate a system bus:

(1) Set te BUS CONTROL switch at the master control center (MCC) to REQ. The system should reply with a message indicating it is premissable to power off the chosen bus.

(2) Move the BUS CONTROL switch to the INH position and verify that no F-level interrupts or emergency action phases occur.

(3) Move the BUS CONTROL switch back to the REQ position.

Note: If a signal processor is equipped, it will be necessary to perform additional steps (a) and (b) below:

(a) If testing PUAB 0, depress the keys below in the following sequence:

(1) BUS DISTRIBUTION REQ INH key on the even CPD.

(2) BUS DISTRIBUTION OFF key.

(3) BUS DISTRIBUTION REQ INH key.

(b) If testing PUAB 1, depress the keys below in the following sequence.

(1) BUS DISTRIBUTION REQ INH key on the odd CPD.

(2) BUS DISTRIBUTION OFF key.

(3) BUS DISTRIBUTION REQ INH key.

Peripheral Unit Address Bus Test

5.02 Before performing PUAB test, it is necessary to isolate the PUAB (paragraph 5.01) to be tested. The PUAB test is also a troubleshooting option, and therefore, may be tested as such.

5.03 To test a PUAB, type

LIB-SET-117c.

after a normal LIB-STA- input. Use the E digit in the LIB-DEC- input to select which bus is to be tested. Otherwise, XCON will use the bus it is currently running on. After typing in the LIB-SET- message:

(1) Connect an oscilloscope to the bus terminal resistor for bit 1. Scope sync is obtained on PUAB bit 0 (bus terminal resistor for bit 0).

(2) Verify pattern for bit 1 (Fig. 12).

(3) Repeat steps (1) and (2) for PUAB bits 2 through 8, 16, 32, and 35 (bus terminal resistors for bits 2 through 8, 16, 32, and 35).

(4) Type LIB-END-c to end test.

Central Pulse Distributor Address Bus Test

5.04 Before performing the CPD address bus test, it is necessary to isolate the CPD bus to be tested. Also, the CPD address bus test is a troubleshooting option, and therefore, may be treated as such.

To test a CPD address bus, type

LIB-SET-118c.

after a normal LIB-STA- input is typed. Use the E digit in the LIB-DEC- input to select which bus is to be tested. Otherwise, XCON will use the bus it is currently running on. After typing in the LIB-SET- message:

(1) Connect an oscilloscope to bus terminal resistor for bit 1. Scope sync is obtained on CAB bit 0 (bus terminal resistor for bit 0).

(2) Verify pattern for bit 1 (Fig. 13).

(3) Repeat steps 1 an 2 for CAB bits 1 through 8, 16, 32 and 33.

(4) Type LIB-END-c to end test.

Peripheral Unit Reply Bus Test

5.05 To test the peripheral unit reply bus, type

LIB-SET-119c.

any time after a normal LIB-STA- input. Use the E digit in the LIB-DEC- input to select the bus to be tested. Otherwise, XCON will use the bus it is currently running on. After typing in the LIB-SET- message:

(1) Connect an oscilloscope to bus terminal resistor for bit 1. Scope sync is obtained on peripheral unit reply bus bit 0 (bus terminal resistor for bit 0).

(2) Verify pattern for bit 1 (Fig. 14).

(3) Repeat steps 1 and 2 for peripheral unit reply bus bits 1 through 8, 15, and 16.

(4) Type LIB-END-c to end test.

6. UTILITY TEST PROCEDURE

Unipolar Enable Test

6.01 The unipolar enable test sends an enable pattern out on each enable lead (Fig. 15). The unipolar enable test is requested by typing in the two lines of general test procedure (paragraph 2.03) with the variables:

ll = 03

e = 0

m = 4

plus the following lines of input:

LIB-SET-116c.

LIB-OCT-00000000c. (octal order)

LIB-OCT-37777777c. (octal mask)

c = Client Number: 0 through 7 for growth and TELCO

00000000 = CPD address of the EN00 enable; use data layout (Fig. 16).

6.02 After the five lines of input given in paragraph 2.30 are typed, the following messages should be printed out.

LIBRARY:TEAM-:TELCO:XCON:TESTING
LIBRARY:TEAM-:TELCO:XCON:UNIPOLAR ENABLE TEST

When the above messages have been printed out, perform the following procedure:

(1) Using internal sync, connect an oscilloscope to the EN00 lead (sweep rate at 10 μsec/cm)

(2) Verify scope pattern for EN00 (Fig. 15).

(3) Repeat steps 1 and 2 for EN01, EN10, and EN11.

(4) Type LIB-END-c to end test.

Bipolar Pulse Test

6.03 The bipolar pulse test is designed to test CPD bipolar points. It sends a pulse pattern out on the P and N leads of a frame (Fig. 17). The bipolar pulse test is requested by typing in the two lines of general test procedure (paragraph 2.03) with the variables

ll = 03

e = 0

m = 4

plus the following lines of input:

LIB-SET-114c.

LIB-OCT-00000000c. (octal order)

LIB-OCT-37777777c. (octal mask)

c = Client Number: 0 through 7 for growth and TELCO

00000000 = CPD Address of the bipolar point use data layout (Fig. 18).

6.04 After the five lines of input, given in paragraph 2.32 are typed, the following messages should be printed out.

LIBRARY TEAM-:TELCO:XCON:TESTING
LIBRARY TEAM-:TELCO:XCON:BIPOLAR PULSE TEST

Number 18

```
-------------------------------------------------------------------------------
DATA LAYOUT FOR OCTAL ORDERS:  CPD
(   22 21)(20 19 18)(17 16 15)(14 13 12)(11 10 09)(08 07 06)(05 04 03)(02 01 00)
(    G  G)( G  R  R)( R  C  C)( C  N  N)( N  N  H)( W  0  0)( 0  0  0)( 0  0  0)
G=GROUP, R=ROW, C=COLUMN, N=CPD NUMBER (0-17), H=HALF(0-1), W=WRMI (=0 NO, =1 YES).
-------------------------------------------------------------------------------
```

Fig. 18—Bipolar Pulse CPD Data Layout

When the above messages have been printed out, perform the following procedure:

(1) Using internal sync, connect an oscilloscope to the P lead at the frame under test (sweep rate at 10 μsec/cm).

(2) Verify scope pattern for P lead (Fig. 17).

(3) Repeat steps 1 and 2 for N lead at frame under test.

(4) Type LIB-END-c to end test.

7. OUTPUT MESSAGES

7.01 There are four types of XCON output messages:

(1) Test status (Table C)

(2) Detailed order analysis (Table D)

(3) System protection (Table E)

(4) Troubleshooting results (Table F)

8. ABBREVIATIONS

AEA	Address of the Enable Address (Address that points to the enable table address).
APLS	Auxiliary Program Library System
ATP	All Tests Pass
CAB	Central Pulse Distributor Address Bus
CATP	Conditional All Tests Pass
CC	Central Control
CPD	Central Pulse Distributor
ESS	Electronic Switching System
GR	Grid
JS	Junctor Scanner
JSD	Junctor Signal Distributor
JSF	Junctor Switch Frame
LS	Line Scanner
LSF	Line Switch Frame
MCC	Master Control Center
MS	Master Scanner
PS	Program Store

TABLE C

TEST STATUS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
LIBRARY:TEAM _:GROWTH:XCON:	Program identification for GROWTH.
LIBRARY:TEAM_:TELCO:XCON:	Program identification for TELCO.
LIBRARY:TEAM_:PITS:XCON:	Program identification for PITS
NEW/OLD NNXX FRMXXX CONTX BUSX	New/old technology, new style frames (remreed or other 1A types) or old style frames. Network number (if network frame), frame type and number, controller, and bus being used.
TESTING	The program is diagnosing the selected controllers.
ATP	All test pass. The frame has successfully completed all controller tests.
CATP	Conditional all tests pass. The frame has completed all controller tests, but must be retested because of a forced condition in testing.
STF	Some tests fail. The test has ended, but the frame does not pass. This message is also printed if the user has forced the program to run through circuit failures.
NOT TESTED	The program was in a test range mode and found this frame not assigned in translations.
BUSY/ACCESS DENIED	The frame requested is currently being used by another XCON team. Access was denied to prevent interference. If testing a range of frames, testing will be advanced to the next available frame.
IN-SERVICE/ACCESS DENIED	The controller requested is currently being used by the system. Access was denied to prevent interference. Testing will advance to the other controller. If testing a range of frames, testing will be advanced to the next available frame.
BB17 KEY 20 NOT OPERATED	The program has suspended to prevent possible interaction of testing from system diagnostics. Pressing key 20 prevents diagnostics from running at the same time as XCON. Resume testing via set 5 input.
INHIBIT DT	DT-INH-. Message must be entered to inhibit dial-tone speed tests. Resume testing via set 5 input.

TABLE C (Contd)

TEST STATUS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
INHIBIT RAD	RAD-INH-, or RAD-INH-2W, or RAD-INH-HL. Message must be entered in inhibit receiver attachment delay calls. Resume testing via set 5 input.
---Continued	An XCON system interface routine has decided to split up the current message into seveal parts in order to satisfy TTY buffer restrictions.
ILLEGAL NUMBER OF LINES	The user has input more/less lines of data then the program requires.
ILLEGAL UNIT TYPE SELECTED	The program was requested to test a unit type that it was not designed to test.
ILLEGAL FRAME TECHNOLOGY	The technology parameter the user input is not current with the unit type requested to test.
ILLEGAL NETWORK NUMBER	The program was requested to test a network number incapable of being tested.
ILLEGAL FRAME NUMBER	The program was requested to test a frame number incapable of being tested.
ILLEGAL ENABLE ROUTE	The program was requested to test an enable route incapable of being tested.
ILLEGAL RANGE OPTION	The program was requested to use a range option not available.
ILLEGAL MODE SELECTED	The program was requested to use a mode option not available.
MS 0 UNASSIGNED	Using unit-type=5 (master scanner) and member number=0, the generic translation subroutine returned on J+O indicating an auxiliary block address = 0 or unassigned frame.
FRAME UNASSIGNED IN TRANSLATIONS	The program is trying to see if translations exist for a frame. The unit-type subtranslator entry (contains auxiliary block addresses) for this frame is zero.
FRAME UNASSIGNED IN PARAMETERS	The program is reading the table X4SCTP and finding the data word set to =3 or unassigned frame.

TABLE C (Contd)

TEST STATUS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
INVALID TRANSLATION DATA	The program requested to test a non-scanner frame, but the generic translations return with a scanner AEA. The program requested to test a frame, but the generic translations returned with an invalid AEA. The program requested to test a non-network frame, but the generic translations returned with a network or signal distributor AEA. The program retrieved the enable for this frame from translations (using the TRUTYN routine) and compared it to the enable obtained from translations (using the NMUTAEA routine). The enables did not agree.
MS UNASSIGNED	Frame has unassigned master scanner number in its FO MSN using unit-type=5 (master scanner) and member number=master scanner number (bits 15-0 or FO MSN). The program is checking if an auxiliary block exists for the master scanner. The auxiliary block was found equal to zero. The FO MSN is stored in the second word of the auxiliary block for the frame.
CIRCUIT TYPE NOT TESTABLE	The program is searching the last word of the auxiliary block for a remreed or ferreed frame (=0 or =1), but the user requested to test a microprocessor controller remreed. The program XCON is not capable of testing this circuit. Use program XMCR for this purpose.

PUAB	Peripheral Unit Address Bus	TSF	Trunk Switch Frame
SAB	Scanner Answer Bus	TELCO	Operating Telephone Company
SD	Signal Distributor	TTY	Teletypewriter
SSD	Supplementary Signal Distributor	USD	Universal Signal Distributor
STF	Some Tests Fail	UTS	Universal Trunk Scanner
TJF	Trunk Junctor Frame	XCON	Universal Controller Test Program

TABLE D

DETAILED ORDER ANALYSIS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
BASE ORDER=XXXXXXXX	Base octal order. This is not necessarily the order being sent to the frame since group-checks and long-binary overides will change this octal order. Base order is only a reference to give a close approximation to what octal information, if any, is being sent to the frame. If pure long-binary information is being sent, this base order will be set to all zeros.
LB45-23=XXXXXXXX, LB22-00=XXXXXXXX	Actual long-binary order being sent to the frame. This represents the exact information sent on the address bus.
(OG G5 G4) (G3 G2 G1) (GC1 GC0 STG) (VCT F S)	Network diagnostic bus layout: OG : =0 If order group normal, =1 If order group error G5 : =0 If group 5 normal, =1 If group 5 error G4 : =0 If group 4 normal, =1 If group 4 error G3 : =0 If group 3 normal, =1 If group 3 error G2 : =0 If group 2 normal, =1 If group 2 error G1 : =0 If group 1 normal, =1 If group 1 error GC1 : =0 If no more-than failures, =1 If more-than failure GC0 : =0 If no less-than failures, =1 If less-than failure STG : =1 If remreed than display group checks, if ferreed than short-to-ground VCT : =0 Path check fail, =1 Path complete; voltage cut through F : =1 When order fails, before broardcast reset S : =1 When order fails, after broadcast reset.
(AP DF) (DR BR AR)	Signal distributor diagnostic bus layout: AP : =0 Register loaded path complete, =1 path incomplete DF : =0 If controller idle, =1 if order fails DR : =0 If register group D unloaded path incomplete, =1 Group loaded BR : =0 If register group B unloaded path incomplete, =1 Group loaded AR : =0 If register group A unloaded path incomplete, =1 Group loaded.
(ENV) (ASW PAR 15) (14 13 12) (11 10 9) (8 7 6) (5 4 3) (2 1 0)	Scanner results layout: ENV : CPDRM flip-flop in B8MAIS, =1 If enable verify return ASW : ASWS flip-flop in B8PUMS, =1 If all-seems-well condition PAR : Parity failure on peripheral reply bus, =1 If failure 15-00 : Scanner answer bus bits

TABLE D (Contd)

DETAILED ORDER ANALYSIS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
(ASW INH) (PCC PCB PCA) (CPDRM CPDEM B) (B B B) (BBB) (B A A) (A A A) (A A A)	Central pulse distributor results layout: ASW : ASWCPD flip-flop in B8PUMS, =1 If all-seems-well condition. INH : INHIBIT flop-flop in CPD (determined to be set if Y register comes back all ones after CPD test lead is pulsed). PCC : PCC flip-flop in B8PUMS, =0 if CPD Z register parity failure PCB : PCB flip-flop in B8PUMS, =0 if CPD Y register parity failure PCA : PCA flip-flop in B8PUMS, =0 if CPD X register parity failure CPDRM : CPDRM flip-flop in B8MAIS, =1 if CPD reply match CPDEM : CPDEM flip-flop in B8MAIS, =1 if CPD echo match B : EXBR7-EXBR0 flip-flops in B8PUMS, indicate which CPD answered A : EXAR7-EXAR0 flip-flops in B8PUMS, indicate which CPD answered.
(F0 S0 T0) (F1 S1 T1)	F, S, and T master scanner point layouts for controller 0 and controller 1.
I XXXXXXX	Initial Frame state (after reset) This is what the frame looked like before a failure occurred.
EB XXXXXXXX	Expected results (before reset) This is what the frame should look like before the system reset pulse is sent out on bit 36.
AB XXXXXXXX	Actual results (before reset) This is what the frame looked like before the system reset pulse was sent out on bit 36.
E XXXXXXXX	Expected results (after reset) This is what the frame should look like after the system reset pulse is sent out on bit 36.
A XXXXXXXX	Actual results (after reset) This is what the frame looked like after the system reset pulse was sent out on bit 36.
PULSED HIGH LEADS: XXXX XXXX ETC. PULSED LOW LEADS: XXXX XXXX ETC.	List of frame leads which should be active for this order. These are a good starting point for any scope work.

TABLE D (Contd)

DETAILED ORDER ANALYSIS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
ACTIVE RELAYS: XXXX XXXX ETC.	List of frame relays which should be operating for this order.
INVALID:	An invalid order is one which, although it may appear to be good, should fail because of the reason listed. If the program stopped here, it is probably because the frame actually accepted this order.
GROUP CHECK >2 >3 <OR ETC. <A <C ETC.	The current order contains a group check failure. List of order groups which should be group checked for this order.
PATH CHECK	An order is being sent which will satisfy group-check circuits but which will not set up a complete pulse path in the frame, thus causing a path check failure.
ORDER TYPE	An unused or illegal order-group is being sent to this frame.
MAINTENANCE ORDER	The maintenance order being sent is no good for this frame type.
HOME/MATE BITS	The order contains an illegal state of home and mate select bits.
MATE STATE DURING CROSS FIRE	The mate controller is not quarantined and a cross-fire order is being sent.
ORDER SEQUENCE	An operate or release order is being sent to a signal distributor magnetic latching relay. This order should fail because the previous order was the same (operate or release).
TEST CONTROLLER STATE	The test controller is quarantined, powered off, or in some state which makes it incapable of executing this order.
UNASSIGNED SCAN ROW	This order is going to an unassigned scan row.
MATRIX CURRENT	The order is going to a CPD point with no load connected across the P N leads.
MAINTENANCE:	Order type being sent to frame under test.
RELEASE	Indicates this is a maintenance release order.
QUARANTINE	Indicates this is a maintenance quarantine order.
TEST POINT ACCESS	Indicates this is a maintenance test point access order.

TABLE D (Contd)

DETAILED ORDER ANALYSIS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
STG	Indicates this is a maintenance STG order.
INHIBIT	Indicates this is a maintenance inhibit order.
POWER OFF	Indicates the frame is powered off.
BUS DEPENDENT	The program determined that the order failed on this bus, but passed on the opposite bus.
INTERMITTENT	The order in question has been retried. The frame sometimes passed and sometimes failed. It may be disirable to use the set 9 input to loop continuously, but stop if a failure occurs. If it is possible to get the frame to fail, then scope the frame for a clue to the nature of the failure. If this fails, try changing out any circuit packs which generate timing pulses.
NOT RETRIED	When the test failed, the program did not retry the order to find out if this is a hard or an intermittent fault. There are three reasons for this: (1) The frame may have fallen out of a maintenance state due to external interference or faulty hardware. (2) The frame may have failed to go into a maintenance state when a maintenance order was sent. (3) The user may have requested troubleshooting options which do not retry the order. In the first two examples, the IA (initial state prior to this order) will be printed for extra information. The reason for not executing a retry is because the frame would have to put back into its original state to retry the order under the same conditions. To do this would mean sending additional maintenance orders. It is known at this point that maintenance orders have a problem. Further tries to alter the frame state at this point would only result in getting further away from the original problem. When desired to force the program to attempt to retry the order, type in a set 6.

TABLE E

SYSTEM PROTECTION OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
WAITING FOR DB	The program is waiting for the diagnostic bus to free up. Testing will resume when it becomes available. Repeated typing of Set 5 will be interpreted as a request to continue testing without using the diagnostic bus. It is possible to test a large percentage of the frame without diagnostic bus use.
DB ACQUIRED-PROCEEDING	The program required the diagnostic bus, but is not available. When the bus becomes available the test proceeds.
F-LEVEL INTERCEPT	A program safety feature has intercepted an order which, if allowed to be sent to the frame, would cause an F-level interrupt. The frame state which is causing this condition will be printed immediately. This may be caused by forcing certain combinations of input options. Remedy this by requesting the test to run on a specific controller after you restore the frame to a normal state.
CONTROLLER POWER OFF	The current order is being sent to a controller which is powered off.
CONTROLLER QUARANTINED	The current order is being sent to a controller which is in quarantine.
F-LEVEL INTERRUPT	An enable verify was not received from the circuit under test. Testing was suspended. During growth testing the generic will print CPD points unassigned. If an F-level interrupt occurs, XCON uses auxiliary block data, not CPDN table information. Thus catagory II translations are not required for this testing. If catagory I translations are in correctly, XCON knows the frame exists but the generic does not.
LIVE ORDER INTERCEPT	A program safety feature has intercepted an order which, if allowed to be sent to the frame, might interrupt an in-service path.

TABLE F

TROUBLESHOOTING RESULTS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
PASSING	The order in question has been retried and the frame is now passing.
FAILING	The order in question has been retried and the frame is now failing.
INTERMITTENT	The order in question has been retried and the frame is now intermittent.
DB ACQUIRED	The user requested the frame be placed on the diagnostic bus. The bus was available and the task completed.
STG SET	The user requested the STG flip-flop in the controller be set. The task was completed.
UNABLE TO TPA	The program tried to use the mate controller to place the test controller on the diagnostic bus, but the mate is unable to do this.
UNABLE TO STG	The program attempted to set the STG flip-flop in the controller, but the frame is unable to do this.
CANT REMOVE CONTROLLER FROM DB	The program tried to use the mate controller to remove the test controller from the diagnostic bus, but the mate is unable to do this.
CANNOT RELEASE CONTROLLERS	The program tried to release both controllers, but the frame is unable to do this.
CONTROLLER RELEASED	The program removed the test controller from the diagnostic bus, and restored it to a normal state.
UNABLE TO RE-ESTABLISH INITIAL CONDITIONS	The program attempted but was unable to place the frame in the same state that it was in prior to failure. Manually place the frame into the states indicated.
ENABLE-VERIFY INHIBIT	The user requested F-level interrupts be inhibited on the frame under test. The task was completed.
ENABLE-VERIFY NORMAL	The user requested F-level interrupts be restored on the frame under test. The task was completed.
NO ORDER SENT, NO ANALYSIS AVAILABLE	The user may have suspended testing before an order was sent to the circuit under test or the program may be waiting for the diagnostic bus. The user may initiate a set 1 to send the order to the circuit and then a set 7 for a detailed printout.

TABLE F (Contd)

TROUBLESHOOTING RESULTS OUTPUT MESSAGES

OUTPUT MESSAGE	EXPLANATION OF MESSAGE
TEST SUSPENDED	The program has suspended due to user or program request. Suspended implies that the program is active, but waiting for a user set option.
BIPOLAR PULSE TEST	See utility tests.
UNIPOLAR ENABLE TEST	See utility tests.
PUB TEST	The program is sending a binary weighted pattern on the peripheral unit address bus. See bus tests.
CAB TEST	The program is sending a binary weighted pattern on the CPD address bus. See bus tests.
SAB TEST	The program is sending a binary weighted pattern on the peripheral unit reply bus. See bus tests.
TEST	LOOPING: User activated a looping LIB SET. CONTINUED: User requested testing to continue. CONTINUED WITHOUT DB: User requested testing to continue without the diagnostic bus. SUSPENDED: User requested the test to temporarily suspended itself.
PROGRAM STATUS:	LOOPING: loop continuously: Set 0 CR set 9. SUSPENDED: Program in a wait mode. Use troubleshooting options. TESTING: The program is being executed. WAITING FOR DB: Program waiting for diagnostic bus to free up.