

## ANALYSIS OF MAIN STORE PROBLEMS

### NO. 2B ELECTRONIC SWITCHING SYSTEM

CONTENTS	PAGE	CONTENTS	PAGE
1. GENERAL . . . . .	1	5. MAS Fault List . . . . .	8
INTRODUCTION . . . . .	1	Table	
TYPES OF FAULTS . . . . .	2	A. Bit Assignments on Bit-Sliced Memory Planes . . . . .	9
A. Hard Faults . . . . .	2	1. GENERAL	
B. Soft Faults . . . . .	2	INTRODUCTION	
MODES OF OPERATION . . . . .	2	1.01 This section provides a general description of the operation of the main store (MAS) audit and how the No. 2B Electronic Switching System (ESS) Processor handles MAS words in error. Also provided is a description of certain output messages which result from the MAS audit and procedures for using these messages to analyze MAS problems.	
A. Double Store Read . . . . .	2	1.02 This section is reissued to upgrade the rating to AT&TCo Standard as a result of field evaluation. Since this is a general revision, arrows ordinarily used to indicate significant changes have been omitted.	
B. Complement Correction . . . . .	4	1.03 The MAS audit program is a part of the main store access routines (MASACS) program (PR-2H355) for the 2B-EF-1, Issue 4 or later, and 2B-EF-2 generic programs. The purpose of the audit is to work with the 3A central control (3ACC) to maintain system sanity when MAS errors occur. In the course of normal instruction processing, the 3ACC can obtain valid data when a MAS error occurs (under proper conditions), by using the double store read or complement correction functions. Certain types of MAS faults will cause a system initialization. The MAS audit reports abnormalities in MAS by TTY output message and attempts correction on words in error so that these errors	
MAIN STORE AUDIT OPERATION . . . . .	5		
2. TROUBLE PROCEDURES . . . . .	7		
A. RCOVRY MAS ERR . . . . .	7		
B. REPT MAS MISMATCH . . . . .	8		
C. REPT MAS COMP . . . . .	9		
D. REPT MAS TRBL . . . . .	10		
<b>Figures</b>			
1. Double Store Read Example—Duplex (Simplified Words) . . . . .	3		
2. Complement Correction—Simplex (Hard Fault Example) (Simplified Words) . . . . .	4		
3. Complement Correction—Duplex (Soft Fault Example) (Simplified Words) . . . . .	5		
4. MASTYPE Word . . . . .	6		

**NOTICE**

Not for use or disclosure outside the  
Bell System except under written agreement

## SECTION 232-305-302

will be corrected when they are encountered by the 3ACC in normal call processing.

**1.04** The following documents provide reference and background information related to this section:

- Section 232-309-101, 2B Processor Description, No. 2B ESS
- Section 254-300-150, 3A Processor Main and Supplemental Stores Description and Theory of Operation, Common Systems
- Main Store Access Routines Program (MASACS) PR-2H355
- Common Base Level Monitor (CBLM), PR-1C950
- Input Message Manual 2H200
- Output Message Manual 2H200.

### TYPES OF FAULTS

**1.05** Most errors in main store words are caused by faults in MAS memory devices. The 2B processor utilizes the insulated-gate-field-effect transistor (IGFET) as the memory cell in the main memory. A binary bit is stored as the absence or presence of electrical charge on the parasitic capacitance of the IGFET memory cell. The main memory chip is an array of either 4K or 16K memory cells mounted in a dual in-line package (DIP). A faulty memory cell can cause a main store word to be in error because the bit represented by that cell can be invalid.

#### A. Hard Faults

**1.06** A failing memory cell which is "stuck" in a high or low state is said to have a hard fault. A write operation will not have an effect on the value the bit is storing. Any attempt to change the state of the failing bit will be unsuccessful. This condition could cause the word containing the failing bit to be in error. The error will be detected as bad parity when the word is read from main store. (Odd parity is used in the 3ACC.)

#### B. Soft Faults

**1.07** A soft fault is an intermittent or temporary memory cell failure. The faulty bit favors one failing state but *can* be set temporarily to the other state. The failing cell can sustain a valid stored state for an arbitrary period of time, then the cell will fail and return to the invalid state. When this bit is written as part of a normal write operation, the bit will change states temporarily then eventually return to the failed state. The word containing the faulty bit will be in error if the bit is storing an improper value when the word is read.

#### MODES OF OPERATION

**1.08** The 2B processor employs two methods for the correction of MAS words in error. These are: double store read and complement correction. The method used depends upon the operating mode of the system: simplex or duplex. Both methods of correction are intended to provide the 3ACC with valid data when a MAS error is detected during a read operation.

#### A. Double Store Read

**1.09** A double store read is hardware initiated and is used only when the system is operating in the duplex mode. In the duplex mode of operation, the on-line and off-line MASs are matched and are duplicates of each other. In this mode, the off-line store is kept up to date and available to the on-line control unit (CU) in case an error occurs in the on-line store. Any write operation directed to the on-line store also occurs in the off-line store so that the matched condition is maintained. Also, the off-line MAS is automatically updated whenever the system is restored to the duplex mode (off-line CU restored to service).

**1.10** If a parity error is detected when a word is read from the on-line MAS, the 3ACC hardware will initiate a read from the same location in the other store when operating in duplex. If the word read from the other store has good parity, the word is returned to the 3ACC and used in place of the erroneous word found in the on-line store. If the word read from the off-line store has bad parity, a system initialization will occur (Fig. 1). The double store read is a wired logic function and is transparent to instruction processing.

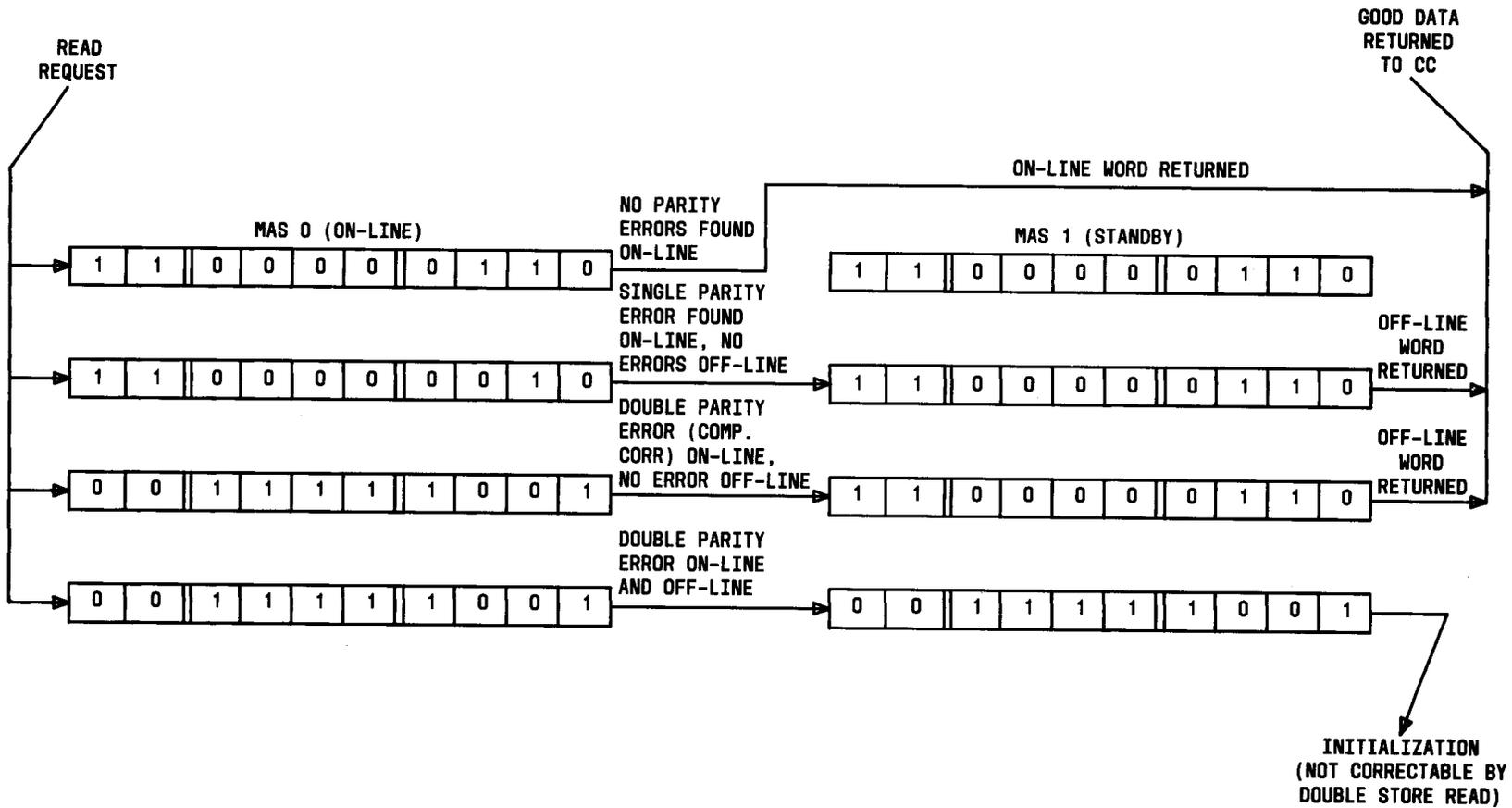


Fig. 1—Double Store Read Example—Duplex (Simplified Words)

**B. Complement Correction**

1.11 Complement correction (Figures 2 and 3) is a method of correcting single bit errors in MAS words which is used when the system is operating in the simplex mode. In simplex, the off-line store is not up to date and is not available for use by the on-line CU. The BDSR bit (bits 12 and 13) of the main memory status register (MMS) will be set to one, indicating block double store read.

1.12 When a single parity error is detected on a read operation in simplex, the main store controller (MASC) issues a store error C (SERC) signal to the 3ACC. The SERC, together with the BDSR=1, causes the 3ACC to invoke a microsubroutine to perform the complement correction. The microroutine complements all bits of the word in error and causes the word to be written back into the same (failing) location. If the error is caused by a hard fault, the failing bit will not change states, thus the word is stored in a correct but complemented form (Fig. 2). The complemented word has both parity bits bad. The double parity

error is a flag to the MAS circuitry when the word is read again which indicates that all bits should be recomplemented before they are returned to the 3ACC.

1.13 If the error is caused by a soft fault, the failing bit may change states when the word in error is complemented and written back at the failing location. This will leave the complemented word with a single parity error (Fig. 3). Single bad parity will be detected when the word is read again and complement correction will be attempted. Thus, a complement correction loop is started and will continue until a time-out occurs and an initialization results.

1.14 Complement correction is used by the MAS audit to correct MAS words found in error. The MAS audit does not use microcode to carry out the correction. Instead, the complement correction is accomplished as part of the instruction processing of the MAS audit program itself. The MAS audit can correct an error caused by a soft fault if good data is available from the other store. The MAS audit program does so by writing the

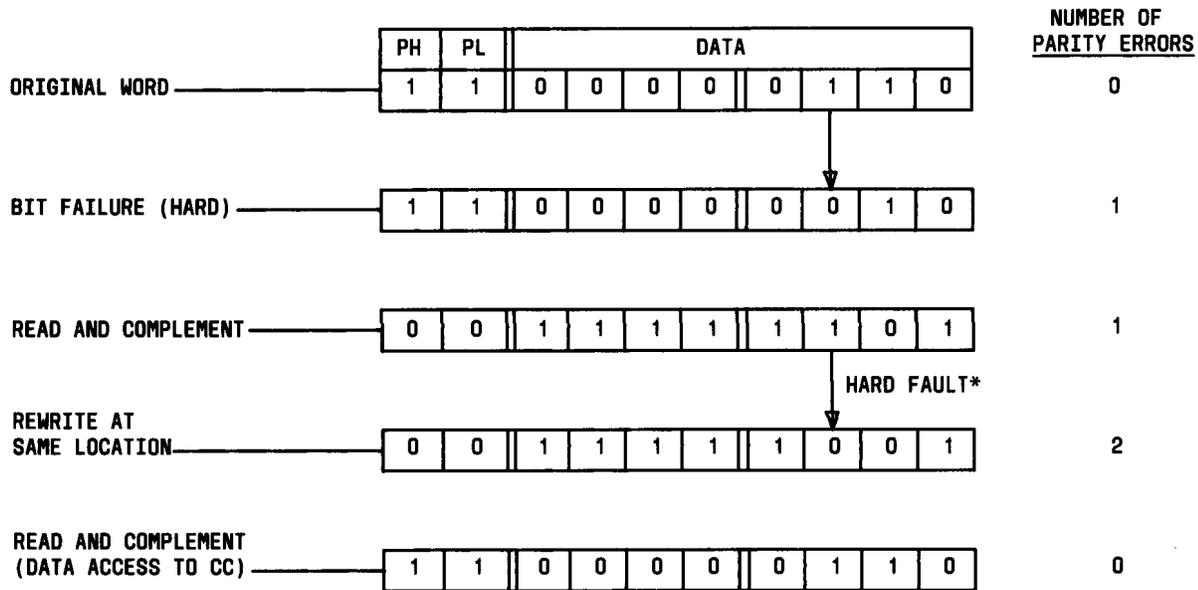


Fig. 2—Complement Correction—Simplex (Hard Fault Example) (Simplified Words)

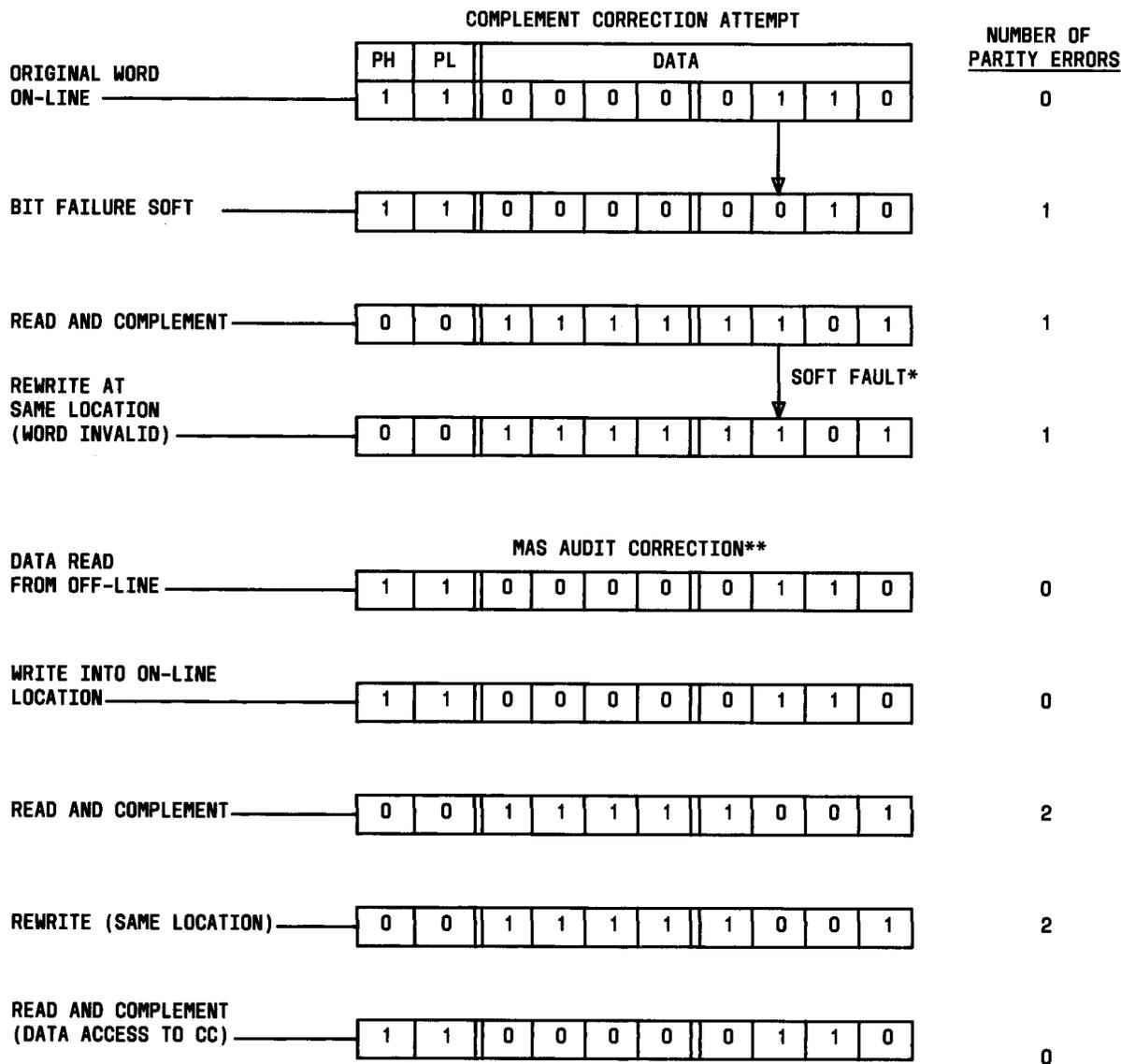


Fig. 3—Complement Correction—Duplex (Soft Fault Example) (Simplified Words)

good data from the other store into the bad location, then carrying out the complement correction procedure on that word (Fig. 3). The result is that the word is stored in a correct but complemented

form (double bad parity), and the bad bit is set to the state the bit normally returns to upon failure. Valid data is obtained when the word is read and recomplemented.

**MAIN STORE AUDIT OPERATION**

**General**

1.15 The main store audit operates continuously on a time available basis, regardless of system mode (duplex or simplex), checking all defined words of MAS and the double store read trap (DSR trap). Attempts are made to correct all words with bad parity, both on-line and off-line, and all corrections are identified by TTY output message. All locations which are already corrected or mismatch between on-line and off-line store locations are identified by TTY output message. No correction is attempted on words that mismatch between stores because the MAS audit cannot determine which word is valid. Single bit faults are explicitly identified by CU, MAS, module (MOD), circuit pack (PACK) and DIP. All locations which cannot be corrected by the audit because of faulty hardware or because good data cannot be obtained from off-line are identified by TTY output message. The MAS audit is compatible with 4K(JL-2 packs, 32K words per MOD), 16K(JL-16 packs, 128K words per MOD) or a mixture of the two types on a main store basis. The MASTYPE word (Fig. 4) is used to identify to the audit which type memory device is used in each MAS.

**Double Store Read Trap**

1.16 Each time a double store read is executed by the system, an entry is made in the DSR trap in MAS to preserve the error for the MAS audit. The DSR trap contains the address of the word in error, the bad data found at that location, and the good data read from the other store. Only one error is preserved at a time in the DSR trap. Each new double store read causes the old error in the trap to be replaced by the new error information. The information in the

trap is used by the MAS audit to generate a TTY output message identifying an error correction. On each cycle of the audit, the DSR trap and a block of 32 store words is examined. The audit is executed a minimum of once each base level loop until all defined words of MAS are examined, before beginning a new cycle.

**MAS Audit Sequence**

1.17 The sequence followed by the MAS audit in checking and correcting one word of store is as follows:

- (1) **Read the on-line word**—Four possible results:
  - (a) Bad data—The audit cannot correct by complement correction (soft fault).
  - (b) Good data—Single parity error found; the audit corrects the word by complement correction, returns good data and generates the RCOVRY MAS ERR message.
  - (c) Good data—Double parity error found; the word is already complement corrected. The audit returns good data and generates the REPT MAS COMP message.
  - (d) Good data—No errors found; the audit returns the good data.
- (2) **Read the off-line word**—Same four results as for the read of the on-line word.
- (3) **Take action**—Seven possible actions:
  - (a) Correct the on-line word with data from off-line. Generate the RCOVRY MAS ERR message.



$M_n = 0$  - MAS  $n$  EQUIPPED WITH JL-2 PACKS (4K DIP MEMORY DEVICES)  
 $= 1$  - MAS  $n$  EQUIPPED WITH JL-16 PACKS (16K DIP MEMORY DEVICES)

**Fig. 4—MASTYPE Word**

- (b) On-line trouble exists; the word cannot be corrected. Generate the REPT MAS TRBL message.
- (c) Correct the off-line word with data from on-line. Generate the RCOVRY MAS ERR message.
- (d) Off-line trouble exists; the word cannot be corrected. Generate the REPT MAS TRBL message.
- (e) Uncorrectable on-line and off-line trouble exists. The word cannot be corrected at either location. Generate a REPT MAS TRBL message for the on-line **and** off-line CUs.
- (f) Match the on-line and off-line data. If mismatched, generate the REPT MAS MISMATCH message.
- (g) No action required.

(4) **Repeat the cycle for the next word of store.**

**Main Store Fault List**

1.18 All single bit errors which are corrected and reported by the RCOVRY MAS ERR message are recorded in a push-down MAS fault list (MASFLIST) kept in temporary store. This list can record eight error entries in a push-down, double word entry format. The list is 16 words long (2 words per entry [Fig. 5]) and each new entry pushes preceding entries two words down. The double word entry in the last position of the list is lost when it is replaced by the preceding double word entry. The MAS audit uses this list to reconstruct RCOVRY MAS ERR messages when an audit is manually requested. The list is self-administering as old entries are always discarded in favor of new entries.

**Manually Requested Audit**

1.19 The MAS audit can be requested with the input message AU:MAS!. This message causes the audit to restart at location zero and continue through the last defined word of MAS. Error messages are printed for all abnormalities known to the audit, both on-line and off-line. Normally the MAS audit prints error messages for the first batch of each type error only. This input

message will cause outputs for **all** locations which are uncorrectable, presently complement corrected, or logically mismatch between corresponding on-line and off-line locations. RCOVRY MAS ERR messages are reconstructed for all errors which have an entry in the MASFLST.

1.20 The MAS audit request is not allowed if the off-line MAS is out of service. However abnormal conditions of the on-line MAS alone may be obtained by using the UCL action-option (AU:MAS;UCL!). This message will cause an audit of the on-line MAS only and errors associated with the off-line store may not be identified.

1.21 Certain types of MAS errors may cause a flood of TTY output messages until the audit completes one cycle and returns to the normal mode of operation. This can be stopped by temporarily inhibiting and reallowing the audit by inputting INH:MASAU!, followed by ALW:MASAU!, at the maintenance (MC) TTY.

**2. TROUBLE PROCEDURES**

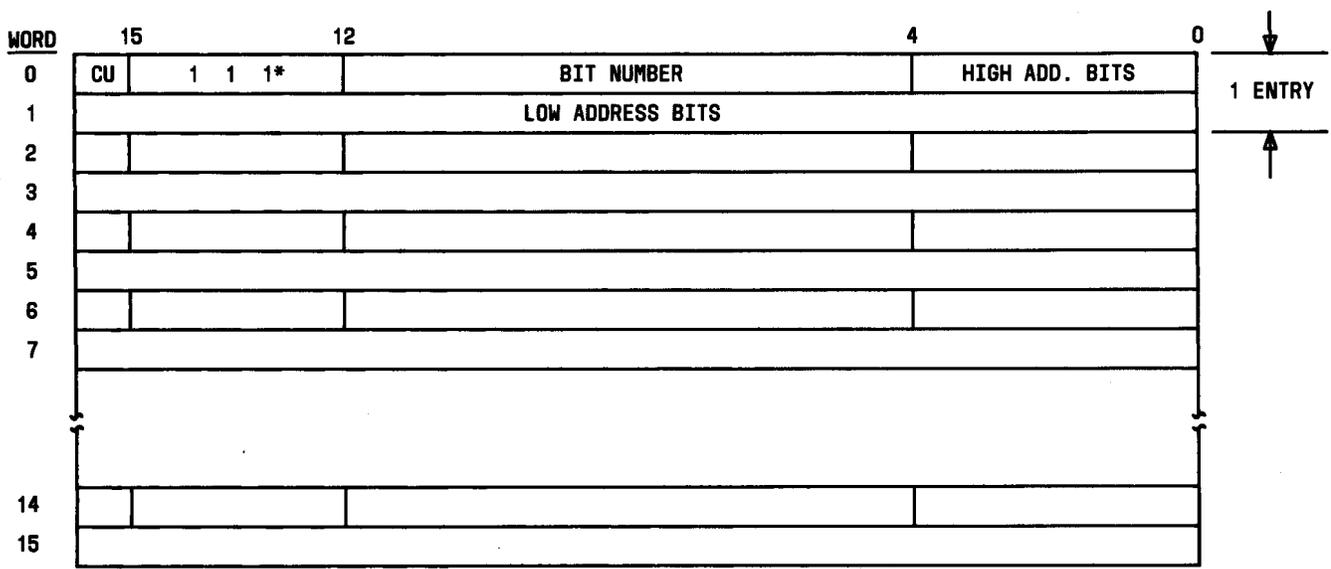
2.01 **Procedural Layout:** The following paragraphs list each output message associated with the main store audit and main store error detection as major headings with explanatory text and procedures following. When an error message is received, the message explanation should be reviewed and the specified procedure followed, as indicated for that message.

**A. RCOVRY MAS ERR**

**RCOVRY MAS ERR cu aaaaaaa gooddata  
baddata bit MASx MODyy PACK vv DIP  
w.z cccc**

2.02 The occurrence of the RCOVRY MAS ERR message indicates that the main store audit has detected a main store word in error and has performed correction. If the error is a single bit fault, the variable fields contain the necessary information for replacement of the faulty circuit pack. A multiple bit failure will result in "99" for the bit and pack identification. Another procedure must be used to identify the faulty pack in this case. Action to be taken is as follows:

- (1) Ensure that the control unit (CU) containing the fault is off-line. (If necessary, restore the off-line CU to service then switch CUs).



\* BITS 12-14 ALL ONES (VALID DATA PRESENT INDICATOR) ON THE FIRST WORD OF EACH ENTRY.

Fig. 5—MAS Fault List

(2) If bit and pack numbers are given in the output message, use this information to locate and replace the faulty circuit pack.

**Note:** The failed circuit pack should be tagged to identify the failing DIP. A copy of the TTY printout should be attached to the failed pack for use in repair.

(3) If bit and pack numbers are not given, request the main store audit by typing the following message at the MC TTY.

AU:MAS!

- (a) If the output from the main store audit gives valid bit and pack numbers, proceed as in Step 2.
- (b) If the output message differs from RCOVRY MAS ERR, refer to the procedure for that output message.
- (c) If the RCOVRY MAS ERR message is repeated, where valid bit and pack numbers are not given, run CU diagnostics.

Type in at the MC TTY—

DGN:CU!

**B. REPT MAS MISMATCH**

**REPT MAS MISMATCH cu aaaaaaa online offline**

**2.03** The REPT MAS MISMATCH message indicates that the MAS audit has detected a logical mismatch between on-line and off-line data at address aaaaaaa. The CU identified is the one currently on-line. No correction has been attempted at either location but double store read is blocked. This error is most likely due to a program bug or procedural error; however, it may be the result of a double bit fault on the same circuit pack. Proceed as follows:

- (1) Determine if this is a double bit fault on the same circuit pack by doing the following:
  - (a) Compare the on-line data to the complement of the off-line data (both in binary).
  - (b) If **exactly** 2 bits mismatch, 8 bit positions apart in the range of 0-15 or 4 bit positions apart in the range 16-23, assume a bad circuit pack associated with the mismatching bits.

- (c) Determine the faulty memory plane by Table A with the mismatching bit numbers.
- (d) Determine the CU containing the faulty pack by comparing off-line and on-line data to listings, if available, or by requesting the MAS audit and looking for a REPT MAS COMP cu message at the same address.

Type in at the MC TTY—

AU:MAS!

- (e) Locate and replace the faulty memory plane.
- (2) If this is not a double bit fault on the same circuit pack, proceed as follows:
- (a) By context of circumstances, determine whether off-line or on-line is valid.
  - (b) Ensure that valid side is on-line, then update the other side. Type in at the TTY—

UPD:OMAS!

**C. REPT MAS COMP**

**REPT MAS COMP cu aaaaaaa gooddata**

**2.04** The REPT MAS COMP message indicates that the MAS audit has encountered a MAS word in complement corrected form. Two parity errors were detected when the word was read from MAS. This could be the result of a recent correction by the on-line CU while operating in simplex or a double bit fault on the same circuit pack. Take the following action:

- (1) Ensure that the CU containing the error is off-line. (If necessary, restore the off-line CU to service then switch CUs).
- (2) Type in at the MC TTY—

AU:MAS!

If the output from this request differs from REPT MAS COMP cu, refer to the procedure for that output message and proceed as specified.

**TABLE A**  
**BIT ASSIGNMENTS ON**  
**BIT SLICED MEMORY PLANES**

BITS		PACK NO. (MOD = EVEN/ODD)	
		EVEN	ODD
0	8	4	31
1	9	5	29
2	10	6	28
3	11	7	27
4	12	8	26
5	13	9	25
6	14	10	24
7	15	11	23
16	20	12	22
17	21	13	21
18	22	14	20
19	23	16	19
PL	PH	17	18

- (3) If the output does not change— Determine the correct data by dumping the on-line data at this address or by referencing listings, if the error did not occur in temporary store.
- (4) Compare the correct data to the complement of the data from this message, then perform substeps b through e from Step 1 of the procedure for output message B (REPT MAS MISMATCH).
- (5) If none of the above procedures are successful— Record the occurrence of this output message, then eliminate the complement correction. Type in at the MC TTY—

UPD:OMAS;UCL!

Followed by—

RST:CU;UCL!

D. REPT MAS TRBL

**REPT MAS TRBL cu aaaaaaa baddata**

2.05 The occurrence of the REPT MAS TRBL message indicates that the MAS audit has encountered a MAS word in error that is uncorrectable. Automatic correction was not possible because of multiple bit hardware failures or because good data was not available from the off-line store. **This indicates a serious condition which may be service affecting. Corrective action must be taken as soon as possible.** Proceed as follows:

- (1) If the CU containing the fault is **not** off-line, ensure that it is by doing the following—
  - (a) Ensure that the off-line CU is in-service (RST:CU!).
  - (b) If the address of the error indicated by this message is **not** in temporary store— Perform an off-line bootstrap to load the off-line store, then switch CUs unconditionally (SW:CU;UCL!). Proceed to Step 2.
  - (c) If the address of the error indicated by this message **is** in temporary store— Switch CUs unconditionally (SW:CU;UCL!). Proceed to Step 2.
- (2) If the CU containing the fault is off-line, request the MAS audit in an attempt to

convert the single parity error into a double parity error (complement corrected), indicated by a REPT MAS COMP message specifying the same address. Type in at the MC TTY—

AU:MAS!

(3) If a REPT MAS COMP cu message occurs, match the good data from the "COMP" message to the bad data **and its complement** from the "TRBL" message. Look for a single bit mismatch.

- (a) If a single bit mismatch is found, assume a bad pack associated with that bit.
- (b) Determine the faulty pack with the bit number by Table A and replace.

(4) If a REPT MAS COMP message does **not** occur, obtain the good data for this address by referencing listings, if possible, or by dumping on-line data at this address. Compare the good data to the bad data **and its complement** from the "TRBL" message. Look for a single bit mismatch. Proceed with substeps a and b from Step 3.

(5) If none of the above procedures are successful, record the event of this "TRBL" message and update the off-line store unconditionally then restore it to service. Type in at the MC TTY—

UPD:OMAS;UCL!

Followed by—

RST:CU; UCL!