

2B PROCESSOR DESCRIPTION

NO. 2B ELECTRONIC SWITCHING SYSTEM

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NOTICE

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1. GENERAL

1.01 This section describes the major components and functions of the 2B processor used with the No. 2B Electronic Switching System (ESS). The 2B processor incorporates 1A and other current

technology and is based on the design of the 3A central control (3A CC).

1.02 The 2B processor provides complete control of the No. 2B ESS. The 2B processor controls the operation of the equipment associated with the No. 2B ESS central office (networks, trunks, service circuits, etc.) and provides the man machine interface necessary for maintenance and administration. The 2B processor is illustrated by the block diagram in Fig. 1 which shows the relationship of the 2B processor to the equipment it controls. The 2B processor consists of two control units (CUs), the maintenance (MTCE) frame, and two supplementary main store frames. The CUs are duplicated for reliability.

1.03 The CU controls all functions performed by the peripheral units. One CU is always in the active or on-line state controlling the peripheral equipment. If a failure occurs in the active CU, the standby or off-line CU can be updated and switched on-line and the faulty CU can be placed out of service. Each CU is a separate and complete switching central control system capable of controlling the office.

1.04 The MTCE frame provides a man-machine interface between the maintenance personnel and the No. 2B ESS central office. The maintenance personnel can access and control the system through the teletypewriter and the system status panel. The MTCE also provides a backup image of the program and translation data in the tape data controller facility.

1.05 Each CU has been designed as a single switchable unit. The subunits which make up a CU are dedicated to each other and treated as one unit rather than individual switchable units.

1.06 Speed of installation and growth has been enhanced by connectorization, which allows plug-in cabling between units. Almost all leads, except power, which interconnect the subunits of a control unit and the MTCE frame are furnished with connectorized cable.

2. NO. 2B ESS INSTRUCTION SETS

2.01 The No. 2B ESS utilizes two basic instruction sets:

- 3A instruction set

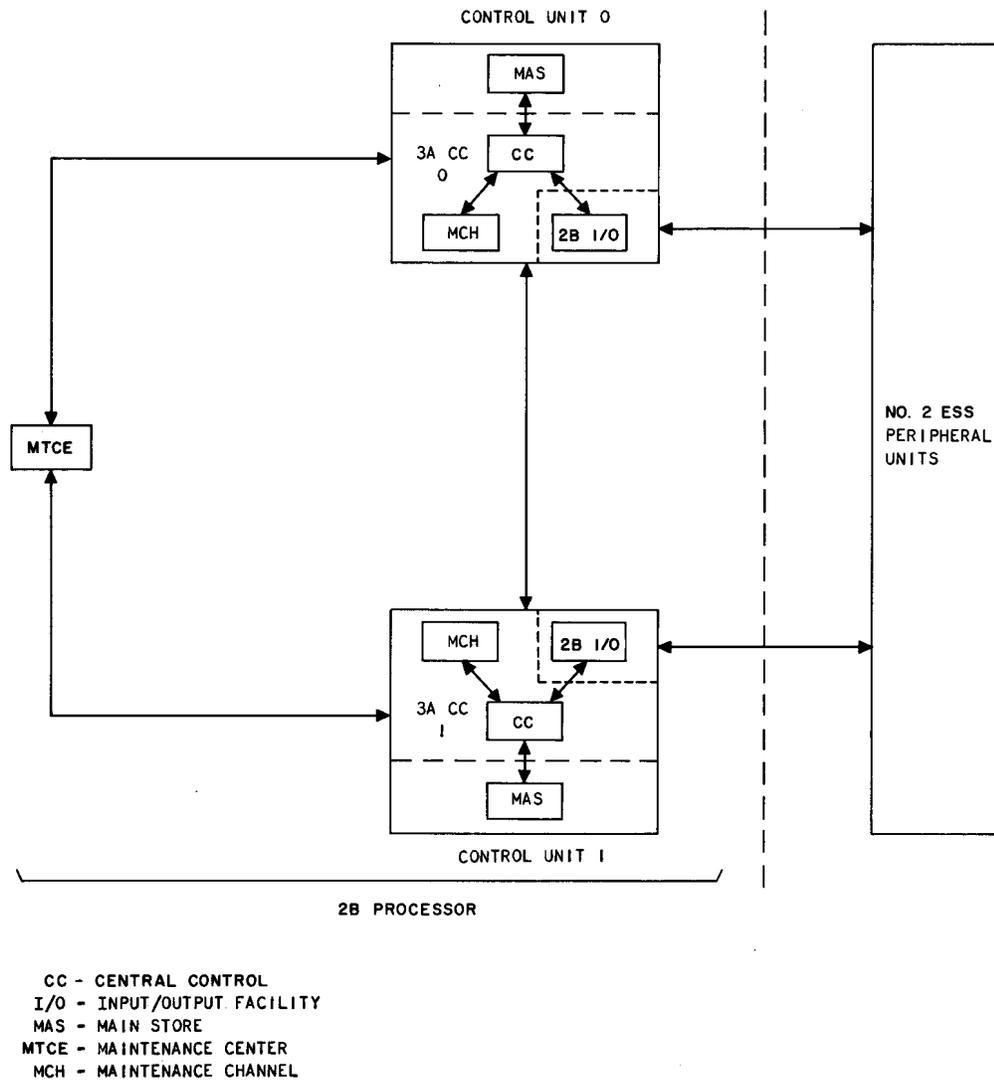


Fig. 1—Block Diagram of 2B Processor

• 2B instruction set.

The 3A instructions are used to control the internal sequencing, diagnostics and maintenance of the 3A CC. The 2B instructions are used for the execution of call processing programs, peripheral unit diagnostic and maintenance programs, and unique 2B programs. The 2B instruction set consists of new 2B instructions and approximately 75 percent of the No. 2 ESS instructions. The new 2B instructions are combined

with both the No. 2 and 3A instructions for the unique 2B programs.

3A INSTRUCTIONS

2.02 The 3A instructions consist of single (full) word instructions and double word instructions (Fig. 2). Single word instructions are the most commonly used; however, double word instructions are used when either 16 bits of data or a 20-bit address is required in an instruction. For more

information on 3A instructions refer to Section 254-300-120.

NO. 2B ESS EMULATED INSTRUCTIONS

2.03 The No. 2B ESS emulated instructions consists of full word instructions and half word instruction (Fig. 3). The half word instructions contain two OP codes and associated address fields and are the most commonly used; however, full word instructions are used when 16 bits of data or a 16-bit address is required in an instruction.

2.04 The basic instruction words are 24 bits long. The full word instructions contain one instruction with a 7-bit OP code, 16-bit address and a transfer allowed (TA) check bit. This check bit is used for detecting improper transfers because of an equipment fault or an error in program. The number of full word instructions is rather small. They are used for absolute program transfers and also for supplying constants for various functions.

2.05 The two half word instructions consists of two 12-bit instructions, each with a 7-bit OP code and a 4-bit address and a TA bit. The 4-bit address is used to denote a value or a modifier. For example, a value associated with a rotate instruction specifies the amount of rotation. A modifier associated with a gating operation specifies the data path from one register to another. The OP code is used to access a set of microinstructions which accomplishes the function indicated by the instruction.

2.06 The instruction mapping of half words into the main store is illustrated in Fig. 4. The mapping is not bit for bit. The emulated OP codes are different bit patterns than the old No. 2 OP code bit patterns. Figure 5 illustrates the mapping of a full word instruction into a 26-bit store word.

UNIQUE 2B INSTRUCTIONS

2.07 The unique 2B instructions consist of full word and half word instructions similar to the No. 2B ESS emulated instructions (Fig. 3). The OP code and address fields of the 2B instructions have the same bit length as the corresponding fields in the emulated instructions. The 2B instructions are formatted and executed exactly like emulated No. 2B instructions.

3. EQUIPMENT DESCRIPTION

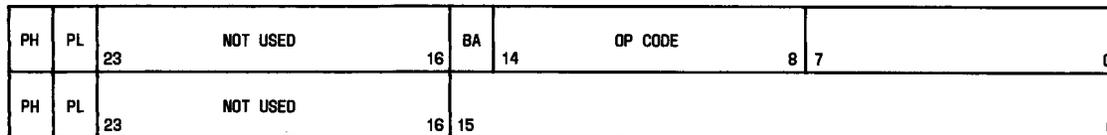
2B PROCESSOR FLOOR PLANS

3.01 Figure 6 illustrates the 2B processor floor plan layout. The 2B processor consists of four frames as follows:

- 2B processor frame
- Maintenance center frame
- Two optional supplementary main store frames (which may be optionally equipped with stores).



A. SINGLE WORD INSTRUCTION



B. DOUBLE WORD INSTRUCTION

Fig. 2—3A Instructions

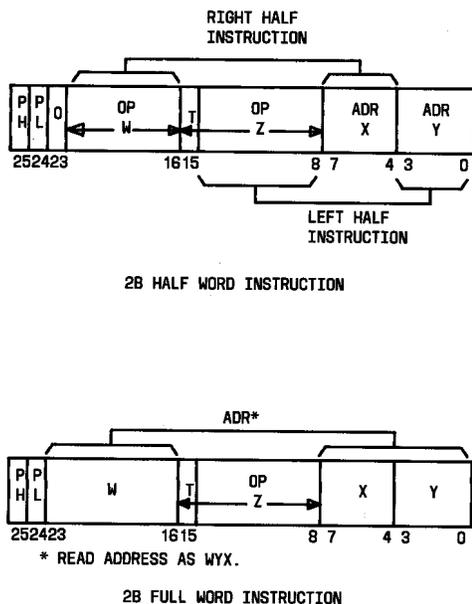


Fig. 3—Unique 2B Instructions and No. 2B Emulated Instructions

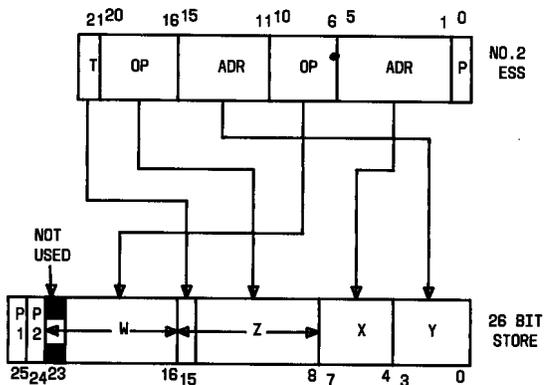


Fig. 4—Mapping of Two Half Word Instructions Into a 26-Bit Store Word

The frames are arranged in a single equipment lineup requiring a maximum aisle length of 10 feet and 10 inches. Standard ESS framework is utilized which is seven feet high.

2B PROCESSOR FRAME

3.02 The 2B processor frame (Fig. 7) is a two-bay frame which is four feet and four inches

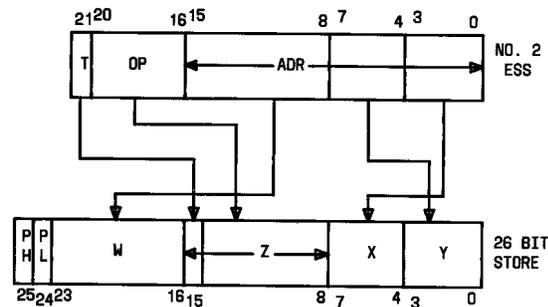
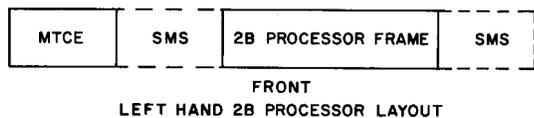


Fig. 5—Mapping of a Full Word Instruction With a 16-Bit Address Into a 26-Bit Store Word



ABBREVIATIONS
 MTCE - MAINTENANCE CENTER
 SMS - SUPPLEMENTARY MAIN STORE

LEGEND

 - INITIALLY INSTALLED EQUIPMENT
 - ALLOCATED SPACE FOR GROWTH

Fig. 6—No. 2B ESS 2B Processor Floor Plan

wide and consists of duplicated CUs. The CUs are designated CU0 and CU1. Each CU bay is comprised of the following units which work together to perform various functions:

- 3A central control (3A CC)
- 2B input/output (I/O) control circuit
- Main store
- Power and fuse unit.

The on-line unit has active control over system actions while the off-line CU is on standby.

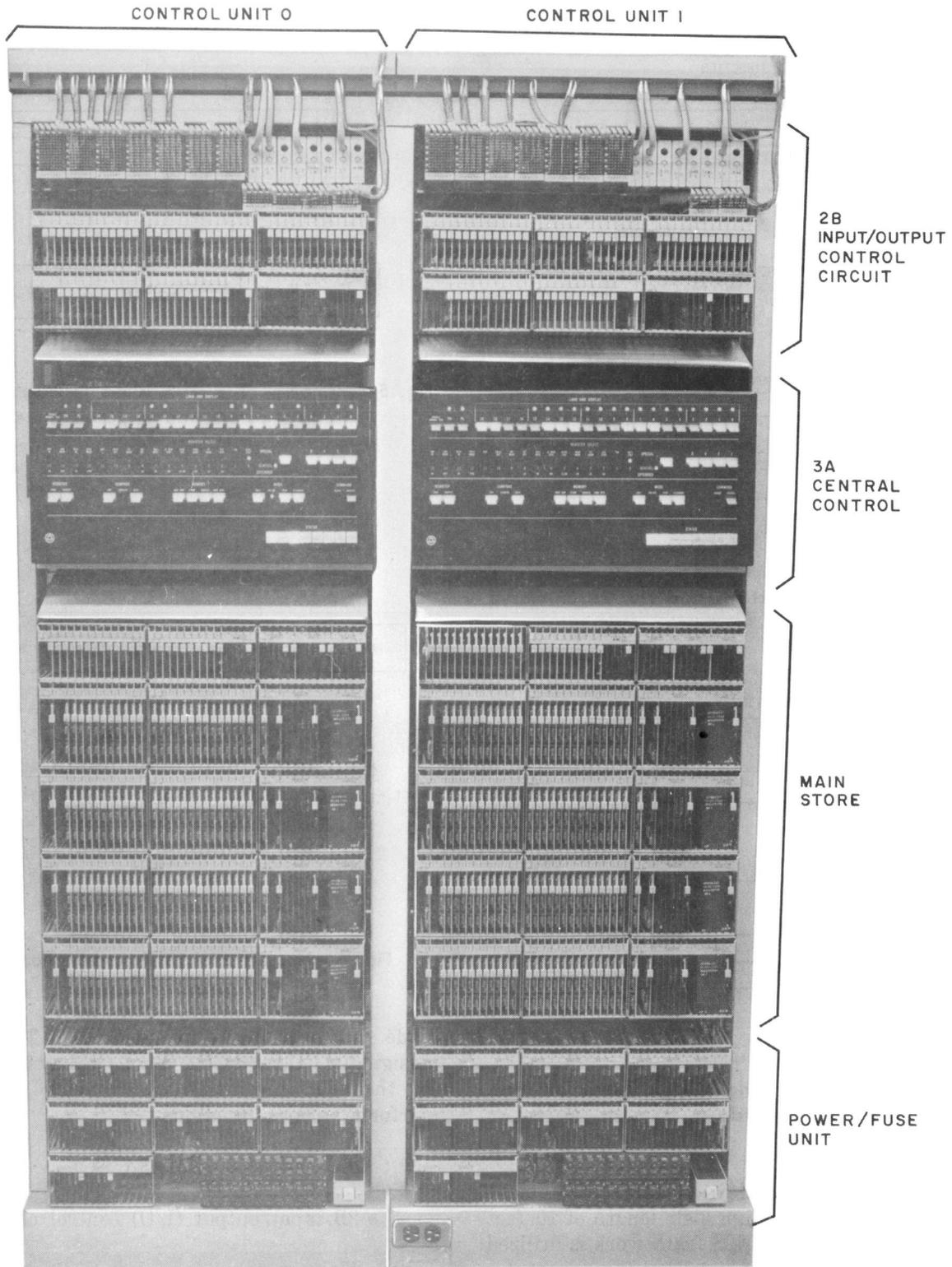


Fig. 7—2B Processor Frame

3.03 For a single common CU to keep up with the flow of information, calls must be processed and program orders must be executed in *real time*. The CU does that by performing its functions on a *time-sharing* basis.

- (a) The term *real time* means that the switching system is presented with a continuous stream of inputs which will not wait or slow down if the system falls behind in handling time. Such a system must be capable of handling all busy-hour traffic without noticeable delays to the customer. Each customer must receive immediate, efficient service.
- (b) The term *time-sharing* refers to many circuits sharing the services of a common circuit, each circuit being served on a sequential basis.

A. 3A Central Control

3.04 The discussion of the 3A CC in this section is of a general nature except for functional information on the 3A CC circuitry which applies only to the No. 2B ESS application (for example: 26-bit store word interface circuitry). Refer to Sections 254-300-110 and 254-300-120 for a detailed description of the 3A CC.

3.05 The 3A CC is the controlling element of the 2B processor and the entire system (Fig. 8). The 3A CC (Fig. 9) is located in the upper mid-section of each bay. The position on the frame provides the operator convenient access to the keys and switches which control the 3A CC and the system. The 3A CC is 23 1/2-inches wide, 12-inches high, and approximately 14-inches deep. Basically it consists of a logic unit and a front control panel.

3A CC Logic Unit

3.06 The 3A CC circuit packs are held in eight 80C apparatus housings which are mounted on a 12-inch mounting plate. FA-, FB-, and FC-type circuit packs are used in the 3A CC. Refer to Section 232-309-111 for detailed information on the circuit packs.

3.07 Two basic types of silicon integrated circuit (SIC) logic gates used in the 3A CC circuitry are the low power diode modified transistor-transistor logic (DT₂L) NAND gate, the high-power DT₂L NAND gate, and the resistor-transistor logic buffer

inverter gate. The low-power gate is used in all logic circuits. The high-power gate is used in special circuits such as cable driver circuits. The buffer inverter gate is used to buffer signals coming in from the backplane. Four to eight gates are packed on an SIC chip. A maximum of 52 SIC chips may be mounted on a ceramic substrate which is approximately 3-1/4 by 4 inches in size. The ceramic substrate is mounted on a removable FA-type circuit pack (4 by 7-3/4 inches) with an 82-pin connector (Fig. 10A). In the 3A CC arrangement for 2B applications, there are 58 FA-type circuit packs with an average of 43 SIC chips on each.

3.08 The FB- and FC-type circuit packs are very similar to each other (Fig. 10B). Both types contain discrete devices and may contain hybrid integrated circuits (HICs). (A HIC is a small ceramic substrate mounted on a board along with other discrete devices.) The major difference between the FB- and FC-type packs is their means of external connections. The FB-type circuit packs use a 42-pin connector; the FC-type pack uses an 82-pin connector.

3A Central Control Panel

3.09 The control panel consists of a 12-inch by 23-1/2 inch plastic panel, silk-screened black with the appropriate nomenclature stencilled in white letters. The panel includes the following apparatus:

- (a) Status indicator lamps and switches
- (b) Light-emitting diodes (LEDs) which display the data or address of the memory or register
- (c) Register select switches for loading or displaying purposes
- (d) Switches for selecting a particular manual function.

3.10 The panel is mounted to an aluminum frame and has a printed wiring board which supports all the apparatus and circuitry necessary for the control panel to function. The entire assembly is hinged to the side brackets of the 3A CC logic unit to provide access to the circuit packs within the unit. Most of the interconnections between the panel and the rest of the 3A CC are accomplished by means of a connectorized flat tape

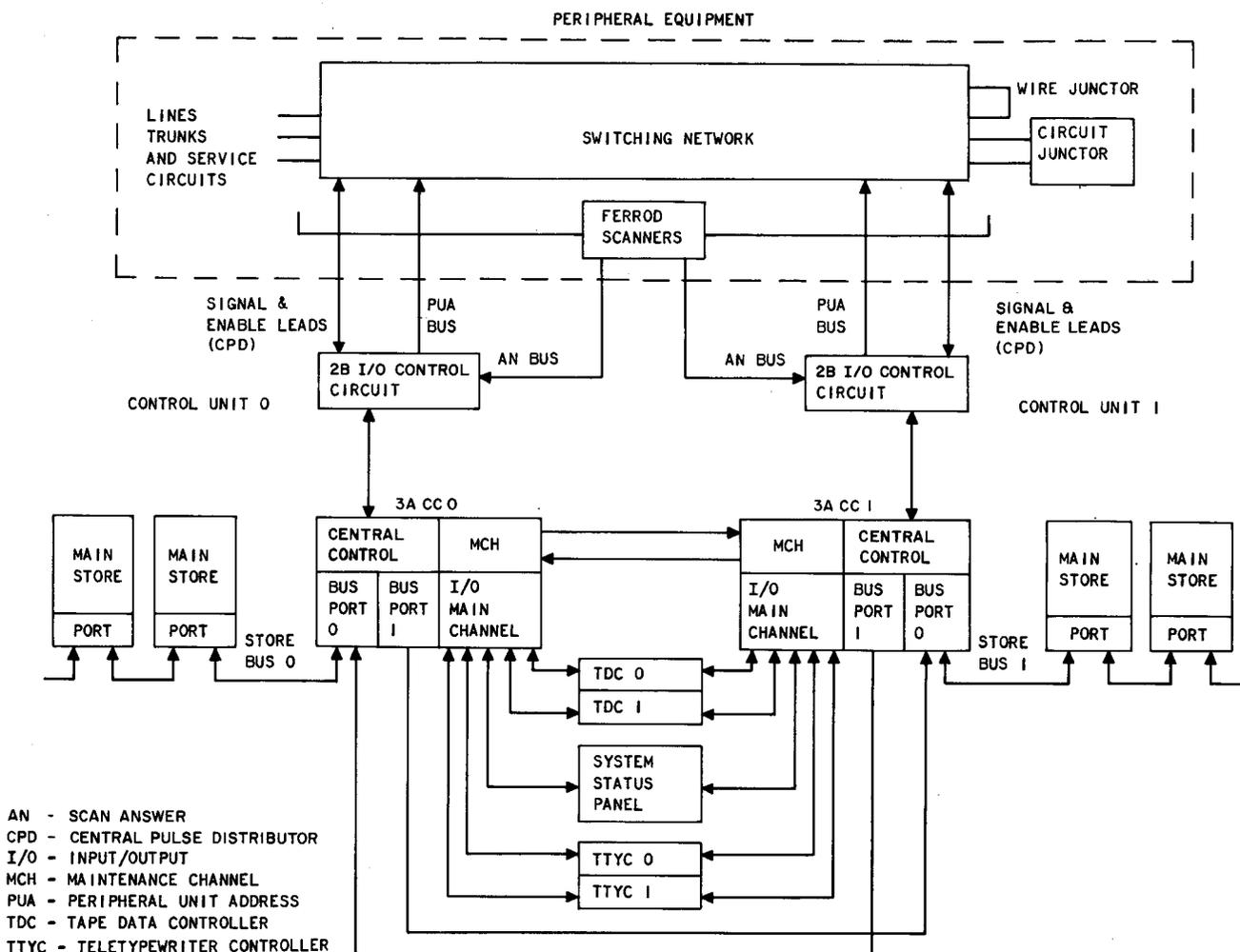


Fig. 8—No. 2B ESS Block Diagram

cable assembly. Some interconnections are by the coaxial cable type.

Functional Sections of 3A CC

3.11 The block diagram in Fig. 11 shows the functional sections within the 3A CC. These sections are as follows:

- System clock
- General registers
- Microprogram control
- Data manipulation logic (DML)
- Interrupt facility
- Main memory control
- I/O channels and controllers
- Maintenance channel and controller
- 3A CC control panel and interface
- Gating bus and bus parity checker
- Miscellaneous registers.

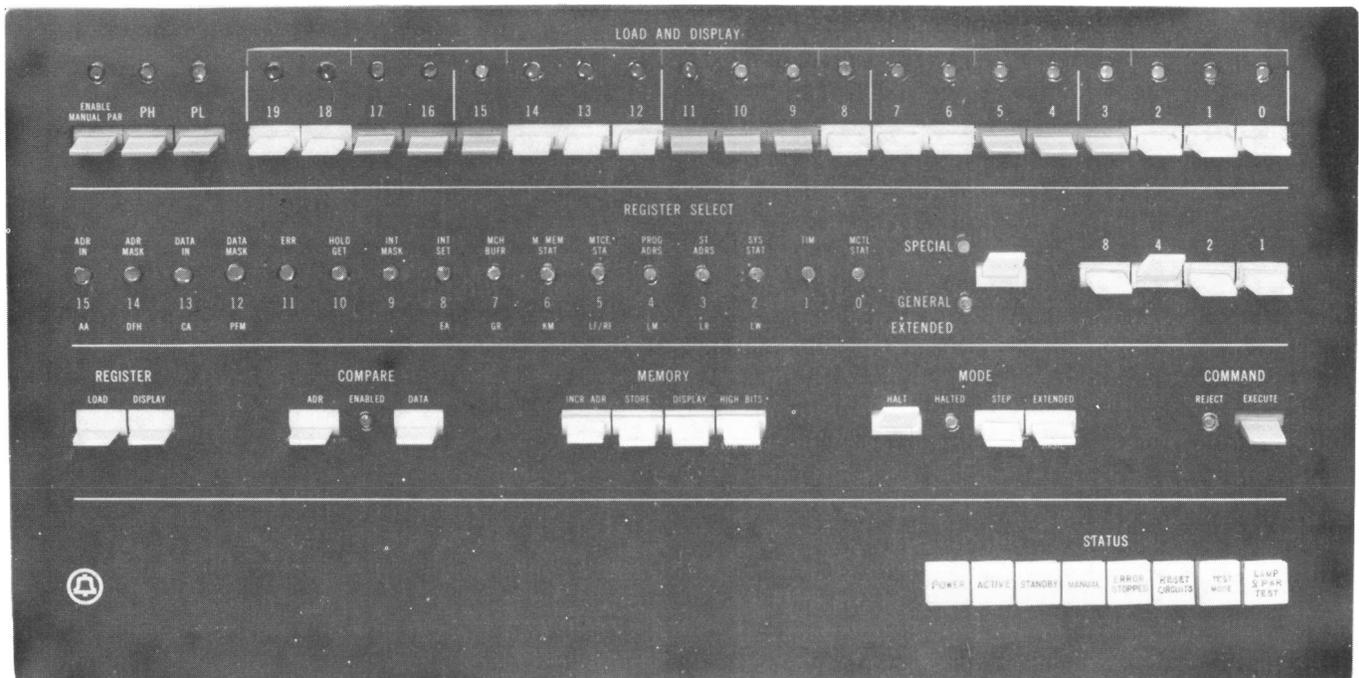


Fig. 9—3A Central Control

System Clock

3.12 The system clock supplies the basic timing pulses necessary to control system actions. Timing pulses generated by the system clock are used for controlling various system functions such as data timing, gate control, synchronization of events, etc. The basic timing signal is generated by a standard crystal oscillator and squaring circuit.

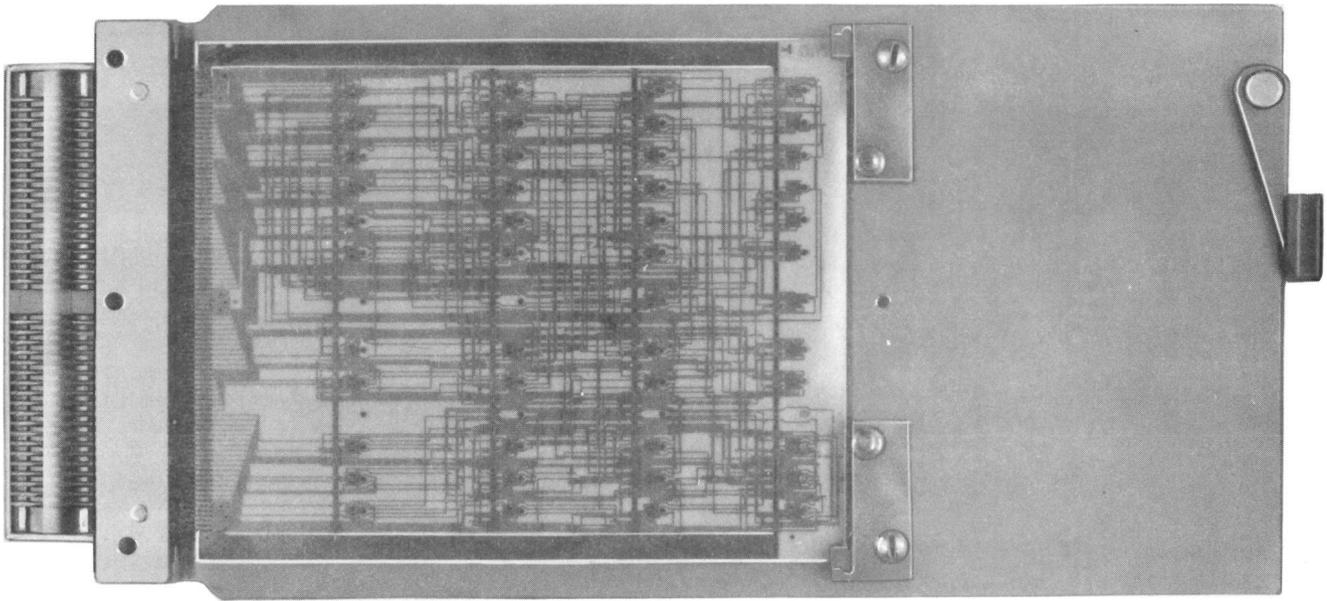
General Registers

3.13 The registers provide a quick access storage medium for storing data being used in the current processing operation. They also provide control and status information for system states, interrupts and errors. The two basic types of registers in the 3A CC are general registers and special registers. The general register organization provides for flexibility in data handling and processing. Each general register stores 18 bits: 16 bits of data and two parity bits. The special registers are dedicated to specific functions and, depending on those functions, may vary in length.

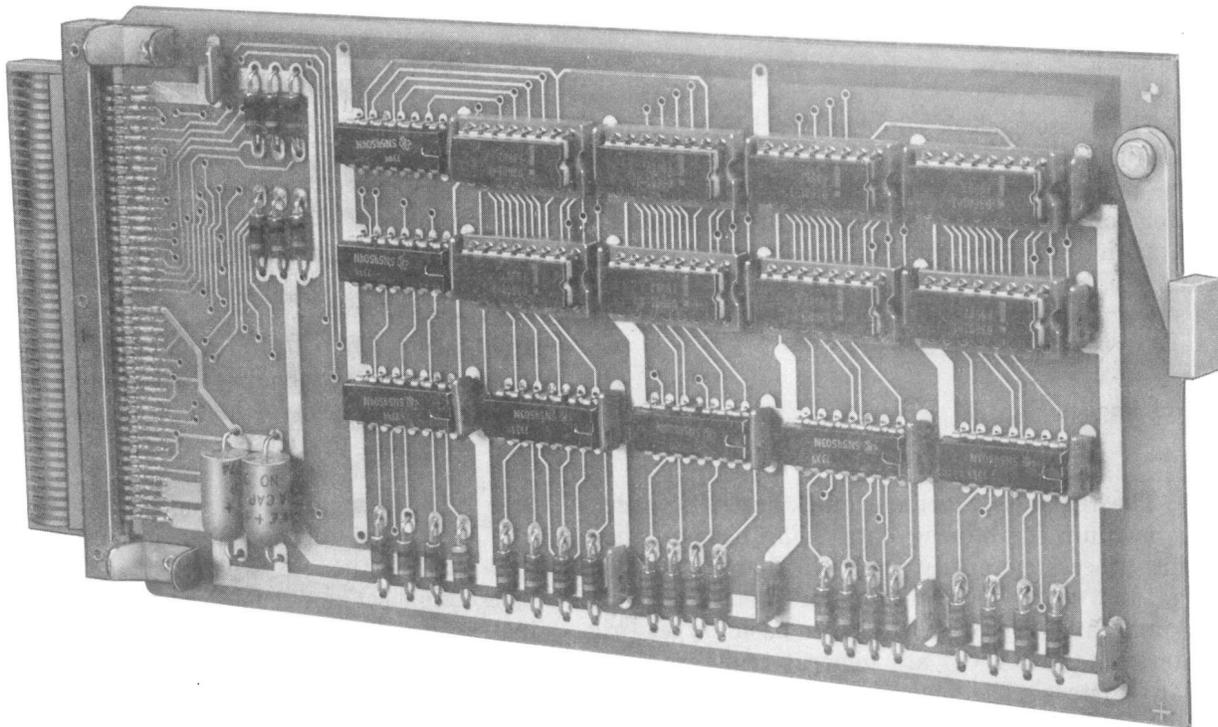
Microprogram Control

3.14 The microprogram control is the center of the 3A CC operation. It directs and controls the operations of the 3A CC by use of sequences of microinstructions. The microprogram control consists of a microstore, several special registers, decoders, translators, logic, and check circuits. These are combined to provide most of the complex controls and sequencing operations required to implement the system instruction set.

3.15 The internal sequencing of actions is controlled by a microprogram structure which results in a highly flexible means of implementing the instruction set and basic control functions. Each instruction which is read from program store is performed by a sequence of microinstructions within the microprogram control. The sequence of microinstructions performs various functions such as gating between registers, data manipulation, sending of control signals, etc, which are necessary to interpret and execute the instruction fetched from program store.



10A. FA-TYPE CERAMIC CIRCUIT PACK (PROTECTIVE COVER AND ENCAPSULATING MATERIAL REMOVED)



10B. FC-TYPE CIRCUIT PACK

Fig. 10—FA and FC-Type Circuit Packs

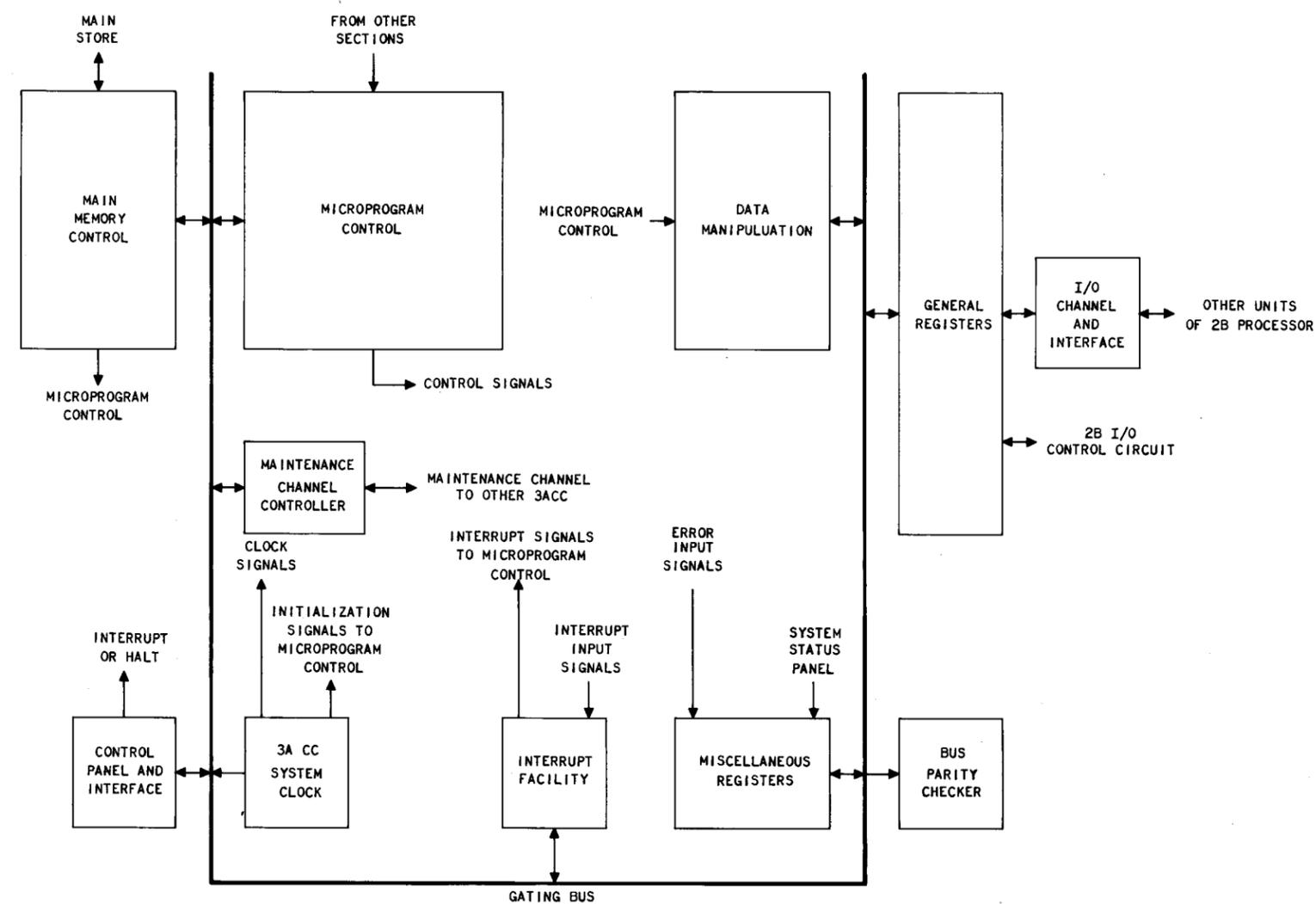


Fig. 11—3A CC Block Diagram

Data Manipulation Logic (DML)

3.16 The DML provides the special registers, matcher, parity generator, and logic necessary to perform such functions as addition, rotation, logical combinations (Boolean functions), and finding low zero. The DML is duplicated for reliability. After a desired function is performed, the results are compared by the matchers. All parity generation is done through this circuit.

Interrupt Facility

3.17 The interrupt facility provides the means of interrupting the program flow so that a timed or more urgent task may be performed. The interrupt facility consists of two special registers (interrupt set and interrupt mask) and interrupt logic which enables any desired input to the 3A CC to be recognized and serviced relative to its priority. Maintenance interrupts are initiated by some peripheral units and I/O errors or errors detected by self-checking circuits of the on-line or off-line CU. The 2B uses a 5 millisecond (MS) interrupt to drive both the 5 and 25 MS input/output programs.

Main Memory Control

Note: Detailed discussion of the main memory control is provided due to describe registers in the 3A CC used only in the 2B application.

3.18 The main memory control provides the interface between the 3A CC and main store (MAS) bus for accessing data from main store and for storing data in MAS. The 3A CC is designed to use a direct-coupled bus in an asynchronous mode. The address portion of the bus is unidirectional while the data portion is bidirectional. The state of the read/write (R/W) flip-flop determines the direction of the data portion of the bus.

3.19 The main memory control (Fig. 12) is made up of a control and sequencing portion and register interface portion. The registers are the main memory status (MMS) register, program address (PA) register, store address register (SAR), store instruction registers (SIR0 and SIR1), store instruction buffer (SIB), store data registers (SDR0 and SDR1), instruction buffer (IB) and the necessary control circuitry.

3.20 The main memory control performs the following functions:

- (a) Buffers the address, data, and control signals to be issued to the MAS bus
- (b) Determines the state of the MAS bus after receiving a memory request from the microprogram control
- (c) Activates a main store cycle if MAS bus is not busy
- (d) On instruction fetches, gates the SAR contents to the PA register so that the PA+1 logic can compute the next store address
- (e) Monitors the bus for a completion signal from MAS
- (f) Buffers the instruction, data, and control signals from MAS bus
- (g) On a read operation, gates the contents of the MAS bus to the SIRs or SDRs
- (h) Sets the data ready (DR) bit to indicate the end of a memory cycle.

3.21 The following provides a description of the main memory control registers.

- (1) **Main Memory Status (MMS) Register**—16-bit register used to store the present state of the main memory control and to formulate commands sent to main store. The bit designations and functions are shown in Table A.
- (b) **Program Address (PA) Register**—20-bit register used to store the last program address which was accessed from main store.
- (c) **Store Address Register (SAR)**—20-bit register which stores the address of the memory location which is to be fetched from memory.
- (d) **Store Instruction Registers (SIR0 and SIR1)**—16-bit registers used to buffer program instructions. SIR0 and SIR1 are both required for buffering 24-bit 2B instructions while only SIR0 is required for 16-bit 3A instructions.

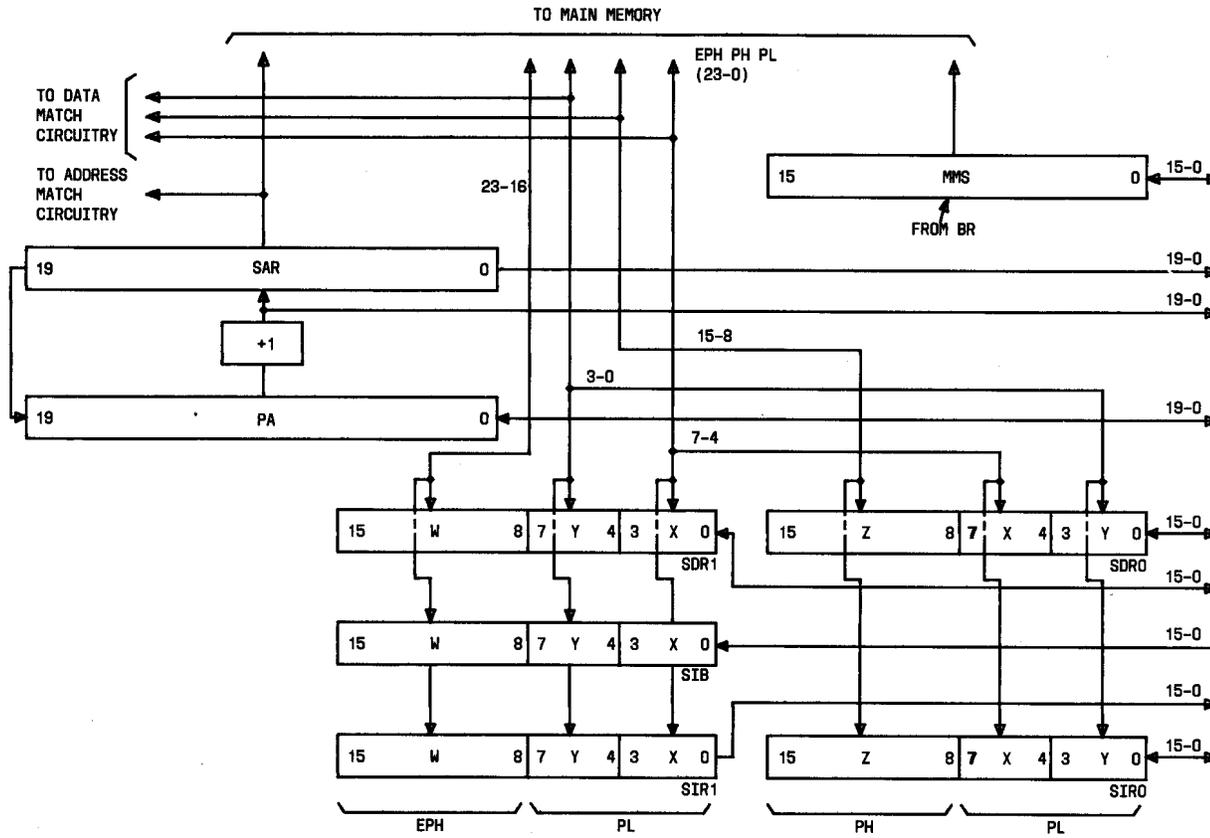


Fig. 12—Main Memory Control

(e) **Instruction Buffer (IB):** The IB is a 16-bit register used to temporarily store the present OP code and operand fields obtained from main store so that the next instruction can be accessed (put in SIR0 and SIR1) concurrently with the execution of the present one (in the IB). The low eight bits of the IB connect to translators which may be used in conjunction with the microcode to control gating, and to define various options or data fields.

(f) **Store Instruction Buffer (SIB)—**16-bit register used for buffering the second half of a 2B instruction before it is loaded into SIR1.

(g) **Store Data Registers (SDR0 and SDR1)—**16-bit registers used to buffer data. SDR0 and SDR1 are both required for buffering program and translation data while only SDR0 is required for buffering call store data.

TABLE A

DESIGNATIONS AND FUNCTIONS OF MAIN MEMORY STATUS REGISTER BITS

BIT	DESIGNATION	FUNCTION
0	Memory Maintenance (MM) 1	Used with MM2 and RW to formulate the command sent in a memory operation
1	MM1	Same as bit 0
2	MM2	Used with MM1 and RW to formulate the command sent in a memory operation
3	MM2	Same as bit 2
4	Read or Write (RW)	Indicates whether memory is to perform a read(1) or write(0) operation
5	RW	Same as bit 4
6	Idle (IDL)	If set, disables all communications to the other 3A CCs memory
7	IDL	Complement of bit 6. If set, disables all communications from other 3A CCs memory
8	Update (UPD)	Indicates whether or not to update the off-line memory
9	UPD	Same as bit 8
10	Isolate (\bar{X} SO)	Prevents the other 3A CC from accessing this 3A CCs memory
11	ISO	Same as bit 10
12	Block Double Store Read (BDSR)	Inhibits double store read
13	BDSR	Same as bit 12
14	Complement Write (CW)	Activates complement write lead of main store bus. Main store controller (MASC) will have last word, write complement of last word, and store in the complement in the last read address
15	Block Error Recovery (BEC)	Inhibits all error recovery procedures within the 3A CC associated with incorrect store read data

Read Operation

3.22 Instruction Fetch: The microcode determines when a new instruction is to be fetched from main store (Fig. 13). The fetch is initiated by the control bits (CA and CB) of the microinstruction register (MIR) which is located in the microprogram control. The enable instruction fetch signal from the binary decoder loads the SAR with the instruction address by gating the contents of the PA+1 logic into the SAR. The request (REQ) and instruction or data (ID) flip-flops are set while the data ready (DR) flip-flop (located in MCS register) is cleared. The REQ flip-flop buffers the store request in case the bus is busy. Setting the IF flip-flop gates the instruction from MAS to the store instruction register(s).

3.23 If the MAS bus is idle, the seize flip-flop is set to inhibit the other 3A CC from accessing the bus. The command, address, and go signals are gated onto the MAS bus. These signals are maintained until the 3A CC receives the store complete signal and the instruction is buffered in the store instruction register(s). The store complete signal sets the DR flip-flop indicating to the microprogram control that the instruction fetch is completed. A single register (SIR0) is required for buffering 3A instructions in the main memory control, while three registers (SIR0, SIB, and SIR1) are required for buffering the No. 2 and 2B instructions (Fig. 14).

3.24 When the DR flip-flop is set the contents of SIR0 are loaded into the instruction buffer (IB) and the contents of SIB are loaded into SIR1. The purpose of the SIB is to improve the efficiency of MAS operations when using the extended MAS bus interface for emulation of the No. 2 ESS half-word command structure. For example, when an instruction is loaded into the SIR0 and the SIB, the first half of a double-word instruction is executed and this first half comes from the SIR0. By gating the SIB to SIR1 when this first half-word instruction is initiated the main memory control is free to issue the next MAS request for an instruction read since both the SIR0 and the SIB are available.

3.25 A 3A double word instruction requires an additional store fetch during the microsequence to obtain the address or data portion of the instruction. This half of the instruction is also read into SIR0. The address or data is gated from

SIR0 to the proper registers for execution of the instruction.

3.26 The last instruction in a microsequence contains an all zeros NA field. This places all zeros in the NA field of the MIR. The microprogram control will loop on the all zeros location until the next instruction is fetched from main store.

3.27 If a No. 2B full word instruction is being executed, the microsequence will control the gating of the address of data portion of the instruction which is stored in SIR1. The address or data will be gated to the appropriate registers by the microsequence to complete the execution of the instruction.

3.28 At the end of the execution of the first half of a No. 2B half word instruction, the microcode transfers to the all zeros location. The contents of SIR1 are immediately gated to the IB and the OP code to the MAR and RAR. The second half word instruction which was buffered in SIR1 will be executed by the appropriate microsequence. During the execution of the instruction which was stored in SIR1, main store is usually addressed. When the microsequence for executing SIR1 is completed, an all zeros NA is reached again. The microprogram control will loop on the all zeros address until the next instruction fetch is completed.

3.29 The all zeros loop is necessary since at the end of a short microsequence the microprogram control must wait for the next instruction to be fetched from main store (Fig. 15). Whenever the all zeros location is read out of the microstore into the NA field, the interrupt lead is checked (except between half-word instructions). If an interrupt is present, whether a main store fetch is completed or not, the starting address of a microsequence to service the interrupt is hardware jammed into the MAR. If an interrupt is not present, the microprogram control loops on the all zeros location until the next instruction from main store is available and is loaded into the MAR by the load new OP code signal (LNOP). An output from the all zeros detector and an indication that the memory cycle is complete (DR=1) results in a new instruction being loaded.

3.30 Data Fetch: When an instruction requires data to be fetched from memory, the

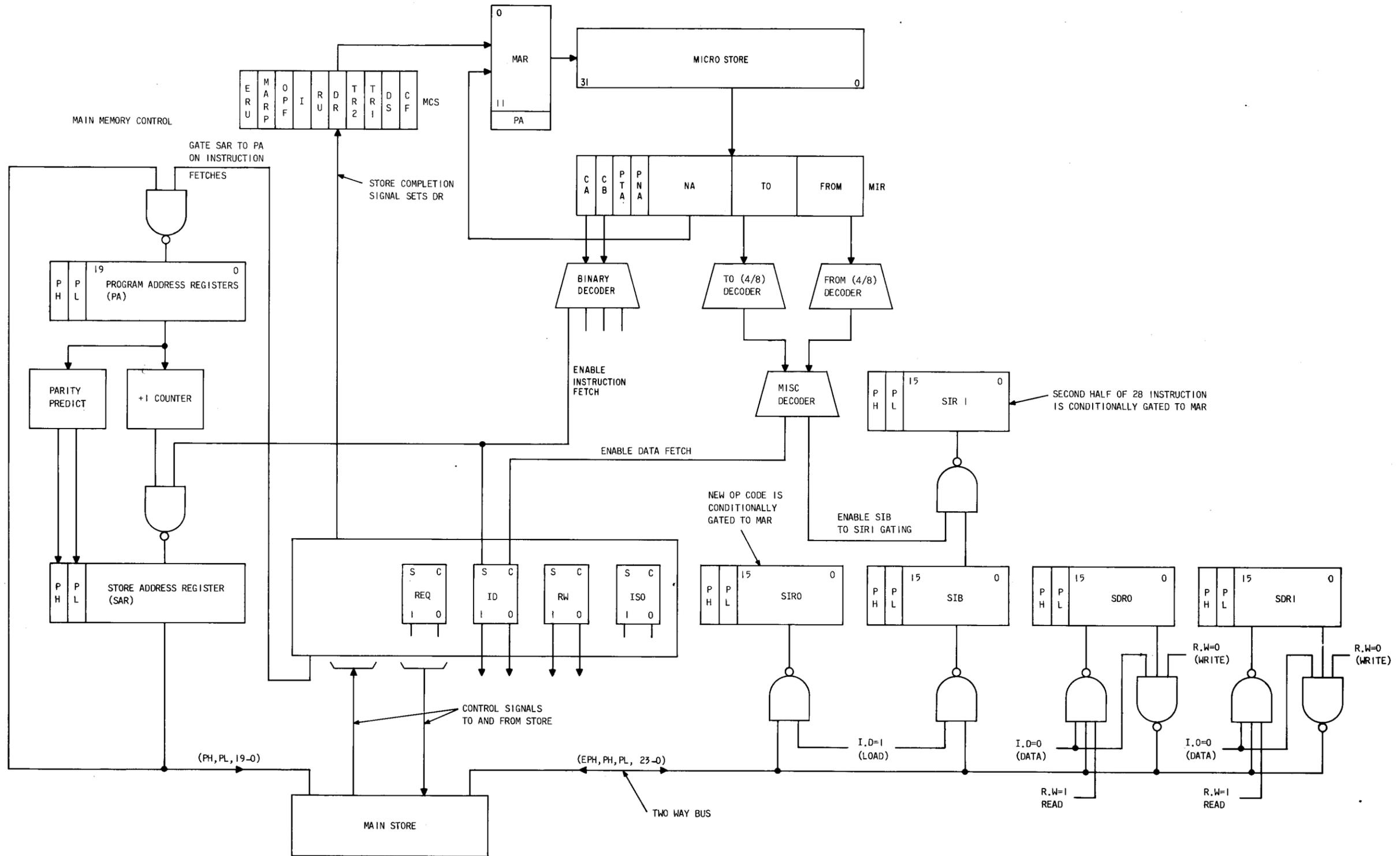


Fig. 13—Main Memory Control-Microprogram Control Interface

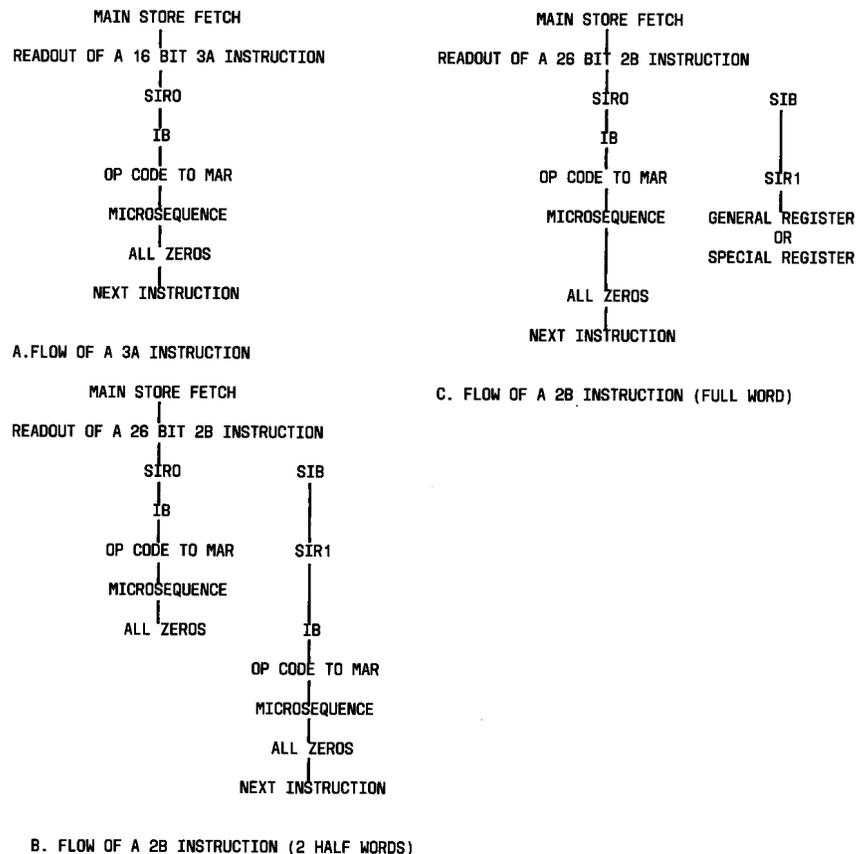


Fig. 14—Flow of 3A and 2B Instructions

microprogram loads the data address into the SAR. The data address may be loaded from another register or calculated within the data manipulation logic (DML). Once the data address is loaded in the SAR, a miscellaneous crosspoint initiates the store request by setting the REQ flip-flop. The ID and DR flip-flops are cleared. The ID flip-flop is cleared (see Fig. 13) to indicate that the information from memory will be gated into the SDR0 and SDR1 and to inhibit the SAR to PA gating. SDR0 and SDR1 are both required for buffering program and translation data while only SDR0 is required for buffering data pertaining to calls in progress.

3.31 When the memory bus becomes idle, an ISO flip-flop is set to inhibit the other 3A CC from accessing the bus. The command, address, and go signals are gated onto the bus. These signals are maintained until the 3A CC has buffered the memory response in SDR0 and SDR1 and set

the DR flip-flop. The setting of the DR flip-flop indicates to microprogram control when the data fetch is completed.

Write Operation

3.32 The data to be stored in memory is loaded into SDR0 and SDR1 (Fig. 13) and the address is loaded into the SAR. Both SDR0 and SDR1 are required for writing program and translation data while only SDR0 is required for writing call processing data into memory. The loading of the SDR(s) clears the read/write (R/W) flip-flop to indicate a write operation. The REQ flip-flop is set and the DR flip-flop is cleared.

3.33 The update (UPD) flip-flop is set unless the off-line CU is not operational, being diagnosed, etc. The data is written into the on-line and off-line stores to keep the standby store up-to-date in case a switch of the 3A CCs become necessary.

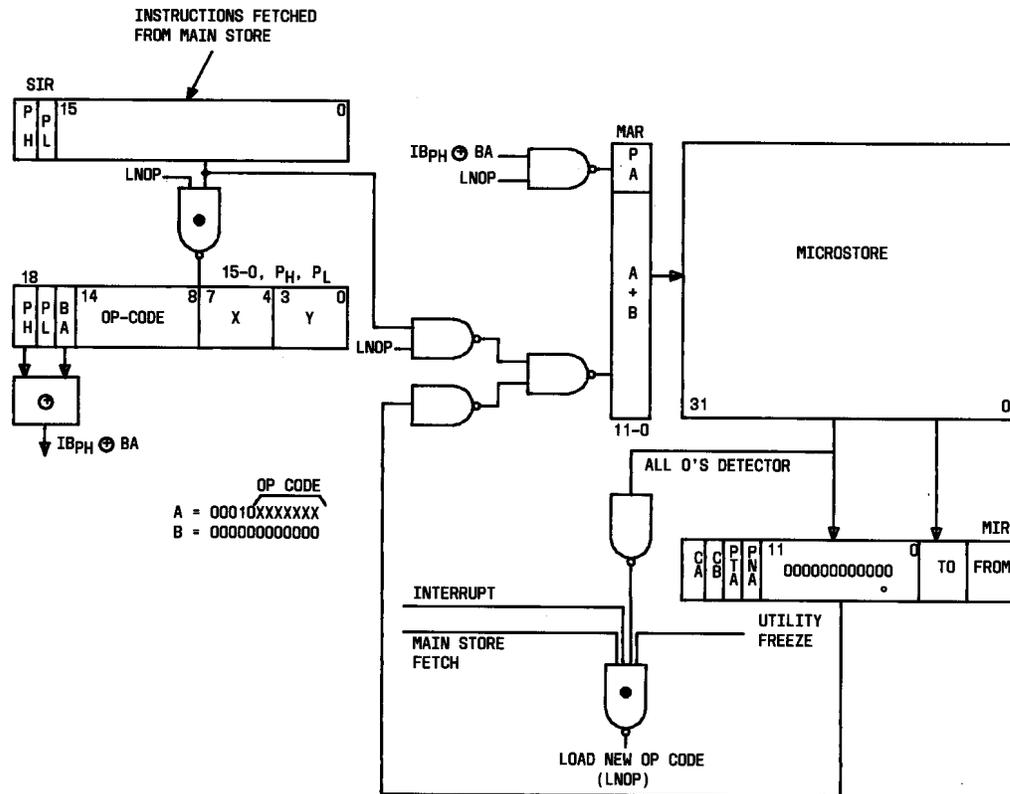


Fig. 15—Load New OP Code Operation

3.34 When the necessary bus becomes idle, the ISO flip-flop is set to inhibit the other 3A CC from accessing the bus. The command, data, address, and go signals are gated onto the bus. These signals are maintained until the 3A CC has buffered the memory response and sets the DR and R/W flip-flops. The setting of the DR flip-flop indicates to microprogram control when the write operation is completed.

I/O Channels and Controllers

3.35 The I/O channels are a means by which information is transmitted to or received from units which are designed to work with serial channels. The I/O channel controllers are the interface between the 3A CC and the units connected by the I/O channels. The 3A CC may control a maximum of 20 I/O main channels. However, for 2B use the addressing of two of these channels is dedicated to the 2B I/O control circuit. Each of the remaining 18 I/O main channel controllers can handle 20 I/O subchannels providing a maximum

of 360 I/O serial subchannels. Refer to Section 254-300-130 for a detailed description of the I/O channels and controllers.

Maintenance Channel and Controller

3.36 The maintenance channel (MCH) and controller provide the main source of communication between the 3A CCs for diagnostic and control unit switching purposes.

3A CC Control Panel and Interface

3.37 The 3A CC control panel provides a manual means for communication between the maintenance personnel and the 3A CC to aid in diagnostics and troubleshooting. The control panel interface consists of special registers (three switch registers display buffer, data input register, data mask register, address input register, address mask register), matchers, and interface logic.

Gating Bus and Bus Parity Checker

3.38 The gating bus is the communications path within the 3A CC. Most information is transferred between functional sections of the 3A CC via this gating bus. The bus parity checker tests the parity of the information placed on the gating bus to ensure its accuracy.

Miscellaneous Registers

3.39 The miscellaneous registers of the 3A CC contain a group of special registers and cable receivers. The cable receivers provide a means for receiving information from the system status panel. The special registers and their functions are as follows:

- (a) Hold-get register—provides a hardware-assisted subroutine facility
- (b) Error register—buffer for error signals
- (c) System status register—buffer for status and control information
- (d) Maintenance state register—buffer for testing purposes
- (e) C register—buffer used as a scratch area by the microprogram.

Interconnections Between 3A CC And Other Units

3.40 All interconnections between the 3A CC and other units (except for relay and power units) are accomplished by one of two types of cabling techniques (Fig. 16). The first type of cable is a 30-gauge, 31-conductor flat ribbon cable which uses a paddleboard assembly at each end; the second consists of coaxial cable which may use a conductor and paddleboard assembly at each end or a standard coax connector.

3A CC Functions in Relationship to Other System Units

3.41 The 3A CC is the controlling unit of the 2B processor and the entire system. The 3A CC is duplicated to provide continuous real-time operation with a high degree of system reliability. The 3A CC uses the program instructions and translation data stored in main memory to direct and control calls through the office as well as aid

in detecting and analyzing improper performance of the equipment involved in this task. One 3A CC always has active control over the system while the other 3A CC operates in a standby mode. Each 3A CC has its own dedicated main memory. The on-line 3A CC keeps both the on-line and standby memory up-to-date so that the standby 3A CC can assume control of the system with an up-to-date storage area.

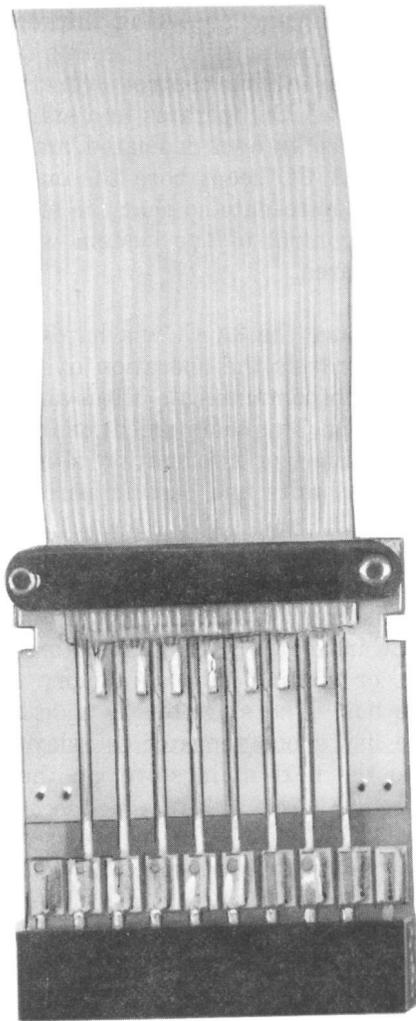
3.42 Since the 3A CC via hardware and software controls the operation of the office, it must be able to communicate with various units within the system. This communication involves the sending and receiving of information to and from other 2B processor units and certain peripheral units.

3.43 The store bus (see Fig. 8) is provided for communication between the 3A CC and the main stores. The functions performed by the 3A CC in relation to the main stores are the reading from or writing into a memory location via the store bus. The store bus is a dc bus. Each main store has a bus repeater to relay the information on to the next main store via the store bus.

3.44 The 3A CC is designed to use a direct-coupled bus in an asynchronous mode. The asynchronous mode of operation provides the system with the flexibility to use a refreshable integrated circuit memory and to advance with the state of the art. The address portion of the bus is unidirectional while the data portion of the bus is bidirectional.

3.45 A cross-coupling mechanism is used to allow the on-line 3A CC to communicate with the off-line store. This makes it possible to keep both stores updated and to perform the double store read function in the event of a parity error during the read operation of the on-line store. The on-line 3A CC will access the off-line 3A CCs main store for only one read operation during the double store read function.

3.46 The 3A CCs must be able to communicate with each other, since the 3A CC is duplicated for system reliability. The maintenance channel (see Fig. 8) provides this communication for diagnostic and control unit switching purposes via the maintenance channel (MCH) controller. The MCH is an asynchronous, semiautonomous data transfer system capable of serial ac data transfers at a rate of 6.67 megabits per second. It provides a half-duplex mode (one-way transmission at a



31-CONDUCTOR RIBBON
CABLE AND PADDLEBOARD
CONNECTOR



COAXIAL CABLES AND
PADDLEBOARD CONNECTOR

Fig. 16—Cabling and Connectors

time) of communication between the duplicated 3A CCs. This communication is necessary for one 3A CC to determine the state of the other 3A CC and for the on-line 3A CC to exercise the other 3A CC as well.

3.47 The MCH controller of the on-line 3A CC is used to perform the following functions in relationship to the other 3A CC:

- Arbitration of on-line/off-line status
- Periodic or diagnostic exercise

- Stopping
- Starting or initializing
- Updating the program timer
- Disabling the I/O
- Controlling the clock.

3.48 The maintenance channel controller consists of special registers (transmit/receive register, command registers, and buffer register), sequence

and control logic, error check circuits, bipolar drivers/receivers, and a command decoder.

3.49 The teletypewriter (TTY) and system status panel (SSP) provide an interface between the operating personnel and the system. The 3A CC communicates to them via their respective controllers, the TTYC and SSPC. The 3A CC communicates with the TTYC to perform the functions of outputting characters to the TTY and receiving input characters from the TTY. The 3A CC must also communicate with the SSPC to perform the functions of sending status information to the SSP and receiving manually requested panel operations. These functions for both TTY and SSP are performed over input/output (I/O subchannels which will be discussed in more detail in 3.55).

3.50 The tape cartridges of the No. 2B ESS provide a backup image of the program and translation data stored in the main stores in case a system failure should mutilate the store contents. The 3A CC must communicate with the tape data controller (TDC) to perform the functions of reading data from the tape or writing information on tape. These functions are performed between the 3A CC and the TDC over an I/O subchannel.

I/O Operations

3.51 The 3A CC has nine miscellaneous decoder control signals and three general purpose registers associated with I/O operations.

3.52 The miscellaneous decoder control signals are generated by the microprogram memory in the 3A CC. These control signals are used in the 2B I/O control circuit to enable gating paths, set or reset flip-flops, or initiate the execution of central pulse distributor or peripheral unit address pulses to control system units which provide service.

3.53 The general registers R9, R10, and R11 (Fig. 17) serve particular functions concerning the I/O operations:

- (a) The control buffer (R9) controls the state of the I/O main channels or the 2B I/O control circuit.
- (b) The output buffer (R10) is used to gate information to the I/O main channels or the 2B I/O control circuit.

- (c) The input buffer (R11) is used to receive data from external units via the I/O main channels and the 2B I/O control circuit.

When these registers are not being used for their I/O functions, they are used as general registers.

3.54 Bits 10 through 15 of R9 are encoded in a 3-out-of-6 code which allows a 1-out-of-20 selection. Eighteen of the 20 possible combinations are used as I/O main channels of the 3A CC. The other two codes are used to access the 2B I/O control circuit which provides parallel communications to the periphery.

I/O Main Channel and Controller

3.55 The serial I/O main channels can be used to communicate with peripheral equipment designed to work with serial channels. Each I/O main channel contains a controller which can handle 20 serial I/O subchannels. The I/O channel controllers are the interface by which information is communicated between the rest of the 3A CC and the other 2B processor units. An I/O channel controller consists of special registers (I/O status register and I/O data register), sequence and logic, decoders, bipolar drivers, bipolar receivers, and error check circuits. The initial system design uses the subchannels of one I/O main channel to communicate with the teletypewriter controllers, tape data controllers, and the system status panel.

B. 2B Input/Output Control Circuit

3.56 The 2B I/O control circuit, performs the interfacing function between the new high-speed processor and the relatively low-speed peripheral equipment (Fig. 18). The 2B I/O control circuit is the buffer circuit through which inputs are received into the processor and from which outputs are transmitted to the peripheral equipment. Every function performed by the 2B I/O control circuit is initiated by miscellaneous decoder control leads from the 3A CC. Refer to Section 232-309-108 for a detailed description of the 2B I/O control circuit.

Communication Links to 3A CC

3.57 The 3A CC has nine miscellaneous decoder control signals, sixteen control and status leads and three general purpose registers (R9, R10, and R11) associated with I/O operations. The

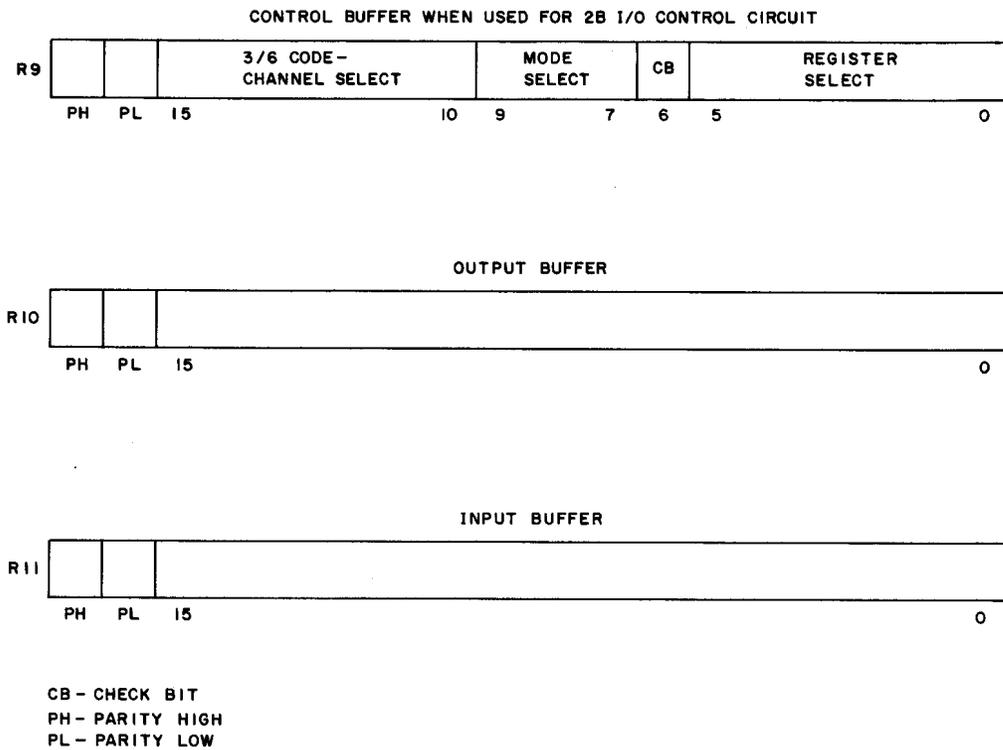


Fig. 17—I/O Register Assignment

miscellaneous decoder signals are generated by the microprogram instructions in the 3A CC. These signals are used in the 2B I/O control circuit to enable gating paths to or from control registers in the I/O, set or reset registers, or initiate the execution of CPD, dial pulse timing, data timing, and PUA pulses. The miscellaneous decoder control signals are only active in the 2B I/O control circuit when the proper 3-out-of-6 codes are decoded. The control leads include the 3A CC system clock phases, a 1.25 millisecond interrupt signal, 2B I/O control circuit error checking information for the CU, and leads which determine if the 2B I/O control circuit is on-line or off-line.

3.58 Register R10 is used to buffer information from the 3A CC to the 2B I/O control circuit. Register R11 is used to buffer information from the 2B I/O control circuit to the 3A CC. Register R9 controls the state of the 2B I/O control circuit when loaded with the appropriate 3/6 selection code. These three registers (R9, R10, and R11) can be loaded and read under control of either the microprogram or main store program.

Communication Links to the Peripheral Units

3.59 Communication between the peripheral equipment and the 2B I/O control circuit is via the peripheral unit address (PUA) bus, the scanner answer (SA) bus, the central pulse distributor (CPD), the dial pulse timing bus, and the data timing bus (see Fig. 18).

Peripheral Unit Address Bus

3.60 The PUA bus contains the transmission lines over which the peripheral units receive address information from the 2B I/O control circuit (Fig. 18). The PUA bus from each 2B I/O control circuit branches out of the PUA bus drivers, Fig. 19 (one east branch and one west branch). Each branch contains 38 twisted pairs. Each twisted pair is an individual 100-ohm balanced ac transmission line.

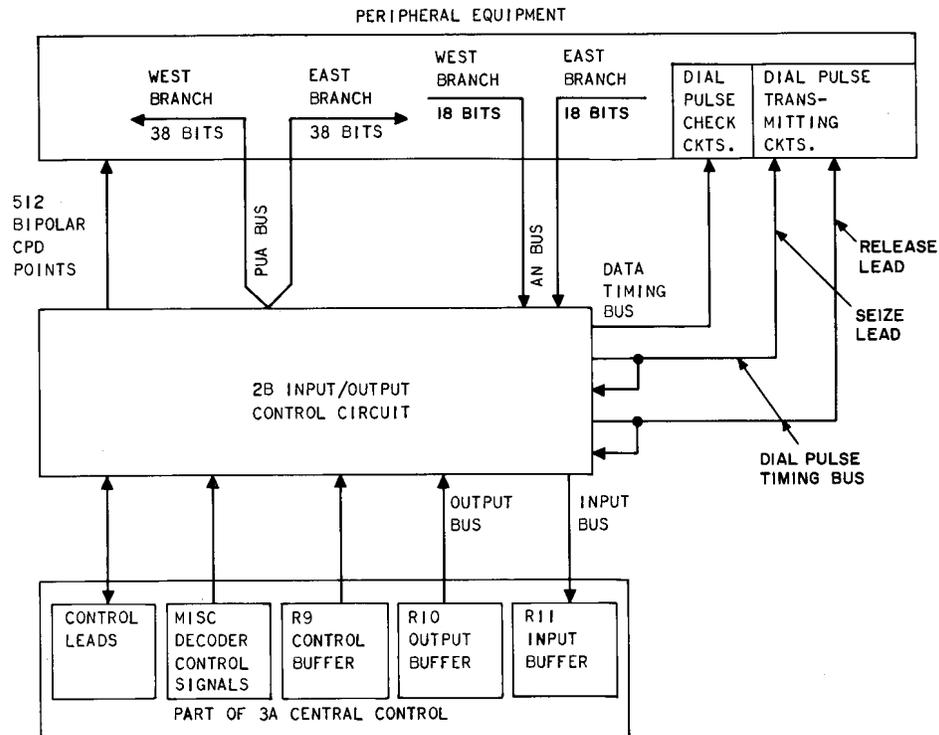


Fig. 18—Simplified 2B Input/Output Control Circuit Bus Connections

Scanner Answer Bus

3.61 The SA bus (see Fig. 18) contains the transmission lines over which scanner ferrod row information is received into the scanner answer register in the I/O control circuit. The AN bus has an east and a west branch similar to the PUA bus. Each branch contains 18-twisted pairs which has 16 scanner leads, an all-seems-well bit, and an enable verify bit. Each twisted pair is an individual 100-ohm balanced ac transmission line.

3.62 The pulses returned from the scanner on bits 0-15 of the SA bus set corresponding bits in the scan answer (SA) register. The all-seems-well (ASW) bit 16 and enable verify (EV) bit 17 associated with this bus are used to set two bits of the I/O error register. The contents of these two bits can be used by the 3A CC in

order to check for the proper execution of peripheral orders.

Central Pulse Distributor

3.63 The CPD is an integral part of the 2B processor and is directly controlled by input-output registers and control signals from the 3A CC. Signals from the CPD are used for the following:

- Selecting and enabling a peripheral unit to receive information from the output bus (PUA bus)
- Communicating with a shift register device via a stream of positive and negative pulses.

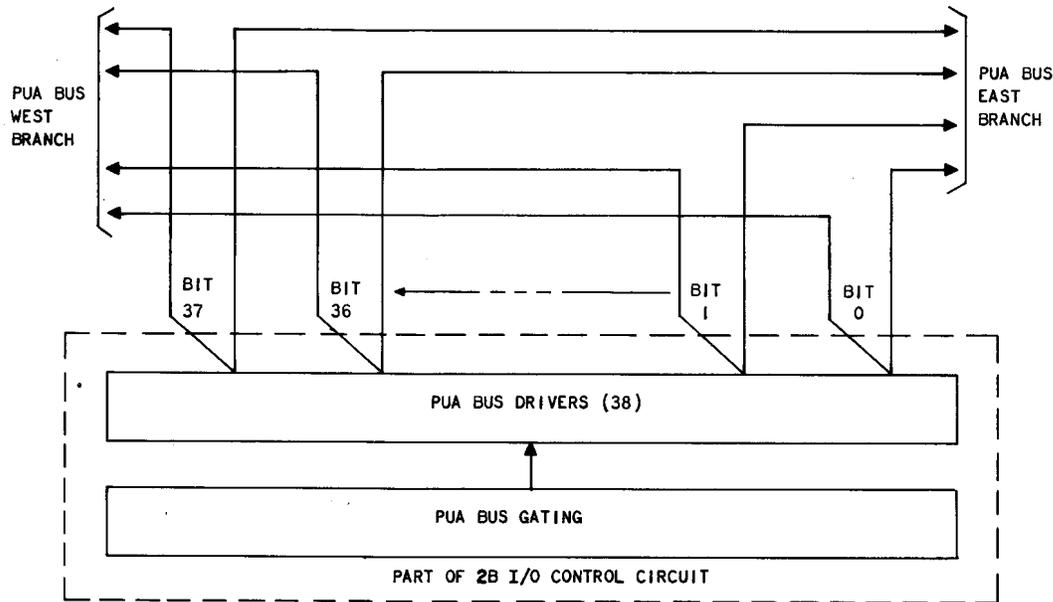


Fig. 19—Peripheral Unit Address Bus Branches

3.64 There are up to 512 bipolar output points in the 2B I/O control circuit. The CPD is used to perform either enabling or signaling. Many of the peripheral units receive their orders from the 2B I/O control circuit over a common bus system, the PUA bus. Enabling pulses from the CPD are used to direct a particular peripheral unit to receive the information appearing on the PUA bus. The enabling signal must be sent to a particular unit before the data is gated onto the PUA bus.

3.65 Signaling directly from the CPD (Fig. 20) is accomplished by sending bipolar outputs over single output pairs. These bipolar outputs can be used to control remotely located ac bipolar flip-flops or the load shift register circuits such as the peripheral decoders or network controllers.

3.66 A matrix CPD arrangement is employed to drive the 512 bipolar CPD points. A pair of 1-out-of-32 point 1A logic translators controls 32-horizontal and 32-vertical matrix driver circuits. The CPD matrix contains 512 transformers, each with a load resistor and a pair of selection diodes. A combination of digital and analog check circuits are used in order to make the CPD self-checking and easily diagnosable.

3.67 When more points are required, supplementary CPD (SCPD) frames (Fig. 21) can be added to control peripheral decoders. Figure 22 illustrates the relationship between the SCPD and the 2B I/O control circuits. Each SCPD frame also contains 512 bipolar SCPD points. CPD and SCPD points are individually connected via dedicated pairs to the points controlled.

Dial Pulse Timing Bus

3.68 The dial pulse timing bus provides the seize and release pulses to the dial pulse transmitting circuits which are located in the peripheral equipment. The seize and release pulses are used to set and reset flip-flops in the dial pulse transmitting circuits. Timing is provided for a 10-pulse per second (10 pps) dial pulse sending rate by the 5 msec interrupt program. The seize and release pulses are transmitted to the dial pulse transmitting circuits via separate wire pairs (see Fig. 18).

Data Timing Bus

3.69 The data timing bus (see Fig. 18) provides a 600 nanosecond (NS) pulse every 1.25 ms to the dial pulse check circuit that is located in the peripheral equipment. The data timing bus consists of a single output pair and a termination.

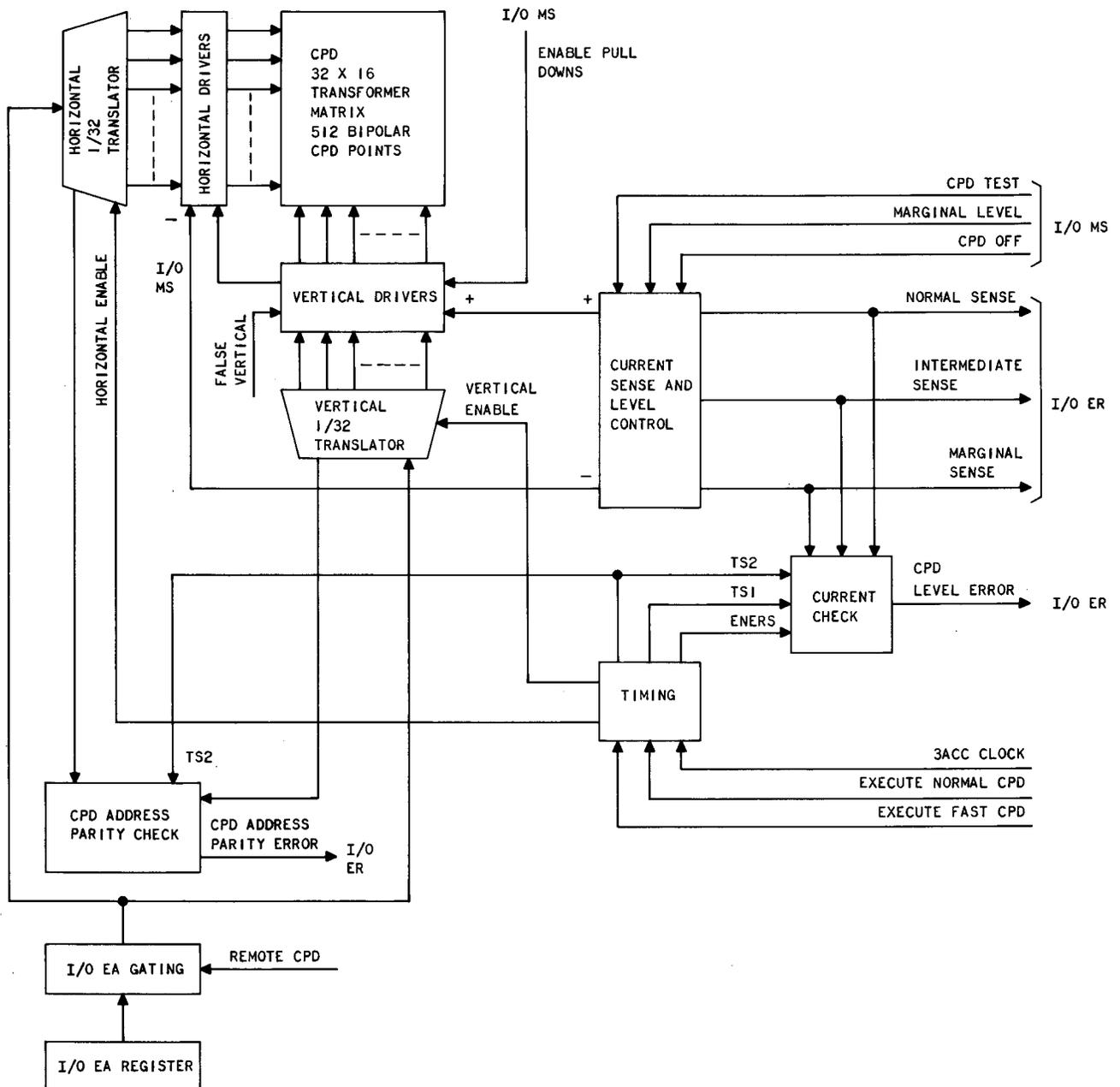


Fig. 20—Central Pulse Distributor

3.70 Refer to Section 232-309-108 for a functional description of the 2B I/O control circuit.

C. Main Store

3.71 The main store (MAS) is the means of storage for the program instructions and

temporary memory used by the 3A CC to direct and control system actions (Fig. 23). The main memory of each 3A CC is composed of at least one store. This store contains a main store controller (MASC) and one to four main store memory units (MASM) with a maximum of 256 K words of storage (where K = 1024 words). This

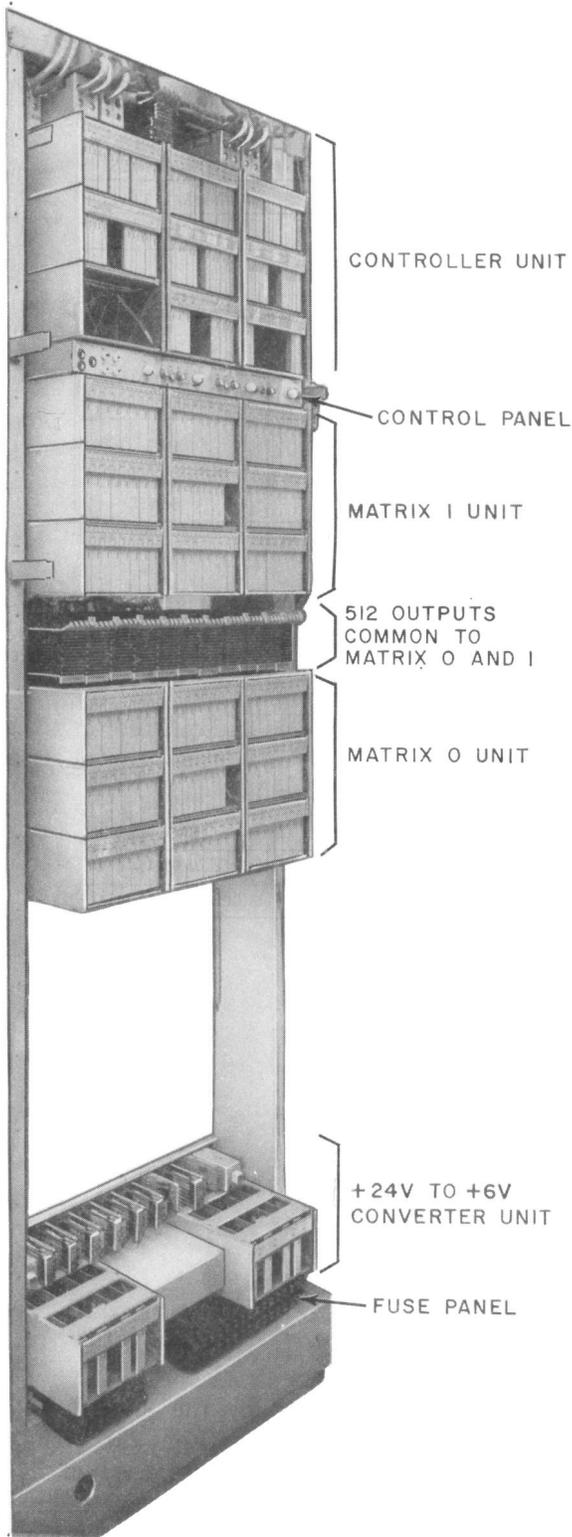


Fig. 21—Supplementary CPD Frame

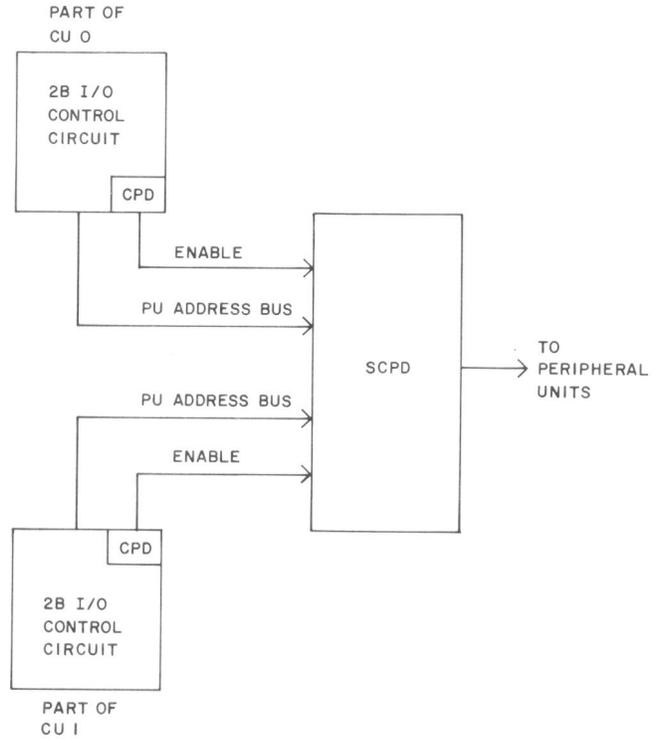


Fig. 22—Relationship of 2B I/O Control Circuits to SCPD

memory is growable in increments of 32K words. Refer to Section 254-300-150 for a detailed description of the MAS.

3.72 The main memory is functionally divided as follows:

- Program store which contains the generic program, parameter, and translation data
- Call store which is used by the 3A CC as a means of storage for transitory data.

3.73 In normal operation, the on-line 3A CC keeps the standby call store up-to-date. In other words, the on-line 3A CC not only writes into its own main store, but also into the main store of the other 3A CC as well. This is done to keep the standby CU ready to take control from the on-line CU in case a trouble is encountered.

3.74 A main store consists of up to eight main store memory modules (MASMO) and one MASC. The MASC is capable of driving all eight

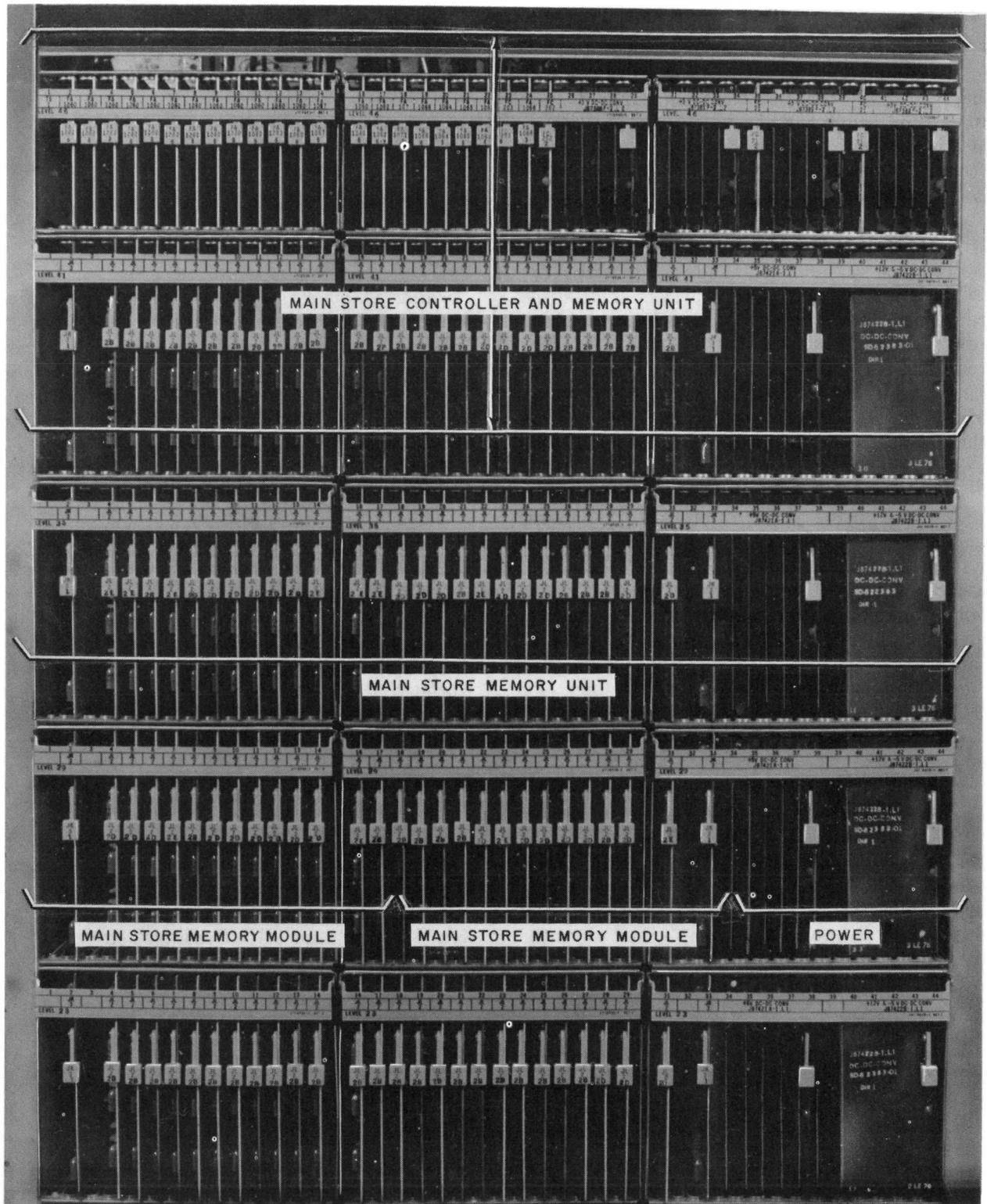


Fig. 23—Main Store

modules in the main store. Each module contains 32K of main memory.

3.75 Up to 256K of main memory (unduplicated) is mounted under each of the two 3A CCs in the 2B processor frame. Another 512K of main memory (duplicated) can be added in supplementary main store frames. Ultimately, the main memory can consist of three main stores (duplicated) with a maximum capacity of approximately 768K words.

3.76 The MASC (Fig. 23) serves as the interface between the 3A CC and the MAS. The MASC is composed of 21 circuit packs, 13 bit-sliced boards (BSB), one timing board (TB), two check boards (CHKBA and CHKBB), two maintenance boards (MTCBA and MTCBB), one command board (CMDB), and one clock board (CKB) and one parity generator board. For more detailed information on the main store refer to Section 254-300-150.

3.77 The main memory is a dynamic, volatile semiconductor type of storage. Dynamic means that the memory is not permanent and must be refreshed at defined intervals (2.2 msec) to preserve the stored information. Volatile means that power is required to retain the store information. If a total power failure occurs a "bootstrap" operation can be performed to reload the information into the MAS from the backup tape system (see 3.103).

Memory Cell

3.78 The insulated-gate-field-effect transistor (IGFET) is used in the memory cell of the main memory. The IGFET is a field effect transistor whose gate is insulated from the semiconductor by a thin intervening layer of insulator, usually thermal oxide. Basically, the

memory cell is made up of three IGFETs and a capacitor. The condition of the capacitor is used to store a 1 or a 0 in the memory cell.

3.79 Three cycles are associated with the memory cell as follows:

- Read cycle
- Write cycle
- Refresh cycle.

Reading a memory cell involves determining whether the capacitor is charged. Writing into a memory cell is accomplished by either storing or removing a charge on the capacitor. A memory cell must be refreshed on a periodic basis since the capacitor will eventually discharge to a point that the stored information is lost. During a refresh cycle the information read from a memory cell is automatically inserted back into the memory cell.

3.80 Program instructions and data are stored in 26-bit words each of which consists of 24-data bits and two parity bits (Fig. 24). The parity low bit (PL) provides parity for bits 0 through 7 and 16 through 19. The parity high bit (PH) provides parity for bits 8 through 15 and 20 through 23.

D. Power and Fuse Units

3.81 The power unit contains the dc-to-dc converters necessary to convert the -48 volts input to 3 volts at 8 amps and +5 volts at 4 amps. The +3 volt and +5 volt sources are required by the 3A CC, MAS and 2B I/O control circuit.

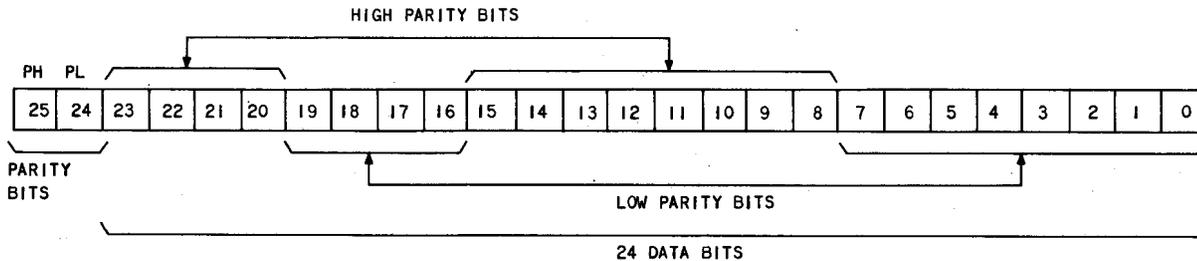


Fig. 24—26-Bit Data Word Layout

3.82 Power is supplied to the frame from a power distributing frame. A triple power feeder feeds +24 volts, -48 volts, and ground. The power feeders are connected to cables which run through the hollow frame uprights to the base of the frame. The filters in the base of the frame filter the 24-volt supply while the 48-volt supply is filtered by the converters. Cables connect the filters to the fuse unit providing fusing and power to all units in the frame and the fuse alarm circuitry.

2B MAINTENANCE FRAME

3.83 The 2B maintenance (MTCE) frame provides the interface between the maintenance personnel and the system. The maintenance personnel can access and control the system through the TTY and the system status and control panel. The MTCE frame was designed as a system maintenance tool for an operating office. The MTCE frame performs the following functions:

- An in-service monitor of the status of the system
- As the test and control center for routine functions
- Provides backup image of the program, and translation
- Provides (optional) remote maintenance capability.

3.84 The MTCE frame (Fig. 25) is a single bay frame and contains the following equipment:

- Maintenance TTY
- Up to 4 TTY controllers
- SSPC circuit
- 2 tape data controllers (TDC)
- Power unit
- Optional E2A telemetry unit.

A. MTCE Teletypewriter

3.85 The primary means of communication between the maintenance personnel and the

2B processor is the MTCE TTY. The maintenance personnel can request via TTY input messages specific actions to be performed by the system. In reply to these input messages, the system acts on the requests and reports on the actions completed. The system reports on the actions through TTY printouts and lamp indicators on the system status panel.

3.86 Normally a model 35 keyboard send-receive (KSR) teletypewriter set is mounted in the MTCE frame. The model 35 KSR is an electromechanical device capable of message transmission at 100-words per minute. All messages received or transmitted are typed on continuous paper.

3.87 Operating personnel can command and interrogate the system by typing input messages per the Input Message Manual (IM-2H200). The system will act upon the input messages and report the results of the action via an output message on the TTY. All output messages are defined in the Output Message Manual (OM-2H200). Programmed diagnostic tests are performed on the system at predetermined times. The TTY provides a printout of all diagnostic tests. The printout is in a coded format. By using a trouble locating manual (TLM) the code can be translated into the probable causes of the system failure. Recent change updates (translations) and change in program store (CHIPS) word procedures can be performed via the TTY.

3.88 A functional description of the TTY facilities used in the No. 2B ESS offices is provided in Section 254-300-190.

B. Teletypewriter Controllers

3.89 The purpose of the TTY controllers is to provide a controlling interface between the 3A CC and the TTY for system maintenance and a variety of administrative tasks. The controller connects the 3A CC and up to four TTY ports in a hub arrangement whereby signals from any one are seen by the others.

3.90 Each TTY unit contains mounting apparatus for two TTY controllers. Two 58C apparatus mountings, one on each end of an 8-inch mounting plate, provide space for four 108-type circuit packs or four AR17 circuit packs or any combination of the two per controller. The unit is wired so that either a 108-type circuit pack or an AR17 circuit

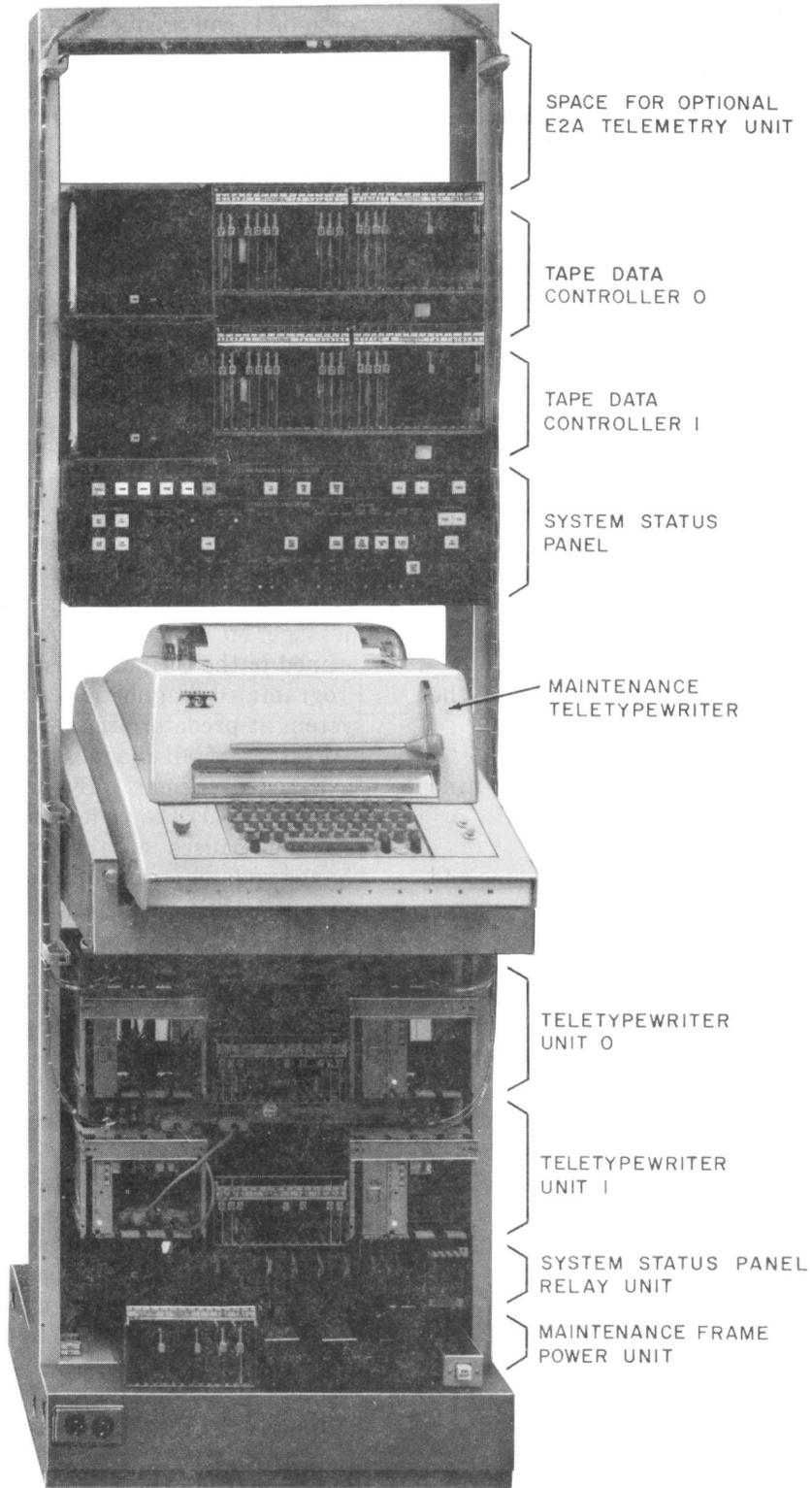


Fig. 25—Maintenance Center Frame

pack may be inserted into the same position. Since the controllers are provided on pluggable circuit packs, only one TTY controller need be equipped at a time. The unit also houses all required data sets for either local or remote TTY operation.

3.91 TTYC Mate Operation: Information which is transmitted to the local maintenance (LM) TTY from the 3A CC is also transmitted to the remote maintenance (RM) TTY through the mate operation of the TTYCs (Fig. 26). Conversely, the same applies to information transmitted to the RM TTY. This is accomplished through a cross coupling of TTYC-0 and TTYC-1. The LM TTY is connected to port 0 of TTYC-0 and the RM TTY is connected to port 0 of TTYC-1. Port 2 of TTYC-0 is cross coupled to port 3 of TTYC-1 and port 2 of TTYC-1 is cross coupled to port 3 of TTYC-0. If TTYC-0 is removed from service due to a fault, the 3A CC can communicate with the LM TTY through TTYC-1 via the cross coupling mechanism. The 3A CC also has access to the RM TTY through TTYC-0, via the cross coupling mechanism, if TTYC-1 is removed from service.

3.92 An 80A apparatus housing is mounted between the two 58C apparatus housings. It provides space for six controller logic circuit packs (three per controller), and two power supply circuit packs.

3.93 Directly above the three apparatus housings is a connector plate assembly. This connector plate assembly contains the connectors required to interface with the 3A CC and the TTYs. Six coaxial cable connectors are mounted on each end of this connector plate to provide the unit with the necessary inputs and outputs from the 3A CC. The remaining eight connectors provide an interface with the TTYs. A power key/lamp is mounted in the center of the connector plate.

C. System Status Panel and System Status Panel Controller

3.94 The system status panel and system status panel controller (SSPC) are located in the upper midsection of the MTCE frame. The system status panel is mounted on the front of the SSPC and provides a communication link between the maintenance personnel and the system. Numerous lamps and keys appear on the panel (Fig. 27) which display the status of the system and provide control

of the system. The main functions of the system status panel and its controller are as follows:

- Visual indicator of the status of the major system units
- Emergency control when manual intervention is needed.

The SSPC interface between the optional E2A telemetry and the 3A CCs for switching control center (SCC) application. Refer to Section 254-300-180 for a detailed description of the system status panel. The peripheral unit status display (see Fig. 27) is the only portion of the system status panel which is unique to No. 2B ESS.

3.95 The system status panel is divided into two parts; the SYSTEM STATUS AND CONTROL which reflects the general system condition, and the SYSTEM EMERGENCY MANUAL CONTROL which is used to stabilize the system via manual intervention during an emergency situation.

3.96 The SYSTEM STATUS AND CONTROL portion of the panel is primarily a display of system health. The display reflects the state of the flip-flop memory element in the SSPC. These flip-flops, in most cases, are controlled and, in all cases are readable via I/O messages from the 3A CCs. The only lamps or key/lamps not associated with a flip-flop logic element are CIRCUIT POWER, LAMP AND POWER TEST, and LAMP POWER.

3.97 The SYSTEM EMERGENCY MANUAL CONTROL portion of the panel is a means to manually restore the system to a healthy state during service affecting trouble conditions. Its operation is more complex than that of the SYSTEM STATUS AND CONTROL portion since several functions require interaction of various keys and circuit logic. For example, the initialization functions such as recent change and stable require the operation of several keys and circuit logic.

3.98 The SSPC is the interface between the 3A CC and the E2A telemetry interface, system status panel and system status panel relay (SSPR) circuits. Figure 28 is a functional block diagram showing the units and their relationship to the rest of the SSPC.

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3.99 The SSPC/3A CC interface packs contain the necessary registers, transmit and receiver transformers, parity checker and generator, etc., to allow communication between 3A CCs and the rest of the SSPC.

3.100 The system status panel interface packs contain the interlocking logic for certain keys and flip-flops associated with the system status panel keys and lamps.

3.101 Both the E2A unit and the E2A interface packs are optional. If equipped, the E2A interface packs provide buffering between the panel interface and the E2A unit.

D. Maintenance Relay Unit

3.102 The maintenance relay unit contains ten AF-10 relays that connect power under certain conditions to the following circuits in the office:

- (a) Alternate bus
- (b) Alarm transfer
- (c) Battery alarm
- (d) Circuit power, Bus A
- (e) Circuit power, Bus B
- (f) Critical alarm
- (g) Emergency line transfer
- (h) Inhibit building alarm
- (i) Major alarm
- (j) Major power alarm
- (k) Minor alarm
- (l) Minor power alarm
- (m) Test control.

E. Tape Data Controller (TDC)

3.103 Two TDCs (Fig. 29) are provided for bulk data storage on magnetic tape. The units are duplicated for system reliability. This storage

serves two purposes. First, a backup image of the program and translation data is kept on tape in case a system failure should mutilate the store contents. Secondly, a copy of the data needed to return translations to the state prior to the last update is kept on tape.

3.104 The TDC utilizes the KS-21447 L2, mini-recorder. The main features of the mini-recorder are:

- Four-track read-after-write head
- Four-track erase head
- End-of-tape sensing
- Beginning of tape sensing
- Cartridge in place sensor
- Write protect sensor
- Two pushbuttons for manual rewind and unload operation.

Refer to Section 254-300-170 for a detailed description of the TDC.

3.105 The TDC utilizes a new KS-coded cartridge (KS-21439 L1) which uses a band drive system. Since there is only one point of contact between the transport and the cartridge for any tape motion, a single drive motor is used. This motor is driven in the forward or reverse directions at 30 or 90 inches per second. Tape tension is internally controlled by the band in the cartridge. The cartridge has a maximum unformatted storage capacity of 20 megabits and a transfer rate of 48K bits/second.

3.106 The TDC provides the following:

- An asynchronous interface and control unit between the 3A CC and a cartridge transport
- A similar optional interface with a synchronous data set
- Bulk data storage
- Non-resident program storage for (2B-EF-2).

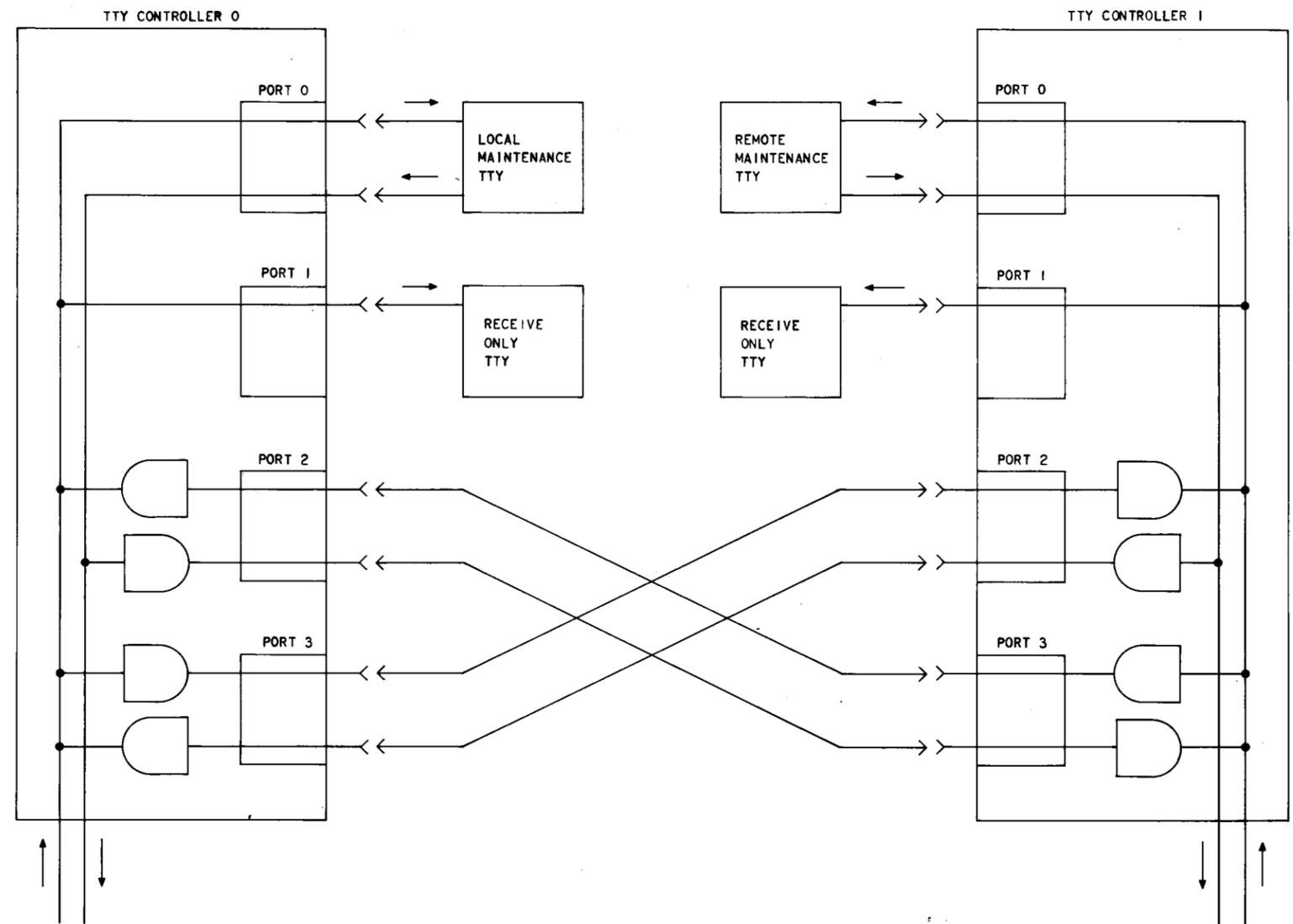


Fig. 26—TTY Controllers Arranged For Mate Operation

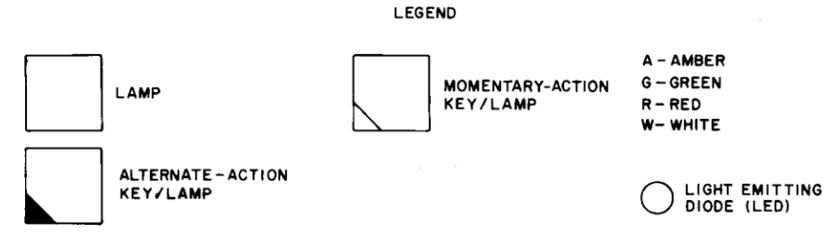
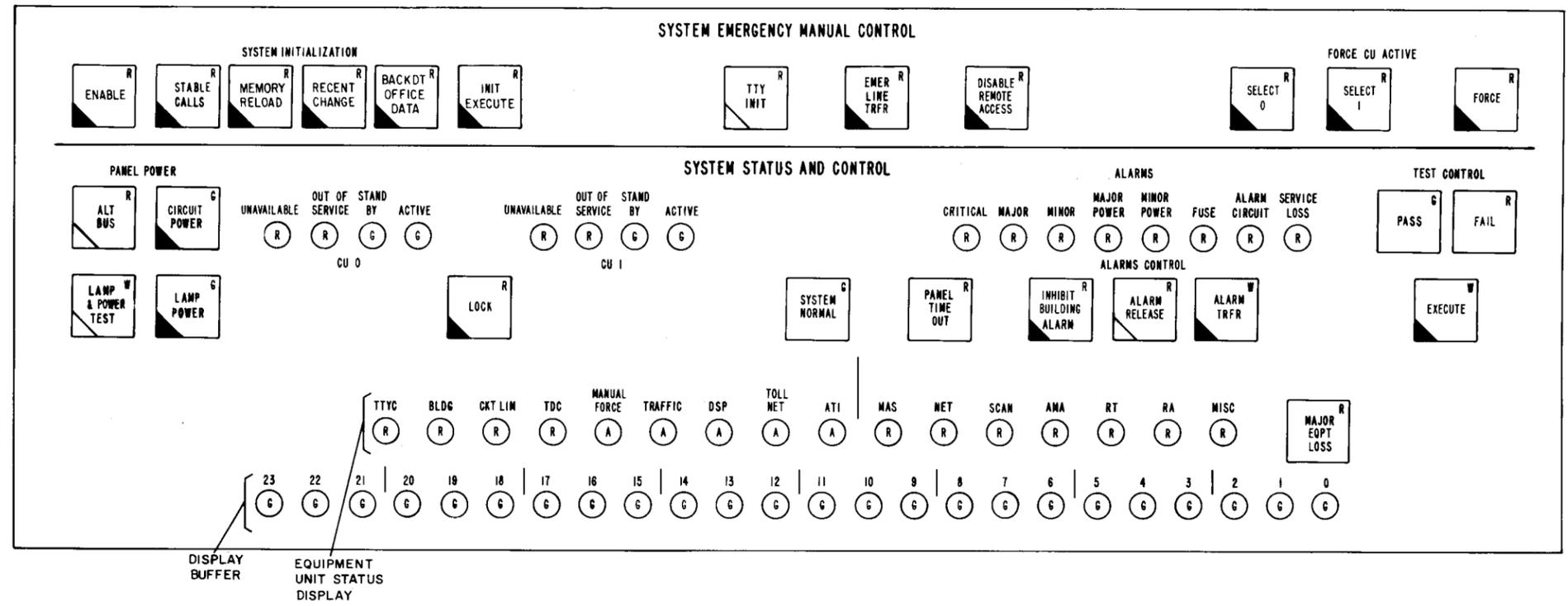


Fig. 27—System Status Panel Lamps, Keys and LEDs

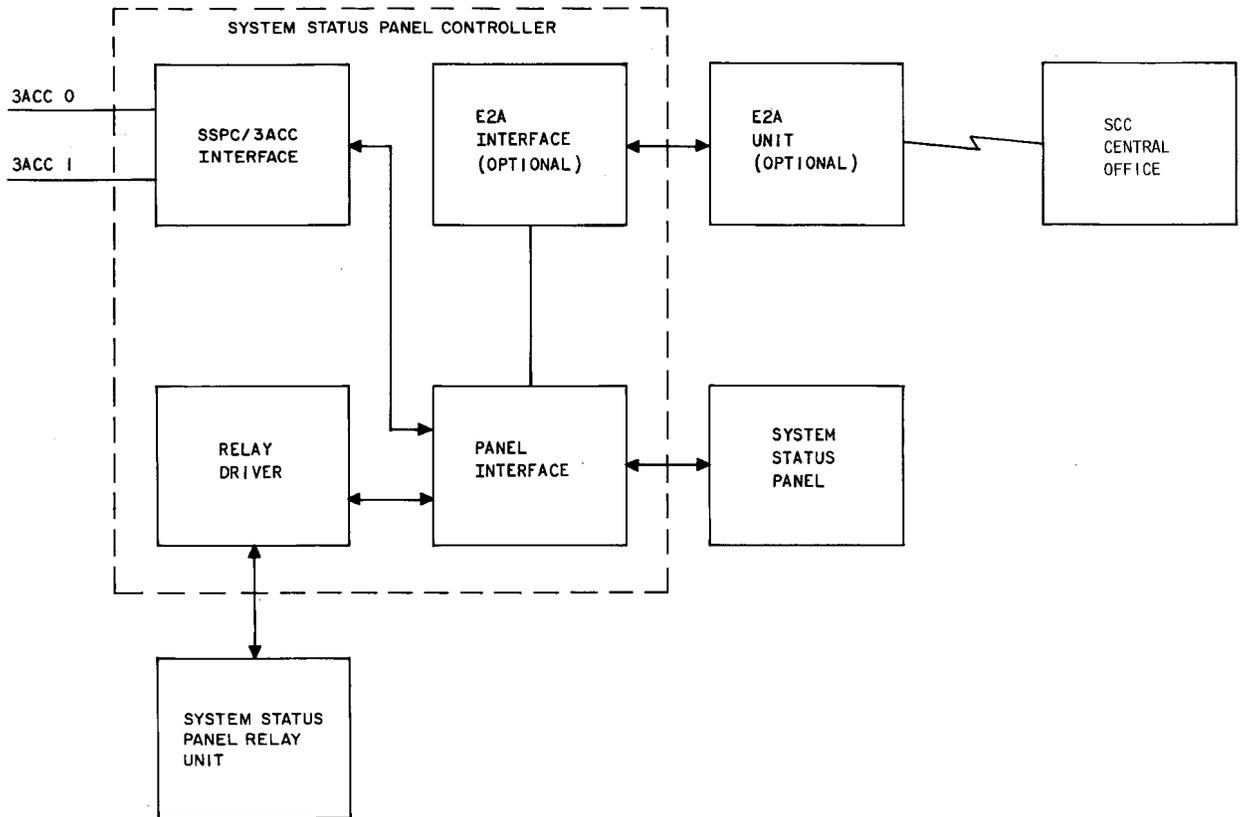


Fig. 28—Block Diagram of SSPC and Its Relationship to Other Units

F. Power Unit

3.107 The power unit contains the dc-to-dc converters necessary to convert -48 volts input to +3 volts at 4 amps. The +3 volts is required by the units located on the MTCE frame.

3.108 Power is supplied to the frame from a power distributing frame through a triple power feeder supplying +24 volts, -48 volts and ground. The power feeders are connected to cables which run through the hollow frame uprights to the base of the frame. The filters in the base of the frame filter the 24-volt supply while the 48-volt supply is filtered by the converters. The fuse panel provides fusing and power to all units in the frame and the fuse alarm circuitry which operates when a fuse fails.

G. E2A Unit

3.109 The optional E2A unit is part of a remote maintenance system that provides the following:

- Surveillance from a remote location
- Ability to remotely recover a system in trouble
- Means to assist local office personnel in diagnosis.

SUPPLEMENTARY MAIN STORE FRAME

3.110 The supplementary main store (SMAS) frame is a single bay frame and is two feet and two inches wide. The SMAS frame may contain up to two main stores for a maximum of

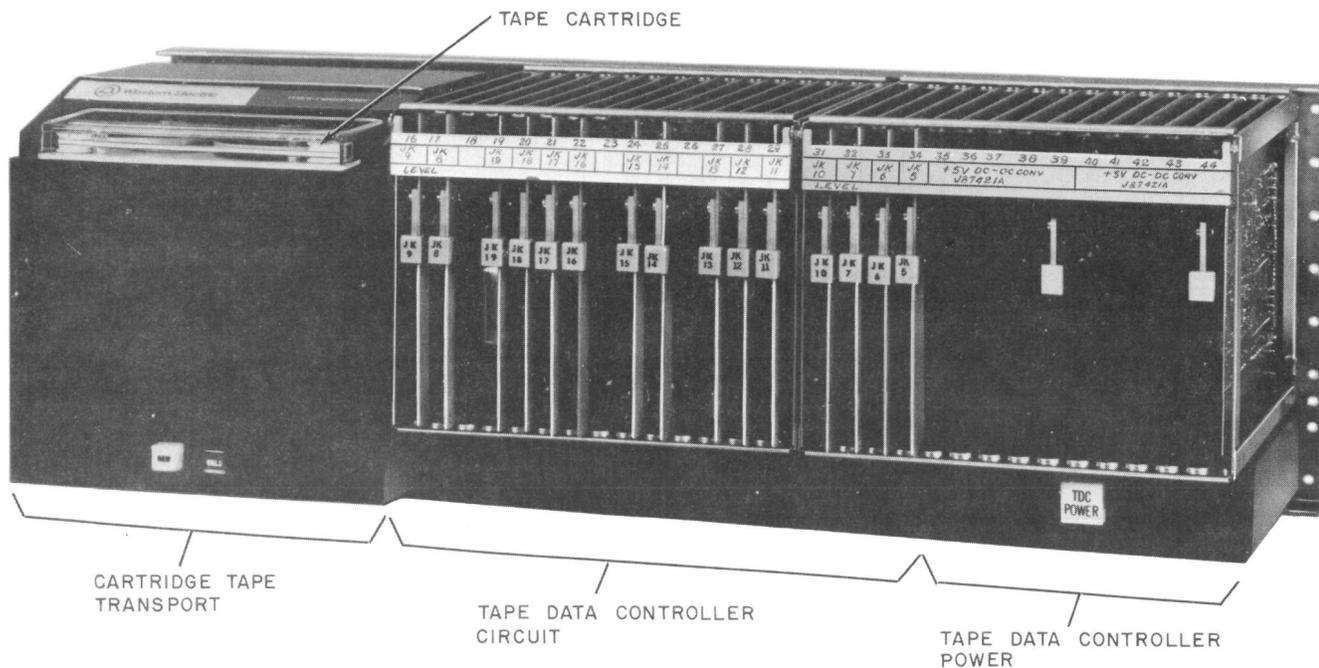


Fig. 29—Tape Data Controller Unit

512K word of additional memory. Refer to Section 254-300-150 for a detailed description of the SMAS.

3.111 If an office requires more than 256K words of memory, the two SMAS frames will be equipped with stores. Each SMAS frame is dedicated to a control unit.

4. MAINTENANCE

MAINTENANCE FEATURES

4.01 The following maintenance features have been applied to the design of the 2B processor:

- Use of long-life components and adequate circuit margins.
- Major units are duplicated to ensure continuous operation and prevent service loss in the event of error or equipment failure. When a trouble condition is detected, the faulty unit is removed from service and the standby unit is placed in service.
- The No. 2B ESS provides extensive program and hardware facilities to detect processor

malfunctions. The maintenance personnel are notified by an alarm indication that a malfunction has occurred and are given the results of the diagnostic test if performed, by teletypewriter printout(s).

- Test and verification routines allow for requested repetitive testing of trouble items and automatic recheck on service restoration.
- Self-checking circuits of the 3A CC give immediate detection of faults. These circuits eliminate the need for synchronous operation and match comparison between control units, while still providing rapid detection of failures.
- Circuits are made rapidly repairable by the use of plug-in units.

4.02 Three functions are involved in the maintenance of the No. 2B ESS.

- (1) **Fault Detection:** Before a fault can be corrected, it must first be detected. Fault detection is accomplished by hardware and/or software.

(2) **Recovery:** After detection of a fault, rapid recovery of the system must occur to ensure the protection of calls in progress and the continuation of the call processing functions.

(3) **Diagnostic and Repair:** After recovery, the fault must be diagnosed and isolated to the unit in trouble for replacement purposes.

FAULT DETECTION

4.03 Fault detection is accomplished by hardware and/or software. The units of the 2B processor are designed to be self checking and utilize the following error checking techniques:

(a) **Bit-Slicing:** Two-bit partitioning or bit slicing is used in the 3A CC and the main store controller to aid in the detection of errors, especially in areas such as general registers. Two-bit slicing means that two bits of each register are on a single circuit board. For example, the first circuit pack contains bits 0 and 8 of every general register. Partitioning is used so that a fault will affect at most only two bits of any register and therefore be detected by the two parity bits.

(b) **Parity Check:** A parity bit is a bit associated with a word to make the total number of ones, including the parity bit, odd. Parity checks are used throughout the 2B processor. Each time information is transferred from one location to another via a data bus, a parity check is performed by a gating bus parity checker. Whenever incorrect parity is found, an error is detected.

(c) **M-Out-of-N Codes:** The m-out-of-n codes are used in various areas of the 3A CC to provide maximum error detection capability such as the control signals required in the I/O channels and microprogram control. The m-out-of-n codes means that "m" number of ones should be present "n" number of bits. For example, four-out-of-eight means that no more than or no less than four ones will always be present. The associated decoder check circuits ensure that the number of ones is correct. If an incorrect code is detected, an error is indicated.

(d) **Duplication:** Some circuits of the 3A CC are duplicated to detect faults such as the data manipulation circuitry. Duplicated circuits

of the 3A CC are given the same inputs and their outputs are then compared to ensure their correctness. Whenever the two outputs differ, an error is detected.

(e) **Periodic Detection Test:** Since the 2B processor uses self-checking circuits, its fault detection is adequate only as long as the check circuits work properly. A combination of hardware and software is used to ensure that the check circuits provide an indication when a fault occurs. Hardware provides a means of simulating test conditions or circuit faults. By appropriately setting up the test conditions and applying a well-designed test sequence, the detection circuitry is checked on a periodic basis to ensure its proper operation.

(f) **Program Timer:** Although the 3A CC is designed to be as self-checking as possible, an overall system sanity check for both hardware and software is provided by the program timer. The use of the hardware timer is closely related to the system program. A reset is generated for the timer only if the program proceeds through the normal program loop correctly within the prescribed period. If the program deviates from the normal course, no reset is given. The timer automatically times out, stops processing, and starts the recovery process.

RECOVERY

4.04 After the detection of a fault, the system must quickly and automatically recover itself to a point or condition where it can function to process calls. The error signals that result from the detected faults are buffered to the error register of the 3A CC. These signals are sorted and divided into three groups with each causing a different set of system actions.

4.05 Interrupts: A demand maintenance interrupt occurs when a fault or difficulty of high priority is indicated. The interrupt program breaks into the program which is being executed. The demand maintenance interrupt immediately initiates corrective action. After the appropriate recovery action is taken control is returned to the base level program which was interrupted. The

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demand maintenance interrupts are initiated by the following control unit errors:

- Attempted off-line store write in write protected area
- Off-line store parity error
- Off-line fast timeout on read or write function
- Error in I/O main channel selection or error in 3-out-of-6 code check circuit
- On-line 3A CC program timer error
- Switch message received by on-line 3A CC telling it to go on-line
- I/O subchannel selection error or I/O channel sequence error
- I/O bad parity.

4.06 Initialization: This action is taken when a trouble occurs which is serious enough to require clearing of memory and/or registers and the restart of the effected unit in a known location. The units of the 2B processor which can be initialized are the 3A CC, MAS controller, MAS, 2B I/O control circuit, and TTYC, SSPC, and TDC. The level of initialization will depend on prior initializations which occurred in a specified period of time. Initialization restarts are handled by the common system initialization (CINIT) program and the application initialization (INITA) program. The stimulus of an initialization is the failure of a check that indicates the integrity of the processor and/or its data base is questionable. An initialization consists of:

- Restoring the CU to a known good state
- Restoring the periphery to a known good state
- Aborting certain activities
- Zeroing or otherwise initializing temporary data
- Bootstrap—partial or complete.

Not all of the preceding are performed on every initialization. An initialization can be more or less drastic depending on which, and to what extent, the preceding routines are invoked. For example, a given initialization may zero none, some, or all of temporary store. In general, the system reaction becomes more drastic each time a previous recovery attempt fails. The escalation is encoded in the level number of the initialization, which is incremented on each failure. The higher the level number, the more drastic the recovery routine becomes.

4.07 When the main memory loses its memory due to a system outage or program bug, the bootstrap loader program is used to completely reload all memory or to partially reload only the mutilated memory from the tape data facility. The bootstrap sequence generally consists of the following steps:

- (1) Bootstrap loader program is loaded into MAS from tape unit.
- (2) Bootstrap loader loads MAS with selected group of system programs which will complete initialization of 3A CC and reload the MAS.
- (3) Load check sum file into MAS to aid in evaluation of MAS contents.
- (4) Hardware initialization performed by system initialization program which was loaded in (2).
- (5) Mutilated blocks (4096 words) of MAS are determined and reloaded from tape.

4.08 The CINIT program is divided into three parts as follows:

- Restoration of CU to a known good state
- Zeroing common system temporary data
- Bookkeeping tasks (formatting of TTY output messages, alarms, etc.).

After each of the three parts are performed an entry is made to the INITA program. The INITA program is also divided into three parts which correspond to the entry points from the CINIT

program. The three parts of the INITA program are as follows:

- Analysis of data and determination of level of initialization to be performed
- Initialization of periphery and temporary store at level determined in first entry
- Bookkeeping tasks are performed and finally the restart of normal processing.

4.09 Switch to Other Control Unit (CU): This action exchanges control from one CU to the other due to a fault in the on-line system.

4.10 Although the system is designed to automatically recover itself under trouble conditions, certain software and/or hardware faults may occur in which the system is unable to reconfigure into a working mode (e.g., continuously switching CUs). In these cases, manual recovery must be performed via hardware which allows maintenance personnel the capability of forcing the system into a fixed configuration and then locking it into that mode. The maintenance personnel have this capability through the system status panel at the MTCE.

DIAGNOSTIC AND REPAIR

4.11 A diagnostic is a test sequence that localizes a fault to an area for repair. The diagnostics operate on a "start small philosophy." This means that before the circuit under test is diagnosed, all circuitry used in that diagnostic will be tested. For example, before the on-line 3A CC runs any diagnostics on the off-line 3A CC, the maintenance channel must first be checked to ensure its proper operation. As the diagnostics continue, that portion of the 3A CC that has been checked increases until correct operation of the total 3A CC is verified. If a failure occurs in the diagnostics, a TTY message is printed which gives a trouble number. This trouble number, when looked up in the trouble locating manual, should indicate the cause of the trouble. Maintenance personnel must then take the appropriate repair actions, such as the replacement of a circuit pack.

5. GLOSSARY

5.01 The following terms and definitions are used in this description.

Asynchronous Operation Refers to the operation of the CUs which is not synchronous. This means that the CUs do not execute the same instruction in synchronism and match the results as an error check. However, the store of the off-line CU is kept up-to-date so the off-line CU can assume control if necessary due to trouble in the on-line CU.

Bit (Binary Digit) A binary unit of information. A bit is represented by one of two possible conditions, such as the characters 0 or 1, on or off, high potential or low potential, conducting or not conducting.

Buffer (a) An isolating circuit used between two other circuits. The isolation may be between high- and low-speed circuits or between high- and low-impedance circuits, (b) A section of call store used to store information until it can be used by the system, (c) That portion of a peripheral decoder which controls relays.

Bus A group of leads providing time-shared communication paths over which information is transmitted from any one of several sources to any of several destinations as governed by gates.

Circuit Pack A circuit used as a convenient means for assembling, on a single mounting, one or more components, such as capacitors, inductors, diodes, resistors, transistors, etc. The components are interconnected to perform one or more circuit functions, such as amplification, gating, timing, etc, required in a circuit.

Central Pulse Distributor (CPD) The CPD enables peripheral frames, such as scanners, and provides facilities for transmitting ac signals to peripheral decoders which controls trunks, service circuits, and circuit junctors.

Call Store (CS) The temporary memory used to store the information pertaining to calls in progress, translation data, maintenance and diagnostic states, traffic and plant registers, etc. Call store is a portion of the MAS.

Enable Pulse A pulse that permits a unit or a circuit to become operative.

Encode To code information into a form suitable for transmission from one unit to another.

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Error A malfunction, the symptoms of which *cannot* be reproduced under program control.

Fault A malfunction, the symptoms of which can be reproduced under program control.

Flip-Flop A device capable of assuming two stable states (set or reset), thereby storing a bit of information. It remains in either state until a signal changes to the other state.

Hopper An area in call store memory used to record a list of items for communication between programs.

IGFET Insulated gate field effect transistor used in MAS memory cell.

Indexing The process of adding the contents of a specified register to that part of an instruction of another register which specifies an address or some data to be operated on.

Initialization A program restart at a fixed location to provide an orderly return to a stable state in the data processing routines. A count of the number of restarts incurred during a given time is used to progressively clear areas until the system recovers its sanity.

Input/Output (I/O) The process of transmitting information from an external source to a system or from a system to an external source.

Instruction A word which directs the 3A CC to perform a particular function.

Interrupt A break in the normal flow of a system or routine such that the flow can be resumed from the point at a later time.

Light Emitting Diode LEDs are chemically grown gallium phosphide crystals that convert direct current into a visible light output without benefit of energy-consuming filaments.

Maintenance The process of keeping equipment in proper working condition.

Maintenance (MTCE) Frame Serves primarily as a system maintenance tool in an operating office.

Memory A unit into which information can be placed to be extracted at a later time; the ability to retain information for later use.

Memory Circuit A circuit which, having been put in some state by an input signal, will remain in that state after the removal of the input.

Memory Device Apparatus having the faculty of retaining one bit of information. A relay, flip-flop, or an insulated gate field (IGFET) effect transistor memory cell.

Off-Line A condition in which equipment is operating correctly but is not called on to perform its primary function.

On-hook The condition that indicates the idle state (loop open) of a station line or other circuit. When a telephone handset is resting on its switchhook, the loop is open and the line is in the on-hook condition.

On-Line A condition in which equipment is performing its primary function.

Parity Bit A bit attached to a word to make the total number of ones, including the parity bit, odd.

Parity Check A check on the validity of a binary word by determining whether the number of ones in the word is odd.

Program A logical sequence of instructions used to control system functions.

Program Store (PS) In No. 2B ESS that part of the MAS which is used to store the sequences of logical operations required for call processing.

Random Access The ability to gain access to any location of a memory unit in a time that is essentially independent of the location.

Read To extract the information stored in a memory device.

Read Only Memory Memory which can only be changed by the replacement of hardware (e.g., the 3A CC microstore circuit packs).

Real Time Actual time of occurrence of an event. A real-time control system is one in which information related to a physical process is converted

by the control equipment quickly enough so that the outputs obtained are useful in controlling that process.

Redundancy The use of additional equipment and facilities to make possible continuity of service in the presence of troubles.

Register A functionally associated set of word storage elements with or without its controls and access; a word repository.

Semiconductors Materials which are in between metals and insulators in their ability to conduct electricity. Also, devices such as diodes and transistors made from semiconductor material.

Serial Pertaining to time-sequential transmission or storage, such as transfer or store in a digit-by-digit time sequence.

Silicon Integrated Circuit An integrated circuit where all the elements such as transistors, diodes, resistors, and capacitors are successively fabricated in or on the silicon and interconnected.

Standby The state of a unit when it is not handling customer switching functions but is ready and able to do so. Units in the standby state may perform

checking operations or be matched against the active units.

Store A unit containing memory devices in which information is kept until the system is ready to use it. A repository for information comprising memory, access, and control.

Subroutine A sequence of programmed instructions to perform a particular function which is common to several programs.

Temporary Memory A read and write memory which contains information that can be changed by the internal circuitry of the system and is not write protected.

Time-Shared Circuit A common circuit whose services are used by a number of circuits during separate time intervals.

Translation Information Information contained in the main store pertaining to individual lines or trunks. It may be used, for example, to convert a directory number into an equipment location, to derive the class of service, etc.

Trouble A malfunction or other condition that causes a deviation from normal system operation.