2B PROCESSOR—FUNCTIONAL DESCRIPTION OF MAIN STORE NO. 2B ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 This section describes the main store used in the No. 2B Electronic Switching System (ESS), and the diagnostics used by the 2B Processor to test the main store.

1.02 This section is reissued to include the supplementary main store and update information pertaining to the memory element.

MEMORY TERMINOLOGY

1.03 The following definitions will be useful in understanding the contents of this section.

(a) ***main store***—The main store is a data storage system consisting of a controller and up to eight memory modules (256K maximum, where K=1024).

(b) ***main store controller***—The main store controller is the circuit used for timing, control, addressing, and data buffering needed in the store operation. ▶The main store controller also provides error detection.◀

(c) ***main store memory module***—A main store memory module is a group of memory planes and associated access and detection circuits constituting 32K 26-bit words.

(d) ***memory plane***—The memory plane is a group of memory cells and associated circuits mounted on a circuit pack.

(e) ***memory cell***—Memory cells are integrated circuits actually used for data storage.

(f) ***random access memory (RAM)***—RAM is an organization of memory cells allowing read or write operations on any memory word during any allowable memory cycle. The sequence of the word addresses in time can be completely random.

(g) ***double store read***—Double store read is the ability for the 3A CC to initiate a new store read operation at the same address in the other store if a parity error is detected when a word is read out of its own store. If the parity is good when read out of the other store, the 3A CC will use the data read out of the other store and continue to process instructions from its own without any immediate corrective action.

(h) ***complement correction***—Complement correction allows the use of a location that has a single stuck bit in it that causes bad parity when read. The bits of the word are complemented and then written back at the failed location. The data is therefore stored in a correct but complemented form. When the data is read two parity errors are detected and all bits out of the location are recomplemented to obtain the correct data. This will be referred to as the ***automatic correction mode.***

(i) ***write protected memory***—Write protected memory is a block(s) of memory that cannot be rewritten as long as it is protected. Each block constitutes 4K of memory. The block is protected by setting its dedicated bit in a write-protect register. All the information in that block is protected until the ▶dedicated bit is reset via a rewrite of that write-protect register.◀

(j) ***volatile memory***—A volatile memory is a memory that will lose information when electrical power is removed.

(k) ***dynamic memory***—A dynamic memory is a memory with a data level decay characteristic such that it must be periodically refreshed to retain information. That type of memory normally dissipates less power than other types of semiconductor memory.

(l) ▶***random-access memory***—A random-access memory is one in which any single word-storage location may be accessed in any single operational cycle, and consecutive operational cycles need not access consecutive word-storage locations.◀

(m) ***nondestructive readout***—A nondestructive readout detection does not cause any alteration of memory information when accessed.

(n) ***access time***—The access time is the time required between the initiation of a store command and the availability of output data.

(o) ***cycle time:*** Cycle time is the minimum time interval between successive store commands.

(p) ***asynchronous store operation***—Asynchronous store operation means store timing is initiated by a processor command but the response from the store does not occur in a predefined time period.

(q) ▶***Supplementary main store frame (SMAS)***—Supplementary main store frame is a single-bay frame that contains up to an additional 512K words (where K = 1024 words).◀

BROAD OVERVIEW

1.04 The main store is the means of storage for the program instruction and data used by the 3A CC to direct and control system action. Each 3A CC, I/O control circuit, store bus, and associated main store(s) forms a control unit and is duplicated for system reliability (Fig. 1). Each control unit is a switchable entity and contains a minimum of one fully equipped main store as its memory.

1.05 A main store contains a main store controller and main store memory ranging in size from 32K to 256K words of storage (where K = 1024 words). The store is growable in increments of 32K word modules and is subdivided functionally into the program store and call store. The program store contains the generic program and translation data, and the call is temporary memory used by the 3A CC as a means of storage for transient data.

1.06 In normal operation, the active 3A CC keeps the standby main store up-to-date. The active 3A CC not only writes into its own store, but into the store of the other 3A CC as well. This is done to keep the standby control unit ready to take control from the active control unit in case of a switch and to keep the standby main store available for a double store read operation.

1.07 The main store is a dynamic, volatile, random-access, semiconductor type of storage. If total power failure occurs, a "bootstrap" operation

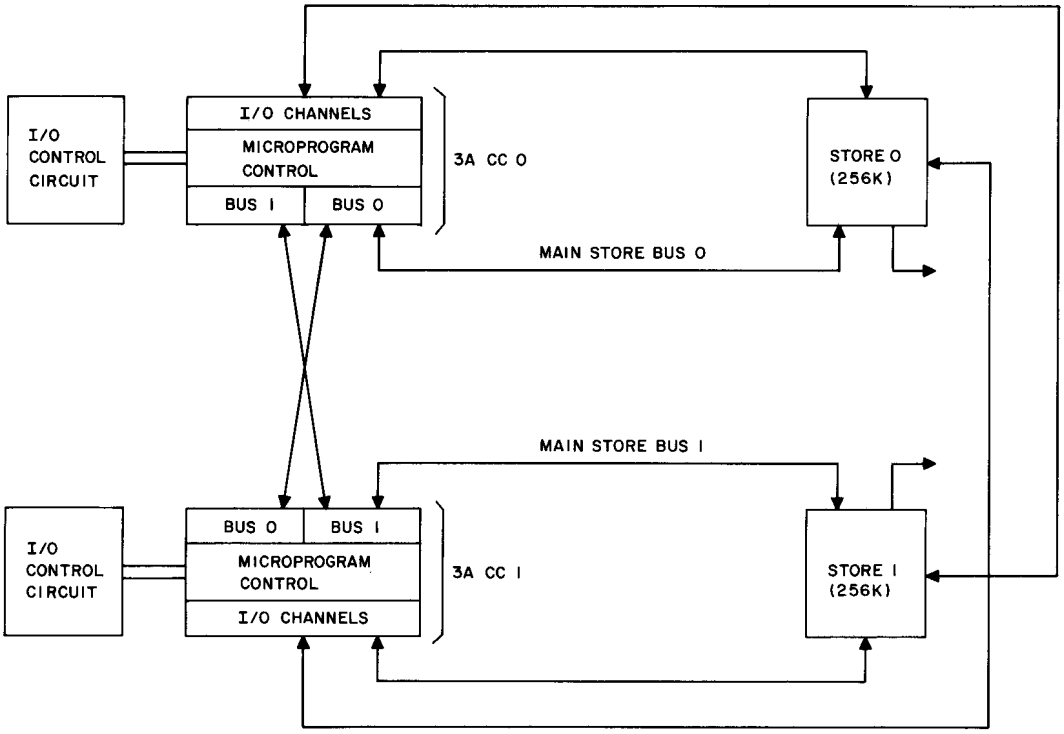


Fig. 1—2B ESS Processor Block Diagram

is performed which is the reloading or rewriting of the information into the memory from the backup tape system.

1.08 Program and data words stored in the main store are 26 bits in length. Each bit of information is stored as the presence or absence of electrical charge on the parasitic capacitance of an insulated gate field-effect transistor (IGFET) memory cell.

1.09 A matrix of these IGFET cells, 64 columns wide and 64 rows deep, is contained on one chip. One chip stores 4K bits of information.

1.10 Data is stored in the main store in a bit-sliced arrangement. Each 26-bit word has two bits stored on each memory plane. Since one chip contains 4K bits, eight chips can contain 32K bits. Two arrays of eight chips each are assembled onto one printed circuit board, along with necessary memory access circuitry, to form one memory plane. Each memory plane is then an array of 32K by two bits.

1.11 Thirteen memory planes, storing a total of 32K by 26 bits, are grouped together in one apparatus mounting, along with one fanout board, to form one main store memory module (Fig. 2).

INTERFACE OF MAIN STORE WITH 3A CC

1.12 The 3A CC will start a store operation by sending the store a "GO" command. Once the store recognizes the "GO" command, the store will initiate timing to execute the command. The maximum time in which the store has to return the information to the 3A CC is approximately 96 microseconds to prevent a time-out. The normal command execution time of the store will be a maximum of two memory cycles and this will only occur if the main store has started a refresh cycle prior to receiving a normal read or write order; otherwise the store commands will be executed in one memory cycle.

1.13 The two basic means of communications between the 3A CC and each main store are the main store bus and I/O subchannel. The main store bus is the primary means of communications

while the I/O subchannel is available for diagnostic purposes ▶and for program-controlled initialization.◀

▶INTERFACE BETWEEN MAIN STORES◀

1.14 ▶The supplementary main store frame is the means of storing additional data. Each 3A CC can have a supplementary main store frame which can house two additional main stores. Each main store has a bus repeater to relay the information on to the next main store via the main store bus.◀

2. EQUIPMENT DESCRIPTION

BASIC EQUIPMENT LAYOUT

2.01 A main store (Fig. 2) consists of up to eight main store memory modules and one main store controller. The controller is capable of driving all eight modules in the main store. Each module contains 32K of main memory.

2.02 The 256K of main memory is mounted under each of the two 3A CCs in the 2B processor frame. ▶Supplementary main store frames will allow the main store to grow to 768K words of memory (duplicated) if needed in the future. Each supplementary main store frame can be equipped with up to two additional main stores. The main stores in the supplementary main store frame are identical to the main store in the processor frame.◀

MAIN STORE

2.03 The main store controller and memory unit is the basic block of main store for one 3A CC. The main store memory unit can be used with only one memory module or with both memory modules equipped. More memory can be grown by adding as many as three more main store memory units.

MAIN STORE CONTROLLER

2.04 The main store controller serves as the interface between the 3A CC and the memory planes. ▶The main store controller is composed of 23 circuit packs and additional power equipment (Fig. 3). They include thirteen bit-sliced boards, one timing board, two check boards, two maintenance boards, one command board, one parity generator board, one bus control board, one power control board and one clock board. These packs are 4 by 7-3/4 inches in size with a 82-pin connector.◀

2.05 Basically, the contents of the bit sliced boards (FA-1060) in the controller are the following:

(a) two bits of the store address register (SAD),

(b) one bit of the refresh address counter (RAD),

(c) a read data strobe,

(d) two bits of the store data register (SD),

(e) two bits of the store error register (SER) in the store,

(f) eight bits of the write protect (WP) register which are used to define the WP area (each bit defines 4096 words),

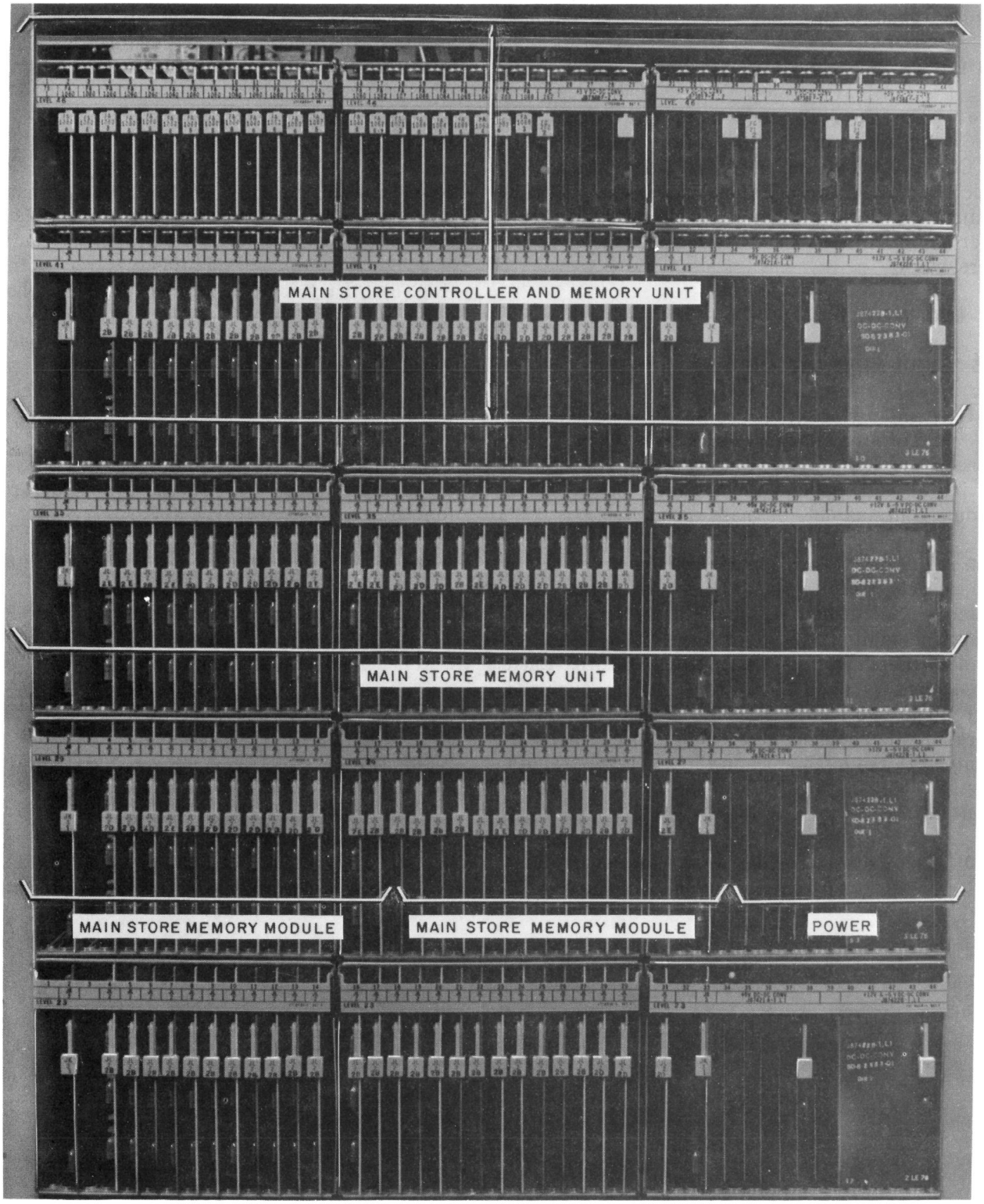


Fig. 2—Main Store

(g) isolate check circuitry, and

(h) diagnostic access circuitry.

Table A shows the bit assignment of the bit-sliced boards.

TABLE A

BIT ASSIGNMENT FOR THE BIT SLICED BOARDS

Bit	PH	PL	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Slice Board Or Board Name	CHKB	8	TB	CHKA	CK	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Store Address Register (SAD)

Bit	5	4	3	2	1	0
Bit Slice Board Or Board Name	3	2	1	0	7	6

Refresh Address Register (RAD)

Bit	PH	PL	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Slice Board	8	8	12	11	10	9	12	11	10	9	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Store Data Register (SD)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Slice Board	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

Store Error Register (SER)

Segment (8 bits)	P	7	6	5	4	3	2	1	0
Bit Slice Board	8	7	6	5	4	3	2	1	0

Write Protect Register (WP)

Legend:

CK — Clock Board
CHKA — Check A Board
TB — Timing Board
CHKB — Check B Board

2.06 The timing board ▶(FA-1071)◀ made up of the following functional components:

(a) one bit (bit 18) of the store address register and the store bus repeater associated with that bit,

(b) store select circuitry and the check circuitry for store select,

(c) a store select error flip-flop,

(d) a timing shift register that determines the main store controller's sequence of events,

(e) a bit 0-10 time active signal generator,

(f) a refresh request flip-flop,

(g) a mode flip-flop,

(h) an idle flip-flop,

(i) a shifter error flip-flop,

(j) refresh mode drivers,

(k) a chip select signal generator,

(l) a store busy flip-flop,

(m) a store complete flip-flop, and

(n) a store go receiver, and

(o) ▶store error C timing.◀

2.07 The check A board (FA-1062) contains the following functional components:

(a) one bit (bit 19) of the store address register and the store bus repeater associated with that bit,

(b) a duplicate 9-stage refresh request counter used to match the refresh counter on check B board,

(c) a duplicate store selection decoder for matching the decoder on the timing board,

(d) a write protect decoder for decoding the one-out-of-eight write protect segments,

(e) a checker for the two-out-of-four command decoder,

(f) a modified address parity high generator circuit which generates a modified parity high bit for the fanout board,

(g) a data parity low checker,

(h) an error bit to buffer results of the check circuit,

(i) the receiver and repeater gates associated with the store-maintenance-state bus lead, and

(j) check circuits discussed in 6.03.

2.08 The contents of maintenance A board (FA-1063) are the following:

(a) a 21-bit shift register,

(b) a 16-bit buffer register, and

(c) control circuits to load and dump these registers.

All are for use with the input/output (I/O) subchannel.

2.09 The contents of maintenance B board (FA-1064) are the following:

(a) circuitry to initialize the entire main store controller,

(b) four-out-of-eight maintenance order decoders and check circuitry,

(c) error register parity low generator, and

(d) error register parity high generator.

2.10 The command board (FA-1065) is made up of the following functional components:

(a) a buffer for the two-out-of-four command code and the associated repeaters for these store bus signals,

(b) read/write circuitry to memory modules,

(c) an error bit B flip-flop (write protect error),

(d) a memory module select decoder ▸for the write protect circuitry,◂

(e) a data parity high checker, and

(f) ▸check circuits discussed in 6.03.◂

2.11 The check B board (FA-1066) contains the following functional components:

(a) one bit (bit PH) of the store address register and the store bus repeater associated with that bit,

(b) modified address parity high driver to modules,

(c) two fanout board maintenance test signal drivers,

(d) A and B branch address parity error circuit receivers,

(e) a memory module refresh select check circuit,

(f) a memory module normal select check circuit, and

(g) a 9-stage refresh request counter used to determine when a refresh operation should be performed.

2.12 The parity generator board (FA-1067) will derive two parity bits from the data sent by the 3A CC. These bits will be stored in the memory module on a write operation from the store data parity bits (SDPL, SDPH) over the low sixteen data bits and the parity that is computed over the two halves of the high eight data bits (SD16-SD23). It also checks the extended parity high bit (SDEPH) against the actual parity of the high eight data bits. When information is read out of the memory, the parity generator also derives the three parity bits that are sent to the 3A CC. Circuitry is provided to allow an isolation test of the three bus parity leads.

2.13 The bus control board (FA-1068) contains the following functional components:

(a) generates store error C signal,

(b) ▸SGO repeater to higher order stores,◂

(c) bus repeaters and buffers for store automatic correction and store complement write, and

(d) bus repeaters for store busy, store complete, store error A and store error C.

2.14 The ▸power control board (FC-262) contains delay lines for store go, store complete, and store error C and power detection and control circuitry.◂

2.15 The clock board (FC-203) is comprised of the following functional components:

(a) power initialize circuitry,

(b) a 14.92537-mHz master clock that is an input to the timing board and the refresh request counters,

(c) one bit (bit 17) of the store address register and the store bus repeater associated with that bit,

(d) the store request bus repeater,

(e) I/O transmit control circuitry for both I/O subchannel, and

(f) discrete circuits containing the following functional components:

(1) I/O reset pulse generator,

(2) I/O buffer bit 0 clear circuit, and

(3) ▸a crystal oscillator described in (b) above.◂

MAIN STORE MEMORY UNIT

2.16 A main store memory unit (Fig. 2) consists of two memory modules (64K) and power converters to drive both modules. The power converters are located on the right of the odd numbered module.

2.17 The main store is composed of a maximum of eight modules. Each module contains thirteen memory planes and one fanout board (Fig. 4). All memory planes in the main store are 6 by 7-3/4 inches in size with a 42-pin connector. The fanout board is also 6 by 7-3/4 inches in size but has a 82-pin connector.

	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1060	FA1067		FA1060	FA1062	FA1071	FA1066	FA1064	FA1065	FA1063	FC203	FA1068	FC262	J87389F		J87389F	FC21	J87389F	FC21	J87389F
SPARE	BSB 0	BSB 1	BSB 2	BSB 3	BSB 4	BSB 5	BSB 6	BSB 7	BSB 9	BSB 10	BSB 11	BSB 12	PGB	SPACE	BSB 8	CHKA	TB	CHK B	MTCB	CMD	MTCA	CK	BUS CONTROL	POWER CONTROL	3 VOLT POWER CONVERTER	SPACE	3 VOLT POWER CONVERTER	3 VOLT REF AND FILTER CKT	3 VOLT POWER CONVERTER	3 VOLT REF AND FILTER CKT	3 VOLT POWER CONVERTER
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26 29	30	31 34	35	36 39	40	41 44

LEGEND:

BSB - BIT SLICE BOARD
PGB - PARITY GENERATOR BOARD
CHKA - CHECK A BOARD
TB - TIMING BOARD
CHKB - CHECK B BOARD
MTCB - MAINTENANCE B BOARD
CMD - COMMAND BOARD
MTCA - MAINTENANCE A BOARD
CK - CLOCK BOARD

Fig. 3—Breakdown of Main Store Controller Packs

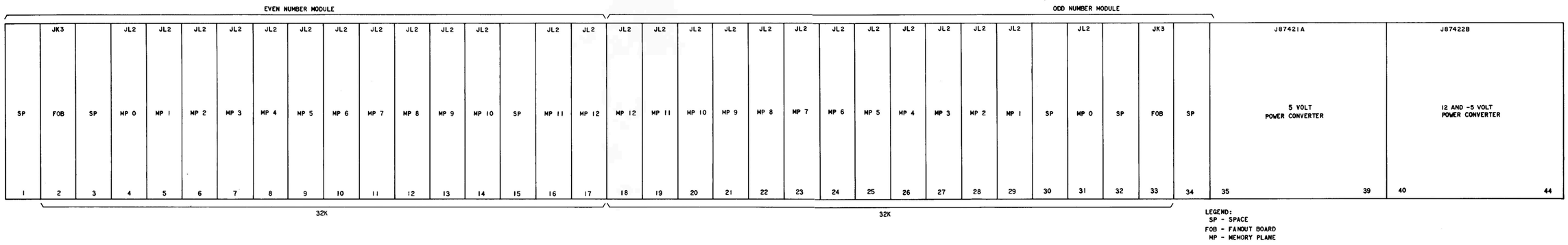


Fig. 4—Breakdown of Main Store Memory Unit Packs

2.18 The fanout board (Fig. 5) is made up of the following functional components:

(a) a decoder for determining if an address applies to one of the words stored in this module,

(b) circuitry to distribute address, refresh, and timing information from the main store controller to the memory planes,

(c) address parity check circuitry, and

(d) circuitry to return timing signals to the main store memory controller for error detection.

2.19 Basically, the contents of each memory plane (Fig. 6) are the following:

(a) sixteen dual-in-line packages (DIPs) containing 4K of memory each,

(b) read output circuitry for two data bits,

(c) Data input circuitry for two bits, and

(d) ▶Selection circuitry to select 2 of 16 memory chips.◀

Fig. 5—Fanout Board

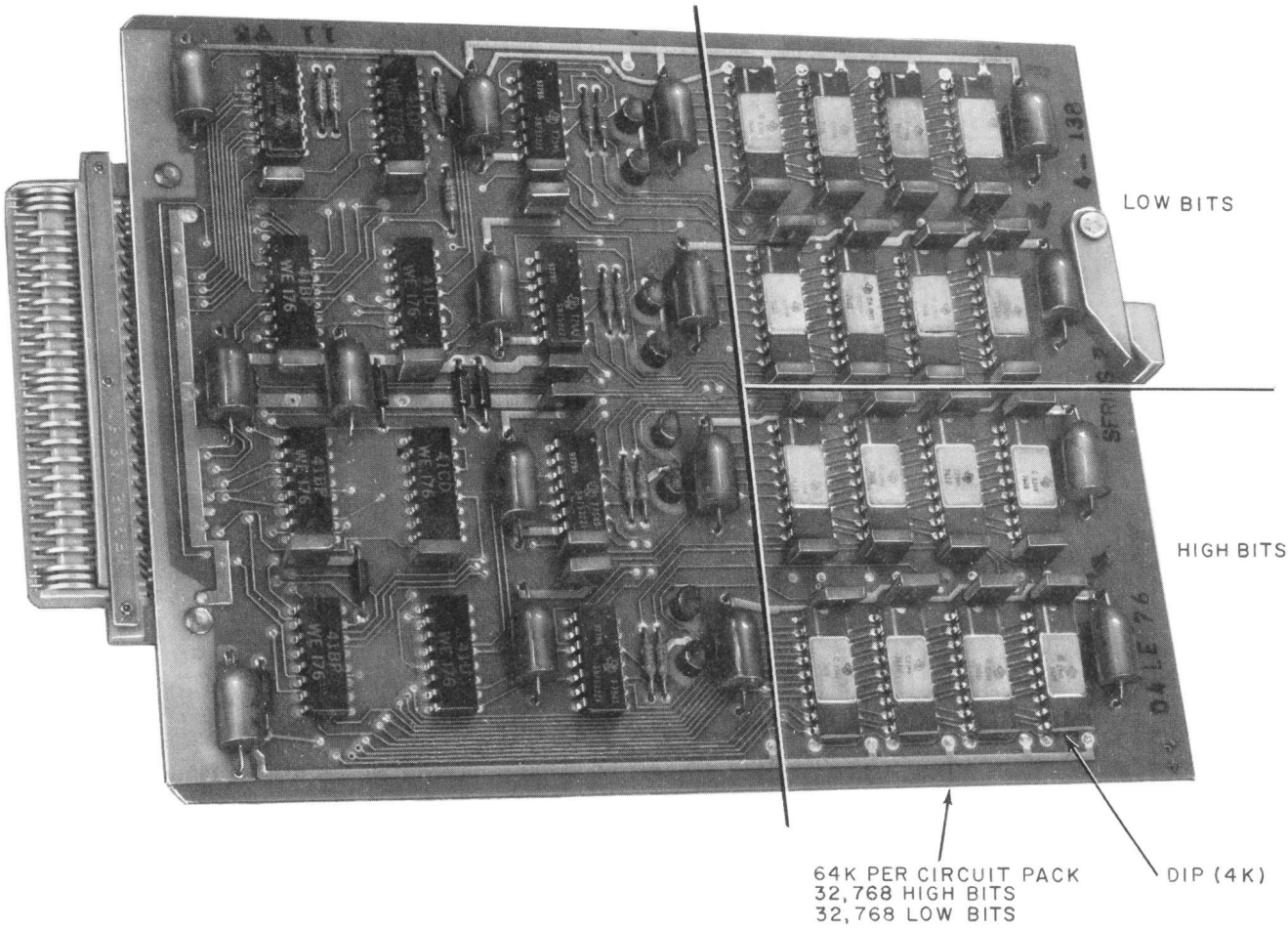


Fig. 6—Memory Plane

2.20 Thirteen memory planes are needed to form a 26-bit word of storage (24 bits of data and two parity bits). These planes are bit-sliced and the bit assignments of the DIPs on the memory planes are shown in Table B.

TABLE B

BIT ASSIGNMENTS OF THE DUAL-IN-LINE PACKAGES ON THE MEMORY PLANES

MEMORY PLANE NO.	ASSIGNMENT OF BITS OF DIPS
0	Bits 0 and 8 of the 32,768 words of storage
1	Bits 1 and 9 of the 32,768 words of storage
2	Bits 2 and 10 of the 32,768 words of storage
3	Bits 3 and 11 of the 32,768 words of storage
4	Bits 4 and 12 of the 32,768 words of storage
5	Bits 5 and 13 of the 32,768 words of storage
6	Bits 6 and 14 of the 32,768 words of storage
7	Bits 7 and 15 of the 32,768 words of storage
8	Bits 16 and 20 of the 32,768 words of storage
9	Bits 17 and 21 of the 32,768 words of storage
10	Bits 18 and 22 of the 32,768 words of storage
11	Bits 19 and 23 of the 32,768 words of storage
12	Bits PL and PH of the 32,768 words of storage

2.21 Two busses go down the store frame (from the store controller), one to drive the even numbered modules and one to drive the odd numbered modules. The fanout board drives all 13 memory planes in the memory module.

2.22 Resistive voltage dividers are used to terminate the far ends of the busses that interconnect the controller and the memory modules. They terminate the transmission lines and convert logic levels ▶from 3 volts to 5 volts going from the controller to the memory module and 5 volts to 3 volts going from the memory module to the controller.◀

2.23 The terminations are resistors mounted on paddle boards (Fig. 7) ▶at the bottom and the top of the main store.◀ Upon growth, another 6-inch memory unit is placed under the existing main store. The paddle boards at the bottom of the existing store are moved to the bottom of the new memory unit. The paddle boards at the top of the existing store remain in place and jumpers are used to connect the bottom of the existing store to the top of the new memory unit.

STORE BUS

2.24 A dc bus goes from each 3A CC to its associated main store (0) and also between the two 3A CCs. Each main store has a bus repeater to relay the information on to the next main store via the store bus. A duplex system includes two control units each having up to ▶three◀ main stores.

2.25 The 3A CC is designed to use a dc bus in an asynchronous mode. The address, ▶command, store request, store go, and complement correction portions of the bus are unidirectional while the data portion of the bus is bidirectional so the same data leads can be used for both read and write operations. The store complete and store error leads are unidirectional going from the main store to the 3A CC. The store busy is an unidirectional lead also. The store busy goes from higher order main store to lower order main store(s) but does not go to the 3A CC. Store busy blocks the loading of the timing shift register in lower order stores.◀

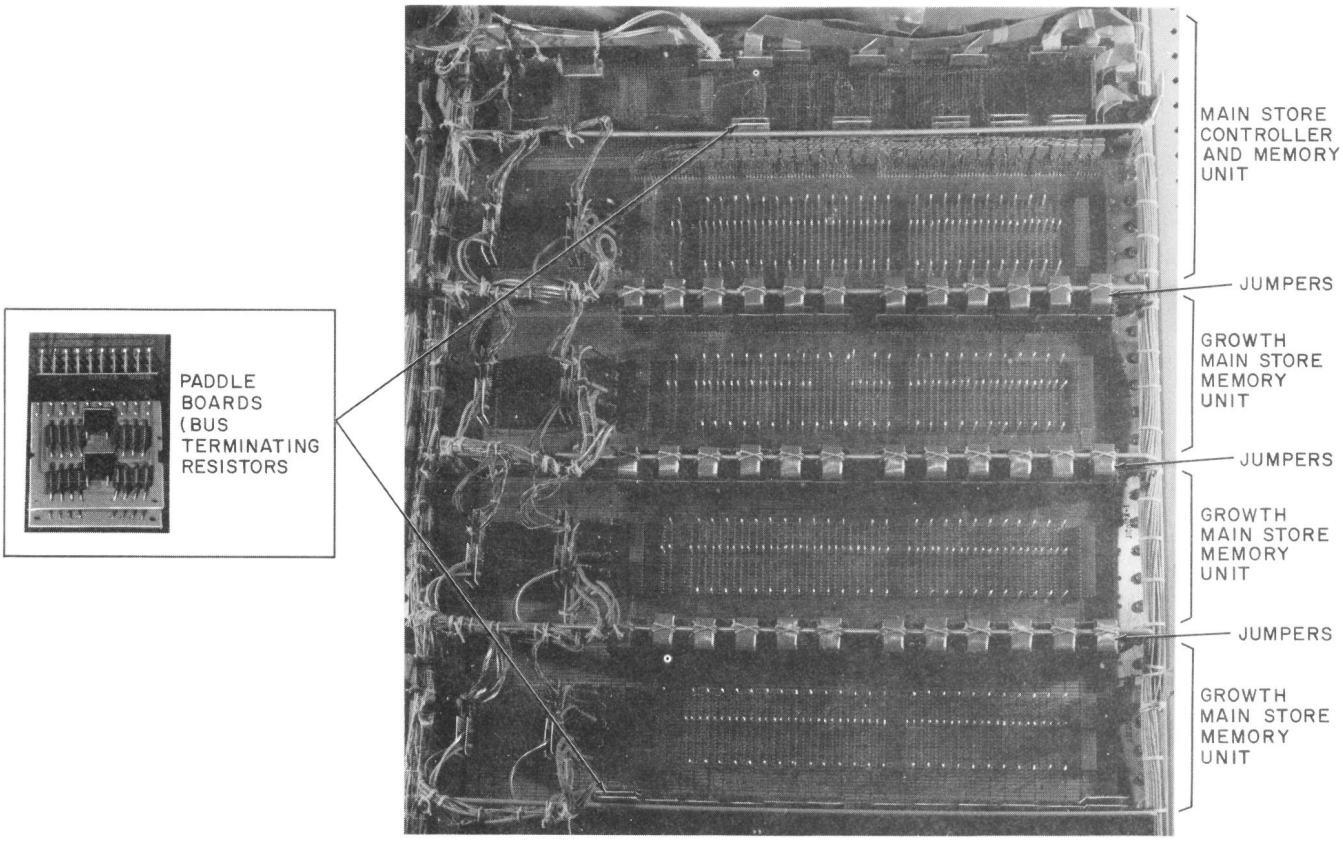


Fig. 7—Main Store—Rear View

2.26 The 63 leads (62 from 3A CC to main store 0) which make up the main store bus are shown in Fig. 8. The address and data leads are bit-sliced after they enter the controller to facilitate error detection. The commands sent to the memory are encoded in two-out-of-four code. A check circuit ensures that one and only one two-out-of-four code is selected. Table C gives the designation and functions of the leads between the 3A CC and main store.

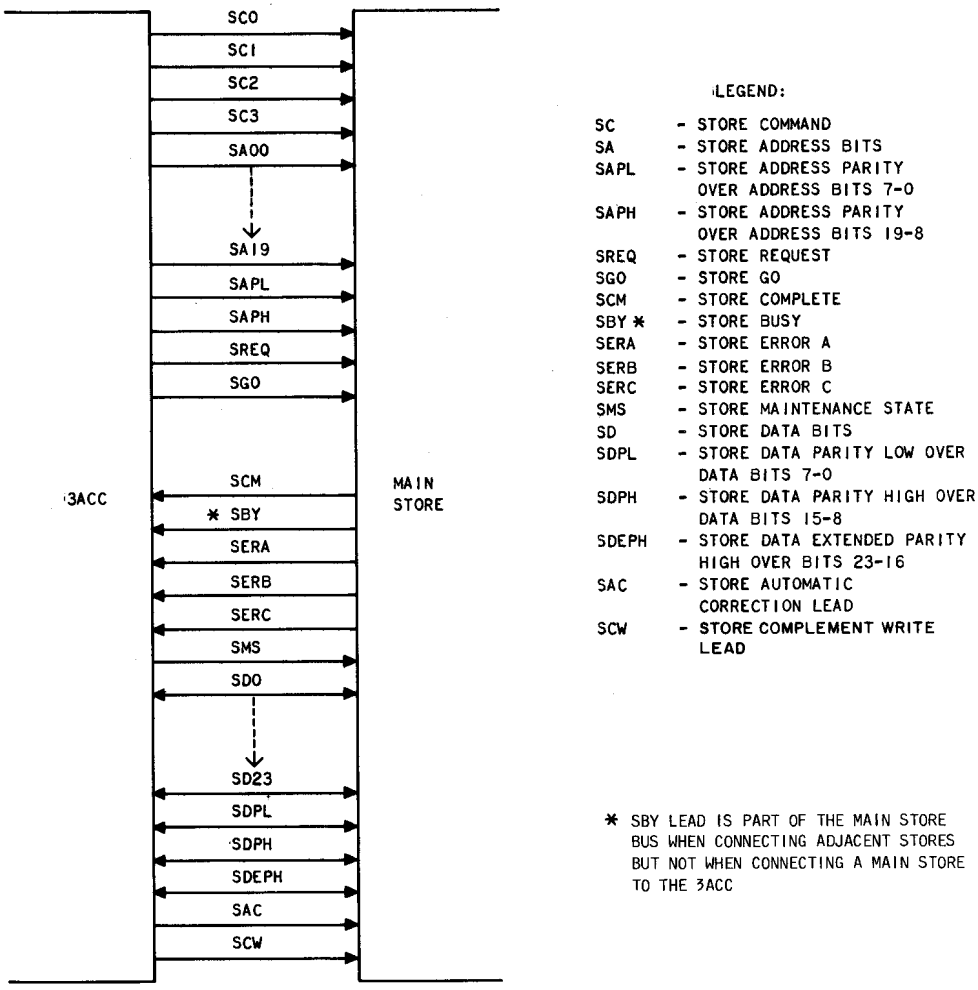


Fig. 8—Main Store Bus Leads

2.27 The interprocessor store bus allows the active 3A CC to communicate with the standby store. This makes it possible to keep the standby store up-to-date and to perform a double store read operation.

TABLE C

DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEADS	FUNCTION
SC3, SC2, SC1, SC0	Store Command Leads 0-3: These leads are used by the 3A CC to issue a 2-out-of-4 command code to the memory. The assignments of the codes are: 1100 = Read The contents of memory at the location defined on the store address bus are returned on the store data bus. 0011 = Write The 24-data bits on the store data bus and the two parity bits calculated by the FA 1067 board are written in the store at the location defined on the store address bus if not in write protect area. 1001 = Read Write Protect This operation returns the contents of one-fourth of the write protect (WP) register in the store controller to the 3A CC. 0110 = Write Write Protect This operation loads one fourth of the WP registers in the store controller. 0101 = Blind Write (not implemented). 1010 = Spare
SREQ	Store Request Lead: This signal is used by a lower priority 3A CC to inform a higher priority 3A CC that it wants sole use of the bus for a multiple cycle operation. This signal is necessary to prevent interwrite problems with multiple users on the bus. It is not necessary for a higher priority user to inform a low priority user of a multiple cycle operation, as the high priority user has the ability to prevent store access by a lower priority user.
SA0-SA19,SAPH,SAPL	Store Address Leads 0-19, Parity High, and Parity Low: SAPH — Parity on SA8 through SA19 SAPL — Parity on SA0 through SA7 SA18,SA19 — Defines which one of the possible three main stores is to be accessed. SA15-SA17 — Defines which one of the eight modules within the defined store is to be accessed.

♦TABLE C (Cont)♦

DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEADS	FUNCTION
SA0-SA19,SAPH,SAPL (cont)	SA3-SA14 — Defines row and column to be accessed. SA0-SA2 — Defines which chips on the memory planes within the defined modules are to be accessed.
SMS	Store Maintenance State: This signal is driven from the parity high bit on the maintenance state register in the 3A CC. It will enable the I/O communication path between the on-line 3A CC and off-line 3A CC only during maintenance functions.
SCW	Store Complement Write: When SCW is active, it will indicate to the main store controller that it should save the last word read out of memory, complement the data, and write it back into memory at the same address. (Complement write is described in 6.02.) The SCW signal to the store in conjunction with a read command causes an error signal to be sent to the 2-out-of-4 checker which provides immediate error detection of the SCW signal.
SAC	Store Automatic Correction: This signal in conjunction with a double parity error on a read causes the main store controller to complement the data and parity bits before it issues a store complete signal.
SGO	Store Go Lead: This is the signal that is put on the bus to tell the store that a store operation has been requested. It is removed after the 3A CC has received the store complete signal. In the case of a read operation, the address and command information is present on the bus. In the case of a write operation, the data, as well as the address and command information, is present on the bus.
SCM	Store Complete Lead: This signal is sent by the store to indicate the end of a store cycle. Error C can be sent back in place of store complete signal.
SBY	Store Busy Lead: This signal is sent by the store to indicate to other main stores that it has been selected. The lead is not returned to the 3A CC.

▶TABLE C (Cont)◀

DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEADS	FUNCTION
SERA	Store Error A Lead: This signal is sent by the store to indicate that a possibly fatal fault has occurred. This signal will cause a switch of control to the standby 3A CC. Some external items to the store controller which would generate a store error signal include address parity error, data parity error during write operation, invalid command code and addressing an unequipped memory module.
SERB	Store Error B Lead: This signal is sent by the store to indicate that a write protect error has been detected. An attempt to issue a write command in a section of memory that has been write protected will result in a store error B signal.
SERC	Store Error C Lead: This signal is sent by the store to indicate that a data parity error has been detected during a read operation. A double store read or complement correction operation will be initiated by the 3A CC.
SD00-SD23, SDPL, SDPH, SDEPH	Store Data Leads 0-23 and Store Data Parity Leads: These leads are used to provide the means of reading the data from or writing the data into the address on leads SA0 through SA19.

BUS SEQUENCING

2.28 The Store GO signal (SGO) is the start of a cycle. The command, address, and data information must follow on the bus within 40 nanoseconds after the start of the SGO transition. Once the store recognizes a SGO command, the store checks to see if it is performing a refresh cycle. If it is not performing a refresh cycle, a normal store operation will be initiated. A bit is then set in the store controller to indicate the bus is being used. ▶The store complete signal tells the processor that the data on the bus is valid. The end of a store cycle is signaled when the processor resets SGO after store complete has gone active. After SGO has gone inactive, store busy will be reset which in turn will cause store complete to go inactive. When the store complete signal goes inactive and all signals are inactive on the bus, the processor is free to use the bus again. Figure 9 shows the timing of the bus signals.◀

BUS REPEATERS

2.29 ▶Bus repeaters are used to relay information from one main store on to the next main store via the main store bus. As described in 2.25, part of the bus is unidirectional and part is bidirectional. Therefore, unidirectional and bidirectional bus repeaters must be used.◀

▶DELAY LINES◀

2.30 ▶As the information is daisy chained from one main store to the next, delay time between the SGO signal and the other signals should not increase. To prevent the delay time from increasing, the system is designed so the SGO signal will go through delay lines on the FC 262 before being sent to the next higher order store.◀

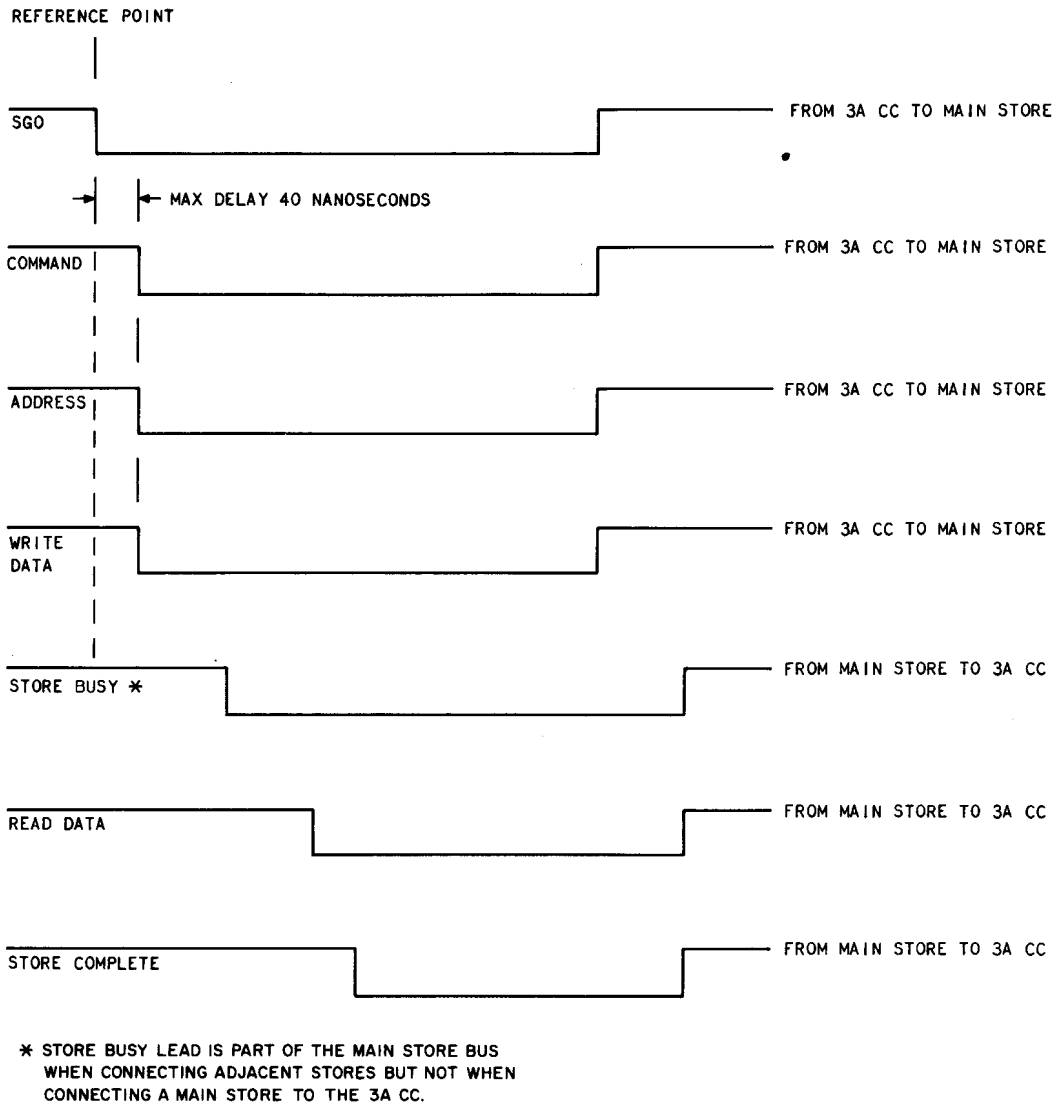


Fig. 9—Bus Sequencing

MAIN STORE POWER

2.31 The main store is equipped with its own power converters except for the power that is supplied to the terminations at the bottom of the main store. The power source for the converters is a frame mounted power unit. This unit supplies +24 volts and -48 volts to the converters of the main store. ◗The power is controlled by the POWER switch on the 3A CC control panel.◖

2.32 The following is a list of power converters and voltage inputs to the memory modules and main store controller:

Designation	Function
J87421A	Supplies 5 volts at 5.6 amps
J87422A	◗Supplies +12 volts at 2.0 amps and −5 volts at 0.5 amps◖

Designation	Function
J87389F	◗Supplies 3 volts at 5.0 amps◖
FC 262	Power control
FC 21	3-volt reference and filter circuit

MAIN STORE POWER ARRANGEMENT

2.33 The converters for each set of two memory modules (0 and 1, etc.) are located to the right of the odd numbered module (Fig. 4). Enough power is supplied by those converters to drive both memory modules.

2.34 The converters for the main store controller are located in the right side of the controller (Fig. 3). Approximately 20 amps of 3-volt power is supplied by the four converters.

3. MAIN MEMORY TECHNOLOGY

MEMORY CELL

3.01 The insulated-gate-field-effect transistor (IGFET) is used in the memory cell of the main memory. The IGFET is a field effect transistor whose gate is insulated from the semiconductor by a thin intervening layer of insulator. ▶Basically, the memory cell is made up of a IGFET and a parasitic capacitance. The function of the capacitance of each cell is to store a 0 or 1 in the memory cell.◀

3.02 The IGFET has three terminals, a source, drain, and gate. ▶Depending on the difference of potential between the gate and the source, the IGFET will be turned on or off making the connection between the source and drain a short or open. The IGFET is used as a switch being turned on or off by the potential present.◀

3.03 ▶When the cell is accessed, the IGFET becomes a short and allows the voltage in the cell to be the same as the voltage on the access line. On a write operation, this allows the cell to either be charged or not charged depending on the voltage on the access line. On a read operation, the access line will have the same voltage as the cell representing a 0 or 1.◀

MEMORY CHIP

3.04 ▶The main memory chip is mounted in a dual-in-line package (DIP). Each DIP contains one memory chip containing 4096 memory cells or bits of stored information. The matrix organization of the memory cells is shown in Fig. 10. The six address bits in Group A are decoded to indicate which of the 64 possible rows are to be accessed. The six address bits in Group B are decoded to indicate which of the 64 columns is to be accessed. Therefore, one memory cell of a chip may be accessed by designating one row and one column. The R/W lead establishes which operation (read or write) is to be performed on the memory cell accessed.◀

MEMORY PLANE

3.05 A memory plane (Fig. 6) consists of 16 memory DIPs arranged in two 2 by 4 matrixes. ▶Each memory DIP contains one memory chip or 4096 bits of information. A memory plane then contains 16 DIPs, each storing 4K of information for a total of 64K bits of storage arranged in a 2 X 32K format.◀

3.06 The memory plane contains 2 bits of 32K words. This follows the bit sliced concept used in the 3A CC. Bit slicing the data and address makes it easier to diagnose a problem and determine the faulty circuit pack.

MEMORY MODULE

3.07 A memory module (Fig. 2) contains 13 memory planes. Each 26-bit word has two bits stored on each memory plane. Two of these 26 bits are parity bits; one over the upper data bits on the 12 memory planes and one over the lower data bits on the 12 memory planes. Because each plane only contains 2 bits of information and parity is kept over both of those bits independently, a fault anywhere on a memory plane will be picked up on the parity check.

4. MAIN STORE OPERATIONS

4.01 Basically, three types of operations are performed in the main memory. These are:

(a) read operation,

(b) write operation, and

(c) refresh operation.

The read and write operations access a store word in a very similar manner. For this reason, the store word access is discussed before the read and write operations and is actually a part of both descriptions. Figure 11 is a functional diagram of the main store controller and may be of use in

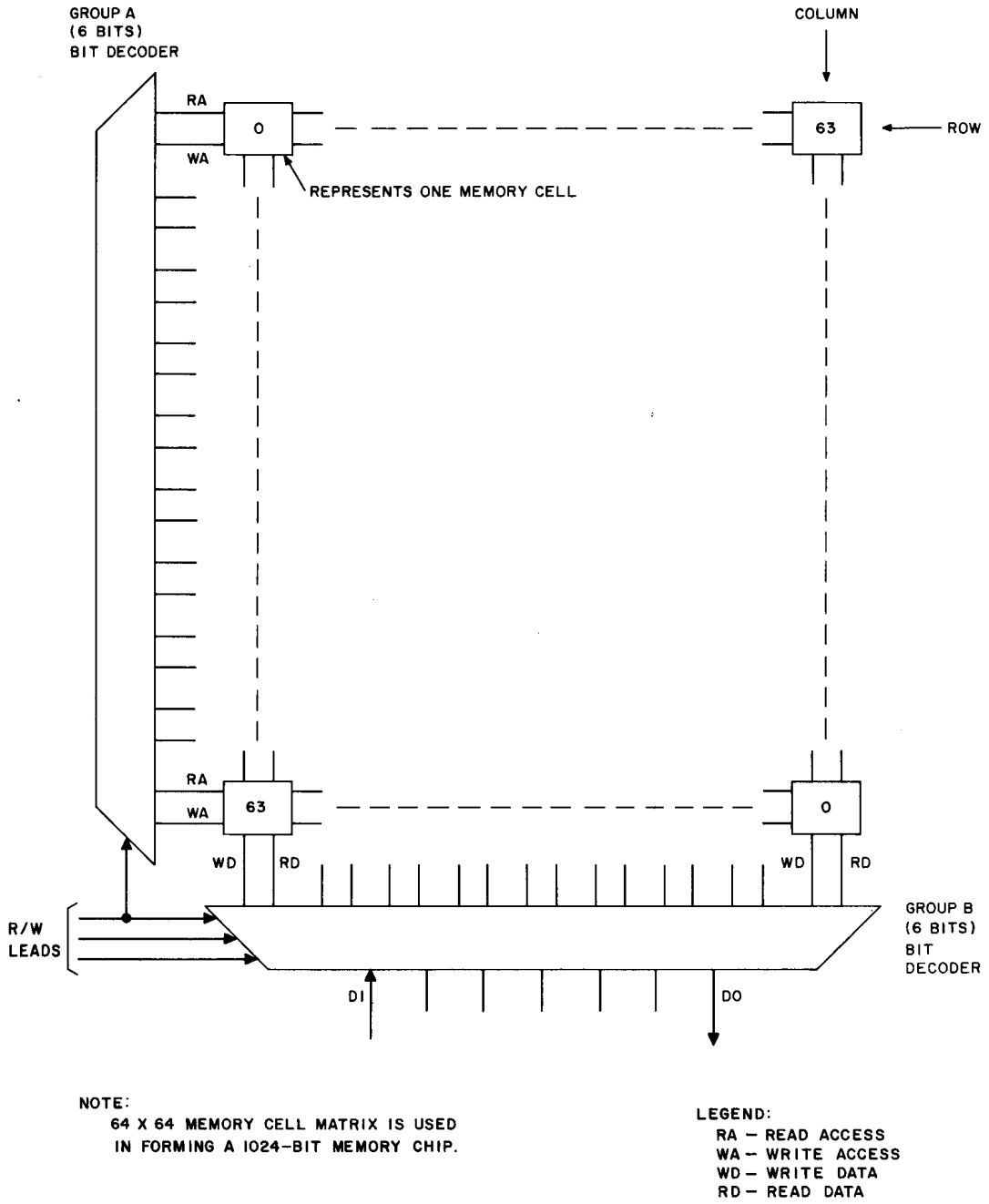
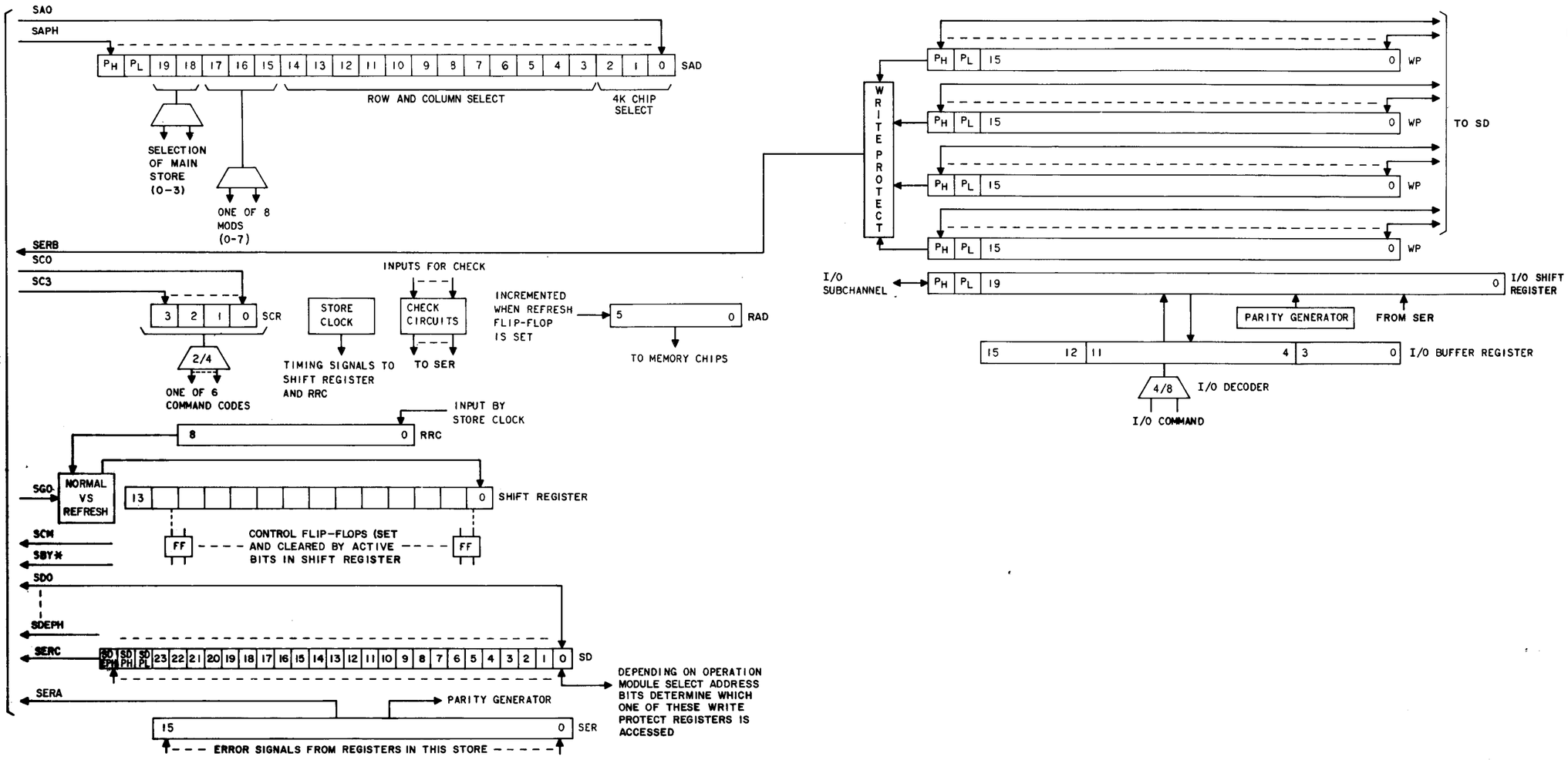


Fig. 10—Organization of Main Memory Chip

understanding the access and operational descriptions that follow.

STORE WORD ACCESS

4.02 The 3A CC transmits the address, command, and SGO signals onto the bus. The address is loaded into the store address register (SAD) and the command is loaded into the store command register (SCR). The SGO signal will start the timing chain provided the store is inactive (not doing a refresh cycle). The SGO signal will put an active bit into the shift register. The active bit shifting through the shift register is used to



LEGEND:
- SA - STORE ADDRESS
- SC - STORE COMMAND
- SAPL - STORE ADDRESS PARITY OVER BITS 7-0
- SAPH - STORE ADDRESS PARITY OVER BITS 19-8
- SREQ - STORE REQUEST
- SGO - STORE GO
- SCM - STORE COMPLETE
- SBY - STORE BUSY
- SERA - STORE ERROR A
- SERB - STORE ERROR B
- SERC - STORE ERROR C
- SD - STORE DATA
- SDPL - STORE DATA PARITY LOW OVER BITS 7-0
- SDPH - STORE DATA PARITY HIGH OVER BITS 15-8
- SDEPH - STORE DATA EXTENDED PARITY HIGH OVER BITS 23-16
- RAD - REFRESH ADDRESS COUNTER
- WP - WRITE PROTECT REGISTER
- SAD - STORE ADDRESS REGISTER
- SCR - STORE COMMAND REGISTER
- SER - STORE ERROR REGISTER
- SD - STORE DATA REGISTER
- RRC - REFRESH REQUEST COUNTER

*SBY LEAD IS PART OF THE MAIN STORE BUS WHEN CONNECTING ADJACENT STORES BUT NOT WHEN CONNECTING A MAIN STORE TO THE 3A CC.

Fig. 11—Functional Diagram of the Main Store Controller

set and clear control flip-flops. These flip-flops direct the actions and sequence of actions within the store.

4.03 Bits 18 and 19 of the address are decoded to determine which store the operation is to be performed in. The remaining address information (bits 0 through 17) and control signals are sent to the fanout board of all the main store modules. Within each main store module, the fanout board determines if the location being accessed is within its associated module by decoding address bits 15 through 17. If the location being accessed is within its associated module the fanout board sends the address (bits 0 to 14) and timing signals to all the memory planes in that module.

4.04 ▶The accessed memory planes decode the address information to determine the chip to be accessed on each plane, and the memory cell on each of the chips to be accessed.◀

4.05 The 4-bit command code is decoded by a two-out-of-four decoder in the controller that indicates the type of operation to be performed. The command codes are shown in Table C.

4.06 Even though the read and write operations access the store in the same manner as that discussed in 4.02 through 4.05 a few differences do occur in the write operation. These differences are as follows:

(a) The 3A CC not only transmits the address, command, and store go information onto the bus, but the data to be written into the addressed location as well.

(b) At the same time that the address and command are loaded into their associated register, the data is loaded into the store data register.

MEMORY CELL WRITE CYCLE

4.07 ▶The data that is loaded into the store date register must be stored in the appropriate memory cells. As discussed in 3.04, an appropriate cell within a chip is accessed by selecting one out of 64 possible rows and one out of 64 possible columns. One bit will be stored at the appropriate location on both the high bits and low bits sides of each of the 13 memory planes. When the cell is accessed the cell's IGFET becomes a short and the data is written into the cell. The IGFET then becomes an open and the data is contained in the cell.◀

MEMORY CELL READ CYCLE

4.08 ▶Reading a memory cell involves determining whether or not the capacitor is charged. The cell is accessed in the same manner as described in the previous paragraph. The data is read out of the cell and loaded into the store data register to be sent back to the 3A CC. The data will continue to be valid in the cell.◀

MEMORY CELL REFRESH CYCLE

4.09 Since the capacitor will eventually discharge to a point that stored information is lost, the memory cell must be refreshed on a periodic basis. The refresh cycle is basically a combination of both a read and a write cycle. During a refresh cycle, the chip automatically inserts the information read from a memory cell back into that memory cell.

4.10 The refresh operation is not initiated by the 3A CC. ***The store initiates its own refresh request.*** ▶The refresh request counter in the store controller initiates a refresh request approximately every 34.3 microseconds.◀ If the store is processing a normal cycle, the normal cycle is completed and the refresh operation is done immediately after the normal cycle is completed. If a refresh operation is in progress and a SGO comes from the 3A CC, the SGO is processed after the refresh operation is completed.

4.11 ▶The store controller has a six bit refresh address register that keeps track of which row is being refreshed.◀ After each refresh cycle, the register is incremented by one so that on the next refresh cycle, the next row is refreshed. ▶A total of 64 refresh cycles is required to refresh the whole store.◀

4.12 In a refresh operation, every single chip in the memory is enabled. Timing signals are transmitted to each of the memory planes to enable every chip. ▶The row of the chip is then selected by a one-out-of-sixty-four decoder on the memory chip. The address which points to the one-out-of-sixty-four row comes from the refresh address register in the controller (Fig. 11).◀

5. SYSTEM OPERATIONS

WRITE OPERATION

5.01 The command code that was decoded by the two-out-of-four decoder indicates that a normal write operation is to be performed. After the store is accessed, the normal write command causes the information in the store data register to be written into each defined memory cell via the data input (DI) leads (Fig. 10). The address is checked to ensure that it is not in a write protect area before the write operation is performed. The parity of the data in the store data register and the address in the store address register is checked. If the parity check indicates an error, a bit in the error register in the store is set. If a write protect error occurs, the write command is inhibited and store error B bit is set. The actual write cycle within each memory cell was discussed in 4.07.

5.02 ▶After the information is written into the memory cells, error bit A is checked to determine if an error occurred during any portion of the write operation. If an error did occur, store complete and store error A signal is sent back to the 3A CC. If an error did not occur, the store complete signal is sent back to the 3A CC via the main store bus.◀ When the 3A CC receives the store complete signal, the go, command, data, and address information can be removed from the bus. The removing of the store go signal causes the store to remove the store busy which in turn removes the store complete signal. The store is now available to process the next request.

READ OPERATION

5.03 The command code that was decoded by the two-out-of-four decoder indicates that a normal read operation is to be performed. After the store is accessed, the normal read command causes the stored information in each of the addressed memory cells to be read out via the data output (DO) leads (Fig. 10) to the store data register. The parity of the data in the store data register and address in the store address register is checked. If the address parity check indicates an error, a bit in the error register in the store is set. The handling of a data parity error is described in 5.04. The actual read cycle within each cell was discussed in 4.08.

5.04 After loading the store data register, the error bits are then checked to determine if any error occurred during any portion of the read operation. If an error other than a double parity error in the automatic correction mode occurred, either a store error A or store error C signal is sent back to the 3A CC. If the error was a data parity error other than the above exception, store error C is sent back to the 3A CC instead of the store complete signal and a double store read or complement correction operation is performed. The double parity error in the automatic correction mode is discussed in 6.02. Any other error causes store error A to be sent back. If a data parity error did not occur the contents of the store data register and a store complete signal are put on the main store bus. When the 3A CC receives the store complete signal, the data signals are loaded into their associated registers and the store go, command, and address information are removed from the bus. The removing of the store go signal resets store busy and removes the data signals. Then store busy resets store complete. If store error A was sent back to the 3A CC, only a command over the I/O subchannel will clear the error signal.

5.05 If the memory does not respond after approximately 96 microseconds, a time-out occurs and the system goes to a recovery program. The typical read access time of the system for the first main store is 1050 nanoseconds or seven microcycles. If a refresh is in process, however, the read access time of the system is approximately two microseconds.

5.06 ▶The store timing is derived by a 14-stage shift register that counts every 67 nanoseconds. The minimum cycle time for the store itself is 938 nanoseconds (14 stages times 67 nanoseconds).◀

5.07 The cycle time for the system is approximately 1200 nanoseconds. This is derived by adding the read access time in 5.05 (1050 nanoseconds) and one cycle (150 nanoseconds) for the system to digest the information.

5.08 On a read operation, the store address leads must propagate all the way to the memory plane in order to define which word is to be read. This is done via the address multiplexer and the fanout board. Once that address information is stable at the memory plane, it defines a memory location that is to be read.

5.09 The store complete lead is used to signal the processor that the readout information from the memory is on the store bus. The processor can use the information on the bus anytime after the store complete lead goes active. ⏵Once the processor recognizes the transmission, it removes the SGO, address, data, and command signals from the bus.⏴

WRITE PROTECT OPERATION

5.10 Some areas in the store need to be protected from accidentally being rewritten. Write protect is a feature that can prevent areas from being rewritten. This is done by placing write protect information in the register dedicated to that purpose in each store controller.

5.11 Each module (32K) is divided into eight 4K blocks that can be write protected. Any number of these blocks can be write protected. However, the minimum unit to be write protected is one block. So, if any part of the block has to be write protected, the whole block is write protected. ⏵If any part of the block has to be (re)written, the whole block cannot be write protected.⏴ Each block has a bit dedicated to it in the write protect register. Table D shows the bit assignments.

TABLE D

WRITE PROTECT REGISTER
BIT ASSIGNMENTS

BIT NO.	BLOCK
0	Mod 0 1st 4K
1	Mod 0 2nd 4K
2	Mod 0 3rd 4K
3	Mod 0 4th 4K
4	Mod 0 5th 4K
5	Mod 0 6th 4K
6	Mod 0 7th 4K
7	Mod 0 8th 4K
8	Mod 1 1st 4K
9	Mod 1 2nd 4K
10	Mod 1 3rd 4K
11	Mod 1 4th 4K
12	Mod 1 5th 4K
13	Mod 1 6th 4K
14	Mod 1 7th 4K
15	Mod 1 8th 4K
16	Mod 2 1st 4K
•	•
•	•
•	•
63	Mod 7 8th 4K
64	Parity Bit
•	•
•	•
•	•
71	Parity Bit

Note: Duplicated for each main store.

5.12 The bits are set in the register by certain data patterns on the data bits. The main store bus is used to load the write protect register.

5.13 A 72-bit write protect register is located in each main store controller (64 bits define the write protected blocks and 8 bits are parity bits. In reality the write protect register is comprised of four 18-bit registers, each having 16 data bits and two parity bits.) Under the write protect command, 18 bits of the write protect register are written at a time. The bits of the register are defined by using store address bits to point to the even memory module in the memory unit (two modules) containing the block(s) to be protected.

5.14 After the write protect register has been written, a verification can be done to make sure the right information was written in the write protect register. This is done by using a read write protect command. The command allows the 3A CC to interrogate 18 bits of the write protect register at a time (16 write protect bits and 2 parity bits).

5.15 When the 3A CC sends a normal write command, the store will check to see if the address is in a write protect region. If the address is write protected, the store will abort the write operation and signal the 3A CC via error bit B that it is trying to write in a write protect region.

6. MAINTENANCE FEATURES

PARITY AND ERROR

6.01 Only two parity bits are stored in the memory module. The controller, using the store data bits and the three parity bits received from the 3A CC, recomputes two parity bits and stores the two parity bits in the main store. When the information is read out of storage, three parity bits are generated by the controller using the data bits and two parity bits from storage. In the store, the low parity bit is over bits 0 through 7 and bits 16 through 19. The high parity bit is over bits 8 through 15 and bits 20 through 23.

6.02 Three store error bits can be sent back to the 3A CC. Store error bit B is sent back to the 3A CC when a write protect error as described in 5.15 has occurred. This error results in an interrupt of the 3A CC. Store error bit C is sent back to the 3A CC instead of a store complete signal when a parity error other than a double parity error in the automatic correction mode occurs on a read operation. This results in the action described in 1.03 (g) or (h). When complement correction takes place, a ***complement write*** is performed. In the complement write mode, write is performed. In the complement write mode, the loading of the data and address registers is blocked so the data in memory at the failing address can be complemented and the input to the command check circuit is jamed so write protected areas can be complemented corrected. When the data is read out, a double parity error will occur signaling the controller to complement the data and send it to the 3A CC. Store error bit A is sent back to the 3A CC when any error other than a write protect error or a read parity error has occurred. This type of error will cause a switch of control to the standby side. ⧫When more than one main store is used per control unit, store error bits A, B, and C are ORed from all main stores and sent back to the 3A CC.⧫

CHECK CIRCUITS

6.03 Check circuits are included on the main store controller circuit boards. Some check circuits are active only when certain diagnostics are being performed; however, many check circuits are utilized during normal system operation. The following is a list of check circuits contained on each circuit board.

- FA-1060—Bit Sliced Boards

  Each bit sliced board has an isolation check circuit. ⧫This check circuit makes sure the store bus data leads of the store being accessed are isolated from data bus signals from the next higher store.⧫ This check is performed under diagnostic control. Refer to Table A for bit sliced board location of bits.

- ⧫FA-1071—Timing Board⧫

  (a) The timing board has a check circuit that under normal system operation makes sure that only one active bit is loaded into the timing shift register described in 2.06 d.

  (b) The timing board has a check circuit that under normal system operation makes sure that the duplicated store select circuits agree.

• FA-1062—Check A Board

Note: The following checks are made during normal system operation.

(a) Check A board has a check circuit to ensure an illegal mode change from refresh to normal or normal to refresh is not attempted in the middle of a store operation.

(b) It has a check circuit to ensure that both refresh request counters are in synchronous operation.

(c) ⧫It has a check circuit to ensure store go (SGO) is still active while a normal store request is being performed.⧫

(d) It has a check circuit to ensure normal load has gone⧫ inactive at the proper time in a store cycle.

(e) It has a check circuit to ensure that the store is not in refresh mode without a refresh request.

(f) It has a check circuit to ensure that the command decoder has one and only one two-out-of-four code set at any one time.

(g) It has a parity checker for "low" data bits (SD0-7 and SD16-19).

(h) ⧫Checks 2-out-of-4 command codes.⧫

• FA-1063—Maintenance A Board

Maintenance A board has a check circuit that under normal system operation ensures that the incoming parity is correct on the received I/O message. The start code on the incoming I/O message is also checked.

• FA-1064—Maintenance B Board

Maintenance B board has check circuitry which ensures that under diagnostics one and only one four-out-of-eight maintenance order is active at the proper time.

• FA-1065—Command Board

(a) The command board has check circuitry to monitor store complete to ensure that it is not generated prematurely.

(b) The command board has a parity checker for high parity data bits (8-15 and 20-23).

(c) The command board has check circuitry to ensure select chip select (SELCS), select read/write (SELRW), and unselect chip select (UNSELCS) signals are echoed back from the appropriate fanout boards properly under normal operation.

• FA-1066—Check B Board

(a) Check B board monitors the response from the fanout board to ensure an address parity error has not occurred.

(b) Check B board monitors the response from the fanout board during the refresh cycle to ensure each module responds with a refresh select signal.

(c) Check B board monitors the response from the fanout board during normal operation to ensure that one and only one module responds with a normal select signal.

• FA-1067—Parity Generator Board

(a) The parity generator board has an isolation check circuit. This check circuit ensures that the parity bits on the store bus of the store being accessed are isolated from the next higher store.

(b) The parity generator board has a check circuit which ensures that the extended parity high bit sent from the 3A CC agrees with the parity generated over bits 16-23 during a write command.

• ⧫FA-1068—Bus Control Board

The bus control board has an isolation check circuit. This check circuit makes sure the store busy, store complete, and store error C store bus leads of the store being accessed are isolated from the same bus signals coming from the next higher store. This

check is performed under diagnostic control.

7. DIAGNOSTICS

I/O SUBCHANNEL

7.01 An I/O subchannel is used when diagnosing the main store. The I/O circuitry in the store controller can receive an I/O message from either 3A CC. However, the main store must receive a signal from its own 3A CC in order to allow the I/O channel from the other 3A CC to gain access to it. This is to prevent a malfunctioning out-of-service 3A CC from having access to a store.

7.02 An I/O message is shifted into the I/O shift register in serial form (Fig. 12). When the start code is detected in the end of the shift register, the message is parallel loaded into the I/O buffer. Either the contents of the error register or the I/O buffer can be transmitted to the 3A CC via the I/O shift register. By transmitting the I/O buffer contents to the 3A CC a loop-around test can be performed. This ensures that the message was sent correctly.

7.03 The eight bits in the center of the maintenance order are sent to the maintenance order decoder (Fig. 13). The eight bits make up a four-out-of-eight code and are decoded to make a one-out-of-thirty selection of maintenance orders.

7.04 The other eight bits shown in Fig. 13 are used as option bits. The option bits allow more than one maintenance state to be active at one time.

7.05 The contents of the Store Error Register (SER) can be sent to the 3A CC via the I/O shift register. The contents of the SER may be either the error(s) that caused the diagnostics to be called in or the results of running diagnostics within the store.

FUNCTIONAL TESTS

7.06 The store diagnostics uses the same start small philosophy that is used throughout 2B diagnostics. Before the circuit under test is diagnosed, all circuitry used in that diagnostic will be tested. This philosophy ensures that if a diagnostic fails, the trouble can be isolated to the circuit under test if the diagnostics are run in sequence.

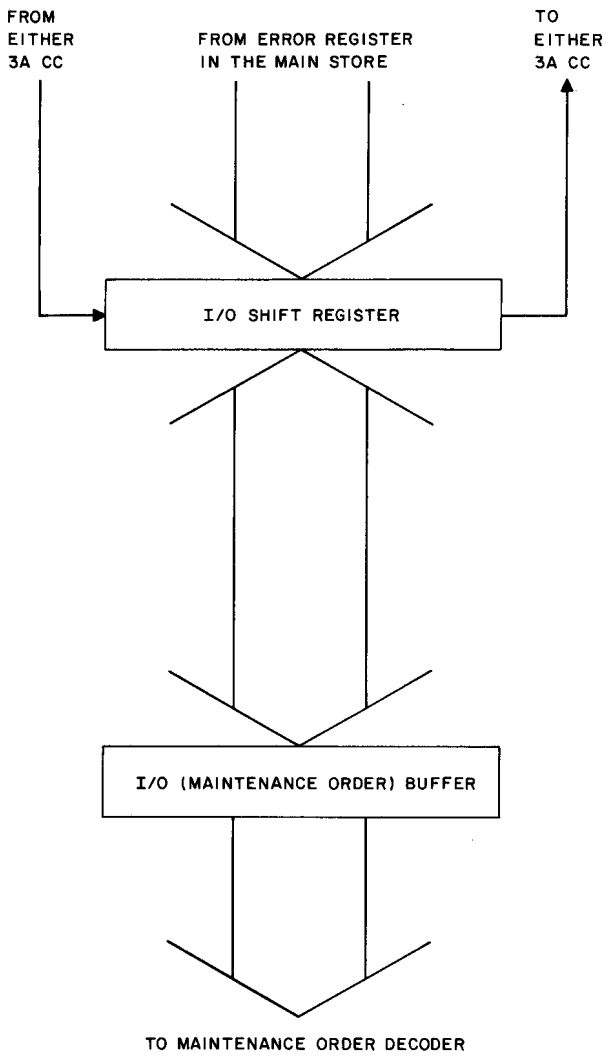


Fig. 12—I/O Diagnostic Access to Store Controller

7.07 The functional tests will follow in order according to test sequence. Test numbers can be obtained from TLM-1C900.

A. I/O Access to Store Controller

7.08 The first circuit to be diagnosed in main store diagnostics is the I/O access to the store controller. This is done because the I/O access is needed to test the rest of the main store.

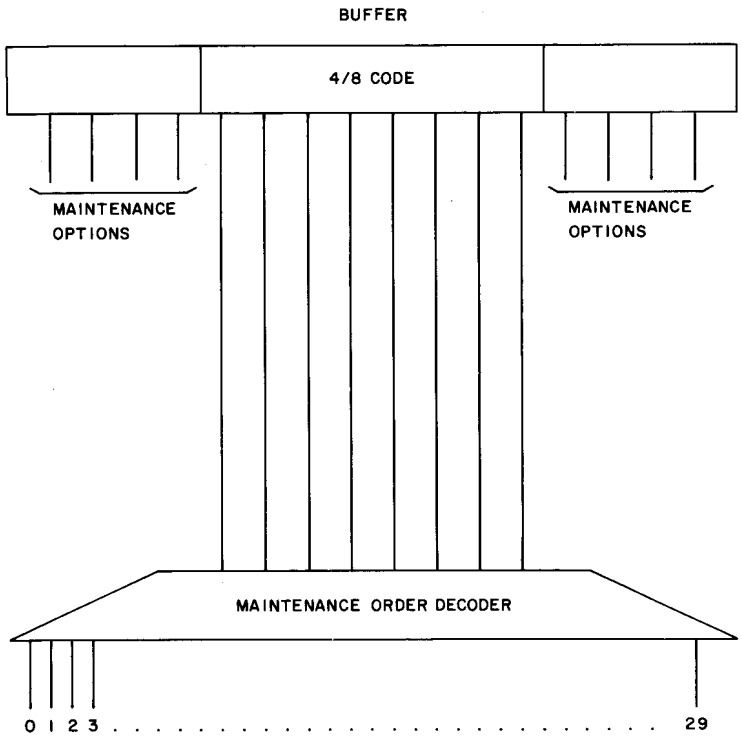


Fig. 13—Maintenance Order Format

The following functional tests are performed on the I/O access to the store controller:

- ▶Unlocks the dedicated access of the off-line processor to its own store. This enables the on-line machine to diagnose the off-line main store via the I/O subchannel.
- Checks that all of the four-out-of-eight maintenance orders can be sent to the store controller to ascertain that they can be transmitted and decoded properly.◀

B. Store Controller Multiplexer Circuitry

7.09 The store controller multiplexer circuitry is diagnosed next. This test checks the timing circuits, both normal and refresh, the refresh counter, the refresh address registers, and the check circuitry associated with these particular circuits. The following functional tests are performed on the store controller multiplexer circuitry:

- Checks the multiplexer circuitry in the store controller.
- Exercises the check circuitry of the multiplexer.

C. Off-line Bus Access to Store Controller

7.10 The off-line 3A CC bus access to the store controller is the next area to be diagnosed. These tests check to see if the off-line 3A CC can communicate with the off-line store controllers via the store bus. The following functional tests are performed on the store bus:

- ▶Checks the command portion of the store bus. Ensures 2-out-of-4 codes are sent with no error signals expected.
- Checks the address portion of the store bus. Addresses are transmitted over the main store bus and then retrieved for validation.
- Checks the data portion of the store bus. Data transmission loop-around test as well as error to ensure proper operation.

- Checks the control portion of the store bus. Control signals are sent and proper operation is ensured.

- Checks the data parity check circuitry. Data patterns are transferred to initiate the various control and parity functions in the main store.

D. Fanout Board Signals

7.11 Since the fanout boards are used to distribute the store address, they are checked next. The equipped fanout boards are checked for both normal and refresh selections. The circuits in the controller which check these signals under normal operation are also tested. The transmission of the store addresses through each fanout board equipped in the store under test is checked. The address parity check circuits on the fanout board are exercised. The memory timing signals are checked through the fanout boards and back to the controller. The following tests are performed on the fanout board signals:

- Checks both the refresh select circuits on the fanout boards and the check circuitry for the refresh select signals. All the memory modules are refreshed at the same time. The refresh select signals are used to indicate to the store controller that the memory modules have been refreshed properly. The check circuitry in the controller is diagnosed by verifying that none of the refresh signals from the equipped fanout boards are stuck active or inactive.

- Checks the normal select circuits on the fanout boards and the check circuitry for the normal selects. Each module is selected one at a time. The check circuitry verifies that one and only one of the modules respond. This is done by the check circuitry in the controller receiving a module select signal back from each selected module in turn. The exercise of the normal select check circuit is completed by applying error conditions and checking for the proper error output.

- Verifies that the address signals can be transmitted from the bit sliced boards in the store controller to the fanout boards in the memory modules.

- Tests the address parity checkers on the fanout boards of all the memory modules.

- Checks that the timing signals are passed from the store controller to the memory plane via the fanout boards. The timing signals are looped back from the fanout board to the controller. The controller then checks to verify that the right timing signals are transmitted. The timing signals are then prevented from being transmitted to the fanout board. This verifies that the check circuitry in the controller can recognize that the timing signals are not being transmitted properly.

E. Write Protect Circuitry

7.12 The write protect circuitry is then diagnosed. These tests check that the write protect register can be written and read. It also checks to ensure that a normal write operation will not be performed in a write protect region and that a normal write can be performed in an unprotected region. The following tests are performed on the write protect circuitry.

- The write-protect registers are initialized and verified. A check is then made to ensure that each bit of the four 16-bit write-protect registers can be written and read independently (only with maintenance store commands).

- Tests are then made to verify that a normal write command cannot write a write-protected area of memory but can write into an unprotected area.

F. On-line Bus Access to Store Controller

7.13 The on-line bus access to the store controller is next in the sequence. This diagnostic checks that access is possible from the active 3A CC through the standby 3A CC bus port to the off-line store controller. The following test is performed on the on-line store bus.

- Verifies that command, address, data, and control signals can be transmitted over the on-line bus. This information is transmitted from the on-line 3A CC through the off-line 3A CC bus port to the off-line store controller.

G. ▶Store Data Bits◀

7.14 ▶Outputs and inputs of the store data bits that were not tested during the off-line bus access to the store controller are now checked for integrity. Control and data bits are tested for stuck active as well as stuck low conditions.◀

H. Memory Module Integrity

7.15 Memory cell integrity is the last diagnostic to be run in the main store. Each equipped module is checked to ensure read and write operations can be performed. The following tests are performed on the memory modules.

- Verifies that data can be transmitted from the bit slice boards in the controller ▶through the store data flip-flop to the first memory module (mod 0), then, if equipped, the same path is verified through module 1.◀ There are separate paths for even and odd memory modules from the controller to the memory planes and from the memory planes back to the controller, so data is transmitted in both directions to verify the paths to and from the data buffer in the store controller.

- Checks the integrity of the memory cells in module 0 using the store access from the on-line 3A CC.

7.16 An off-line memory test routine is then loaded into memory module 0. This routine is used in the following test:

- Verifies the integrity of memory cells testing first memory module 1 and proceeding through memory module 7.

7.17 A check is made before each module is tested to ensure the module is equipped. A store limit word is used to perform this check. If this word indicates the module is not equipped, the rest of this test is aborted.

Note: Each separate store diagnostic test is run on each equipped main store in the system before the next sequential test is initiated.