FUNCTIONAL DESCRIPTION OF TAPE DATA FACILITY NO. 2B ELECTRONIC SWITCHING SYSTEM

CONTENTS PAGE

1. GENERAL

1.01 This section provides a physical and functional description of the Tape Data Contoller (TDC) unit and Tape Cartridge (TC) used in the No. 2B Electronic Switching System (ESS). Refer to Fig. 1.

1.02 When this section is reissued, the reason for reissue will be provided in this paragraph.

1.03 The TDC unit and tape cartridge provide a memory backup facility for the 2B processor. If the volatile semiconductor main store (MAS) becomes mutilated, it will automatically be reloaded from information stored on the tape cartridge.

1.04 The TDC unit provides the read/write circuitry, control circuitry, and drive mechanism for the tape cartridge. The tape cartridge is a magnetic tape storage device for duplicate MAS information and information required to reload the MAS.

1.05 If the MAS information is destroyed, the processor microprogram control circuitry is alerted by hardware error detection circuits and/or a free running software resettable timer reaching a time-out count. The microprogram control sends orders to the TDC unit that starts the reloading of the affected MAS from information stored on the magnetic tape.

1.06 The TDC unit also provides an optional data set terminal for a remote administrative location.

1.07 There are two TDC units located in a No. 2B ESS office. The TDC units are designated 0 and 1 and are assigned to the 3A Central Contol designated 3A CC 0 and 3A CC 1, respectively. The control interface between the 3A CC and TDC units allows either 3A CC to interface with either TDC unit or both TCD units (Fig. 2).

2. PHYSICAL DESCRIPTION

2.01 Each TDC unit is installed on an 8 by 12 by 23 inch mounting plates (Fig. 3). These plates are located on the maintenance (MTCE) frame as shown in Fig. 4.

2.02 A TDC unit (Fig. 1) consists of a Tape Data Controller Circuit, Tape Data Controller Power supply, and a Cartridge Tape Transport (CTT). A tape cartridge is used with the TDC unit as the data storage device.

A. Tape Data Controller Circuit (Fig. 1)

2.03 The TDC Circuit consists of 13 JK-type circuit packs housed in two 87B apparatus mountings. (Two additional circuit packs are required for the optional data set function.) The circuit packs and

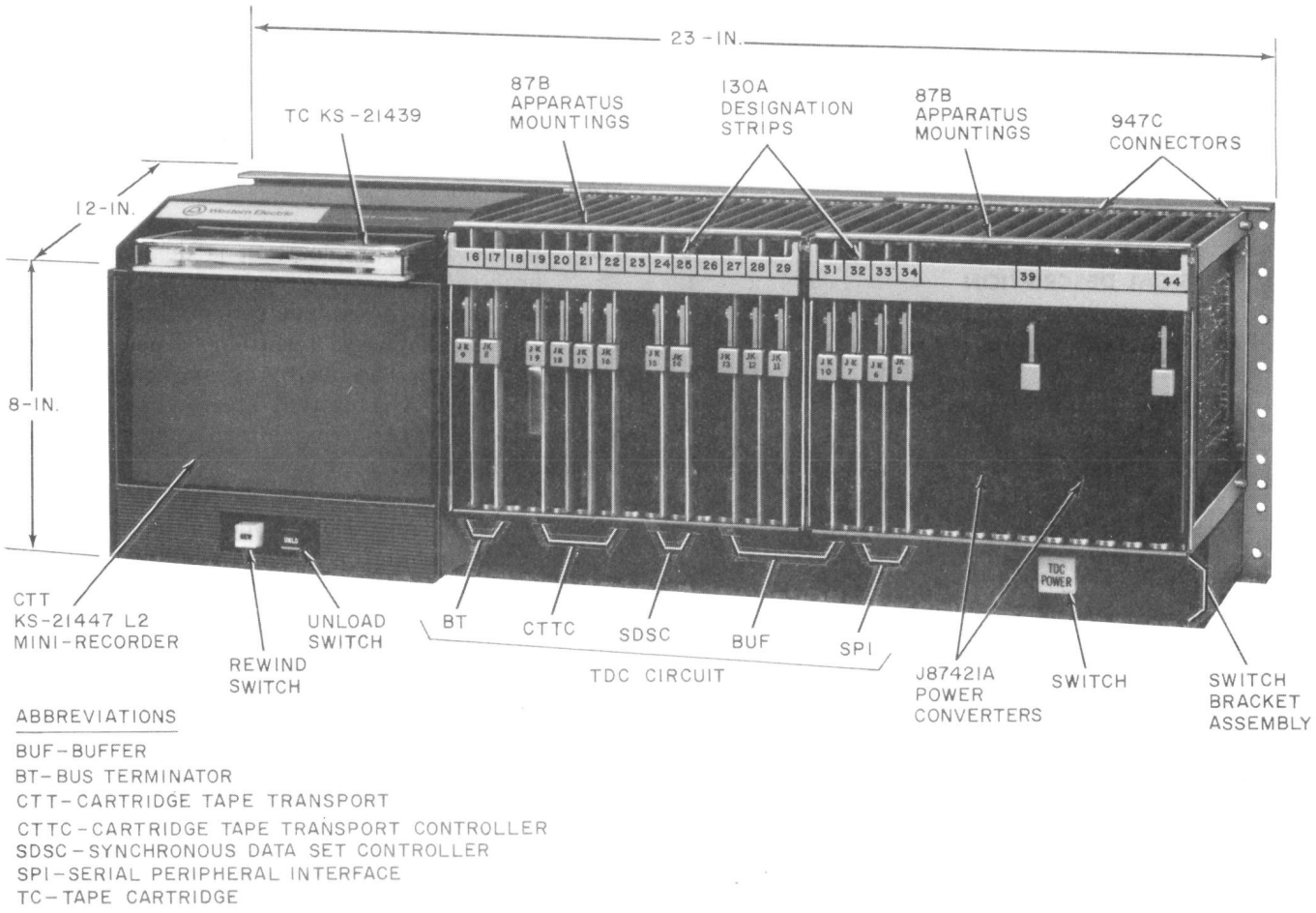


Fig. 1—Tape Data Controller Unit "0" or "1" J1C053A Front View

location are identified by two 130A designation strips.

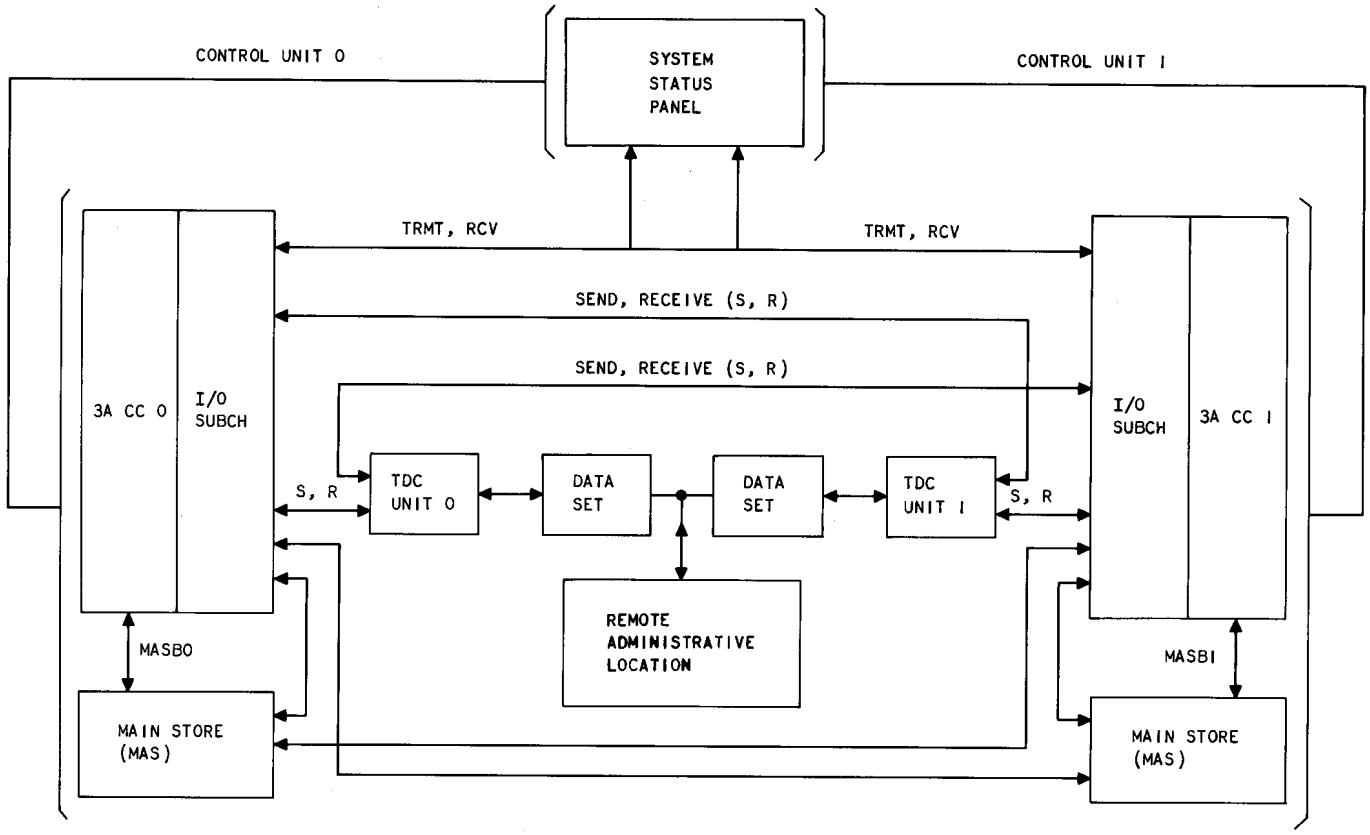


Fig. 2—Tape Data Controller Unit Interface Block Diagram

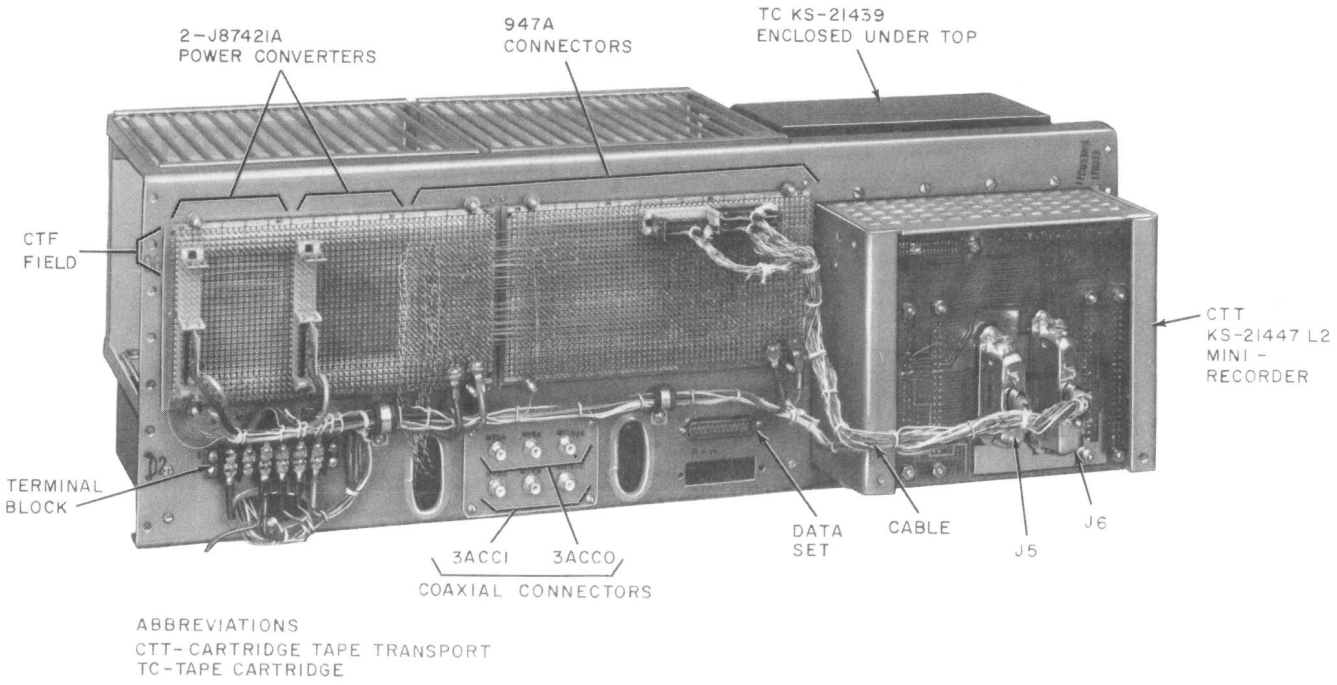


Fig. 3—Tape Data Controller Unit "0" or "1" J1C053A Rear View

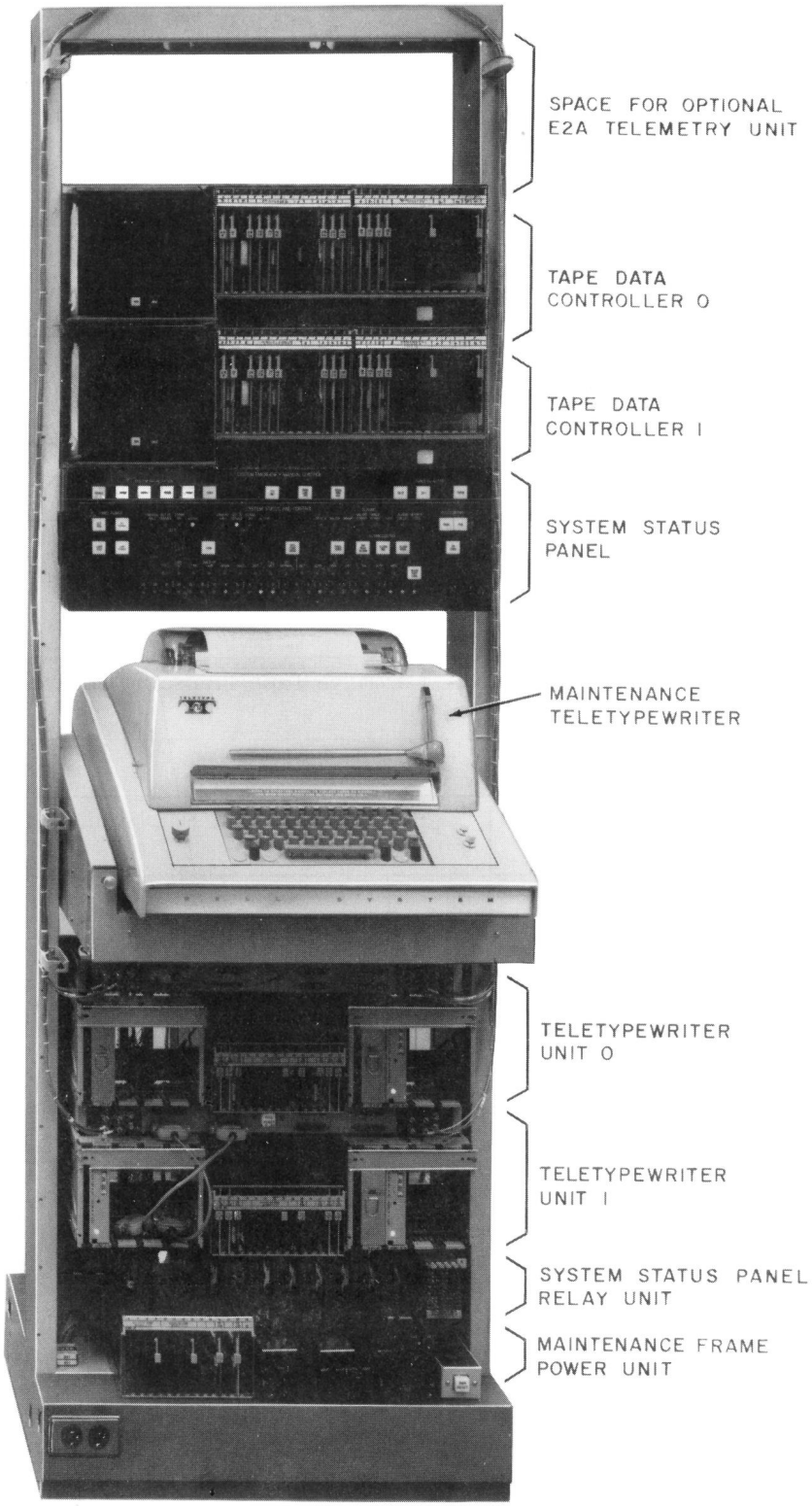


Fig. 4—Maintenance Frame

2.04 These circuit packs group together electrically to perform specific functions. These functions as well as type and location are listed in Table A.

TABLE A

TDC CIRCUIT PACK IDENTIFICATION

LOCATION	CIRCUIT PACK TYPE	FUNCTION
44-39	J87421A	+5 Volt Power Supply
34 33 32	JK5 JK6 JK7	Serial Peripheral Interface Circuitry (SPI)
17 16	JK8 JK9	Bus Terminator (BT)
30 29 28 27	JK10 JK11 JK12 JK13	Buffer Circuitry (Buf)
22 21 20 19	JK16 JK17 JK18 JK19	Cartridge Tape Transport Controller (CTTC)
24 25	JK15 JK14	Synchronous Data Set Circuit (SDSC)

2.05 Should the optional data set function be used, type JK14 and 15 circuit packs would be inserted into locations 25 and 24, respectively, as shown in Fig. 1.

B. Tape Data Controller Power (Fig. 1)

2.06 Logic level power is distributed to the circuit packs from two J87421A power converters (Fig. 5). These converters located in position 39 and 44 of the 87B apparatus mountings develop +5 volt outputs from +24 volt and −48 volt inputs.

2.07 The power converters have light emitting diode indicators that indicate incorrect output voltage. The indicators will light if the output voltage goes above +5.36 volts (overload) or below +4.66 volts (underload).

2.08 A manual switch designated TDC POWER (Fig. 1) mounted on the right side of the switch bracket assembly controls the +24 volt and −48 volt to the power converters and cartridge tape transport. Power is available if the TDC POWER switch indicator is illuminated.

2.09 The J87421A and JK circuit packs plug into 947C and 947A connectors (Fig. 3), respectively. The connectors are mounted through a Multi-Layer Printed Wiring Board that furnishes +5V power and ground to the connectors (Fig. 6). Signal paths between circuit packs are wire wrapped to connector pins (Fig. 3).

2.10 Mounted through the wiring board above and below the connectors are Coaxial Terminal Fields (CTF Fig. 3 & 6). These fields are normally used for coaxial cable connections; however, in the TDC unit application they serve as a connector for the TDC circuit and CTT interconnecting cable (Fig. 3).

2.11 Information is transferred between the 3A CC and TDC units by way of coaxial cables. These cables connected between the 3A CC's I/O and TDC unit jacks MYSA, MYRA, MYSB and MYRB (Fig. 3). Cables between 3A CC 1 and

MYRB, 3A CC 0 and MYRA transfer information to the TDC circuits, and cables between 3A CC 1 and MYSB, 3A CC 0 and MYSA transfer information to the 3A CC.

C. Cartridge Tape Transport (Fig. 7)

2.12 The Bell Labs designed KS-21447, L2 Mini Recorder is a separate unit attached to the TDC unit mounting plate (Fig. 3). The power and control cables, mounted in the rear, connect from the TDC circuits CTF and power terminal board to J5 and J6 of the CTT. The cable connected to J6 provides interface for logic, contol and power, and the cable connected to J5 provides the interface for all input/output data.

2.13 Removal of the front cover provides access to four circuit packs held in place by eight card guides. These circuit packs designated CP1 through CP4 provide logic and control, servo, read, and write circuitry. The CTT has a 4-track read-after-after-write head (only 3 are used for writing) and a 4-track erase head. It provides status sensing for End of Tape (EOT), Beginning of Tape (BOT), Cartridge in Place (CIP), and Write Protect.

2.14 The tape drive system is a capstan motor assembly. It is located at the front center of the CTT and is controlled by the processor or two manual pushbuttons labeled REW and UNLD. The two pushbuttons must be enabled by the processor to provide manual rewind and unload operations.

2.15 The CTT is air-cooled through a vent plate and has a cover to protect the data cartridge from dust contamination.

D. Tape Cartridge (Fig. 8 & 9)

2.16 The KS-21439 TC consists of a case 4 by 6 by .66 inches housing 300 feet of 1/4-inch wide magnetic tape, drive system, and sensing and protection devices.

2.17 The case consists of an aluminum base plate which serves as a reference mounting plane and the tape hub and belt pulley axle-mounting plate. The case has a plastic cover with a tape access door. The door is spring loaded and automatically closes when the cartridge is removed from the transport and opens as the cartridge is inserted allowing tape to tape head contact.

2.18 The tape is transported between hubs by an internal belt that is coupled by an internal belt capstan to the CTT drive motor capstan. Located at the top and bottom of the supply hub is an enlarged flange. This flange prevents the tape from rubbing any stationary surfaces.

2.19 Hole patterns placed at appropriate locations on the tape allow for BOT, EOT, Early Warning (EW) and Load Point (LP) sensing (Fig. 10). A mirror mounted in the case directs light through the hole patterns to sensors in the CTT.

2.20 Located in the case is a file protect device (File Protect Plug). This device, when activated, prevents writing on tracks 2, 3, and 4. (Track 1 is always protected.) When the File Protect Plug is rotated to the "SAFE" position no writing can take place. For normal operation, the plug should be set to the NON-SAFE position.

3. FUNCTIONAL DESCRIPTION

A. General

3.01 The 2B processor main store is a volatile semiconductor memory and is therefore subject to data multilation. To give the 2B processor a quick recovery capability, it is equipped with two backup memory storage facilities (TDC unit and tape cartridges).

3.02 The on-line 3A CC attempts to keep the on-line and standby MASs identical. If errors accumulate in both MAS to a point that the processor cannot configure itself to function efficiently, the error information will be corrected from data stored on tape.

3.03 If a bootstrap is necessary, the microcode program initializes the designated TDC unit for the affected 3A CC and the Common System Initial Program Loader (CIPL) will be written into the affected main store. The CIPL is a subfile of the Bootstrap file and gives the 3A CC enough intelligence to determine which MAS blocks must be restored, select these blocks from tape, and read them into the affected store areas. After the CIPL or "Bootstrap program" is written into core, hardware initialization takes place and

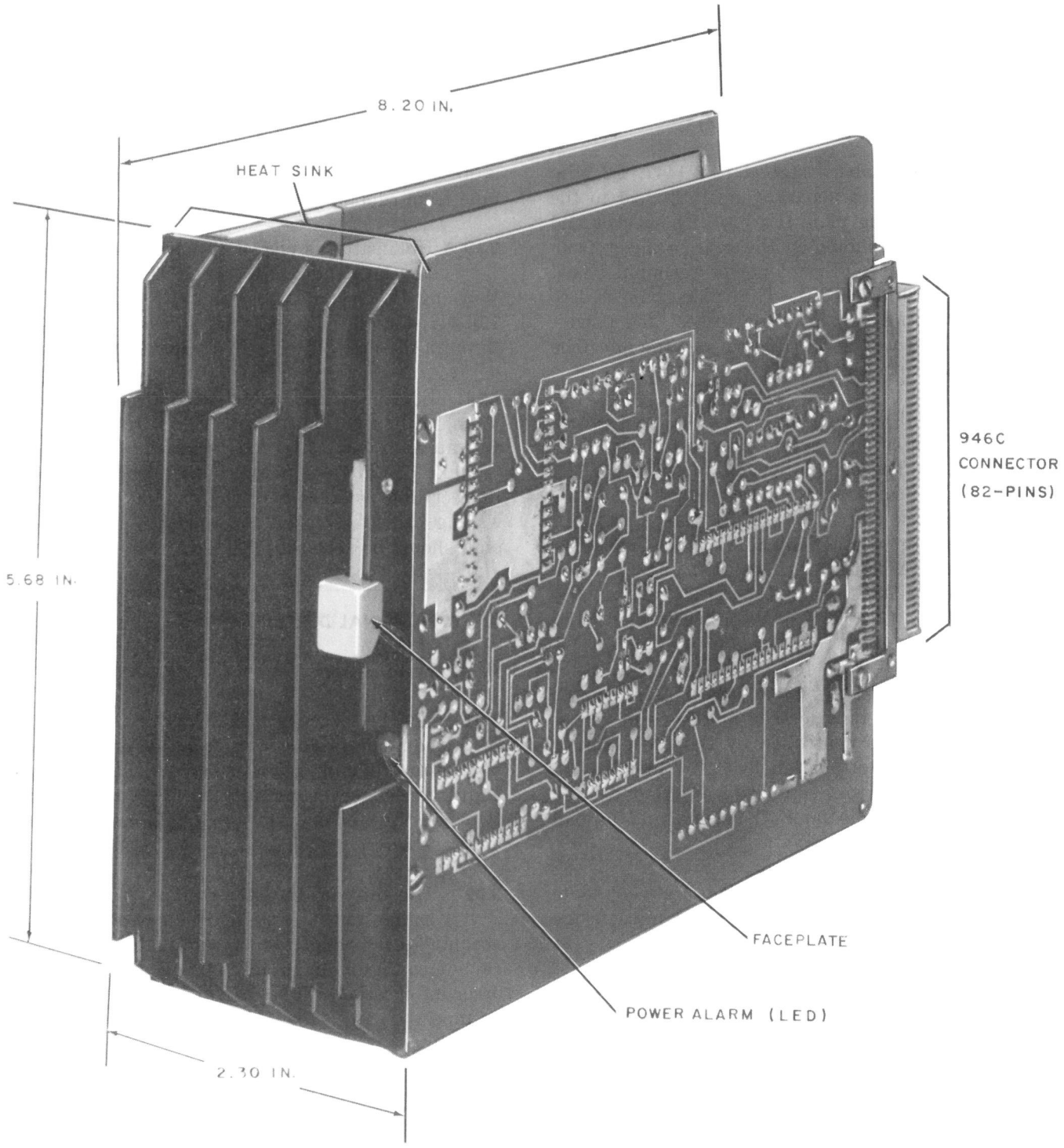


Fig. 5—S7 Power Converter

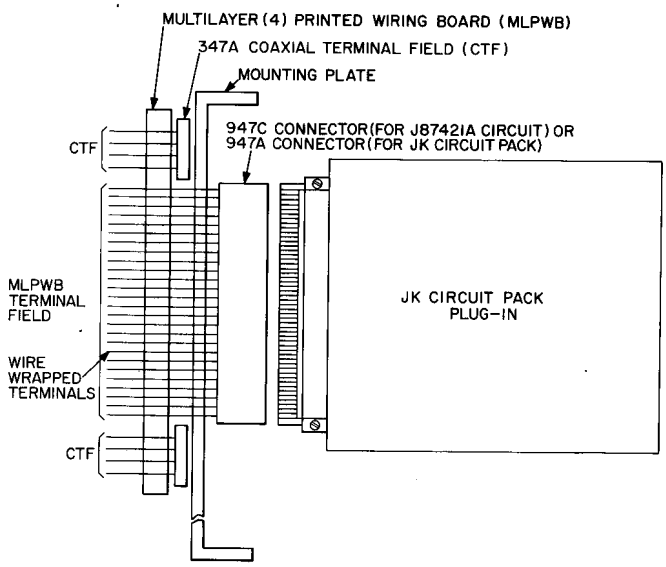


Fig. 6—Side View of TDC MLB Assembly Associated Connectors, and Circuit Pack

verification checks are made to determine the operating capability of the 3A CC. If the 3A CC can operate as the on-line 3A CC, the other TDC unit is made available and the MAS writing process will continue using two TDC units (this speeds up recovery time). If the other TDC unit is unavailable, the process continues using one TDC unit.

3.04 TDC unit initialization and MAS writing can also be initiated from manual control buttons located on the system status panel.

3.05 During a normal operating mode the control of the TDC unit can be established through processor programs. The cartridge tape handles (CTAPH) program allows other (client) programs to perform such operations as read, write, read continuous, read one block, position tape within a file, backspace one block at a time, and open file.

3.06 Figure 11 is a block diagram indicating the interface required to establish communications between the 3A CC and the TDC units.

3.07 Information is exchanged between the 3A CC serial I/O channels and the TDC unit in spurts of serial bipolar pulses. There are 20 I/O main channels comprised of 20 subchannels each. The TDC unit interface requires two subchannels, one from 3A CC 0 and one from 3A CC 1 to each unit.

3.08 The information is transferred in 21-bit messages formulating commands or data words. These words are formated into a 3-bit start code, 8-low and 8-high ordered data or control bits, and two parity bits (one following each set of eight data bits and designated PL and PH). The replies to these words are 21-bit data or status words.

B. TDC Circuits

3.09 The TDC circuit provides an asynchronous interface and control unit between the 2B processor and slow serial data from the CTT and optional data set terminal. The TDC circuit is divided into logical devices:

(1) Serial Peripheral Inteface

(2) Cartridge Tape Transport Controller

(3) Buffer

(4) Synchonous Data Set Controller

(5) Bus Terminator

3.10 The ***serial peripheral interface*** generates the timing and command signals required to transfer information between the 3A CC and TDC circuits. Information is transferred serially from the 3A CC to the serial peripheral interface and in parallel from the serial peripheral interface to the cartridge tape transport controller, buffer, synchronous data set controller, and bus terminator. All information exchanged between the 3A CC and the TDC unit passes through the serial peripheral interface.

3.11 Data information is transferred to either a buffer circuit register or a bus terminator register. Data in the buffer register will be serially shifted into one of two 1024-bit buffers to be written on tape or sent to the optional data set terminal. Data transferred to the bus terminator register is used during maintenance operation to determine if the parallel bus is operated properly.

3.12 Command information sent to the serial peripheral interface is sensed on the parallel bus by all perpheral devices. Each command is

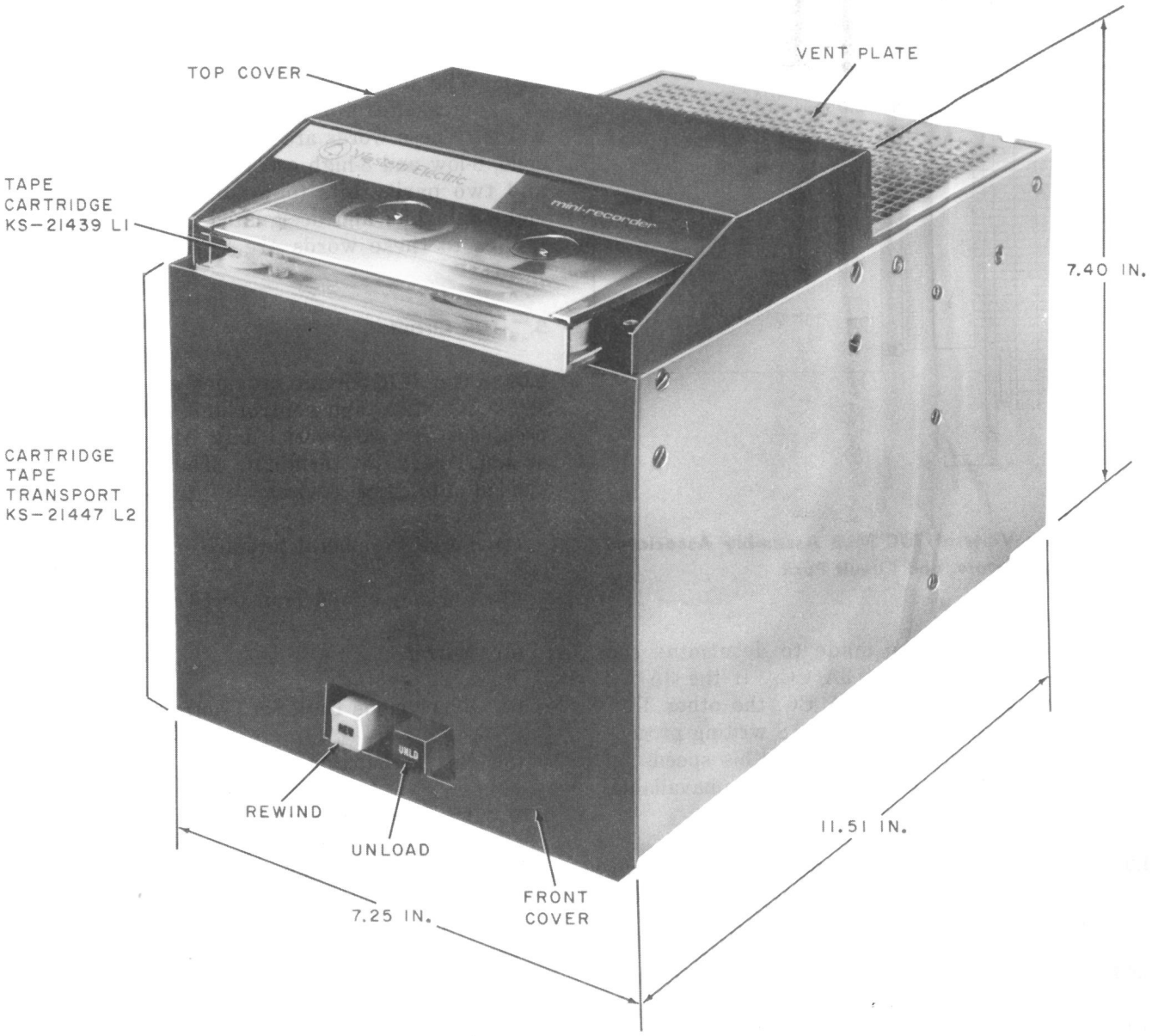


Fig. 7—Cartridge Tape Transport—KS-21447 L2 and Associated Tape Cartridge—KS-21439 L1

defined by a device code and only the approprite unit will respond to it.

3.13 The parallel bus consists of 32 leads connected between the serial peripheral interface and other devices. The 32 leads include 16 information leads, 6 control leads, 7 response leads, and 1 clock lead.

3.14 The 16 information leads are bidirectional leads used to either send data and commands to the devices or receive data and status from the devices.

3.15 The 6-control leads are Send Data, Initialize, Acknowledge Interrupt, Send Status, Receive Command and Receive Data. The Send Data, Initialize, Acknowledge Interrupt and Send Status control signals are generated from the serial peripheral interface commands defined in Table B. It should be noted that the Send Status control signal is also generated on every command with a

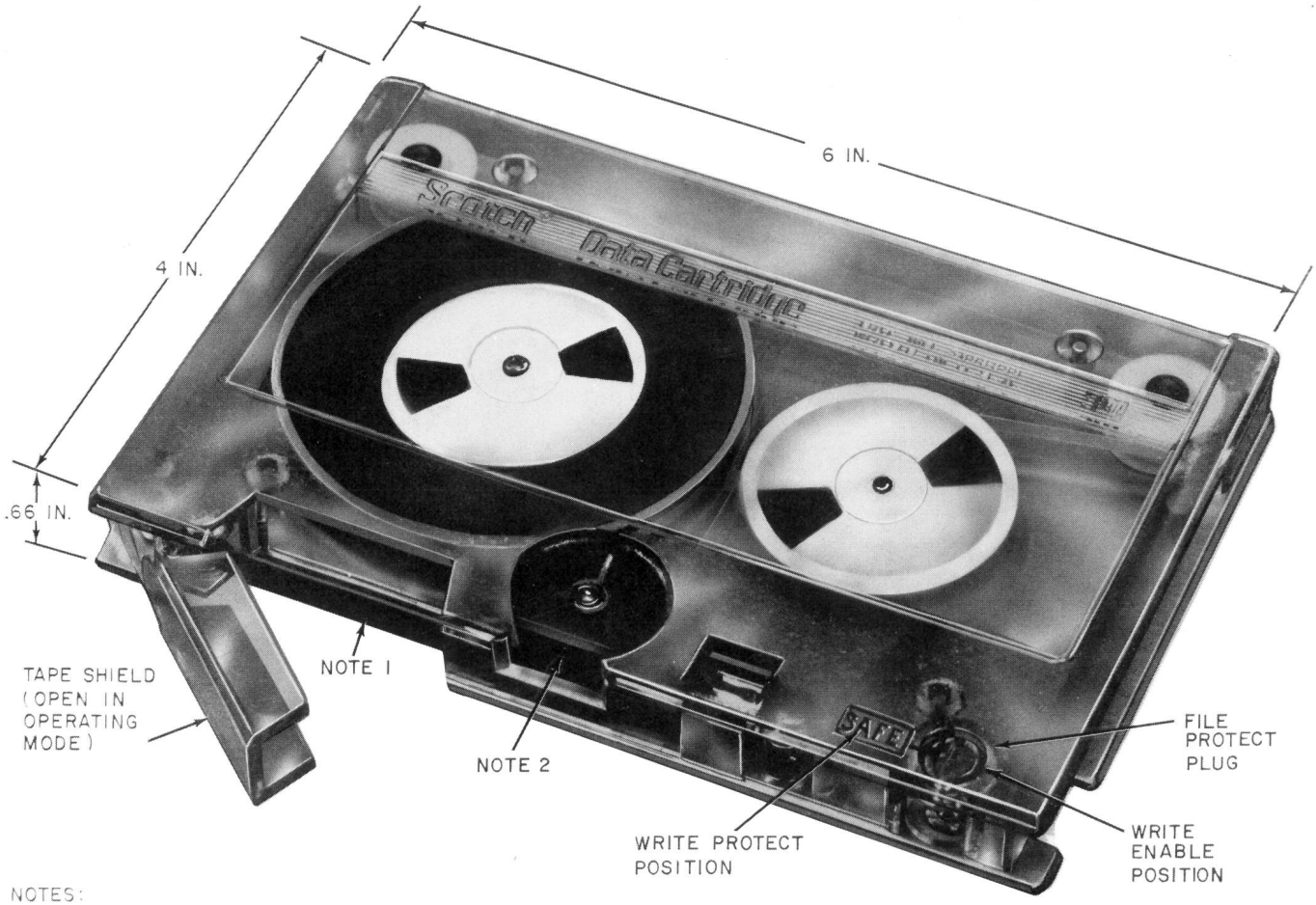


Fig. 8—Data Cartridge—KS-21439 L1

101-start code. Therefore those devices having status reply capabilities will transfer status information to the 3A CC in response to every command with a 101-start code.

3.16 The Receive Command control signal is generated from the 101-start code. This start code combined with a proper device code enables the appropriate device to accept succeeding control signals. All other devices will ignore the command.

3.17 The Receive Data control signal is generated from the 011-start code. This signal requests the previously addressed device (buffer or bus terminator) to except the succeeding data information.

3.18 Five of the seven response leads are ready (RDY), wait (WAIT), synchronization (SYNC), error (ER), and interrupt (INT). The devices send responses to the 3A CC through these leads.

3.19 The addressed device transmits a logic level "1" over the RDY lead to indicate that it has executed the previous command to a point where it is ready to respond to the next command.

3.20 If a control signal is given to the addressed device on the bus when it is not ready, the

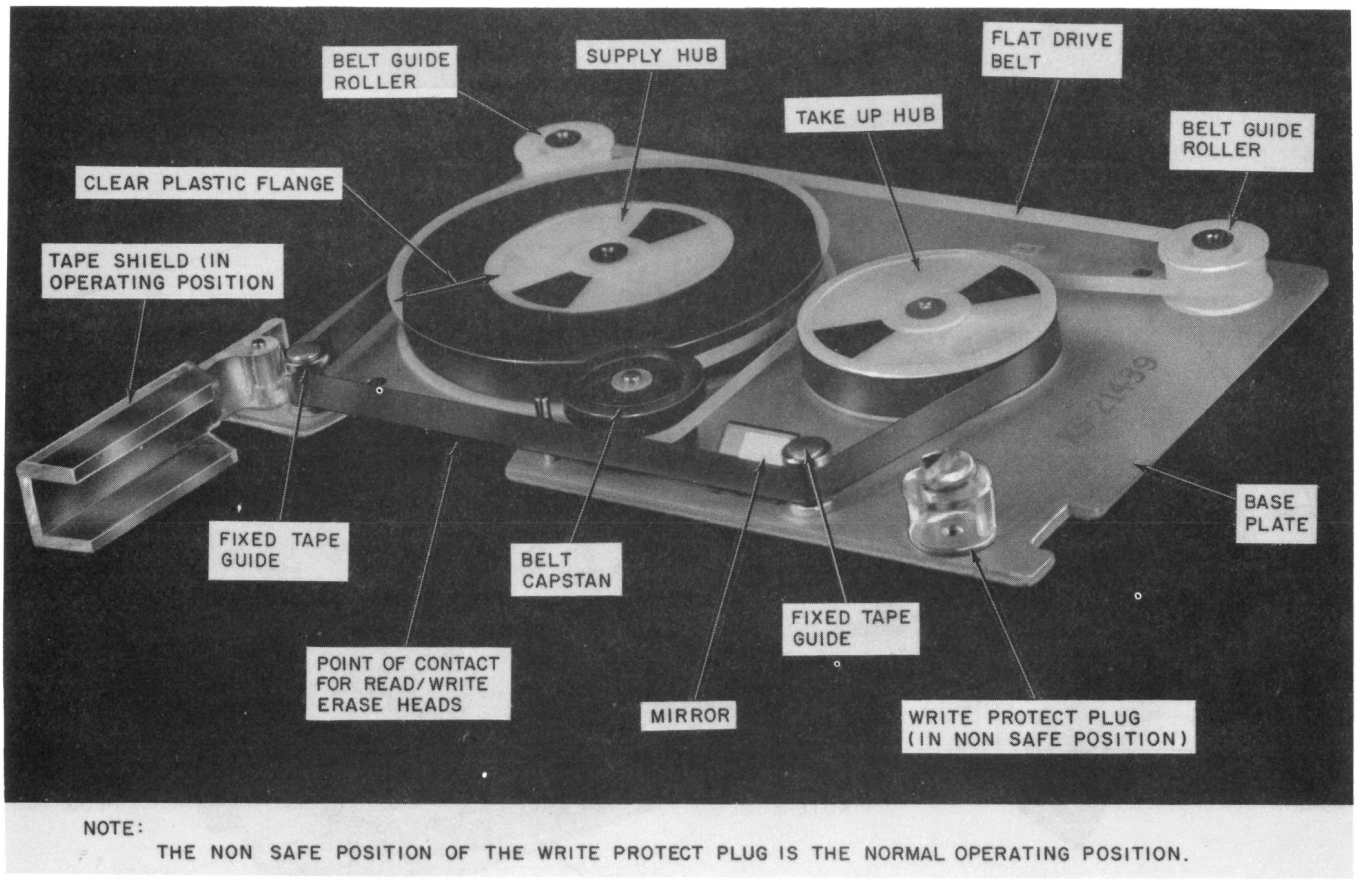


Fig. 9—Data Cartridge—KS-21439 Transparent Cover Removed

device will set the WAIT lead to a "1". The data and control signal will be held steady until the WAIT is set to "0" by the device. The SYNC signal is a response to the control signals. The response is a logic 1" written 250 ns after a control signal is issued and a logic "0" within 250 ns after a control signal is removed. It coordinates with the WAIT and RDY signals to properly time the gating of information out of the serial peripheral interface.

3.21 ER is set to a "1" whenever the addressed device has discovered an abnormal condition.

3.22 INTP is set to "1" when any device on the bus wishes to interrupt the 3A CC (not used in 2B).

3.23 The remaining two leads are Generate Parity and Generate Parity Reply. These leads are used to control the generation of parity bits for the reply words resulting from a send status control signal. The reply word from a device is gated on to the parallel bus and a generate parity signal is sent to the bus terminator from the device. The bus terminator generates the proper parity and sends a signal back to the device acknowledging the generation of parity.

3.24 The ***cartridge tape transport controller*** provides the control and timing signals for tape track selection, tape reading and writing, and, tape motion. All information transferred between the cartridge tape transport and 3A CC passes through the cartridge tape transport controller. The cartridge tape transport controller phase encodes this information before it is written on tape. It generates the preamble and postamble and adds them to each block of data when writing on tape, and removes them from the data blocks being transferred to the buffer during read operations.

3.25 The cartridge tape transport controller provides a cyclic redundancy check circuit for read and read-after-write error detector. Data

written on tape is compared with data sent to the tape to determine if the data was written correctly.

3.26 The ***buffer*** unit provides two serial buffer memories and their associated circuitry to temporarily store data transferring to or from the cartridge tape transport or optional data set terminal. It provides counter signals and status flags to indicate to the 3A CC and serial peripheral interface device when a buffer has been serviced. (The buffer has the capability of interrupting the 3A CC for servicing; however, this feature is not used in the No. 2B ESS.)

3.27 Each buffer memory is 1024 bits long. The gating paths for data and shift pulses for the two buffers are such that the 3A CC always has access to one buffer and the selected peripheral has access to the other. While the peripheral unit fills or empties the on-line buffer, the 3A CC empties or fills the off-line buffer.

3.28 The peripheral unit will transfer information to a buffer only on command from the 3A CC. The buffer will control the amount of information transferred but not the direction of transfer.

3.29 Communication between the buffer and other peripheral devices is established over the 8-lead serial bus. This bus provides a path for signaling and transmitting serial information between the buffer and other devices. Only one peripheral device can use these leads at a given time.

3.30 The following is a brief description of the eight serial bus leads.

- Buffer Active Counter Carry (BACR O)—A low going pulse on this lead indicates to the peripheral devices that the on-line buffer counter has been clocked with 1024 pulses on the Buffer Shift Pulse lead and the buffers have switched.

- Buffer Active 16-Bit Counter Carry (BA16CR O)—A pulse on this lead indicates to the peripheral device that the on-line buffer counter has been clocked with 16 pulses on the BSHP O lead.

- Buffer Shift Pulse (BSHP O)—This is the clock pulse lead for the on-line shift register. A clock pulse supplied by a peripheral device shifts data into or out of the on-line shift registers.

- Serial Data Out (SDOT O)—Data is shifted out of the on-line buffer onto this lead in a nonreturn to zero information format in response to shift pulses on the BSHP lead.

- Serial Data In (SDIN O)—A peripheral device may gate information on to this lead only during a read mode. This data is shifted into the on-line buffer by BSHPO.

- Buffer Overflow (BOFL O)—A logic 1 is transmitted over this lead at the coincidence of Buffer Ready flag being set and the trailing edge of the active buffer counter carry pulse. The last active buffer will remain in the on-line position and no more clock pulses will be accepted from the peripheral devices.

- Fill the On-Line Buffer (FILL O)—A peripheral device may cause right adjustments of a partial message in the on-line buffer. This feature is required for devices which handle data blocks that are not in even increments of the buffer size (1024 bits). The buffer uses its own clock to right adjust.

- Buffer Clock (BCLK)—The buffer unit has a free-running clock for the purpose of stuff and fill operations. A device specifically designed to operate with this buffer may use this clock for other purposes.

3.31 The ***bus terminator*** provides the proper loading to electrically terminate the common parallel bus and serial buffer bus leads. It generates the proper parity for status words originating from other circuits and aids in establishing the integrity of the parallel bus during maintenance operations.

C. Cartridge Tape Transport

3.32 The cartridge tape transport provides the hardware and circuitry necessary to control the tape motion, indicate status, and read and write information from or on the tape cartridge. It writes and reads data in the American National Standards Institute (ANSI) 1600 bit per inch phase encoded format.

3.33 The cartridge tape transport drives the tape cartridge at a constant operating speed of 30 inches per second in forward and reverse. It also has a fast forward or rewind speed of 90 inches per second.

3.34 Four circuit packs, CP1 through CP4, provide the circuitry necessary to the operation of the cartridge tape transport:

- CP1-LOGIC and CONTROL CIRCUIT decodes the motion commands from the cartridge tape transport controller and indicates the status of the system. Indications of tape motion, unit on-line, tape off reel, BOT and EOT are sent to CP3 and CP4 to control reading and writing of the tape cartridge and to the I/O connector for use by the cartridge tape transport controller. The decoded motion commands are sent to CP2.

- CP2-SERVO CIRCUIT controls the speed of the DC motor which drives the tape cartridge. It deskews and decodes the marker detectors to provide the indications of Beginning of Tape Marker (BOTM), Load Point-Early Warning Marker (LPEWM), and End of Tape Marker (EOTM).

- CP3-WRITE CIRCUIT decodes the write track selected and provides write current to the write head. The status information sent from CP1 can inhibit writing of data.

- CP4-READ CIRCUIT reads information off of the tape and decodes it into digital data. It reads 1600 bits per inch, phase encoded formatted data from a tape running at 30 inches per second. It decodes the track to be read and when data is stable clocks it to the cartridge tape transport controller.

4. COMMANDS

4.01 The 3A CC controls the TDC unit by transmitting commands to the serial peripheral interface, cartridge tape transport controller, buffer, and bus terminator. The commands to these devices are identified by a command code, device code, and 101 start code. Each device addressed by a command responds with a reply containing status or data information. Normally the reply, if it is not a data word, contains a device code and a start code of 011 (any exceptions are identified in the tables describing the commands and replies). Data words transfered between the 3A CC and TDC unit have a start code of 011 but do not have a device code.

4.02 Illustrations of data word, command and reply formats for each device, tabularized listings of each command function, and expected reply are detailed in the following figures and tables:

- Serial Peripheral Interface Fig. 12 Table B

- Cartridge Tape Transport Controller Fig. 13 Table C

- Bus Terminator Fig. 14 Table D

- Buffer Fig. 15 Table E.

5. TAPE DESCRIPTION

5.01 The 2B ESS tape cartridge contains a 4-track magnetic tape. This tape serves as a storage device for information necessary to restore the 2B processor MAS.

5.02 The write protected Track 2 (Fig. 16) contains the Bootstrap and Generic program. Track 2 contains the check sum and translations. Track 3 contains the remaining translations, patches, and a backdate of translation. Track 4 contains the directory.

5.03 The bootstrap file contains instructions in a format that can be loaded by the processor microstore. These instructions, when loaded, restore the system to a state of initialization that allows loading of mutilated areas of MAS off of the appropriate tape files.

5.04 The bootstrap file is segmented into two subfiles. The first subfile contains the common system initial program loader (CIPL), and the second subfile contains excerpts of the generic program.

5.05 The program reload operation can be initiated manually from the System Status panel, or it will be initiated automatically by the processor microcode instructions if store mutilation is recognized.

5.06 The check sum file contains information pertaining to system parameters needed by the bootstrap program to reload MAS. Within this file there are two check sum words for every 4096-word MAS blocks stored on tape. These words are constants derived from exclusive oring all the words of a 4096-word block. The constants are used in comparison with regenerated constants derived from the same words to determine which blocks have become mutilated.

5.07 The backdate file contains information that, when written over the present translations, will generate a prior version of translations in the MAS.

5.08 The Directory gives the physical position and other related data concerning every file.

5.09 The generic, translations, and patch files are data blocks containing information, that when read into the 2B processor MAS, will restore the 3A CC software to an operating condition.

5.10 The MAS data stored on tape is formated into blocks and files. A sequential number of blocks identified by a given name of up to eight characters is known as a file (as an example the 8-character name for the bootstrap file is BOOTSTP). A block (Fig. 17) is a grouping of 16-bit words in multiplex of 64. for the No. 2B ESS a block contains 898 16-bit words. Each block contains a preamble word, address word, cycle redundancy check word, postamble word and 894 data words. (The preamble and postamble words are not considered part of the 64-word multiple.) Since the 2B MAS word width is 24 bits, the 894-word data area is capable of storing 594 No. 2B ESS words.

5.11 The first two words of the data area are length and address information. The length information indicates the number of consecutive store words to be loaded from the starting address.

5.12 The data area is preceded by the preamble and block address. The preamble is a hardware block synchonizing code and the block address defines the block physical position from BOT. Terminating the block is a cyclic redundancy check (CRC) character and a postamble word. The postamble is another hardware block synchronizer and the CRC is used to determine the quality of data transferred.

5.13 There is a guaranteed 3564 inches of usable tape length. Each block plus interblock gap requires 10.53 inches $\pm$.43 inches allowing 338 $\pm$14 blocks on a track. Seven blocks are required per 4096 No. 2B ESS MAS words (six 594-word blocks and one 532-word block).

6. MAINTENANCE FEATURES

6.01 The TDC unit's circuitry is designed to test the accuracy of information transmitted to and from the 3A CC. If an error is detected, the TDC unit responses to the 3A CC will identify a fault status. The isolation of the circuit at fault can be simplified by program diagnostic routines.

6.02 Each TDC unit has circuitry to check the parity of serial words transmitted from the 3A CC to the TDC unit. If a parity error is detected in the serial information transmitted from the 3A CC serial peripheral interface (SPI), the SPI responds by sending a "serial parity error" reply to the 3A CC. This word is designated by a 101-start code, 111 device code and bit 8 set to a "1". If a parity error is detected in a word transmitted over the parallel bus from the SPI to the buffer, the buffer responds by sending a "buffer status" word with a 101-start code, it's own device code, and the parallel parity error bit set to a "1" back to the 3A CC.

6.03 The cyclic redundancy check in combination with the read-after-after-write circuitry provides the capability of testing the accuracy of tape data writing. The cyclic redundancy check circuitry and the word block cyclic redundancy check character provides the capability of testing the accuracy of tape data reading. Any command to the CTTC can be issued to determine the status of the cyclic redundancy check circuit. If the test indicates an error, the CTTC's reply word will be returned to the 3A CC with a 101-start code.

6.04 When a "send status" (SST) command is issued, the reply word start code of the addressed device indicates the error status. If the addressed device has a fault the reply word start code will be 101.

7. DIAGNOSTICS

7.01 The common system tape maintenance (CTAPM) program provides the capability of isolating faults within the TDC unit. This

program provides sub-programs that isolate the fault to the cartridge tape transport or TDC Circuits. If the fault is detected in the TDC circuits, these sub-programs can be used to isolate the fault to a particular device (serial peripheral interface, buffer, cartridge tape transport, and bus terminator).

7.02 The common system tape maintenance program is initiated manually and the resulting failure message printout will indicate the faulty device. These maintenance programs also serve as periodic exercise tests when called automatically.

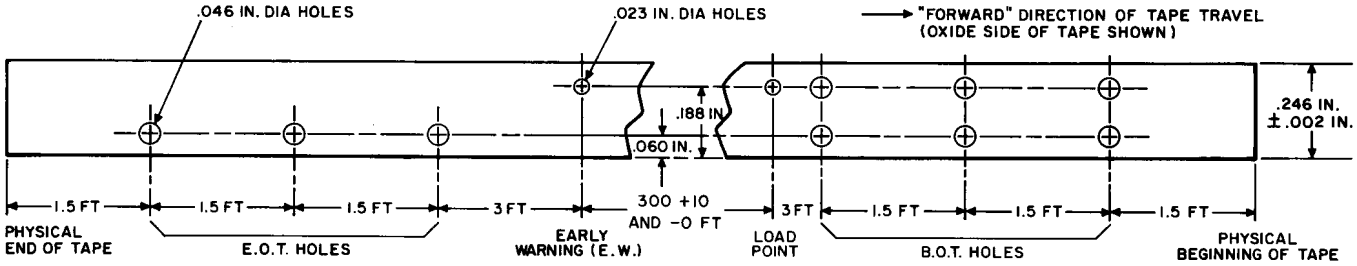


Fig. 10—Tape Hall Pattern for Sensing Tape Position

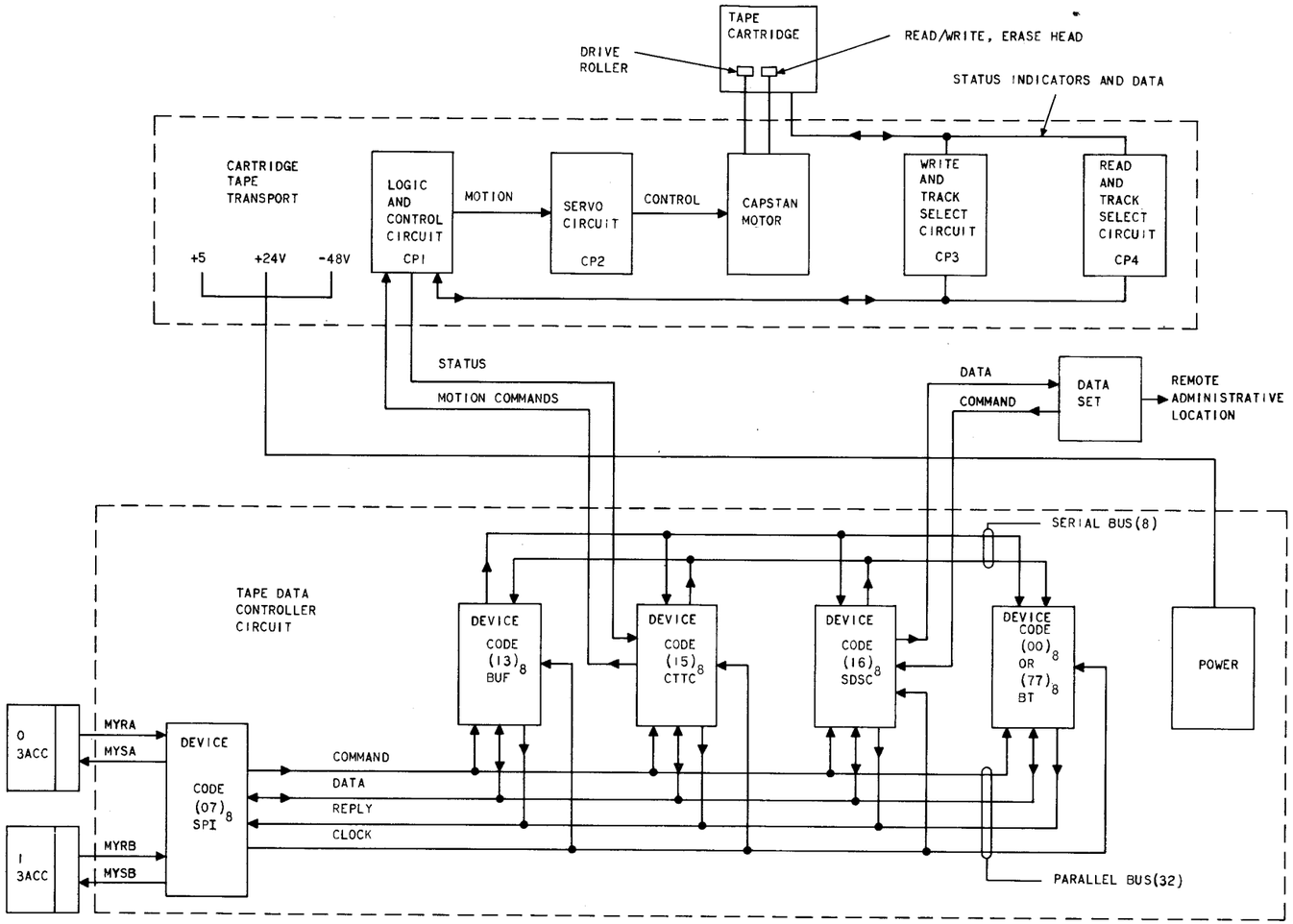


Fig. 11—Tape Data Controller Unit Functional Block Diagram

TABLE B
SERIAL PERIPHERAL INTERFACE (SPI)
COMMANDS

CMD CODE (OCTAL)	COMMANDS	FUNCTION
200	SEND DATA (SD)	A 16-bit data word with correct parity is transferred from a previously addressed device to the 3A CC. In 2B it is used to transfer data from the buffer to the 3A CC. The bus terminator and CTTC do not respond to this command.
100	INITIALIZE (INIT)	An initializing pulse is sent to all devices connected to the serial peripheral interface. All devices are forced to assume a known state. Upon completion of the order no device is addressed. The reply is all zeros with correct parity and an 011 start code.
040	ACKNOWLEDGE INTERRUPT (ACK INT)	The TDC unit does not interrupt the 3A CC in a No. 2B ESS; however, the command capability is present. The normal reply will be all zeros with correct parity and an 011 start code. If the BR (buffer ready) flag is set and the Buffer Interrupt is enabled, Bit 1 of the reply will be a 1. The 101 start code is returned if a device is addressed and this device has an error condition.
020	SEND STATUS (SST)	Sends the 3A CC status word with correct parity from a device previously addressed. The bus terminator responds by returning its register contents with a 101 start code. If no device is addressed, no reply is returned.
(Any bit pattern with an odd number of "1s")	SERIAL PARITY ERROR REPLY (SPE)	This reply is returned to the 3A CC from the serial peripheral interface in response to any 21-bit message containing an odd number of ones.

TABLE C
CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC)
COMMANDS

CMD CODE (OCTAL)	COMMANDS	FUNCTION
0 (Bit 7 of command word is an "0")	TAPE STOP (T STOP)	Stops the tape. If the read head is crossing data, the stop order will be issued at the next interblock gap (IBG). The heads will stop in an IBG of the addressed track from read/write speeds, unless the stop command is issued near the end of the IBG. The heads may not be in a gap if stopped from a fast speed because of the coast time. The reply is the command tape transport controller Command Reply.*
*The reply to all command tape transport controller commands tape status will be the Command Reply. Refer to Table D for details.		
1 (Bit 7 of command word is an "0")	TAPE REWIND (TRWD)	This command moves the tape in the reverse direction at 90 inches per second (IPS) until BOT is reached then stops, starts and proceeds at 30 (IPS) to LP (load point) and stops. Software command or a manually initiated command performs the same function.
0 (Bit 7 of command word is set to a "1")	TRANSPORT MAINTENANCE STOP (TMSTOP)	TMSTOP command functions as follows: (a) Completely disables the transport. (b) Stops any operation in progress. (c) Motion commands will not be accepted by the transport. (d) Transport becomes deselected. (e) READY will go false (NOT READY). (f) CTT circuit will go into the maintenance state. *Note:* This state may be cleared by issuing the initalize or tape clear maintenance command.
1 (Bit 7 of command word is set to a "1")	TRANSPORT INITIALIZE (TINIT)	TINIT command clears all internal flags and then a "REWIND" (see other OCTAL 1 this table) is accomplished. *Note:* This command will not work if the "transport maintenance stop" command is in force.
2	TAPE SHIFT CYCLIC REDUNDANCY CHECK (TSCRC)	This command causes the 16-bits of the cyclic redundancy circuit register to be shifted to the buffers. After the CRC character has been shifted, a fill order is sent to the buffer circuits which will right-adjust the buffer containing the CRC character as the first word from the buffer. *Note:* This command functions only while in the maintenance mode.

TABLE C (Cont)

CMD CODE (OCTAL)	COMMAND	FUNCTION
3	TAPE WRITE INTERBLOCK GAP (TWIB1 - TWIB4)	This command writes (at 30IPS in the forward direction) on a preselected track (1 of 4) a magnetized gap time for 1.5 inches (Fig. 9) in length.
4	TAPE STATUS (TSTAT)	Refer to Table F and Fig. 14C.
5	TAPE FAST FORWARD (TFF1) - (TFF4)	Moves the tape in the forward direction at 90IPS. Though the data is ignored, the "Data Detect" bit of the tape status command can be monitored to count the number of blocks crossed on any one of four tracks.
6	TAPE WRITE STOP (TWSTP)	The cartridge tape transport controller is enabled to stop a write operation at the end of the data coming from the loaded on-line buffer. The cartridge tape transport controller adds the postamble, creates a portion of the interblock gap, and then stops the transport. Track address is not affected by this command and write stop clears automatically following the sequence. *Note:* Write stop should only be used during a write operation.
7	TAPE READ A BLOCK (TRB1 - TRB4)	This command reads one block of data from a preselected track (one of four). The transport will stop in the interblock gap following the block being read. If the buffer being filled by the cartridge tape transport controller is not full at the end of the data block, a fill order will be issued to the buffer circuits which causes a right-adjust of that buffer so that it can be properly unloaded by the 3A CC. There is no indication that a fill operation has occurred, so the 3A CC has to know how much data was in that block or an end of the file word should be used. A cyclic redundancy check is done as the data is shifted to the buffers. A cyclic redundancy check error status can be monitored at the end of the operation by issuing a status command and observing the start code of the reply.
10	TAPE MAINTENANCE (TMAINT)	The tape maintenance command disables the transport by taking it out of service. In this mode, any command except rewind may be sent to the cartridge tape transport controller with the expectation of the correct reply. Due to the transport being out of service "RDY" bit in reply word will show false (not RDY). While in this mode, the reply from a rewind command will be that of a stop. In this mode, the write read and cyclic redundancy check circuits may be completely exercised and due to command replies

TABLE C (Cont)

CMD CODE (OCTAL)	COMMAND	FUNCTION
10 (Contd)		being taken near the cartridge tape transport outputs, less a few gates the cartridge tape transport controller may also be completely exercised.
11	TAPE FAST REVERSE (TFR1 — TFR4)	This command moves the tape in the reverse direction at 90IPS. Data on the track is ignored, but the data detect bit (11) of the status command word may be monitored to count the number of blocks crossed on any one track.
12	TAPE CLEAR WRITE STOP (TCWS)	This command resets the write stop flag and is generally only used in a maintenance situation to cancel a tape write stop command.
13	TAPE WRITE (TWT1 - TWT4)	This command initiates the writing of one block of data on a preselected track. This data is phase encoded and is taken from the buffers. The cartridge tape transport controller generates and adds a preamble and postamble to the data block which are deleted during a read operation. The end of data to be written is indicated by issuing a tape write stop command to the controller. This command causes a postamble to be generated and written on the tape following the end of data from the on-line buffer. Also this command causes the transport to stop after writing a portion of the interblock gap. The write command initiates a read-after-write sequence within the cartridge tape transport controller during which the data being read back from the tape is compared to the data being written on the tape by the cyclic redundancy check circuit. The error status of the cyclic redundancy check may be examined by issuing a status command at the end of the write operation and observing the start code of the reply. This data is not shifted back via the buffers.
14	TAPE CLEAR CRC (TCCRC)	This command clears the cyclic redundancy check register; however, this command is functional only while in the maintenance mode.
15	TAPE BACK SPACE (TBS1 - TBS4)	The back space command causes the tape to move in the reverse direction at 30 IPS across one data block on any track. If the read head is stopped on a data block when the command is issued, it will move to the preceding interblock gap. During the back space command data is ignored but the data detect bit of the status word will indicate when the read head is stopped on a data block.
16	TAPE CLEAR MAINTENANCE (TCMTC)	This command clears or resets the maintenance mode. This command should not be issued unless the cartridge tape transport controller is in the stop mode.

TABLE C (Cont)

CMD CODE (OCTAL)	COMMAND	FUNCTION
17	TAPE READ (TRT1 - TRT4)	This command initiates a continuous read operation from a preselected track until a stop command is issued. A cyclic redundancy check is done as the data is shifted to the buffers. An error status may be checked during any interblock gap after a time elapse of 200 microseconds (into the gap), by issuing a status command to the cartridge tape transport controller and observing the start code of the reply. The cyclic redundancy check is cumulative over the full number of blocks read during a single read operation.

TABLE D
BUS TERMINATOR (BT)
COMMANDS

OCTAL ORDER CODE	COMMAND	FUNCTION
	BT address 0 and BT address 1 (BTADD0) (BTADD1)	The BT is addressed only in a maintenance mode by a device code of all zeros or all ones. Once addressed the BT will respond to any receive data bit configuration. The reply will be a match of the order and a 101 start code.

TABLE E
BUFFER (Buf)
COMMANDS

OCTAL ORDER CODE	COMMAND	FUNCTION
0	Buffer Status Reply Request (BSTAT)	This is a no-operation control order. The reply is the 16-bit buffer status word. Refer to Table G and Fig. 16B for bit definition.
1	Clear Buffer Ready Flag (BCLRBRF)	Clears the buffer ready flag. The reply is the 16-bit buffer status word.
2	Buffer Load State Commands	The reply for the following commands is the 16-bit buffer status word.
	Buffer Set Interrupt on and off BSINTØN BSINTØFF	Bit 9 set to a 1 or a 0 enables or inhibits the buffer ready flag demand interrupt capabilities, respectively. Bits 10, 11, and 12 of the order being zero reset the load, unload, and stuff states.
	Buffer Set Load State - Interrupt On (BSLDØN)	Buffer is primed to accept succeeding 16-bit data words from the 3A CC interrupt disable bit 9 is a Ø. Load State bit 10 is a 1.
	Buffer Set Load State - Interrupt Off (BSLDØFF)	Buffer is primed to accept succeeding 16-bit data words from the 3A CC. Interrupt disable bit 9 is a 1. Load state bit 10 is a 1.
	Buffer Set Unload Interrupt On (BSUNLDØN)	The buffer is primed to respond to succeeding send data command. Interrupt disable bit 9 is an Ø. Unload state bit 11 is a 1.
	Buffer Set Unload Interrupt Off (BSUNLDØFF)	The buffer is primed to respond to succeeding send data commands. Interrupt disable bit 9 is a 1. Unload state bit 11 is a 1.
	Buffer Set Stuff State Interrupt On Buffer Set Stuff State Interrupt Off (BSTFON) (BSTFOFF)	A partial message is right adjusted in the currently off-line buffer and the off-line buffer counter is incremented to the number of bits stuffed behind the partial message. Interrupt disable bit 9 is set to a Ø for BSTFON or a 1 for BSTFOFF.
3	Buffer Fill (BFILL)	Bits are shifted into the on-line buffer. The buffer ready flag is set when the operation is completed. The reply is the 16-bit buffer status word.
4	Not Used	
5	Buffer Clear the Off-Line Counter (BCLRØCN)	The current off-line buffer counter is cleared. The reply is the 16-bit buffer status word.

TABLE E (Cont)

OCTAL ORDER CODE	COMMAND	FUNCTION
6	Buffer Switch Buffers (BSWB)	The position (on-line off-line) buffers and their associated counters are switched. The reply is the 16-bit buffer status word.
7	Buffer Initialize (BINIT)	The buffer unit is reset. Both buffer counters and stuff counters are cleared. Buffer 1 is set on-line, and the stuff, fill, load and unload states are reset. The reply is the 16-bit buffer status word.

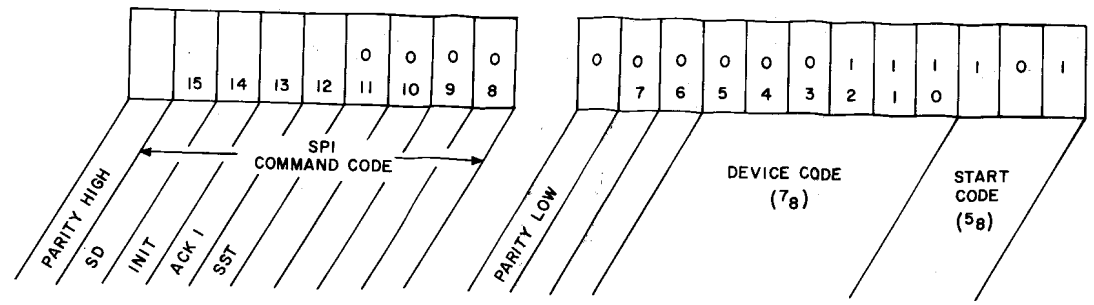
TABLE F
CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC)
TAPE STATUS (TSTAT) BIT FUNCTIONS

BIT NUMBER	BIT TITLE	FUNCTION
0-5	Addressed Device Code	Defines device being controlled.
6	Cartridge Write ENABLE	Bit set to a "1" indicates that tape tracks 2, 3, and 4 are writable. The file plug (Fig. 7) is not in the "SAFE" position.
7	READY STATUS	Bit set to a "1" indicates that the cartridge is in place and initialization has been completed.
8	END OF TAPE (EOT)	Bit set to a "1" indicates that the tape is in position at the end of tape. The EOT marker (Fig. 11) is sensed via light sensors.
9	TAPE OFF REEL (TOR)	Bit set to a "1" indicates the tape is broken or off the reel. If tape is moving, a tape stop is caused and all motion commands are inhibited.
10	TAPE IN MOTION	Bit set to a "1" indicates tape is moving.
11	DATA DETECT	Bit set to a "1" indicates data is being detected on a moving tape. Since the bit becomes an "O" when the tape is stop or an interrecord gap is detected, it provides a search function at high speeds (each data block can be counted). This bit is also used to indicate a valid data block is being read.
12	MAINTENANCE STATUS	Bit set to a "1" indicates to the 3A CC unit that the TDC unit is in a maintenance mode.
13	REWINDING	Tape is rewinding. Bit will remain a "1" until the load point marker is sensed. During this time all other commands to the TDC unit are inhibited.
14	Beginning of Tape (BOT)	This bit remains a "1" during the time BOT markers are passing the read head. (Fig. 11)
15	Manual Operation Enable	Bit set to a "1" indicates the cartridge tape transport is enabled to operate manually. Normally, the TDC unit will have been removed from service.

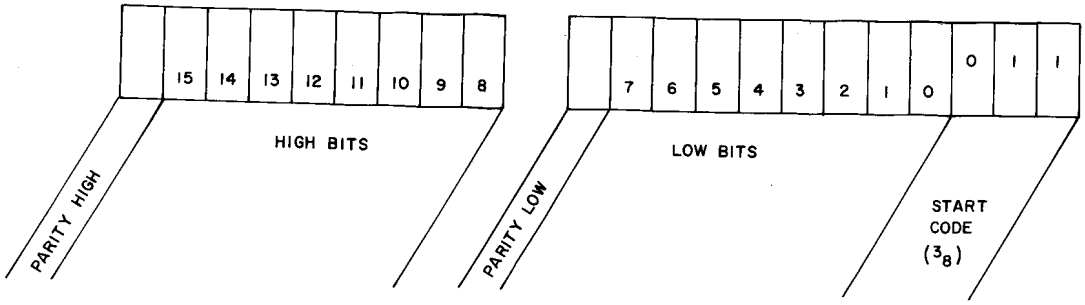
TABLE G

BUFFER STATUS WORD BIT DEFINITION

BIT NUMBER	BIT TITLE	FUNCTION
0-5	Address Device Code	Defines the device being controlled.
6	Parallel Parity Error (PPE)	If bit is set to a "1", a parity error was detected on the last 16-bit data word from the 3A CC. Buf status word reply will have a start code of 101.
7	Buffer Ready (BR)	Bit is set to a "1" indicates that the last active buffer was filled or emptied by the peripheral device and placed off-line.
8	Ready (RDY)	Bit is set to an "0" whenever (1) buffer unit is doing a "stuff" or a serial shift between the input/output buffer register and the off-line shift register. (2) immediately following the set "unload" command and a stuff command (3) after each receive data bit configuration sent to the buffer (4) during a stuff operation.
9	Interrupt off (INTOFF)	Not used.
10	Load State (LOAD)	When set to a "1" LOAD state is set. The buffer is primed to accept 16-bit data words from the 3A CC.
11	Unload State (UNLOAD)	When set to a "1", "unload" state is set. The buffer is primed to send 16-bit data words to the 3A CC for each send data command.
12	Stuff State (STUFF)	Bit set to a "1" indicates the buffer unit is performing or has completed a right-adjustment of a partial buffer message in the off-line buffer.
13	Active Buffer (ACTIVE)	When set to a "1", buffer 1 is online. When set to an "0", buffer 0 is on-line.
14	Buffer Overflow (BOFL)	Bit set to a "1" indicates the 3A CC did not service the last buffer ready flag before the peripheral device filled or emptied the currently active buffer. The coincidence of BR being set and the trailing edge of the 1024th shift pulse of the on-line buffer is BOFL getting set. The buffers will not toggle, and any further shift pulses from the peripheral device are ignored.
15	Fill the On-Line Buffer (FILL)	When bit is set to a "1", the buffer unit is in the process of right-adjusting the currently on-line buffer. The fill function is performed in response to a peripheral device signed or command from the 3A CC. The fill bit goes to "O" when the function has been completed.



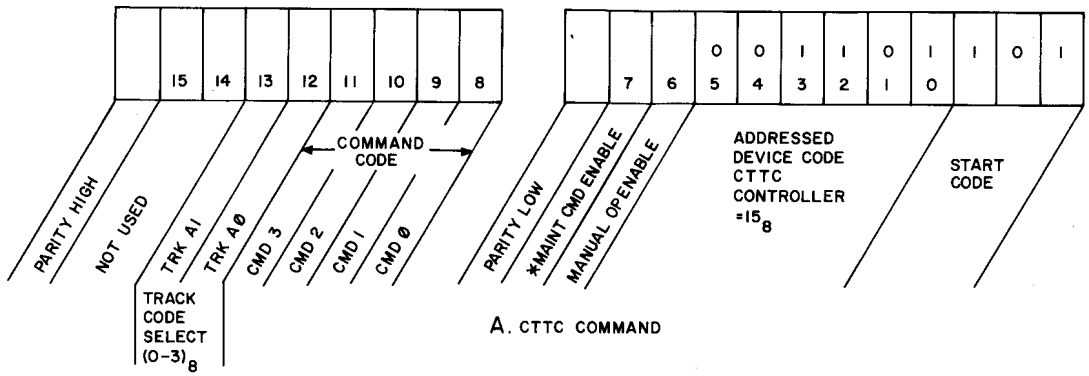
A. SPI COMMAND WORD



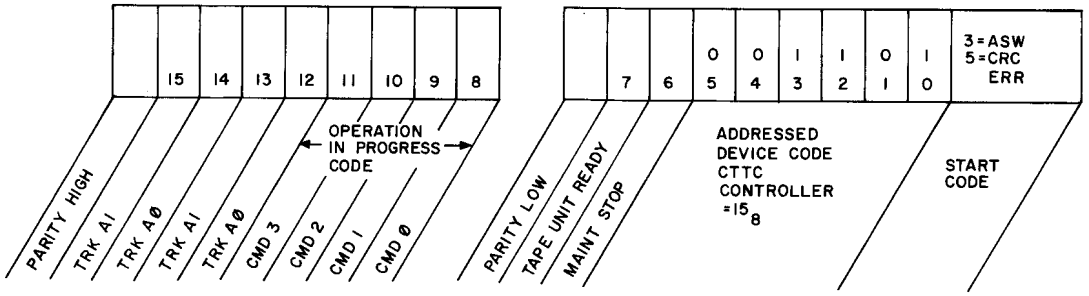
B. DATA WORD

SPI COMMAND CODES$_8$	
200	SEND DATA (SD)
100	INITIALIZE (INIT)
040	ACKNOWLEDGE INTERRUPT (ACK I)
020	SEND STATUS (SST)

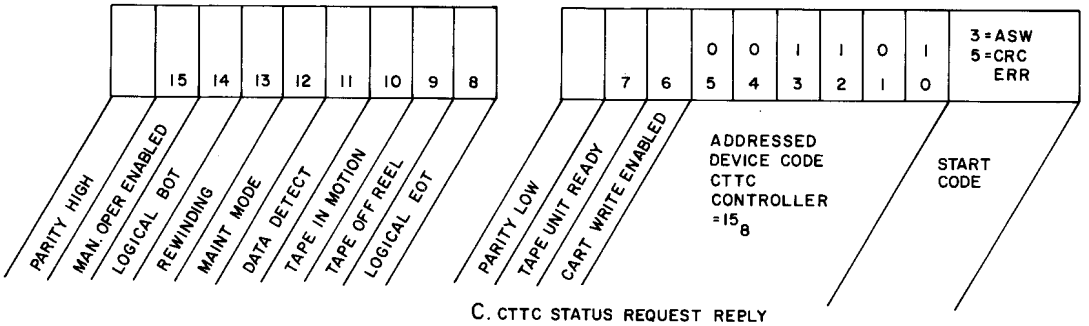
Fig. 12—Serial Peripheral Interface (SPI) Command and Data Word Format



A. CTTC COMMAND



B. CTTC COMMAND REPLY



C. CTTC STATUS REQUEST REPLY

* BIT 7 IS USED TO DESIGNATE 2 ADDITIONAL COMMANDS HAVING CMD CODES 0_8 AND 16_8

CTTC COMMAND CODES (INOCTAL) AND FUNCTION	
0 TAPE STOP 0 TRANSPORT MAINTENANCE STOP (BIT 7=1) 1 TAPE REWIND 1 TRANSPORT INITIALIZE (BIT 7=1) 2 TAPE SHIFT CRC 3 TAPE WRITE IBG 4 TAPE STATUS REQUEST 5 TAPE FAST FORWARD	6 TAPE WRITE STOP 7 TAPE READ A BLOCK 10 TAPE MAINTENANCE 11 TAPE FAST REVERSE 12 TAPE CLEAR WRITE STOP 13 TAPE WRITE 14 TAPE CLEAR CRC 15 TAPE BACK SPACE 16 TAPE CLEAR MAINTENANCE 16 TRANSPORT INITIALIZE (BIT 7=1) 17 TAPE READ

Fig. 13—Cartridge Tape Transport Controller (CTTC) Command and Reply Format

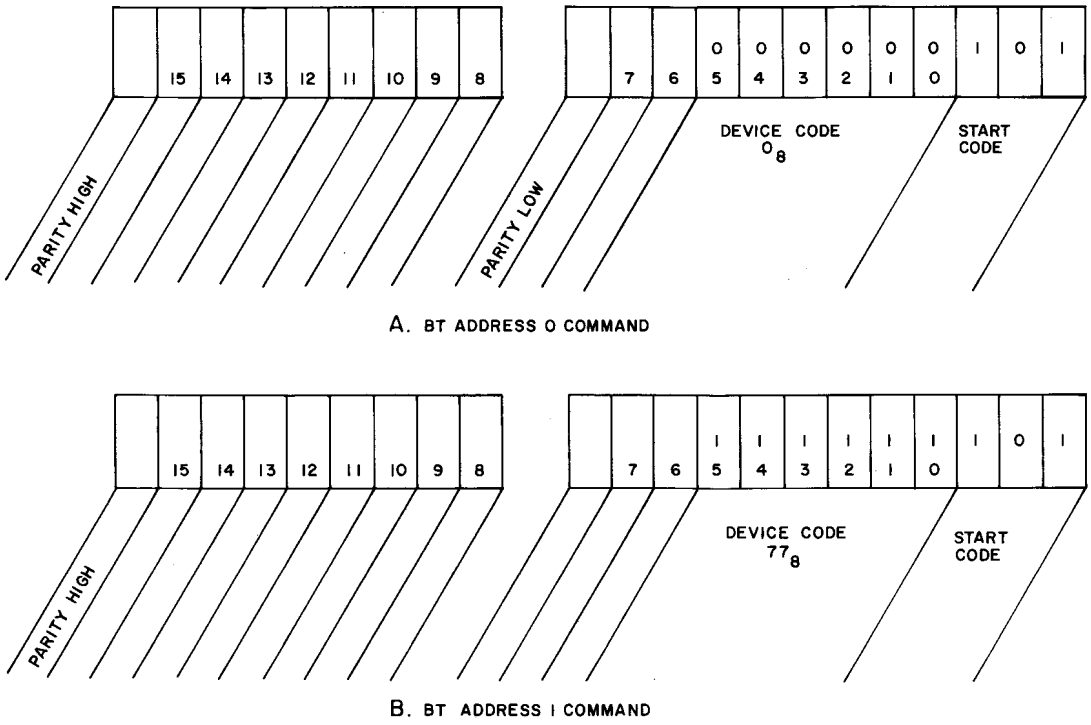
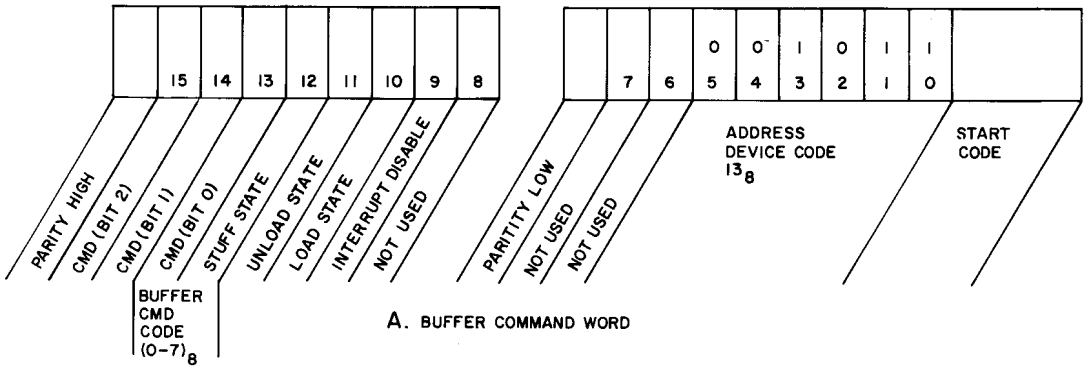
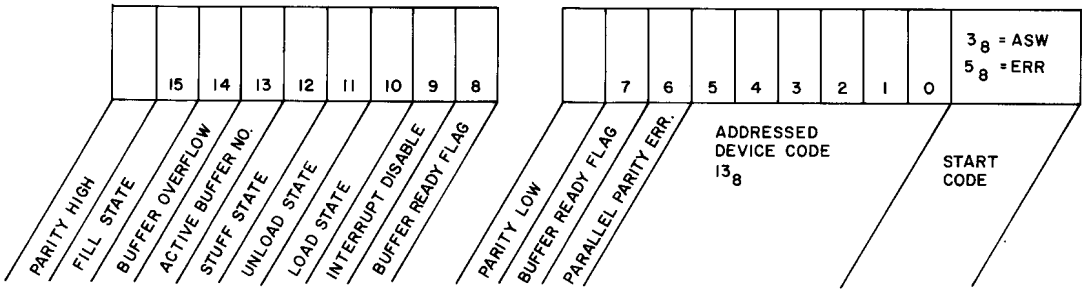


Fig. 14—Bus Terminator (BT) Command Format



A. BUFFER COMMAND WORD



B. BUFFER STATUS REPLY WORD

BUFFER COMMAND CODES (INOCTAL) AND FUNCTION
0 BUFFER STATUS REPLY REQUEST
1 CLEAR BUFFER READY FLAG
2 BUFFER LOAD STATE
3 BUFF FILL
4 NOT USED
5 BUFFER CLEAR THE OFF-LINE COUNTER
6 BUFFER SWITCH BUFFERS
7 BUFFER INITIALIZE

Fig. 15—Buffer Command and Status Reply Format

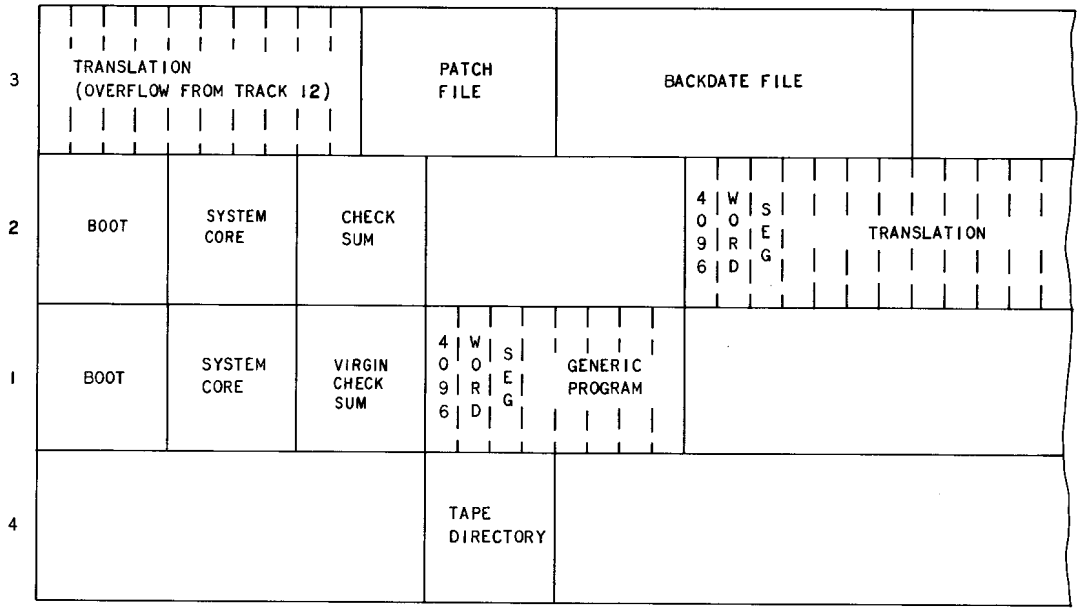


Fig. 16—Tape Format (File Basis)

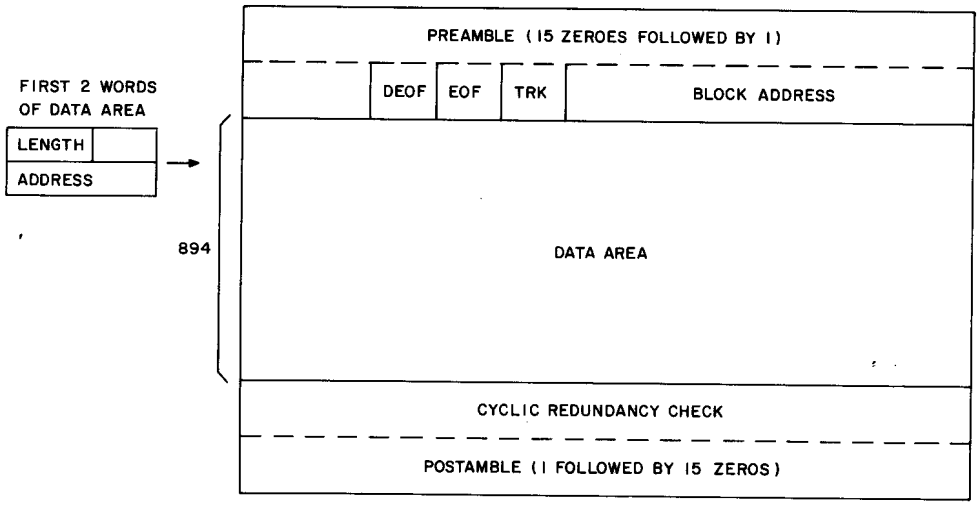


Fig. 17—Tape Block