2B PROCESSOR

FUNCTIONAL DESCRIPTION OF INPUT/OUTPUT CONTROL CIRCUIT

NO. 2B ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 This section provides a physical and functional description of the 2B Input/Output (I/O) control circuit (Fig. 1) of the 2B Processor and its associated interfaces with peripheral equipments.

A functional description of the 2B I/O control circuit is supported by functional block diagrams and schematics. Locational diagrams and various photographs are used to support the physical description.

1.02 Abbreviations and Acronyms—Abbreviations and acronyms are used in the text and associated diagrams to conserve space and prevent long words and phrases. A listing of abbreviations and acronyms is provided in a glossary located at the end of this section.

2. PHYSICAL DESCRIPTION

2.01 The 2B I/O control circuit is located in the processor frame immediately above the 3A CC control panel as shown in Fig. 1. The 2B I/O control circuit consists of 64 circuit packs. Figure 2 shows the physical location of these circuit packs. The implementation of the 2B I/O control circuit required the development of 11 new circuit packs. A description of each unique circuit pack and a statement about the circuitry it contains is provided in Part 5 of this section.

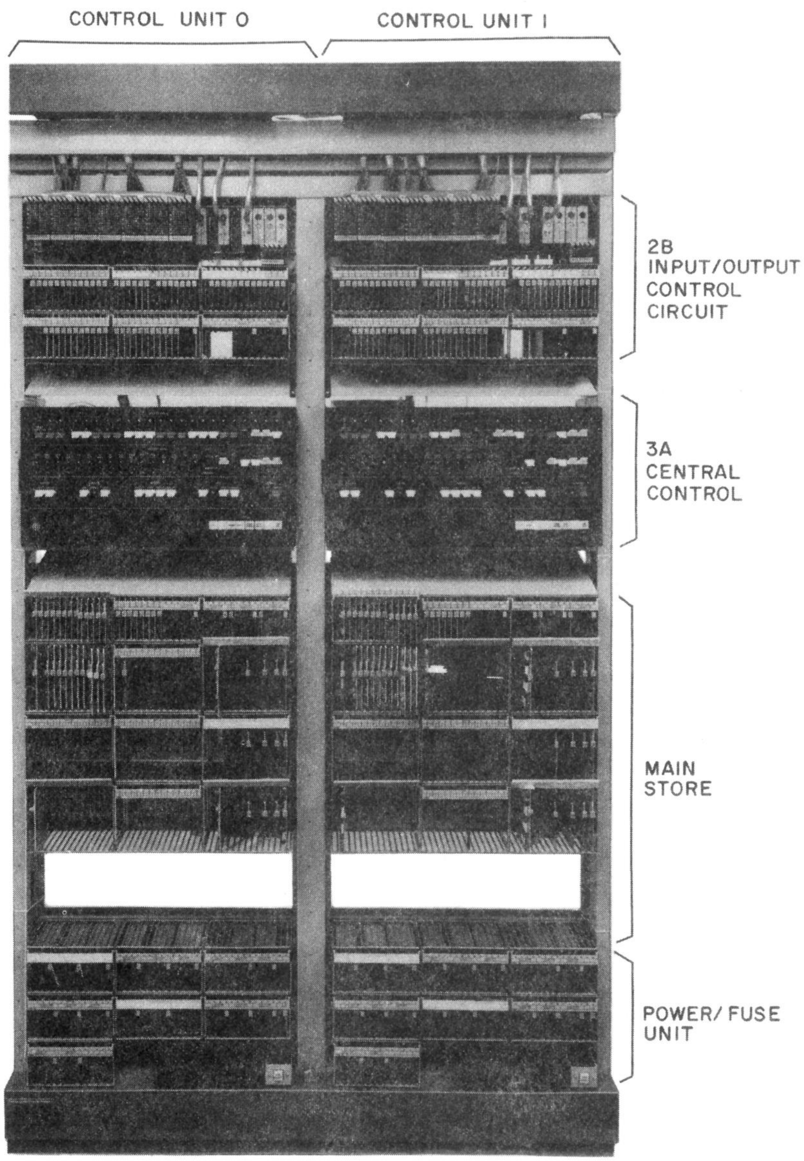


Fig. 1—No. 2B Processor Frame

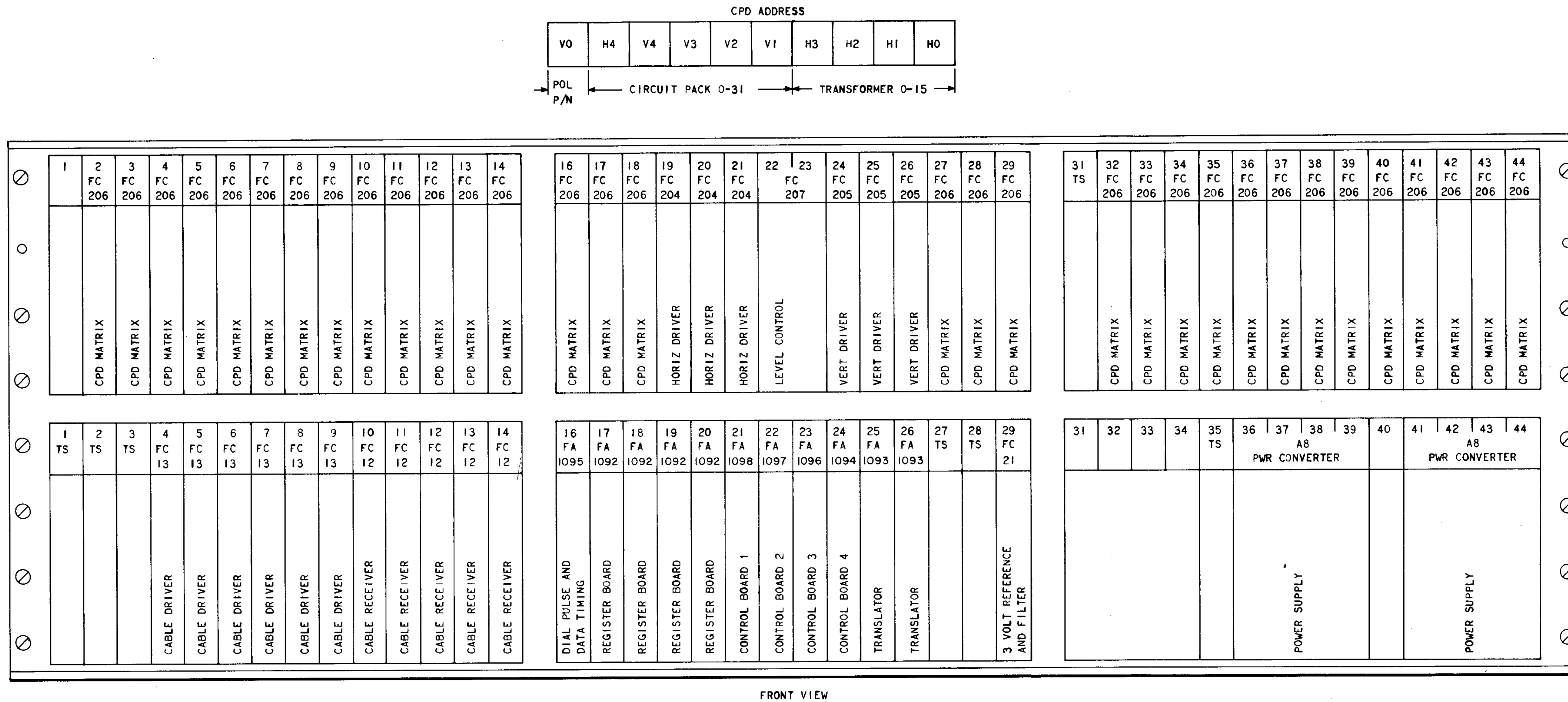


Fig. 2—Circuit Pack Locations

3. FUNCTIONAL DESCRIPTION AND OPERATION

3.01 The 2B input/output (I/O) control circuit (Fig. 3) provides the communication link between the high speed 3A CC processor and the relatively slow speed peripheral equipment. The 2B I/O control circuit is the buffer circuit through which inputs are received into the 3A CC processor and from which outputs are transmitted to the peripheral equipment. No modifications to existing No. 2 ESS peripheral equipment or to the 3A CC are required for them to be compatible with the 2B I/O control circuit.

3.02 ***I/O Communication with Peripheral Units***—The 2B I/O control circuit interfaces with the peripheral units via the central pulse distributor (CPD) outputs, the peripheral unit address (PUA) bus, the scan answer (SA) bus, and the data and dial pulse timing buses.

Central Pulse Distributor (CPD)

3.03 The CPD is used to send control pulses to the peripheral units. There are up to 512 bipolar output points in the 2B I/O control circuit. When more points are needed, supplementary CPD (SCPD) frames can be added. Each supplementary frame contains 512 bipolar SCPD points. CPD and SCPD points are individually connected via private pairs to the points controlled. The CPD is used to perform either enabling or signaling. Many of the peripheral units receive their orders for the 2B I/O control circuit over a common bus system, called as the PUA bus. Enabling pulses from the CPD are used to direct a particular peripheral unit to receive the information appearing on the PUA bus. The enabling signal must be sent to a particular peripheral unit before the data is placed on the PUA bus.

3.04 Signaling and enabling of peripheral units is accomplished by sending bipolar outputs over single output pairs. These bipolar outputs can be used to control remotely located bipolar flip-flops or to load shift register circuits such as the peripheral decoders.

3.05 CPD Matrix—The CPD of the 2B I/O control circuit consists of 512 bipolar points. In an actual office there will be two 3A CCs and two I/O control circuits, and therefore, two matrices of 512 transformers each. A majority of the CPD output points from the two I/O control circuits are multipled (connected in parallel). In the No. 2B ESS, multipling is done at the connectors coming to the terminal strips. Multipling at the connectors reduces the number of points on the terminal strips, but still allows each 2B I/O control circuit to have access to 512 bipolar CPD points. The actual number of output points on the terminal strips for both of the I/O control circuits is 656. There are 368 terminals that are multipled to each I/O control circuit plus 144 terminals on each I/O control circuit that are not multipled for a total of 656.

3.06 CPD Point Selection—A CPD point is selected in two stages using a matrix scheme as illustrated in Fig. 4. Horizontal and vertical translation is performed by 1A-type logic. Each translator selects 1-out-of-32 points by decoding 5 bits in the I/OEA register. The vertical lead is the first to be selected and the last to be turned off. The horizontal lead determines the timing of the CPD pulse and enables the CPD pulse in the timing window created by the vertical pulse.

3.07 Each vertical driver consists of two components, (pull-down and selection) as shown in Fig. 5. One of the 32 vertical pull-down circuits is always disabled, and the remainder enabled. The disabled pull-down is determined by the contents of the I/OEA register. The unselected verticals (pull-down enabled) have a low impedance path to ground which allows shorted semiconductor faults to be detected by an analog check circuit. At the appropriate point in time, (determined by the vertical enable pulse) the selected vertical (VS) lead is activated resulting in a low impedance path to a positive potential supplied by the level control circuitry. The disable vertical pull-down and vertical selection are not performed simultaneously because transistor storage times in the vertical select circuitry could result in overlaps in transistor "on" times, which would appear as a shorted semiconductor fault to the check circuitry.

3.08 A horizontal selection results in a low impedance path to ground with the unselected horizontals having a high impedance path to a positive battery potential. With the horizontal selection made, a current flow path (Fig. 5) is completed through the matrix. In order to avoid ground noise which could affect the 1A logic in the frame, the matrix current flow path does not pass through the frame ground, but instead passes through wiring in the backplane and on the circuit packs which make the CPD point section. Energy for the CPD pulses is supplied by a capacitor on the level control circuit pack, (FC 207), which is filtered from the power supply.

3.09 In addition to determining the selected matrix column, the vertical translation determines which of the two primary windings of the matrix transformer is selected and, thus, the polarity of the pulse. One of the I/OEA register bits at the input of the vertical translator is the CPD address polarity bit. When a local CPD point is being selected EA bit 15 controls parity. In the remote mode (for SCPD frame enable) EA bit 0 controls polarity.

PERIPHERAL UNIT ADDRESS BUS AND REGISTERS

3.10 The peripheral unit address (PUA) bus consists of 38 pairs of balanced ac 100-ohm transmission lines over which the peripheral units receive data from the 3A CC via the I/O control circuit. Each of the 38 PUA bus drivers drive two 100-ohm lines in parallel, one of these lines is designated as the east branch of the PUA bus and the other the west branch (Fig. 6).

3.11 The PUA register is 38 bits wide. Since the 3A CC is basically a 16-bit processor, three registers are needed to buffer the data that is to be put on the PUA bus. These registers are PUA0, PUA1, and PUA2. Register PUA0 buffers bits 0-15, register PUA1 buffers bits 16-31, and register PUA2 buffers bits 32-37 and is a 6-bit register.

3.12 The PUA registers can be loaded from two sources. Like all registers in the I/O control circuit they can be loaded from 3A CC output buffer R10. They can also be loaded from the X and Y 1/8 decoders that decode the bits of R10. Two 1-out-of-8 decoders (X and Y—Fig. 3) are enabled when in either the SCAN or REMOTE mode. The inputs for the X decoder are bits 12-14 of R10 in the REMOTE mode and bits 0-2 of R10 in the SCAN mode. The inputs for the Y decoder are bits 6-8 of R10 in the ***remote*** mode and bits 3-5 of R10 in the SCAN mode. The 1-of-16 decoder RZ (REMOTE Z) is enabled only in the REMOTE mode. The inputs to RZ are bits 9-11 and 15 of R10. When in the External Peripheral Unit Bus Order (XTPUBO) mode, bits 2-5 of R10 are gated through the XTPUBO decoder. These bits emerge from the decoder as bits 32-35 and are gated into bit positions 32-35 of the PUA2 register. Zeros from the XTPUBO decoder are gated into bit positions 36 and 37 of the PUA2 register. To load the PUA registers directly from R10 the I/O control circuit must be in the ***local*** mode. If neither of the inputs to a PUA register is enabled and the control signal that loads the PUA register is activated, all "0s" will be loaded into the PUA1 and PUA2 registers. For example, if control buffer R9, puts the I/O control circuit into the SCAN mode, and bits 0-2 of R9 are "1s", and the miscellaneous decoder control signal LDRI/O (Table A) is activated, all of the PUA registers will be loaded simultaneously. PUA1 and PUA2, bits 16-37, will be loaded with "0s" because no inputs to these bits are enabled. PUA0 bits 0-7 will be loaded with the results of the 1-out-of-8 decoding of bits 0-2 of R10. PUA0 bits 8-15 will be loaded with 0-2 of R10. PUA0 bits 8-15 will be loaded with the 1-out-of-8 decoding of bits 3-5 or R10.

Scanner Answer (SA)

3.13 The SA bus (Fig. 3) consists of 16 pairs of balanced 100-ohm transmission lines. Ferrod row information is transmitted to the scanner answer register via these transmission lines. Two bits of data other than ferrod row information are also transmitted by way of these lines to the I/O error register (I/OER). These bits, all-seems-well (ASW) bit 16, and enable verify (EV) bit 17 are used by the 3A CC to check for the proper execution of peripheral orders. Two scanner answer bus branches designated east and west are "ORed" at the output of their cable receivers (Fig. 7). The use of two scanner answer bus branches makes the layout of the office easier because the SA bus can be more easily routed to the peripheral units and remain within the length requirement for the bus. The SA register is used to buffer data from the SA bus.

3.14 ***Loading the Scanner Answer Register***—The SA register can be loaded from R10 or individual bits set to "1s" directly from the "OR" of the two scanner answer bus branches. The SA register can be cleared (set to all "0s") by a miscellaneous decoder control signal (CLSA.ER). When loading the SA register from R10, the set inputs from the scan answer bus must be disabled so that they do not affect the loading. Disabling of the scan answer set inputs is accomplished by setting bit 7 in the I/OMS register (Table C) to the "1" state.

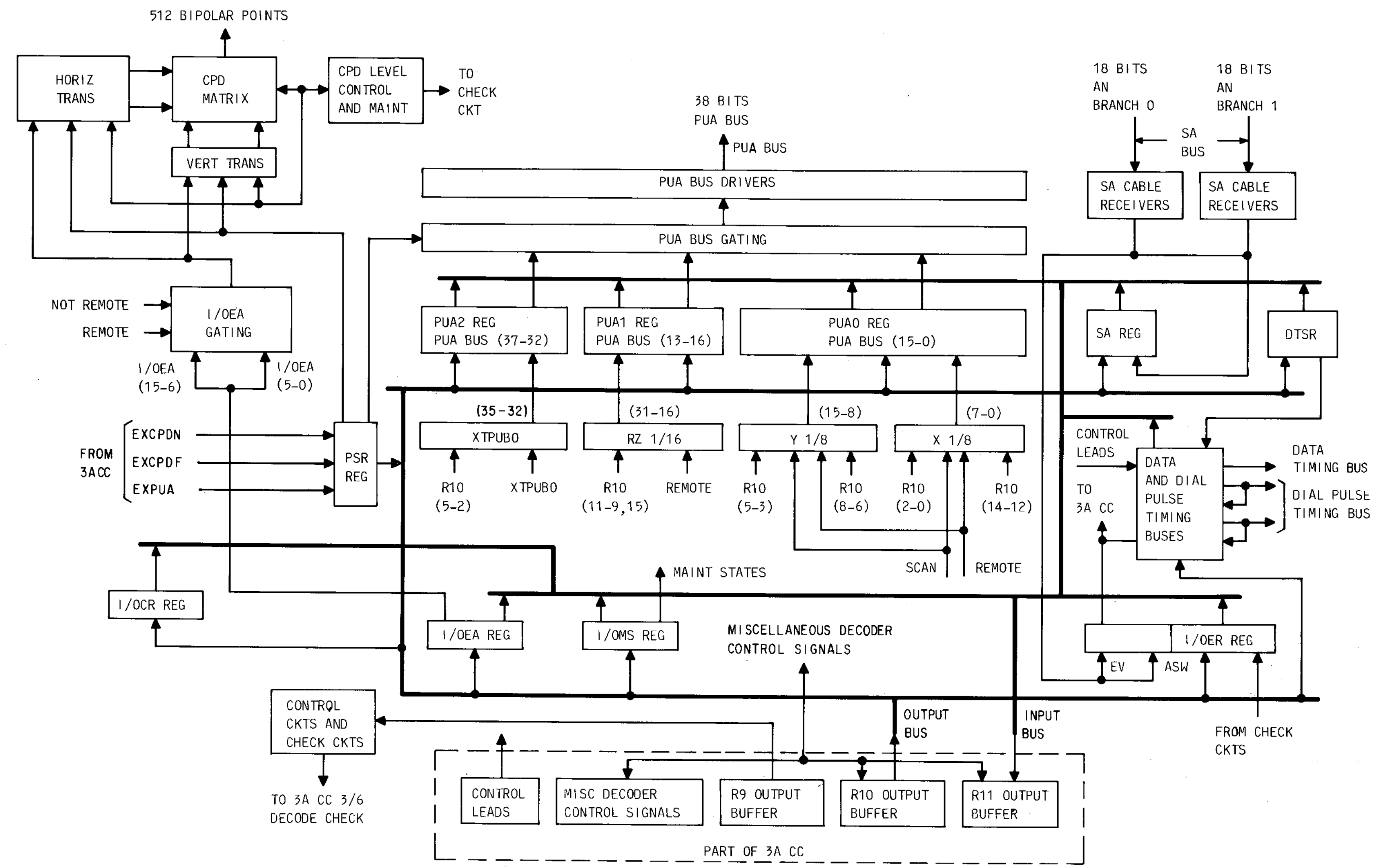


Fig. 3—2B I/O Control Circuit Block Diagram

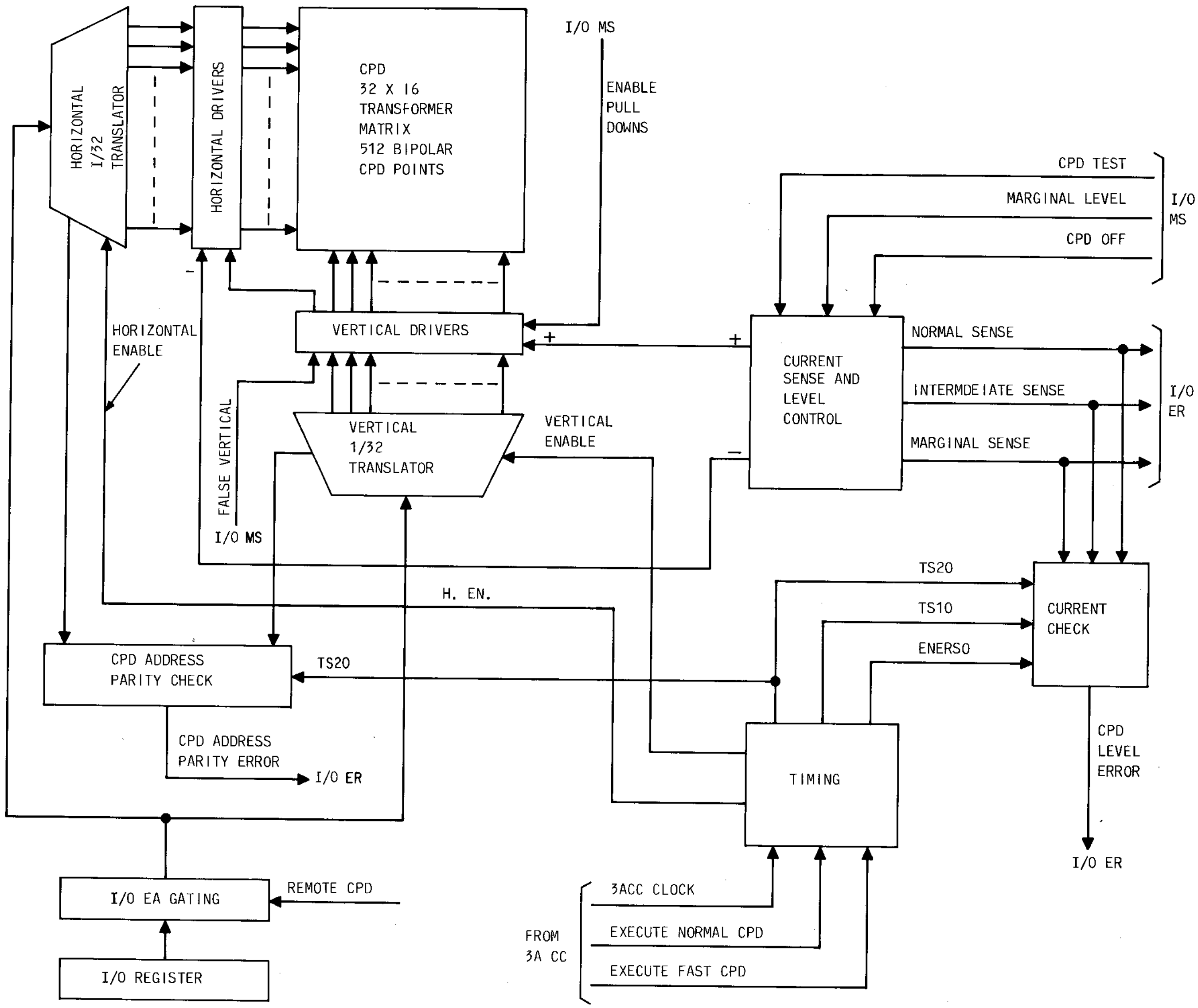


Fig. 4—Central Pulse Distributor

3.15 Pulse Shift Register (PSR)—The PSR (Fig. 3) is a 12-bit shift register which generates the CPD and PUA timing pulses. The PSR is reset to all "Os" after it has generated its required pules. The loading of the PSR is described in 3.20.

3.16 Data Timing Shift Register (DTSR)—The DTSR (Fig. 3) is a 6-bit register which generates dial pulse timing pulses and data timing pulses.

3.17 The dial pulse timing pulses consist of seize (SZ) and release (RL) pulses which are used to set and reset flip-flops of the dial pulse transmitting circuits in the peripheral units. The outputs of these flip-flops are used to generate the dial pulses. The sending rate of the dial pulses is 10 pulses per second. The SZ and RL pulses (Fig. 18) are sent to the dial pulse transmitting circuits via separate wire pairs. These wire pairs comprise the dial pulse timing bus (Fig. 8). The SZ and RL pulses are 600 NS in width. One SZ and one RL pulse is generated every 100 MS (Fig. 18). The time interval between a SZ pulse and the next RL pulse is 40 MS. The time interval between a RL pulse and the next SZ pulse is 60

MS. The timing of the SZ and RL pulses generates a 40-percent make interval and a 60-percent break interval. Two miscellaneous decoder signals from the 3A CC (STSZ and STRL Table A and Fig. 18) are used to generate the SZ and RL pulses.

Dial Timing Bus

3.18 The dial pulse timing bus provides a circuit path for the seize and release pulses to the dial pulse transmitting circuits which are located in the peripheral equipment. The SZ and RL pulses are transmitted to the dial pulse sending circuits via separate wire pairs (Fig. 8). These wire pairs comprise the dial pulse timing bus.

3.19 Gating of Seize and Release Dial Pulse Timing Signals—Under control of the 3A CC, seize and release pulses can be gated onto the dial pulse timing bus (Fig. 3). If a seize pulse (Fig. 18) is to be transmitted, the SZ flip-flop in the I/O CR (bit 11) register must be set to the "1" state prior to the generation of the data timing pulse. Similarly, if the release pulse is to be transmitted, the RL flip-flop in the I/O CR (bit 12) register must be set to the "1" state prior to the generation of the data timing pulse. The SZ and RL flip-flops are set by two miscellaneous decoder control signals (STSZ and STRL Table A). These signals are enabled only when the proper 3-out-of-6 code is loaded into bit positions 10 through 15 of R9 (the control buffer of the 3A CC, Fig. 9). This 3-out-of-6 code is different from that used for all other I/O control circuit functions. The SZ and RL flip-flops are automatically reset to "0" at the end of each data timing pulse.

3.20 Loading the Pulse Shift Register (PRS) and the Dial Pulse and Dial Timing Shift Register (DTSR)—The PSR and the DTSR are loaded from 3A CC register R10 (Fig. 3). To load these registers from R10, their shift leads must be held to "0" or low state and their internal resetting to "0s" at the end of a timing sequence must be blocked. In addition an enable loading I/O MS bit must be set to a "1". The shift lead of the PSR is disabled by bit 1 of the I/O MS register being set to a "1". Bit 11 of the I/O MS register performs the same function for the DTSR. The resetting function of the PSR is blocked by bit 0 of the I/O CR being set to a "1". Bit 13 of the I/O MS register performs the same function for the DTSR. Bit 2 of the I/O MS register being set to a "1" enables the PSR to be loaded from R10. Bit 12 of the I/O MS register being set to a "1" performs the same function for the DTSR.

3.21 The DTSR also generates data timing pulses of 600 NS duration. Every 1.25 MS an interrupt signal from the 3A CC is applied to the DTSR register. This signal enables the shifting of the register every 150 NS. Taps on the register are used to generate the 600 NS data timing pulses. These timing pulses are transmitted to the data timing circuits located in the peripheral equipment via the data timing bus.

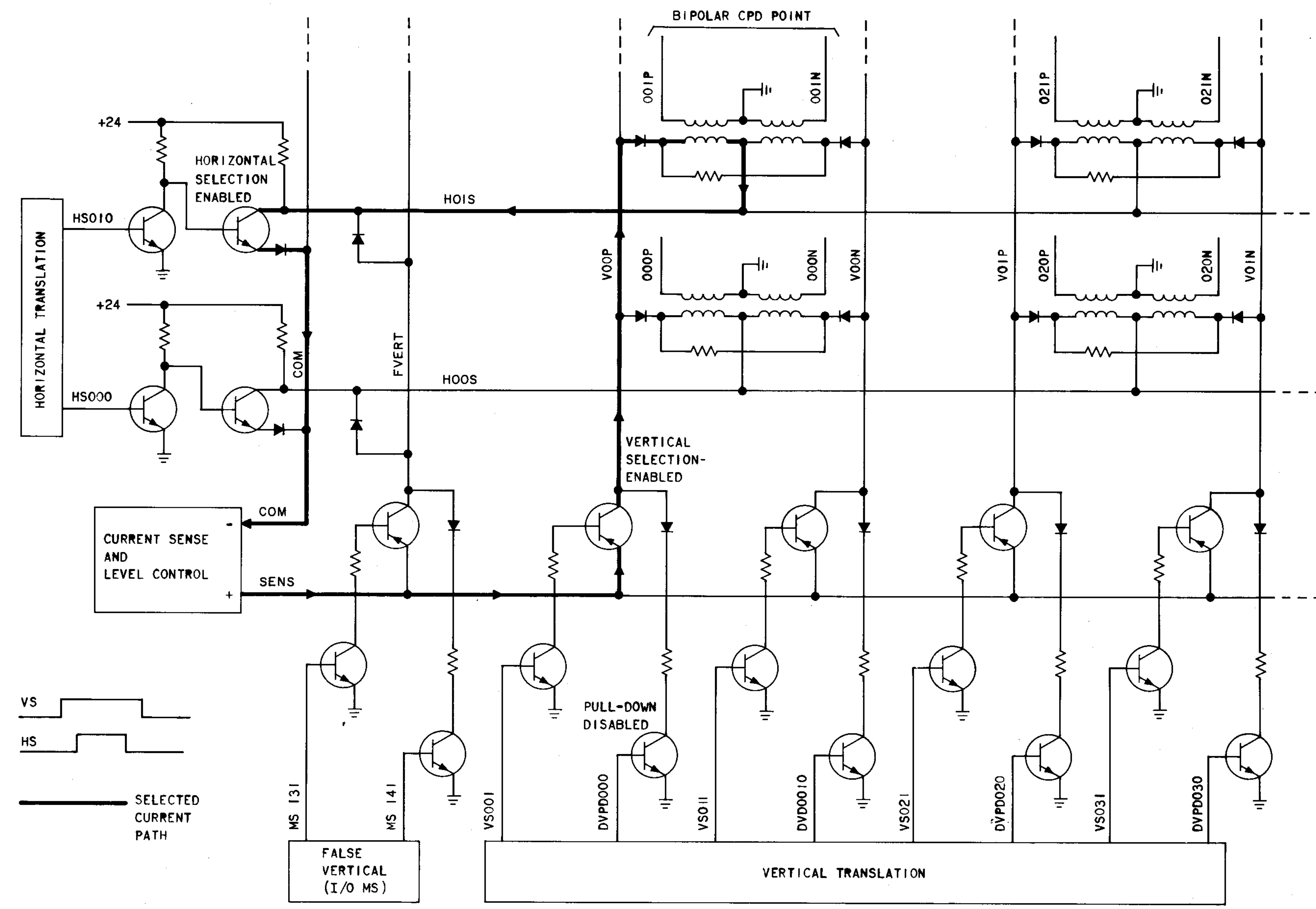


Fig. 5—CPD Matrix

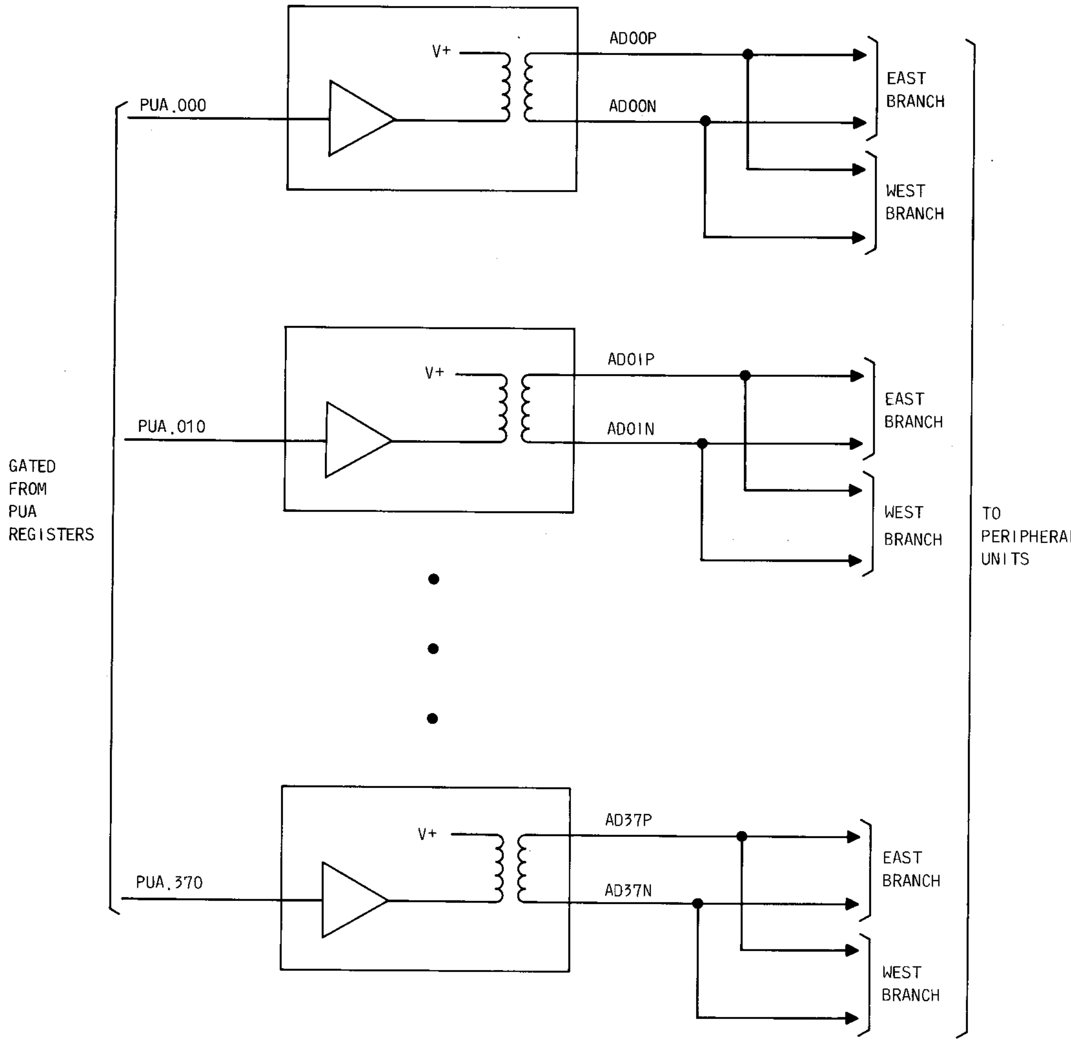
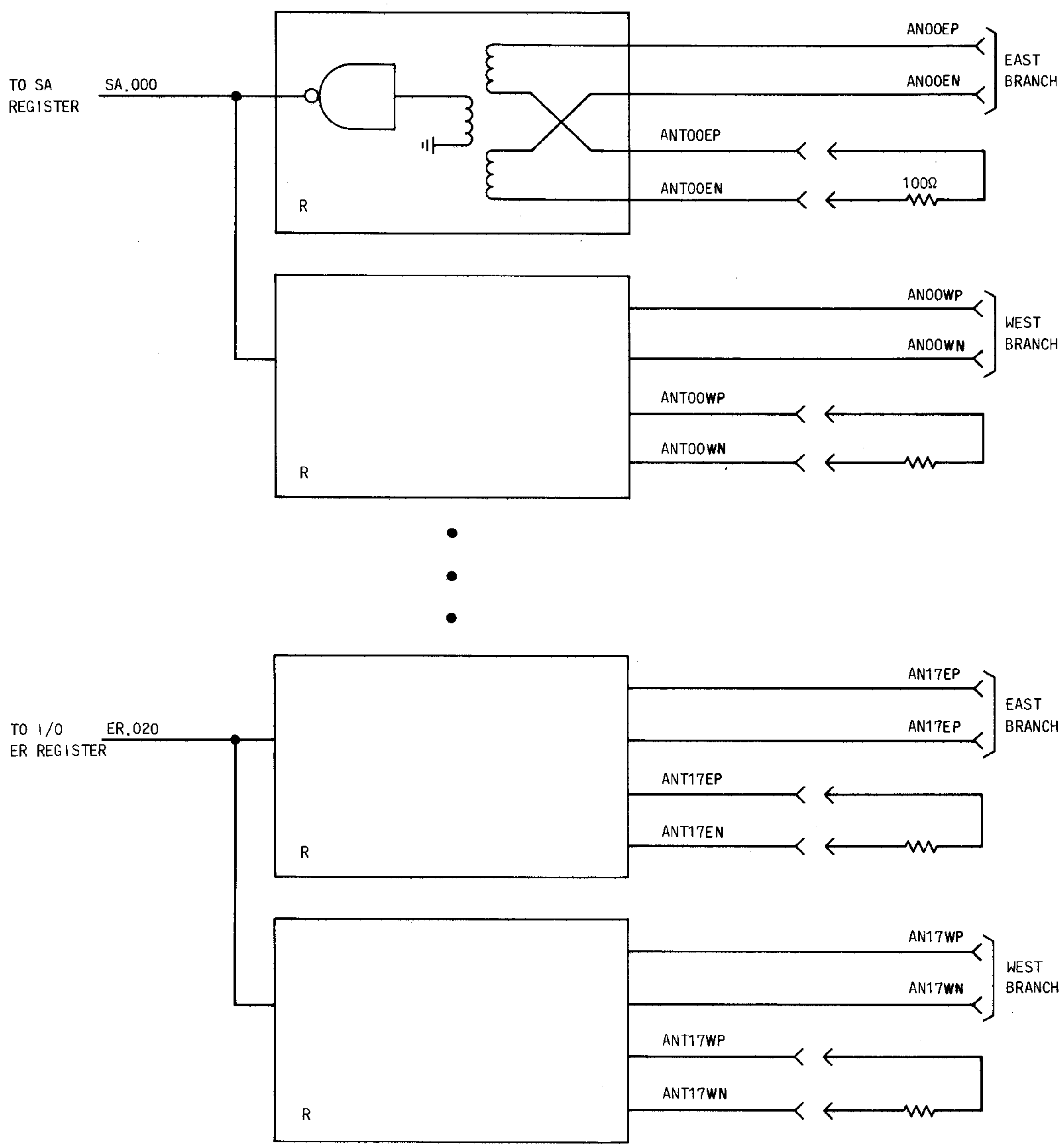


Fig. 6—PUA Bus Drivers



SA REGISTER BIT	BUS BIT	
SA.000	0	FERROD ROW INFORMATION
SA.010	1	
SA.020	2	
•	•	
•	•	
•	•	
SA.140	14	
SA.150	15	
ER.040	16	ALL SEEMS WELL (ASW)
ER.020	17	ENABLE VERIFY (EV)

Fig. 7—Scan Answer Receivers

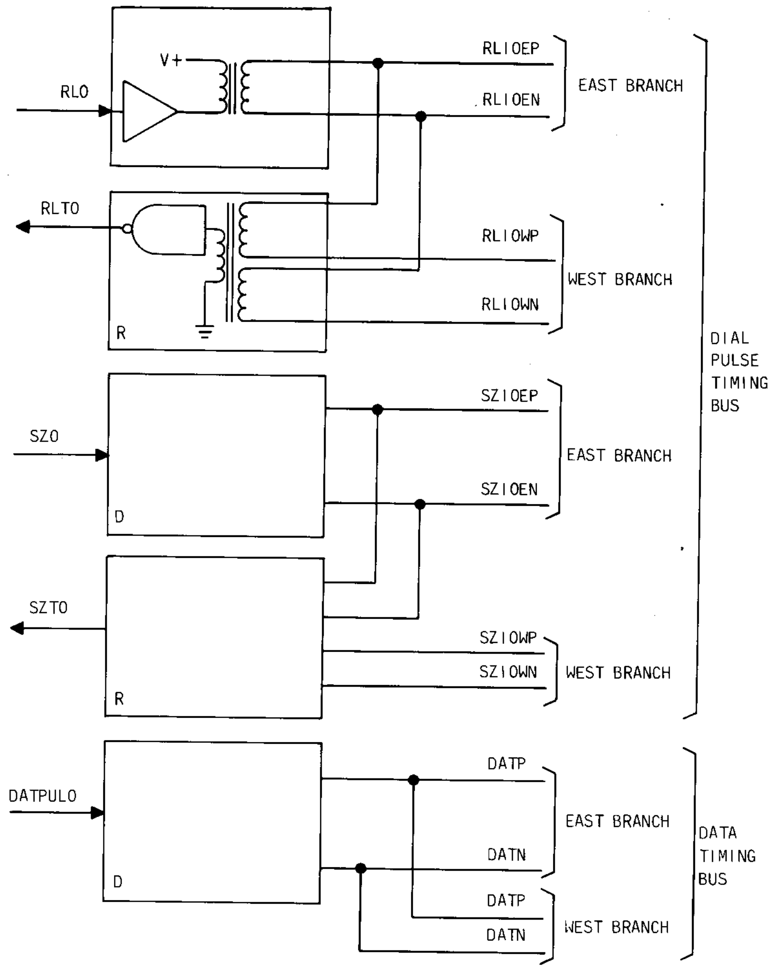


Fig. 8—Dial Pulse and Data Timing Buses

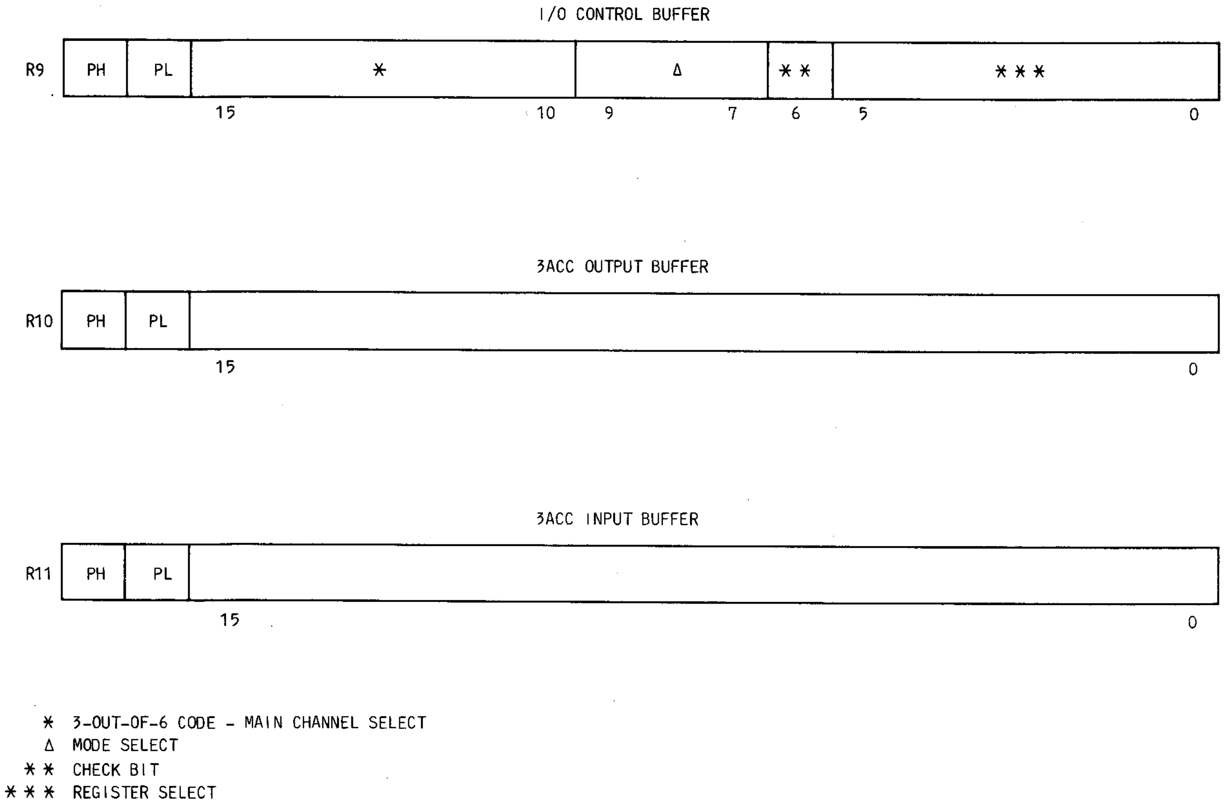


Fig. 9—I/O Register Assignment for I/O Control Circuit

3.22 Communication With the 3A CC—The 3A CC has nine miscellaneous decoder control signals and three general purpose registers (R9, R10, R11) associated with I/O operations. The miscellaneous decoder control signals are generated by the microprogram memory in the 3A CC. These control signals are used in the I/O control circuit to enable gating paths, set or reset registers or initiate the execution of CPD, PUA data timing, and dial pulse timing pulses. Table A lists the functions of each miscellaneous decoder control signal. Figure 9 shows how general purpose registers R9, R10, and R11 of the 3A CC are used.

TABLE A

MISCELLANEOUS DECODER CONTROL SIGNALS

LDRI/O	LoaDs one or more Registers in the I/O.
LDR11	LoaD R11 in the 3A CC with the contents of one of the I/O registers.
EXCPDN	EXecute CPD Normal — Starts the execution of a normal CPD pulse.
EXCPDF	EXecute CPD Fast — Starts the execution of a fast CPD pulse.
EXPUA	EXecute PUA - Gates the contents of the PUA registers onto the PUA bus.
CLSA.ER or STRL	CLears SA register and I/OER or SeTs ReLease flip-flop (bit in I/OCR) depending on the 3-out-of-6 code loaded into bits (15-10) of R9.
STSZ	SeTs SeiZe flip-flop (bit in the I/OCR).
TEST	TESTs the I/O control circuit by loading processor status flip-flops, TR1, TR2, and DS.
SPARE	

3.23 Register R10, the 3A CC output buffer, is used to pass information from the 3A CC to the 2B I/O control circuit. R11, the 3A CC input buffer, is used to receive information from the 2B I/O control circuit. R9, the control buffer, controls the state that the 2B I/O control circuit is in. These three buffers are loaded and read under control of the 3A CC microprogram. Figure 9 provides detailed data on how the three fields of R9 are decoded. Bits 10 through 15 of R9, the control buffer, are encoded in a 3-out-of-6 code. The 20 possible 3-of-6 code combinations comprise what is called a main channel. Two of these 20 codes are used by the 2B I/O control circuit of the No. 2B ESS. One of these codes is used for the generation and testing of the seize and release pulses for the dial pulse timing bus. The other code is used for all other I/O circuit functions. The miscellaneous decoder control signals (Table A) are active in the 2B I/O control circuit only when the proper 3-out-of-6 code is decoded.

3.24 Bits 7 through 9 and a check bit (bit 6) of register R9 are decoded to select one of eight possible modes that the 2B I/O control circuit can be in. Bit 6 is always the complement of bit 7 and is used in a check circuit described in 4.10. The functions of the eight modes are as follows:

(1) SCAN—The 2B I/O control circuit is to execute a scanner order.

(2) REMOTE—The 2B I/O control circuit is to select a remote CPD point (SCPD).

(3) XTPUBO—The 2B I/O control circuit is to execute an external peripheral unit bus order.

(4) LOCAL—The 2B I/O control circuit is to select a local CPD point.

(5) EXLOAD—The EXLOAD mode is used to increase the number of registers that can be loaded under control of R10 from 6 to 12. During the extended load mode, bits 0 through 5 of control buffer R9 define six registers in the 2B I/O control circuit that can be loaded either with the contents of buffer R10 or from other sources. Each bit defines a specific register.

(6) READ—During the read mode bits 0 through 5 of buffer R9 define six registers in the I/O control circuit whose contents can be read into input buffer R11. Each bit defines a specific register.

(7) EXREAD—The extended read mode is used to increase the number of registers from 6 to 12 in the 2B I/O control circuit whose contents can be transferred into buffer R11. Only four of the possible six EXREAD bits are being used. can be transferred into buffer R11.

(8) TEST—The test mode is used to check a portion of a check circuit.

The normal modes of operation are SCAN, REMOTE, XTPUBO, and LOCAL. The other four modes (EXLOAD, READ, EXREAD and TEST), are used for maintenance purposes.

3.25 ***Loading and Reading 2B I/O Control Circuit Register***—For maintenance purposes, any register in the 2B I/O control circuit can be loaded from output buffer (R10) in the 3A CC and may be read into input buffer (R11). The control buffer (R9) controls the loading and reading of the registers. Control buffer R9 has the capability to control up to 12 registers. Table B lists these registers. The functions of these registers are described in 3.10 thru 3.21 and 3.29 through 3.34.

TABLE B

I/O CONTROL CIRCUIT REGISTERS

PUA0	Peripheral Unit Address register 0 (PUA bits 15—0)
PUA1	Peripheral Unit Address register 1 (PUA bits 31—16)
PUA2	Peripheral Unit Address register 2 (PUA bits 37—32)
I/OEA	Input/Output Enable Address register
I/OMS	Input/Output Maintenance State register
I/OER	Input/Output Error Register
I/OCR	Input/Output Control Register
PSR	Pulse Shift Register
SA	Scanner Answer register
DTSR	Dial Pulse and Data Timing Shift Register

3.26 To load input buffer R11 from a register in the 2B I/O control circuit, the contents of the I/O control circuit register must be gated onto the input bus of buffer R11 (Fig. 3). The register containing data to be gated into R11 is selected by R9. The 3A CC then activates the miscellaneous decoder control signal (LDR11) which enables R11 to receive the contents of the input bus. Registers in the I/O control circuit that are less than 16 bits in length gate zeros into the unused bit positions of R11. The contents of more than one register at a time may be gated onto the input bus of R11. When this happens R11 will be loaded with the "OR" of the data of more than one register. Similarly, more than one register can be loaded at a time from R10 (a hardware limitation limits the number to four). The registers that will be loaded depends on the inputs to the registers being enabled when the Miscellaneous Decoder Control signal LDRI/O is activated. Miscellaneous Decoder Control signal LDRI/O gates data from R10 onto the output bus. The registers that this data is loaded into are selected by R9. When loading a register from R10, other inputs to the register must be disabled to prevent other data from being loaded on top of the R10 data. The disabling of these inputs is described in the sections on the individual registers.

3.27 On-Line/Off-Line Control—The 3A CC processor controls whether or not the 2B I/O control circuit is on-line or off-line. The 3A CC can force the 2B I/O control circuit off-line when either the DISI/O (disable input/output) or the LOL (lock-off-line) signals are activated. These signals are generated by circuits of the 3A CC. Whenever either the DISI/O or the LOL signals are present the 2B I/O control circuit cannot generate central pulse distributor (CPD), peripheral unit address (PUA), data timing, or dial pulse timing pulses. The 2B I/O control circuit may also be switched off-line by setting the ***stop*** flip-flop in the 3A CC to the "1" state or by setting the ***central control*** flip-flop in the 3A CC "0" state. The output of these flip-flops resets the ***run*** flip-flop of the 2B I/O control register and thus places the unit off-line.

3.28 I/O Control Circuit Status Bits—Three conditional flip-flops in the 3A CC (TR1, TR2, and DS) are used to monitor the status of the I/O control circuit. The flip-flops are loaded with the status of the I/O central circuit whenever the test miscellaneous decoder control signal is activated. The status flip-flops are loaded with a combination of information from the I/O error (I/OER) register. The error bit (EROR) of the I/OER indicates that an error has been detected by the error checking circuits of the I/O control circuit. The enable verify (ER), and the all-seems-well (ASW) bits are returned to the I/OER by peripheral circuits to indicate the status of orders sent from the I/O circuit. These three bits are combined to produce the following status signals to the 3A CC:

Error to test register 1 (TR1) = EROR

Error to test register 2 (TR2) = EROR + EV

Error to data status register (DS) = EROR + EV +ASW

When the I/O circuit is placed in the dial pulse main channel mode (one of the two main channels used for the I/O control circuit) the DS bit is used to monitor the status of the dial pulses being sent to peripheral units. When in this mode the EROR, EV, and ASW bits are disabled.

3.29 ***Input/Output Enable Address (I/OEA) Register***—The I/OEA register (Fig. 4) is used to store CPD address information. The I/OEA register can be loaded only from R10 and is the only register in the I/O control circuit that contains 16-data bits and two parity bits. The parity bits are used in the error check circuits which are described in 4.06. The CPD address information stored in the I/O EA is divided into two fields. Bits 6-15 contain address information that is used for the selection of a CPD output in the local CPD matrix. Two of bits 0-5 contain address information that is used to select a CPD output that enables a supplementary CPD (SCPD1) frame when the I/O circuit is in the remote mode. The two bits used for the SCPD frame enable are not sufficient for a complete CPD point selection; 10 bits are needed for a full selection. Since only a limited number of CPD outputs are needed to select a SCPD frame, four of the CPD address bits are jammed to a constant when the I/O circuit is in the remote mode. Figure 10 shows the arrangement of the EA used for remote and local CPD addressing. The HO through H4 and V0 through V4 designations assigned to bits designate the two fields of five bits used to generate the two 1-of-32 selection. These selections made by the horizontal and vertical translators select the CPD output and polarity of the output pulse (horizontal and vertical selections). (Fig. 10.)

CPD ADDRESS BIT	9	8	7	6	5	4	3	2	1	0
	V0 *	H4	V4	V3	V2	V1	H3	H2	H1	H0

	WHEN NOT IN REMØTE MODE	WHEN IN REMØTE MODE
H0	= I/ØEA6	I/ØEA1
H1	= I/ØEA7	I/ØEA2
H2	= I/ØEA8	I/ØEA3
H3	= I/ØEA9	I/ØEA4
V1	= I/ØEA10	I/ØEA5
V2	= I/ØEA11	1
V3	= I/ØEA12	1
V4	= I/ØEA13	0
H4	= I/ØEA14	1
V0(POLARITY)	= I/ØEA15	I/ØEA0

* 0 PRODUCES A POSITIVE PULSE
  1 PRODUCES A NEGATIVE PULSE

Fig. 10—CPD Address Format

3.30 ***Input/Output Maintenance State (I/OMS) Register***—The outputs from the I/OMS register are used as control signals to put the I/O control circuit into different maintenance states. The maintenance states include states for enabling test circuits, and for enabling and disabling various registers or register inputs. The I/OMS register can be loaded only from R10. Table C lists the function of each I/OMS bit.

TABLE C

I/OMS BIT ASSIGNMENT

Bit 0 (DEXPUA — Disable) EXecuting PUA pulses)	When in the "1" state, information cannot be gated onto the PUA
Bit 1 (DISSFT — DISable ShiFT)	When in the "1" state, shift pulses to he PSR shift register are blocked. A shift pulse to the PSR shift register is generated if bit 1 goes from a "1" state to a "0" state, and both the ENSH and the SHT bits of the I/OCR are in the "1" state.
Bit 2 (ENLR10 — ENable Loading from R10)	When in the "1" state, the shift register that generates CPD and PUA pulses (PSR) can be loaded from R10; resetting bits CPDN and CPDF of the I/OCR from bits in the PSR is blocked. When in the "0" state, the shift register will be reset to all zeros if the load PSR control lead is activated.
Bit 3 (DISSHC — DISable SHift Control)	When in the "1" state, the set and reset inputs from clock phases P0 and P2 to the SHT bit of the I/OCR are disabled and SHT can be loaded from R10.
Bit 4 (DISPUL — DISable PULse)	The states of DISPUL and the RUN bit of the I/OCR determine whether or not CPD and PUA pulses can be generated.

DISPUL STATE	RUN STATE	PULSES
0	0	disabled
1	0	enabled
0	1	enabled
1	1	disabled

Bit 5 (MCPDL — Marginal CPD Level)	When in the "1" state, the output of the CPD amplitude control circuit is in the MARGINAL state which causes any CPD pulses sent to be at a marginal current level.
Bit 6 (OFFCPDL — OFF CPD Level)	When in the "1" state, the output of the CPD amplitude control circuit is in the OFF state which disables the sending of CPD-pulses.
Bit 7 (DISSA — DISable Scanner Answer)	When in the "1" state, the SA register can only be loaded from R10 or reset to all "Os" by CLSA.ER.
and	
(DTS2ER — Disable TS2 and Current Level ERror)	Also, when in the "1" state, the current level bits in the I/O Error register are set during TS1 instead of TS2. The current level error bit input (I/OER Bit 5) is also disabled.
Bit 8 (DISER — DISable Error Register)	When in the "1" state, the I/OER can only be loaded from R10 or reset to all "Os" by CLSA.ER.

TABLE C (Cont)

I/OMS BIT ASSIGNMENT

Bit 9 (DISTMB — DISable TiMing Buses)	The states of DISTMB and the RUN bit 9 of the I/OCR determine whether or not the data timing bus and the dial pulse timing bus are active.

DISTMB STATE	RUN STATE	BUSES
0	0	disabled
1	0	enabled
0	1	enabled
1	1	disabled

Bit 10 (DISBUS — DISable BUSes) and	When in the "1" state, both the data timing bus and the dial pulse timing bus are inactive; resetting of the RUN bit of the I/OCR from the 3A CC is blocked. This maintenance state overrides the DISTMB maintenance state
(TCCPD — Test Current for the CPD)	Also, it provides test current (25 mA) which should produce a current level error when this bit is set to a "1".
Bit 11 (DSDTSH — DiSable Data Timing SHift pulses)	When in the "1" state, the shift pulses to the shift register that generates data and dial pulse timing pulses (DTSR) are blocked. A shift pulse to the data and dial pulse timing shift register is generated if bit 11 goes from a "1" state to a "0" state and both the DISDTC bit of the I/OMS register and the SHFT bit (bit 13) of the I/OCR are in the "1" state.
Bit 12 (ER10SR — Enabling Loading R10 into Shift Register) and	When in the "1" state, the shift register that generates data and dial pulse timing pulses (DTSR) can be loaded from R10. When in the "0" state, the shift register will be reset to all "0s" if the load DTSR control lead is activated.
(AVPA — All Vertical Pull-downs Activated)	Also, when set in the "1" state, all the vertical pull-down transistors are activated.
Bit 13 (DISDTC — DISable Data Timing Control) and	When in the "1" state, data and dial pulse timing pulses are disabled; the set and reset inputs to the SHFT bit in I/OCR from clock phases PO and P2 (Table A) are disabled (SHFT can be now loaded from R10); the internal clear of the data and dial pulse timing shift register is disabled; DSDTSH can be used as a shift pulse.
(MVCPD — Maintenance Vertical of CPD Selected)	Also, when set in the "1" state, the maintenance (false) vertical for horizontal selection testing is activated.

TABLE C (Cont)

I/OMS BIT ASSIGNMENT

Bit 14 (MVPCPD—Maintenance Vertical Pull-down of CPD Activated)	When in the "1" state, the false vertical pull-down transistor is activated while the other pull-down transistors are off.
Bit 15	Spare

3.31 ***Input/Output Error Register (I/OER)***—The I/OER is used to buffer both the enable verify (EV) and the all-seems-well (ASW) bits from the scanner answer bus and the results of the error check circuits. Table D lists the functions of each I/OER bit.

TABLE D

I/OER BIT ASSIGNMENT

Bit 0 (ERROR — ERror OR	Set the "1" state if any check circuit detected an error.
Bit 1 (ERMODED — ERror MODE Decode)	Set to the "1" state if the mode selection check circuit detected a mode decode error.
*Bit 2 (EV — Enable Verify)	Set to the "1" state by the return of the EV bit of the scanner answer.
Bit 3 (ERREGD — ERror REGister Decode)	Set to the "1" state if the register decode check circuit detected an error.
*Bit 4 (ASW — All-Seems-Well)	Set to the "1" state by the return of the ASW bit of the scanner answer.
Bit 5 (ERCPDL — ERror CPD Level)	Set to the "1" state if a CPD level error is detected.
Bit 6 (ERCPDA — ERror CPD Access)	Set to the "1" state if the CPD access check circuit or the loading I/OEA check circuit detected an error.
*Bit 7 (OCPDAP — Odd CPD Address Parity)	Set to the "1" state by the odd CPD address parity bus.
*Bit 8 (ECPDAP — Even CPD Address Parity)	Set to the "1" state by the even CPD address parity bus.
*Bit 9 (CPDMC — CPD Marginal Current)	When set to the "1" state, the CPD output current is above the marginal current level.
*Bit 10 (CPDIC — CPD Intermediate Current)	When set to the "1" state, the CPD output current is above the intermediate current level.
*Bit 11 (CPDNC — CPD Normal Current)	When set to the "1" state, the CPD output current is above the normal current level.
Bits 12 through 15	Spares

*These bits provide information storage and buffering and do not directly indicate errors.

3.32 The I/OER can be loaded from R10 or individual bits may be set from either the check error circuits or the EV and ASW bits from the scanner answer bus. When loading the I/OER from R10, the inputs from the check circuits and the scanner answer bus must be disabled. This is accomplished by setting bit 8 (DISER) of the I/OMS register to the "1" state. The I/OER can be cleared by the miscellaneous decoder control signal CLSA.ER.

3.33 ***Input/Output Control register (I/OCR)***—The I/OCR (Table E) consists of a 6-bit field (bits 0-5) and a 5-bit field (bits 9-13). The bits in the 6-bit field are used to control the generation of CPD and PUA pulses. Four bits, (bits 10-13) from the 5-bit field are used to control the generation of data and dial pulse timing pulses. Bit 9 is the RUN flip-flop. This flip-flop controls whether or not the 2B I/O control circuit is on-line. If the I/OCR is to be loaded from R10, all inputs from other registers must be disabled. These registers are disabled by setting them into the required state at their input source or disabling them with maintenance states.

TABLE E

I/OCR BIT ASSIGNMENT

Bit 0 (ENSH — ENable SHift)	This bit enables the shift pulses to the PSR when a CPDN, CPDF or PUA pulse is to be generated.
Bit 1 (SHT — SHifT)	This bit generates the shift pulses for the PSR using system clock phases P0 and P2.
Bit 2 (PUA — execute PUA)	This bit is set by the EXPUA miscellaneous decodes control signal. It enables the generation of a PUA timing pulse.
Bit 3 (CPDF — execute CPD Fast)	This bit is set by the EXCPDF miscellaneous decoder control signal. It enables the generation of the fast CPD pulse.
Bit 4 (CPDN — execute CPD Normal)	This bit is set by the EXCPDN miscellaneous decoder control signal. It enables the generation of a normal width CPD pulse.
Bit 5 (VS — Vertical Select)	This is a timing bit which gates the vertical selection in CPD selection.
Bit 6 — not used	
Bit 7 — not used	
Bit 8 — not used	
Bit 9 (RUN — RUN)	This bit controls the on-line, off-line status of the I/O circuit.
Bit 10 (DPT — Dial Pulse Test)	This bit receives the SZ and RL pulses from the dial pulse timing bus and monitors the status of the dial pulses being generated.
Bit 11 (SZ — SeiZe)	This bit is set by the STSZ miscellaneous decoder control signal. It enables the gating of a seize pulse to the dial pulse timing bus.
Bit 12 (RL — ReLease)	This bit is set by the STRL miscellaneous decoder control signal. It enables the gating of a release pulse to the dial pulse timing bus.
Bit 13 (SHFT — SHiFT)	This bit is used to generate the shift pulses for the DTSR using system clock phases P0 and P2.
Bit 14 — not used	
Bit 15 — not used	
Bit 16 — not used	

3.34 ***CPD Level Control Circuit***—The voltage level used for generating the CPD pulses is controlled by the CPD level control circuit. The current through the CPD matrix is also monitored by this circuit. A simplified diagram of this circuit is shown on Fig. 11. The CPD level control circuit has four modes or states of operation. These states are the ***normal, marginal, intermediate,*** and ***off.*** Three of these operational states, (***marginal, intermediate,*** and ***off***) are used for maintenance testing.

- The normal state results automatically from not being in any one of the other states. When in the normal state current is provided to the CPD matrix to generate normal level CPD pulses.
- The marginal (MARG 1) state is used to insure the insensitivity of the cable receivers to noise and crosstalk.
- The intermediate (TEST 1) state is used to check the sensing circuitry.
- The off state inhibits current flow to the level control circuit. In this state the current applied to the CPD matrix is turned off.

3.35 Voltage to CPD matrix via the ***sens*** lead is controlled by zener diode D1 and emitter follower transistor Q3. The current for CPD pulses is supplied by the charge on capacitor C2 and is monitored by sensing the voltage across resistor R3. Integrated circuit A1 is an operational amplifier which amplifies the voltage detected across resistor R3 and supplies this voltage to A2, A3, and A4. These integrated circuits are differential comparators. Each of these comparators senses when the matrix current exceeds a specific level. Comparator A2 provides an output when it detects current flowing in the matrix equivalent to a normal level CPD pulse. Comparator A3 monitors for intermediate level current and A4 for marginal level current.

3.36 ***Output Timing Pulses***—The pulse shift register (PSR) receives clock pulses from the 3A CC and converts these clock pulses into timing pulses (Fig. 12) for the I/O control circuits. The loading of the PSR is described in 3.20. The timing pulses generated by the timing circuit are as follows:

(1) ***Vertical select***—The vertical select pulse enables the vertical translator to select 1 of 32 CPD transformers out of 512, and to select the polarity of the output pulse.

(2) CPDN or CPDF (horizontal enable)—The CPDN or CPDF pulses enable the horizontal translator to select 1 of the 32 transformers selected by the vertical select. The time duration of this pulse determines the time duration of the CPD pulse, (450 NS for CPDN, and 300 NS for CPDF).

(3) ***TS10*** (test strobe 1), ***TS20*** (test strobe 2), and ***ENERSO*** (enable error strobe) Fig. 4 and 12—These timing pulses are used to enable test for shorts and opens in the CPD transformer matrix as well as to test the CPD address parity and gate the results into the error register.

(4) ***PUA*** (peripheral unit address)—This pulse causes the 38 bits contained in the PUA registers to be gated onto the PUA bus. This gating determines the width of the PUA pulse, normally 450 NS.

3.37 The CPDN, CPDF, and PUA timing pulses are executed under control of the 3A CC. The control pulses that initiate these timing pulses are the miscellaneous decoder control signals EXCPDN, EXCPDF, and EXPUA (see Table A and Fig. 3).

3.38 The EXCPDN pulse sets bit 4 of the I/O control register, (Table E), which enables the PSR and the pulse generation circuits to produce a normal width CPD pulse. The timing signals generated are the vertical select, CPDN (horizontal enable), TS10, TS20, and ENERSO (Fig. 12).

3.39 The EXCPDF pulse sets bit 3 of the I/OCR, (Table E), which enables the PSR and the pulse generation circuitry to produce a fast CPD pulse. The timing signals generated for the fast pulse are the vertical select and the CPDF (horizontal enable). No error test strobes are generated for the fast CPD pulse.

3.40 The EXPUA pulse sets bit 2 of the I/OCR, (Table E), which enables the PSR and pulse generation circuits to produce a PUA pulse. The time duration of the PUA pulse is 450 NS.

3.41 Figure 12 shows the relative timing of the pulse outputs from the timing circuit and the timing pulses from the 3A CC when executing

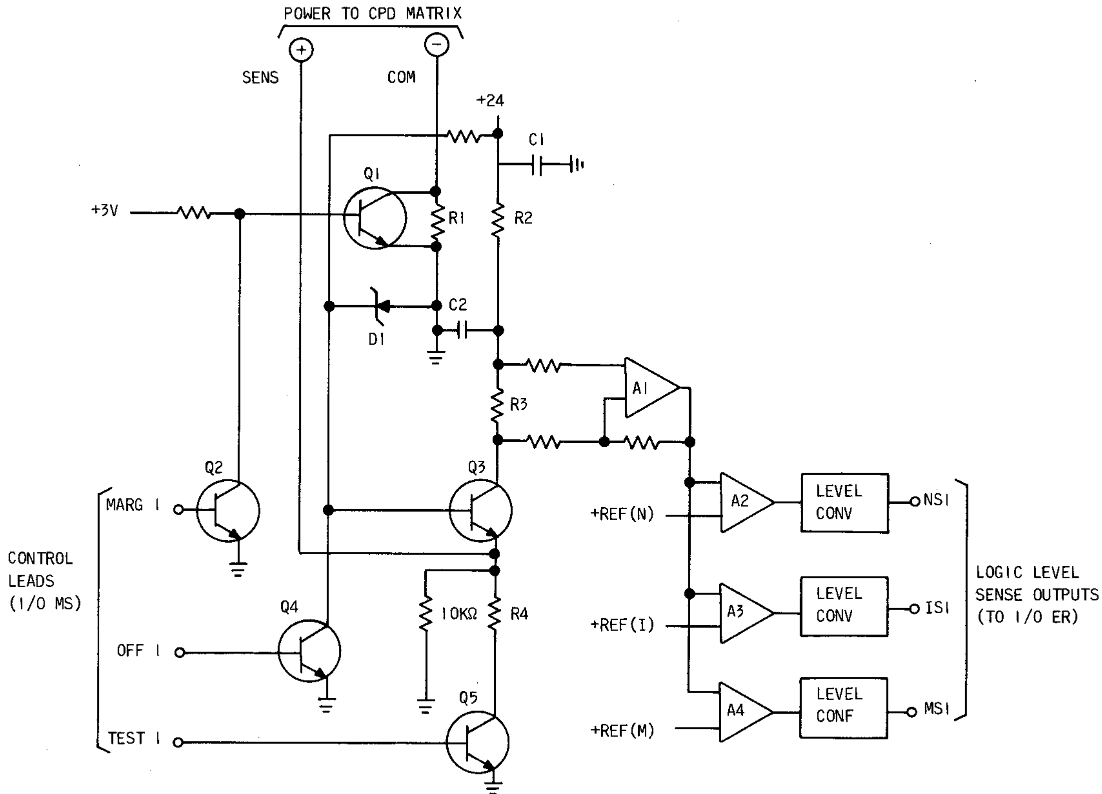


Fig. 11—Level Control Circuit

a typical peripheral unit order. The EXCPDN and the EXPUA pulses are generated by the 3A CC. The VERTICAL SELECT, CPDN TS1O, TS2O, ENERSO, and the PUA pulses are generated by the pulse shift register. The first pulse required to execute a typical peripheral unit order is EXCPDN. The EXCPDN pulse enables the pulse shift register (PSR) to start generating timing signals beginning with the next 3A CC clock cycle. The first signal generated by the PSR is the VERTICAL SELECT. The VERTICAL SELECT pulse enables the vertical translator to select 1 of 32 CPD transformers and the polarity of the CPD output. The next pulse generated is TS10 followed by CPDN, TS2O, and ENERSO. The TS1O, TS2O, and ENERSO are used to test for CPD address parity and for shorts or opens in the CPD transformer matrix. The CPDN pulse enables the horizontal translator to select 1 of the 32 transformers selected by the vertical select, and gate the CPD pulse from that transformer. The next pulse, EXPUA, causes the PSR to generate a PUA pulse which causes the data that has been loaded in the PUA registers to be gated onto the PUA bus. The EXPUA pulse is not generated until 1.95 USEC after the beginning of the EXCPDN pulse. The reason for this is that the same shift register that generates the CPD pulse also generates the PUA pulse, therefore it must be reset before it can generate the PUA pulse. Once the PUA pulse has been sent to a peripheral unit, the 3A CC must wait for a scan answer (SA) reply. The SA reply is received via the SA cable receivers and loaded into the SA registers. This scan answer data is gated into input buffer R11 of the 3A CC. The 3A CC checks the scan answer data for errors. Providing no errors are found, another peripheral unit order can be executed. For this particular order sequence a peripheral unit order can be executed every 7.35 μs. Whenever the 3A CC sends the execute CPD fast (EXCPDF) pulses to the I/O control timing circuits, a peripheral unit order can be executed every 3.9 μs. When the EXCPDF order is received, the pulse shift register will not generate the test strobe pulses TS1O, TS2O, and ENERSO.

3.42 Typical 2B I/O Control Circuit Orders to Peripheral Equipment—The XTSCO (external

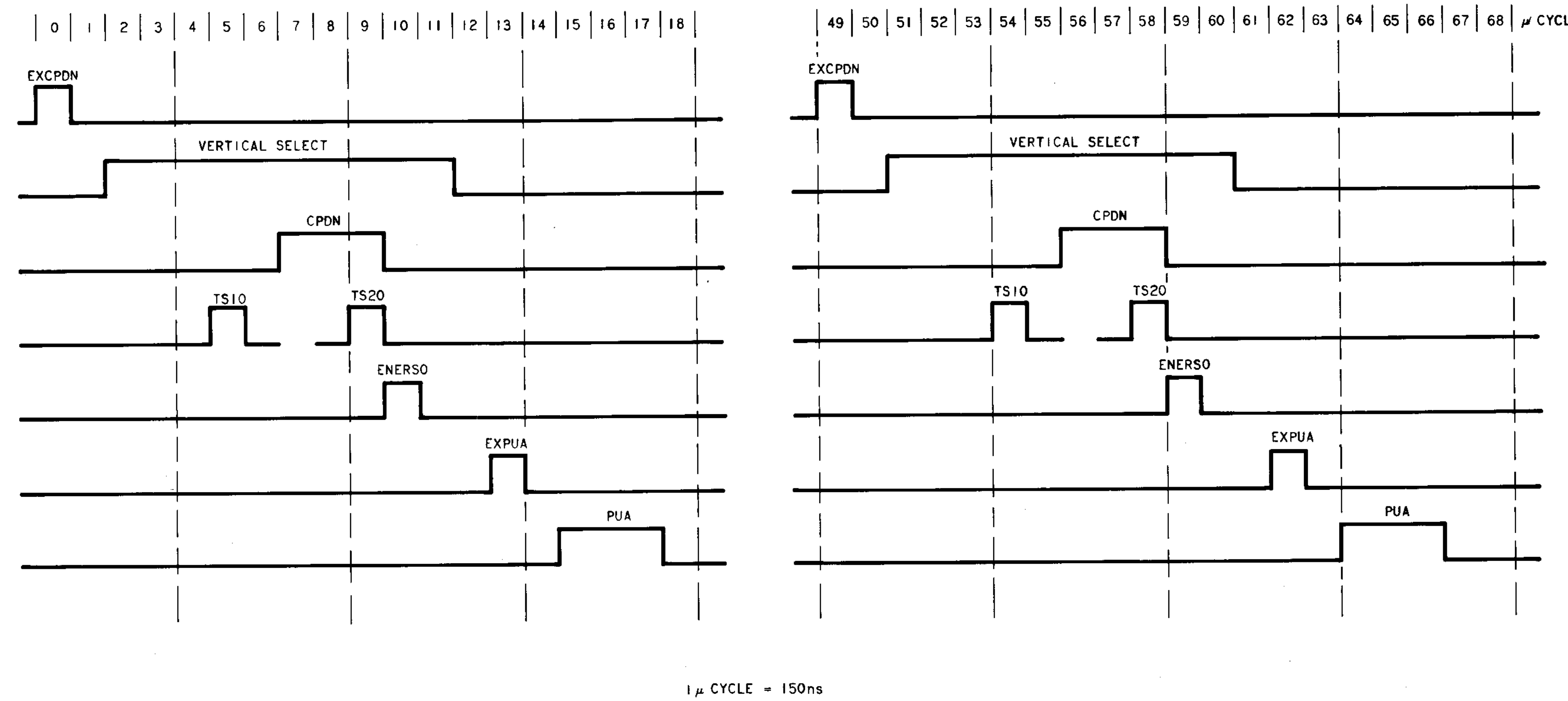


Fig. 12—Timing Pulses

scanner order) command will be used to illustrate how an external scanner order is executed. This command is used for interrogating the state of scan ferrods. Each scanner frame contains 64 rows of ferrods, and each row contains 16 ferrods. One row of ferrods is interrogated at a time. The results of the interrogation (outputs from 16 ferrods) are sent back to the I/O circuit via the scanner answer was and are used to set bits in the SA register. The scanner row to be interrogated is defined by the contents of the enable address (EA) register in the 3A CC. The scanner answer results are loaded into the logic register (LR) in the 3A CC from the SA register in the I/O circuit via the R11 bus.

3.43 Figure 13 illustrates how the 3A CC EA register is used to define a specific scanner row. Bits 0-2 and 3-5 of the EA are decoded in the 2B I/O control circuit (Fig. 13) into two 1-out-of-8 codes which are used to define 1-out-of-64 rows. Bits 6-15 loaded into the I/O EA register and are via a CPD point. The address of the scanner row is transferred to the scanner via the PUA bus. The X decoder decodes a 1-of-8 selection from EA bits 0-2. The Y decoder decodes a 1-of-8 selection from EA bits 3-5. The results from the two 1-out-of-8 decoders are used to set specific bits of the PUA. The X decoding is loaded into PUA bits 0-7. The Y decoding is loaded into PUA bits 8-15. A "1" is loaded into bit positions X and Y+8 of the PUA. All other PUA bits are in the "0" state (Fig. 13).

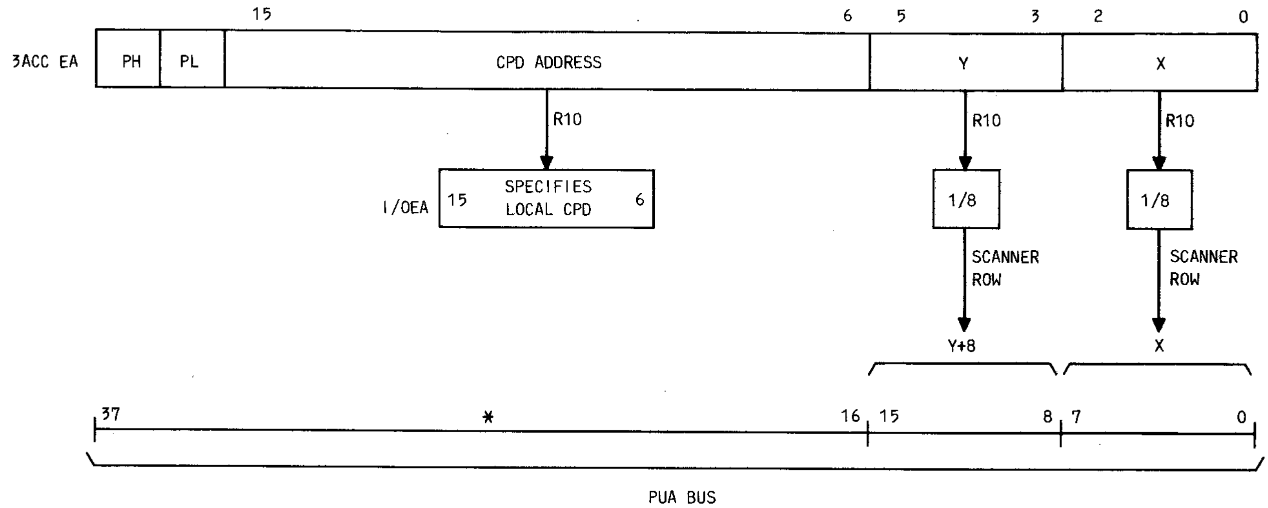
3.44 Figure 14 shows the steps that the microprogram must take in order to execute the XTSCO command. R9 bits 10-15 are loaded with the proper 3-out-of-6 code. Bits 7-9 of R9 put the 2B I/O control circuit into the SCAN mode (000). Ones in bit positions 0-3 of R9 enable loading into the three PUA registers and into the I/OEA register. Bit 6 is used as a check bit. Activating miscellaneous decoder control signal CLSA.ER clears both the SA register and the I/OER and allows the processor to sample a bus to see if the proper 3-out-of-6 code was decoded (4.04).

3.45 Activating miscellaneous decoder control signal LDRI/O (Table A) transfers the contents of R10 (which contains the contents of the 3A CC EA register) into the I/OEA register and simultaneously loads the three PUA registers. PUA bits 0-15 are loaded with the results of the Y and X decoding. Bits 16-37 of the PUA are all set to "0" because in the SCAN mode no inputs to these bits are enabled. Activating miscellaneous decoder control signal EXCPDN generates a CPD pulse (selected by bits 6-15 of the I/OEA register) which enables a specific scanner frame to receive the output of the X and Y decoders appearing on the PUA bus. Activating miscellaneous decoder control signal EXPUA gates the contents of the PUA registers onto the PUA bus. The 3A CC must time the interval between the operation of miscellaneous decoder control signals EXCPDN and EXPUA. The minimum amount of time between the EXCPDN and EXPUA signals is 1.95 usec. The scanner answer results returned from the addressed scanner are loaded into the SA register. Activating the miscellaneous decoder control signal TEST loads conditional flip-flops data status, test register 1, and test register 2 in the 3A CC. The 3A CC then checks to see if a scanner all seems well (ASW) or enable verify (EV) signal has been received, and checks to see if any of the hardware check circuits have detected an error.

3.46 The microprogram waits a sufficient time (long enough for the scanner answer) after the execution of EXPUA before activating the TEST control signal. Activating the LDR11 control signal loads R11 in the 3A CC with the contents of the SA registers. The processor must calculate the parity bits for R11 before it loads the LR (general purpose processor register) with the contents of R11.

3.47 The XTPUBV (external peripheral unit bus order with enable verify) command will be used to illustrate how an external peripheral unit bus order is executed. The XTPUBV is used to transfer information to the automatic message accounting (AMA) frames. The contents of two general purpose registers in the 3A CC (GR and LR) must be transferred to registers PUA0 and PUA1 (bits of 0-31) of the PUA during the EXPUBV command. PUA (bits 32-35) of the bus buffer registers are loaded from bits 2-5 of the EA register, and bits 36 and 37 are set to "0s" for the XTPUBV command. Bits 6-15 of the EA select a CPD output to enable the unit will receive the data sent over the PUA bus. After the execution of the command, the processor expects an EV.

3.48 Figure 15 shows the steps that the microprogram takes in order to execute the XTPUBV command. R9 is loaded with the proper 3-out-of-6 code. Bits 7-9 or R9 put the 2B I/O control circuit



* BITS (37-16) = "0" STATE

Fig. 13—Scanner Row Address Decode

1. LOAD R9 WITH:

15			10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6		0	0	0	1	0	0	1	1	1	1

2. LOAD R10 WITH THE CONTENTS OF THE EA 3ACC REGISTER.
3. ACTIVATE THE CLSA.ER MISCELLANEOUS DECODER CONTROL SIGNAL.
4. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
5. ACTIVATE THE EXCPDN MISCELLANEOUS DECODER CONTROL SIGNAL.
6. ACTIVATE THE EXPUA MISCELLANEOUS DECODER CONTROL SIGNAL.
7. ACTIVATE THE TEST MISCELLANEOUS DECODER CONTROL SIGNAL.
8. ACTIVATE THE LDR11 MISCELLANEOUS DECODER CONTROL SIGNAL.
9. CALCULATE PARITY ON R11.
10. LOAD LR WITH THE CONTENTS OF R11.

Fig. 14—Execution of XTSCO Command

into the LOCAL mode (011). A "1" in bit 0 of R9 enables loading into the PUA0 register from R10. Activating miscellaneous decoder control signal CLSA.ER clears both the SA register and the I/OER and allows the processor to sample a bus to see if the proper 3-out-of-6 code was decoded (4.04). Activating miscellaneous decoder control signal LDRI/O loads the contents of R10 into the PUA0 register. Changing the contents of R9 enables loading into the PUA1 register from R10. Activating the miscellaneous decoder control signal LDRI/O will load PUA1 with the contents of R10 which is now loaded with the contents of the LR register. Activating the TEST miscellaneous decoder control signal allows the processor to sample a bus to see if the proper 3-out-of-6 code was decoded (4.04), and to see if any hardware errors have been detected. Changing the contents of R9 puts the I/O control circuit into the external peripheral unit order (XTPUBO) mode, enables loading into I/OEA from R10, and enables loading bits 32-35 into the PUA2 register from R10 bits 2-5. Activating the LDRI/O signal loads I/OEA with the contents of R10 (now loaded with the contents of the EA register), zeros bits 36 and 37 of the PUA2 register, and loads bits 32-35 of the PUA2 register with bits 2-5 of R10, respectively. Activating the miscellaneous decoder control signal EXCPDN generates a CPD pulse which is selected by bits 6-15 of the I/OEA register to enable the selected unit. Activating the miscellaneous decoder control signal EXPUA places the contents of the PUA registers onto the PUA bus to be received by the enabled frame. The processor times the interval between the execution of the EXCPDN and EXPUA signals as described in 3.38.

3.49 The XTPDOMn (external CPD order with maintenance options) command will be used to illustrate the execution of an external CPD order. This instruction is normally used to control peripheral decoder circuits via a supplementary CPD (SCPD) point. This instruction also jams a constant onto bits 32-37 of the PUA bus (bits 36 and 37 are always in the "0" state). The 2B I/O control circuit contains 512 bipolar CPD points (3.03). When more CPD points than this are needed, a SCPD frame is added. Each supplementary frame contains 512 bipolar SCPD points. To select a SCPD point, the address of the point must be transferred to the SCPD frame via the PUA bus. Figure 16 shows how the contents of the EA register in the 3A CC are decoded to select a SCPD point. Bits 6-14 define the XZY fields of the SCPD point. Bit 15 determines the polarity of the SCPD pulse, and bits 0-5 determine the SCPD frame and controller to be used by selecting a local CPD point which enables the correct SCPD frame.

3.50 In order to save address decoders in each supplementary frame, the address information is put onto the PUA bus in a decoded form. Decoders X, RZ, and Y decode the address directly from R10. Figure 17 shows how the 2B I/O control circuit selects a SCPD point. R9 is loaded with the proper 3-out-of-6 code. Bits 7-9 of R9 put the I/O control circuit into the LOCAL mode (011). A "1" in bit position 2 of R9 enables loading into the PUA2 register from R10. Activating the miscellaneous decoder control signal CLSA.ER clears both the SA register and the I/OER and allows the processor to sample a bus to see if the proper 3-out-of-6 code was decoded (4.04). Activating the miscellaneous decoder control signal LDRI/O loads the contents of bits 0-5 of R10 (which is loaded with the maintenance option constant to be loaded into PUA2) into bits 32-37 of PUA2. Changing the contents of R9 puts the I/O control circuit into the REMOTE mode, enables loading the I/OEA register from R10, loads the PUA0 register from

1. LOAD R9 WITH:

15		10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6	0	1	1	0	0	0	0	0	0	1

2. LOAD R10 WITH THE CONTENTS OF THE 3ACC GR.
3. ACTIVATE THE CLSA ER MISCELLANEOUS DECODER CONTROL SIGNAL.
4. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
5. LOAD R9 WITH:

15		10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6	0	1	1	0	0	0	0	0	1	0

6. LOAD R10 WITH THE CONTENTS OF THE 3ACC LR.
7. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
8. ACTIVATE THE TEST MISCELLANEOUS DECODER CONTROL SIGNAL.
9. LOAD R9 WITH:

15		10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6	0	1	0	1	0	0	1	1	0	0

10. LOAD R10 WITH THE CONTENTS OF THE 3ACC EA.
11. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
12. ACTIVATE THE EXCPDN MISCELLANEOUS DECODER CONTROL SIGNAL.
13. ACTIVATE THE EXPUA MISCELLANEOUS DECODER CONTROL SIGNAL.
14. ACTIVATE THE TEST MISCELLANEOUS DECODER CONTROL SIGNAL.

Fig. 15—Execution of XTPUBV Command

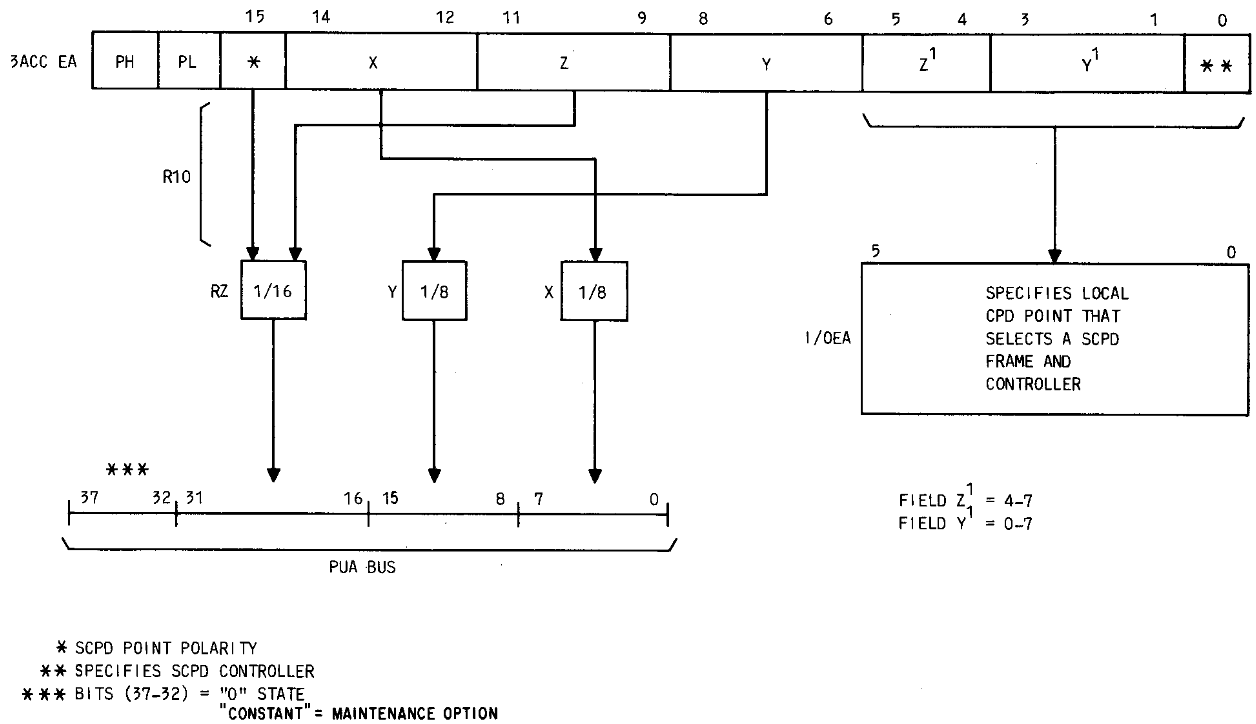


Fig. 16—Addressing for Supplementary CPD

the X and Y decoders, and PUA1 register from the RZ decoder. Activating the miscellaneous decoder control signal LDRI/O loads the I/OEA register with the contents of R10 and simultaneously loads PUA0 and PUA1 from the X, Y, and RZ decoders. Activating the EXCPDN execute normal signal generates a CPD pulse which is selected by bits 0-5 of the I/OEA register to enable the selected unit. Activating the miscellaneous decoder EXPUA signal places the contents of the PUA registers onto the PUA bus to be received by the enabled unit. The 3A CC processor times the interval between the execution of the EXCPDN and EXPUA signals as described in 3.43.

4. MAINTENANCE AND DIAGNOSTICS

GENERAL

4.01 There are no normal controls or indicators associated with the 2B I/O control circuit. Trouble indications are via a coded TTY printout. These trouble codes are referenced in a trouble locating manual (TLM-IC900-D). The trouble locating manual will aid the craftsman in locating the faulty circuit.

4.02 ***Check Circuits***—The 2B I/O control circuit contains circuitry to perform checks on dial pulse timing, 3-out-of-6 code decoding, CPD selection, loading of the I/OEA register, CPD pulse level, mode selection, and register selection.

4.03 ***Dial Pulse Timing Check***—The 2B I/O control circuit contains two cable receivers that pick off the seize (SZ) and release (RL) pulses (Fig. 18) from the dial pulse timing bus. These pulses are used to set or reset the dial pulse test (DPT) flip-flop in the 2B I/O control circuit. The 3A CC can transfer the contents of the DPT bit into the DS conditional flip-flop in the 3A CC by loading R9 with the proper 3-out-of-6 code and by activating ***test*** (a miscellaneous decoder control signal). By sampling the state of the DPT flip-flop, the 3A CC can determine if the seize and release pulses are being correctly generated.

4.04 3-out-of-6 Code Decoding Check—Whenever the 2B I/O control circuit recognizes the two 3-out-of-6 codes that are associated with its operations, it puts the complement of the code onto a bus that goes to the 3A CC. The 3A CC samples the contents of this bus each time the TEST or CLSA.ER miscellaneous decoder control

1. LOAD R9 WITH:

		15 … 10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6	0	1	1	0	0	0	0	1	0	0

2. LOAD BITS (5-0) OF R10 WITH THE CONSTANT TO BE LOADED INTO BITS (37-32), RESPECTIVELY, OF THE PUA.
3. ACTIVATE THE CLSA.ER MISCELLANEOUS DECODER CONTROL SIGNAL.
4. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
5. LOAD R9 WITH:

		15 … 10	9	8	7	6	5	4	3	2	1	0
PH	PL	3/6	0	0	1	0	0	0	1	0	1	1

6. LOAD R10 WITH THE CONTENTS OF THE 3ACC EA REGISTER.
7. ACTIVATE THE LDRI/Ø MISCELLANEOUS DECODER CONTROL SIGNAL.
8. ACTIVATE THE EXCPDN MISCELLANEOUS DECODER CONTROL SIGNAL.
9. ACTIVATE THE EXPUA MISCELLANEOUS DECODER CONTROL SIGNAL.
10. ACTIVATE THE TEST MISCELLANEOUS DECODER CONTROL SIGNAL.

Fig. 17—Execution of XTPDOMN Command

signals are activated. Since one of these control signals is activated after each time the contents of R9 are changed, this code is checked each time R9 is gated into.

4.05 ***CPD Selection Check***—CPD points are selected by decoding either bits 6-15 or 0-5 of the I/OEA register. To check for proper CPD selection the parity of the CPD address, which is stored in the I/OEA register, is calculated (4.06). When a CPD point is selected, it returns the parity of its address to the I/OER register via an even parity or an odd parity bus. The returned parity is compared to the calculated parity. If it does not agree, bit 0 , and bit 6 in the I/OER are set. Bit 0 being set indicates that a check circuit has detected an error. Bit 6 being set indicates that the CPD access check or the I/OEA check circuit detected an error. The error circuitry involved in this check is enabled by the Test Strobe 2 (TS2O) signal (3.37).

4.06 ***Loading of the I/OEA Register Check***—Proper loading of the I/OEA from R10 is checked each time a CPD point is selected. The CPD selection test circuit is capable of detecting errors in loading the I/OEA. When calculating the parity over the CPD address, the address bits are not used. When not in the REMOTE mode, parity over the CPD address bits is calculated by using the parity high and the parity low bits of the I/OEA register and the calculated parity of I/OEA bits 0-5. When in the REMOTE mode, parity over the CPD address is calculated by using the parity low bit, the calculated parity of bits 6 and 7, and the known parity of the four constant CPD address bits that are jammed in "remote".

4.07 By calculating the parity over the CPD address by a means independent of the address bits, any single bit gating error into I/OEA will be detected by the CPD selection test circuit. To increase the probability of detecting multiple bit gating errors into the I/OEA register, the parity of bits 0-7 of the I/OEA register is calculated and compared to the parity low bit. If this comparison indicates an error, the same two bits that are set in the I/OER register by a CPD selection error are set. Although both the CPD selection check and the I/OEA loading check are data dependent, they will detect all single bit faults and the most probable types of multibit faults.

4.08 ***CPD Pulse Level Check***—Each time a CPD point is selected a check is made on the current levels through the CPD circuits. This current is checked by current sensing circuits in the level control circuit. Current sensed after the vertical selection but before the horizontal indicates a short. A lack of current during horizontal selection indicates an open. During normal operation of the CPD matrix, any short or open in any CPD semiconductor is detectable with the exception of an open in a vertical pull-down transistor. Opens

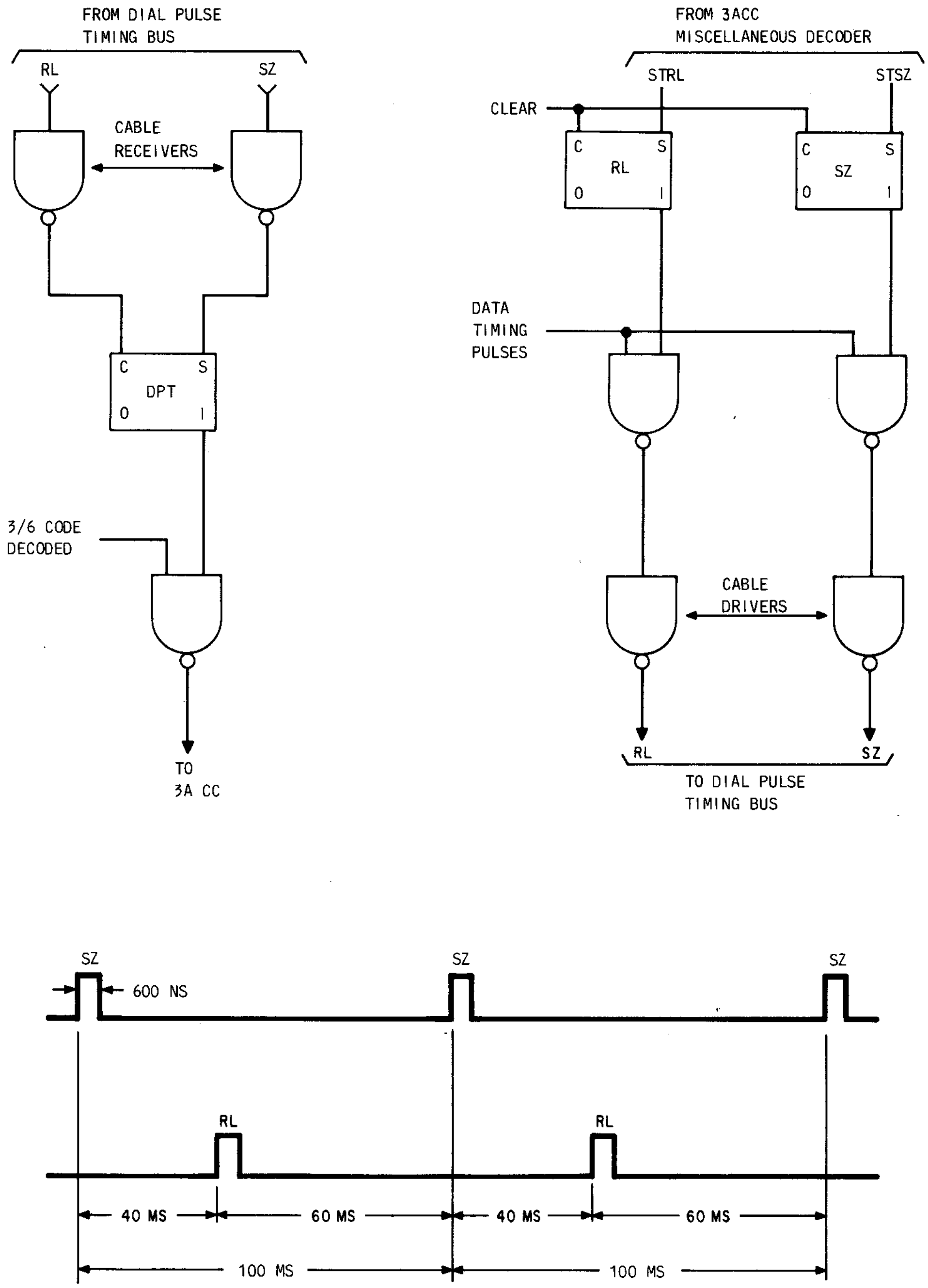


Fig. 18—Generation, Test, and Timing of Seize and Release Pulses

in vertical pull-down transistors can be detected during periodic maintenance tests. Vertical pull-down transistors are maintenance devices and are not essential to the operation of the CPD matrix.

4.09 Test strobe signals TS10, TS20, and ENERSO (Fig. 4 and 12) are used to check for current level errors in the sending of CPD pulses. TS10 checks the current level in the CPD matrix after the vertical selection has been made but before the horizontal selection has been made. If current is detected at this time it indicates a short in the CPD matrix. An error detected by TS10 is normally gated to the I/OER register. By using a maintenance state, TS10 can be used to gate the current level information into the I/OER register. When this is done the current level inputs to the I/OER register are disabled. TS20 is normally used to gate the current level information from the level control circuit to the I/OER register. The current level bits of the I/OER register are output to the check circuits which monitor the CPD current levels. Using the I/OER bits and ENERSO as an enable the CPD matrix can be checked for opens by detecting an absence of current. Also, When the check circuits detect and error, it is gated to the I/OER register by activating the ENERSO test strobe signal.

4.10 ***Mode Selection Check***—The check bit, (bit 6) and bits 7, 8, and 9 of R9 are decoded to determine which of the 8 modes (3.24) the I/O control circuit is in. To check for proper mode selection, the parity of bits 7, 8, and 9 is calculated by using the parity high bit and bit 6 of R9. The parity can be calculated from these 2 bits because the parity of bits 10 through 15 is always odd due to the 3-out-of-6 code and because bit 6 is always the complement of bit 7. Once a mode has been selected, the mode select circuit returns what it determines to be the parity of bits 7, 8, and 9 of R9 to the check circuit. If the returned parity does not agree with the calculated parity, bits 0 EROR and 1 ERMODED are set. The mode selection check circuit is sampled each time miscellaneous decoder control signal LDRI/O is activated. This check is data dependent but it will detect all single bit faults and the most likely multiple bit faults. If in the TEST mode, the mode selection check circuit should indicate an error. This fact is used to check part of the check circuit.

4.11 ***Register Selection Check***—Bits 0-5 of R9 are used to define registers to be loaded or read. Register selection is checked by calculating the parity of R9 bits 0-5 and comparing this to the R9 parity low bit. Bit 6 is always the complement of bit 7, therefore the parity of these two bits will always be odd. Thus, the parity of bits 0-5 should always be the complement of the parity low bit.

5. No. 2B INPUT/OUTPUT CONTROL CIRCUIT, CIRCUIT PACKS

5.01 Circuit pack FA 1098 (control board 1) contains circuitry that performs the following functions:

(1) One-of-eight (1-of-8) mode selection, which controls the mode of operation of the I/O circuit. The mode is decoded from register R9 bits 9-7.

(2) Mode decoding, which compares the parity of the selected mode against the calculated parity of the mode selection address. The parity is calculated by comparing the high parity bit of R9 and the mode address check bit (bit 6) of R9.

(3) Storage and buffering of the parity high and parity low bits for the I/O enable address register. These two bits are received via the R10 parity high and low bits.

(4) Generation of the signals which control the loading and reading of the ten I/O circuit registers. These signals are generated under control of the mode selected by R9 bits 9-6, the register selection determined by R9 bits 5-0, and the load register Misc. Decoder crosspoint from the 3A CC.

(5) Register selection check circuitry which calculates the parity of the register selection bits and compares the calculated parity to the R9 parity low bit.

(6) Compares the parity of the actual CPD selection with the parity of the enable address received via the central pulse distributor (CPD) access check circuits.

5.02 Circuit pack FA 1097 (control board 2) contains circuitry that performs the following functions:

(1) Generation of timing and test strobe signals for central pulse distributor (CPD) and peripheral unit address (PUA) pulses. These

signals and pulses are generated by a 12 bit pulse shift register.

(2) Generation of timing signals for central pulse distributor normal (CPDN) or central pulse distributor fast (CPDF) output pulses and three test strobe signals for testing of the selection and the gating of CPDN pulses.

(3) Generation of timing pulses that are used to gate data onto the PUA bus.

(4) Generation of enabling signals that enable the gating of bits 5-2 of R10 into bit positions 35-32 of the PUA2 register when the I/O control circuit is in the XTPUB0 mode.

(5) Gating the X-field of the CPD address to the CPD translators. When the I/O circuit is in the remote mode the three bits of the X-field are jammed to a constant. When not in the remote mode bits 14-12 of the IOEA register are gated to the translators.

(6) Gating of the bit that determines the polarity of the CPD output pulse to the translators. When the I/O circuit is in the remote mode, EA bit 0 is used to determine polarity. When the I/O circuit is not in the remote mode. EA bit 15 determines polarity.

(7) Controls the execution of CPD and PUA pulses, and the shifting of the pulse shift register (PSR).

5.03 Circuit pack FA 1096 (control board 3) contain circuitry that performs the following functions:

(1) Generation of the one-of-sixteen (1-of-16) code which is decoded from R10 bits 15 and 11-9 and loaded into bits 31-16 of the PUA for remote CPD orders.

(2) One-of-eight (1-of-8) decoding of R10 bits which is loaded into PUA0 bits 7-0 for scan and remote CPD orders. Bits 2-0 of R10 are decoded for scan orders and bits 14-12 are decoded for remote CPD orders.

(3) Gating of the Y and Z fields from the I/O EA register to the CPD translators. When the I/O circuit is not in the remote mode bits 11-6 of the EA register are gated to the translators. In the remote mode, bits 5-1 and one jammed bit in the Z field are gated to the translators.

5.04 Circuit pack FA 1094 (control board 4) contains circuitry that performs the following functions:

(1) Calculates the parity of selected CPD addresses with parity information from the one-of-thirty-two (1-of-32) horizontal and vertical selects.

(2) One-of-eight decoding of R10 bits which are loaded into bit positions 15-8 of PUA0 in remote and scan modes. Bits 8-6 of R10 are loaded in remote, and bits 5-3 are loaded in scan.

(3) Checking of error circuits that monitor CPD current levels from the level control circuit and error indications to the I/O error register. Gating circuits also load the monitored current levels into the I/O error register as indicator bits.

5.05 Two translator circuit packs are used to develop the two 1-of-32 selections (horizontal and vertical) for CPD access. Circuit pack FA 1093 (translator board) contains circuitry that performs the following functions:

(1) Generation of 1-of-16 horizontal selection. A general purpose translator on one of the boards ties the two 1-of-16 translators together to form a 1-of-32 selection circuit.

(2) Calculation of the parity of the selected horizontal lead.

(3) Generation of a 1-of-16 vertical selection. A general purpose translator on one of the boards ties the two 1-of-16 translators together to form a 1-of-32 vertical selection circuit. The vertical selection circuits include the generation of pull-downs used for maintenance testing of the I/O circuit.

(4) Calculation of the parity of the selected vertical lead.

5.06 Circuit pack FA 1095 (dial pulse and data timing) contains circuitry that performs the following functions:

(1) Generates the timing for the data and dial pulse timing signals.

(2) Generation of the data timing and pulse timing signals which are used to gate the dial pulse timing signals which are under control of the 3A CC.

(3) Decodes the main channel select field from R9 bit 15-10.

(4) Monitors the dial pulse timing signals which are sent to the peripheral units.

(5) Generates the shift pulses for the data timing shift register (DTSR).

(6) Determines the on-line or off-line status of the I/O circuit.

(7) Checks the status of the I/O control circuits and returns the result of these checks to the 3A CC.

5.07 Circuit pack FA 1092 (register board) contains circuitry that performs the following functions:

(1) Stores four bits of the following six I/O registers: (Four register boards are used to make up the complete register section.)

(a) PUA0

(b) PUAI

(c) SA

(d) I/O EA

(e) I/O ER

(f) I/O MS

(The four register boards used together make up 16 bits of each of these registers.)

(2) Stores two bits of register PUA2

(The four register boards used together make up 8 bits with only 6 of these bits used for the PUA2 register.)

(3) Contains the circuitry that controls loading and reading of these seven registers.

5.08 Vertical Driver Circuit FC 205—The vertical drivers receive the 1-of-32 vertical selection from the translator boards and use it to do part of the CPD output selection. This selection will access a lead that is common to 32 CPD transformers which are contained on two FC 206 circuit packs. The lead selected determines the polarity of the pulse from the CPD transformers selected. Each FC 205 circuit pack has 11 vertical drivers. Three FC 205 circuit packs are used for the 1-of-32 selection.

5.09 Horizontal Driver Circuit FC-204—The horizontal drivers receive the 1-of-32 horizontal selection from the translator boards and use it to complete the selection of a CPD transformer. The horizontal selection selects one of the 32 CPD transformers that has been accessed by the vertical selection and times the output pulse sent from this transformer. Each FC 204 circuit pack has 11 horizontal drivers. Three FC 204 circuit packs are used for the 1-of-32 selection.

5.10 Circuit pack FC 206, (the CPD matrix circuit), contains the CPD transformers along with load resistors and selection diodes. These transformers are used to send pulses to peripheral units. The output pulses from each transformer can be positive or negative and are used to perform either enabling or signaling functions. In addition, the transformers provide for dc isolation between the 3A CC and peripheral equipment.

5.11 Circuit pack FC 207, (the level control circuit), contains circuitry that performs the following functions:

(1) Circuitry to control the voltage level used to generate a CPD pulse.

(2) Circuitry to monitor the CPD current levels

(3) 200-ohm load resistors for the 3A CC clock signals.

5.12 Cable Receiver Circuit Pack FC 12—The cable receivers receive data from the peripheral units and transfers this data to registers in the I/O circuit. Five cable receiver circuit packs are used to receive 18 bits of data from the east and west branches of the scanner answer bus and to sample dial pulse timing information.

5.13 Cable Driver Circuit Pack FC 13—The cable drivers transmit data and timing pulses to the peripheral units. Six cable driver circuit packs are used to transmit the 38 bit peripheral unit address, dial pulse timing signals, and the data timing pulse.

5.14 Circuit pack FC 21, the +3 volt reference and filter circuit, contains the following circuitry:

(1) A filter circuit for the +3 volt power supply

(2) A +3 volt reference.

5.15 The A8 power converters provide +3V power for the circuit packs of the I/O.

6. GLOSSARY

6.01 The following is a glossary defining terms used in No. 2B ESS.

SECTION	TITLE
AN	Answer
ASW	All Seems Well
CC	Central Control
CPD	Central Pulse Distributor
CR	Control Register
DPT	Dial Pulse Test
DS	Data Status
DTSR	Data Timing Shift Register
EA	Enable Address
ESS	Electronic Switching System
EV	Enable Verify
Fig.	Figure
HORIZ	Horizontal
HS	Horizontal Select
I/O	Input/Output
MAINT	Maintenance
MARG	Marginal
MISC	Miscellaneous
MS	Maintenance State
ms	millisecond
ns	nanosecond
PH	Parity High
PL	Parity Low
PSR	Pulse Shift Register
PUA	Peripheral Unit Address
REG	Register
RL	Release
RZ	Remote Z
SA	Scan Answer
SCPD	Supplementary Central Pulse Distributor
SENS	Sense
SZ	Seize
TR	Test Register
TRANS	Transformer
TS	Test Strobe
USEC	Microsecond
VERT	Vertical
VS	Vertical Select