CONTROL COMPLEX

INTERFACES AND THEORY OF OPERATION

NO. 3 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

INTRODUCTION

1.01 This section describes in general terms the interfaces and theory of operation of the control complex, a subsystem of the No. 3 Electronic Switching System (ESS).

1.02 ➧This section is being reissued to include some additions and changes to update the Control Complex Interfaces and Theory of Operation

No. 3 Electronic Switching System. Change arrows have been used to indicate changes.◆

PURPOSE OF CONTROL COMPLEX

1.03 The control complex (Fig. 1, 2, and 3) is that portion of the No. 3 ESS office equipment which provides logical control of the office. All system functions necessary for processing calls (including maintenance routines) are directed by the control complex. Man-machine interface is accomplished via a local and/or remote teletypewriter (TTY), the control panel of the 3A Central Control (3A CC), and the system status panel (SSP). One control complex is capable of supporting a No. 3 ESS at full capacity.

CONFIGURATION OF CONTROL COMPLEX

1.04 No. 3 ESS is designed to accommodate up to 4500 customer lines with full feature service in a small office environment. The control complex subsystem is designed to provide basically a single work position control facility whenever the office is attended. Unattended operation is facilitated via the TTY, telemetry, and administrative data links to another office designated as the Switching Control Center System (SCCS).

1.05 Physically, the control complex consists of a processor frame and a maintenance frame (Fig. 1 and 2). Figure 4 is a block diagram of control complex units.

PROCESSOR FRAME

1.06 ◆The processor frame (part of Fig. 1 and 2) is divided into two bays (0 and 1), each of which contains duplicated equipment. Controlled and protected (fused) power is obtained from the processor power unit of each bay. The processor frame consists of the following units:

- 3A CC and control panel
- Main store (MAS)
- Processor power supply unit.◆

A. 3A CC and Control Panel

1.07 Each 3A CC contains all the necessary logic required to direct and control the processing of data within the No. 3 ESS. Two 3A CCs normally operate in duplex such that one 3A CC has active control over the system, while the other 3A CC assumes a standby mode. The on-line 3A CC keeps both the on-line MAS memory and the standby MAS memory up to date. The standby 3A CC can assume control of system tasks if a failure or excessive errors occur in the on-line 3A CC. When the standby 3A CC or its associated MAS is inoperative, the on-line 3A CC and its MAS carry the load.

1.08 Keys and lamps on the 3A CC control panel provide status and manual control of the 3A CC for maintenance and trouble analysis purposes. The control panel provides the capability to operate the standby 3A CC off-line for diagnostic purposes. Light emitting diodes (LEDs) display the data or address of a MAS memory location or register. Key-type switches are used in selecting desired manual control. ***The 3A CC control panel should be used only in an off-line control unit or if the system is inoperative.***

B. Main Store

1.09 The MAS consists of the main store controller (MASC) and the main store memory (MASM). The MASM consists of the program store which contains the generic program and translation data as well as the temporary store which is used by the 3A CC as a means of storage for transitory data. The program store portion of the MAS is protected from inadvertent writing into its contents by a hardware write-protect feature. The MASC is the interface between the 3A CC and its associated MASM. The MASC controls storage and retrieval of data to and from MASMs in response to commands from the 3A CC. It controls the refreshing of memory modules, provides the write-protect circuitry, and collects diagnostic and error information to be sent to the 3A CC. The main store bus (MASB) interconnects the 3A CC and MAS via the MASC.

C. Processor Power Supply Unit

1.10 Both processor bays (0 and 1) receive +24V and -48V from the power distribution system. Power is fused, filtered, and distributed to power converter modules in the power supply unit or to converters in individual units such as the MASCs and MASM where voltages are required.

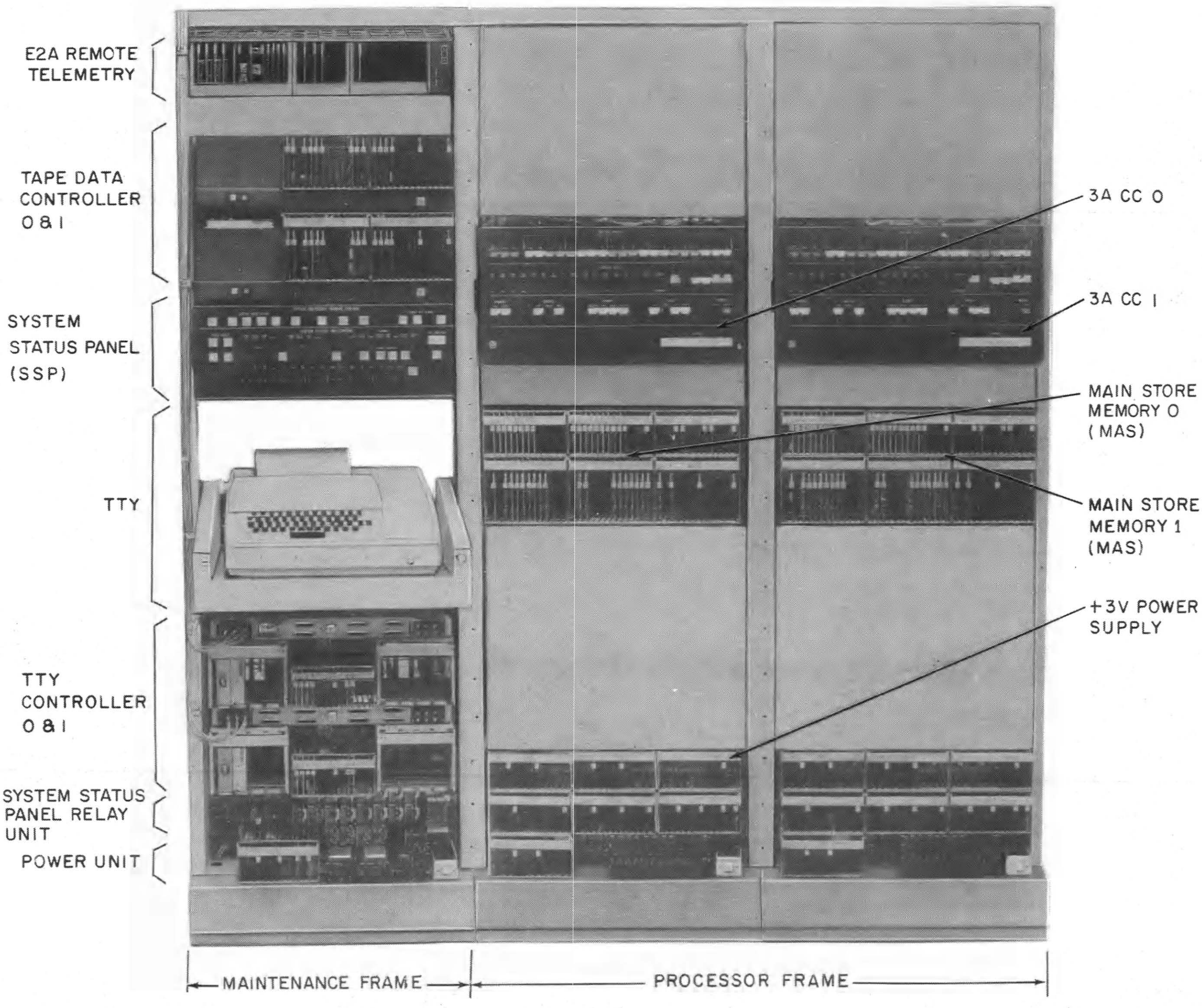


Fig. 1—Control Complex—Front View

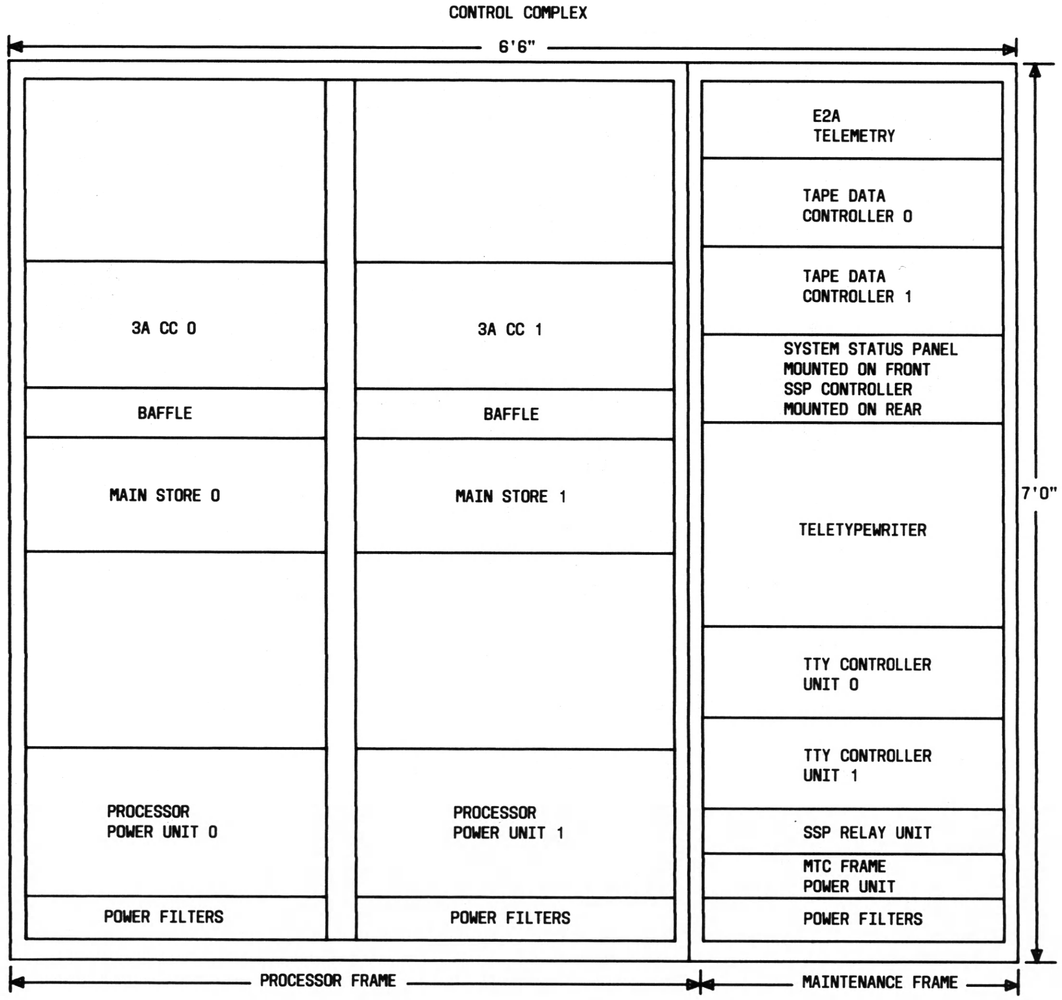
MAINTENANCE FRAME

1.11 ➧The maintenance (MTCE) frame (part of Fig. 1 and 2) consists of one bay of equipment which contains:

- E2A telemetry unit (optional)
- Tape data controller (TDC) 0
- Tape data controller 1
- System status panel/system status panel controller (SSP/SSPC)
- Teletypewriter (TTY)
- Teletypewriter controller (TTYC) unit 0
- Teletypewriter controller unit 1
- System status panel relay (SSPR) unit
- Maintenance frame power unit.⬅

A. E2A Telemetry Unit

1.12 ➧The E2A telemetry provides a communication link between the system status panel control



➧Fig. 2—Control Complex—Rear View⧏

(SSPC) and an SCC. It receives command information from and transmits responses to the SCC via a private line data facility or the direct distance dialing (DDD) network. The SCC is thus able to monitor system status and execute certain emergency control operations for a specific system. It also shares control of selected SSPC functions with the SSP switch related to the function on an ORed basis. Control signals from the E2A to the SSPC are transmitted via coaxial cable, and scanned SSPC functions are transmitted to the E2A via twisted pair leads.⧏

B. Tape Data Controller

1.13 ➧The TDC provides a magnetic tape memory system for the 3A CC. In various applications, it provides a magnetic tape copy of programs and data files required as backup for the volatile main store memories (resident programs) and various nonresident (paged) routines and diagnostics.⧏ The TDC units are designated 0 and 1. The TDC 0 is always used by both 3A CC 0 and 1 unless it has a problem, then TDC 1 is used. The on-line 3A CC keeps both on-line and standby TDC units updated with identical information, although there are instances when the on-line 3A CC can read from both TDCs simultaneously.

C. System Status Panel and System Status Panel Controller

1.14 ➧The SSP operates in conjunction with the SSPC and SSPR, and provides a visual display of general system health. It provides local manual switching capability and also forms an

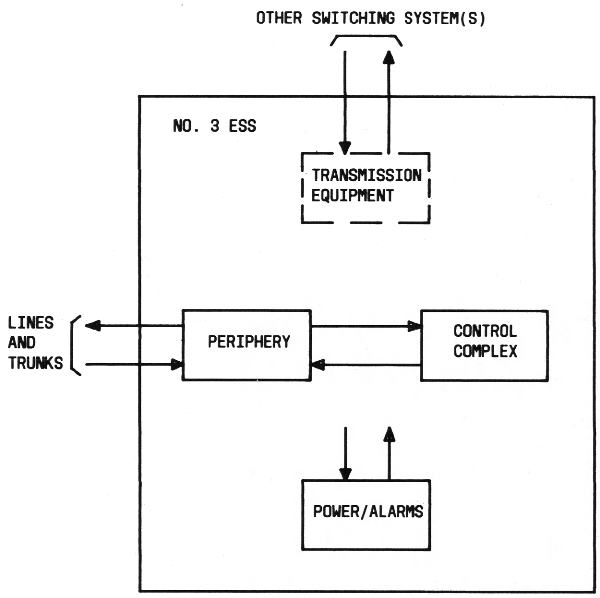
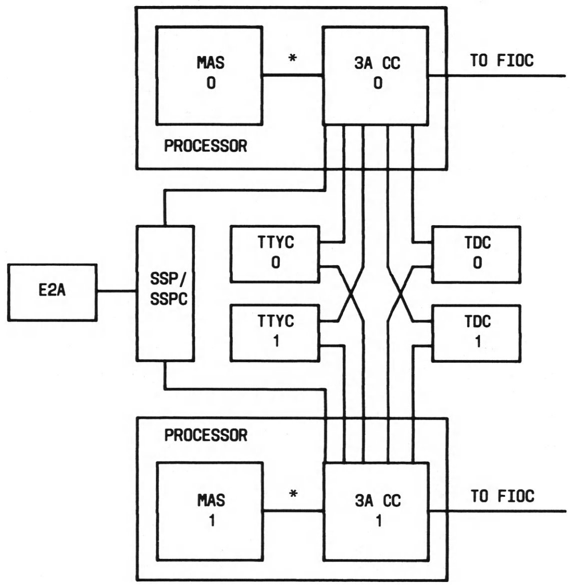


Fig. 3—Equipment Subsystem Interfaces



* PARALLEL BUS. ALL OTHER INTERCONNECTIONS SHOWN ARE SERIAL.

Fig. 4—No. 3 ESS Control Complex—Block Diagram

integral part of the interface circuitry to the E2A telemetry for SCC applications. The SSP thus provides for the following local and remote maintenance functions:

(a) Remote (SCC) monitoring of SSP.

(b) Emergency manual control by allowing entry of a manual request for a system initialization simultaneously to both 3A CCs.

(c) A means of forcing a 3A CC on-line or off-line.

(d) Local control of other switching functions through switches that are interrogated via program initiated input/output (I/O) messages to the SSPC.

1.15 The SSPC contains the interlock and control logic and display buffers required for operation of the SSP. It provides the I/O circuitry for communication between a 3A CC and the SSP, pulse driver circuits for the system initialization function, and timing functions. The SSPC also contains buffering circuitry required for communication between the SSP and the E2A telemetry unit.

D. System Status Panel Relay Unit

1.16 The SSPR unit provides a relay interface between the SSPC and office alarms or various system peripheral frames as required. The circuit also contains power sequencing relay logic and alternate bus switching relays pertaining to the SSPC and SSP power supply.

E. Teletypewriter and Teletypewriter Controller

1.17 The TTY facilities (TTYs plus TTY control units) provide the primary means of communication between operating personnel and the system. Operating personnel may request, via TTY input messages, specific actions to be performed by the system. The TTY output messages provide system response to such requests, as well as periodic printouts of system status and error conditions.

1.18 Each TTY control unit (0 and 1) in the maintenance frame provides mounting facilities and power conversion for two TTYC circuits. Each circuit has four ports, with each port capable of controlling one TTY. The TTYC circuits are numbered 0 through 3, with even-numbered circuits (0 and 2) appearing in TTY control unit 0 and odd-numbered circuits (1 and 3) appearing in TTY control unit 1. The TTYCs are also called ***left*** and ***right,*** as viewed from the rear of the TTY control unit.

1.19 Each TTYC provides the interface between the 3A CC and up to four TTY ports. The four TTY ports associated with each TTYC comprise a hub arrangement, whereby signals from any one are seen by the others. Ports 0 through 3 are associated with TTYC circuits 0 and 1 ***(right)*** and ports 4 through 7 are associated with TTYC circuits 2 and 3 ***(left).*** The local maintenance TTY (contained in the maintenance frame) is usually assigned to port 0 of TTYC 0. The remote maintenance channel and other port assignments may vary with equipment usage. Appropriate system application documentation should be consulted for TTY port assignments.◀

F. ▶Maintenance Frame Power Unit

1.20 The maintenance frame power unit provides the power fusing and distribution for all units appearing in the maintenance frame. It includes circuits that detect fuse failures and other power problems within the maintenance frame. On-unit visual indications and relay interfacing to off-unit office alarm circuits for these failures are provided. Also included is a power alarm test feature for testing portions of the minor alarm circuit of all dc-to-dc converters within the frame.◀

CONTROL UNIT

1.21 The SSP/SSPC, in association with a processor (3A CC, MAS, and bus), define a control unit (CU) (Fig. 5). The processor is involved in the handling of calls and is duplicated for reliability purposes. The SSP and SSPC portion of the CU used to address the 3A CC for selective control and maintenance are not directly involved in customer call processing; therefore, they are not duplicated. Either, or both, the SSPs and SSPCs can be out-of-service without affecting call processing. In either case, the TTY, whether local or remote, monitors system status. (TTY services to suit each office are supplied using various options.)

2. SIGNAL AND CONTROL INTERFACES—CONTROL COMPLEX TO PERIPHERY

2.01 Control complex signal and control signals interface with peripheral equipment in the following two areas (Fig. 6):

- 3A CC with the frame input/output controllers (FIOC)
- Teletypewriter controllers and E2A telemetry with the low profile combined distributing frame (LPCDF). The LPCDF is a 7-foot high CDF used to interface between inside and outside plant equipment.

A. 3A CC Interface With FIOC

2.02 The 3A CC controls the peripheral equipment over a 6.67-megabit per second serial I/O main channel. Twenty subchannels are available in the 3A CC main channel. Subchannels serve as the interface between the 3A CC and the FIOCs which, in turn, interconnect with the network controller (NWC), scanner controller (SC), and peripheral pulse distributor (PPD).

2.03 Four subchannels (5-coax lead) of each 3A CC are connected to their respective FIOC (0 and 1) by connectorized coaxial cables (Fig. 7). Refer to 3.37 through 3.52 for additional coverage.

B. TTYC and E2A Telemetry Interface With LPCDF

2.04 Eight TTY ports using two TTYCs are provided to facilitate a variety of TTY unit options for local and remote applications (Fig. 6 and 8). TTY information can be distributed through each individual port or any combination of ports including four in parallel. TTYC 0 unit has four ports (0 through 3) used for the optional local maintenance TTY and remote maintenance TTYs. TTYC 1 unit also provides four miscellaneous ports (0 through 3) that are used to facilitate autoconnect (dial-up) for remote locations such as the Remote Service Bureau (RSB) via the LPCDF. Desired options are obtained by interconnecting the equipment with dedicated cables. The basic TTY use options are:

- Local TTY—with Electronic Industries Association (EIA) interface
- Remote TTY
- Local TTY—with current loop interface.

2.05 E2A telemetry equipment provides the means of transferring system status and control between the No. 3 ESS and the SCC (Fig. 9). Connectorized cabling interconnects the E2A telemetry and the LPCDF. The LPCDF provides the necessary cross-connection for trunking to access the remote SCCS.

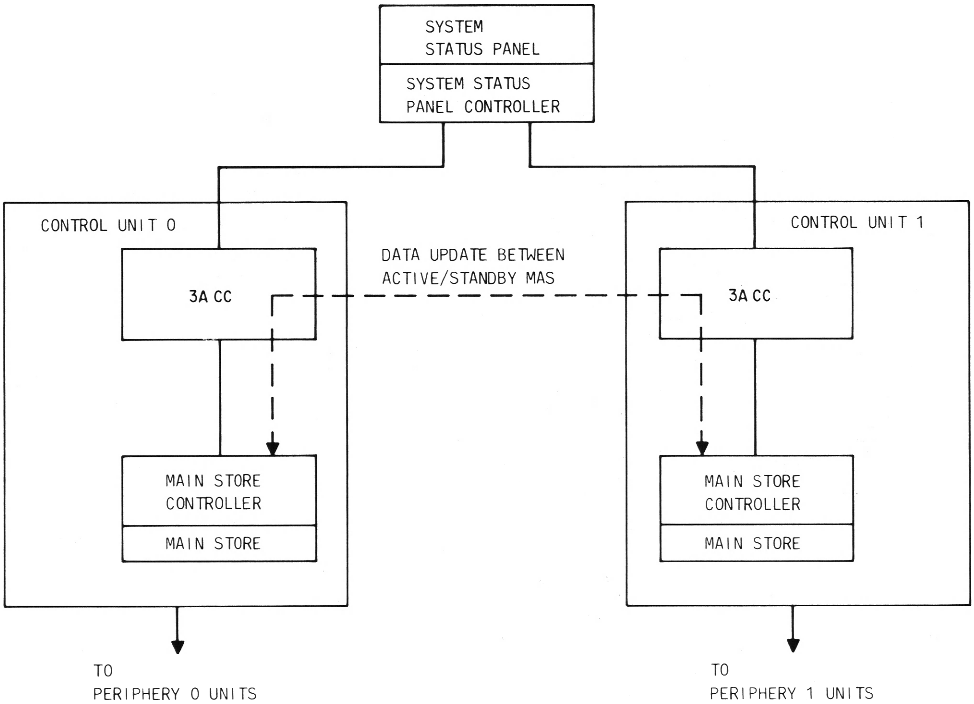


Fig. 5—No. 3 ESS Control Units 0 and 1—Block Diagram

3. THEORY OF OPERATION—CONTROL COMPLEX SIGNAL AND CONTROL INTERFACE CIRCUITS

INTRODUCTION

3.01 The 3A CC uses five basic entities to transfer control signals and data within the control complex. These are:

1. Main store bus (MASB)
2. Maintenance channel (MCH)
3. Input/output subchannel (IOSC)
4. Interrupt (INT) facility
5. System status panel (SSP/SSPC).

MAIN STORE BUS AND ASSOCIATED OPERATION

3.02 The 3A CCs and MASs communicate over unbalanced, direct-coupled (dc) bus system MASB. Use of this bus system eliminates the need for bus transformers and permits standard 1A logic gates to be used as the bus drivers and bus receivers. Using 1A gates avoids interface problems with the logic used to couple the main store busses (MASBs) and allows data and address logic to be incorporated into the bit-slicing circuit packages. Address, data, and control leads that make up the MASB are identified in Fig. 10. In all cases, the active signal is near ground potential in the back plane of the 3A CC for MASB signals.

3.03 To protect against overvoltage and/or excessive current faults between 3A CCs, special fuse protection in FB6 circuit packs are included in each 3A CC. This fuse protection is series-connected in each MASB lead that cross-connects between the 3A CCs. Figure 11 traces store address lead 0 (SA0) as a typical MASB circuit.

A. Processor Bus Controller

3.04 The MASB signals are controlled by the 3A CC via the processor bus controller (PBC). Figure 12 shows the PBC in respect to other functional areas of 3A CC. The main store controller (MASC) receives signals from the PBC, performs the designated functions, then responds via the MASB. Table A identifies the MASB leads and defines their functions.

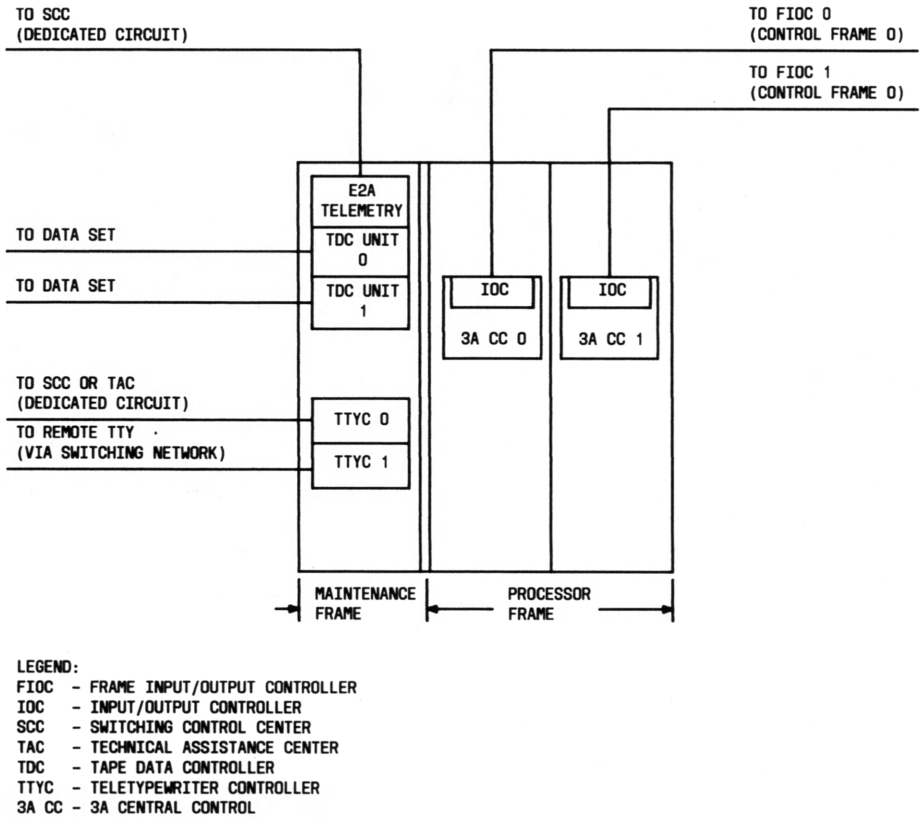


Fig. 6—Control Complex to System Interface Signal and Control

3.05 PBC functions can be divided into two parts:

- Address and data logic
- Control and sequencing logic.

The address and the data portion consist of four registers used to address the MAS and to buffer data to and from the MAS.

B. PBC Address and Data Signals

3.06 The store address register (SAR) is used to buffer the address of the present MAS request; its outputs may be gated directly onto the MASB. The program address (PA) register supports the SAR by saving the last address from which a processor instruction was fetched. In addition to the SAR and PA registers, there is combinational logic directly attached to the outputs of the PA register. This circuitry is called PA+1 logic and is used to increment the MAS addresses for requests to consecutive MAS locations. The SAR sends addresses to a similar register, store controller address register (SCAR), located in the MASC. The SCAR buffers address signals received from the PBC to access locations in the MAS.

3.07 The 16-bit store data register (SDR) in the PBC is used to buffer data from the MAS on a read request. On a write request, it contains the data to be written into the MAS; therefore, SDR functions are considered bidirectional. The store instruction register (SIR) in the PBC is a 16-bit register. It buffers instructions as they are fetched from the MAS. The SDR sends and receives. The SIR receives data signals from the MASC on the MASB via the store data (SD) signals. Attached to the SD signals in the MASC is a 16-bit register called the store controller data register (SCDR). It is used to buffer the data signals sent to and from the PBC and MAS.

C. PBC Control and Sequencing

3.08 PBC control and sequencing provides the control interface between microprogram control and the MASC. Its primary function is to

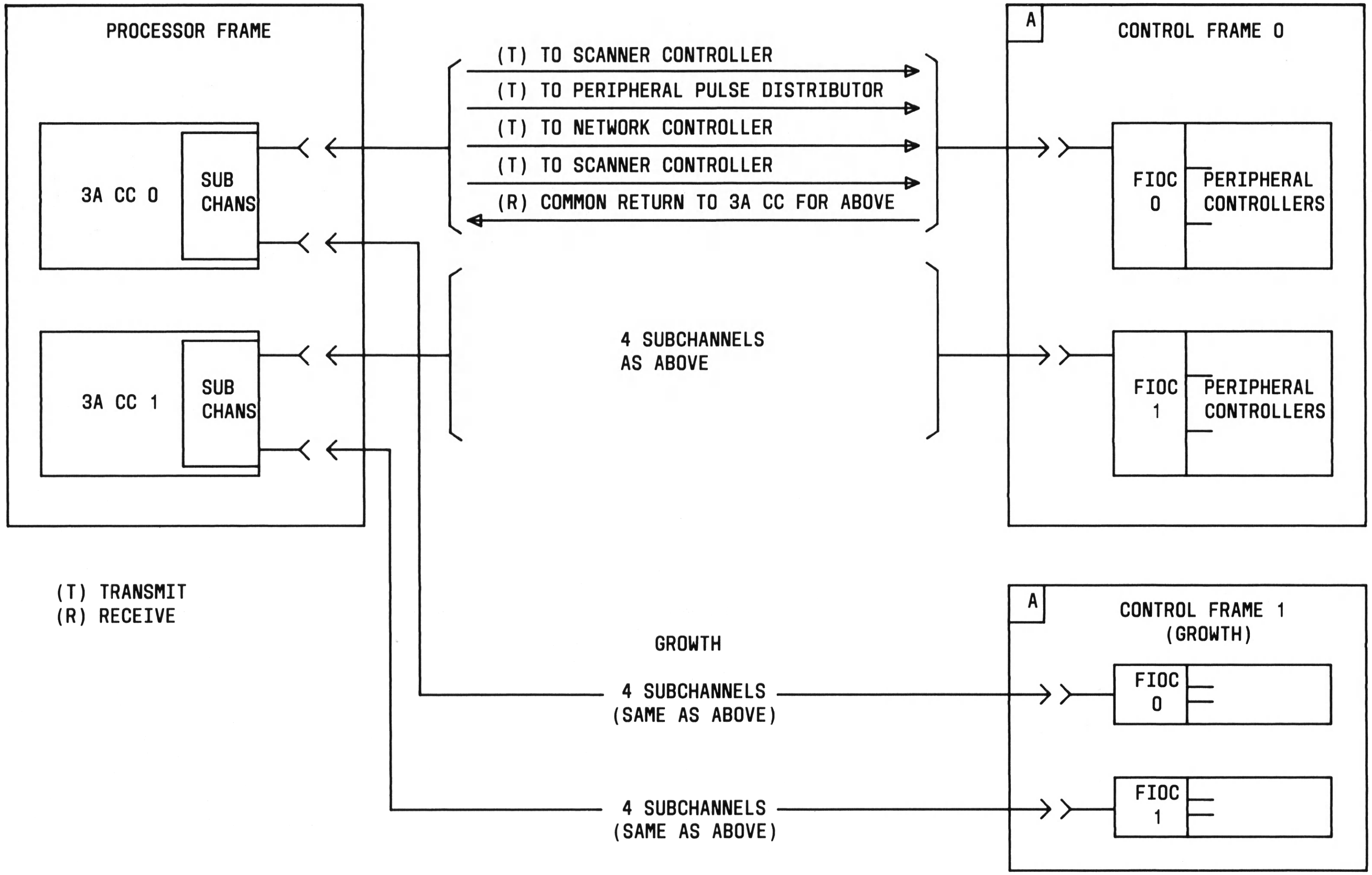


Fig. 7—Signal Leads Between Control Complex (3A CC) and Control Frame (FIOCs)

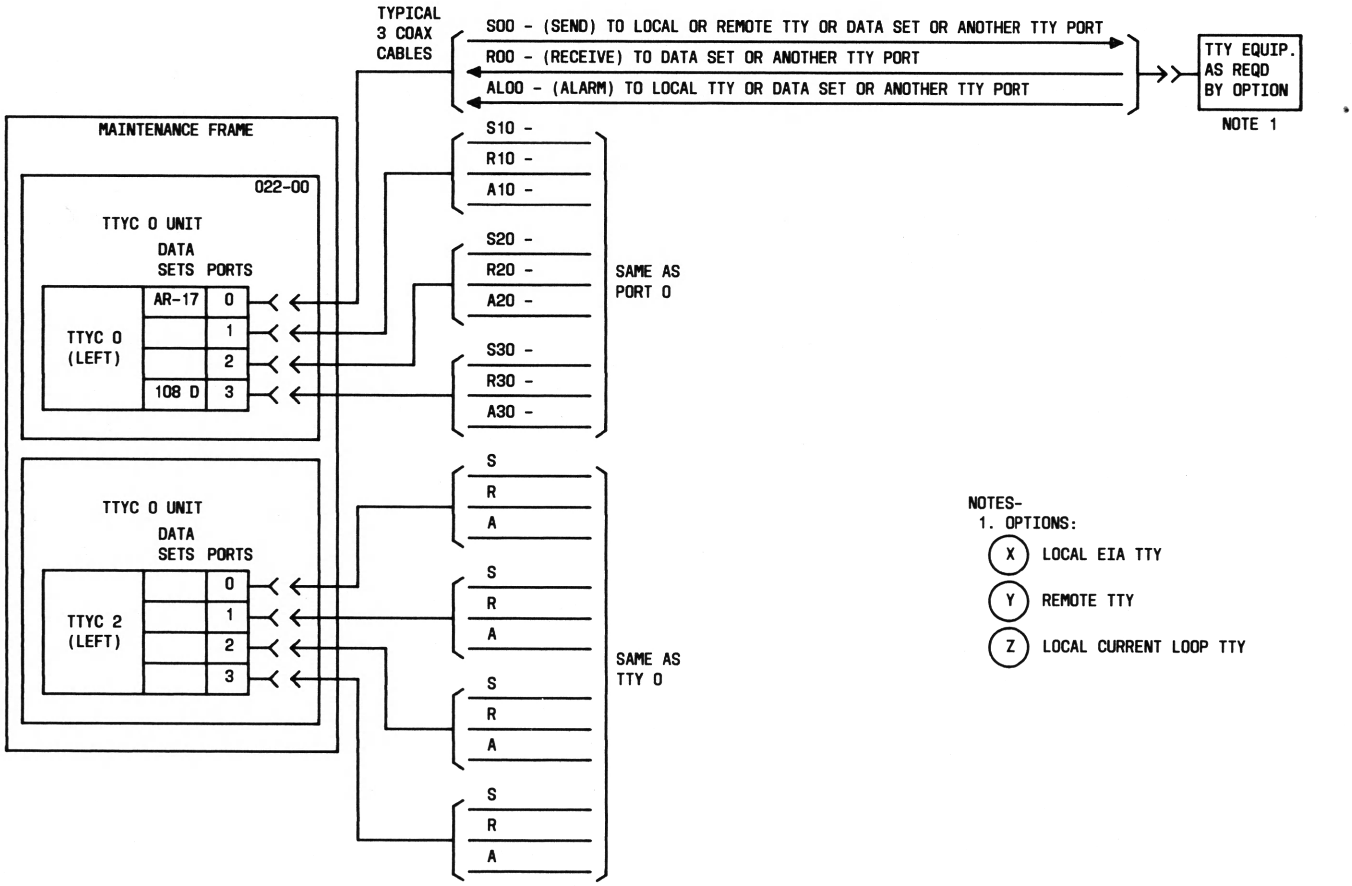


Fig. 8—Signal Leads Between Teletypewriter Controllers and Optional Teletypewriter Equipment

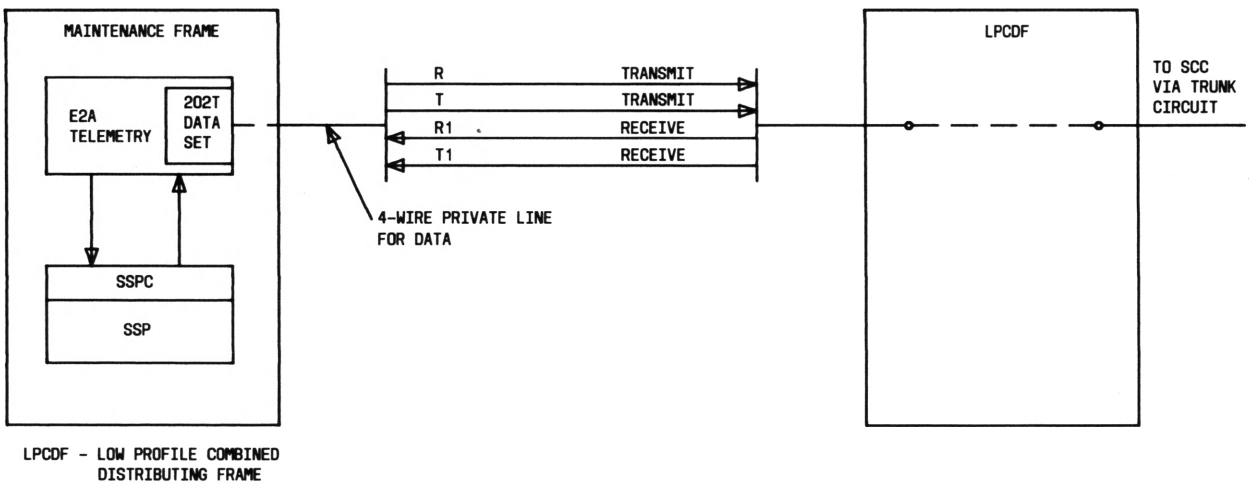


Fig. 9—Signal Leads Between E2A Telemetry Unit and LPCDF

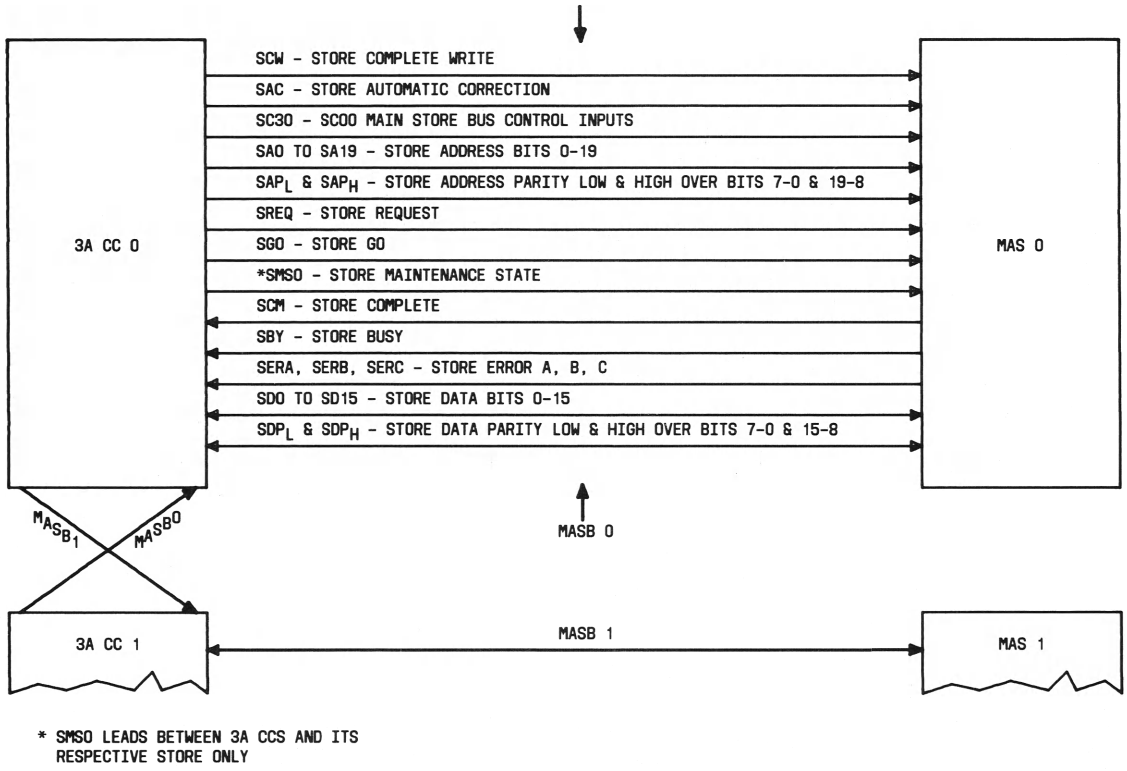


Fig. 10—Main Store Bus Leads Between 3A CC 0, 3A CC 1, and Respective Main Stores

receive, buffer, and execute MAS requests initiated by microcontrol in the 3A CC. The PBC control of the MASB can be further subdivided into two separate functional operations:

- Static conditions—Controls that remain fixed during a memory cycle
- Dynamic conditions—Controls that determine the sequence of a given memory cycle.

3.09 ***Static states*** on the MASB are buffered in the main memory status (MMS) register of the PBC. Table B shows bit designations and functions of this register. Figure 13 shows a layout of MMS bit assignments and the eight possible states of the four MAS command leads (SC3 through SC0). The MMS controls such functions as: whether a read or write is to be performed, whether writes are issued to both MASBs, which MASB is active in case of a read, etc.

3.10 During a 3A CC initialization procedure, the MMS is loaded, using microprogram control by a microcontrol data command. This command obtains a constant from microstore to define the initial state of the MASB. The loaded MMS then determines the basic mode of operation of the MASB for subsequent memory requests to be used during initialization. Once the initialization sequence has started to access MAS instructions, the MMS can be altered using maintenance type instructions to define the normal operating state of the PBC and the associated MASB.

D. PBC Dynamic Conditions

3.11 The dynamic conditions of the PBC are those states through which the control logic must sequence in the process of (1) issuing a MAS request to the MASC, (2) receiving the appropriate response, and (3) then completing the memory cycle. To perform this sequencing, there are five main flip-flops that buffer the control states being sequenced. Each of the flip-flops is identified and its function briefly defined below. However, only the GO flip-flop signal is carried on the MASB. The other four flip-flops support the PBC functions during a given memory cycle via other circuit leads.

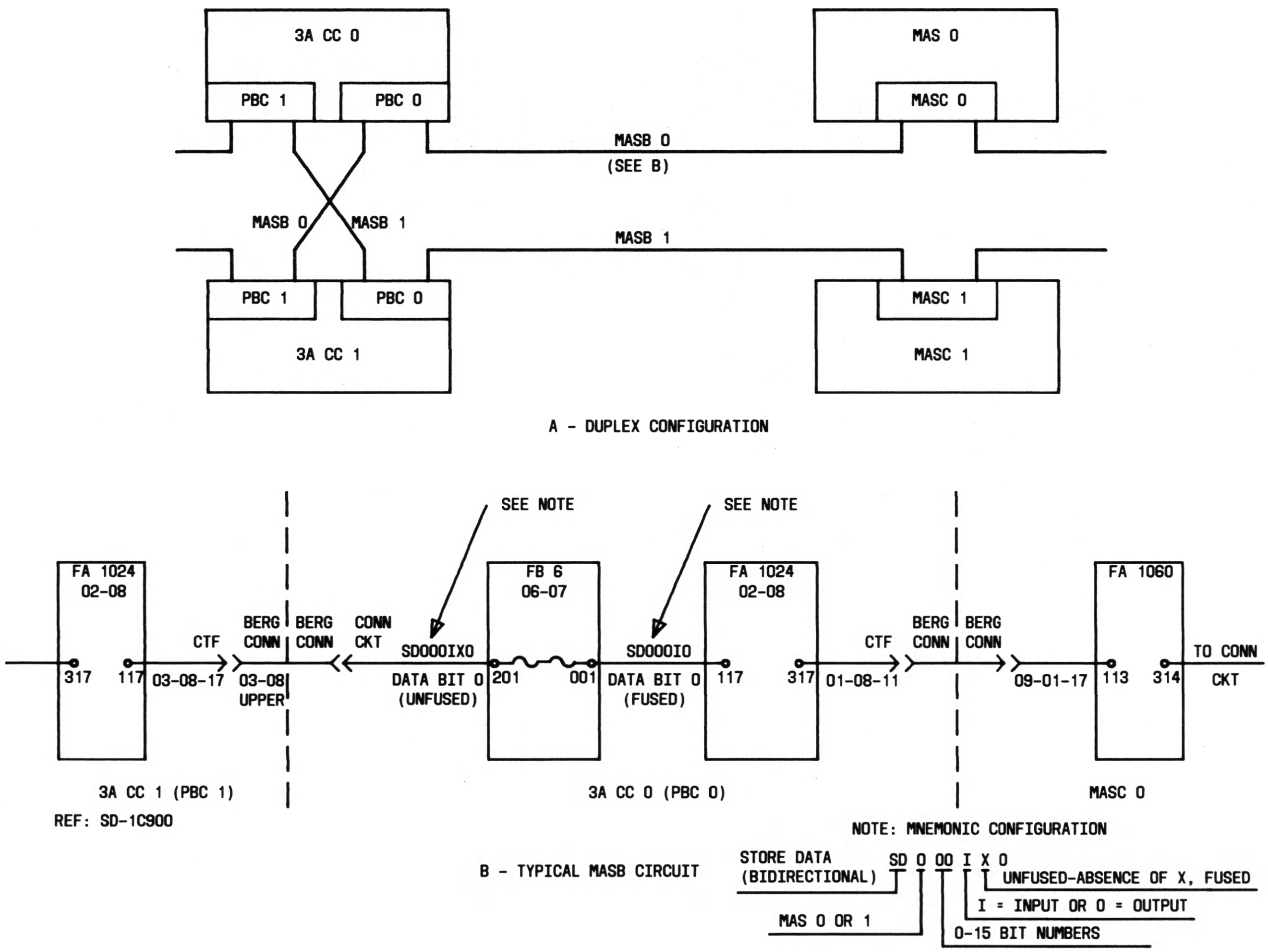


Fig. 11—Typical Main Store Bus Circuit Showing Special Circuit Protection

3.12 The ***request flip-flop*** indicates that a request for a memory cycle has been issued by microcontrol. This flip-flop does not provide the STORE REQUEST signal used on the MASB. Setting the request flip-flop starts a memory cycle.

3.13 The ***seize flip-flop*** is used to indicate that the PBC is in process of issuing a memory request to the MAS. The flip-flop does not get set until the MASB is idle. The seize flip-flop functions to isolate the MASB from units of lower priority so they do not interfere with the memory cycle presently in progress. At the completion of the memory cycle, the seize flip-flop will be reset, allowing other users on the MASB to issue their request to the MAS.

3.14 The ***GO flip-flop*** is used to activate the SGO signal on the MASB. This indicates to the MASC that the address data (if a write cycle) and the other control signals on the MASB are stable before a memory cycle can begin. The GO flip-flop becomes active approximately the same time the seize flip-flop becomes active. The GO flip-flop becomes inactive when the store complete (SCM) signal returns from the MAS and sets the data ready (DR) flip-flop indicating that the MAS has completed the requested memory cycle; ie, the GO flip-flop is reset when the DR flip-flop is set.

3.15 The ***data ready (DR) flip-flop*** is used to indicate to microcontrol that the MAS has completed the requested memory cycle. It is set in response to an active store complete (SCM) signal returning from the MASC. For each memory cycle, the state of the SCM signal is gated to the

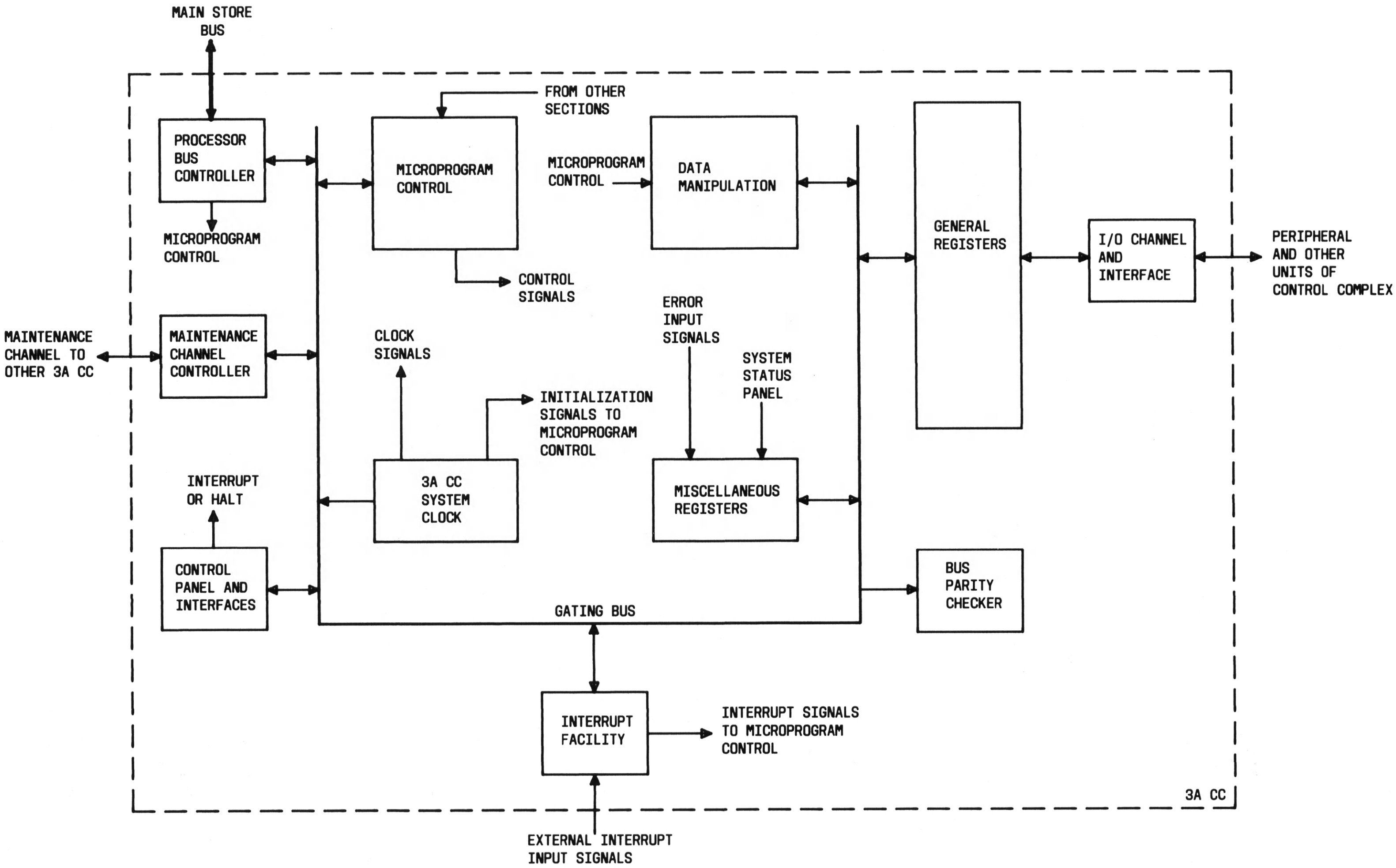


Fig. 12— Block Diagram of the 3A Central Control

TABLE A

TYPICAL DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEAD	FUNCTION
SC3, SC2, SC1, SC0	*Store Command Leads 0 Thru 3:* These leads are used by the 3A CC to issue a 2-out-of-4 command code to the memory. The assignments of the codes are: 1100 = Read The contents of memory at the location defined on the address leads are returned on the data leads. 0011 = Write The 16 data bits and 2 parity bits on the data leads are written in the store at the location defined on the address leads. 1001 = Load-Write-Protect This operation returns the contents of the write-protect (WP) register in the store controller to the 3A CC. 0110 = Store-Write-Protect This operation loads the WP registers in the store controller. 0101 = Blind-Write This operation (when hardwire enabled) writes data into write-protected areas of memory. Blind-write not intended for field use. 1010 = Spare
SREQ	*Store Request Lead:* This signal is used by a lower priority. 3A CC to inform a higher priority 3A CC that it wants sole ownership of the MASB for a multiple cycle operation. This signal is necessary to prevent interwrite problems with multiple users on an MASB. It is not necessary for a higher priority user to inform a low priority user of a multiple cycle operation, as the high priority user has the ability to prevent store access by a lower priority user.
SGO	*Store Go Lead:* This is a signal that is put on the bus to tell the store that a store operation has been requested. It is removed after the 3A CC has received the store-complete (SCM) signal. In the case of a read operation, the address and command information is present on the bus. In the case of a write operation, the data, as well as the address and command information, is present on the bus.
SCM	*Store Complete Lead:* This signal is sent by the store to indicate that the readout information is present on the bus for read operations. It is also sent on a write operation to indicate that the command, data, go, and address information may be removed from the bus.
SERA	*Store Error A-Lead:* This signal is sent by the store to indicate that a possibly fatal fault has occurred. This signal will cause an initialization of the 3A CC. Some external items to the store which would generate an SERA signal include a parity error on either address or data, an invalid command code, and an unequipped store location address.

➧ TABLE A (Contd) ➧

TYPICAL DESIGNATIONS AND FUNCTIONS OF THE MAIN STORE BUS LEADS

LEAD	FUNCTION
SERB	*Store Error B-Lead:* This signal is sent by the store to indicate that a write-protect error has been detected. This signal will cause an initialization of the 3A CC. An attempt to issue a write command in a section of memory that has been write-protected will result in an SERB signal.
SD0-SD15, SDP_H, SDP_L	*Store Data Leads 0 Thru 15, Parity High, and Parity Low:* These leads are used to provide the means of reading the data from or writing the data into the address on leads SA0 thru SA19.
SA0-SA19, SAP_H, SAP_L	*Store Address Leads 0 Thru 19, Parity High, and Parity Low:* SAP_H — Parity on SA8 thru SA19. SAP_L — Parity on SA0 thru SA7. SA18, SA19 — Defines which one of the possible four main store circuits is to be accessed (only one main store circuit in No. 3 ESS so only one legal code). SA3 thru SA16 — Defines which bits on the memory chips within the defined modules are to be accessed for 16K-bit memory. SA15-SA17 — Defines which one of the eight memory modules within the defined store is to be accessed for 4K-bit memory. SA3-SA14 — Defines which bits on the memory chips within the defined modules are to be accessed for 4K-bit memory. SA0-SA2 — Defines which 4K chips will be enabled on each memory plane.
SERC	*Store Error C-Lead:* This signal is sent by the store to indicate that bad parity was detected on the word accessed. This signal will be sent in lieu of the SCM signal. The bad data and the address at which it is located will be present on the MASB at the time the SERC becomes active.
SMS	*Store Maintenance State:* This signal is sent by the 3A CC to its MAS to override the disabling of the I/O serial channel port from the other 3A CC. This signal will prevent a fault in the off-line 3A CC from interfering with the on-line diagnostics.
SAC	*Store Automatic Correction:* The SAC signal is sent to MASC during Block Double Store Read (BDSR) state. The MASC, when detecting a double parity error on read, complements the data and parity. Parity error signals are disabled.
SCW	*Store Complement Write:* Causes a word with a bad parity bit to be complemented and written into the address from which it was read. Parity bits are also complemented. Write-protect check is disabled in SCW mode. The 3A CC sends SCW signal when required during simplex mode.

TABLE B

MNEMONIC AND FUNCTIONS OF THE MAIN MEMORY STATUS REGISTER (MMS)

BIT	MNEMONIC	FUNCTION
0-1	MM1	MEMORY MAINTENANCE: Used with MM2 and RW to formulate the command sent in a memory operation.
2-3	MM2	MEMORY MAINTENANCE: Used with MM1 and RW to formulate the command sent in a memory operation.
4-5	RW	READ OR WRITE: Indicates whether memory is to perform a read (logical one) or a write (logical zero) operation.
6	IDL	IDLE: If set, disables all communications to the other 3A CC memory.
7	IDL	IDLE: Complement of bit 6. If set, disables all communication from other 3A CC memory.
8-9	UPD	UPDATE: Indicates whether or not to update the off-line memory.
10-11	ISO	ISOLATE: Prevents the other 3A CC from accessing the memory of this 3A CC.
12-13	BDSR	BLOCK DOUBLE STORE READ: Inhibits double store read.
14	CR	COMPLEMENT WRITE: Activates complement write lead of main store bus; main store controller will have last word, and store in the complement in the last read address.
15	BEC	BLOCK ERROR RECOVERY: Inhibits all error recovery procedures within the 3A CC associated with incorrect store read data.
16	CW	Same as bit 14.
17	BEC	Same as bit 15.

DR flip-flop. This permits the DR flip-flop to be tested by microcontrol.

3.16 The ***instruction or data (ID) flip-flop*** indicates whether the memory cycle being issued is an instruction type or data type. If the ID flip-flop equals one, the word returned from the MAS is put into the SIR. If it equals 0, the returned word is put into the SDR register. The ID flip-flop is also used to determine the state of the signal control 3 (SC3) lead on the MASB. This lead determines whether the cycle being issued is a read or write cycle. If the ID flip-flop is equal to one, a read is requested independently of the read-write (RW) flip-flop. This allows the RW flip-flop to set independently of the present state of the PBC. The ID flip-flop equals to one also determines whether the SAR is gated into the PA register at the start of the memory cycle so that the PA+1 logic can compute the next sequential address for the following instructions.

E. 3A CC MASB Duplex Operation

3.17 To connect each 3A CC onto both MASB 0 and MASB 1 in a duplex configuration, two PBC units for each 3A CC are required. This is due to the self-checking capability of each 3A CC.

MMS BITS			MASB LEADS SC3 - SCO 2-OUT-OF 4 DECODED BITS				
0,1	2,3	4,5					
MM2	MM1	RW	SC3	SC2	SC3	SCO	DESCRIPTION
0	0	0	0	0	1	1	NORMAL STORE WRITE
0	0	1	1	1	0	0	NORMAL STORE READ
0	1	0	1	0	0	1	READ - WRITE PROTECT REG
0	1	1	0	1	1	0	WRITE - WRITE PROTECT REG
1	0	0	0	1	0	1	SPARE - BLIND WRITE
1	0	1	1	0	1	0	SPARE
1	1	0	0	0	1	1	WRITE - LOCK STATE
1	1	1	1	1	0	0	READ - LOCK STATE

MM - MAIN MEMORY

A - 8 POSSIBLE STATES OF MAS COMMANDS

BEC	CW	BDSR	BDSR	ISO	ISO	UPD	UPD	IDL	IDL	RW	RW	MM2	MM2	MM1	MM1	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BITS

BEC - BLOCK ERROR RECOVERY
BDSR - BLOCK DOUBLE STORE READ
CW - COMPLEMENT WRITE
ISO - ISOLATE
IDL - IDLE
MM - MAIN MEMORY
R-W - READ-WRITE
UPD - UPDATE

B - MMS REGISTER LAYOUT

Fig. 13—Main Memory Status (MMS) Register Layout

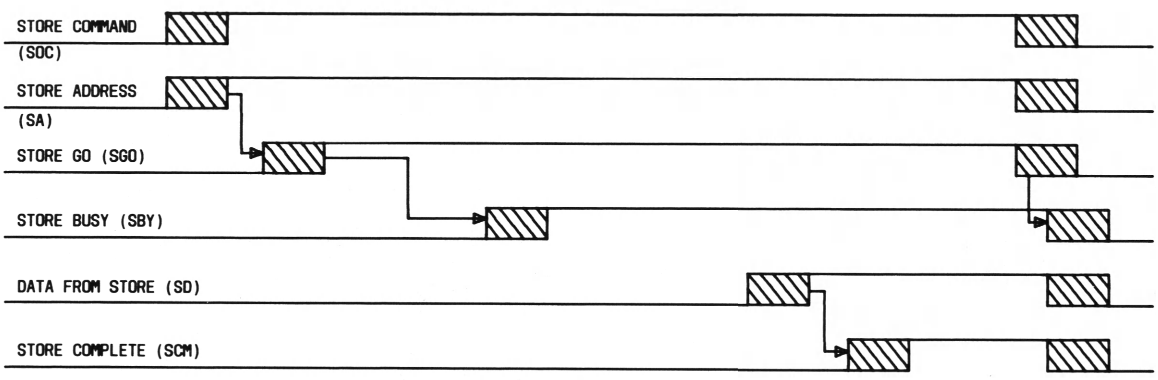
The off-line 3A CC is not kept in sync with the on-line 3A CC. Under normal conditions, the on-line 3A CC must keep a redundant copy of the memory contents in the off-line store. This is normally done using the update mode of a PBC by issuing concurrently all write commands from the on-line 3A CC to both MASs. Also for maintenance purposes, read or write data can be issued to either MAS from a given 3A CC. In order to issue store commands to either or both MASs, one PBC is associated with each MASB.

F. MASB Sequencing

3.18 Since the 3A CC operates asynchronously with the MAS, the only MASB timing requirements are related to the sequence in which signals are generated. This process involves interaction between the 3A CC and MAS unit during a memory cycle. Timing on the MASB during a normal read cycle is illustrated in Fig. 14.

3.19 After the active PBC has determined the bus is free, it issues a ***seize*** signal and gates store address (SA), the store data (SD) (if write command), the store command signal (SC), and store go (SGO) signal onto the bus. The ***seize*** signal reverses the use of the MASB for the duration of the memory cycle, thus preventing any interference from the other processor. The gating path used by the SGO signal contains sufficient delay to ensure that the SDO and SA information is present on the bus before the SGO signal becomes active. These signals are maintained until the active 3A CC has buffered the MAS response initiated by the store complete signal (SCM).

3.20 Removal of the SGO signal is used to inform the MAS that the 3A CC has processed the MAS response. After the MAS has received a



NOTE:
CROSS HATCHED AREAS REPRESENT
TIMING VARIATIONS IN THE SIGNALS

Fig. 14—Main Store Bus (MASB) Sequencing

1-to-0 transition on the SGO signal and has performed any required clean up processing, it removes the store busy (SBY) signal to indicate it is ready to process a new MAS request. The only requirement as to when the SBY signal is activated by the MAS is that it must precede the store complete (SCM) signal, because the presence of the SGO signal will prevent access by the off-line 3A CC which is on the MASB between the on-line 3A CC and its MAS.

G. Accessing Off-Line MAS

3.21 A normal read is issued by the on-line 3A CC to its associated store via the PBC. For example, in Fig. 11A if 3A CC 0 is on-line, the read is issued via PBC 0 to MAS 0. The PBC associated with the off-line store (PBC 1) does not issue a read command out on the store bus. It does, however, duplicate many of the functions for this read cycle that are performed in PBC 0. In this way, error detection can be achieved by the matching of the two PBC operations. For write commands in which the system is in the UPDATE mode, both PBCs perform the identical functions and issue write commands out onto their respective store buses.

3.22 In addition to the normal read of the on-line store, the 3A CC can issue read commands to the off-line store with the use of special commands. These commands, via microcode, change the contents of the main memory status (MMS) register which contains two bits, called the IDLE bits. These bits define which PBC, 0 or 1, is to be active for a given memory cycle. It is these two bits that the "read other store" command complements so that a read can be issued to the off-line store instead of the on-line store. At the termination of the "read other store" command, the microcode must return the MMS to its previous state. It should be noted that on normal read commands to the on-line store the MMS is not affected.

H. Write-Protect Feature

3.23 Write-protect (WP) is provided on 4K address block increments and is implemented by circuitry within the MASC. The MASC contains a register with a bit for each 4K block. If the 3A CC issues a write to an address that has been write-protected by the MAS WP circuitry, the MASC will issue a write protection error (store error B) to the 3A CC, and appropriate action will be taken.

3.24 The ability of the 3A CC to access and change the state of the WP register is provided by two of the states of the MASB control leads (SC3 to SC0). These control states are a function of the MMS register in the 3A CC (Fig. 13). Once the MMS is loaded, the WP registers can be changed via a normal write cycle to the MASC; ie, an address is loaded into the SAR that corresponds to the correct WP register. There are four 16-bit registers for each MASC. The contents to be written into the WP register are obtained from the contents loaded into the SDR. With the register loaded, the write is performed exactly the same as a normal write cycle between the 3A CC and the MASC.

I. Error Detection

3.25 Error signals are divided into four types:

- Those which result in a switch to the other 3A CC
- Those which cause an automatic retry of a MAS read operation
- Those which store parity error
- Those which cause an interrupt.

Table C identifies bit designations and functions of the error register (ER). The error signals which result in a switch are in the ER bits 0 through 9; bits responsible for hardware initialization are ER bits 11 through 13; and the bits that result in an interrupt are ER bits 14 through PH. Bit 10 indicates a MAS read parity error. The signals from bits 0 through 9 are ORed together, and the resulting signal is gated with the block hardware check bit. This resulting signal is ORed with the switch message from the program timer. This signal is then used to stop the 3A CC and send a switch message to the other 3A CC. When the 3A CC is locked on-line (LON=0), the system is initialized instead of switched. The signals from bits 11 through 13 are ORed together, gated with the block hardware check bit, and sent to the hardware initialization circuit. The signals from bits 14 through PH are ORed together, then sent directly to the interrupt set register (IS). For maintenance reasons, an interrupt level can be blocked by setting the corresponding interrupt mask bit. If bit is set, either a double store read is attempted or a complement correction cycle is initiated in an effort to obtain the failing memory location.

J. Double Store Read

3.26 The double store read (DSR) technique is used to recover from failures that occur in the memory cell. The DSR uses the reception of the SERC signal to set ER bit 10 and to reverse the output state of the IDLE flip-flop. This redirects the read that is first given to the on-line MAS over the off-line MAS. The SERC signal indicates a parity error on a read command, and the MASC sends this signal to the 3A CC instead of the SCM signal. When the read is redirected to the off-line MAS, the PBC gates the accessed data from the off-line MASB into the appropriate registers. The cycle is completed by the SCM signal from the off-line MAS, and as far as the 3A CC is concerned, it is unaware that the data it accessed came from the off-line 3A CC.

K. Complement Correction

3.27 There are significant periods of time when the off-line MAS is unavailable, ie, recent change procedures for translation data updates which require the 3A CC processor to be placed in the simplex mode. Complement correction is used to correct memory locations when in the simplex mode. Complement correction depends upon the failing memory cell to be stuck in the wrong state. The nonfailing bits of the word are complemented, and hence the data is stored in a connected (but complemented) form. The SERC signal, together with the fact that the DSR mode is blocked, will cause the 3A CC to invoke a microsubroutine to perform the actual complement correction function.

MAINTENANCE CHANNEL

3.28 The maintenance channel (MCH) interconnects and provides communication between the 3A CCs. It is a serial 6.67 MB/S data transfer system that consists of two identical controllers, one located in each 3A CC. Each MCH controller is connected to the other by two coaxial cables. One cable is used for transmitting and the other is used for receiving information (Fig. 12). The MCH system is operated in half duplex mode in which only 1-way transmission is permitted at a given time.

A. MCH Configuration

3.29 Basically the MCH controller consists of a transmit-receive register (MCHTR), an MCH command (MCHC) register, an MCH buffer (MCHB) register, sequence and control logic, gating circuits, error check circuits, and a command decoder which decodes the command portion of the received message. The MCHTR, MCHC, and MCHB are designated as "special" registers and have access to the 3A CC gating bus. These registers interface with the 3A CC via the normal of register-to-register commands.

B. MCH Registers

3.30 The MCHC register is an 8-bit shift register which has parallel access to the 3A CC gating bus. It transmits to the MCHC in the off-line 3A CC. This register contains a start bit and the 3-out-of-7 operation code executed by the MCH. Functioning with the MCHC is the 22-bit MCHTR shift register. The MCHTR is loaded via the gating bus. It has access to the MCHB and receives from the off-line MCHTR. The MCHTR register accepts the data portion of the MCH message. MCHTR and MCHC registers make up a single 30-bit shift register (Fig. 15B). The combined shift registers, under control of the main sequencer, serve as the MCH transmit register and serve as the receive register in processing data and commands between the 3A CCs.

3.31 The MCH message format (Fig. 15B) shows a 22-bit data field including P_H and P_L. Other data fields may be used. For 16-bit data fields, the high 4 bits of the data high field are not used. For 12-bit data fields, only the high data field is used with its P_H bit. Data field loading is determined by the destination of the command to be transmitted.

3.32 The 22-bit MCHB register (Fig. 15A) buffers incoming or outgoing data, which is gated to or from any internal register within the 3A CC.

C. MCH MAS Transmit Sequence

3.33 In normal operation, a transmission is initiated by software. Figure 16 is an outline of

➧ TABLE C ➧

TYPICAL ERROR REGISTER (ER) FUNCTIONAL ASSIGNMENTS

BIT	MNEMONIC	DESIGNATION	FUNCTION
0	TODER	To Decoder Error	
1	FRMDER	From Decoder Error	
2	IBER	IB X, Y Field Error	
3	BUSER	BUS Parity Error	
4	DMLER	DML Match Error	Error which results in a switch off-line unit
5	MARER	MAR Parity Error	
6	CLKER	Clock Error	
7	MSTRER	My Store Error A	
8	MADER	MAR — RAR Match Error	
9	FRER	Function Register Parity Error	
10	SRPE	Store Read Parity Error (Error C)	Main store parity error
11	MSTWRP	My Store Write Protect Error (Error B)	Error which results in an interrupt
12	MFSTER	My Store Fast Time-Out Error	Responsible for hardware initialization-MRF error
13	BAER	Branch Allowed Error	
14	OWRTER	Other Store Write Protect Error	
15	OSTRER	Other Store Error	
16	OFSTM	Other Store Fast Time-Out Error	
17	IOMLTER	I/O Multiple Channel Select Error	Error which results in an interrupt
18	PTRER	PT Reset Received by On-Line CC Error	
19	SWER	Switch Received by On-Line CC Error	
PL	IOER	I/O Channel Error	
PH	IOPARER	I/O Bad Parity Received Error	

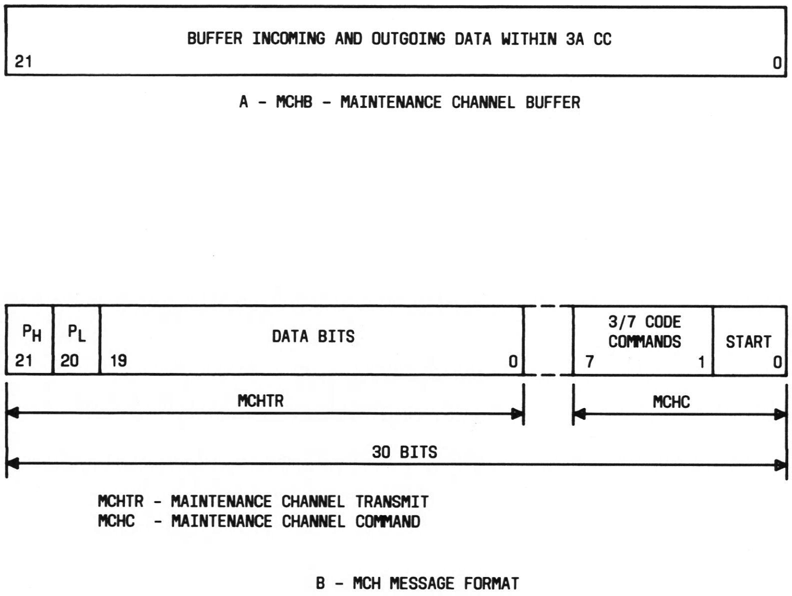


Fig. 15—Maintenance Channel (MCH) Register Layout

steps which are necessary in order to send a message over the MCH.

3.34 Software can override the MCH operation at any time in the transmit sequence by issuing an idle MCH microinstruction. A command of this type will result in the direct initialization of the MCH controller in the on-line 3A CC and will indirectly initialize the MCH controller in the off-line 3A CC. If, by reason of a failure in the MCH circuitry, normal interprocessor communication is lost, the interrupt facility may be used as backup to perform limited functions. A special interrupt attempt (level 7) is assigned as an interrupt from the other 3A CC. If the MCH fails, this interrupt is activated, and the interrupted 3A CC looks in its associated MAS for information that has been written by the other 3A CC.

3.35 Transmissions via the MCH are initiated by either 3A CC independent of on-line/off-line status. There are no priorities in obtaining access to the MCH by either the on-line or off-line 3A CC. The first to obtain the MCH has preference. The on-line 3A CC is, however, protected by inadvertent orders over the MCH from the off-line by hardware inhibits. The off-line 3A CC must make an ordered sequence of transmissions in order to affect the on-line 3A CC, thus preventing a malfunctioning off-line machine from interfering with an operational 3A CC. The MTCE transmission link is seized and controlled by the 3A CC/MCH controller making the first request. The initiating MCH controller serves as the master controller and the other MCH controller will become a slave to the master controller. The two MCH controllers are ac-coupled to provide isolation, thereby preventing hard faults in one processor from affecting the other. These controllers operate asynchronously, deriving the necessary clocking directly from the incoming data message bit stream. Some error detection is integrated into the design of the MCH, and parity is preserved in the transmitted message. An automatic transmission is initiated if a fatal error is encountered within the 3A CC. This transmission via the MCH coaxial leads results in the standby processor coming on-line to take over call processing.

D. MCH Functions

3.36 Approximately 23 functional commands are processed by the MCH. Some of the functions use bit-stream timing (BST) and other function commands use clock timing from the on-line 3A

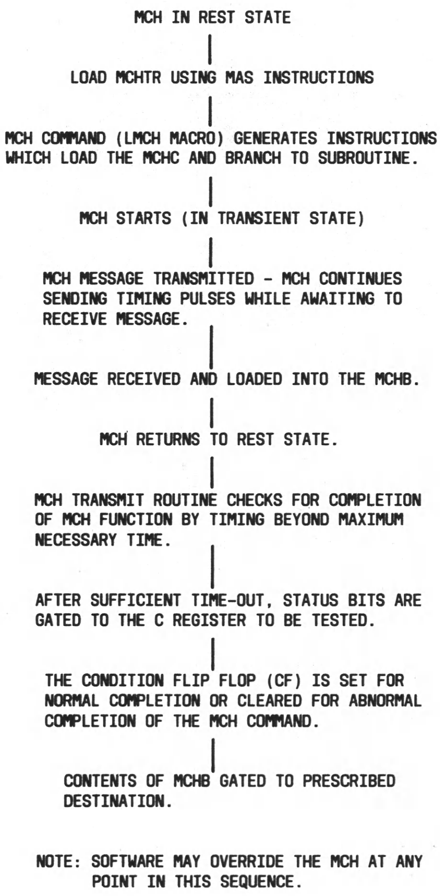


Fig. 16—Typical MCH MAS Transmit Sequence

CC. Types of functions processed by the MCH are:

1. Returns error register (ER), system status (SS) register, and miscellaneous bits from the other 3A CC
2. Loads and controls MCHB and MCHTR registers
3. Processes data to the microinstruction register (MIR) and microaddress register (MAR)
4. Transmits disable signals
5. Sets and resets flip-flops for system control
6. Updates the off-line program timer when used in normal call processing routine
7. Performs hardware initializations of the off-line 3A CC in order to switch it on-line
8. Controls system clock.

INPUT/OUTPUT CHANNELS/SUBCHANNELS

3.37 The I/O channels are another means of interconnecting and providing communication between the 3A CC and its periphery (Fig. 12). The I/O channels make up an asynchronous, serial (6.67 MB/S) data transmission system capable of sending and receiving 21-bit messages. Only one (I/O main channel 0) of a possible 20 main channels is used for the No. 3 ESS. However, since the 3A CC is designed for common system use, it is necessary to select channel 0 by the 3-out-of-6 main channel select code. This makes additional main channels available for growth in the No. 3 ESS. The 3A CC has a wired capability of 3 main channels (0, 1, and 2). Each main channel has 20 subchannels. The I/O channel functions processed at the 3A CC are accomplished by the input/output controller (IOC).

A. Input/Output Controller

3.38 The IOC consists of the I/O status register (IOS) and the I/O data register (IOD), the start code register (STRT), sequence and control logic, error check circuitry, and other intraprocessor gating paths.

3.39 The IOC registers interface with the 3A CC via three general registers; the control buffer (R9), the output buffer (R10), and the input buffer (R11). Figure 17 provides layouts of these registers.

B. Input/Output Registers

3.40 The IOS register consists of 12 bits, structured in two 6-bit fields, subchannel select (SCS) and sequencer control (SCTL) fields (Fig. 18A). The SCS field is loaded from R9 by a special set of control signals and contains the subchannel address. The flip-flops which make up the SCTL field are wired as a rotatable shift register (bits 5 through 0). This shift register may be jammed by a special set of 3A CC control signals to specific 3-out-of-6 code constants which identify the start of a particular control sequence to be followed. Part of the SCTL (bit 3 through 0) may also be loaded from R9 along with the remaining 2 bits (5 and 4) forced to a 01 pattern. The SCTL codes

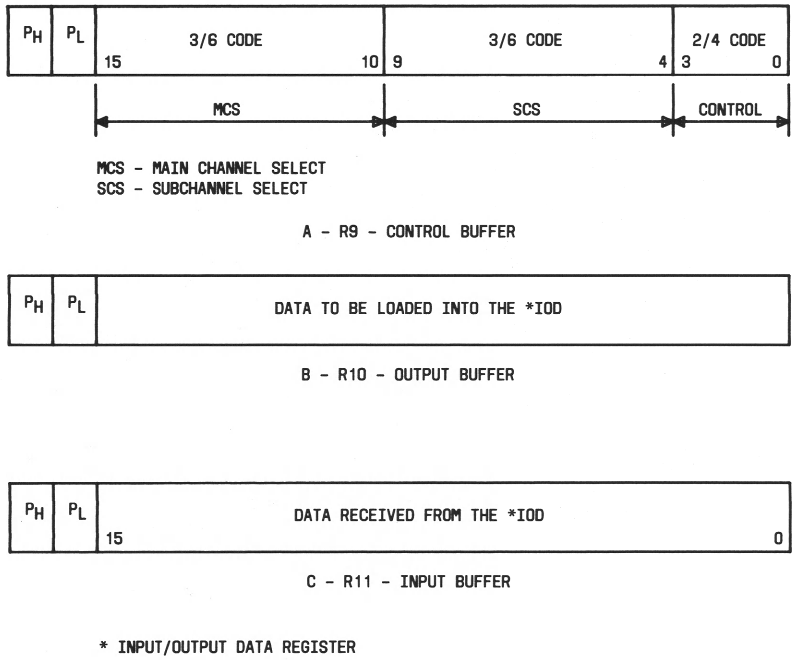


Fig. 17—Input/Output 3A CC Interface General Registers

loaded in this manner from R9 are 2-out-of-4 in order for the 6-bit SCTL field to contain a valid 3-out-of-6 configuration. The SCTL field functions as a sequence code generator within the operation of the IOC sequencer. For maintenance purposes, the IOS is unloaded to R11 via the I/O return data bus by exercising a particular sequence of control signals.

3.41 The IOD register functions as a transmit/receive buffer for the data portion of the I/O message (Fig. 18B). This register is parallel loaded from R10 via a special gating bus and is unloaded via the I/O return data bus to R11.

3.42 The STRT shift register consists of three bits at the low end of the IOD register to accommodate start codes. It is forced to specific bit configurations by particular control signals. This register cannot be gated into or gated from; it is strictly used as an internal IOD register. The IOD, together with STRT, makes up the single 21-bit input/output controller shift register.

C. I/O Subchannels

3.43 The I/O subchannels (IOSCs) provide direct channels of communication between the 3A CC, the MTCE frame units (Fig. 4) and the peripheral controllers (scanner, network, and peripheral pulse distribution Fig. 6 and 7). The IOSCs convey several types of information, including control signals, data for processing control signals, and the processing of maintenance information. Table D shows typical IOSC function assignments.

3.44 Each of the 20 IOSCs can address its periphery via a dedicated cable driver and cable receiver. Only one of the IOSCs can be activated at a given time since they share the common control and sequencing logic of the main channel.

3.45 A sequence of microinstructions issued from the microstore of the 3A CC is used to first load the IOSC and then to initiate an IOSC message. This instruction ultimately arrives at the cable driver. In operation, a 21-bit serial message is outpulsed to the selected peripheral unit and, in response, a 21-bit message is returned from the unit (Fig. 18C). Each message uses a 3-bit start code and an 18-bit data field. The data field includes two 8-bit fields and two parity bits. The message has even overall parity, with the two parity bits maintaining odd parity over their respective fields.

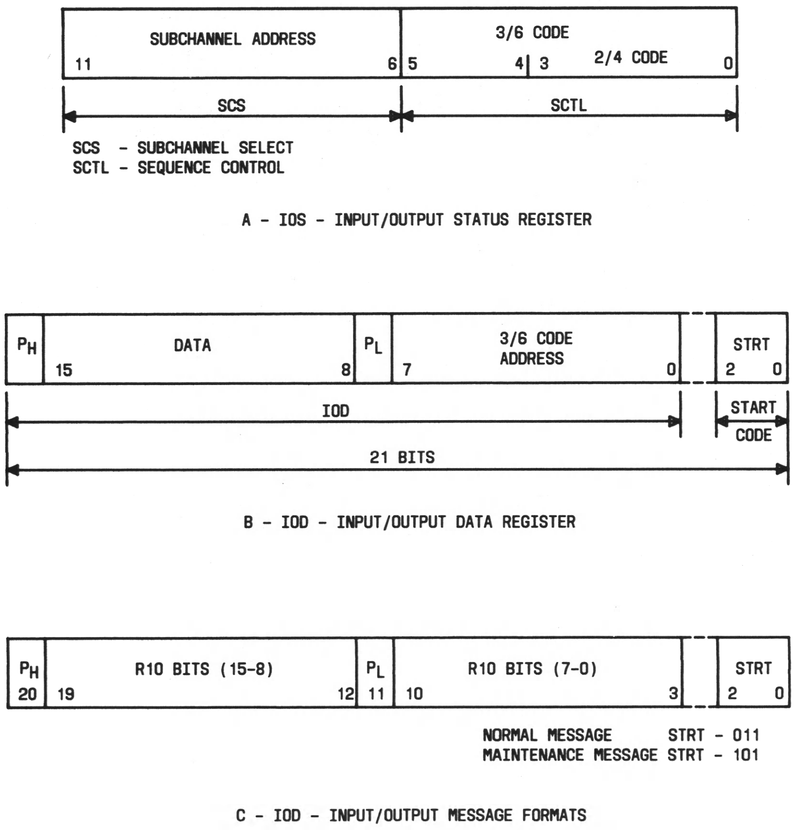


Fig. 18—Input/Output Controller (IOC) Registers

3.46 Two legal start codes are used for I/O messages. The 011 pattern is called the normal start code, and 101 the maintenance start code, as indicated in Fig. 18C. The IOC recognizes either of the two start codes and raises separate flags to the processor for identification.

D. IOC Sequencing

3.47 Autonomous control of the I/O channel is performed by the IOC sequencer. Once initiated, the sequencer directs the transmit/receive operation of the IOC without software intervention. The state diagram of the IOC sequencer is shown in Fig. 19. The IOC has three major operational sequences:

- Transmit receive maintenance
- Transmit receive normal
- Receive only.

The major states of these sequences are: idle, transmit, receive, and message complete. The sequences and states within the sequences are identified by unique 3-out-of-6 codes. The IOC sequence logic contains a 3-out-of-6 to 1-out-of-20 state decoder and the logic necessary to produce state change signals. An error detection circuit makes a continuous check on the states of codes as they are produced for protection against false sequencing.

E. IOSC/Functional Unit Interfaces

3.48 Each 3A CC I/O subchannel is normally interconnected to another unit in the system by two coaxial cables: a transmit cable and a receive cable. This is indicated in Fig. 20 between the MASCs, TDCs, TTYCs, SSPC, and to the FIOCs which are peripheral to the control complex. Note that the TDCs are duplicated for reliability and have separate I/O subchannels associated with each unit. The TTYCs, on the other hand, are duplicated but not for reliability. They provide

➧ TABLE D ➧

TYPICAL INPUT/OUTPUT SUBCHANNEL (IOSC) ASSIGNMENTS

IOSC	SYMBOL	ASSIGNMENT
0	SSP	System Status Panel
1	SPARE	Spare
2	TAPE 0	Tape Data Controller Unit 0
3	TAPE 1	Tape Data Controller Unit 1
4	SPARE	Spare
5	TTY 0	Teletypewriter Unit 0
6	TTY 1	Teletypewriter Unit 1
7	MAS 0	Main Store Memory (On-Line)
8	OMAS 0	Main Store Memory (Off-Line)
9	TTY 2	Teletypewriter Unit 2
10	TTY 3	Teletypewriter Unit 3
11	NWC 0	Network Controller 0
12	NWC 1	Network Controller 1
13	PPD 0	Peripheral Pulse Distributor 0
14	PPD 1	Peripheral Pulse Distributor 1
15	SPARE	Spare
16	LS 0 Thru 3	Line Scanner 0 Thru 3
17	LS 4 Thru 7	Line Scanner 4 Thru 7
18	LS 8 Thru 11	Line Scanner 8 Thru 11
19	LS 12 Thru 15	Line Scanner 12 Thru 15

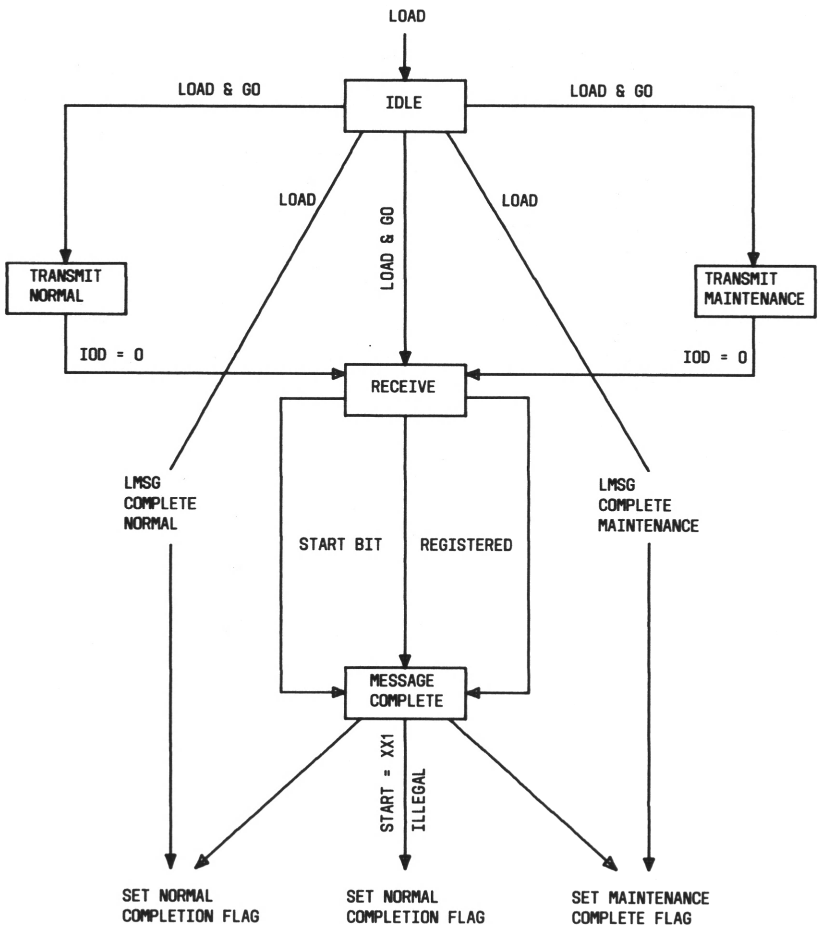


Fig. 19—Input/Output Controller (IOC) Sequence Chart

additional TTY ports, if necessary, for unique functions such as service order inputs. Leads to the FIOCs are the exception to the normal channel configurations. Paragraph 3.52 provides additional information.

3.49 The I/O subchannel leads interconnect the 3A CCs and MASCs to access the MASs for diagnostic purposes and to facilitate subchannel functions for duplex operation of the processors. Information sent to the MAS may be returned via the receive I/O subchannel by the 3A CC (loop around test) or the contents of the error register may be received to help isolate the trouble.

3.50 The I/O subchannels between the 3A CC and the TDCs access the tape data controller units. The tape system contains software information not stored in MAS as well as the same information in the MAS. These I/O subchannels provide the 3A CCs with the means to perform the functions of reading the tape contents or writing information onto the tapes as required to support system operation and maintenance.

F. TTY and SSP IOSCs

3.51 The I/O subchannel leads between the 3A CCs and TTYC access the TTY units. Similarly, I/O subchannel leads access the SSP via the SSPC. These leads provide an interface between the SSP (where manual input and output take place) and the rest of the system. The TTY is used to communicate with the 3A CC to perform administrative and maintenance type functions. See 3.58 through 3.65 for more detailed description of SSP interface.

3.52 Four I/O subchannels (Fig. 7) interconnect each 3A CC with its respective frame

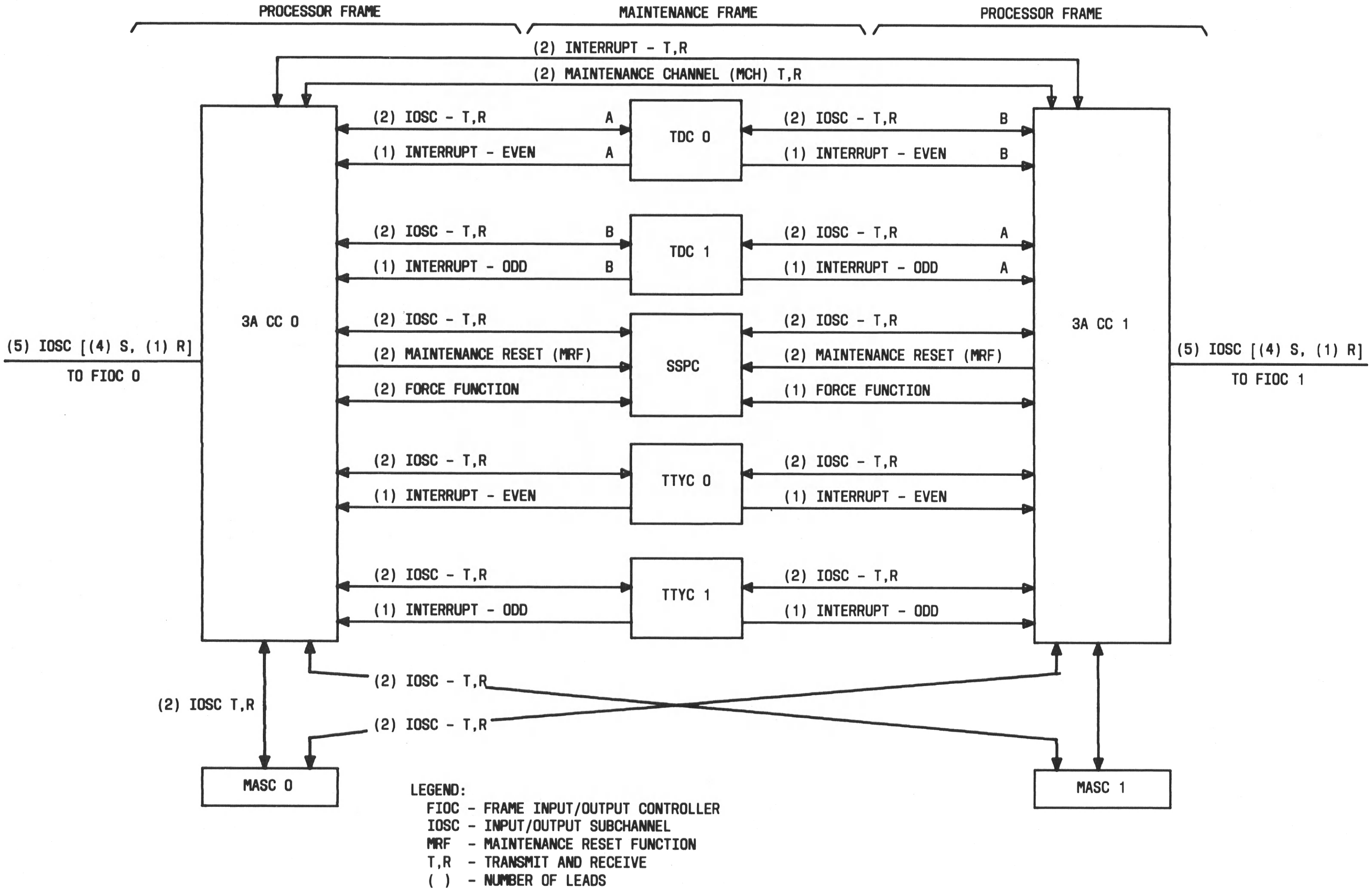


Fig. 20—Control Complex Control Leads

input/output controller via FIOCs (0 and 1) to provide the following: two transmit leads to communicate with the scanner matrix via the scanner controller, one transmit lead to communicate with the peripheral decoders via the peripheral pulse distribution (PPD), and one transmit lead to communicate with the switching network via the network controller. Only one receive lead via the FIOC is used as a common return to the 3A CC for the peripheral controllers.

INTERRUPT FACILITY

3.53 The interrupt facility (Fig. 12) selects 3A CC inputs based on system priority. Interrupt level programs break into the base level loop on a periodic timed basis or upon demand. When the interrupt level program has timed out or completed its allotted work, control is returned to the base level.

3.54 The purpose of the interrupt facility in the 3A CC is to provide a fast and efficient response to either critical timed functions or functions that occur infrequently but must be serviced quickly. The interrupt facility thus allows the program to do normal base level work while waiting for the peripheral device response.

A. Interrupt Registers

3.55 The interrupt facility functions with peripheral units via the interrupt set (IS) and interrupt mask (IM) registers. Each of these registers contains 18 bits; 16 data bits plus parity bits P_H and P_L. Each data bit accounts for an interrupt level. The highest level of interrupt is bit 0, with priority decreasing to bit 15. The IM register functions to individually mask IS bits as part of the interrupt facility function. Table E shows typical IS register function assignments.

B. Interrupt Facility Function

3.56 Depending on the time of the interrupt relative to a microsequence, a period of up to one complete instruction sequence may elapse before an interrupt is acknowledged by miroprogram control. Monitoring or testing for an interrupt is performed at the end of each microinstruction sequence when all zeros are read out of the microstore. Before a new operation (OP) code is loaded into the microaddress register (MAR), the state of the interrupt lead is checked. If an unmasked interrupt is present and the block interrupt (BIN) flip-flop is not set, a hard-wired interrupt address is gated to the MAR before the previous memory fetch is completed. This address initiates a microstore routine that tests for the highest level of interrupt within the IS and translates the bit position of that interrupt to a data constant. This constant points to the main memory program which processes that type of interrupt. During this process, the microprogram control sets the BIN flip-flop which is used to block any additional interrupts from being serviced until the present interrupt is disposed of.

C. Interrupt/Functional Unit Interface

3.57 The 3A CC interrupt facility is interconnected to other units in the system by coaxial cables as indicated in Fig. 20. The interrupt facility shares circuits between tape data controllers 0 and 1 and teletypewriter controllers 0 and 1 as well as 3A CC 0 and 1.

SYSTEM STATUS PANEL

A. Introduction

3.58 The system status panel (SSP) provides visual status and manual control for a No. 3 ESS office (Fig. 21). The SSP, together with the maintenance TTY, provides the means of allowing the crafts person to communicate with the system. The SSP accepts manual inputs and translates them into signals recognizable by the system. System status is displayed in a manner to provide immediate and recognizable indication to the crafts person. The SSP functions are basically divided in two areas of service:

- System emergency manual control (SEMC) which is used to manually stabilize the system during an emergency. The SEMC portion of the SSP has several functions that require interaction of various keys and circuit logic.

- System status and control (SSC) which is primarily a display of system condition. Generally, the display reflects the state of the flip-flop memory elements in the SSP logic unit.

3.59 A common read-write 8-bit data bus is used for processing data between the various status and key memory elements, and the I/O circuit

➧ TABLE E ➧

TYPICAL INTERRUPT SET (IS) REGISTER ASSIGNMENTS

BIT	MNEMONIC	FUNCTION	SOFTWARE INTERRUPT
0	*	INTP A	
1	UTILI	Utility Interrupt (External) INTP B	INTe
2	*	INTP C	
3	ADMI	Address or Data Match	
4	*	INTP D	INTk
5	ERRI	Error Register (Internal)	
6	*	INTP E	INTj
7	OCCI	Other CC (External)	
8	5MSI	Hardware Interrupt (Timing Counter 5)	
9	TCI	Hardware Interrupt (Timing Counter 10)	
10	TTYEI	TTY and Tape-Even (External)	INTa/INTb
11	TTYOI	TTY and Tape-Odd (External)	INTc/INTd
12	*	INTP F	INTh
13	MANI	Manual Panel Execute	
14	*	INTP G	INTq
15	I	INTP H	INTf

*Symbols are defined in common system library.

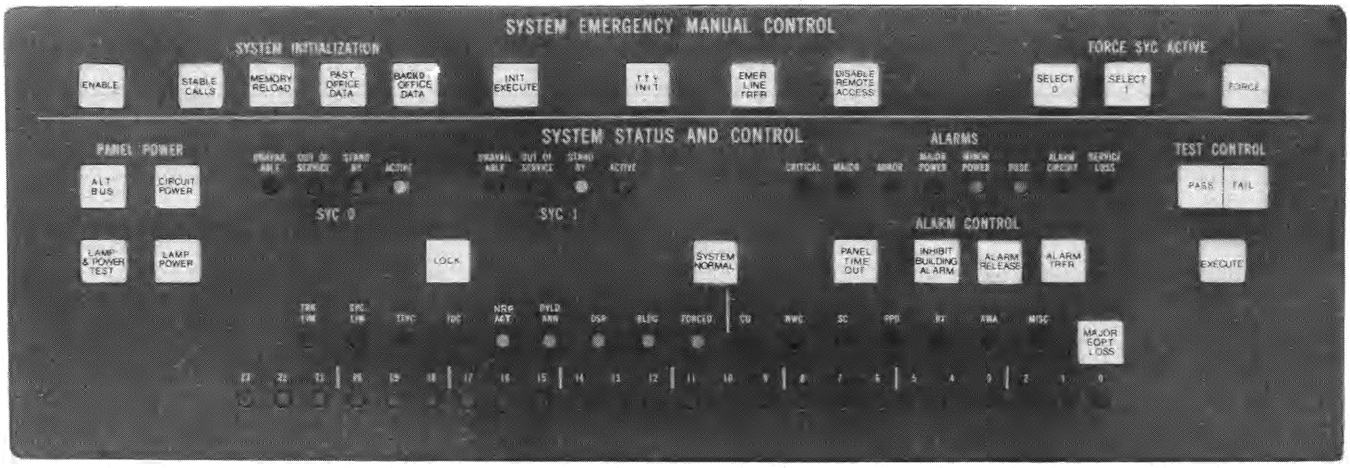
shift register. A 21-bit register is used to communicate between the SSP and the 3A CCs. This is accomplished by the 6.67-MHz serial I/O channel via coaxial cable (Fig. 22). Bipolar pulses are transmitted which are interpreted as positive or negative signals at the 3A CCs.

B. SSP/SSPC Circuit Configuration

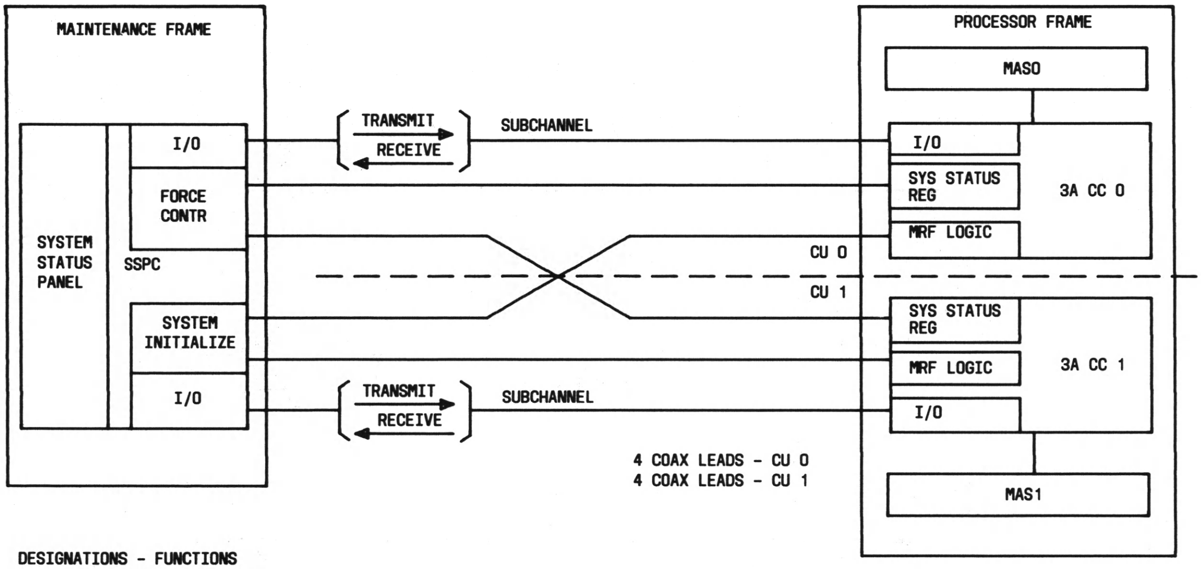
3.60 Flip-flops in the SSPC are used as memory elements which are grouped to form twelve 8-bit buffers. These buffers are used to store status and control information. Each buffer is program accessible via the serial I/O message from the 3A CCs. Most messages are program writable, and all are program readable. Only CIRCUIT POWER, LAMP AND POWER TEST, and LAMP POWER lamps and/or keys are not associated with a flip-flop memory element.

C. SSP/SSPC Key Buffers

3.61 The four 8-bit key buffers have external inputs. They can be set or reset by keys



◆Fig. 21— System Status Panel (Panel for No. 3 ESS Application Shown)◆



DESIGNATIONS - FUNCTIONS
CU - CONTROL UNIT (0 AND 1)
FCU01 - FORCE CUO ON-LINE & FORCE CU1 OFF-LINE
FCU11 - FORCE CU1 ON-LINE & FORCE CUO ON-LINE
MRFO, MRF1 - MAINTENANCE RESET FUNCTION SINGLE PULSE FOR SYSTEM INITIALIZATION

NOTE: DESIGNATIONS INDICATE LEAD FUNCTION AS DEFINED THEY DO NOT NECESSARILY REPRESENT CIRCUIT LEAD NAMES

Fig. 22—SSP Signal and Control Leads

on the SSP (eg, manual initialization, SEMC) or other external inputs. Table F shows assignments, SSP functional name, and the designated area location on the SSP. This will assist in defining the types of system functions indicated and controlled at the SSP.

D. SSP/SSPC Status Buffers

3.62 The eight 8-bit buffers are associated with system status and are set or reset by program control. Status buffers 0 through 4 indicate system control and status. Status buffers 5 through

TABLE F

SSP KEY BUFFERS — BIT ASSIGNMENTS

BIT	KEY BUFFER	SSP FUNCTIONAL NAME	SSP FUNCTIONAL AREA
0		* Enable	System Emergency Manual Control (SEMC)
1		LOCK	Select SYC 0 or 1
2		SELECT 0	SEMC
3	0	SELECT 1	SEMC
4		TTY UNIT	SEMC
5		EXECUTE	TEST CONTROL
6		* MEMORY LOAD	SEMC
7		Spare	SEMC
0		LOCK P	
1		FORCE	SEMC
2		FAIL	TEST CONTROL
3		PASS	TEST CONTROL
4	1	DISABLE REMOTE ACCESS	SEMC
5		ALTERNATE BUS	PANEL POWER
6		SERVICE LOSS	
7		* INITIATE EXECUTE	SEMC
0		Critical	Status Lamp
1		Panel Timeout	Autonomous Timer
2		Spare	
3		Spare	
4	2	Spare	
5		MINOR (Audible)	Alarm (Bell)
6		MAJOR (Audible)	Alarm (Gong)
7		CRITICAL (Audible)	Alarm (Gong)
0		EMERGENCY LINE TRANSFER	SEMC
1		Spare	
2		INHIBIT BUILDING ALARM	ALARM CONTROL
3		ALARM TRANSFER	ALARM CONTROL
4	3	ALARM RELEASE	ALARM CONTROL
5		* STABLE CALLS	SEMC
6		* PAST OFFICE DATA	SEMC
7		* BACKDATE OFFICE DATA	SEMC

* Used for system initialization

7 control LEDs on the SSP numbered 0 to 23. These serve as a display for information requested by TTY input message. Table G will assist in identifying usage of system status indications.

E. SSP Register

3.63 Since the SSP I/O message register communicates with 3A CC I/O message register, it also comprises 21 bits in the same configuration as the 3A CC I/O message register (Fig. 18C). The start code is always 011 while the operation (OP) code is a 01 for a write-read operation. This writes data into the SSP flip-flop memory, as addressed from a 3A CC. The data is read and transmitted back to the 3A CC for comparison. The OP code 10 is used for a read only operation. A nonnormal start code or bad

TABLE G

SSP STATUS BUFFERS – BIT ASSIGNMENTS

BIT	STATUS BUFFER	SSP FUNCTIONAL NAME	FUNCTIONAL AREA
0 1 2 3 4 5 6 7	0	ACTIVE (SYC 0) STANDBY (SYC 0) OUT OF SERVICE (SYC 0) UNAVAILABLE (SYC 0) ACTIVE (SYC 1) STANDBY (SYC 1) OUT OF SERVICE (SYC 1) UNAVAILABLE (SYC 1)	SYSTEM CONTROL
0 1 2 3 4 5 6 7	1	Building Power SYC Spare (Critical Indicator) Peripheral A Peripheral B SERVICE LIMIT TRAFFIC LIMIT Spare	Major Equipment
0 1 2 3 4 5 6 7	2	Miscellaneous (MISC) Auto Message Accounting (AMA) Ringing & Tone Plant (RT) Periph. Pulse Distr. (PPD) Scan. Controller (SC) Network Controller (NWC) Control Unit (CU) FORCED	Major Equipment
0 1 2 3 4 5 6 7	3	SYSTEM NORMAL MAJOR EQUIPMENT LOSS ALARM CIRCUIT MAJOR POWER MINOR POWER MINOR MAJOR FUSE	Major Equipment
0 1 2 3 4 5 6 7	4	Building (BLDG) Dynamic Service Protect (DSP) Overload Announce (OVLD ANN) Spare (Nonresident Program Active) Tape Data Controller (TDC) TTY Controller (TTYC) Service Limit (SVC LIM) Trunk Limit (TRK LIM)	Other
7-0	5		Status Display, LED 7-0
7-0	6		Status Display, LED 15-8
7-0	7		Status Display, LED 23-16

parity causes the message just received to be retransmitted to both 3A CCs with its start code set to maintenance (101).

F. Manual System Initialization

3.64 Manual system initialization can provide an example of functions which can be performed at the SSP. Keys used to perform a manual system initialization can be identified in Fig. 21 as EMERGENCY MANUAL CONTROL KEYS (SYSTEM INITIALIZATION). Key/lamps associated with system initialization are:

- ENABLE
- STABLE CALLS
- MEMORY RELOAD
- PAST OFFICE DATA
- BACKDT OFFICE DATA
- INIT EXECUTE.

Operation of the ENABLE key manually enables control of other system initialization functions. Operation of the STABLE CALLS key provides a manual request for an initialization level which will clear all stable and transient calls. Operation of the MEMORY RELOAD key manually requests an initialization level which will "bootstrap" from tape into MAS a copy of generic program and the first copy of office data. The PAST OFFICE DATA key is used to request an initialization level which will load from tape into MAS the most recent of two backup copies of office data. By depressing both MEMORY RELOAD and PAST OFFICE DATA keys, the initialization level will load the generic program as well as the most recent backup of office data. BACKDT OFFICE DATA is the same as PAST OFFICE DATA except the oldest backup copy of office data is selected instead of the most recent backup copy. Operation of the INIT EXECUTE key manually forces a system initialization. It causes a single initialization pulse to both control units (MRF pulse) to be generated. Key buffer register bits light the associated key/lamp on the SSP. Figure 23 shows the basic initialization sequence. To abort initialization before operating the INIT EXECUTE key, manually reset all keys.

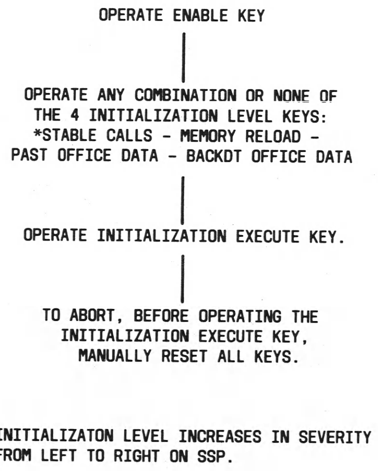


Fig. 23—Manual System Initialization Flowchart

3.65 Four SSP keys, STABLE CALLS, MEMORY RELOAD, PAST OFFICE DATA, and BACKDT OFFICE DATA select the initialization level. Severity increases from left to right in respect to the lamp/key positions on the SSP. If no initialization level key is operated, an initialization level is performed which clears all transient calls.

4. THEORY OF OPERATION—PROCESSOR POWER AND ALARM CIRCUITS

INTRODUCTION

4.01 The processor frame receives its power from a power distribution frame. Processor bay 0 is on power circuit A and bay 1 is on circuit B. Potentials of -48V and +24V are supplied to the processor frame power circuits (PFPC) where local fusing and further distribution to processor units are provided. Power modules (dc-to-dc converters) in the processor frame power unit (PFPU) derive the +3V and +5V potentials required by the 3A CC. The MAS and MASC also contain power converters required to provide their operating voltages.

POWER CONTROL

A. Power Control Sequencing

4.02 All converters are controlled via the power circuit in conjunction with the 3A CC control panel POWER key/lamp (Fig. 24). A +24V start (+24ST) signal is required to activate the converters.

These signals are provided via contacts on relays STA 0, STB 0, and STB 1. A 2-step (A and B) power-on sequence is used. Relay STA 0 operates when the POWER key is in the on position. The STA relay enables the A power converters. A timing circuit triggered by the STA relay then activates the STB relay. This allows the B converters to power up after the A converter has stabilized.

4.03 In powering up the 3A CC, there are two functions that must be performed to ensure the newly powered-up 3A CC does not interfere with normal operation.

(a) The I/O channel interface must be inhibited during the power-up transient state. This is performed by using the lock-off-line state (derived from the system status keys) to inhibit the I/O subchannels. Note that for normal powering up and down of the off-line 3A CC, it should be locked off-line. Thus, the power converters that are enabled by the STA relay power up the locked-off-line associated circuitry (as well as a small amount of other circuitry) in the 3A CC. This provides an inhibit signal starting in the first part of the power-up sequence. Then the power is enabled to the B converters which, in turn, enable the power to the I/O subchannels (as well as the remaining circuitry in the 3A CC). This inhibit signal will be maintained until the lock-off-line function is removed.

(b) The second function that must be performed by the power-up sequence is to initialize the off-line 3A CC to a static state. This is performed by jamming the microcontrol to an initialization address. The microcontrol will be held in this starting address until the B converters have stabilized and then a contact closing the STB relay will result in allowing the microcontrol to begin executing an initialization sequence. This sequence is very fast (3 μsec) and depends only on the operation of the microcontrol. The result of this sequence is to initialize the powered-up 3A CC and put it into "halt loop." The halt loop is the normal state of an off-line 3A CC.

4.04 When powering down, the off-line 3A CC is again assumed to be in the locked-off-line state, and the reversed sequence of the STA and STB relays is initiated. Thus, the B converters power down first with the inhibit signal coming from the locked-off-line circuitry (powered by the A converters) preventing any outputs from the I/O subchannel during the power-down sequence. No attempt is made to control the microcontrol sequencing when powering down. Figure 25 shows a power-down sequence and Fig. 26 shows a power-up sequence.

4.05 Circuit operating voltages (+3V, +5V) are controlled by the 3A CC control panel power key; however, the -48V and +24V associated with power (input to the converters, reference circuits and indicators) are not. ***These voltages will be present in various processor frame units when the POWER key/lamp indicates power is off.***

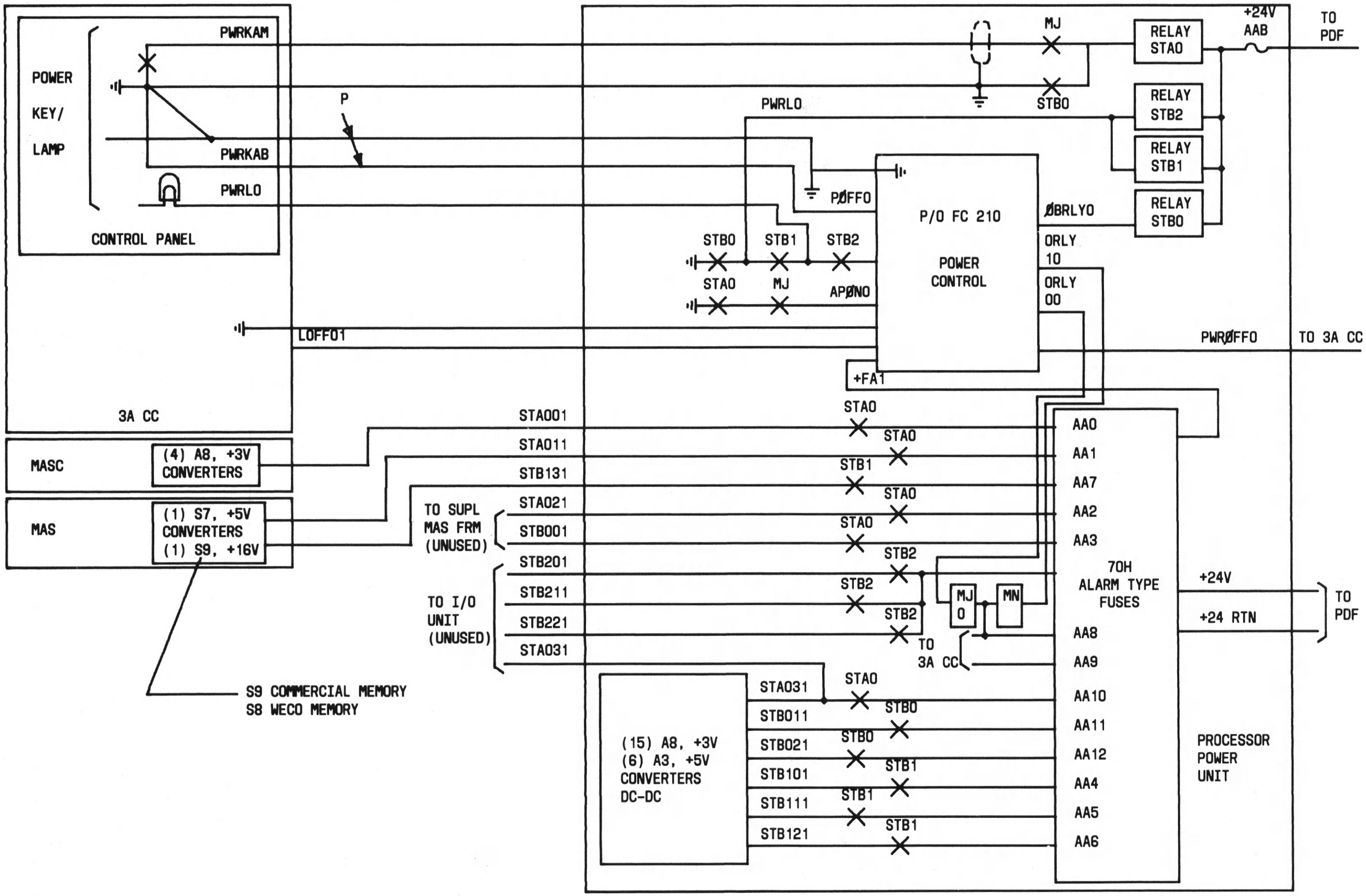
4.06 The power circuit has an interlock to prevent accidental removal of power from the on-line processor. A control signal from the 3A CC can prevent power shutdown independent of the POWER key when the processor is on-line.

B. +3V Power Distribution

4.07 The dc-to-dc converters equipped in the PFPU supply +3 volts required by the 3A CC logic. Regulation to within ±0.1 volt is achieved by sensing and filtering at the load (Fig. 27). An FB152 CP located in the 3A CC supplies a +12 volt reference from +24 volts for the +3 volt converters in the processor frame. An element of an FC21 CP also located in the 3A CC provides local filtering, monitors the +3 volts at the load, and derives a +3 volt reference from the +12 volt reference. Each FC21 CP contains two elements; therefore, each FC21 CP serves two J87389F converters. Each +3 volt converter can supply up to 5 amperes. The 3A CC requires a minimum of 12 converters to supply its +3 volt requirements. The PFPU is designed to accept additional converters for growth.

C. +5V Power Distribution

4.08 Other dc-to-dc converters equipped in the PFPU supply +5 volts to the 3A CC microprogram store, control panel LEDs, and MASM termination circuits. Local sensing and filtering at the converter, instead of at the load, and an internal reference are employed with the converters. This provides the capability to maintain the voltage at the load within ±0.5 volts. Each +5 volt



Note: For purposes of clarity, the alpha character "0" is slashed when it appears in combination with numeric zeros.

Fig. 24—Processor Frame Power Control and Fuses

POWER ON

OPERATE CKT PWR KEY TO
OFF POSITION

POWER OFF*
NO START SIGNALS TO
ASSOCIATED CIRCUITS.
PWR LAMP GOES OUT

3A CC HOLDS IN INITIALIZED
STATE WHEN POWER COMES
BACK ON

NO MAJOR ALARM UNLESS AN
ALARM CONDITION EXITS

*IF CONDITIONS ALLOW POWER REMOVAL

Fig. 25—Power-Down Sequence

OPERATE CIRCUIT POWER KEY.

RELAY STA0 OPERATES. +24 VOLTS AVAILABLE
TO ASSOCIATED CIRCUITS.

500 MS TO 2-MINUTE DELAY.

WHEN TIMED OUT, STB0 OPERATES. +24 VOLTS
SUPPLIED TO ASSOCIATED CIRCUITS.

RELAYS STB1 AND STB2 OPERATE. +24 VOLTS
SUPPLIED TO ASSOCIATED CIRCUITS. MICROCONTROL
IS JAMMED TO STARTING INITIALIZATION
ADDRESS.

POWER LAMP IS LIGHTED ON 3A CC CONTROL PANEL.

500 MS TO 2-MINUTE DELAY.

WHEN TIMED OUT, POWER CONTROL LEAD TO 3A CC
GOES HIGH. ALL CIRCUIT POWER STABILIZED.
MICROCONTROL PERFORMS INITIALIZATION.
(3 MICROSECONDS)

3A CC NO LONGER HELD IN INITIALIZED STATE.
NORMAL POWER ON.

MICROPROGRAM IN HALT LOOP.

Fig. 26—Power-Up Sequence

converter can supply up to 5 amperes. An additional +5 volt converter is required for each 1K words of microstore in the 3A CC. The basic PFPU is equipped with three +5V converters.

FUSES

4.09 All units in the processor frame are fused at the PFPU (Fig. 24). Positive 24 volts is supplied via 3/4-ampere alarming-type fuses. Fuses are limited to 3/4 ampere to ensure that they will be blown by a fault in the circuit they feed before the main fuse in the PDF will blow. A blown alarm-type fuse puts +24 volts on the alarm bus via the operated alarm contact. This connects to the fuse alarm 1 network (FA1 net) where it causes a major alarm. All -48 volt fuses are 3-ampere fuses which will be blown by a local fault before the PDF main fuse. These are no-alarming fuses; however, each 3-ampere fuse is paralleled by a 1/2-ampere alarm-type fuse which performs the alarm function. An overcurrent in a circuit fed by this combination blows both fuses. Caution must be exercised to avoid having the 1/2-ampere alarm fuse in place without the load carrying 3-ampere fuse in place. If the load current is in excess of 1/2 ampere, the alarm fuse will blow. The alarm contact of a blown alarm fuse places -48 volts on the fuse alarm 0 network (FA0 net) which results in a major alarm.

ALARM CIRCUITS

4.10 Each converter provides an out-of-limits power alarm (PA) signal and an out-of-control fuse alarm (FA) signal. The FA signal can be due to a converter supplying excessive output current or being grossly out of voltage limits. The converter will shut itself down for an FA condition. The converter FA signal is powered by a +24V start lead and, therefore, goes away when power is shut down. However, a flip-flop in the PFPU holds the alarm condition until it is retired via the PWR RESET key after the trouble is cleared. An illuminated LED on the individual responsible converter accompanies either the PA or FA. The LED is extinguished by the PWR RESET key.

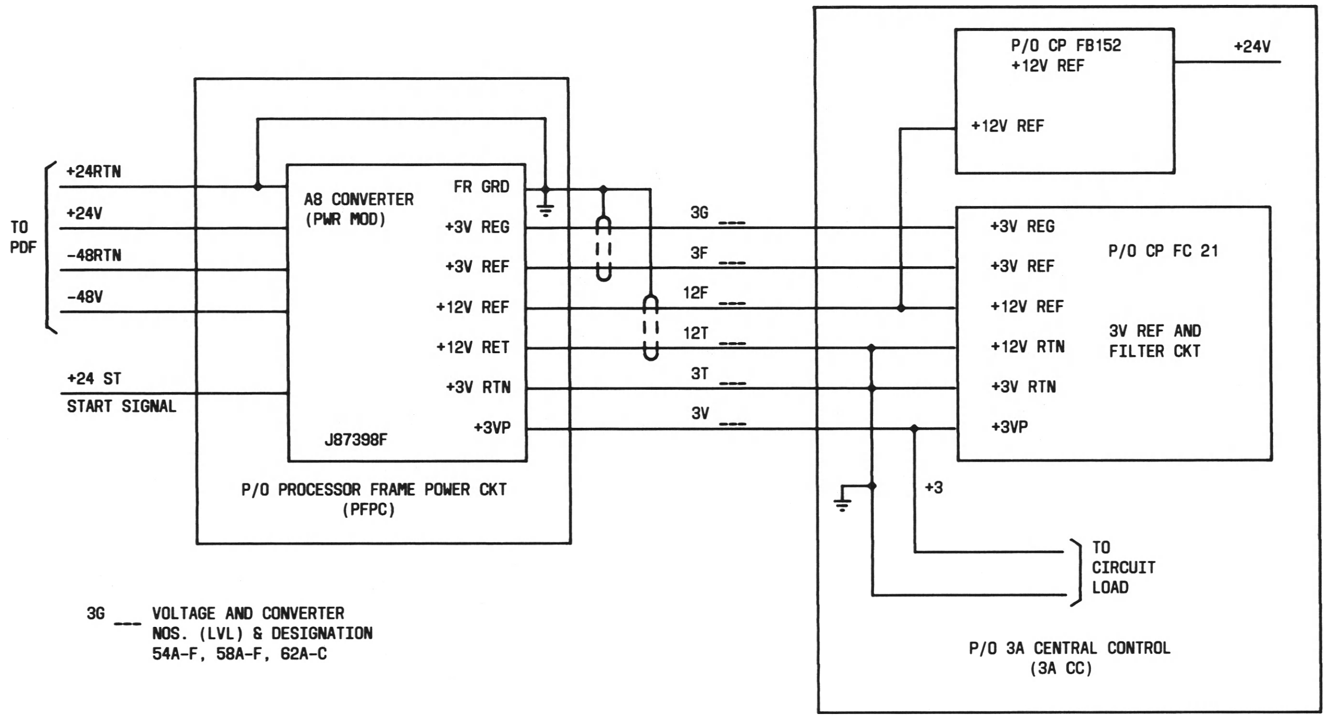


Fig. 27—Processor Frame Typical 3V Distribution

A. Major Alarm

4.11 The FA signal for all converters, the MAS and MASC 5V converter PA signals, plus the blown fuse signals are combined and detected by the PFPU. The combined signal is latched and converted to a major alarm. The major alarm is reported to the on-line processor via the scanner circuit and to the office alarm circuits. Since a portion of the processor can be without power when a major alarm occurs (due to a blown fuse or a converter shutdown), the PFPU removes processor power. Power may be restored when the trouble is cleared by operating the PWR RESET key on the PFPU panel.

B. Minor Alarm

4.12 The PA signal for all converters (except the 5V converters associated with the MAS and MASC units) are collected by the PFPU where it is latched and converted to a minor alarm signal. The minor alarm is reported to the on-line processor via the scanner circuit and to the office alarm circuit. The minor alarm is reset by the PWR RESET key on the PFPC panel.

C. Alarm Test

4.13 Response to a PA condition can be tested by circuits in the PFPU. A power alarm test (PAT) can be initiated by the 3A CC control panel LAMP AND POWER TEST key (Fig. 21). For a no-fault condition, the LED on each converter will be illuminated while the key is held and be extinguished when the key is released. This test can also be performed automatically by operating a decoder point and monitoring the minor alarm scan point. Success or failure of the automatic PA test is determined by monitoring the minor alarm scan point instead of observing the illuminating or extinguishing of converter LEDs.

THEORY OF OPERATION—MAINTENANCE FRAME POWER AND ALARM CIRCUITS

A. ♦Power Distribution

4.14 The -48 volt dc power and +24 volt dc power from central office power distribution circuits are supplied to the maintenance frame via four ED-5A079-10 connectors. These connectors provide both A bus (-48BA, +24AA) and B bus

(-48BB, +24AB) power connections. Resistance-capacitance (RC) filtering is provided for the +24 volt power circuits. The -48 volt dc power and +24 volt dc power are then distributed to appropriate fuse blocks for further distribution via the maintenance frame power unit.

4.15 Fuses in the maintenance frame power unit (Fig. 28) are generally Western Electric 70-type fuses. In some instances, however, a Bussman type GBB fast-blowing fuse is used. The Bussman fuses are used where a 70-type fuse, rated at 2 amperes or higher, cannot be guaranteed to blow more quickly than the main supply fuse used in some applications. Since the Bussman fuses have no alarm arrangement compatible with the fuse blocks provided, each is paralleled by a low-amperage 70-type fuse to provide a fuse alarm source.

B. Power and Alarm Control

4.16 The power and alarm control circuits (Fig. 29) for units appearing in the maintenance frame are located in the maintenance frame power unit. Alarm control flip-flops, located on two FC210 circuit packs in this unit, are buffered from system monitors and central office alarm circuits by five alarm relays. These alarm relays are designated MN, MJ0, MJ1, MJ2, and MJ3, and are normally operated. When an alarm condition occurs, the associated alarm control flip-flop is set, thereby releasing the relay to indicate the alarmed condition. After the trouble has been corrected, the alarm control flip-flops may be reset by momentarily depressing the PWR RESET switch located on the maintenance frame power unit.

4.17 The MN relay flip-flop monitors a power alarm (PA) lead that is connected to every

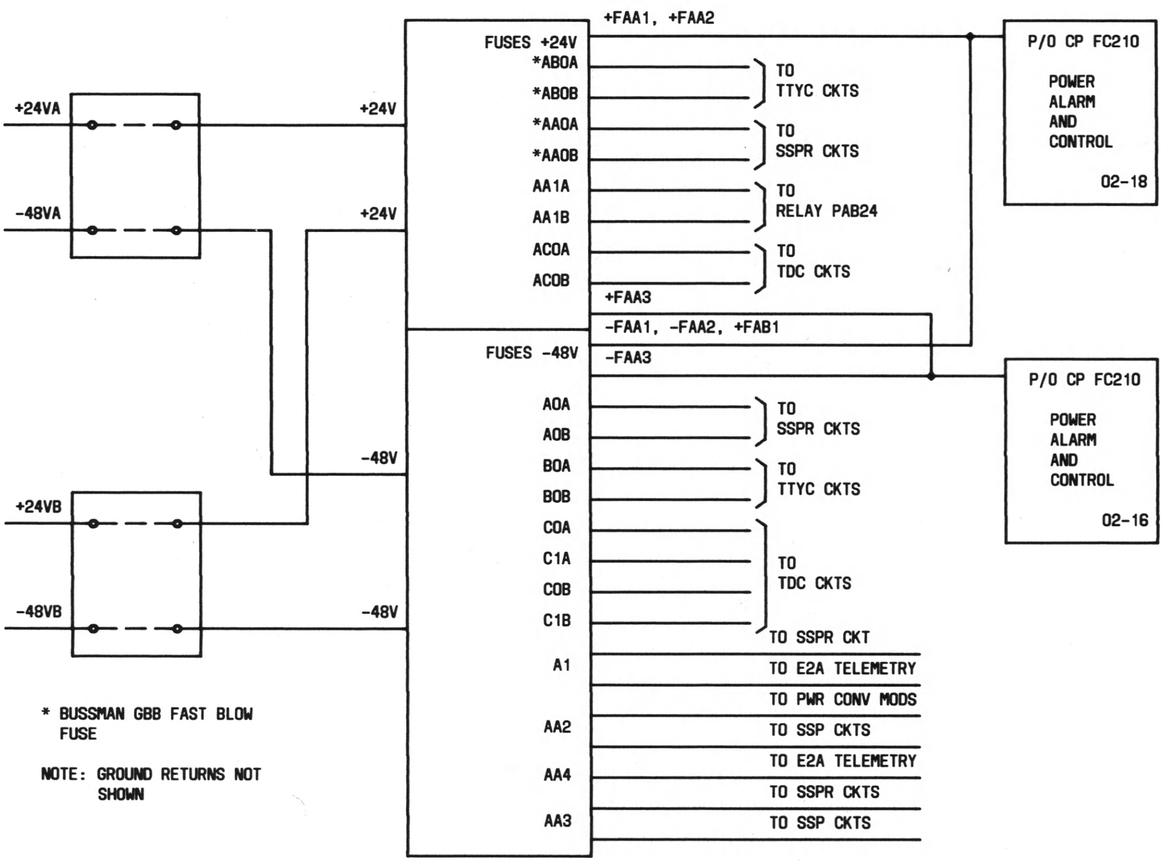
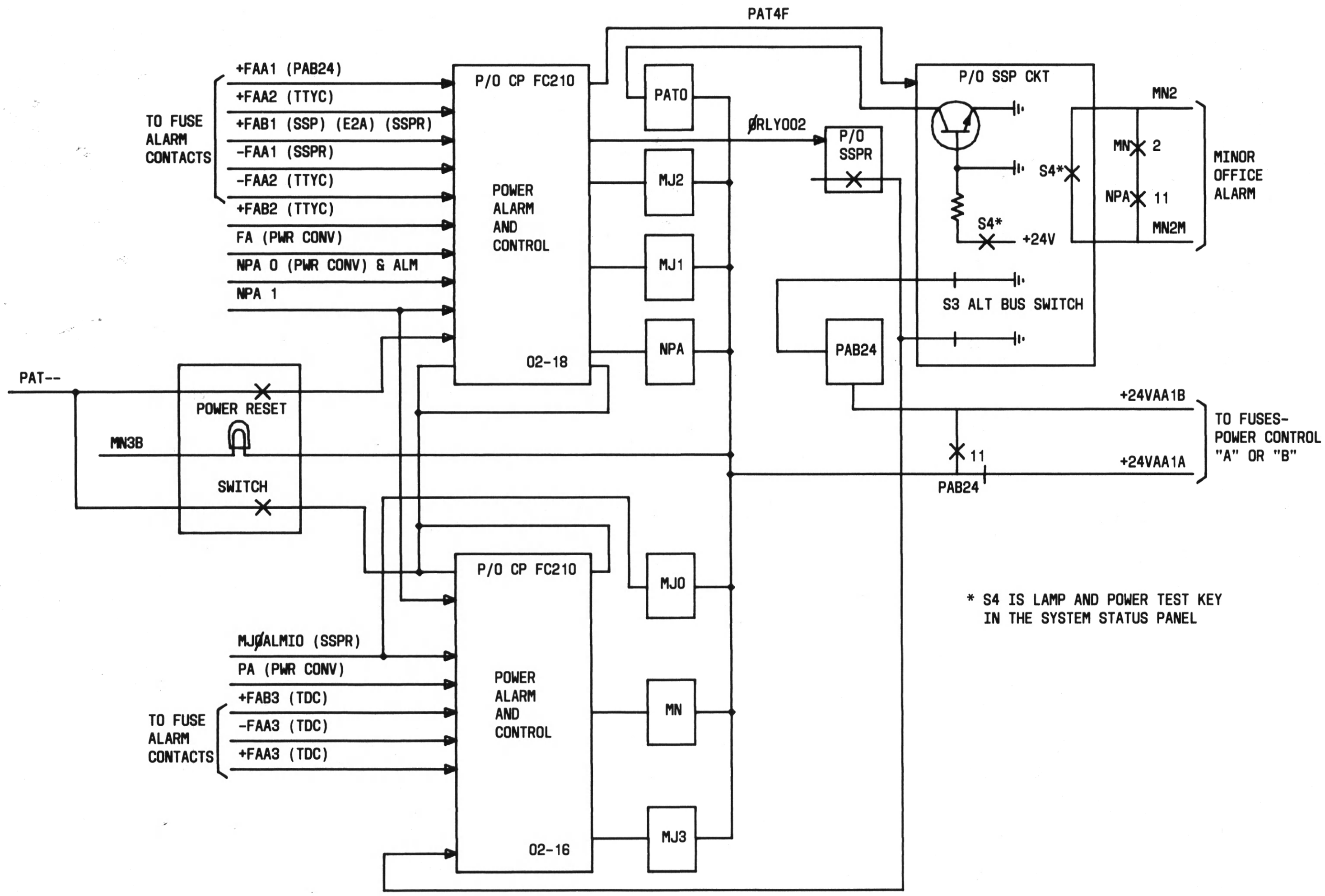


Fig. 28—Maintenance Frame Power Distribution and Fuses



Note: For purposes of clarity, the alpha character "0" is slashed when it appears in combination with numeric zeros.

Fig. 29—Maintenance Frame Power and Alarm Control

dc-to-dc converter appearing in the maintenance frame. The PA lead is activated when the output voltage of a converter drifts out of tolerance, thereby causing the MN relay to release. Release of the MN relay results in a minor alarm to the 3A CC.

4.18 The MJ0 relay monitors the fuse alarm (FA) lead associated with the SSPC, and the MJ1 relay monitors all fuses associated with the SSP related circuits. An alarm condition in either of the two dc-to-dc converters that supply +3 volts dc to the SSPC activates the FA lead, thus causing MJ0 relay to release. Release of the MJ0 relay removes the +24 volt dc start voltage from both converters, thereby removing the +3 volts dc power from the SSPC circuit. Since SSPC related power is connected in an alternate bus switching arrangement, any fault capable of blowing one fuse in the alternate bus arrangement is likely to blow the alternate fuse after the bus transfer is made. When a fuse associated with the SSP related circuits blows, the MJ1 relay releases. The MJ2 relay monitors fuse alarms and the converter fuse alarm lead associated with the TTYC circuits appearing in the maintenance frame. The MJ3 relay monitors fuse alarms and the converter alarm lead associated with the TDC circuits.

C. Power Alarm Test

4.19 The power alarm (PA) circuits appearing in the maintenance frame may be tested on a limited basis by a series loop connection between all dc-to-dc converters and voltage reference circuits contained in the frame. This connection provides the ability to test the minor alarm indicator circuits and the integrity of the series-connected PA loop. The test is initiated either by operating the LAMP & POWER TEST key on the SSP, or by system software.

D. Power Sequencing

4.20 Power sequencing relay logic is provided in the SSPR to control the dc-to-dc power converters located in the maintenance frame power unit. A finite time interval is required for the +3 volt converter output to stabilize after application of the converter start voltage. Power sequencing provides a time delay following converter start-up to ensure a known initial state of the SSPC circuits when the +3 volt converter power is applied. A power sequence occurs either when the SSP CIRCUIT POWER key is operated or when an alternate bus switch has occurred.

E. Alternate Bus Switching

4.21 An alternate bus switching arrangement is provided which automatically attempts to switch from the primary A power buses to alternate B power buses when loss of bus power occurs. Two alternate bus switching relays for the SSP and SSPC are contained in the SSPR. These relays monitor, and are powered by, the +24 volt dc A bus and -48 volt dc A bus, respectively, via fusing in the maintenance frame power unit. Both relays are held normally operated. Release of either relay will result in a transfer of its associated power source from the primary A bus to the secondary B bus.

4.22 Loss of +24 volt A bus power, or of the ground path to its relay monitor, releases the relay and transfers the +24 volt power source to the secondary B bus. Similarly, loss of -48 volt A bus power, or of the ground path to its relay monitor, releases the relay and transfers the -48 volt power source to the secondary B bus. Release of the -48 volt bus switching relay also forces release of the +24 volt bus switching relay, thereby switching both power sources. Release of the +24 volt bus switching relay, however, does not have a similar effect on the -48 volt relay. The reason for this difference is that the momentary loss of either the +24 volt or -48 volt source to a dc-to-dc converter can cause a converter shutdown. Removal and reapplication of the +24 volt start input to the converter will initialize the converter to a power-on state. Switching of the +24 volt source from one bus to the other provides the required power sequencing to the converter start input.

4.23 The maintenance frame power circuit is designed for operation from the +24 volt dc B power bus. The B bus power is supplied through contacts of a bus switching relay which is powered from the +24 volt B bus. The relay is held normally operated via a ground path through normally closed contacts on ALT BUS key at the SSP. If the B bus power fails, the relay will release, thus transferring to the standby +24 volt A power bus. Restoration of the B bus power source will automatically operate the relay to transfer the maintenance frame power unit to the B bus power source.◀

F. Software Power Alarm Test

4.24 When a software request for a PAT occurs, the alarm circuits will function similarly to the manual PAT. The PAT0 relay is operated by a peripheral decoder crosspoint and the MN relay alarm is not masked. A software interrogated circuit monitors the MN relay. Upon detecting the release of the MN relay, the peripheral decoder releases the PAT0 relay. After the PAT0 relay is released, if the MN relay and the NPA relays do not operate within approximately 150 milliseconds, the software may assume a failure has occurred and take appropriate actions.

5. MAINTENANCE OF CONTROL COMPLEX

INTRODUCTION

5.01 The maintenance plan involves redundancy of equipment; visual, audible, and printed automatic detection information; diagnostics and automatic maintenance recovery programs.

AUTOMATIC TROUBLE DETECTION

5.02 Automatic trouble detection takes on the following forms:

1. Check Circuits—Self-checking in the control complex is performed by the 3A CC and the MAS. If a failure is detected by a check circuit, under normal situations, a switch to the other system control will occur.

2. Call Processing Tests—During call processing, many checks are performed which verify the integrity of the peripheral hardware and the accuracy of internal data. Any detected failure initiates a recovery action.

3. Routine Test—These are tests of hardware performed automatically on a scheduled basis (for example every 24 hours). These tests may also be manually requested via the local or remote maintenance TTY.

AUTOMATED MAINTENANCE FACILITIES

5.03 Automated maintenance facilities are divided into two general types:

1. Recovery—When failures are detected, the system takes corrective action to identify the failed unit and remove it from service. The results of such actions are indicated on the maintenance TTY and the system status panel.

2. Diagnostics—Programmed diagnostics are initiated manually via the maintenance TTY. These provide the capability for accessing, testing, and exercising selected portions of the system.

MAINTENANCE SOFTWARE

5.04 The maintenance programs include those programs which relate to maintenance of the system hardware. Functions performed by these programs are:

(a) To detect equipment troubles and/or stored program inconsistencies

(b) To provide an attempt to recover and reconfigure a working system when failure occurs.

Some maintenance of these programs may be performed through use of the 3A CC control panel and/or the TTY.

RESIDENT PROGRAMS

5.05 The MAS of the processor contains the resident programs which include all call processing programs and some fault detection programs in a write-protected portion of the MAS. Write-protected memory can only be changed by using special instructions. A backup source of these programs is maintained by the tape data controller unit in the MTCE frame.

5.06 The resident programs are arranged in order based on their relative importance. The order is composed of two major categories: the normal call processing and maintenance (base level) programs and the called-in programs which interrupt normal call processing (interrupt level).

5.07 Base level includes all call processing programs plus all maintenance tasks that can be deferred or are of low priority. These are called in at the end of the normal call processing loop.

5.08 Interrupt level programs break into the base level loop on a periodic timed basis (input/output interrupt) or upon demand (maintenance interrupt) when a fault or trouble of high priority is discovered. When the interrupt level program has timed out or completed its allotted work, control is returned to the base level.

NONRESIDENT PROGRAMS

5.09 Infrequently used programs such as fault diagnosis programs and service order programs are nonresident in that they are only stored on the duplicated tape cartridges in the MTCE frame. These programs pertain to the control and administrative tasks or report on areas that need maintenance attention. Some maintenance functions performed by these programs report system status, including service statistics and performance which reflect the basic condition of the system. Also, the tape cartridge may store essential information which could be used in conjunction with the trouble locating manual (TLM).

REMOTE MAINTENANCE

5.10 The No. 3 ESS provides an option for unattended operation. Remote control of maintenance and operation is facilitated by E2A telemetry and teletype communication between the office and a switching control center. The centrally located switching control center system (SCCS) provides sufficient display, control, and alerting capabilities to enable No. 3 ESS remote maintenance.

5.11 There are two SCCS hardware configurations. The No. 1 SCCS configuration has manual capabilities to provide remote monitoring, control, and maintenance of a central office. A hard-wired command and display (C&D) console and TTY are utilized as the man-machine interface. The No. 2 SCCS configuration provides a minicomputer with an associated cathode-ray tube (CRT) and keyboard to be used to collect and analyze office data. The minicomputer performs automatic analysis of output messages and generates supplementary SCCS alarms and has automatic storage of output messages for later scanning, condensation, and statistical reporting. The No. 2 SCCS is preferred for remote operation of the No. 3 ESS office.

5.12 With either SCCS configuration, the TTY link is of primary importance. Teletypewriter messages supplement the E2A telemetry control information by providing recordable status and maintenance information. The SCCS normally monitors the No. 3 ESS via part 1 of TTY0 (maintenance TTY) using a dedicated line with data sets at both ends. Section 233-141-100, Centralized Office Maintenance, Description and Theory of Operation provides greater detail pertaining to remote operation of the No. 3 ESS.

5.13 In the event that all ports on TTY0 become inoperative, the No. 3 ESS program will automatically establish a connection between the SCCS dedicated line and TTYC1 using a relay applique circuit. If the SCC still fails to respond properly, the program will queue and/or discard messages until the dedicated line is repaired or SCCS personnel establishes a dial-up connection using the ESS autoconnect facility.

6. REFERENCES

6.01 The following list of BSPs contain information which is relevant to this section:

SECTION	TITLE
233-000-003	General Description
233-110-000	Control Complex, Description
233-121-110	Frame Input/Output Controller, Description and Theory of Operation
233-130-100	Power Equipment, Description
233-141-100	Centralized Office Maintenance, Description and Theory of Operation
233-150-100	General Description, Software Subsystem Description
254-300-110	3A Central Control Description, Common Systems
254-300-120	3A Central Control, Theory of Operation, Common Systems

SECTION	TITLE
254-300-130	Input/Output Interfaces, Description and Theory of Operation, Common Systems
254-300-150	3A Processor Main and Supplemental Stores, Description and Theory of Operation, Common Systems

7. GLOSSARY

7.01 A glossary of terms is provided to aid in understanding this section.

Asynchronous—Functional units operate/interface without a fixed time relationship.

Autonomous—The device can perform its primary function without external assistance.

Bit Sliced—Technique of placing consecutive bits of a data word on different circuit packs in order to improve probability of error detection in case of a bit failure.

Bootstrap—A program in microstore which, in the event of main store memory loss, calls up the initialization program from tape in an attempt to generate a complete workable active system.

Buffer—A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another.

Common Control System—A switching system which makes use of common equipment which is not part of the talking connection but is used to establish a connection and then becomes available to establish other connections.

Cross Point—A control signal developed by a gating circuit when signals representing specified events (usually outputs of decoders) are present at the inputs to the gating circuit. Also may mean the gating circuit itself.

Diagnostic—A program which functions to isolate a fault within the unit under test.

Fault—The failure of an electronic circuit to perform a function for which it was designed, and which can be reproduced by the system.

Flip-Flop—A device capable of assuming two stable states (set or clear), thereby storing a bit of information. It remains in either state until a signal changes it to the other state.

Frame Input/Output Controller (FIOC)—An interface between the 3A CC and the peripheral controllers. It converts the information between serial and parallel forms (depending upon the direction of flow) and gates the data to and from the peripheral controllers.

Generic Program—A standard program modified for the specific use of a particular office.

Initialization—(Also referred to as maintenance reset function [MRF]). Restart of the 3A CC at a known state and condition. The two basic types are system generated and manually generated.

LPCDF—Low profile combined distributing frame (7-feet high). For low ceiling ESS type offices. Used for terminating and cross-connecting outside plant cable pairs, trunk and transmission equipment, etc.

Light Emitting Diodes—LEDs convert direct current into a visible light output without energy-consuming filaments.

Line—Anything that connects to a network terminal which is not classified as a trunk or service circuit. Usually a pair of wires which serves to connect a customer telephone to a terminal on the network.

Macro—A group or set of machine language instructions identified by a particular name and which perform a specific function.

Microcode—Microcode is the set of instructions encoded in the 3A CC read only memory. Microcode instructions control all internal operations of the 3A CC.

Microinstruction—One of the 32-bit instruction words encoded in the microstore of the 3A CC microprogram control. The microstore is a read-only memory which contains all the microinstructions that control the 3A CC.

Network Controller (NWC)—That part of a system control which receives orders from the CU (via the FIOC) and establishes paths in the network.

A system control may contain up to two network controllers.

Off-Line—Equipment operating, normally as an exercise, but not involved in actual call processing.

On-Line—Equipment operating in an actual call processing mode.

Peripheral Pulse Distributor (PPD)—That part of a system control which receives orders from the control unit (via the FIOC) and sends bipolar pulses to peripheral decoders. A system control may contain up to two PPDs.

Read—To retrieve the information stored in a memory device.

Redundant—Exceeding what is necessary for normal expected operation to assure more reliable performance.

Refresh—To restore information stored in a memory device on a periodic or cyclic basis.

Scanner Controller (SC)—That part of a system control which receives orders from the CU (via the FIOC) and replies with the scan results of a row of 16 scan points. A system control may contain up to two scanner controllers.

Scan Point—A location at which a ferrod is connected in order to determine the status of a customer line, trunk, or test point.

Semiautonomous—The device requires external assistance to perform some of its primary functions.

Time-Shared Circuit—A common circuit which accommodates several other circuit functions during different time intervals.

Transitory Data—That data which resides temporarily in memory (call store) during all processing and maintenance.

Write—To insert information into a memory device.