SCANNER DESCRIPTION AND THEORY OF OPERATION
NO. 3 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

1.01 This section provides descriptive and theory information on the scanners used in the No. 3 Electronic Switching System (ESS).

1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.

1.03 The scanner serves as a constant monitor of subscriber lines to detect off-hook originations and on-hook terminations, to check the status of talking paths, and to check certain test points and other miscellaneous points (e.g., alarms).

1.04 The scanner transmits system status to the 3A central control (3A CC) upon request. The relationship of the scanner within the No. 3 ESS peripheral system is shown in Fig. 1. The scanner controller (SC) receives address information via the frame input/outout controller (FIOC) from the 3A CC. The address information designates a particular ferrod sensor row (consisting of 16 ferrod sensors) to be interrogated within the scanner matrices. The interrogation results are returned to the 3A CC via the FIOC.

2. EQUIPMENT DESCRIPTION

2.01 The No. 3 ESS scanners are located on the network and control frames (Fig. 2 and 3). There are two designated types of scanners; the universal scanner and master scanner. Each scanner is physically composed of an SC and a maximum of eight ferrod arrays. One ferrod array (512 ferrod sensors) is located on each network frame. The initial control frame (0) contains an SC (duplicated) and the master scanner ferrod array. The SC on control frame 0 can accommodate the first seven network frames. Control frame 1 provides the second SC (duplicated) to accommodate network frames 8 through 15. Control frame 1 does not provide an additional master scanner array. A No. 3 ESS office is equipped with only one master scanner array.

SCANNER CONTROLLER

2.02 An SC is arranged to accommodate 4096 scan points and is the duplicated portion of the scanner. The SC is part of the peripheral control unit (Fig. 4). A total of 31 circuit packs physically makes up the SC. The No. 3 ESS software considers the SC (31 packs) as two functional controllers. Therefore, unlike the other peripheral controllers within a peripheral control unit, the SC is accessed by two subchannels (3.01). The SC consists of the following plug-in circuit pack types:

(a) Scanner control circuit (FA997)

(b) Timer circuit (FB413)

(c) Interrogate current driver (FB288)

(d) Interrogate matrix (FC330)

(e) Detector circuit (FC135)

(f) Test circuit (FB412).

FERROD SENSOR ARRAYS

2.03 The scanner ferrods are organized to form 512 scan points per master scanner or universal scanner. The master scanner ferrods are mounted on twenty-four FC184 and eight FC183 circuit packs. The universal scanner ferrods are mounted on four FC182 circuit packs, four FC183 circuit packs, and twelve switch packages (type

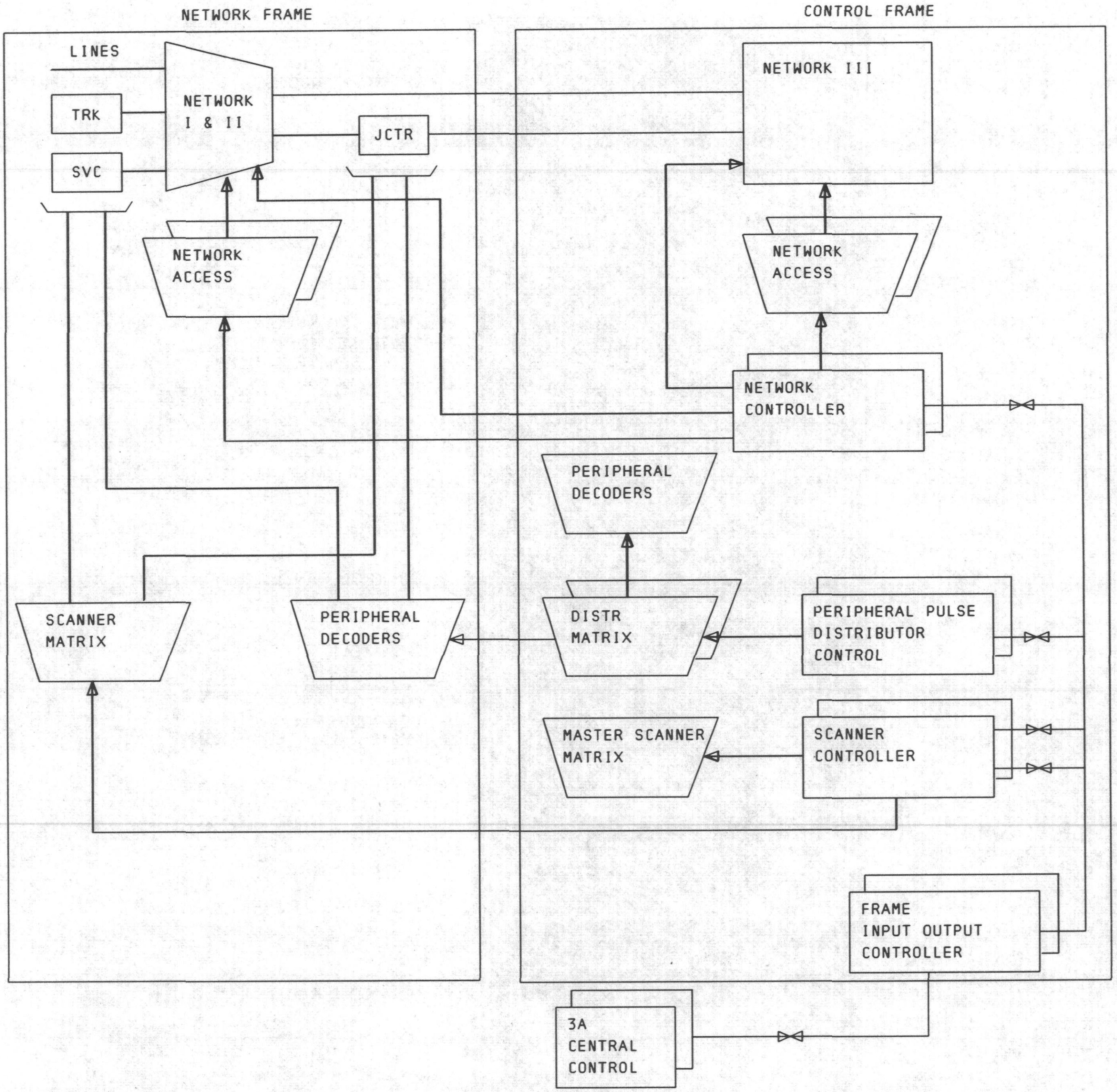


Fig. 1—No. 3 ESS Peripheral System

296-6C). Each circuit pack contains 16 ferrod sensors. The FC182 circuit pack contains 2B ferrods, while the FC183 and FC184 circuit packs contain 2C ferrods. Each switch package contains thirty-two 2A ferrods.

2.04 Each point to be scanned is connected to a current sensing device called a ferrod sensor. The ferrod consists of a ferrite stick with a pair of control windings. The control windings are connected in series with the circuit to be supervised.

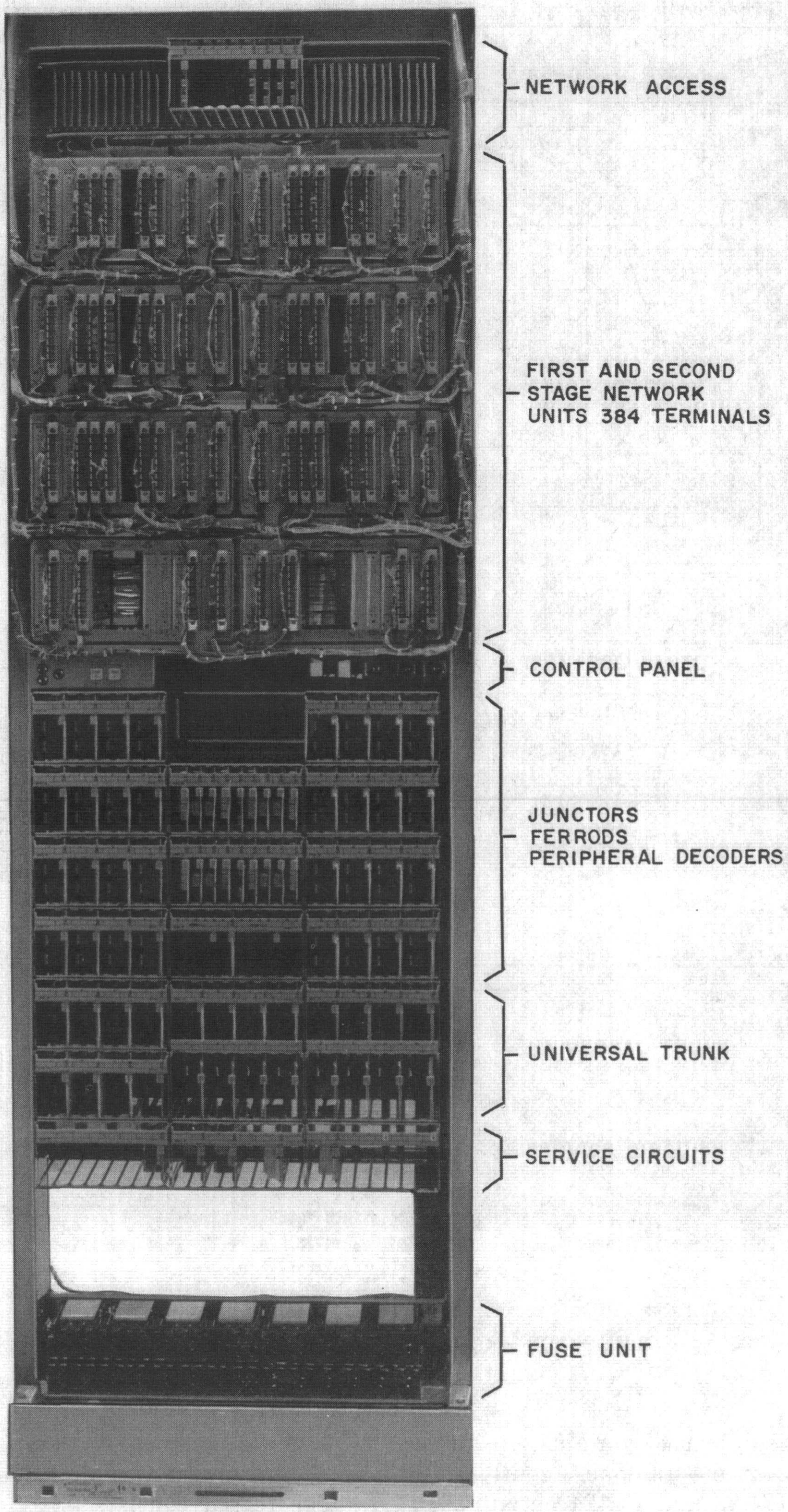


Fig. 2—Network Frame

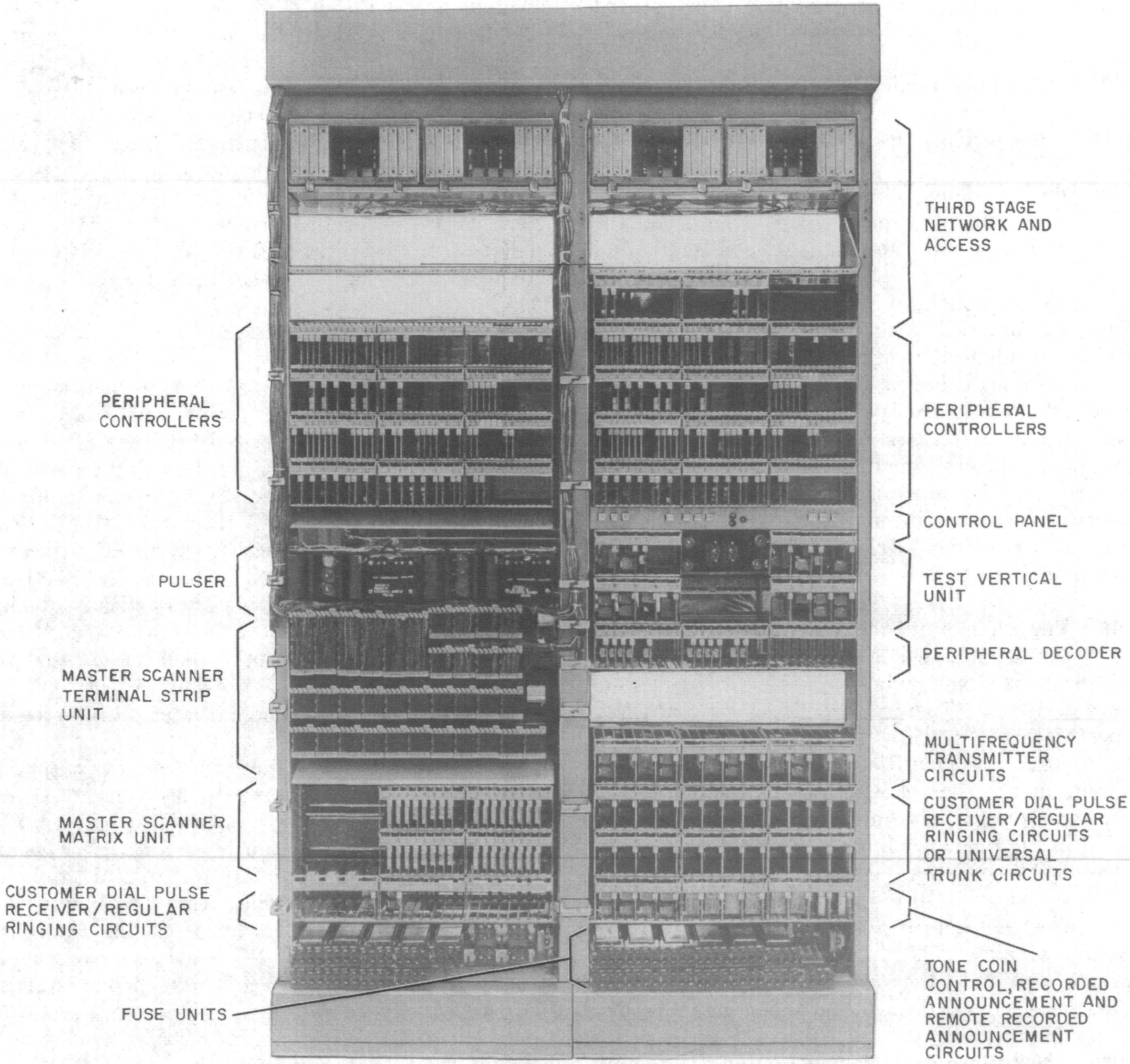


Fig. 3—Control Frame 0

A single-turn interrogate winding and a single-turn readout winding are threaded through two holes in the center of the ferrite stick (Fig. 5).

2.05 The magnetic coupling between the interrogate and readout windings is determined by the magnetic state of the ferrite stick. When current flows in the control windings, the ferrite stick is in a saturated magnetic condition. The ferrite stick is in a nonsaturated magnetic condition when no current flows in the control windings.

2.06 To determine the state of a ferrod, a 500-mA bipolar pulse is applied to the interrogate winding. The negative half-cycle of the interrogate pulse is used to reset the ferrite stick to its maximum negative magnetic remanent state. The positive half-cycle of the interrogate pulse is used to read out the magnetic state of the ferrite stick.

2.07 When the control windings are not energized, the interrogate pulse changes the magnetic state of the ferrite stick. Changing the magnetic flux induces a nominal voltage of 200 millivolts in the readout winding. This readout is a logical zero. When the control windings are energized, the interrogate pulse does not change the magnetic flux of the ferrite stick because it cannot overcome the state established by the control windings. Therefore, practically no voltage is induced in the readout winding (less than 25 millivolts). This readout is a logical one. Thus, when an interrogate pulse is applied, the presence or absence of a readout pulse indicates whether there is current flow in the control windings. If the circuit being observed is, for instance, a customer line, the on-hook (open) condition results in a readout of zero and the off-hook (closed) condition results in a readout of one.

2.08 The change in the magnetic state of the ferrite stick when the interrogate winding is pulsed is represented by the ferrod sensor characteristics. The characteristics of the three types of ferrod sensors (2A, 2B, and 2C) used in the system are identified in Fig. 6. When the current in the control windings of the 2A ferrod is 5.5 mA or less, the interrogate pulse induces a signal in the readout winding. This value (5.5 mA) is called the nonoperate current. When the control winding current is 10 mA or more, the interrogate pulse does not induce a significant signal in the readout winding. This value (10 mA) is called the operate current. Ferrods have approximately a 2-to-1 ratio between operate and nonoperate currents.

2.09 The 2A ferrods, which operate on a loop-start basis (Fig. 7), are used to recognize the initial request for service from ordinary customer lines. The 2A ferrods are also used for ground start operations (Fig. 8). These ferrods recognize requests for service from prepay coin and PBX lines.

2.10 The 2B ferrods are used in junctors for supervision (Fig. 9). These ferrods provide supervision in both directions for intraoffice calls and supervise the line during interoffice conversation.

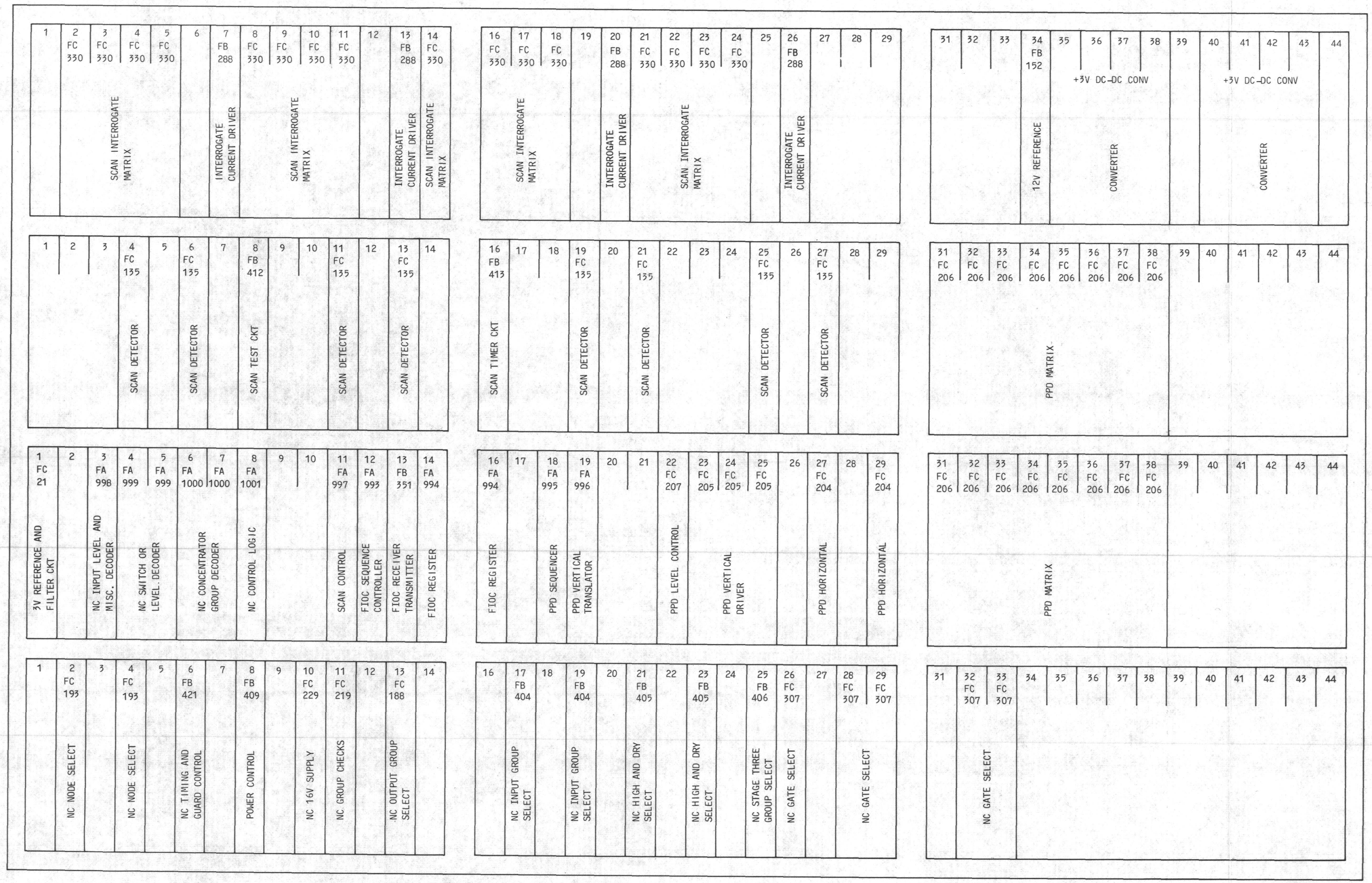
2.11 The 2C ferrods are used for all universal trunks and most service circuits. All these ferrods are of the loop wiring type (Fig. 10). The 2C ferrods are also used as the master scanner ferrods and are associated with both loop wiring and battery and ground wiring (Fig. 11). The battery and ground ferrods are used for alarms, common system equipment, multifrequency (MF) receiver supervisory scan points, and the pretrip/ring trip scan points on the ringing circuits. The loop ferrods are generally used as the additional scan points for those service and trunk circuits which require more than one scan point.

3. FUNCTIONAL DESCRIPTION

3.01 There are two main sections in each scanner, the current-sensing ferrods (which are wired to the points to be supervised) and the SC (which provides selection information necessary to interrogate the ferrod row). The SC receives address information via the FIOC from the 3A CC (Fig. 12). An enable signal activates the SC to accept the data and act upon it. To reduce electrical loading on critical leads, the SC is logically divided into two parts. One part is accessed via FIOC subchannel A, while the other part is accessed via subchannel D. The SC provides a path to the selected ferrod sensor row, initiates an interrogate pulse, and detects the results of the interrogate pulse. The FIOC interface with the SC output is 16 data bits corresponding to the output of one row of 16 ferrods. Also, two timing (reply enable) signals specify a period during which the FIOC is to receive these interrogate results and an all-seems-well (ASW) indication. The results are then returned to the 3A CC from the FIOC via the REPLY cable. The SC provides error checks to ensure the validity of the data being returned to the 3A CC.

3.02 The SC interface with the ferrod array is a pair of wires from each transformer in the SC to the interrogate winding of a row of ferrod sensors (Fig. 13). The bipolar interrogate pulse is looped through two sets of eight ferrods to make one ferrod row. The readout windings of each of the 16 ferrod sensors in a row are connected to data detectors in the SC. Each readout loop includes 32 ferrods, one from each of the 32 rows. The ferrod array is not duplicated but can be accessed by either system control (SYC) 0 or 1.

3.03 Each scanner contains five hundred twelve 2A, 2B, or 2C ferrods. The active or idle state of each ferrod is controlled by the circuit



LEGEND:
FIOC = FRAME INPUT OUTPUT CONTROLLER
NC = NETWORK CONTROLLER
PPD = PERIPHERAL PULSE DISTRIBUTOR

Fig. 4—Peripheral Control Unit

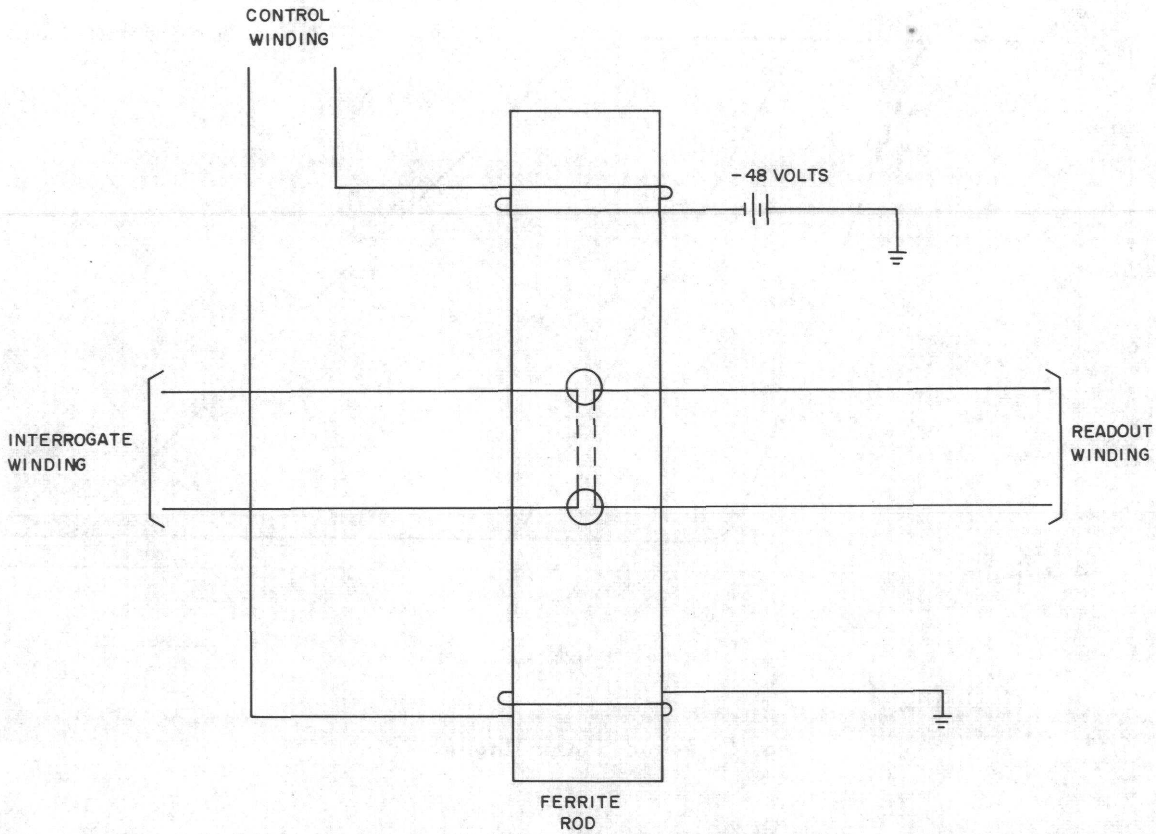


Fig. 5—Ferrod Schematic Diagram

connected to the control winding. Thus, circuit conditions can initiate requests requiring system action.

3.04 The designated types of ferrod arrays used in the No. 3 ESS are the universal scanner ferrod array and the master scanner ferrod array. The universal scanner array is used to notify the system of customer service requests and to provide the supervision functions in junctors, trunks, and service circuits. The master scanner array also monitors trunk and service circuits, maintenance circuits, and alarm circuits. Fig. 14 and 15 show the general assignments of circuit scan points for both types of arrays.

4. THEORY OF OPERATION—SIGNAL AND CONTROL CIRCUITS

4.01 The SC consists basically of input circuitry, an interrogate matrix, and output circuitry. The input circuitry transforms the low-level address information into signals which can operate the transformers in the interrogate matrix. The interrogate matrix consists of a 16-by-16 array of transformers. The output circuitry converts the ferrod outputs into signals which can be used by the FIOC. A functional block diagram of the SC is shown in Fig. 16 and 17. The scanner portion of the peripheral controller schematic diagram (SD-3H110-01) contains the following functional schematics (FSs): FS17, scanner control; FS18, scanner interrogate matrix; FS19, scanner interrogate drivers; FS20, scanner detectors; and FS21, +3 volt and +24 volt power distribution. The following paragraphs contain a description of each FS with the exception of FS21, which is included in Part 5.

SCANNER CONTROL (FS17 OF SD-3H110-01)

4.02 The sequencer (scanner control) receives data information from the FIOC which provides the following.

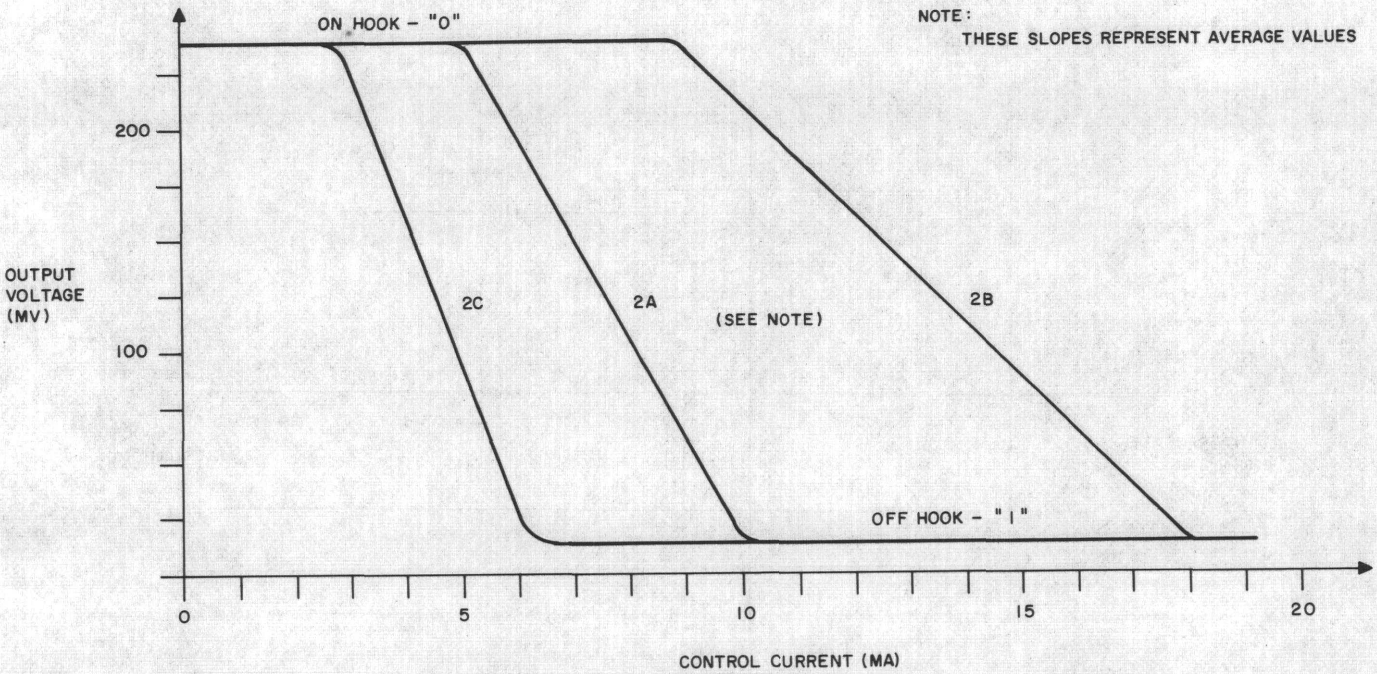


Fig. 6—Ferrod Sensor Characteristics

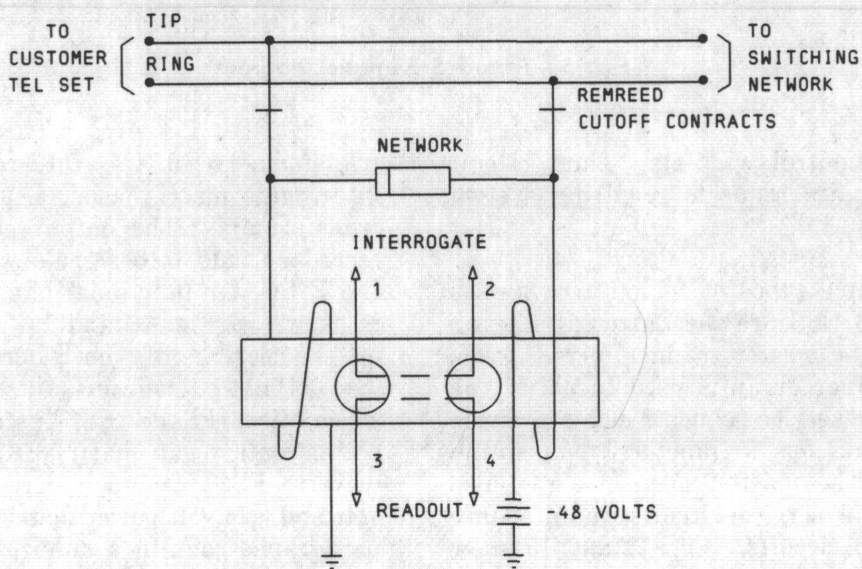


Fig. 7—Loop Start Wiring Using 2A Ferrod

(a) ***Horizontal Translation:*** Data bits 4, 5, 6, 7, and data parity low (D_{PL}) signals drive two 1-out-of-8 decoders. The total combined output of both decoders (DR0 through 15) provides a 1-out-of-16 selection for a horizontal (16 transformers) in the interrogate matrix.

(b) ***Vertical Translation:*** Data bits 8, 9, 10, and data parity high (D_{PH}) signals drive a 1-out-of-8 decoder. The output of the decoder (SL0 through 7) provides a 1-out-of-8 selection of an interrogate current driver in each half of the interrogate matrix. The final 1-out-of-2

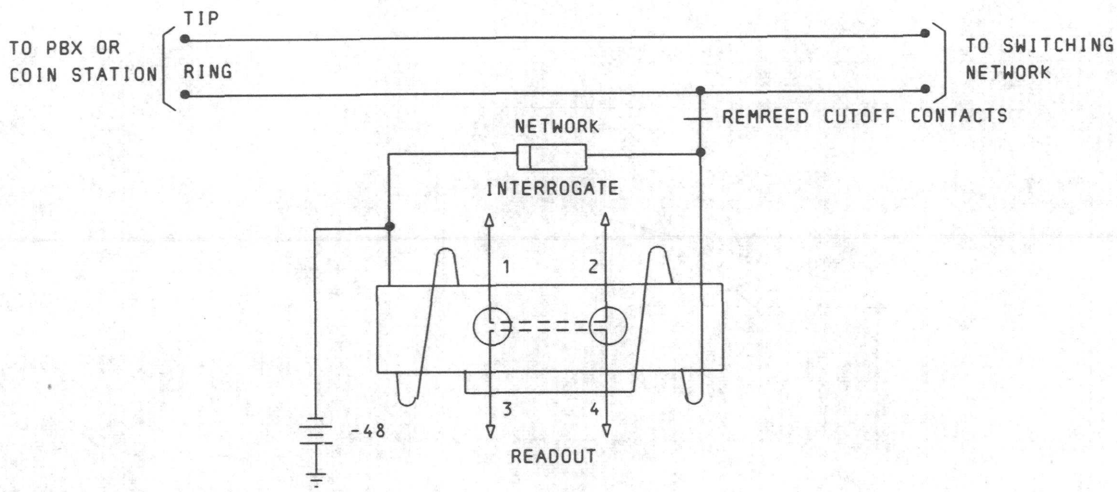


Fig. 8—Ground Start Wiring Using 2A Ferrod

selection (completing the 1-out-of-16 selection) is determined by the subchannel enable signals, GCTL0 and GCTL3, in the timer (refer to 4.03).

(c) ***Order Decoding:*** Data bits 11, 12, 13, and 14 drive a 1-out-of-7 decoder which functions as an order decoder. Fig. 18 contains a list of the scan order codes. A scanner order to the FIOC requires one serially transmitted data word from the 3A CC. This data word contains not only the order code but the necessary information to select a row of ferrods to be interrogated.

(d) ***Status Decoding:*** Data bits 0 and 1 of the load and transfer orders, along with two power control signals and a signal from the mate controller, drive the A- and B-control flip-flops to determine whether this controller is on-line.

(e) ***Enable:*** The subchannel enable signals, GCTL0, GCTL3, and GCT (the combined enable signal), are internally distributed within the sequencer. These enable signals are also passed to the timer.

4.03 The scanner timer (FB413, Fig. 17) receives the ORed enable signal, GCT, from the sequencer. It then returns a TM10 signal to the sequencer and a CS signal to the first column of circuit packs in the interrogate matrix. The TM10 signal in the sequencer is used to enable the outputs of the horizontal and vertical decoders. It is also used to gate out a PULSE signal to the timer. The PULSE signal in the timer drives a timing chain (Fig. 19). The interrogate matrix is divided into two parts, the left half (subchannel 0) and right half (subchannel 3). The interrogate current driver data is sent to both halves. Referring to the timing chain, the subchannel enable signal determines which of the NPD 0/3 and PPD 0/3 signals will be sent to the interrogate current drivers. The NST and PST signals are sent back to the sequencer to gate check information into two 2-bit registers (ASW REG on Fig. 17). The ANDed output of the two registers drives the ASW bit that is sent back to the FIOC. The LCT and RDGCT signals are sent to the FIOC where the leading edges of these signals define a period to receive interrogate results and the ASW check.

SCANNER INTERROGATE MATRIX (FS18 OF SD-3H110-01)

4.04 The selected horizontal and vertical in the interrogate matrix intersect at a transformer. This transformer sends the interrogate pulse to a row of 16 ferrods. The negative pulse to the ferrods clears the ferrod; i.e., it initializes the magnetic material to its maximum negative remanent state. This prepares the ferrods for the positive pulse which will then generate the maximum change in magnetic flux, assuring a complete (full amplitude) readout pulse. The first four circuit packs in the interrogate matrix contain the horizontal drivers and receive the outputs from the horizontal decoder in the scanner control. These packs also receive from the timer a CS signal which turns on power to the horizontal drivers. Each of these circuit packs contains check circuitry to determine when

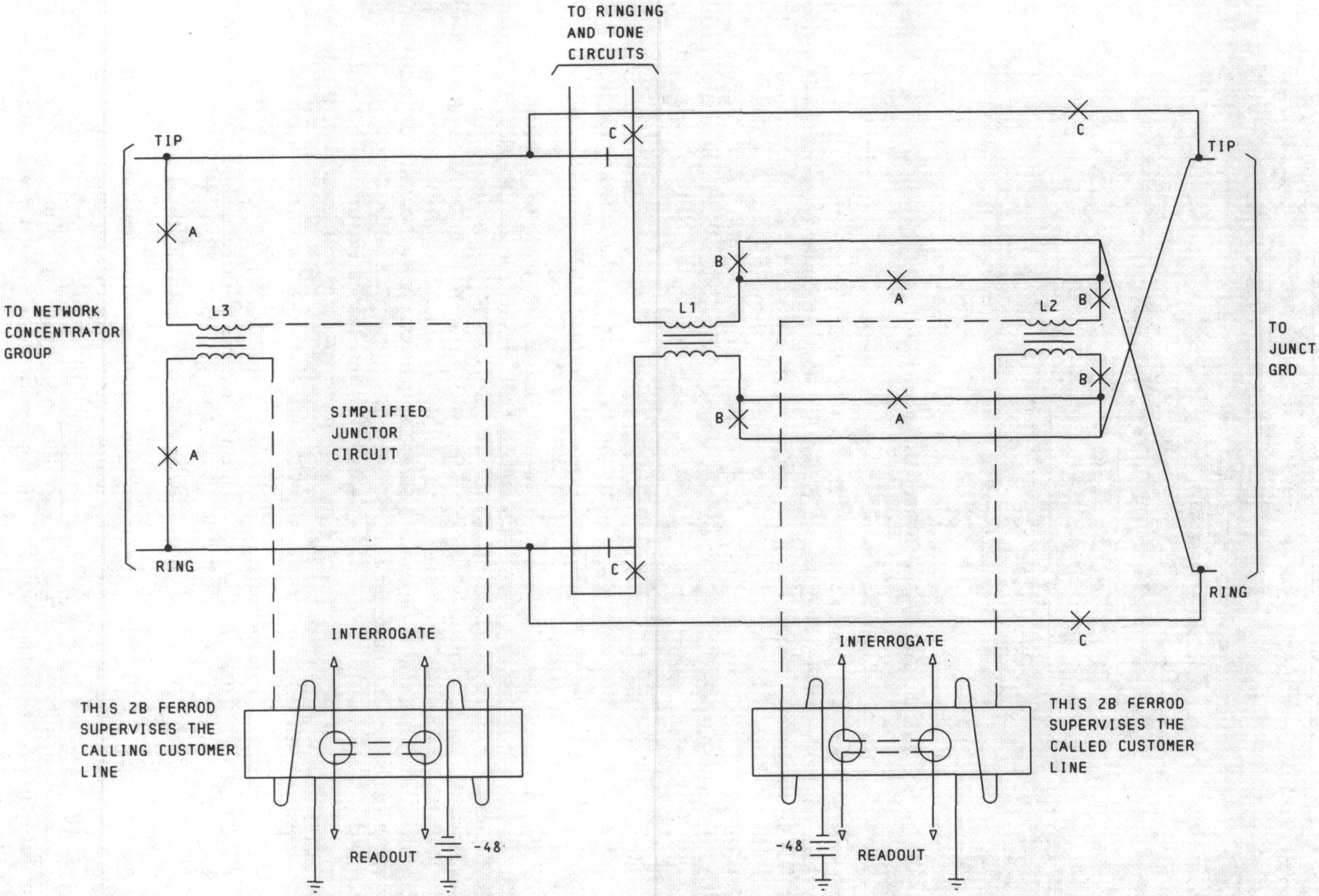


Fig. 9—Junctor Supervision Using 2B Ferrod

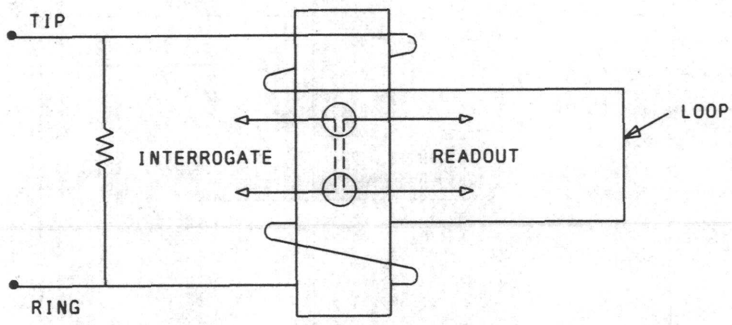


Fig. 10—Loop Wiring Using 2C Ferrod

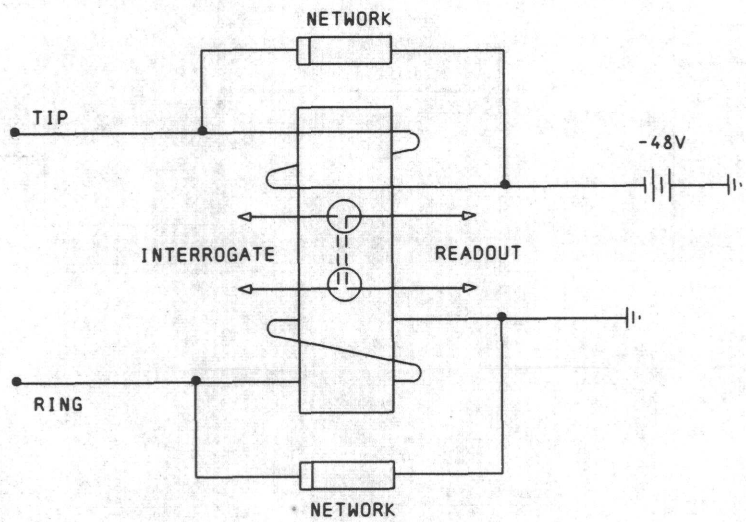


Fig. 11—Battery and Ground Wiring Using 2C Ferrod

more than one horizontal has been enabled. The NO output signal is sent to a detector on the first interrogate driver circuit pack. The outputs of the horizontal drivers in the first column are multipled to the other matrix packs in the same horizontal.

SCANNER INTERROGATE DRIVERS (FS19 OF SD-3H110-01)

4.05 The interrogate current driver address information is received from the sequencer. The timer sends the NPD signal to all drivers in the selected half of the matrix. The particular driver circuit that is enabled sends a pulse to a vertical of 16 transformers in the interrogate matrix, resulting in a negative output pulse. Similarly, the PPD signal follows, and a positive interrogate pulse is sent to the interrogate matrix. Circuitry on the first driver pack performs a 1-out-of-N check on the horizontal and vertical selection. One detector is connected to the first four matrix packs to check the horizontal selection. The other detector connects to all of the interrogate current driver packs to check the vertical selection. Less-than-one and greater-than-one indications are sent to the sequencer, where they are examined twice, once during the negative (NPD) pulse and again during the positive (PPD) pulse. If all of the checks are satisfactory, an ASW signal is sent to the FIOC.

SCANNER DETECTORS (FS20 OF SD-3H110-01)

4.06 The data detectors receive the readout pulses from a column of ferrods. The detector circuit output will pulse low (on-hook) when a

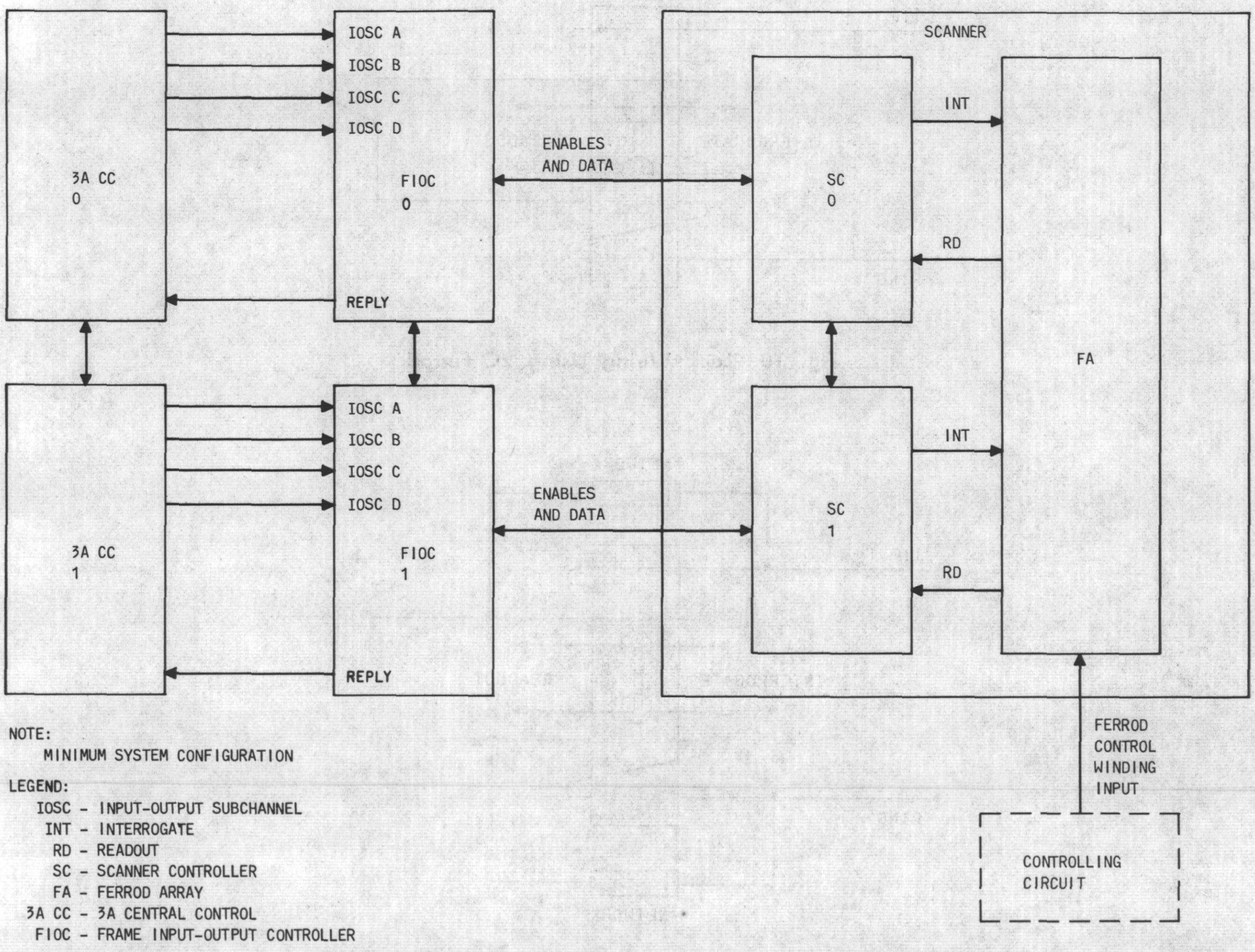


Fig. 12—Scanner Interfaces

current pulse is present at its inputs. All 16 returns are detected at one time by a single circuit pack in each of the duplicated scanners. There is one duplicated detector circuit pack for each 512 ferrods. The left-half group of four detector packs (0 through 3) sends outputs to FIOC subchannel 0, while the right half (4 through 7) sends outputs to subchannel 3. Four data bits (2 through 5) from both groups of detectors are routed through the sequencer. Under normal order conditions, the bits are gated through the sequencer to the FIOC. Under maintenance conditions, these bits will be used to return other information to the FIOC.

5. POWER AND ALARM CIRCUITS

+3 VOLT POWER DISTRIBUTION (FS21 OF SD-3H110-01)

5.01 The power system of the scanner controller (Fig. 20) contains two J87389F (A8), +3 volt converters; one FC21, +3 volt reference and filter circuit pack; and one FB152, +12 volt reference circuit pack. The power system also distributes +24 volts, +3 volts, and ground (GRD) to the SC circuit packs via the multilayer printed wiring boards (MLPWB). The control winding current for battery and ground ferrods in the master

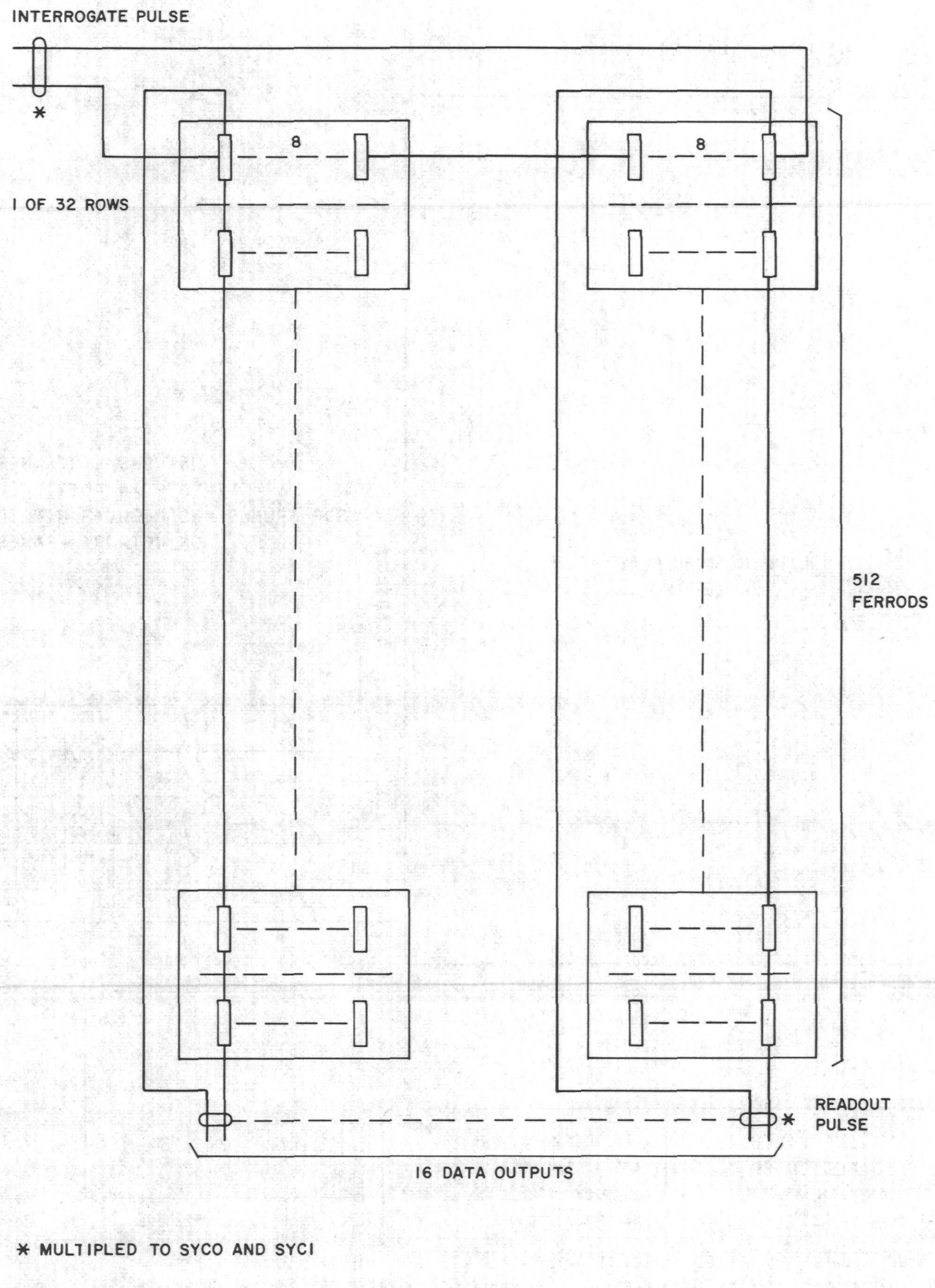


Fig. 13—Ferrod Array Interfaces

scanner is provided by the -48 volt power frame via the control frame circuit. The control frame circuit also provides +24 volts and -48 volts to the two A8 power converters.

5.02 The control frame circuit provides power control, fusing, and alarms for the peripheral control unit. The power control and alarm circuit consists of four circuit packs: two FB414, 3-volt power controls, 0 and 1; and two FB415 alarms, 0 and 1. A control panel and two fuse panels are associated with the control frame power. The control panel has three nonlocking (NLK) keys (ON, REQ, and OFF) and two lamps (OOS and PWR OFF) which are duplicated for peripheral control units 0 and 1. The fuse panel contains power fuses

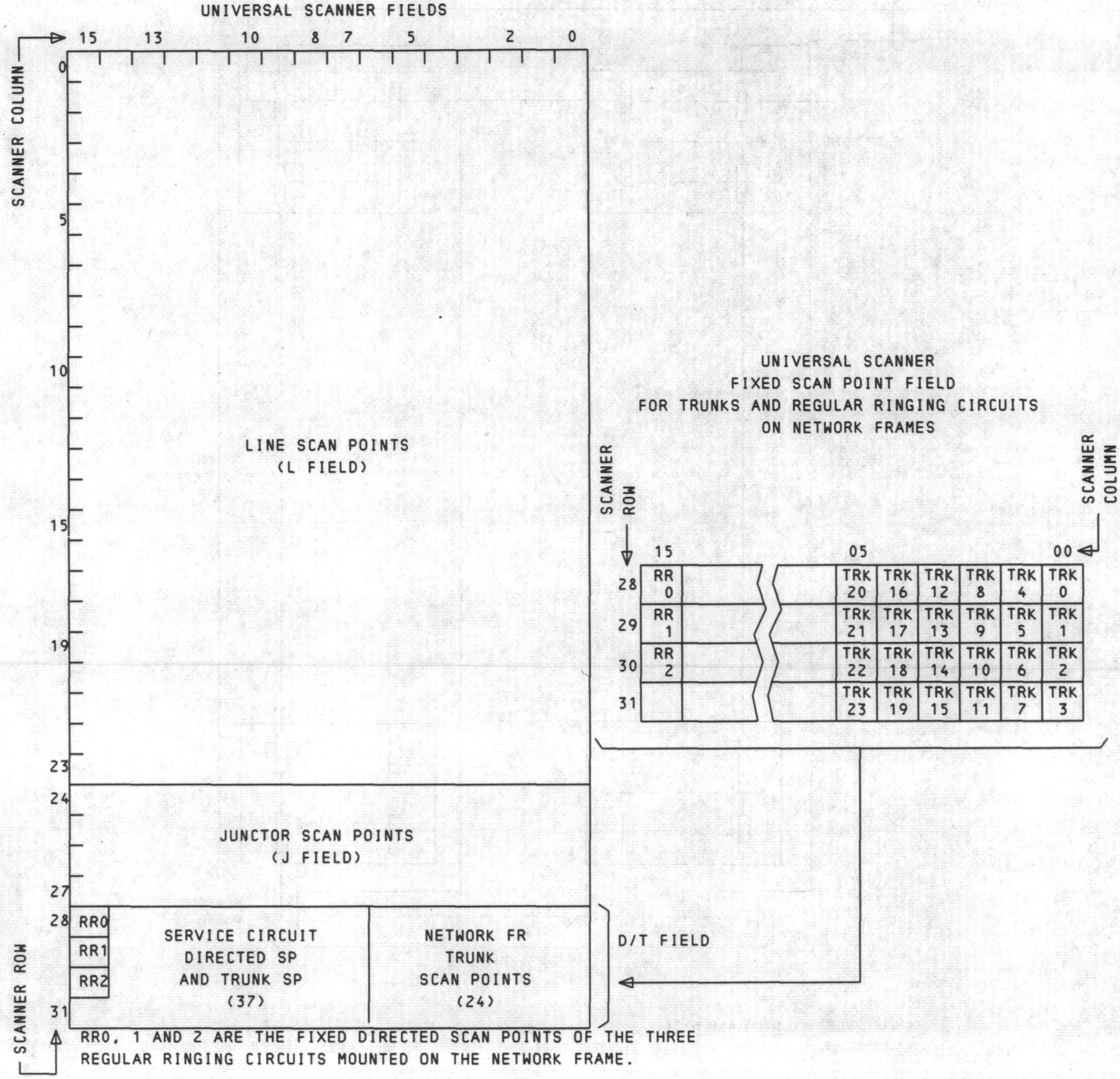


Fig. 14—Universal Scanner Ferrod Array Layout

for protecting each controller in the periphery. The control frame circuit (SD-3H902-01) contains the following power related functional schematics: FS41, +24 volt power control, fusing, and alarms; FS42, -48 volt power control, fusing, and alarms; FS43, power sequencing; FS44, alarm and test; and FS45, scan points. The following paragraphs contain general information concerning SD-3H902-01.

+24 VOLT POWER CONTROL, FUSING, AND ALARMS (FS41 OF SD-3H902-01)

5.03 The control frame circuit separately distributes +24 volts to each MLPWB in the peripheral control circuit when each PWR relay is operated. Each power lead is fused with a 70-type fuse. When the fuse opens, an auxiliary circuit is

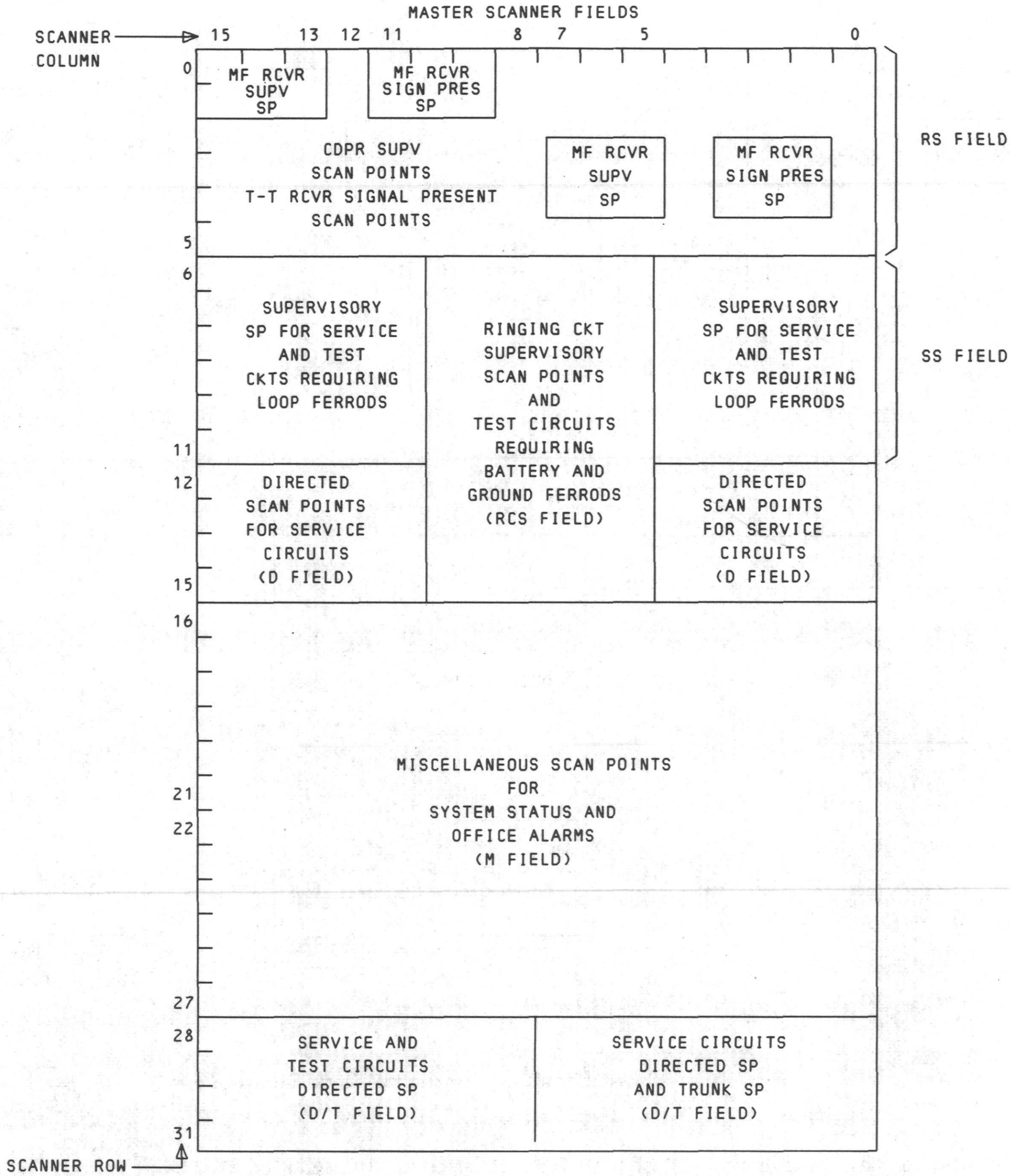


Fig. 15—Master Scanner Ferrod Array Layout

completed which provides +24 volts to operate one of the 24FA relays. Separate fuses exist in the fuse panels for peripheral control circuits 0 and 1. In addition to distributing +24 volts to all four A8 power converters, the control frame circuit starts the converters by switching +24 volts to their 24VST lead. The switching occurs under the following conditions: the 24ST relay operated, the 24FA relay released, and the 48FA relay released.

-48 VOLT POWER CONTROL, FUSING, AND ALARMS (FS42 OF SD-3H902-01)

5.04 The control frame circuit separately distributes -48 volts to a large number of individually

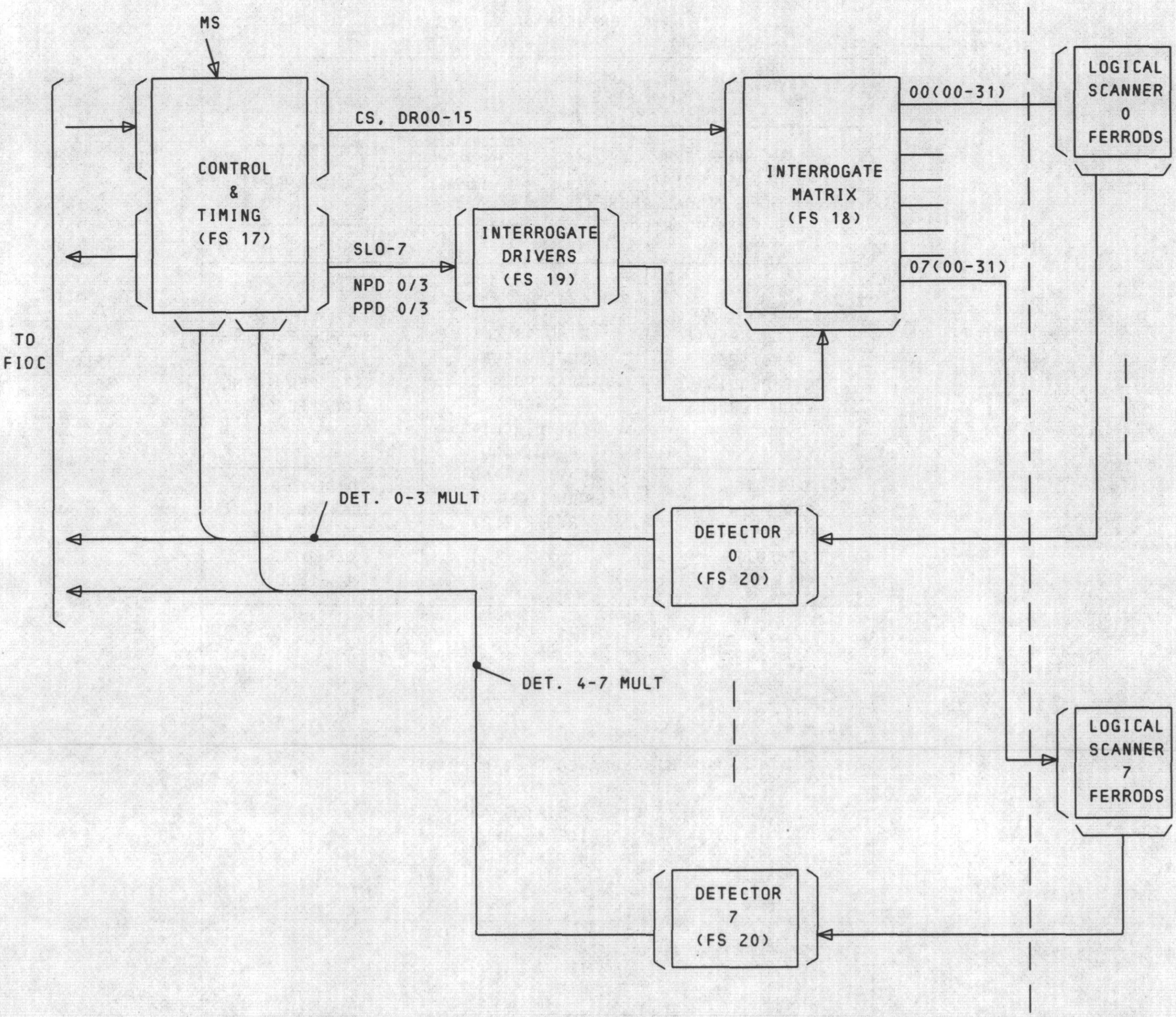


Fig. 16—Scanner Controller Functional Block Diagram

fused circuits in the periphery. When a fuse opens, the auxiliary circuit operates one of the 48FA relays or one of the SFA relays. The 48FA relays are only operated by the fuses on the lines distributing -48 volts to the A8 power converters. Any of the remaining -48 volt fuses, when blown, will operate the SFA relays.

POWER SEQUENCING (FS43 OF SD-3H902-01)

5.05 Each set of A8 power converters is started by depressing the associated ON (NLK) key on the control panel, which provides a ground path to operate the associated 24ST relay. The associated set of power converters must supply +3 volts to a transistor circuit before it can provide a ground path to operate the appropriate PWR relay. This relay keeps the 24ST relay operated after the ON (NLK) key is released. The PWR OFF lamp is extinguished, while the OOS (out of service) lamp remains lighted. When the REQ (NLK) key is depressed, the request ferrod scan point notifies software to run diagnostics on the peripheral controllers. Once diagnostics are complete, the controllers are restored to service. The OOS lamp is extinguished when the peripheral decoder releases

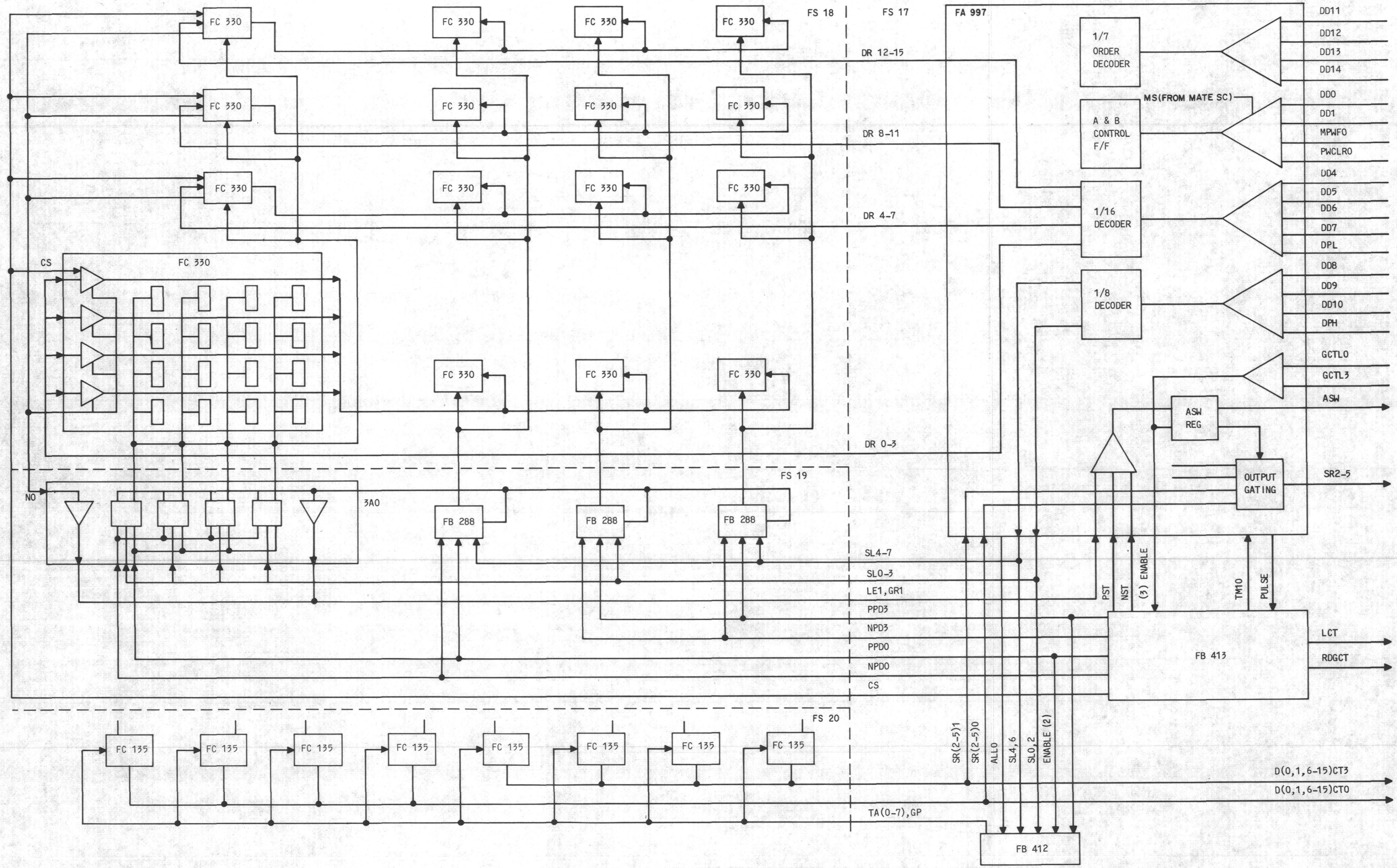


Fig. 17—Scanner Controller Functional Block Diagram—Detailed

ORDER	REPLY FORMAT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ORDER TYPE
		ORDER					LS			ROW								
12	A	0	1	1	0	0	V	V	V	H	H	H	H	A	A	A	A	NORMAL SCAN
0	A	0	0	0	0	0	V	V	0	X	X	X	X	A	A	A	A	ALL ZEROS
0	A	0	0	0	0	0	V	V	1	X	X	X	X	A	A	A	A	ALL ONES
3	B	0	0	0	1	1	V	V	V	H	H	H	H	A	A	A	A	ASW STATUS
3	B	0	0	0	1	1	V	V	V	H	H	H	H	B	B	B	B	<1 HORIZ
3	B	1	0	0	1	1	V	V	V	H	H	H	H	A	A	A	A	<1 VERT
10	B	0	1	0	1	0	V	V	V	H	H	H	H	A	A	A	A	>1 HORIZ (HHHH ≠ 0000)
5	B	0	0	1	0	1	V	V	V	H	H	H	H	A	A	A	A	>1 VERT (VVV ≠ 000)
6	C	X	0	1	1	0	X	X	X	X	X	X	X	X	X			LOAD (BIT 1 ——► A1-FF, BIT 0 ——► B1-FF)
9	C	X	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	TRANSFER

AAAA = ANY COMBINATION OF BITS HAVING EVEN PARITY.

BBBB = ANY COMBINATION OF BITS HAVING ODD PARITY.

X = NOT SIGNIFICANT

H = INPUT TO 1/16 HORIZONTAL (DRO-15) DECODER.

V = INPUT TO 1/8 VERTICAL (SLO-7) DECODER.

Fig. 18—Scan Order Formats

the OOS relay. The circuitry for removing power operates in practically the same way. When the REQ (NLK) key associated with the off-line peripheral controllers is depressed, software responds by removing the controllers from service and lighting the OOS lamp. Once the OFF (NLK) key is depressed, a transistor circuit releases the PWR and 24ST relays, lights the PWR OFF lamp, and disables the A8 power converters. Should emergency removal of power be required, depressing the REQ (NLK) and OFF (NLK) keys simultaneously will force the A8 power converters to be disabled and the +24 volts to be removed from the peripheral control unit.

ALARM AND TEST (FS44 OF SD-3H902-01)

5.06 The lamp circuit has a lamp test capability. Depressing the LP & PWR TEST (NLK) key closes a circuit path to light both sets of OOS, PWR OFF, and FA lamps. Individually, the OOS lamp is lighted with the OOS relay operated; the PWR OFF lamp is lighted with the PWR relay released; and the FA lamp is lighted with the

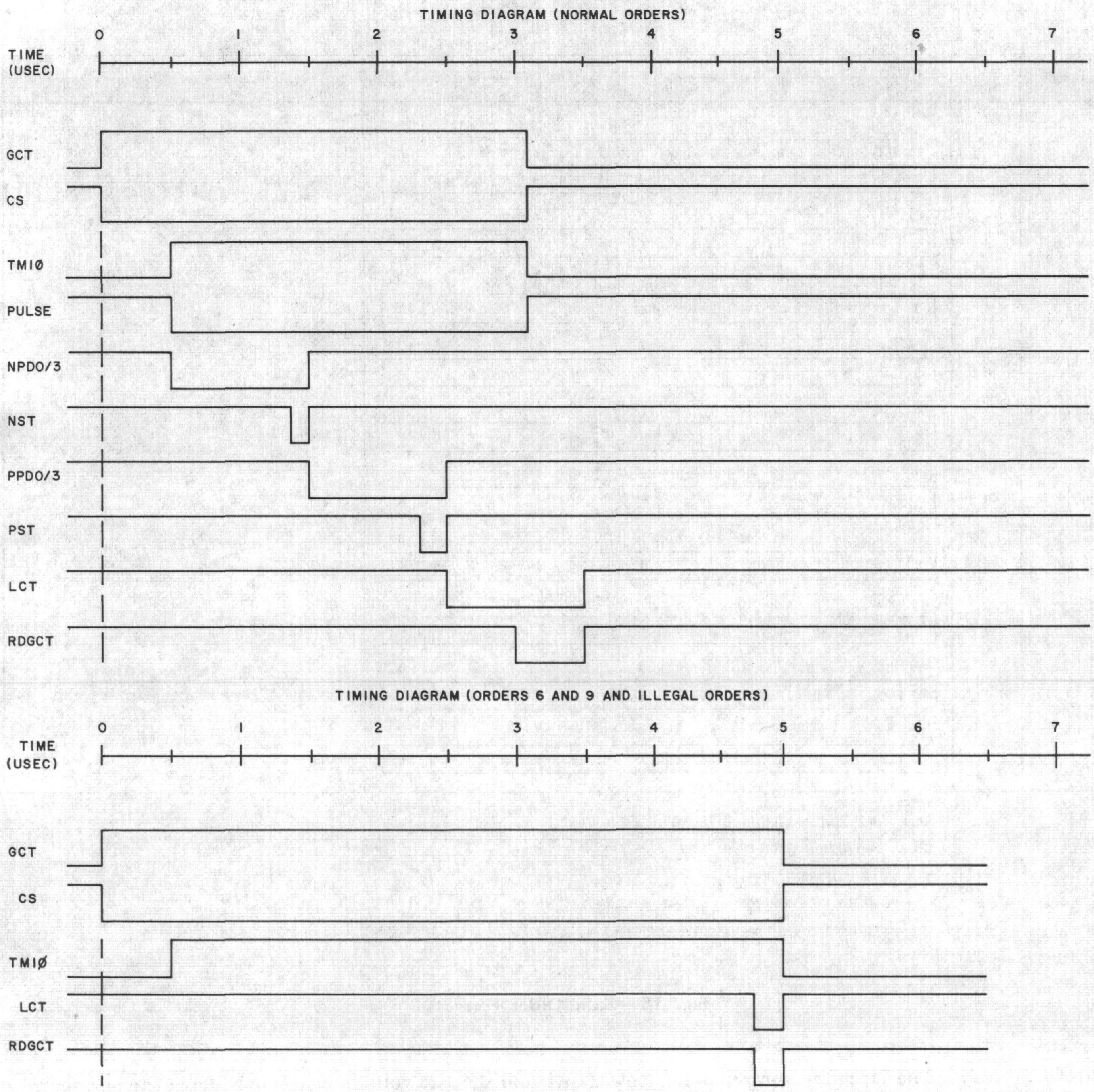


Fig. 19—Scanner Timing Diagram for Normal Order Sequence

24FA, 48FA, or SFA relay operated. The alarm circuit has the capability for a number of different alarms. The A8 power converters have an overvoltage and overcurrent fuse alarm (FA) signal. This FA signal is sent to the alarm circuit where a transistor switch operates the CFA relay. The alarm circuit keeps the CFA relay operated until released by depressing the LP & PWR TEST (NLK) key. This is necessary since the loss of one converter will shut off all power to one peripheral control unit. The A8 power converters and the FB152 reference board also have an out-of-voltage limits power

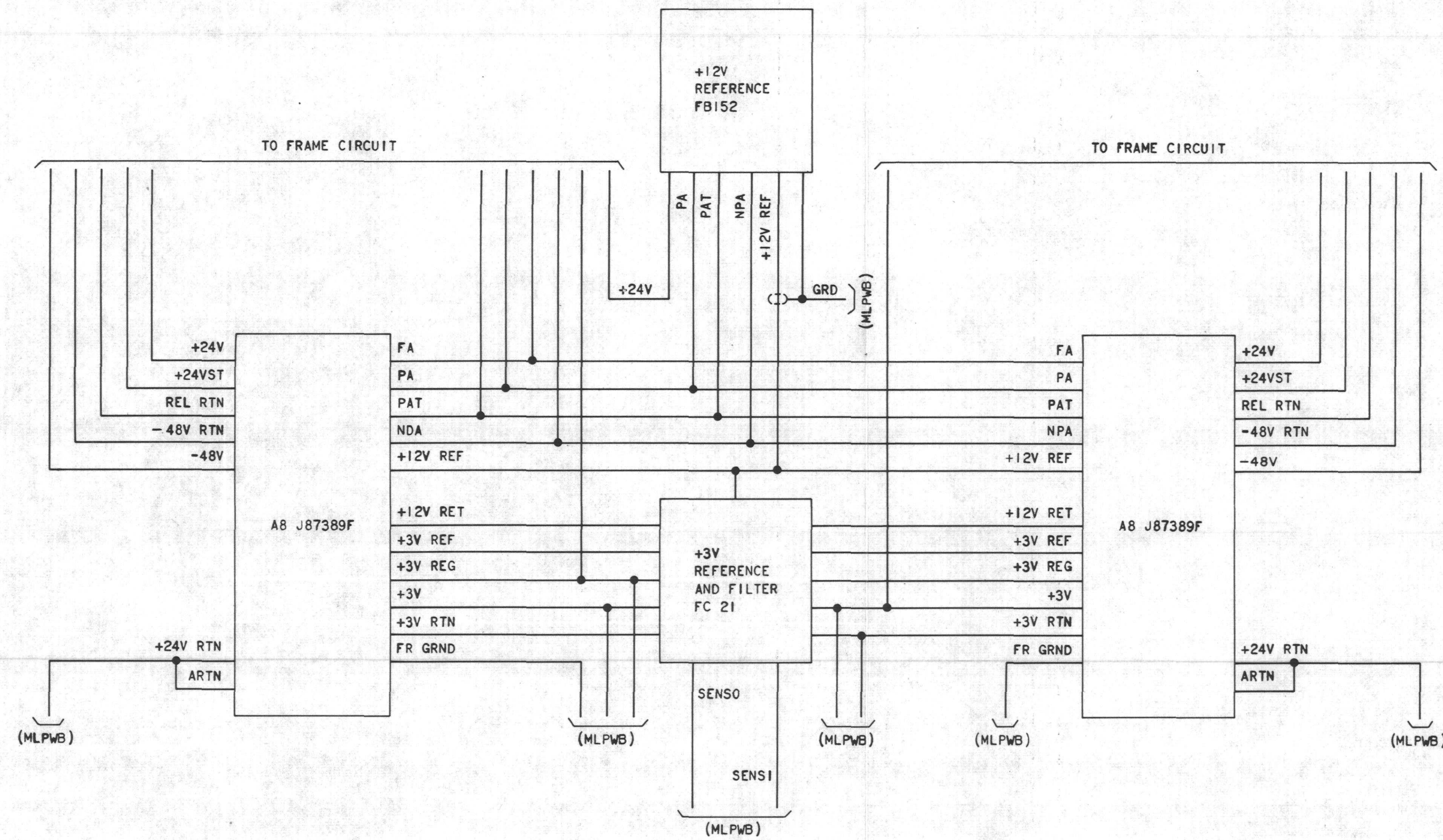


Fig. 20—+3 Volt Power Distribution

alarm (PA) signal. Similarly, this PA signal is sent to the alarm circuit where another transistor switch operates the CPA relay.

5.07 The alarm circuit has the facility for the power alarm test (PAT). The system via the peripheral decoder operates the PAT and OOS relays. A PAT signal is sent to the set of A8 power converters and the FB152 board. They should respond by operating the CPA relay and thus unsaturating the PA scan point. In the alarm circuit, the NPA relay operates only when an A8 or an FB152 fails to give a PA signal. The NPA relay then keeps the PA scan point saturated. As the PAT relay is released, a ground is briefly applied to the NPA leads of the A8 converters and FB152 reference board to extinguish the converters light emitting diodes (LEDs). If the OOS relay is released, then a PAT signal can also be generated by depressing the LP & PWR TEST (NLK) key. When the key is released, a ground is sent to extinguish the LEDs. When there is no PA signal, the associated LED fails to light. Scan points are not affected by a manual PAT.

SCAN POINTS (FS45 OF SD-3H902-01)

5.08 The scan point circuit contains three ferrods (request, power alarm, and major control alarm) which are concerned with power control and alarms. The state of certain relays and keys determines whether current flows in the ferrod control windings. The request ferrod is saturated with the 24ST relay operated and the REQ (NLK) key released. The power alarm ferrod is saturated with the 24ST relay operated and under any of the following conditions: the LP & PWR TEST (NLK) key depressed, the REQ (NLK) key depressed, the NPA relay operated, or the CPA relay released. The request and power alarm ferrods are encoded into four states (OFF, REQUEST, ON, and POWER ALARM). When both ferrods are unsaturated, the state is OFF. With the request ferrod unsaturated and the power alarm ferrod saturated, the state is REQUEST. When both ferrods are saturated, the state is ON. With the request ferrod saturated and the power alarm ferrod unsaturated, the state is POWER ALARM. The major control alarm ferrod is saturated with all three relays, CFA, 24FA, and 48FA, released. All three ferrods are duplicated for peripheral controllers 0 and 1.

6. MAINTENANCE

6.01 The SC has a number of checks that can be made under its control. Some checks are initiated each time a ferrod scan is requested. The other checks are initiated by special maintenance and status order codes. The responses of these special orders are used by software to locate the trouble. Fig. 21 contains the responses for each scan order code.

NORMAL ORDER CHECKS

6.02 The SC under normal conditions performs an ASW check. This check contains several subchecks in the various functional schematics (refer to Part 4). Summarizing the subchecks, the interrogate matrix checks to determine when more than one horizontal has been enabled. The interrogate current drivers check to determine when more than one or less than one driver for a vertical has been enabled. These drivers also detect the failure to select a horizontal in the interrogate matrix. All these checks are made twice, once for the negative (NPD) pulse and again for the positive (PPD) pulse. The check information is sent to the sequencer where it is converted to an ASW output.

6.03 The SC also performs two operational checks that are not a part of the ferrod scan request. These checks verify the operation of the data detector by returning either all zeroes or all ones to the 3A CC. The sequencer decodes the all-zeroes/all-ones write order and inhibits the outputs of the horizontal translator. As a result, no ferrods are pulsed and a less-than-type of ASW failure occurs. When address data bit 8 is a one, no zero signals are generated by the scanner test board and the data detectors normally return all ones to the 3A CC. When any zero is returned, this indicates a failure in any of four detector boards.

6.04 The scanner test board contains the circuitry to generate all-zero signals which are applied as inputs to a particular detector board. When the all-zeroes/all-ones write order is sent with address data bit 8 equal to zero, the horizontal translators are again inhibited and no ferrods are pulsed. However, in this case, the test board sends an all-zeroes signal to a particular detector board based on data received from the sequencer. This data consists of even vertical select signals (SL0, SL2, SL4, and SL6) and two vertical timing

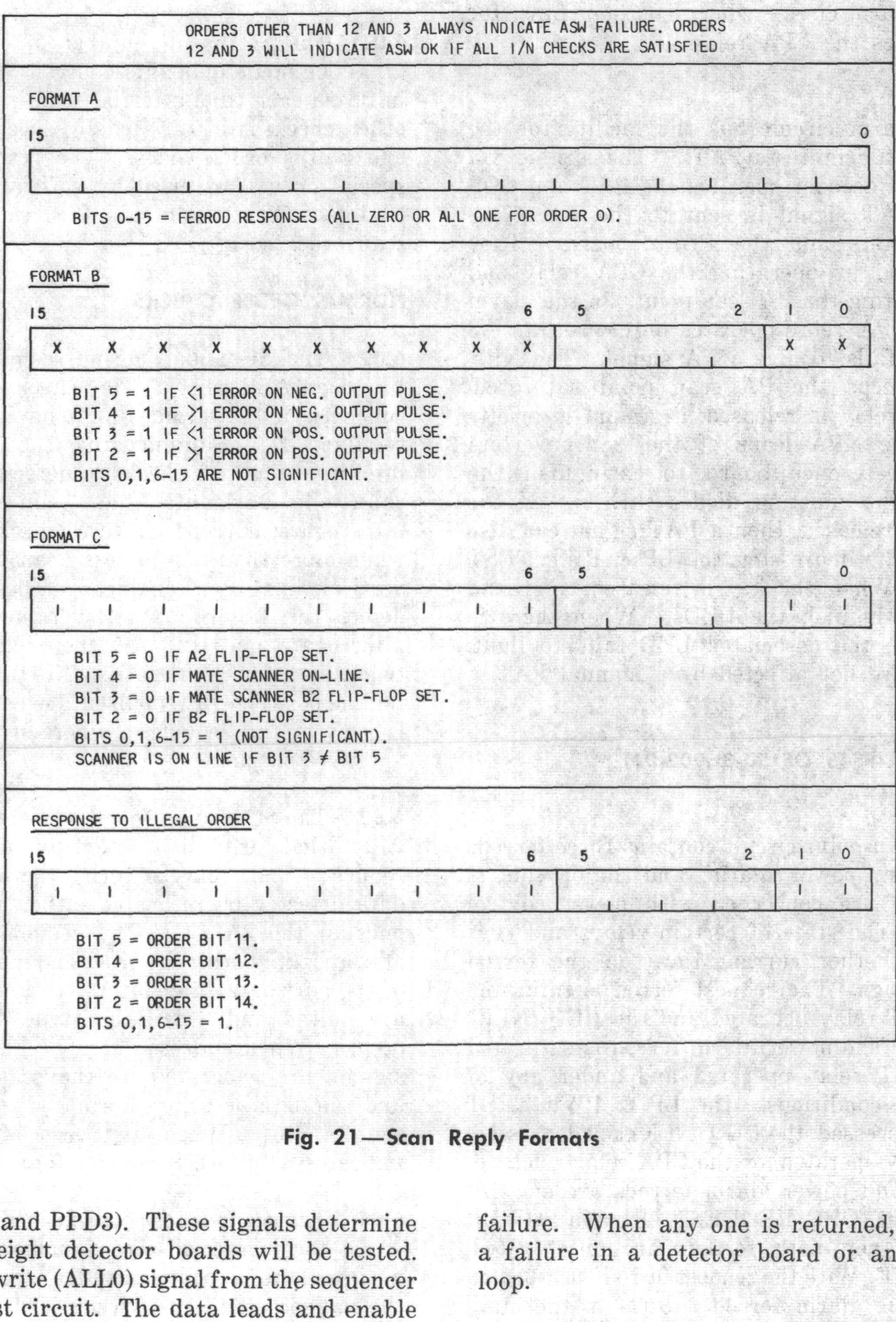


Fig. 21—Scan Reply Formats

signals (PPD0 and PPD3). These signals determine which one of eight detector boards will be tested. The all-zeroes write (ALL0) signal from the sequencer enables the test circuit. The data leads and enable signal select a particular transistor switch which, when energized, sends a current pulse to a detector board. This pulse is transformer-coupled into each of the 16 columns on the detector pack and will cause current to flow in each readout loop. The 16 detector outputs will pulse low, and all zeroes are returned to the 3A CC along with an ASW failure. When any one is returned, this indicates a failure in a detector board or an open readout loop.

6.05 The all-zeroes and all-ones write orders use the same order code, but the column address sent with the order is different. When an even address is sent (data bit 8 equals 0), the test board is activated and an all-zeroes response is returned. When an odd address is sent (data bit 8 equals 1), the test board is not activated and an all-ones response is returned. Since these orders inhibit the interrogate row translator, the subsequent 0/N row selection results in a less-than-type ASW failure being returned.

MAINTENANCE ORDER CHECKS

6.06 Through the use of diagnostic programs, the 3A CC can perform maintenance checks on the SC. The SC can read failure information out of the two 2-bit registers in the sequencer and can also force ASW failures in the horizontal and vertical selection. The order codes used are the ASW status order, the 2/N horizontal order, and the 2/N vertical order.

6.07 The ASW status order performs much like the normal scan order except that bits 2 through 5 of the reply do not come from the detector outputs but from the two 2-bit registers which contain the results of the ASW checks. This order is also used to test the 0/N selection checks by disabling the decoders using the parity technique described in 6.10 and 6.11.

6.08 The 2/N horizontal order performs like the ASW status order except that the output of the order decoder is used to force on the zero output of the horizontal decoder. If a horizontal address other than zero is sent in the order, two horizontals will be selected. This results in an ASW failure, and bits 2 and 4 of the reply will be one, indicating a greater-than-one error on the positive and negative pulses, respectively.

6.09 In a similar manner, the 2/N vertical order forces on the zero output of the vertical decoder. If a vertical address other than zero is sent in the order, two verticals will be selected. This results in an ASW failure, and bits 2 and 4 of the reply will be ones.

6.10 The SC has the ability to cause 0/N selection errors by making use of the interaction between the unused bits in the scanner order word and the machine-generated parity bits which accompany the order. Data bit 15 is used to affect parity bit D_{PH} which connects to the vertical decoder. Data bits 0 through 3 are used to affect parity bit D_{PL} which connects to the horizontal decoder.

6.11 The vertical decoder receives its input from data bits 8 through 10 and bit D_{PH}. If data bit 15 is set to one in an otherwise normal order, the 3A CC will maintain parity in the high half of the word by inverting D_{PH}. This results in an invalid bit pattern being fed to the vertical decoder, causing no output to be selected. Similarly, placing an odd-parity combination in data bits 0 through 3 will affect bit D_{PL} and cause a failure in the horizontal decoder, which receives its input from data bits 4 through 7 and D_{PL}. Either of these cases results in an ASW failure. If the order code is 0011 (ASW status), then bits 3 and 5 of the reply will be one, indicating a less-than-one error on the positive and negative pulses, respectively.

STATUS CONTROL ORDERS

6.12 The SC also has two status orders that control the operational state; i.e., active or standby. These are the load (status) and transfer (status) orders. The load order loads data bits 0 and 1 into the B1 and A1 flip-flops, respectively. The transfer order gates this data from the first-level flip-flops into the B2 and A2 flip-flops. These second-level flip-flops control the operational status of the SC and its mate SC.

6.13 The status of the SC is controlled by its A2 flip-flop and the B2 flip-flop of the mate SC. If these two flip-flops are in the same state, the status of the SC is standby. If they are different, the SC is active. Similarly, the SC B2 flip-flop and the mate SC A2 flip-flop control the status of the mate SC. While the SC is in standby condition, a status signal inhibits the horizontal and vertical decoders and the timing chain, preventing any interference with the active SC through the ferrod matrix.

6.14 The response to the load and transfer orders is as follows: bit 2 equals 0 if the B2 flip-flop is set; bit 3 equals 0 if the B2 flip-flop in the mate SC is set; bit 4 equals 0 if the mate SC is in the active state; and bit 5 equals 0 if the A2 flip-fop is set. The status orders are used by the software performing initialization, diagnostics, and recovery.

7. REFERENCES

7.01 The following Bell System Practices apply to this section.

Section	Title
966-210-100	General Description—No. 3 ESS
233-121-110	Frame Input/Output Controller Description and Theory of Operation
233-120-100	Switching Network Description and Theory of Operation
233-142-000	Task Oriented Practices Maintenance Volumes
233-151-125	Input Processing and Scanning
233-151-130	Call Processing
233-151-150	Translations

8. GLOSSARY

8.01 A glossary of terms is provided to aid in the understanding of definitive words used in this section.

Bipolar Pulse—A pulse that may have either positive or negative polarity

DATA DETECTORS—The circuit that detects the output of the ferrods

ERROR—Less-Than Type—An error where selection of m/N is desired and an actual selection of less than m is made

ERROR—Greater-Than Type—An error where selection of m/N is desired and an actual selection of greater than m is made

Ferrod Array—All the ferrod sensors that comprise a single No. 3 ESS scanner

Ferrod Sensor—The stick of ferrite and associated windings that act as a current sensing device

Ground Start—Usually lines that originate at a PBX or coin station, whereby the presence of ground provides a method of signaling for originations

Interrogate—Determining if a system action is necessary, depending upon whether a scan point has a service request

Interrogate Current Driver—The circuit that generates the bipolar current pulse sent to the transformer matrix

Interrogate Matrix—A 16-by-16 transformer matrix that sends the interrogate pulse to the ferrods

Loop Start—Signaling methods which use the metallic loop formed by the trunk conductors and terminating bridges

Scan Point—A scanning address (in binary form) of a line or a trunk

Scanner Controller—The circuit that controls the interrogation of the ferrod array

System Control—The combination of the 3A CC, main store, FIOC, scanner controller, network controller, and peripheral pulse distributor that comprises the portion of the system which is switchable as a single unit

Translation—The conversion of information received in one form to another form (for example, in switching machines the translation of digits received to those required to complete a call)

70-Type Fuse—A small fuse containing a spring which, upon release by the fusing wire, completes an auxiliary circuit to operate an alarm