# PERIPHERAL PULSE DISTRIBUTOR AND
# PERIPHERAL DECODER
# DESCRIPTION AND THEORY OF OPERATION
# NO. 3 ELECTRONIC SWITCHING SYSTEM

| CONTENTS | PAGE |
|---|---|

| CONTENTS | PAGE |
|---|---|

## 1. GENERAL

**1.01** This section provides the description and theory of operation of the peripheral pulse distributors (PPDs) and the peripheral decoders (PDs) as applied in the peripheral equipment of the No. 3 Electronic Switching System (ESS).

**1.02** When this section is reissued, the reason for reissue will be contained in this paragraph.

### PURPOSE

**1.03** The PPD receives data from the 3A central control (3A CC) via the frame input/output controller (FIOC). The PPD transmits data to a PD which determines the state of trunk, junctor, and service circuit state relays as directed by the 3A CC.

### CONFIGURATION

**A. Peripheral Pulse Distributor**

**1.04** The PPDs are duplicated in the No. 3 ESS. Two PPDs are located on each control frame as part of the peripheral controllers (Fig. 1A and 1B). One PPD on each control frame and its associated FIOC function under the control of 3A CC 0. The duplicate PPD and FIOC function under control of 3A CC 1.

**B. Peripheral Decoder**

**1.05** The PDs are located on control, network, test, and miscellaneous frames near their associated relays (Fig. 1B, 1C, 1D, 1E, and 1F). Two PD circuits are mounted together on one circuit pack and are referred to as a peripheral decoder group (PDG).

**1.06** Peripheral decoders are not duplicated; each PD receives data from either of the peripheral

LEGEND:
FIOC = FRAME INPUT OUTPUT CONTROLLER
NC = NETWORK CONTROLLER
PPD = PERIPHERAL PULSE DISTRIBUTOR

**Row 1 (top band)**

| Col | Code | Function |
|---|---|---|
| 2 | FC 330 | SCAN INTERROGATE MATRIX |
| 3 | FC 330 | SCAN INTERROGATE MATRIX |
| 4 | FC 330 | SCAN INTERROGATE MATRIX |
| 5 | FC 330 | SCAN INTERROGATE MATRIX |
| 7 | FB 288 | INTERROGATE CURRENT DRIVER |
| 8 | FC 330 | SCAN INTERROGATE MATRIX |
| 9 | FC 330 | SCAN INTERROGATE MATRIX |
| 10 | FC 330 | SCAN INTERROGATE MATRIX |
| 11 | FC 330 | SCAN INTERROGATE MATRIX |
| 13 | FB 288 | INTERROGATE CURRENT DRIVER |
| 14 | FC 330 | SCAN INTERROGATE MATRIX |
| 16 | FC 330 | SCAN INTERROGATE MATRIX |
| 17 | FC 330 | SCAN INTERROGATE MATRIX |
| 18 | FC 330 | SCAN INTERROGATE MATRIX |
| 20 | FB 288 | INTERROGATE CURRENT DRIVER |
| 21 | FC 330 | SCAN INTERROGATE MATRIX |
| 22 | FC 330 | SCAN INTERROGATE MATRIX |
| 23 | FC 330 | SCAN INTERROGATE MATRIX |
| 24 | FC 330 | SCAN INTERROGATE MATRIX |
| 26 | FB 288 | INTERROGATE CURRENT DRIVER |
| 34 | FB 152 | 12V REFERENCE |
| 35 | +3V DC–DC CONV | CONVERTER |
| 40 | +3V DC–DC CONV | CONVERTER |

**Row 2**

| Col | Code | Function |
|---|---|---|
| 4 | FC 135 | SCAN DETECTOR |
| 6 | FC 135 | SCAN DETECTOR |
| 8 | FB 412 | SCAN TEST CKT |
| 11 | FC 135 | SCAN DETECTOR |
| 13 | FC 135 | SCAN DETECTOR |
| 16 | FB 413 | SCAN TIMER CKT |
| 19 | FC 135 | SCAN DETECTOR |
| 21 | FC 135 | SCAN DETECTOR |
| 25 | FC 135 | SCAN DETECTOR |
| 27 | FC 135 | SCAN DETECTOR |
| 31 | FC 206 | PPD MATRIX |
| 32 | FC 206 | PPD MATRIX |
| 33 | FC 206 | PPD MATRIX |
| 34 | FC 206 | PPD MATRIX |
| 35 | FC 206 | PPD MATRIX |
| 36 | FC 206 | PPD MATRIX |
| 37 | FC 206 | PPD MATRIX |
| 38 | FC 206 | PPD MATRIX |

**Row 3**

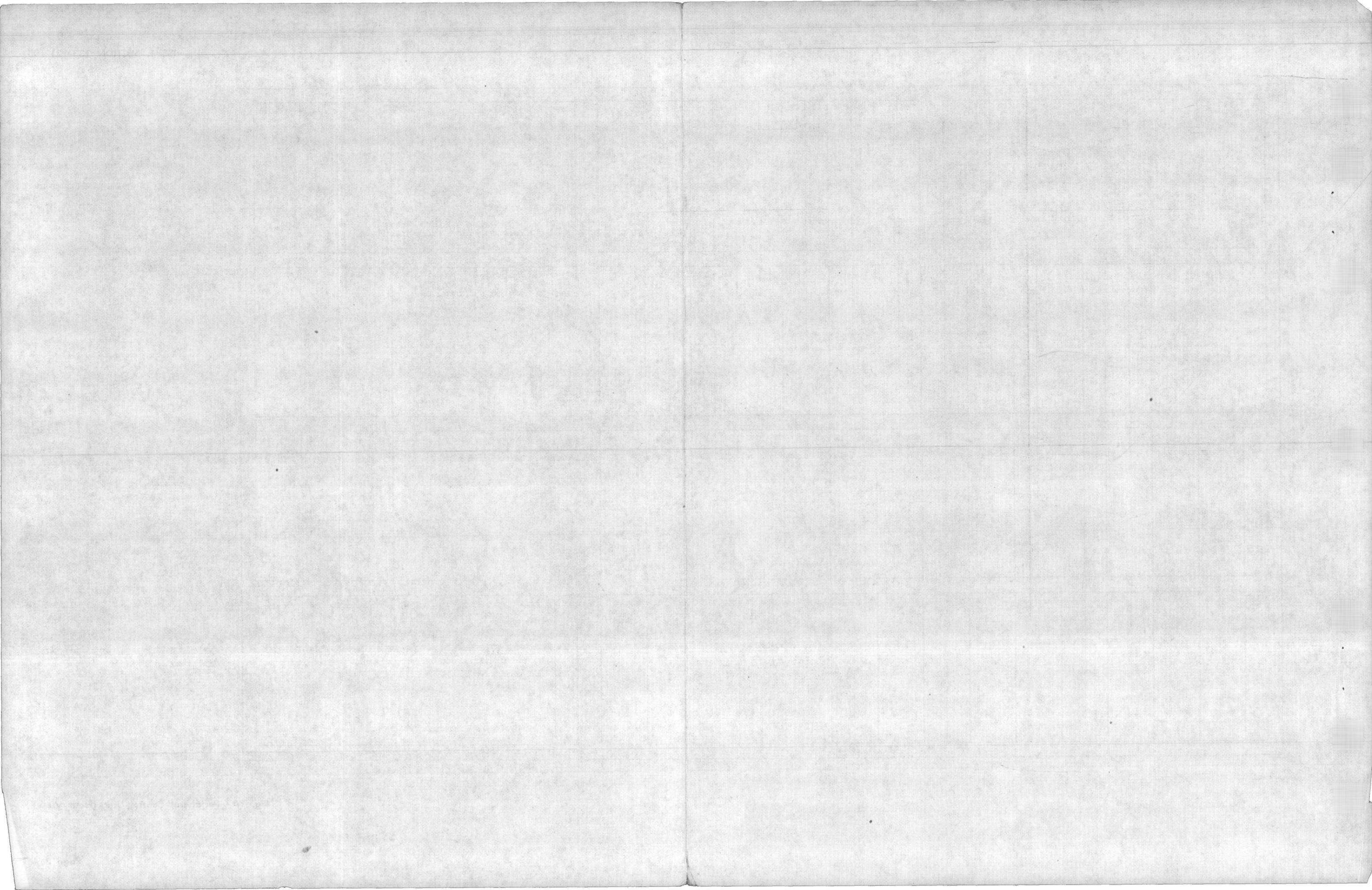| Col | Code | Function |
|---|---|---|
| 1 | FC 21 | 3V REFERENCE AND FILTER CKT |
| 3 | FA 998 | NC INPUT LEVEL AND MISC. DECODER |
| 4 | FA 999 | NC SWITCH OR LEVEL DECODER |
| 5 | FA 999 | NC SWITCH OR LEVEL DECODER |
| 6 | FA 1000 | NC CONCENTRATOR GROUP DECODER |
| 7 | FA 1000 | NC CONCENTRATOR GROUP DECODER |
| 8 | FA 1001 | NC CONTROL LOGIC |
| 11 | FA 997 | SCAN CONTROL |
| 12 | FA 993 | FIOC SEQUENCE CONTROLLER |
| 13 | FB 351 | FIOC RECEIVER TRANSMITTER |
| 14 | FA 994 | FIOC REGISTER |
| 16 | FA 994 | FIOC REGISTER |
| 18 | FA 995 | PPD SEQUENCER |
| 19 | FA 996 | PPD VERTICAL TRANSLATOR |
| 22 | FC 207 | PPD LEVEL CONTROL |
| 23 | FC 205 | PPD VERTICAL DRIVER |
| 24 | FC 205 | PPD VERTICAL DRIVER |
| 25 | FC 205 | PPD VERTICAL DRIVER |
| 27 | FC 204 | PPD HORIZONTAL |
| 29 | FC 204 | PPD HORIZONTAL |
| 31 | FC 206 | PPD MATRIX |
| 32 | FC 206 | PPD MATRIX |
| 33 | FC 206 | PPD MATRIX |
| 34 | FC 206 | PPD MATRIX |
| 35 | FC 206 | PPD MATRIX |
| 36 | FC 206 | PPD MATRIX |
| 37 | FC 206 | PPD MATRIX |
| 38 | FC 206 | PPD MATRIX |

**Row 4 (bottom band)**

| Col | Code | Function |
|---|---|---|
| 2 | FC 193 | NC NODE SELECT |
| 4 | FC 193 | NC NODE SELECT |
| 6 | FB 421 | NC TIMING AND GUARD CONTROL |
| 8 | FB 409 | POWER CONTROL |
| 10 | FC 229 | NC 16V SUPPLY |
| 11 | FC 219 | NC GROUP CHECKS |
| 13 | FC 188 | NC OUTPUT GROUP SELECT |
| 17 | FB 404 | NC INPUT GROUP SELECT |
| 19 | FB 404 | NC INPUT GROUP SELECT |
| 21 | FB 405 | NC HIGH AND DRY SELECT |
| 23 | FB 405 | NC HIGH AND DRY SELECT |
| 25 | FB 406 | NC STAGE THREE GROUP SELECT |
| 26 | FC 307 | NC GATE SELECT |
| 28 | FC 307 | NC GATE SELECT |
| 29 | FC 307 | NC GATE SELECT |
| 32 | FC 307 | NC GATE SELECT |
| 33 | FC 307 | NC GATE SELECT |

Fig. 1A—Peripheral Control Unit (Front View)

THIRD STAGE
NETWORK AND
ACCESS

PERIPHERAL
CONTROLLERS

PERIPHERAL
CONTROLLERS

CONTROL PANEL

PULSER

TEST VERTICAL
UNIT

MASTER SCANNER
TERMINAL STRIP
UNIT

PERIPHERAL DECODER

MULTIFREQUENCY
TRANSMITTER
CIRCUITS

MASTER SCANNER
MATRIX UNIT

CUSTOMER DIAL PULSE
RECEIVER / REGULAR
RINGING CIRCUITS
OR UNIVERSAL
TRUNK CIRCUITS

CUSTOMER DIAL PULSE
RECEIVER / REGULAR
RINGING CIRCUITS

FUSE UNITS

TONE, COIN
CONTROL, RECORDED
ANNOUNCEMENT AND
REMOTE RECORDED
ANNOUNCEMENT
CIRCUITS

**Fig. 1B—Control Frame**

pulse distributors depending on which 3A CC is active. Each PD is dedicated exclusively to the control of 12 state relays. Each peripheral decoder is typically associated with up to four trunk, junctor, or service circuits.

## 2. PHYSICAL DESCRIPTION

**2.01** PPDs and PDs are provided on circuit packs. They are arranged for plug-in installation in apparatus mountings on the equipment frames (Fig. 1A and 1C).

## PERIPHERAL PULSE DISTRIBUTOR

**2.02** Each PPD requires up to 24 circuit packs. These circuit packs are broken down into six different types (3.02).
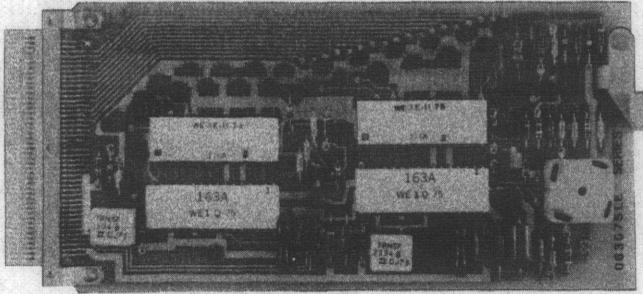
Fig. 1C—Peripheral Decoder

## PERIPHERAL DECODER

**2.03** Two PDs are mounted together on one replaceable circuit board and are referred to as a peripheral decoder group (PDG). Each circuit board provides 24 outputs.

## GROWTH

**2.04** When office capacity requires eight or more network frames, a second control frame must be added. This second control frame will be equipped with two PPDs and will accommodate network frames 8 through 15. An office equipped with 7 network frames can have up to 256 PDs. Since the main growth of an office is the addition of network and miscellaneous frames, growth for the PDs will be determined by the addition of each frame.

## INTERFACES

### A. Peripheral Pulse Distributor

**2.05** The PPDs interface with the 3A CC via the FIOC. Parallel data is transmitted between the FIOC and PPD via a data bus. Within the PPD, this data is used to select 1 of 256 PDs. The PPD sends a positive or negative pulse to the selected PD. One order from the 3A CC is required to send one pulse to the PD. Seven orders from the 3A CC are required to supply the seven input pulses needed by the PD. In the No. 3 ESS system, the relationship between the PPD, PD, and associated circuitry is shown in Fig. 2.

### B. Peripheral Decoder

**2.06** The PDs interface with the 3A CC via the PPD through the FIOC. The input signals from the PPD are low-speed serial bipolar pulses. These pulses are used to select a group of three relays called a triplet and set them in the desired state.

**2.07** The relays selected are located on the junctors, service circuits, special line circuits, ringing and tone plant, trunk and test circuits, and other circuits as required.

## 3. FUNCTIONAL DESCRIPTION

### PERIPHERAL PULSE DISTRIBUTOR

**3.01** Data is transmitted in parallel form to the PPD from the associated FIOC.

**3.02** The PPD consists of the following functional circuit packs (Fig. 3).

| QUANTITY | CIRCUIT PACK |
|---|---|
| 1 | Control and timing, and horizontal translator (FA995) |
| 1 | Vertical translator (FA996) |
| 3 | Vertical driver (FC205) |
| 2 | Horizontal driver (FC204) |
| 1 | Level control (FC207) |
| Up to 16 | Transformer matrix (FC206). |

**3.03** The control and timing, and horizontal translator circuit receives the portion of the data word necessary to provide timing and a 1-out-of-16 horizontal selection on the 16 by 16 transformer matrix. The horizontal translation circuit is interfaced to the transformer matrix by the horizontal driver.

**3.04** The vertical translator receives that portion of the data word necessary to provide a 1-out-of-32 vertical selection on the 16 by 16 transformer matrix. In addition to selecting the matrix column, the vertical translation determines which of the two primary windings of the matrix transformer is selected and thus the polarity of
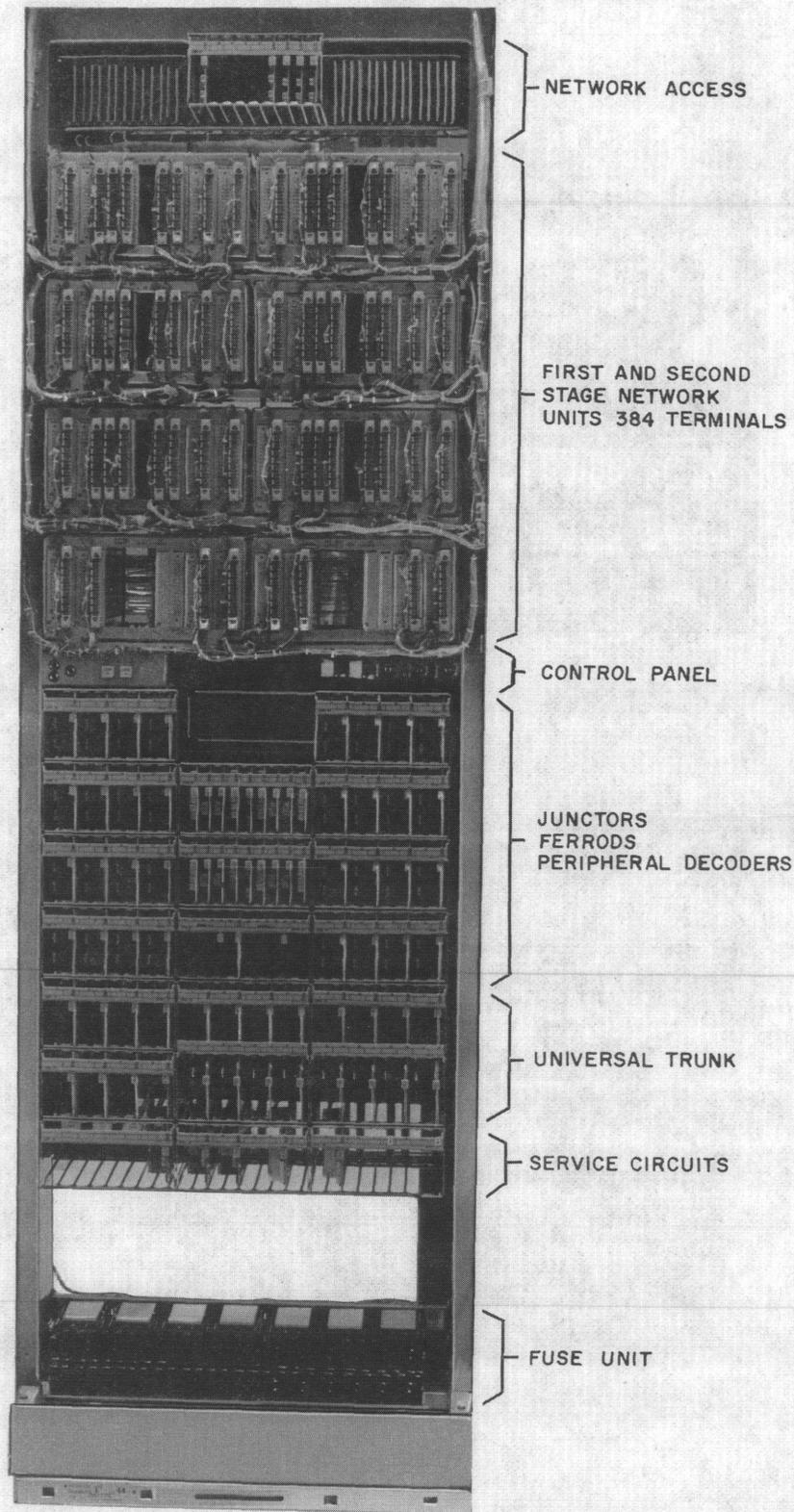
NETWORK ACCESS

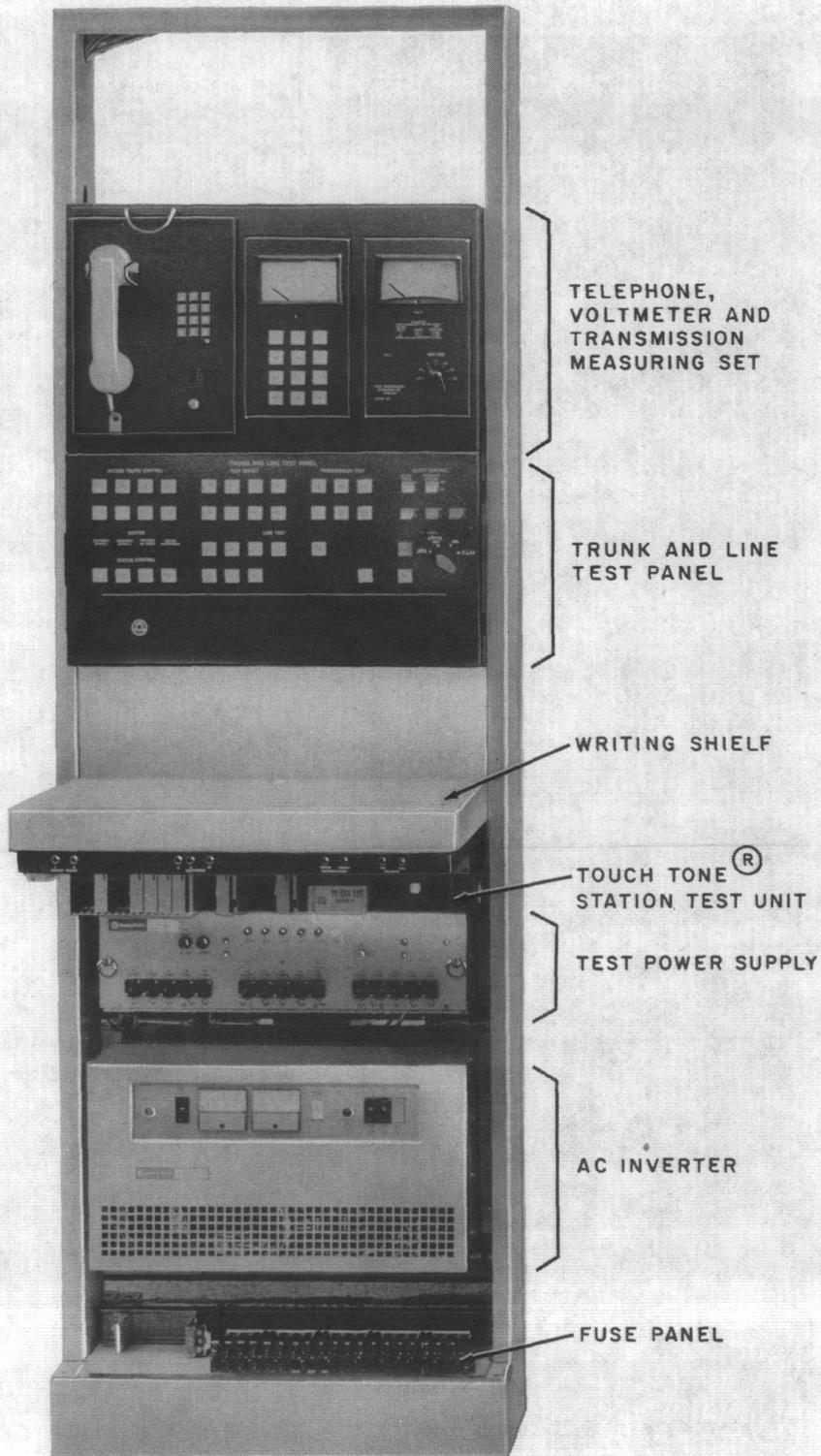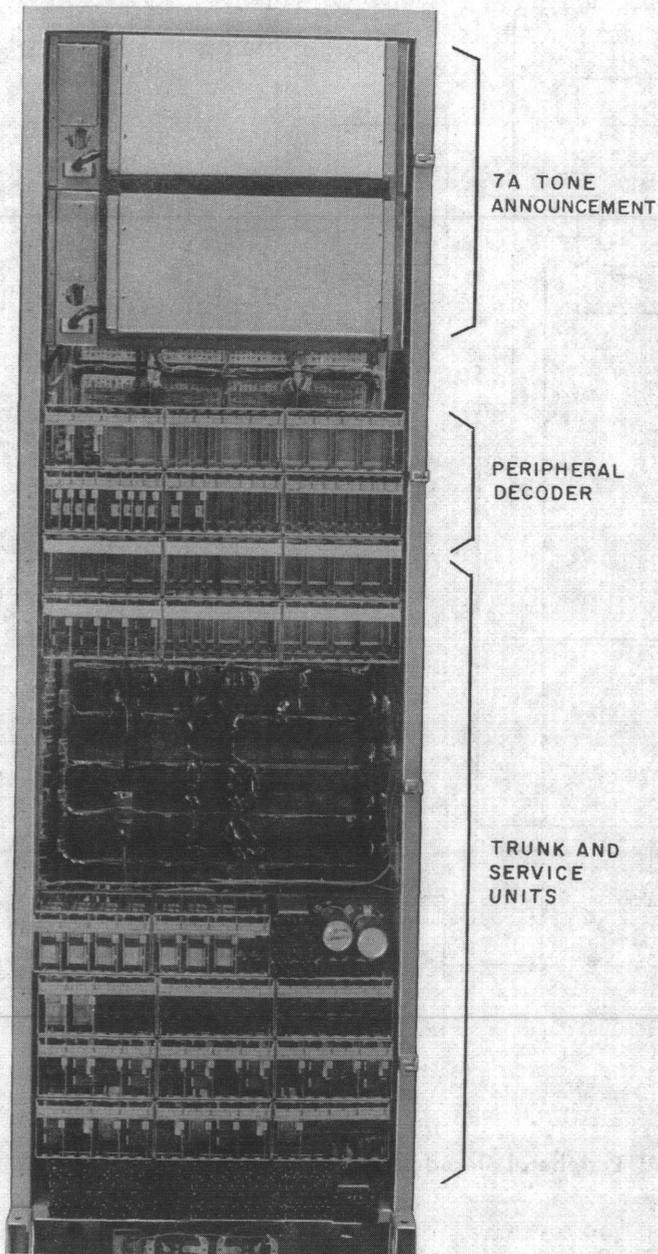FIRST AND SECOND
STAGE NETWORK
UNITS 384 TERMINALS

CONTROL PANEL

JUNCTORS
FERRODS
PERIPHERAL DECODERS

UNIVERSAL TRUNK

SERVICE CIRCUITS

FUSE UNIT

Fig. 1D—Network Frame

TELEPHONE,
VOLTMETER AND
TRANSMISSION
MEASURING SET

TRUNK AND LINE
TEST PANEL

WRITING SHIELF

TOUCH TONE®
STATION TEST UNIT

TEST POWER SUPPLY

AC INVERTER

FUSE PANEL

Fig. 1E—Test Frame

**Fig. 1F—Miscellaneous Frame**

(Figure labels: 7A TONE ANNOUNCEMENT, PERIPHERAL DECODER, TRUNK AND SERVICE UNITS)

the output pulse. The vertical translator is interfaced to the transformer matrix by the vertical driver.

**3.05** The level control circuit provides necessary maintenance checks to the transformer matrix, monitors current through the matrix, and provides a 16-volt supply to drive transformers in the matrix.

**3.06** The selected transformer in the matrix sends out low-speed serial bipolar pulses to a peripheral decoder.

## PERIPHERAL DECODER

**3.07** The data is transmitted in serial bipolar pulses from the PPD to the PD.

**3.08** The PD (Fig. 4) consists of the following:

- Transformer

- Shift register

- A 1-out-of-4 translator

- Four buffers.

**3.09** Incoming pulses are detected by the transformer and placed into the 7-bit shift register. These bits are received sequentially.

**3.10** Upon receipt of the last data bit, the shift register gates the stored information into one of the four buffers.

**3.11** Within each buffer, the necessary circuitry is provided to receive and store the data from the shift register and, according to the data received, control three state relays. The relays are typically located on one trunk, junctor, or service circuit.

## 4. THEORY OF OPERATION

### PERIPHERAL PULSE DISTRIBUTOR

**4.01** The PPD receives 16 data bits (Fig. 5) from the FIOC. This data is used to make a 1-out-of-16 horizontal selection and a 1-out-of-32 vertical selection. It is also used for testing and maintenance within the PPD.

**4.02** Each PPD consists of the following circuit packs (Fig. 3):

- Control and timing, and horizontal translator (FA995)

- Vertical translator (FA996)
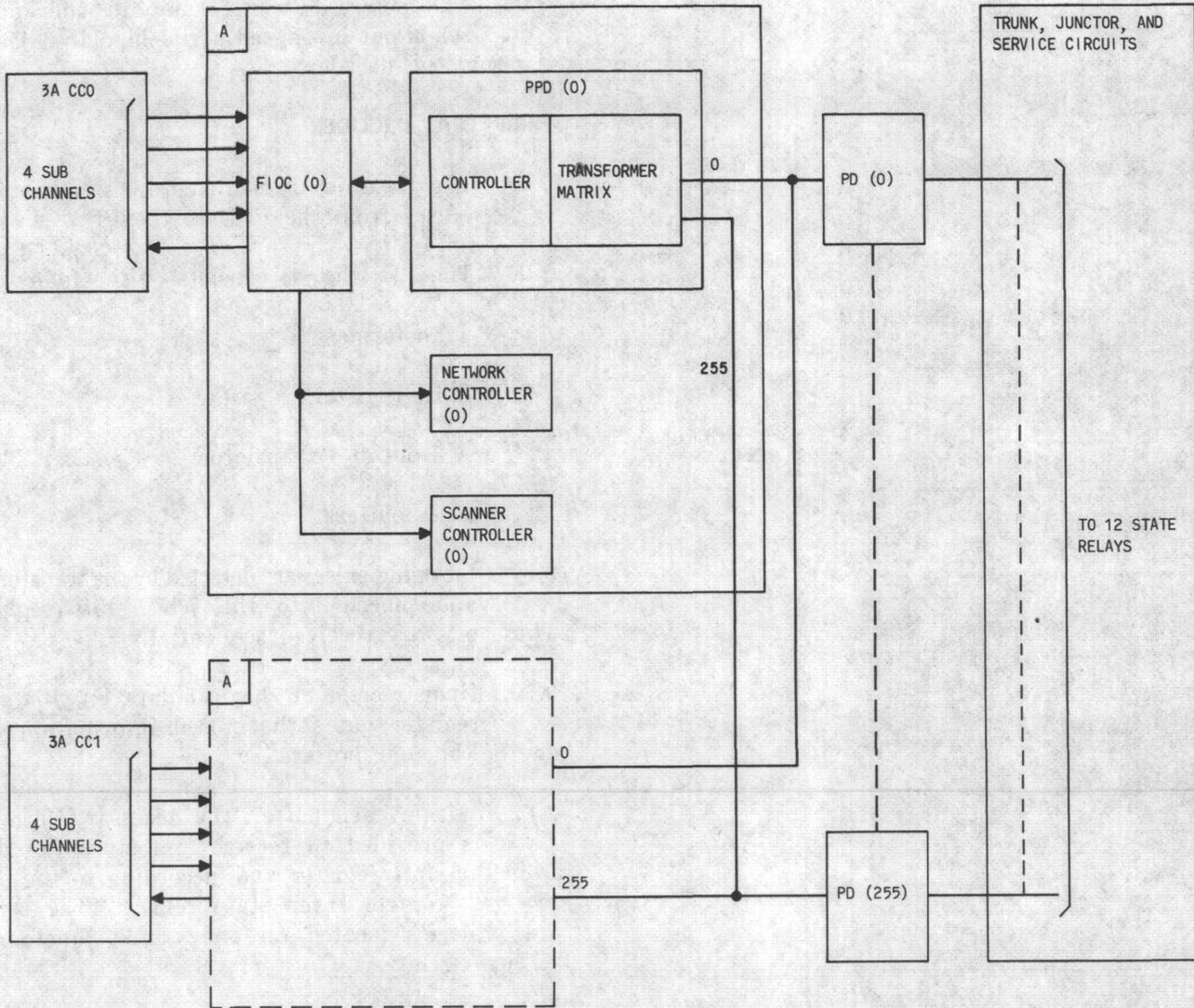
- Horizontal drivers (FC204)

**Fig. 2—Peripheral Pulse Distributor and Peripheral Decoder—Interface**

- Vertical drivers (FC205)

- Transformer matrix (FC206)

- Level control (FC207).

## A. Control and Timing, and Horizontal Translator (FA995)

**Control and Timing Circuit**

**4.03** The control and timing circuit controls the timing sequence within the PPD. Timing is accomplished by the use of a state register (Fig. 6). This state register consists of six flip-flops A, B, C, D, E, and F. The enable signal (GCTL1) is received from the FIOC and is fed to each of these six flip-flops to clear them whenever the circuit is not enabled. The clock pulse SCLK0 is derived from CLK81 which is received from the FIOC. This clock pulse drives each of the six flip-flops (A, B, C, D, E, and F) in the state register.

**4.04** This state register acts as a shift counter. The output of each flip-flop drives the input of the next flip-flop. The complement of the F flip-flop is fed back to the A flip-flop input. Each 1-to-0 transition in the clock pulse (SCLK0) will
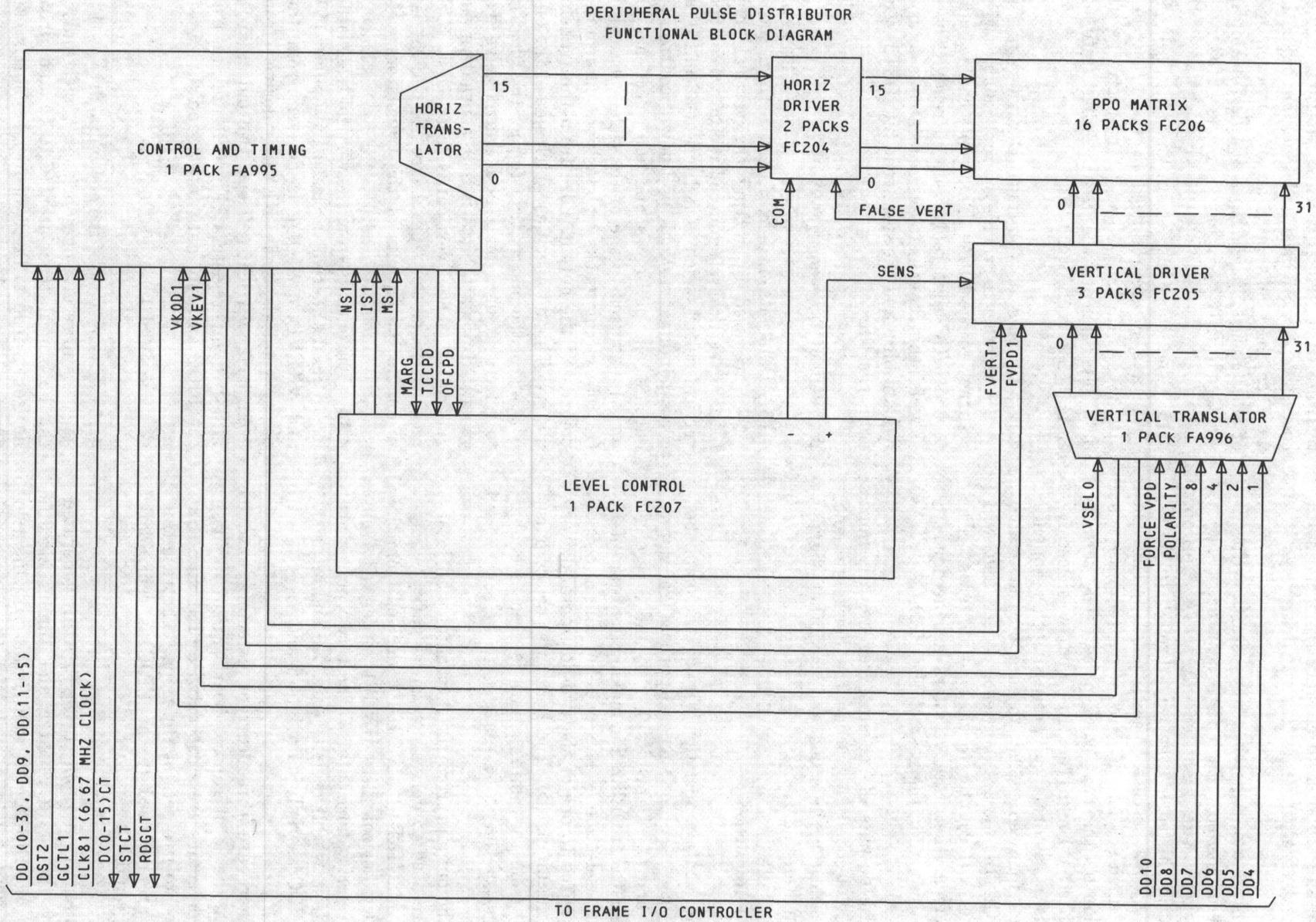
PERIPHERAL PULSE DISTRIBUTOR
FUNCTIONAL BLOCK DIAGRAM



Fig. 3—Peripheral Pulse Distributor Functional Block Diagram

cause the shift counter to advance from one state to the next (Fig. 7).

**4.05** This state register always starts with all zeros loaded. Each PPD sequence (Fig. 7) begins when a one is shifted into the A flip-flop. This one is shifted all the way through to the F flip-flop by six successive clock pulses. The one is complemented, and a zero is shifted into the A flip-flop on the next clock pulse. The zero is then shifted through the flip-flops by successive clock pulses. In normal call processing this sequence is always followed. The absence of the enable signal (GCTL1) occurs between orders and will cause the shift counter to clear to all zeros. The outputs from the state registers are decoded to provide timing for the rest of the PPD.

**4.06** The outputs of the state register flip-flops are decoded to provide the horizontal and vertical selection intervals and the other signals shown in Fig. 7.

**Horizontal Translation**

**4.07** Horizontal translation (Fig. 8) is accomplished by the use of four general-purpose translators A, B, C, and D. Data bits 0, 1, 2, and 3 received from the FIOC are utilized in making the 1-out-of-16 horizontal selection. The one horizontal output selected is fed to one of the two horizontal drivers (FC204) circuit packs. The horizontal select pulse (HSEL0) from the timing circuit is used to enable the output of the translators.

**4.08** The outputs from the horizontal translators are used to derive horizontal parity signals HKOD1 and HKEV1. HKOD1 is derived from the odd parity horizontals. HKEV1 is derived from the even parity horizontals. These two pulses are gated into a two-bit register (Fig. 12) and returned to the FIOC as reply data bits 6 and 7.

**4.09** There are three current detectors located on the level control board FC207. These current detectors are strobed twice (TS1 and TS2) and gated to two sets of flip-flops. The resulting outputs are returned to the FIOC as reply data bits 0 through 5.

**4.10** A number of replies to the FIOC are generated by the state register and timing circuit. There is one flip-flop in this circuit utilizing two inputs GCTL1 (enable signal from the FIOC) and

SCLK0 (clock pulse). This flip-flop toggles on successive clock pulses and gives an indication of whether there has been an odd or even number of clock pulses. The output of this flip-flop is the start code (STCT) returned to the FIOC.

**4.11** The outputs of flip-flops A, B, C, D, E, and F are returned to the FIOC as data bits 15, 14, 13, 12, 11, and 10, respectively. These data bits indicate the final timing state of the PPD. (See reply word, Fig. 5.)

**4.12** Outputs of flip-flops E and F are gated together to provide the reply enable (RDGCT) returned to the FIOC. This reply enable indicates to the FIOC that reply data is ready. The point at which this reply enable is generated is determined by data bit 9 and the start code bit (DST2) received from the FIOC.

**B. Vertical Translator (FA996)**

**4.13** Data bits 4, 5, 6, 7, and 8 from the FIOC are used in making the vertical selection (Fig. 9). Vertical selection consists of two components: vertical select which is a 1-out-of-32 (4.16), and a corresponding vertical pull-down control. Two outputs, one pull-down and one select, are chosen and transmitted to one of the three vertical driver (FC205) circuit packs. Data bit 8 determines the polarity of the output pulse from the transformer matrix. This bit specifies which side of the primary winding of the matrix transformer (FC206, Fig. 10) to select. If data bit 8 is a 1, a positive pulse is generated; if data bit 8 is a 0, a negative pulse is generated. The vertical select pulse (VSEL0) received from the timing circuit (FA995) is used to enable the outputs of the translators.

**4.14** The outputs from the vertical translators are used to derive vertical parity pulses (VKOD1 and VKEV1). VKOD1 is derived from the odd parity verticals, and VKEV1 is derived from the even parity verticals. These two pulses are gated into two bit registers (Fig. 12) and returned to the FIOC as reply data bits 8 and 9.

**C. Horizontal Driver (FC204)**

**4.15** The purpose of the horizontal drivers (Fig. 10) is to receive one horizontal select pulse from the horizontal translator (FA995) and drive one horizontal lead to the transformer matrix (FC206). There are two horizontal driver (FC204) circuit
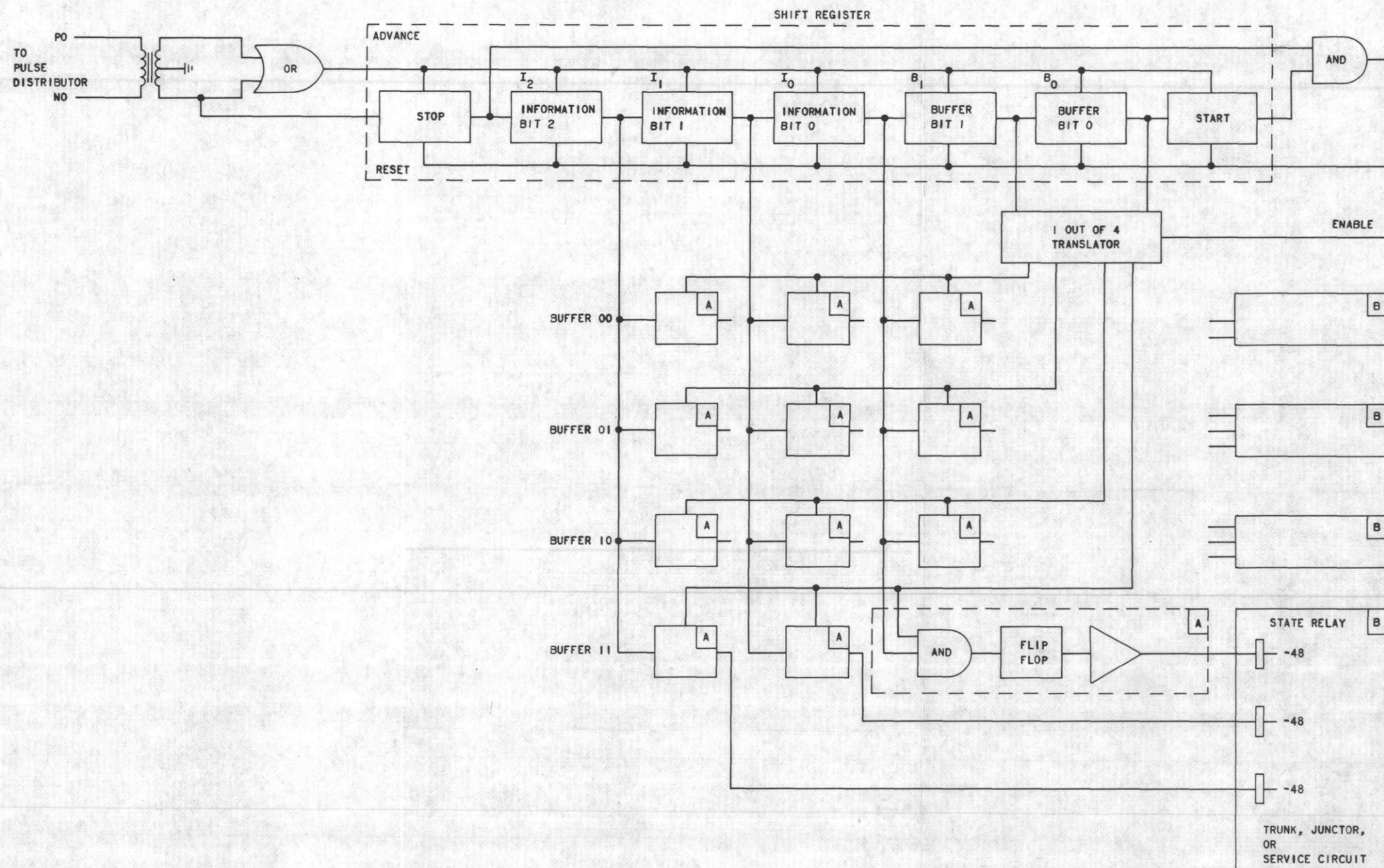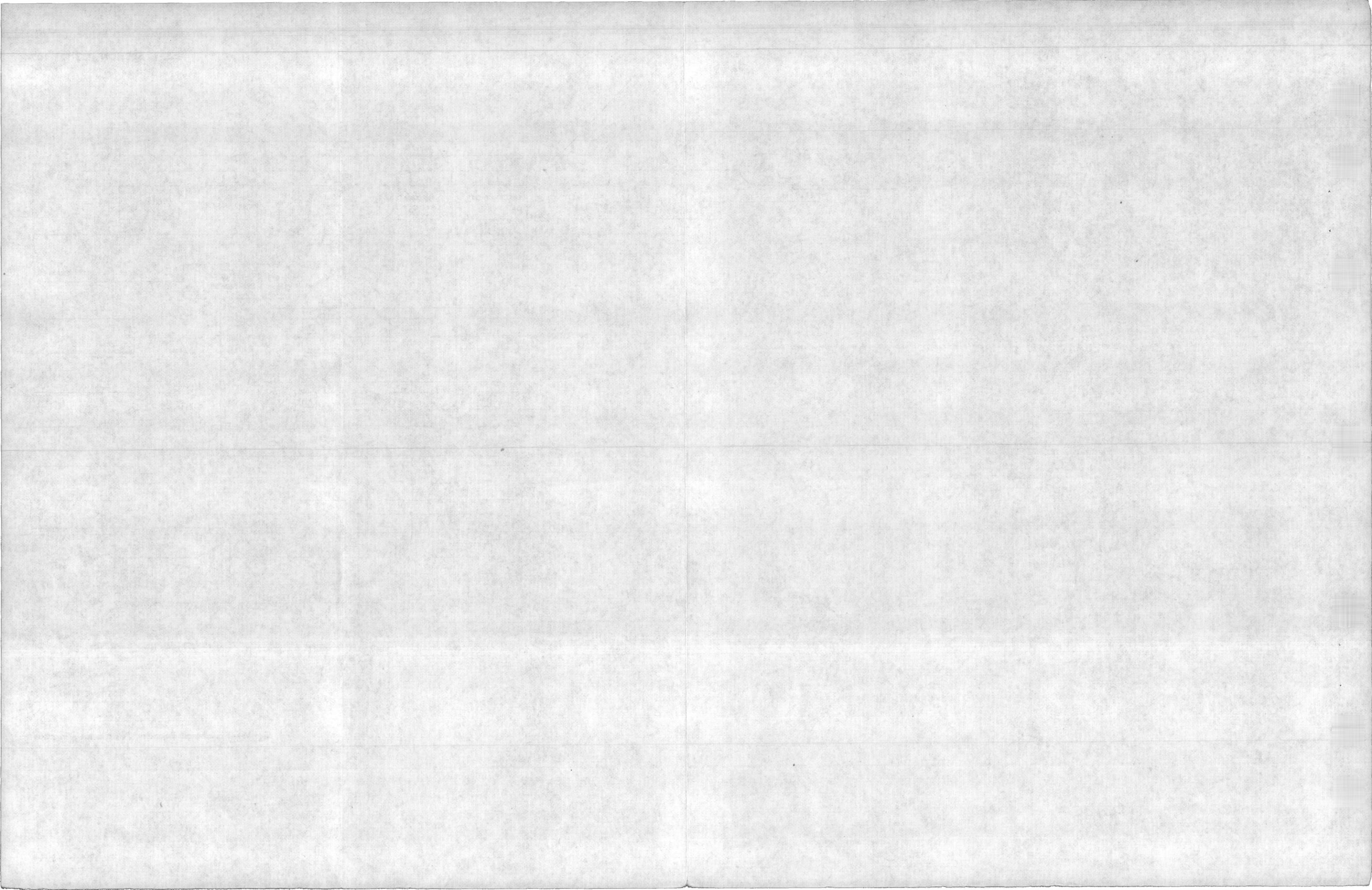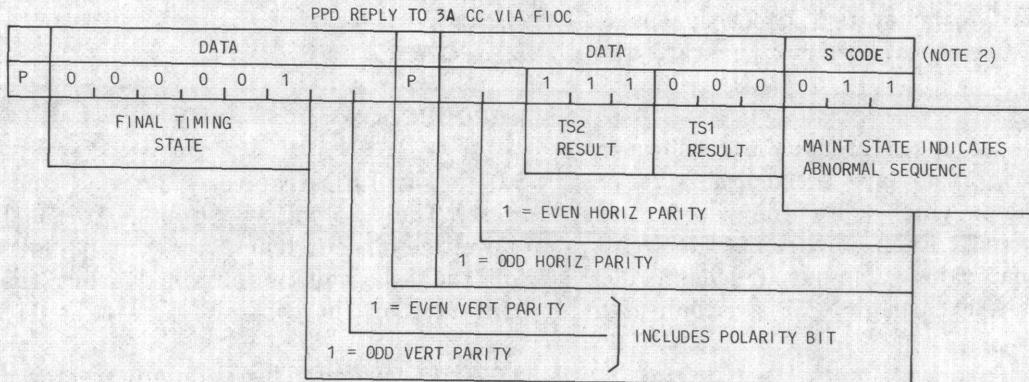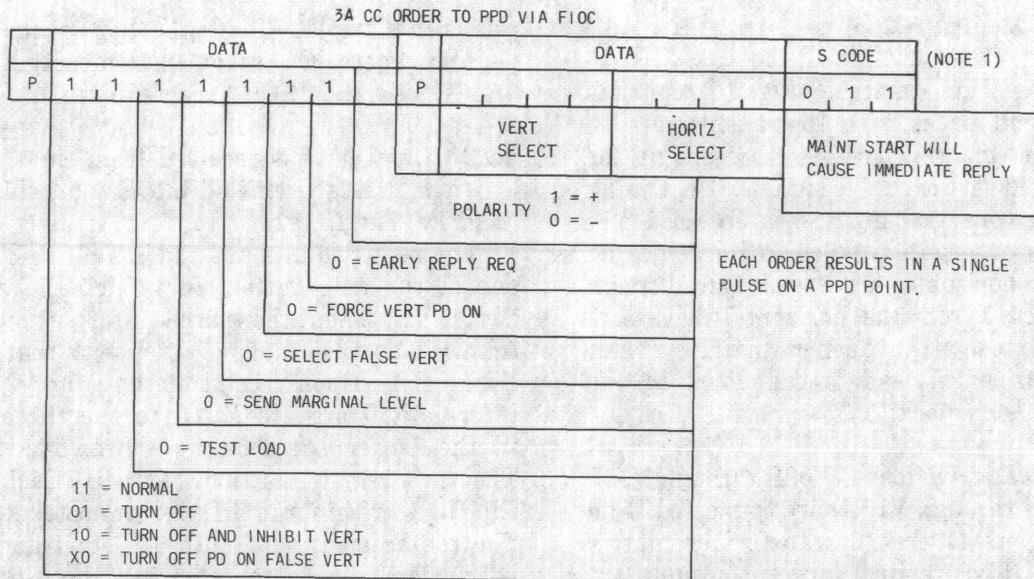
Fig. 4—Peripheral Decoder Functional Diagram

3A CC ORDER TO PPD VIA FIOC

| DATA | | DATA | | S CODE | (NOTE 1) |

| P | 1 1 1 1 1 1 1 | P | | 0 1 1 |

VERT SELECT

HORIZ SELECT

MAINT START WILL CAUSE IMMEDIATE REPLY

POLARITY  1 = +  0 = -

0 = EARLY REPLY REQ

EACH ORDER RESULTS IN A SINGLE PULSE ON A PPD POINT.

0 = FORCE VERT PD ON

0 = SELECT FALSE VERT

0 = SEND MARGINAL LEVEL

0 = TEST LOAD

11 = NORMAL
01 = TURN OFF
10 = TURN OFF AND INHIBIT VERT
X0 = TURN OFF PD ON FALSE VERT

PPD REPLY TO 3A CC VIA FIOC

| DATA | | DATA | | S CODE | (NOTE 2) |

| P | 0 0 0 0 0 1 | P | 1 1 1 0 0 0 | 0 1 1 |

FINAL TIMING STATE

TS2 RESULT

TS1 RESULT

MAINT STATE INDICATES ABNORMAL SEQUENCE

1 = EVEN HORIZ PARITY

1 = ODD HORIZ PARITY

1 = EVEN VERT PARITY

1 = ODD VERT PARITY

} INCLUDES POLARITY BIT

| DATA | | | | | | | | | DATA | | | | | | | | | S CODE | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HIGH P | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | LOW P | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 2 | 1 | 0 |

BIT ASSIGNMENT

NOTES:
1. THE START CODE IS USED IN THE FIOC TO GENERATE THE DST2 OUTPUT TO THE PPD.
2. THE START CODE IS GENERATED IN THE FIOC USING THE STCT INPUT FROM THE PPD.

**Fig. 5—Peripheral Pulse Distributor Data Format**

packs in the PPD. The horizontal select pulse [HS(00-15)0] is received from the horizontal translator and gated through the circuit pack. The selected horizontal is connected by the driver to the negative (COM) output of the level control board (FC207).

**D. Vertical Driver (FC205)**

4.16 The purpose of the vertical drivers (Fig. 10) is to receive one vertical select pulse and one vertical pull-down pulse from the vertical translator (FA996) and drive one vertical of the transformer matrix (FC206). There are three vertical drivers (FC205) in the PPD. The vertical select pulse [VS(00-31)1] is used to connect the positive (SENS) output from the level control board (FC207) to the selected vertical. The vertical pull-down pulse [VP(00-31)0] turns off the transistor which normally clamps this vertical to ground through a resistor.

### E. Transformer Matrix (FC206)

**4.17** The transformer matrix (Fig. 10) consists of 16 circuit packs with 16 transformers on each pack. This matrix acts as a crosspoint for the horizontal and vertical drive signals. Depending on these signals, one transformer is accessed and sends a positive or negative pulse to its dedicated PD. The sixteen horizontal drive leads (H0 through H15) are connected from the horizontal drivers to each of the sixteen transformer matrix circuit packs. One horizontal lead is connected to one transformer on each pack.

**4.18** The vertical drive leads (V00P through V15P and V00N through V15N) are connected from the vertical drivers to the 16 transformer matrix circuit packs. Two vertical driver outputs are connected to each circuit pack where they connect to each transformer on that pack. One of the two drivers is used to generate the positive pulse while the other driver is used to generate the negative pulse.

**4.19** Drive pulses are passed through the transformer. The output pulses are either positive or negative depending on which side of the transformer winding was selected. Each of the matrix circuit packs has 16 output pairs. The output leads (P000 through P255 and N000 through N255) are connected to the PDs.

### PERIPHERAL DECODER

**4.20** The peripheral decoder consists of the following:

- Input transformer
- Shift register
- A 1-out-of-4 translator
- Four buffers.

The PD determines the state of trunk, junctor, and service circuit state relays as directed by the 3A CC via the PDD through the FIOC.

**4.21** Each PD is designed to operate external relays upon command of bipolar pulses from the transformer matrix. These relays are organized in four groups of three called triplets. Seven input pulses are needed to set the state of the relays in a triplet. Since the PPD sends one pulse per data message - seven data messages from the 3A CC (via the FIOC) are required.

**4.22** Input data is received from the transformer matrix and shifted into a 7-bit shift register (Fig. 4). The first bit (start bit) is always a logical 1. The next two bits are address bits which specify one of the four buffers for which the message is destined. Then the three information bits are followed by the final bit (stop bit) that is always a logical 1. Upon receipt of the stop bit, the three information bits are gated to the three flip-flops in the buffer specified by the two address bits. The shift register is then cleared. Each of the 12 flip-flops within the PD is connected to a relay. The requirement that both the start and stop bits be present allows for clearing the shift register after an incomplete message by sending a string of seven zeros.

## 5. POWER

### INTRODUCTION

**5.01** The PPD requires +24 volts and +3 volts. The +24 volts is supplied to the PPD from the miscellaneous frame and the +3 volts required for the 1A logic is obtained from the +3 volt converter on the control frame (Fig. 11).

**5.02** Power may be manually removed from or restored to the PPD by properly operating several nonlocking keys. These keys are located on the control panel of the control frame.

**5.03** The power required to operate the PD is obtained from the -48 volt power plant. Located on the PD is a -7 volt dc-to-dc converter which is used for the logic. The output of the PD is a ground intended to operate -48 volt state relays in trunk, junctor, and service circuits.

### POWER AND ALARM CIRCUITS

#### A. +3 Volt and +24 Volt Power Distribution

**5.04** All the circuits in a peripheral control circuit has its own power system: two J87389F, +3 volt converters; one FC21, +3 volt reference and filter circuit pack; and one FB152, +12 volt reference circuit pack. The power system also distributes +24 volts, +3 volts, and ground (GRD) to the PPD circuit packs via the multilayer printed
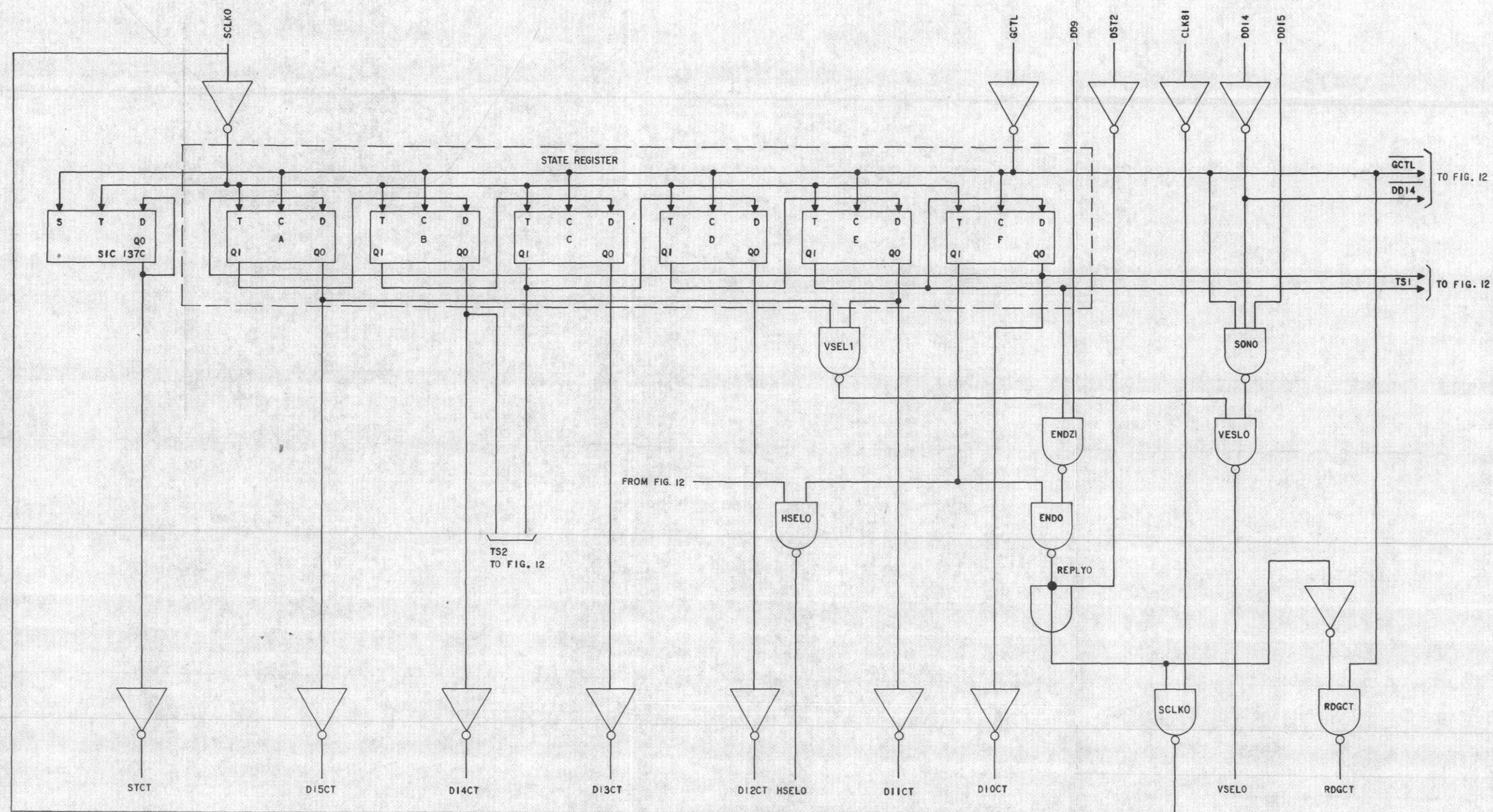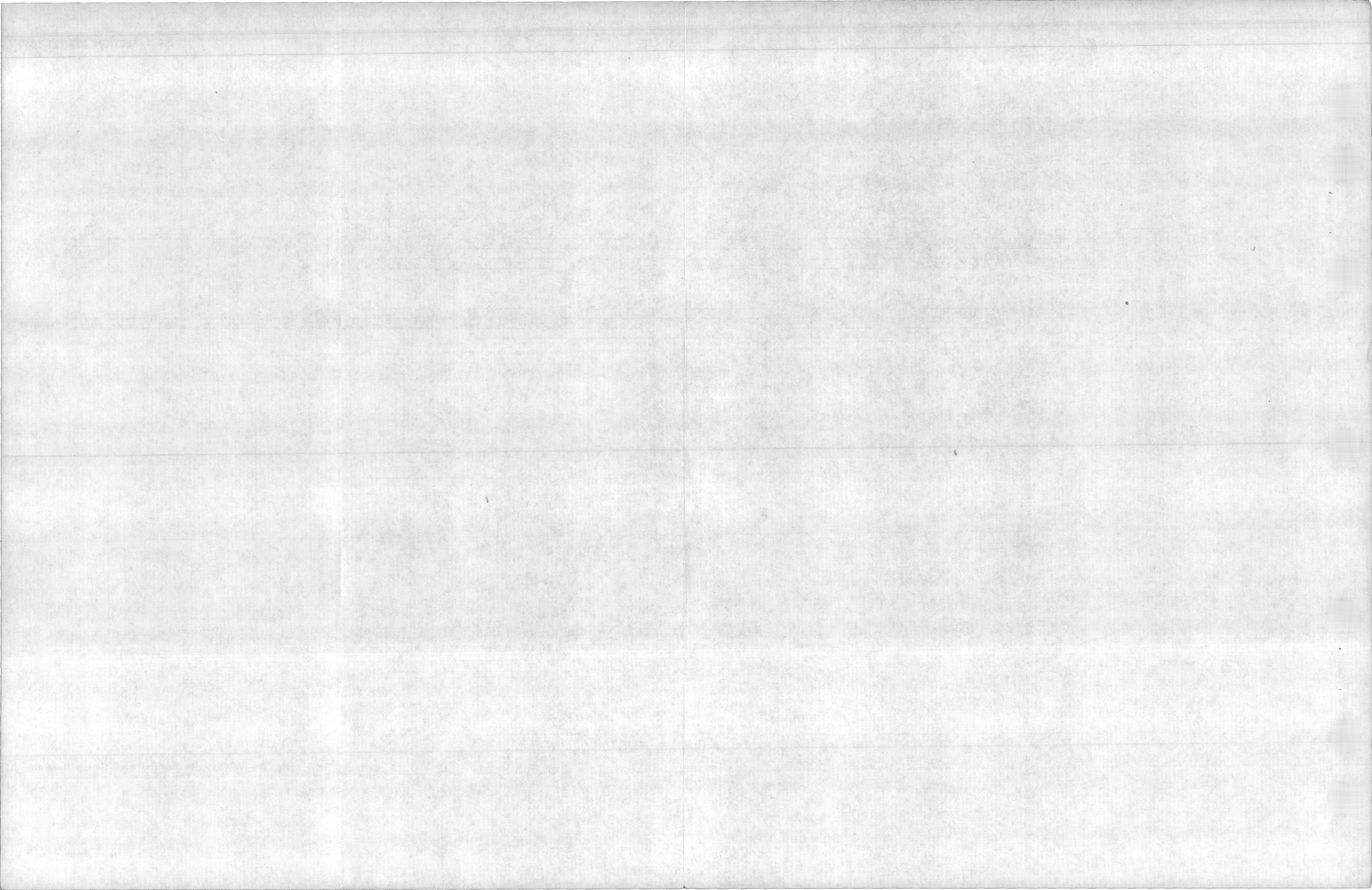
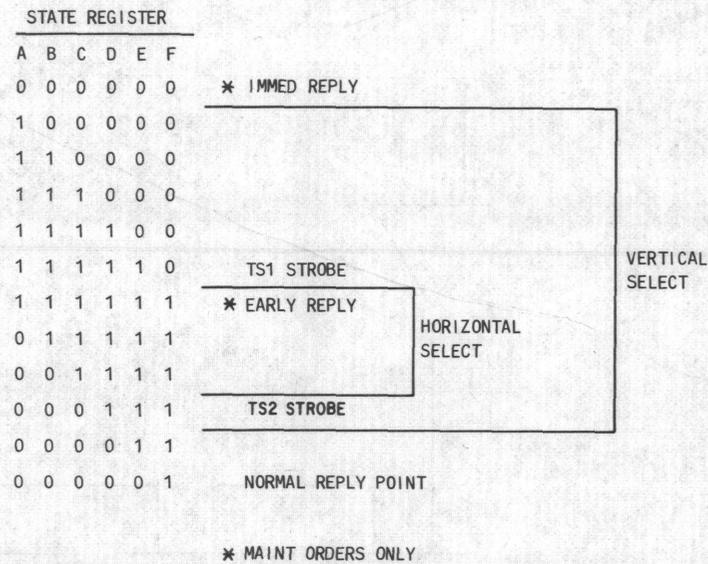Fig. 6—FA995 State Register and Timing Diagram

```
        STATE REGISTER

      A  B  C  D  E  F

      0  0  0  0  0  0    * IMMED REPLY

      1  0  0  0  0  0

      1  1  0  0  0  0

      1  1  1  0  0  0

      1  1  1  1  0  0

      1  1  1  1  1  0    TS1 STROBE                    VERTICAL
                                                        SELECT
      1  1  1  1  1  1    * EARLY REPLY
                                          HORIZONTAL
      0  1  1  1  1  1                     SELECT

      0  0  1  1  1  1

      0  0  0  1  1  1    TS2 STROBE

      0  0  0  0  1  1

      0  0  0  0  0  1    NORMAL REPLY POINT


                          * MAINT ORDERS ONLY
```

**Fig. 7—Peripheral Pulse Distributor Sequence Chart**

wiring boards (MLPWB). The control frame circuit also provides +24 volts and +48 volts to the two J87389F power converters.

**5.05** The control frame circuit provides power control, fusing, and alarms for the peripheral controllers. The power control and alarm circuit consists of four circuit packs: two FB414, 3-volt power control 0 and 1; and two FB415, alarm 0 and 1. Associated with the control frame power is a control panel and two fuse panels. The control panel has three nonlocking (NLK) keys (ON, REQ, and OFF) and two lamps (OOS and PWR OFF) which are duplicated for peripheral controller 0 and 1. The fuse panel contains power fuses for protecting each controller in the periphery. The control frame circuit (SD-3H902-01) contains the following power related functional schematics: FS41- +24 volt power control, fusing, and alarms; FS42- +48 volt power control, fusing, and alarms; FS43- power sequencing; FS44- alarm and test; and FS45- scan points. The various circuits associated with SYC 0 and SYC 1 points are duplicated.

**B.  +24 Volt Power Control, Fusing, and Alarms**

**5.06** The control frame circuit separately distributes +24 volts to each MLPWB in the peripheral control circuit when each associated PWR relay is operated. Each power lead is fused with a 70-type fuse. If the fuse opens, an auxiliary circuit is completed which provides +24 volts to operate one of the 24FA relays. Separate fuses exist in the fuse panels for peripheral control circuit 0 and 1. In addition to distributing +24 volts to all four J87389F power converters, the control frame circuit also starts the converters by switching +24 volts to their 24VST lead. The switching occurs under the following conditions: the 24ST relay operated, the 24FA relay released, and the 48FA relay released.

**C.  -48 Volt Power Control, Fusing, and Alarms**

**5.07** The control frame circuit separately distributes -48 volts to a large number of individually fused circuits in the periphery. If a fuse opens, the auxiliary circuit operates one of the 48FA relays or one of the SFA relays. The 48FA relays are only operated by the fuses on the lines distributing -48 volts to the J87389F power converters. Any of the remaining -48 volt fuses, when blown, will operate the SFA relays.

**D.  -48 Volt Power For Peripheral Decoder**

**5.08** Power for the PD circuit is provided by the -48 volt power frame via the control frame circuit. Included in this circuitry is a -48 to -7 volt dc-to-dc converter required to drive the logic. An output of -48 volts is required to operate the state relays.
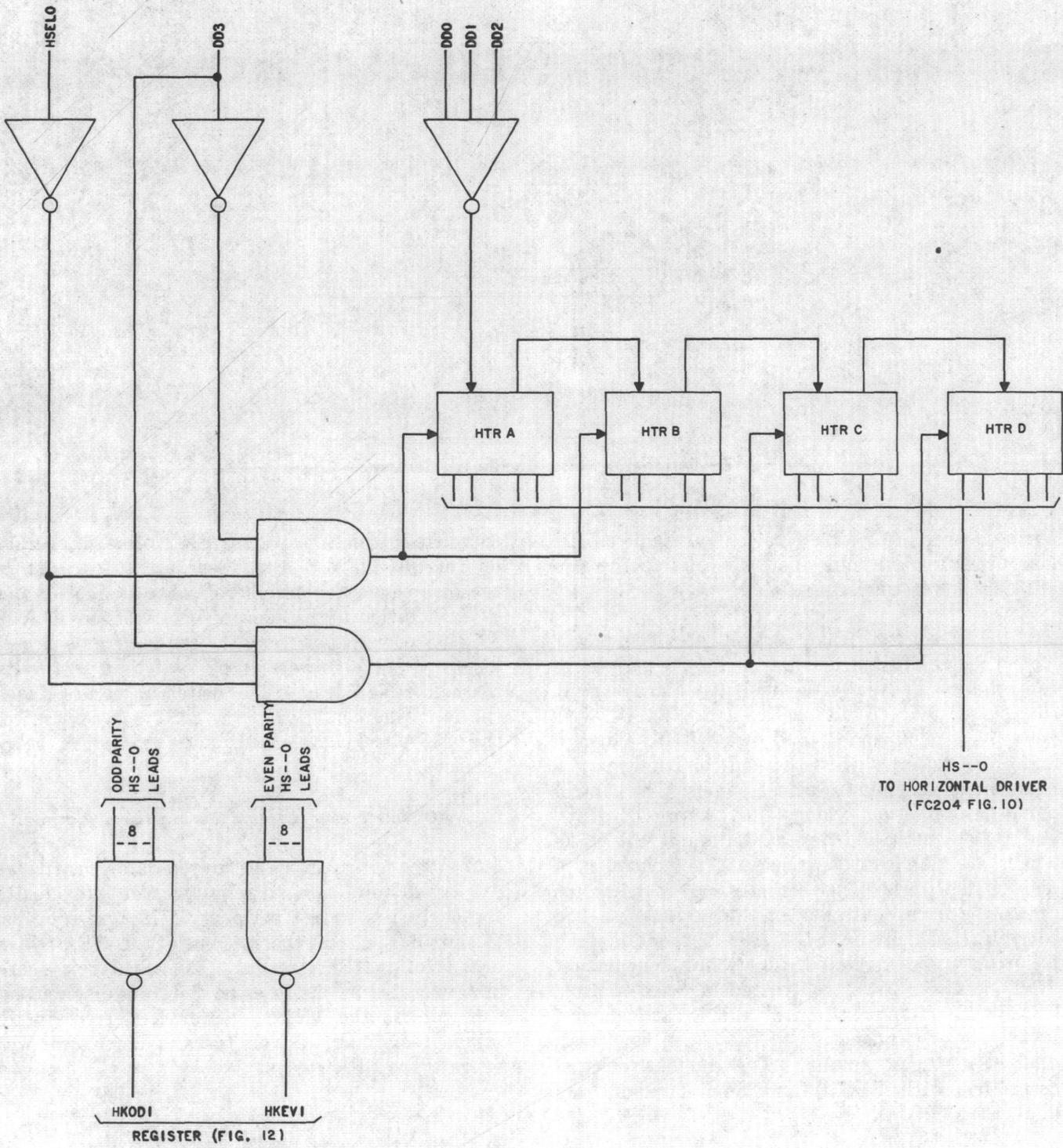
Fig. 8—FA995 Horizontal Translation Diagram

**Fig. 9—FA996 Vertical Translation Diagram**

## E. Power Sequencing

**5.09** Each set of J87389F power converters is started by depressing the associated ON (NLK) key on the control panel which provides a ground path to operate the associated 24ST relay. The associated set of power converters must supply +3 volts to a transistor circuit before it provides a ground path to operate the appropriate PWR relay. This relay keeps the 24ST relay operated after the ON (NLK) is released. The PWR OFF lamp is extinguished while the OOS lamp remains lighted. When the REQ (NLK) key is depressed, the request ferrod scan point notifies software to run diagnostics on the peripheral controller. Once diagnostics are complete, the controllers are restored to service. The OOS lamp is extinguished when the peripheral decoder releases the OOS relay. The circuitry for removing power operates much in the same way. When the REQ (NLK) key associated with the off-line peripheral controllers is depressed, software responds by removing the controllers from service and lights the OOS lamp. Once the OFF (NLK) key is depressed, a transistor circuit releases the PWR and 24ST relays, the PWR OFF lamp is lighted and the J87389F power converters are disabled. Should emergency removal of power be required, depressing the REQ (NLK) and OFF (NLK) keys simultaneously will force the J87389F power converters to be disabled and +24 volts to be removed from the peripheral controllers.

## F. Alarm and Test

**5.10** The lamp circuit has a lamp test capability. Depressing the LP & PWR TEST (NLK) key closes a circuit path to light both sets of OOS, PWR OFF, and FA lamps. Individually, the OOS lamp is lighted with the OOS relay operated; the PWR OFF lamp is lighted with the PWR relay released; and the FA lamp is lighted with the 24FA, 48FA, or SFA relay operated. The alarm circuitry has the capability for a number of different alarms. The J87389F power converters have an overvoltage and overcurrent fuse alarm (FA) signal. This FA signal is sent to the alarm circuit where a transistor switch operates the CFA relay. The alarm circuit keeps the CFA relay operated until released by depressing the LP & PWR TEST (NLK) located on the control panel in the control frame. This is necessary since the loss of one converter will shut off all power to one peripheral control circuit. The J87389F power converters and the FB152 reference board also have an

out-of-voltage limits power alarm (PA) signal. This PA signal is likewise sent to the alarm circuit where another transistor switch operates the CPA relay. The alarm circuit has the facility for power alarm test (PAT). The system, via the peripheral decoder, operates the PAT and OOS relays. A PAT signal is sent to the set of J87389F power converters and the FB152 board. They should respond by operating the CPA relay and thus unsaturating the PA scan point. In the alarm circuit, the NPA relay operates only if a J87389F or a FB152 fails to give a PA. The NPA relay then keeps the PA scan point satuated. As the PAT relay is released, a ground is briefly applied to the NPA leads of the J87389F converters and FB152 reference board to extinguish the light emitting diodes (LEDs). When the OOS relay is released, a PAT signal can also be generated by depressing the LP & PWR TEST (NLK) key. When the key is released, a ground is sent out to extinguish the LEDs. If there is no PA signal, the associated LED fails to light. Scan points are not affected by a manual PAT.

## G. Scan Points

**5.11** The scan-point circuit contains three ferrods which are concerned with power control and alarms. The state of certain relays and keys determines whether current flows in the ferrod control windings. The request ferrod is saturated with the 24ST relay operated and the REQ (NLK) key released. The power alarm ferrod is saturated with the 24ST relay operated and any of the four following conditions: the LP & PWR TEST (NLK) key depressed, the REQ (NLK) key depressed, the NPA relay operated, or the CPA relay released. These two ferrods are encoded into four states (OFF, REQUEST, ON, and POWER ALARM). When both ferrods are unsaturated, the state is OFF. With the request ferrod unsaturated and the power alarm ferrod saturated, the state is REQUEST. When both ferrods are saturated, the state is ON. Finally, with the request ferrod saturated and the power alarm ferrod unsaturated, the state is POWER ALARM. The major control alarm ferrod is saturated with all three (CFA, 24FA, and 48FA) relays released. All three ferrods are duplicated for peripheral controllers 0 and 1.
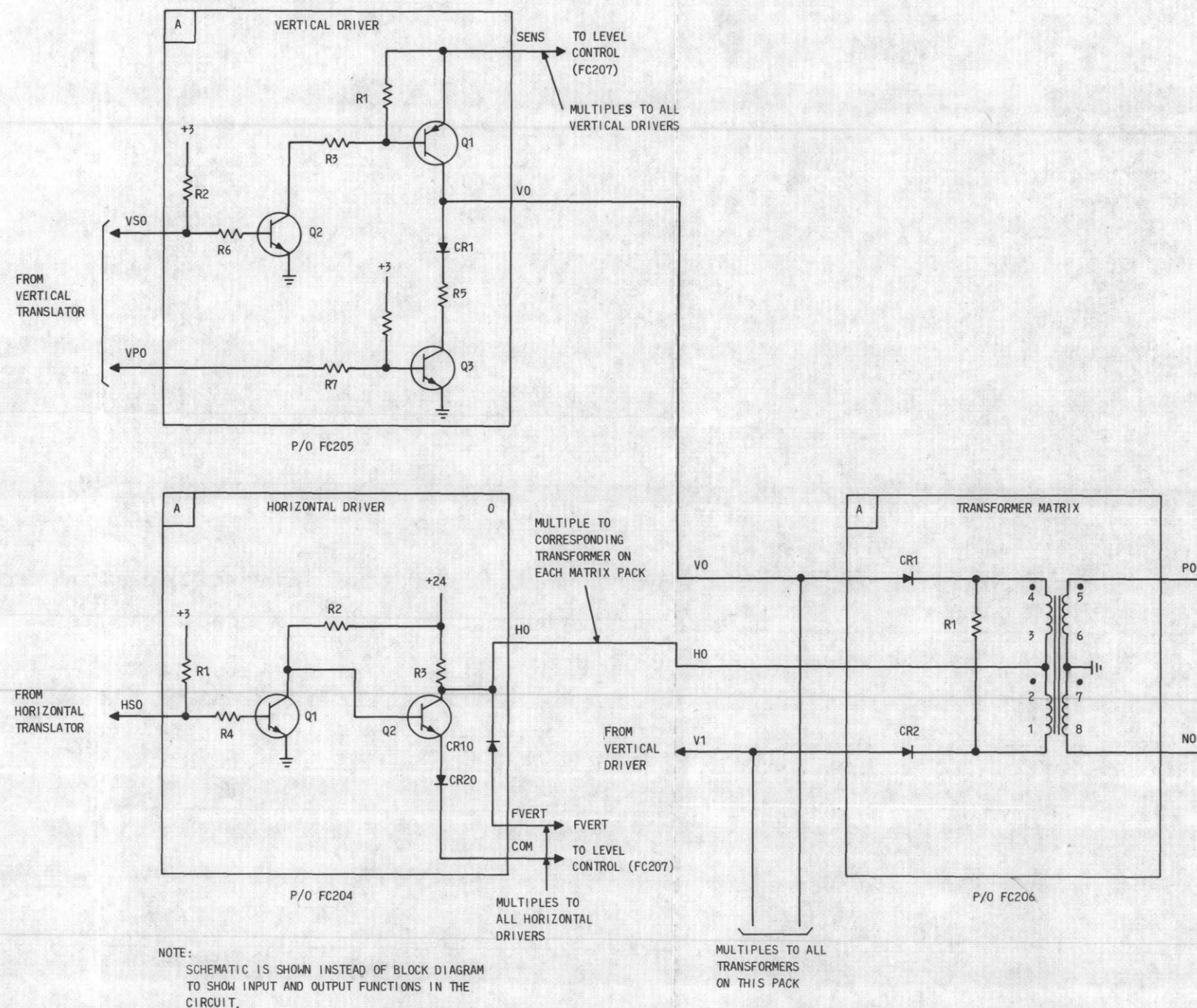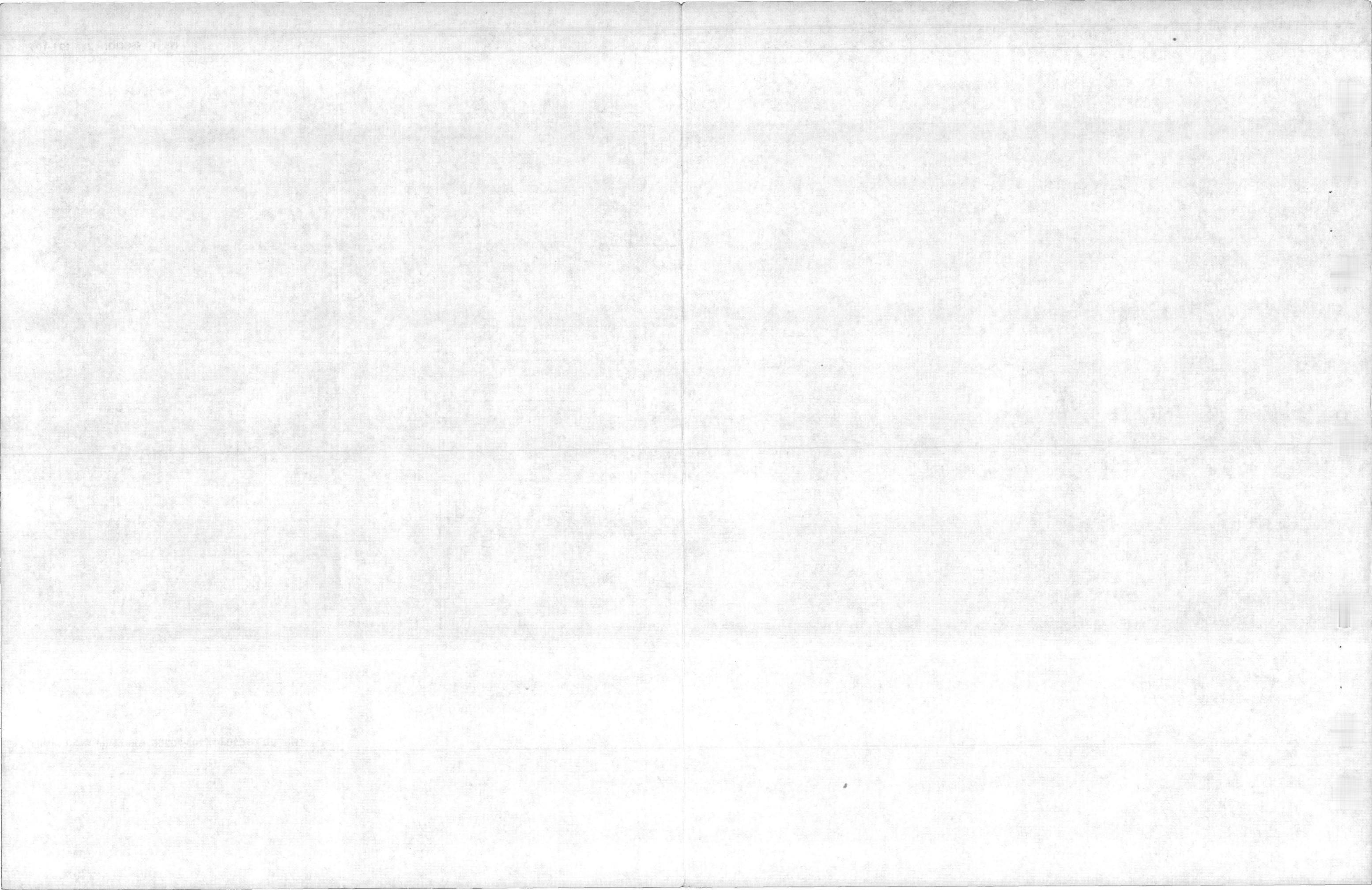
**VERTICAL DRIVER** (P/O FC205) — SENS TO LEVEL CONTROL (FC207), MULTIPLES TO ALL VERTICAL DRIVERS, R1, R2, R3, R5, R6, R7, Q1, Q2, Q3, CR1, VO, VSO, VPO, FROM VERTICAL TRANSLATOR, +3

**HORIZONTAL DRIVER** (P/O FC204) — MULTIPLE TO CORRESPONDING TRANSFORMER ON EACH MATRIX PACK, FROM HORIZONTAL TRANSLATOR, HSO, R1, R2, R3, R4, Q1, Q2, CR10, CR20, HO, FROM VERTICAL DRIVER, FVERT, COM, TO LEVEL CONTROL (FC207), MULTIPLES TO ALL HORIZONTAL DRIVERS, +3, +24

**TRANSFORMER MATRIX** (P/O FC206) — CR1, CR2, R1, VO, HO, V1, PO, NO, MULTIPLES TO ALL TRANSFORMERS ON THIS PACK

NOTE:
SCHEMATIC IS SHOWN INSTEAD OF BLOCK DIAGRAM TO SHOW INPUT AND OUTPUT FUNCTIONS IN THE CIRCUIT.

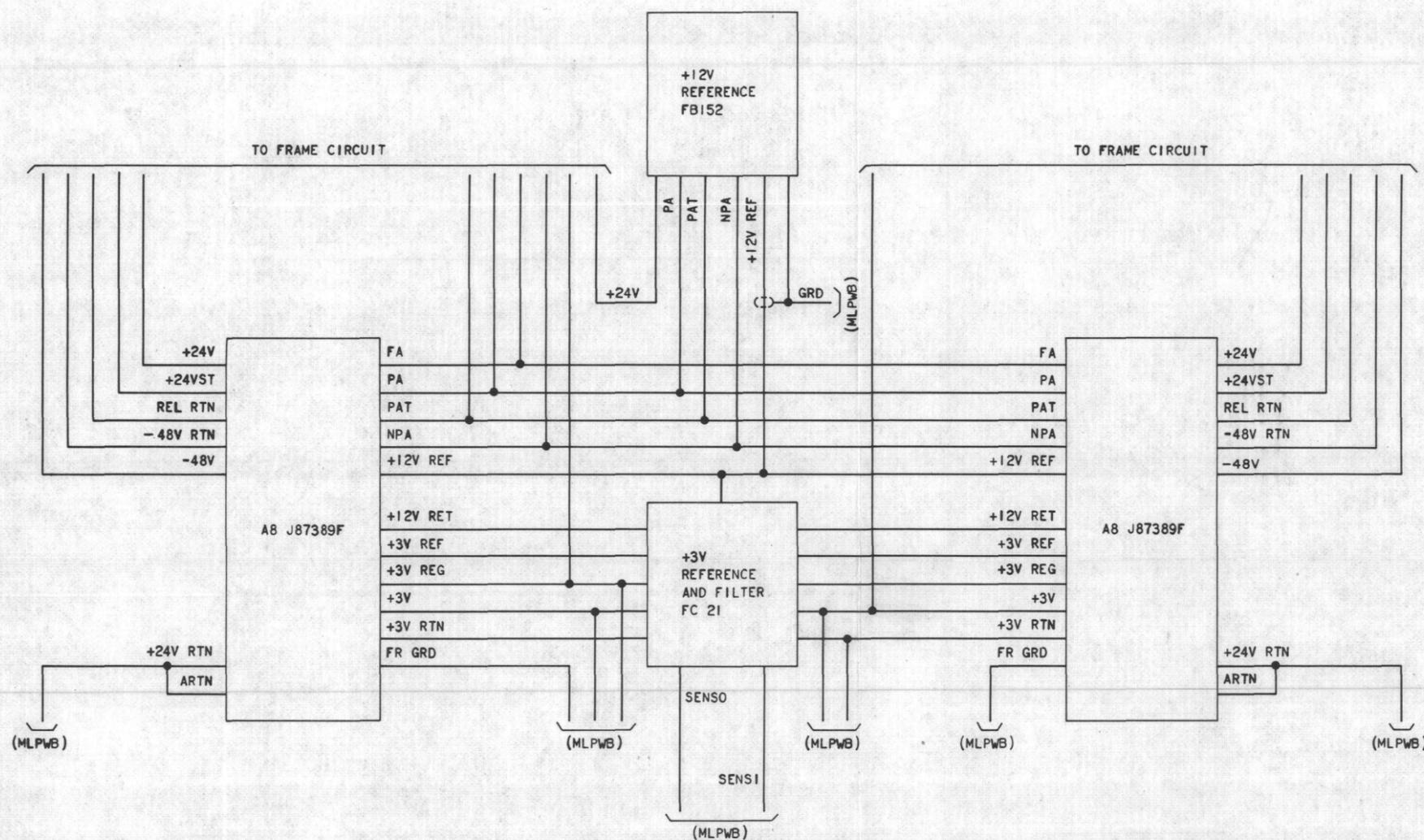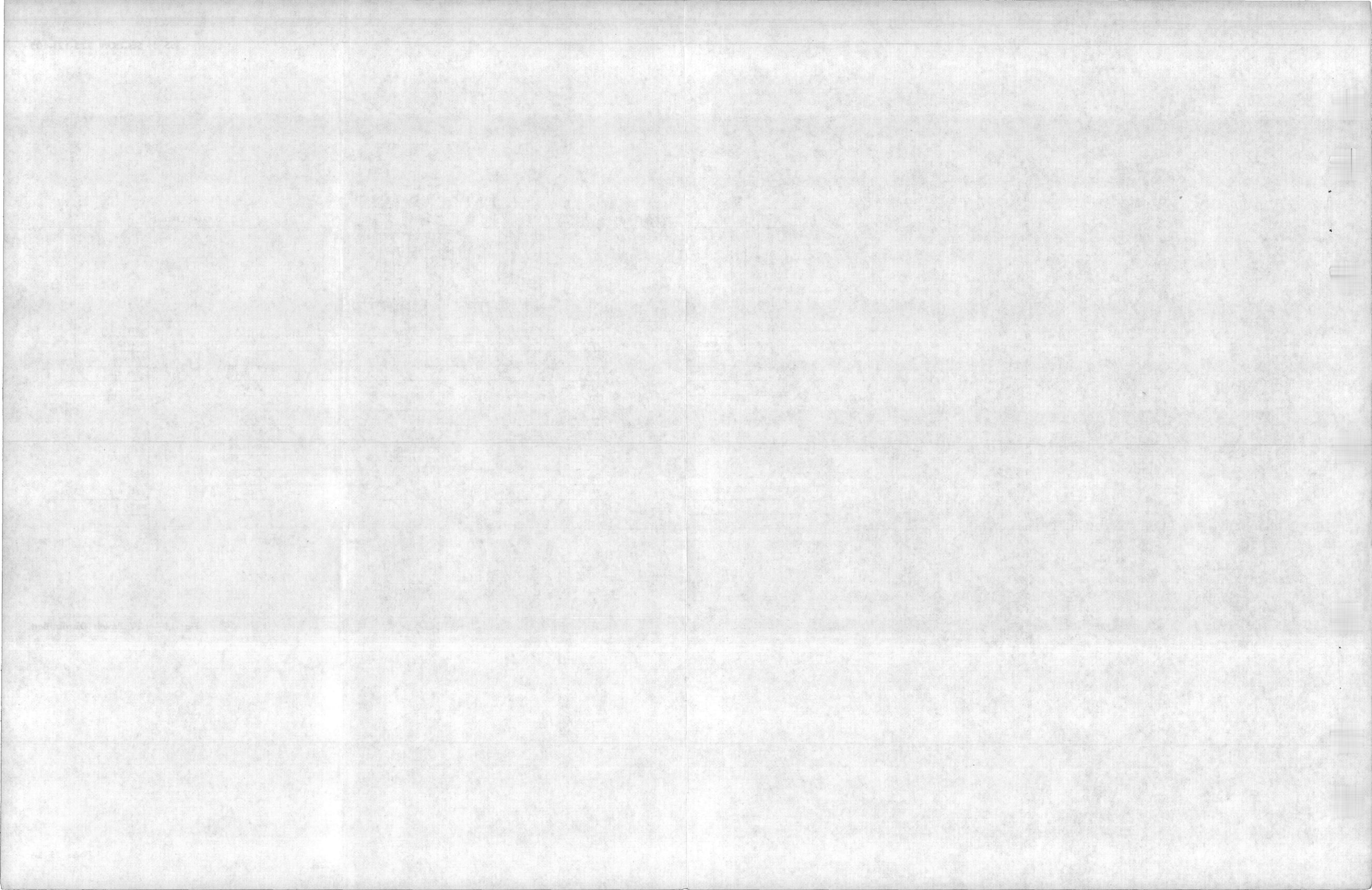**Fig. 10—FC204-FC205-FC206 Functional Relationship**

Fig. 11—+3V Power Distribution

## 6. MAINTENANCE

### INTRODUCTION

#### A. Peripheral Pulse Distributor

**6.01** Trouble detection is accomplished in the PPD by current sensing tests in the level control circuit (FC207). After the transformer matrix vertical is selected, a test is made to verify that no current flows in the matrix. After the transformer matrix horizontal is selected, a test is made to verify that current does flow.

**6.02** An indication of the sources or failure of the trouble detection tests is returned via the FIOC to the 3A CC. The 3A CC initiates a fault-recovery sequence and transmits the original order a second time under control of the recovery procedures. If the second trial fails, system control (8.01) is switched to the alternate 3A CC which terminates the original order to the alternate FIOC and alternate PPD.

#### B. Peripheral Decoder

**6.03** A trouble condition within the PD is indicated by the failure of the associated state relays to operate or release in accordance with data transmitted from the PPD. Indications of PD or state relay failures are not transmitted to the 3A CC via the PPD and FIOC. However, the trouble condition is detected in subsequent checks and diagnostic tests in the call processing programs. If failures persist, the affected trunk, junctor, or service circuit is removed from service. Manual diagnostics (programmed diagnostics which are manually initiated via the maintenance TTY and provide the capability for testing selected parts of the system) can be performed to determine whether the failure occurred in the PD or in a trunk, junctor, or service circuit.

#### C. Trouble Indicators

**6.04** Failures are indicated by TTY messages which identify problem areas. Audible alarms are sounded and visual indications are shown on the system status panel (SSP).

### THEORY OF OPERATION

**6.05** The PPD can perform several maintenance and test checks. Some of these are initiated during normal call processing while others are initiated by special maintenance orders. The PPD control performs the following actions in sequence:

(a) Clear

(b) Vertical select on

(c) Test strobe 1

(d) Horizontal select on

(e) Test strobe 2

(f) Horizontal select off

(g) Vertical select off

(h) Reply.

**6.06** The vertical selection applies positive voltage (SENS) from the level control board (FC207) to the vertical side of the transformer matrix.

**6.07** Test strobe 1 (TS1) is a check to determine that current is not flowing in the matrix just prior to horizontal select being turned on. This is primarily to check for shorted diodes in the matrix. Voltage is applied to the vertical to be driven. All nonselected verticals are grounded by means of the pull-down transistors. These vertical pull-down transistors are normally on except in the one selected vertical. If any of the diodes in the nonselected verticals are shorted, current from the level control board (FC207) will flow through the shorted diode to a nonselected vertical and then to ground through its pull-down transistor. This current would be sufficient to operate a current detector in the level control board (FC207). There are three thresholds of current detection in the FC207 board (low-to-high these are: MS1 marginal, IS1 intermediate, and NS1 normal). At TS1 strobe time in the normal order sequence, if any current is flowing, it is an indication of a shorted matrix diode, falsely activated horizontal driver or ground fault somewhere in the transformer matrix. Test strobe 1 (Fig. 6) is generated by the outputs of the E and F flip-flops of the state register (FA995). The strobe and the outputs of the current detectors are fed into three flip-flops (Fig. 12).

**6.08** Following TS1, horizontal selection is made by activating a horizontal driver which begins the output pulse by connecting the selected horizontal

to a ground at the COM terminal of the level control board (FC207).

**6.09** Test strobe 2 (TS2) occurs at the end of the horizontal select interval. This test strobe (Fig. 6) is generated by the outputs of the C and D flip-flops in the state register (FA995). Test strobe 2 is a check to verify that normal current level is flowing in the matrix. TS2 strobes the output of the three detectors on the level control board (all active on normal order) into three flip-flops (not the same flip-flops fed by test strobe 1).

**6.10** Horizontal select is turned off by the setting of the flip-flop which records the marginal level detector (MS1) during test strobe 2. The vertical select is then turned off, and a reply is sent to the 3A CC via the FIOC.

**6.11** The following list shows the function of the reply data bits (Fig. 5) returned to the 3A CC via the FIOC:

0-2: state of current detector on test strobe 1

3-5: state of current detectors on test strobe 2

6-7: one-out-of-two code indicating even-or-odd parity horizontal selected

8-9: one-of-out-two code indicating even-or-odd parity vertical selected

10-15: final state of the six state register flip-slops.

**MAINTENANCE ORDERS**

**6.12** The FA995 board receives data bits 9, 11 through 15 and DST2 (start code) from the FIOC. The FA996 board receives data bit 10. These data bits are utilized in performing the special maintenance functions.

**6.13** A maintenance start code (DST2) requests an immediate reply without clocking the state register (Fig. 6). This reply verifies that all registers and state flip-flops have been cleared to an all zero state. The PPD sequence always starts in this state.

**6.14** The early reply in the PPD sequence (Fig. 7) is requested by data bit 9 from the FIOC. Early reply provides a reply point while horizontal select is being performed. Since the contents of the state register are part of this reply, it will confirm that the state register does get to the all ones state.

**6.15** A check of the pull-down transistors can be made using data bit 10 from the FIOC. The pull-down transistor on the selected vertical is forced to stay on providing a current path through the vertical driver board (FC205) to ground prior to horizontal selection. This current will be seen when the current detectors are strobed by test strobe 1 thus verifying that the vertical pull-down transistor is grounding the vertical.

**6.16** Data bit 11 is used in the selection of the false vertical. A false vertical path does not go through any transformer in the matrix. It allows current to flow from the level control (FC207) board through the horizontal driver without producing any pulse at the matrix output. The primary function is to exercise the standby PPD by sending it through as much of a normal cycle as possible without generating any actual outputs which would interfere with normal call processing. Data bits 14 and 15 are used in this case to inhibit the normal vertical select and turn off the pull-down transistor which normally grounds the false vertical.

**6.17** The marginal level condition is generated by data bit 12. It drops the current from the level control board through the transformer matrix to a level which is insufficient to operate the PD. This allows the vertical translator and drivers of the standby PPD to be exercised without interfering with normal call processing. The marginal level pulse is also used in the diagnosis of the PD. A message containing a marginal pulse is transmitted to check that the input sensitivity of the PD has not increased to the point that it might pick up stray noise.

**6.18** The intermediate level condition is generated by data bit 13. A combination of data bits 14 and 15 inhibiting the normal vertical selection is also used in this condition. A resistance test load is applied directly to the voltage output of the level control board to provide a current level between the marginal and normal sense thresholds. This current level is used to verify the thresholds
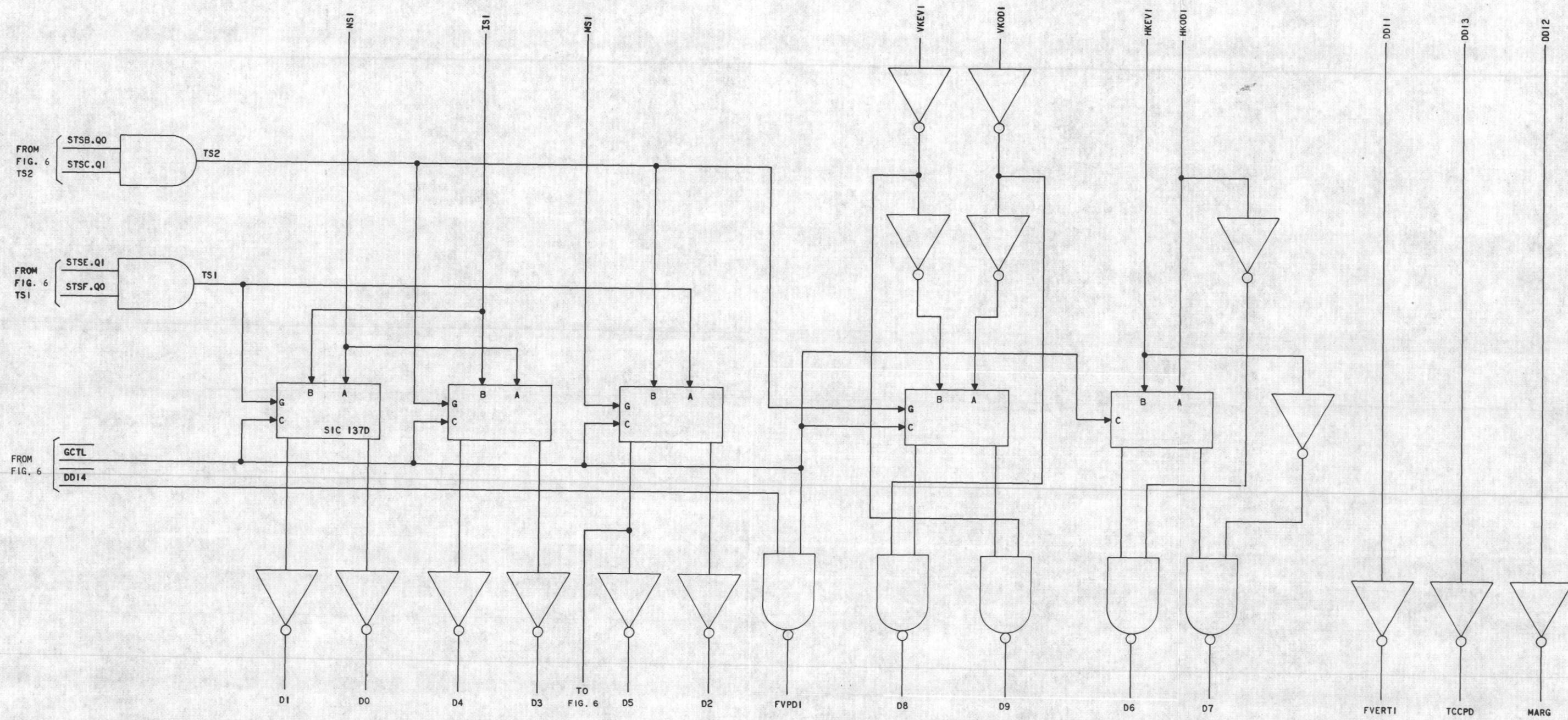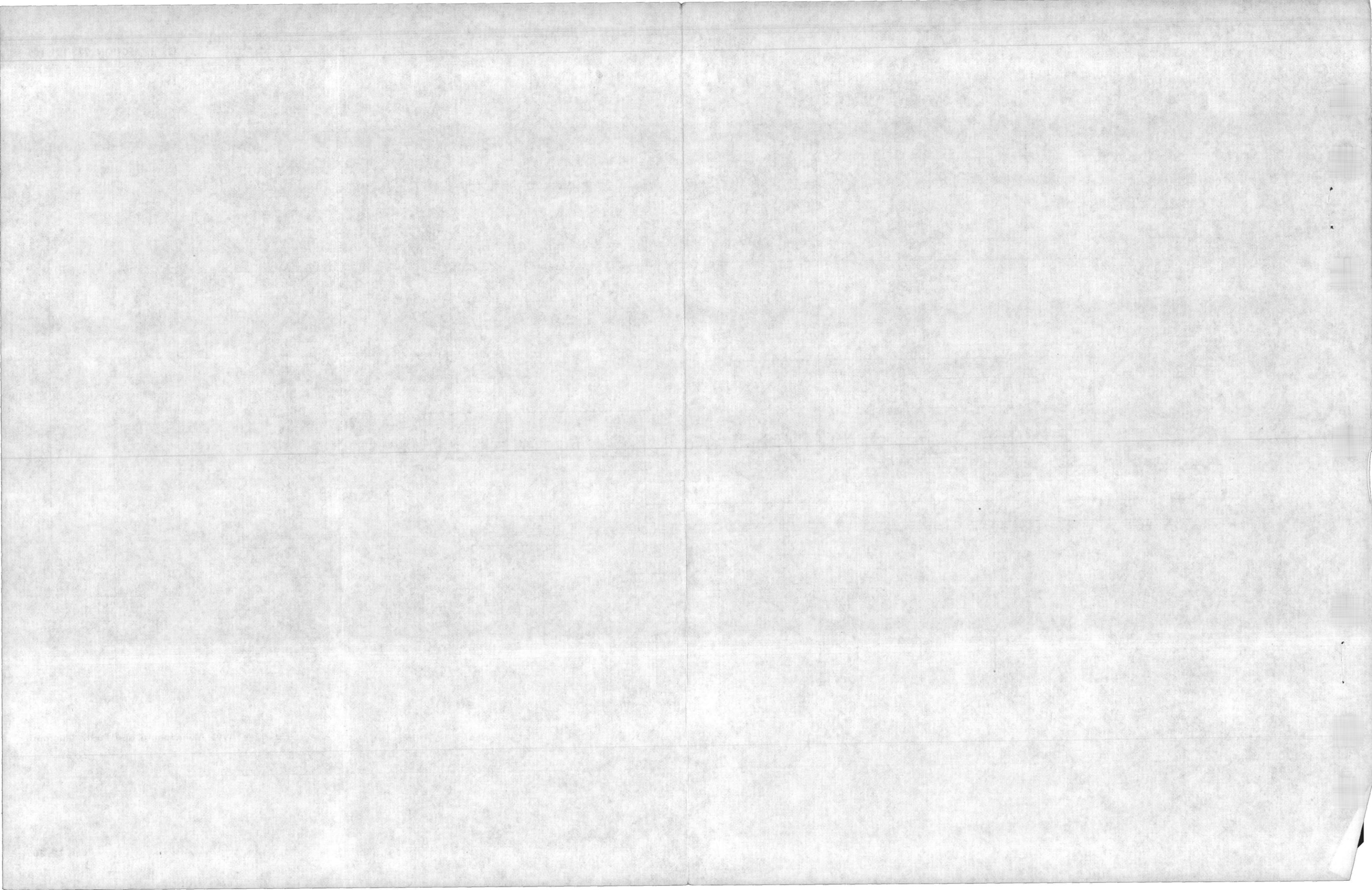
Fig. 12—FA995 Maintenance and Parity Diagram

of the current detectors in the level control board (FC207).

**6.19** Several functions are provided by data bits 14 and 15. Coded in one-of-four combinations as follows:

| BITS 15 , 14 | ACTION |
|---|---|
| 1 , 1 | Normal order (no special action) |
| 0 , 1 | Turn off (the flip-flop which controls voltage on level control board is cleared) |
| 1 , 0 | Turn on (the flip-flop which controls voltage on the level control board is set) |
| | Inhibit vertical selection |
| | Turn off pull-down transistor on false vertical |
| 0 , 0 | Turn off pull-down transistor on false vertical. |

## 7. REFERENCES

**7.01** Listed below are additional sections and other documents which are relevant to this section.

Section 966-210-100—General Description No. 3 Electronic Switching System

Section 233-121-110—Frame Input/Output Controller Description and Theory of Operation No. 3 Electronic Switching System

Section 233-142-100—TOP Maintenance Volume

SD-3H110-01—Peripheral Control Circuit

SD-3H150-01—Distribute Point Circuit

CPS-FC181—Peripheral Decoder Circuit

## 8. GLOSSARY

**8.01** A glossary of terms is provided to aid in the understanding of definite words in this section.

*Buffer*    A storage device used to compensate for a difference in the rate of flow of information or time of occurrence of events when transmitting from one device to another.

*Frame Input/Output Controller*    An interface between the 3A CC and the peripheral controllers. It converts the information between serial and parallel forms (depending upon the direction of flow) and gates the data to and from the peripheral controllers.

*Junctor*    A circuit associated with the switching network which provides a path for a call through the network.

*Service Circuit*    An auxiliary circuit connected through the switching network to lines or trunks as required.

*State Relay*    Miniature wire-spring relays which provide the critical functions in trunk, service, and junctor circuits.

*System Control*    The combination of the control unit, FIOCs, network controllers, scanner controllers, and peripheral pulse distributors which together provide complete control of the periphery and whose status is switchable as a single unit. Except for the system status panel, the system control is duplicated for reliability purposes.

*Trunk*    A channel connecting switching centers or exchanges. An interface circuit for transmission and supervisory purpose.