FRAME INPUT/OUTPUT CONTROLLER
DESCRIPTION AND THEORY OF OPERATION
NO. 3 ELECTRONIC SWITCHING SYSTEM

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1. GENERAL

INTRODUCTION

1.01 This section provides a physical and functional description and the theory of operation of the frame input/output controllers (FIOCs) which are part of the periphery in the No. 3 Electronic Switching System (ESS).

1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.

PURPOSE OF FIOC

1.03 The FIOC units provide the interface for data transmission between the 3A central control (3A CC) and peripheral controllers (scanner controller, network controller, and peripheral pulse distributors).

1.04 The FIOC performs the following functions:

- Receives serial bit streams from the 3A CC and converts the stream to parallel signals for the peripheral controllers
- Checks incoming messages from 3A CC for validity (parity, start code)
- Provides enable signals for addressed peripheral controller
- Accepts a reply-enable and data from the addressed peripheral controller
- Generates parity and a start code for the reply
- Transmits the reply back to the 3A CC.

CONFIGURATION

1.05 Two FIOCs, two scanner controllers, two network controllers, and two peripheral pulse distributor controllers are provided on each control frame. One control frame (Fig. 1) is provided for No. 3 ESS offices equipped with up to seven network frames. An additional control frame is provided in offices equipped with eight or more network frames.

1.06 On the control frame, the FIOC and peripheral controllers are duplicated. One FIOC and each of the three peripheral controllers function under control of 3A CC 0; the duplicate FIOC and peripheral controllers function under control of 3A CC 1 (Fig. 2A).

1.07 Data is transmitted between each 3A CC and its dedicated FIOC via input/output subchannels. Four subchannels are used with each FIOC on one control frame. Four additional subchannels are used with each FIOC on the second control frame, when provided.

1.08 Data is transmitted in 6.67-megabit serial bipolar pulses between the 3A CC and FIOC. Data is transmitted in parallel form between the FIOC units and peripheral controllers (Fig. 2B).

2. PHYSICAL DESCRIPTION

2.01 The FIOCs are provided on circuit packs arranged for plug-in installation in apparatus mountings on the control frame. Each FIOC consists of four circuit packs: one FB351, one FA993, and two FA994.

INTERFACES

2.02 Each FIOC is connected to its controlling 3A CC by five coaxial cables. Four coaxial cables are used to send data to the FIOC. Each of these four cables corresponds to a 3A CC subchannel. The cable selected determines which peripheral controller is to receive the data. Coaxial

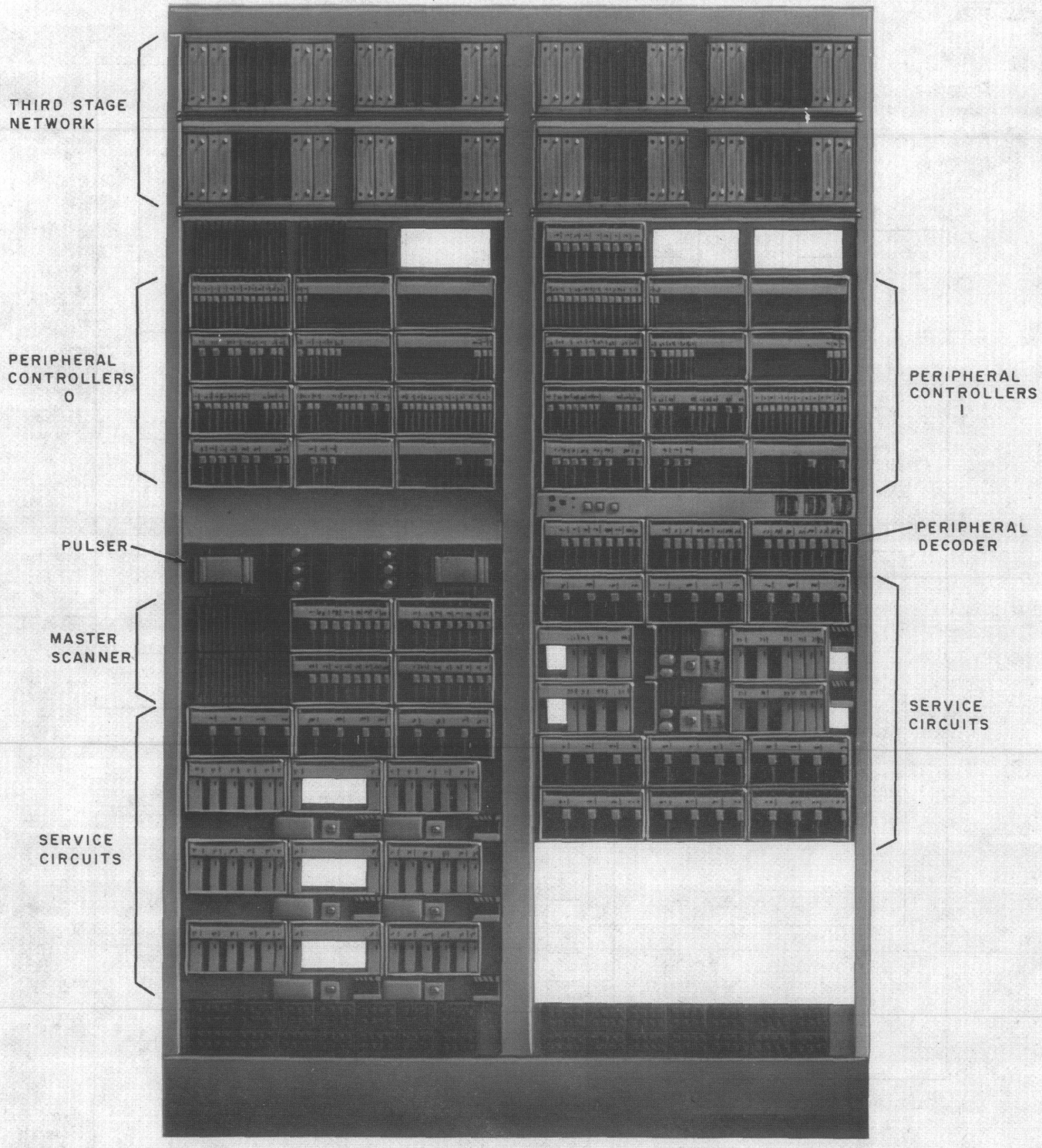


Fig. 1—Control Frame

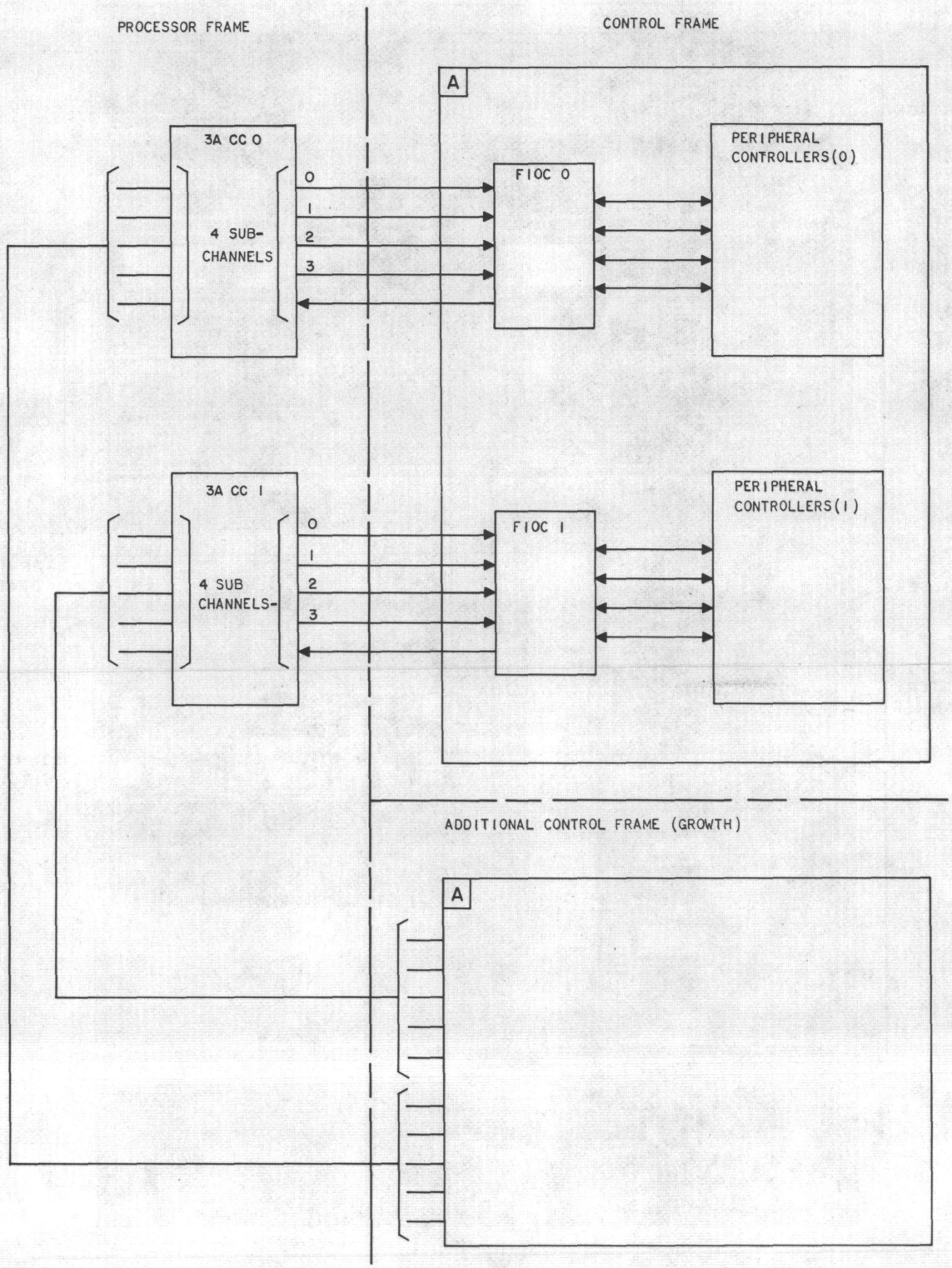


Fig. 2A—FIOC Relationship to No. 3 ESS System—Function Diagram

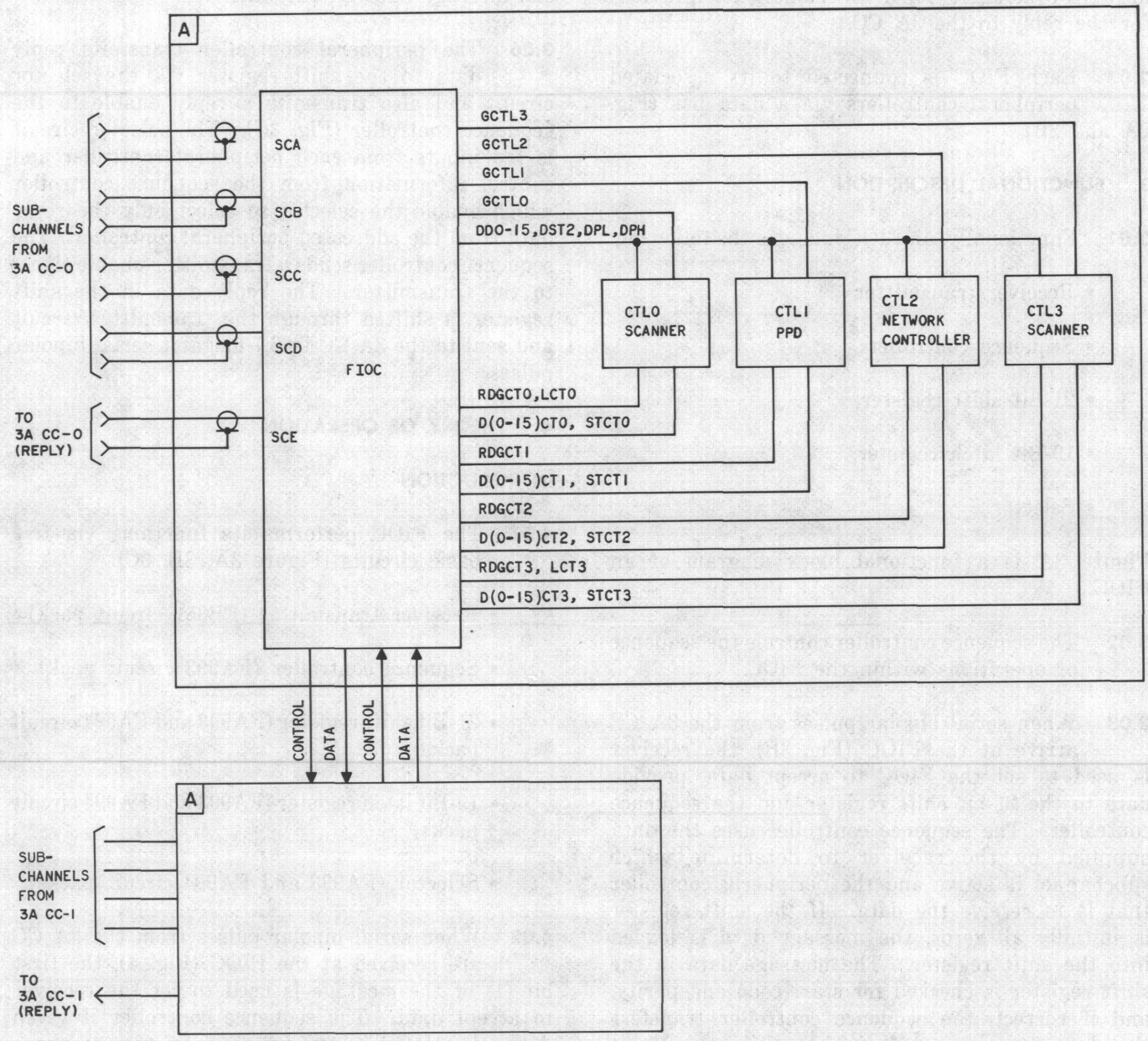


Fig. 2B—FIOC Relationship to No. 3 ESS System

cables 0 and 3 are associated with the scanner controller. Cable 1 is associated with the peripheral pulse distributor. Cable 2 is associated with the network controller. The fifth coaxial cable provides for the reply to the 3A CC.

2.03 Each FIOC is connected to its associated peripheral controllers via a data bus (Fig. 2A and 2B).

3. FUNCTIONAL DESCRIPTION

3.01 Functionally, an FIOC includes the following:

- Receiver/transmitter
- Sequence controller
- 21-Bit shift register
- 19-Bit latch register
- Selector.

Figure 3A is a functional block diagram of an FIOC.

3.02 The sequence controller controls the sequence of operations within the FIOC.

3.03 When serial bipolar pulses from the 3A CC arrive at the FIOC (Fig. 3B), the receiver is used to set the FIOC to accept data, provide data to the 21-bit shift register and the sequence controller. The sequence controller uses the data supplied by the receiver to determine which subchannel is active and the peripheral controller that is to receive the data. If the shift register is initially all zeros, the message data is loaded into the shift register. The message data in the shift register is checked for start code and parity, and if correct, the sequence controller transfers the data from the shift register into the 19-bit latch register.

3.04 The 21-bit shift register provides the capability to serially load message data from the 3A CC and transmit this data in parallel form. The shift register also provides the capability for the reply data from the peripheral controller to be parallel loaded and serially shifted to the 3A CC.

3.05 The message data from the shift register is loaded into the 19-bit latch register. The latch register then supplies this data to the peripheral controllers via a data bus. The sequence controller enables the addressed peripheral controller to accept the message data on the data bus.

3.06 The peripheral controller transmits reply data to the shift register via the selector circuit and also transmits a reply enable to the sequence controller (Fig. 3C). The selector circuit is fed inputs from each peripheral controller and control information from the sequence controller which enable the selector to select only the reply data from the addressed peripheral controller. The sequence controller sends a transmitter-enable signal to the transmitter. The reply data in the shift register is shifted through the transmitter circuit and sent to the 3A CC in 6.7-megabit serial bipolar pulses.

4. THEORY OF OPERATION

INTRODUCTION

4.01 The FIOC performs its functions via five basic circuits (Figure 3A, 3B, 3C).

- Receiver/transmitter (FB351 circuit pack)
- Sequence controller (FA993 circuit pack)
- 21-Bit shift register (FA993 and FA994 circuit packs)
- 19-Bit latch register (FA993 and FA994 circuit packs)
- Selector (FA993 and FA994 circuit packs).

4.02 When serial bipolar pulses from the 3A CC are received at the FIOC (Fig. 4), the first bit (1) of the message is used to set the receiver to accept data. The sequence controller is given data via the receiver which sets the sequence controller in the receive or purge state. The sequence controller records the active 3A CC subchannel and waits until the received data has been shifted into the 21-bit shift register.

4.03 After the 21-bit shift register is serially loaded, the sequence controller signals the receiver to stop shifting the shift register and transfers the data out of the shift register into the 19-bit latch register. The latch register places the data onto the data bus. This data is present

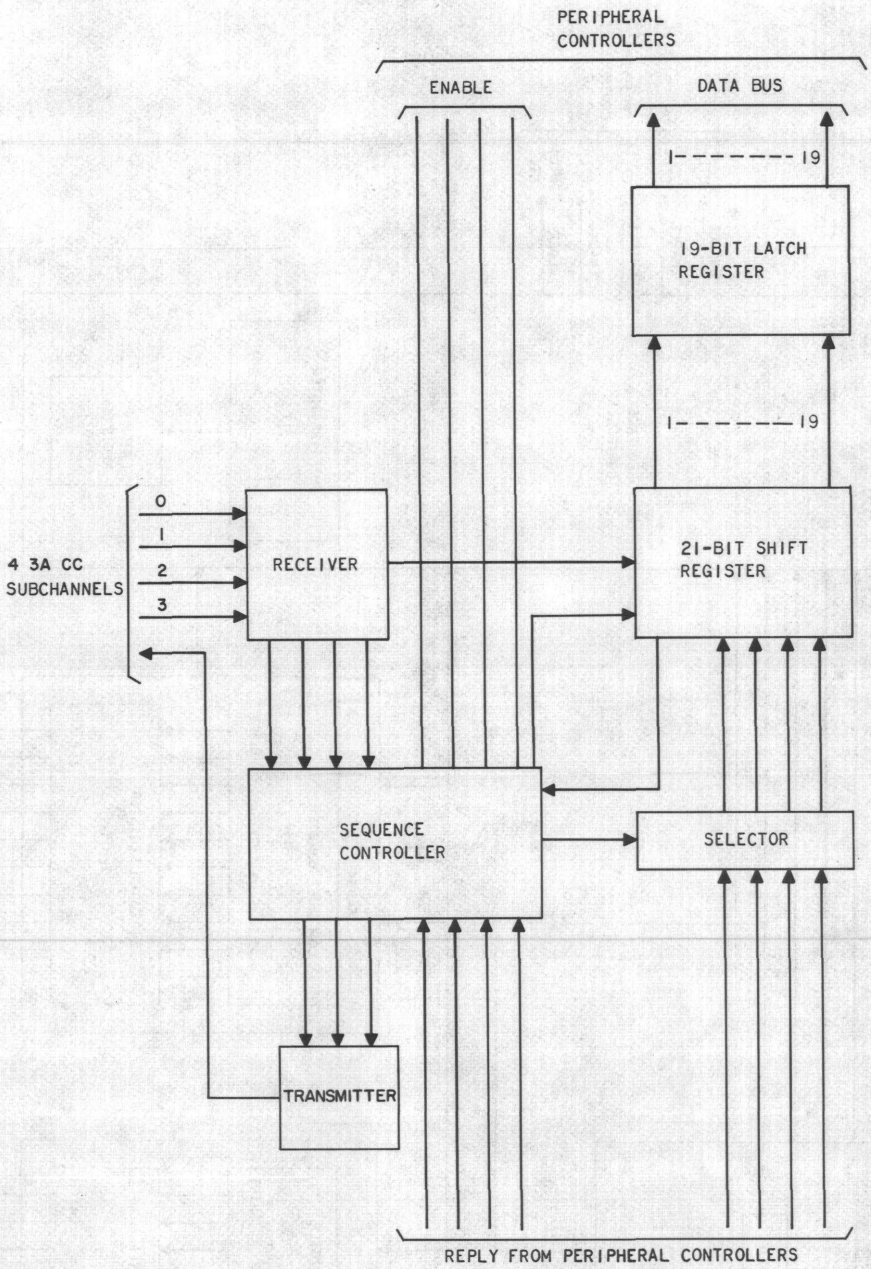


Fig. 3A—FIOC Functional Diagram

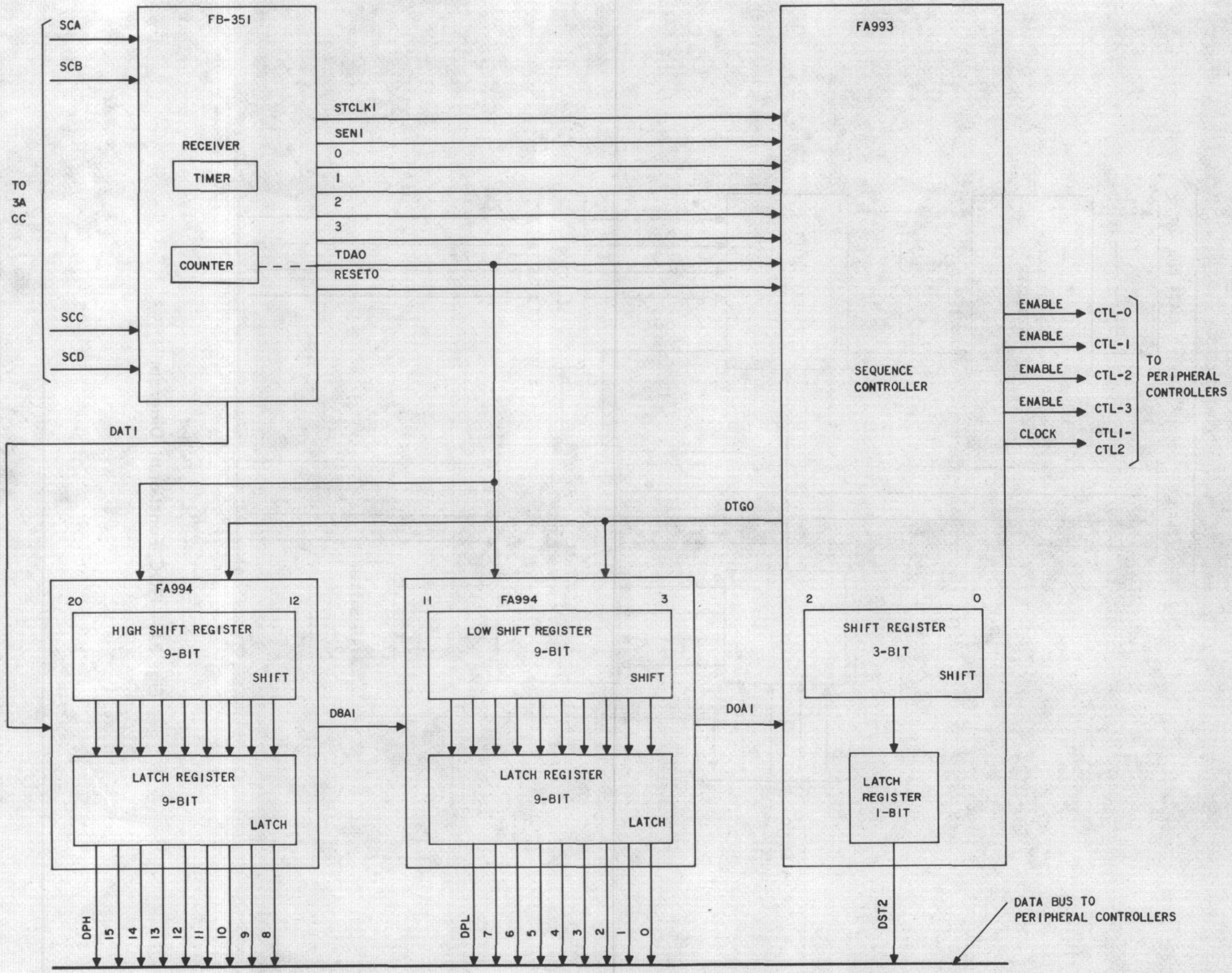


Fig. 3B—3A CC to Peripheral Controller Functional Diagram

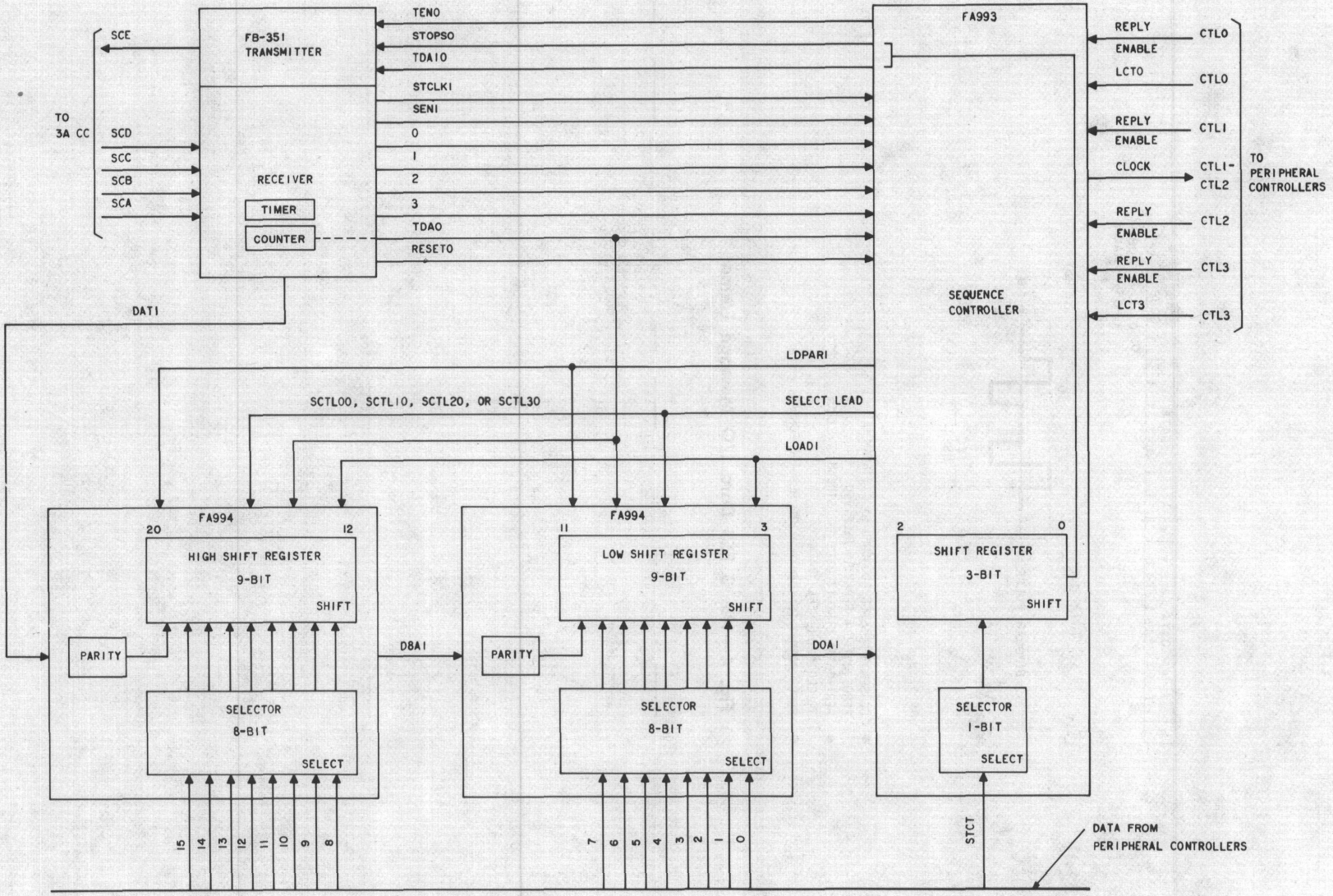
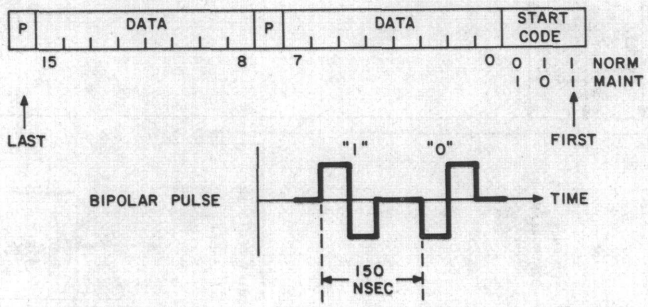


Fig. 3C—Peripheral Controller to 3A CC Functional Diagram



- CC SENDS MESSAGE FOLLOWED BY A STREAM OF ZEROS UNTIL A REPLY IS RECEIVED
- PERIPHERAL CIRCUIT USES THE STREAM OF ZEROS TO CLOCK THE REPLY BACK
- REPLY FORMAT IS IDENTICAL TO MESSAGE FORMAT

Fig. 4—No. 3 ESS Data I/O Message Format

on the data bus until new data comes into the latch register. The sequence controller enables the addressed peripheral controller to accept the data on the data bus.

4.04 When the peripheral controller has reply data ready, it transmits a reply enable to the sequence controller. The peripheral controller reply data is parallel-loaded into the shift register via the selector circuit. Selector circuit control is supplied by the sequence controller. This allows the selector circuit to accept data from the correct peripheral controller.

4.05 The sequence controller enables the transmitter. The reply data (16 data bits, 2 generated parity bits, and 3 bits of a generated start code) is then gated through the transmitter via the sequence controller. The transmitter converts the reply data input to bipolar pulses and transmits them to the 3A CC.

4.06 After communication between the 3A CC and FIOC is completed, the absence of a bit stream places the receiver in the idle state.

RECEIVER/TRANSMITTER (FB351)

A. Receiver

4.07 Prior to data transmission from the 3A CC, the FIOC receiver is in the idle state. The receiver was placed in the idle state by the action of the discrete timer (C1, T1, and T2). The absence of an input message from the 3A CC (for approximately 1 microsecond) causes the timer capacitor to charge enough to operate the timer to the ON state. The operation of the timer to the ON state sets the idle flip-flop. An input message (Fig. 4) is transformer-coupled from the 3A CC to the receiver and transmitted over the SCA, SCB, SCC, or SCD leads (Fig. 3B). When the first data bit (1) of an input message is received, the timer capacitor starts to discharge. At least three pulses must be received to ensure the timer transition to the OFF state.

4.08 The receiver derives clock pulses (STCLK1) from the bipolar bit stream and gates them to the sequence controller. The first clock pulse of a new message, in combination with the output of the idle flip-flop (RESET0), is used to reset the sequence controller to the PURGE or RECEIVE state. The idle flip-flop is then cleared at the end of the first message bit.

4.09 The receiver also generates a 6.67 MHz clock signal (CLK81) which is used by the network controller and peripheral pulse distributor for internal sequencing.

4.10 The receiver gates data to the sequence controller (RCVX00, RCVX10, RCVX20, or RCVX30) indicating which subchannel (0 through 3) is active. Serial data (21 bits) is gated by the receiver to the shift register (high/low shift register) input (DAT1). The shift clock (TDA0) is also gated to the shift register. The shift clock (as well as the state clock pulse, STCLK1) is derived in the receiver by two flip-flops. One flip-flop is set by the negative lobe of the bipolar pulse and the other is set by the positive lobe. The combination of both flip-flops being set and the absence of a positive or negative lobe is used to generate the shift pulse and to reset the two flip-flops in preparation for the next message bit. When the initial 1 of the message is shifted to the end of the shift register, the sequence controller gates a signal (STOPS0) to the receiver to inhibit further shift pulses.

4.11 The 3A CC follows the message data with a stream of zero bits until a reply is received from the peripheral controller via the transmitter. Communication between the 3A CC and the FIOC is complete when the reply has been received by the 3A CC. After the 3A CC stops sending data, the FIOC goes into the idle state.

B. Transmitter

4.12 The transmitter gates the reply data from the peripheral controller (with correct parity and start code) to the 3A CC. The reply data message format is the same as No. 3 ESS input/output message format (Fig. 4). When reply data is ready, the sequence controller sends a transmit-enable signal (TEN0) to the transmitter (Fig. 3C). The initial 1 of the reply is gated into the transmit data flip-flop (TDATA) by the shift inhibit flip-flop (INHS0). After this 1 is transmitted, the output of the transmitter enable flip-flop (TEN) is used to clear the shift inhibit flip-flop. Subsequent shift pulses (TDA0) cause the shift register to send the reply bits, in sequence, to the transmitter via lead TDA10. The reply data and reply data complement are clocked through the transmitter using the zeros

being received from the 3A CC as clocking pulses. The reply data is used to generate bipolar pulses in the transmitter. The transmitter transformer-couples these bipolar pulses via the coaxial cable (SCE) to the 3A CC. The data transmission is complete when all 21 bits of data (18 bits from the shift register and 3-bit start code from sequence controller) are transmitted to the 3A CC.

SEQUENCE CONTROLLER (FA993)

4.13 The sequence controller controls the sequence of operation within the FIOC. When a data message is sent to the FIOC, the receiver sends a STCLK1 pulse and a RESET0 signal to the sequence controller which are used by the sequence controller to clear the five-bit state register. The state register flip-flops (STA, STB, STC, STD, and STE) are the main control devices in the sequence controller. STCLK1 is also used as a clocking pulse for the state registers. The receiver sends a subchannel identify signal to the sequence controller (RCVX00—subchannel 0, RCVX10— subchannel 1, RCVX20—subchannel 2, RCVX30— subchannel 3). This signal sets a latch in the sequence controller. This latch identifies which peripheral controller is to receive the message.

4.14 The operation of the sequence controller can be described by use of a state diagram (Fig. 5). The state number (00000) represents the condition of the state register - the first digit corresponds to STA, the second digit to STB, etc. STCLK1 and RESET0 from the receiver initially set the sequence controller into either the PURGE (00000) or RECEIVE (10000) state. This is determined by the shift register (AZKL0 from low shift register, AZKH0 from high shift register all zero check signal). If the register contains all zeros, the sequence controller goes into the RECEIVE state; otherwise, the sequence controller goes into the PURGE state.

4.15 In the PURGE state, the message data is ignored and the zeros following the data message are shifted into the shift register loading it with all zeros. These zeros are normally used to clock reply data to the 3A CC. Since the 3A CC does not receive a reply from the peripheral controller, it retries the message. This time, because the shift register is loaded with all zeros, the sequence controller goes into the RECEIVE state. The shift register must be loaded with all zeros, so that the sequence controller can detect when the first bit (1) of the message is shifted into the rightmost slot of the shift register. When the leading "1" is detected in the rightmost slot of the shift register, the sequence controller goes into the TRANSFER (10001) state and generates the data transfer gate (DTG0) to load the data from the shift register into the latch register. Two conditions must now be satisfied before the sequence controller will advance to the GO state (GO0-01110 for scanner controller, GO1-10110 for PPD, GO2-11010 for network controller, and GO3-11100 for scanner controller). Either a normal start code (110) and correct parity (PKT from both FA994s) must be received or a maintenance start code (101) and any parity must be received. If one of these two conditions is not met, the sequence controller stays in the TRANSFER state and the 3A CC will retry the message. If either of these two conditions is met, the sequence controller goes into one of the GO states.

4.16 In the GO state the controller enable lead (GCTL0—scanner controller, GCTL1—PPD 1, GCTL2—network controller, or GCTL3—scanner controller) is activated. This signal enables the addressed peripheral controller to accept the data already placed on the data bus by the 19-bit latch register. In the GO state a selector circuit enable lead (SCTL00—scanner controller, SCTL10—PPD, SCTL20—network controller, and SCTL30—scanner controller) is activated for the selection of reply data from the addressed peripheral controller. Additionally, during the GO state the LOAD1 lead is activated to load (in parallel) the reply data from the addressed peripheral controller into the shift register via the selector circuit.

4.17 During the GO state, the reply data enable lead (RDGCT0—scanner controller, RDGCT1—PPD, RDGCT2—network controller, and RDGCT3—scanner controller) from the addressed peripheral controller must be activated for the sequence controller to go to the reply (RPL) state (11110). During the RPL state, the load parity lead LDPAR1 is activated to load generated parity into the parity locations in the shift register. Also, during the RPL state the transmitter enable lead (TEN0) is activated. This allows the transmitter to begin the transmission to the 3A CC. The controller enable leads (GCTL0, GCTL1, GCTL2, and GCTL3) must be inactive for the sequencer controller to advance to the transmit (XMIT) state (11111).

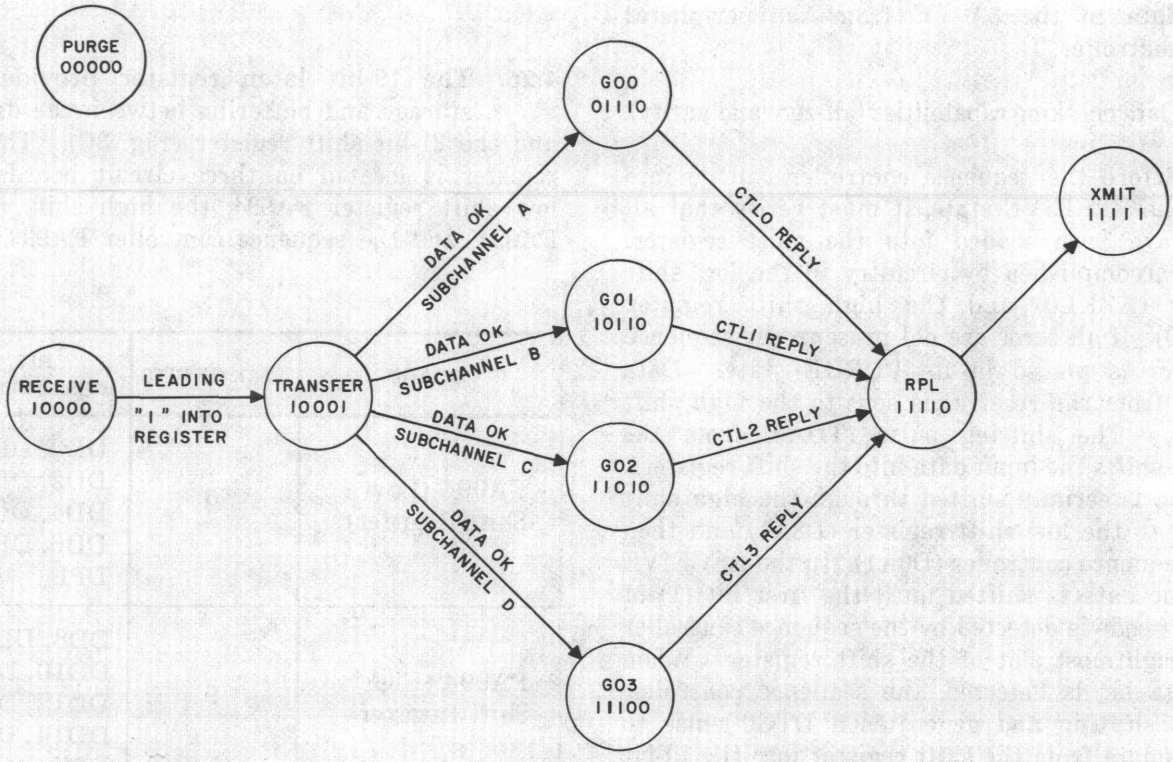


Fig. 5—Sequencer Controller State Flow Chart

4.18 With the sequence controller in the XMIT state, the 16 data bits and the 2 generated parity bits are serially shifted from the shift register to the sequence controller. A 3-bit start code is generated and shifted ahead of the data and parity bits to the transmitter. The transmitter converts this data to bipolar pulses and sends it to the 3A CC using the incoming zeros from the 3A CC as clocking pulses. These zeros are also shifted into the shift register.

4.19 Leads LCT0 and LCT3 are dedicated to the scanner. These leads control the loading of the reply from the scanner into the shift register. During a specified time interval when leads LCT0 or LCT3 are low, a momentary low on the reply data leads will load a zero into the associated bit in the shift register.

21-BIT SHIFT REGISTER (FA993-FA994)

4.20 The 21-bit shift register is located on three circuit boards - the low shift register FA994, the high shift register FA994, and the sequence controller FA993 (Fig. 3C).

BOARD	NO. OF BITS	BIT DESIGNATION
FA994 (Low Shift Register)	9	DD0, DD1, DD2, DD3, DD4, DD5, DD6, DD7, DPL
FA994 (High Shift Register)	9	DD8, DD9, DD10, DD11, DD12, DD13, DD14, DD15, DPH
FA993 (Sequencer Controller)	3	3-bit start code

4.21 Functionally the shift register provides:

- Serial-in/parallel-out shift register for data to the peripheral controller from the 3A CC

- Parallel-in/serial-out shift register for reply data to the 3A CC from the peripheral controller

- Data checking capabilities (all-zero and parity).

4.22 Before the sequence controller can go into the RECEIVE state, it must verify that all zeros have been loaded into the shift register. This is accomplished by circuitry in the low shift register (AZKL0) and the high shift register (AZKH0). If all zeros are not present, the sequence controller is placed in its PURGE state. Data (DAT1) from the receiver is sent to the high shift register. The shifting pulse (TDA0) from the receiver shifts the input data into the shift registers. The data is serially shifted through the high shift register to the low shift register (D8A1) and then to the sequence controller (D0A1). In the RECEIVE mode the data is shifted until the first bit (1) of the start code is detected by the sequence controller in the rightmost slot of the shift register. When this data bit is detected, the sequence controller inhibits shifting and generates a DTG0 pulse to load the data from the shift register into the 19-bit latch register (21 bits minus 2 bits of start code).

4.23 The low shift register and high shift register send parity information to the sequence controller (PKT). The sequence controller performs a parity check on the data sent from the 3A CC and provides for the generation of parity on the reply data sent from the peripheral controller.

4.24 Data returned from the peripheral controller is loaded (in parallel) into the shift register via a selector circuit which was enabled by the sequence controller. After the shift register is loaded, the generated parity bits (DPL and DPH), on command from the sequence controller (LDPAR1), are loaded into the shift register.

4.25 When the sequence controller goes into the XMIT state, the reply data (16 data bits, 2 generated parity bits and 3-bit start code) is gated serially to the transmitter. (TDA0 is derived from the incoming bit stream and provides the shifting pulse). As the reply data is being shifted out of the shift register, the incoming zero bits (used for clocking reply data out) are loaded into the shift register.

19-BIT LATCH REGISTER (FA993-FA994)

4.26 The 19-bit latch register provides data storage and buffering between the data bus and the 21-bit shift register (Fig. 3C). The latch register is located on three circuit boards - the low shift register FA994, the high shift register FA994, and the sequence controller FA993.

BOARD	NO. OF BITS	BIT DESIGNATION
FA994 (Low Shift Register)	9	DD0, DD1, DD2, DD3, DD4, DD5, DD6, DD7, DPL
FA994 (High Shift Register)	9	DD8, DD9, DD10, DD11, DD12, DD13, DD14, DD15, DPH
FA993 (Sequencer Controller)	1	DST2

4.27 The latch register is loaded with the data from the shift register when the sequence controller goes into the TRANSFER state. The data in the latch register is placed onto the data bus (parallel). This data is present on the data bus until changed by another data message.

SELECTOR (FA993-FA994)

4.28 The selector provides control gating for the reply data from the peripheral controllers to the shift register. The control is provided by the sequence controller.

4.29 The selector is located on three circuit boards - the low shift register FA994, the high shift register FA994, and the sequence controller FA993.

BOARD	NO. OF BITS	BIT DESIGNATION
FA994 (Low Shift Register)	8	D0CT__, D1CT__, D2CT__, D3CT__, D4CT__, D5CT__, D6CT__, D7CT__
FA994 (High Shift Register)	8	D8CT__, D9CT__, D10CT__, D11CT__, D12CT__, D14CT__, D15CT__
FA993 (Sequencer Controller)	1	STCT__

4.30 The selector has data inputs from five sources: the duplicate (mate) FIOC, scanner (CTL0 and CTL3), peripheral pulse distributor (CTL1), and network controller (CTL2). The sequence controller provides the control (mate FIOC-READ0, CTL0-SCTL00, CTL1-SCTL10, CTL2-SCTL20, and CTL3-SCTL30) so the selector will accept data from the correct source.

4.31 When the sequence controller is in the GO state, it enables the proper selector enable lead (SCTL_) so the selector will gate only the information from the addressed peripheral controller into the shift register.

5. POWER

INTRODUCTION

THEORY OF OPERATION—POWER AND ALARM CIRCUIT

+3 VOLT AND +24 VOLT POWER DISTRIBUTION

5.01 ***Power Requirements:*** Power for the FIOC is obtained from the control frame. The FIOC requires +3 volts for the logic.

5.02 ***Power and Alarm Circuits:*** The +3 volt power converter J87389F, +3 volt power reference and filter circuit pack (FC21), and one +12 volt power reference circuit (FB152) are supplied in the peripheral control unit. The -48 volts supplied by the power plant to the control frame is converted by the converter J87389F to the +3 volts required by the FIOC.

5.03 All the circuits in a peripheral control unit have their own power system: two J87389F, +3 volt power converters; one FC21, +3 volt power reference and filter circuit pack; and one FB152, +12 volt power reference circuit pack. The power system also distributes +24 volts, +3 volts, and ground (GRD) to the peripheral controllers circuit packs via the multilayer printed wiring boards (MLPWB) (Fig. 6). The control frame circuit also provides +24 volts and -48 volts to the two J87389F power converters.

5.04 The control frame circuit provides power control, fusing, and alarms for the peripheral controllers. The power control and alarm circuit consists of four circuit packs: two FB414, 3-volt power control 0 and 1; and two FB415, alarm 0 and 1. Associated with the control frame power is a control panel and two fuse panels. The control panel has three nonlocking (nlk) keys (ON, REQ, and OFF) and two lamps (OOS and PWR OFF) which are duplicated for peripheral controller 0 and 1. The fuse panel contains power fuses for protecting each controller in the periphery. The control frame circuit (SD-3H902-01) contains the following power-related functional schematics: FS41 - +24 volt power control, fusing, and alarms; FS42 - -48 volt power control, fusing, and alarms; FS43 - power sequencing; FS44 - alarm and test; and FS45 - scan points. The various circuits associated with SYC 0 and SYC 1 are duplicated.

+24 VOLT POWER CONTROL, FUSING, AND ALARMS

5.05 The control frame circuit separately distributes +24 volts to each MLPWB in the peripheral control unit when each PWR relay is operated. Each power lead is fused with a 70-type fuse. When the fuse opens, an auxiliary circuit is completed which provides +24 volts to operate one of the 24FA relays. Separate fuses exist in the fuse panels for peripheral control circuit 0 and 1. In addition to distributing +24 volts to all four J87389F power converters, the control frame circuit starts the converters by switching +24 volts to their 24VST lead. The switching occurs under the following conditions: The 24ST relay operated, the 24FA relay released, and the 48FA relay released.

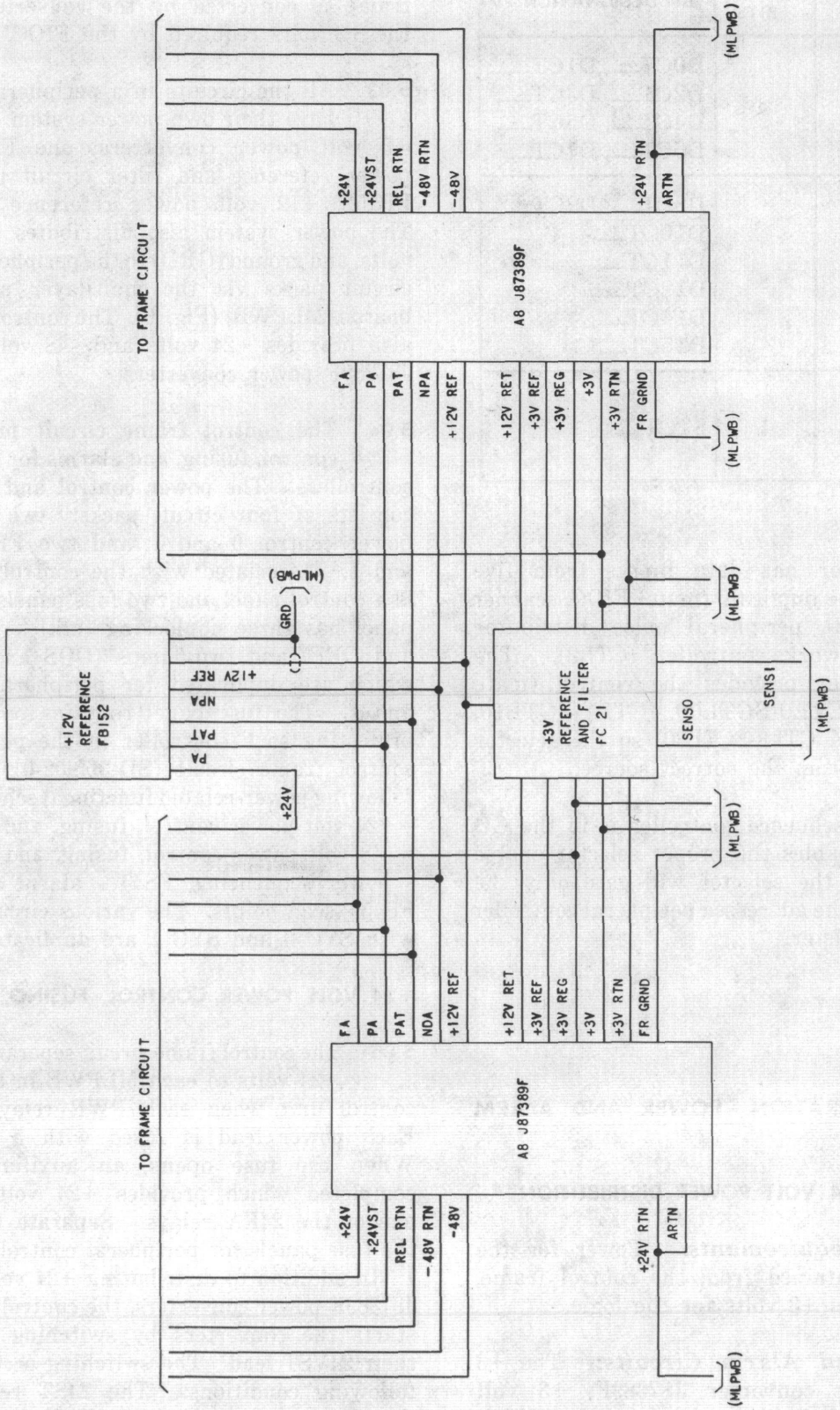


Fig. 6—+3 Volt and +24 Volt Power Distribution

-48 VOLT POWER CONTROL, FUSING, AND ALARMS

5.06 The control frame circuit separately distributes -48 volts to a large number of individually fused circuits in the periphery. If a fuse opens, the auxiliary circuit operates one of the 48FA relays or one of the SFA relays. The 48FA relays are only operated by the fuses on the lines distributing -48 volts to the J87389F power converters. An open fuse in any of the remaining -48 volt fuses will cause the SFA relays to operate.

POWER SEQUENCING

5.07 Each set of J87389F power converters is started by depressing the associated ON (nlk) key on the control panel which provides a ground path to operate the associated 24ST relay. The associated set of power converters must supply +3 volts to a transistor circuit before it provides a ground path to operate the appropriate PWR relay. This relay keeps the 24ST relay operated after the ON (nlk) key is released. The PWR OFF lamp is extinguished while the (out-of-service) OOS lamp remains lighted. When the REQ (nlk) key is depressed, the request ferrod scan point notifies software to run diagnostics on the peripheral controller. Once diagnostics are complete, the controllers are restored to service. The OOS lamp is extinguished when the peripheral decoder releases the OOS relay. The circuitry for removing power operates much in the same way. When the REQ (nlk) key associated with the off-line peripheral controllers is depressed, software responds by removing the controllers from service and lights the OOS lamp. Once the OFF (nlk) key is depressed a transistor circuit releases the PWR and 24ST relays. The PWR OFF lamp is lighted and J87389F power converters are disabled. Should emergency removal of power be required, depressing the REQ (nlk) key and OFF (nlk) key simultaneously will force the J87389F power converters to be disabled and the +24 volts to be removed from the peripheral controllers.

ALARM AND TEST

5.08 The lamp circuit has a lamp test capability. Depressing the LP & PWR TEST (nlk) key closes a circuit path to light both sets of OOS, PWR OFF, and FA lamps. Individually, the OOS lamp is lighted with the OOS relay operated; the PWR OFF lamp is lighted with the PWR relay released; and the FA lamp is lighted with the 24FA, 48FA or SFA relay operated. The alarm circuit has the capability for a number of different alarms. The J87389F power converters have an overvoltage and overcurrent (fuse alarm) FA signal. This FA signal is sent to the alarm circuit where a transistor switch operates the CFA relay. The alarm circuit keeps the CFA relay operated until released by depressing the LP & PWR TEST (nlk) key located on the peripheral control panel in the control frame. This is necessary since the loss of one converter will shut off all power to one peripheral control circuit. The J87389F power converters and the FB152 reference board also have an out-of-voltage limits (power alarm) PA signal. Similarly, this PA signal is sent to the alarm circuit where another transistor switch operates the CPA relay.

5.09 The alarm circuit has the facility for power alarm test (PAT). The system, via the peripheral decoder, operates the PAT and OOS relays. A PAT signal is sent to the set of J87389F power converters and the FB152 board. These should respond by operating the CPA relay and thus unsaturating the PA scanpoint. In the alarm circuit the NPA relay operates only when a J87389F or a FB152 fails to give a PA. The NPA relay then keeps the PA scan point saturated. As the PAT relay is released, a ground is briefly applied to the NPA leads of the J87389F converters and FB152 reference board to extinguish the light emitting diodes (LEDs). When the OSS relay is released, a PAT signal can be generated by depressing the LP & PWR TEST (nlk) key. When the key is released, a ground is sent to extinguish the LEDs. When there is no PA, the associated LED fails to light. Scan points are not affected by a manual PAT.

SCAN POINTS

5.10 The scan point circuit contains three ferrods which are concerned with power control and alarms. The state of certain relays and keys determines whether current flows in the ferrod control windings. The request ferrod is saturated with the 24ST relay operated and the REQ (nlk) key released. The power alarm ferrod is saturated with the 24ST relay operated and any of the four following conditions: the LP & PWR TEST (nlk) key depressed, the REQ (nlk) key depressed, the NPA relay operated, or the CPA relay released. These two ferrods are encoded into four states (OFF, REQUEST, ON, and POWER ALARM).

When both ferrods are unsaturated, the state is OFF. With the REQUEST ferrod unsaturated and the POWER ALARM ferrod saturated, the state is REQUEST. When both ferrods are saturated, the state is ON. Finally, with the REQUEST ferrod saturated and the POWER ALARM ferrod unsaturated, the state is POWER ALARM. The major control alarm ferrod is saturated with all three CFA, 24FA, and 48FA relays released. All three ferrods are duplicated for peripheral controllers 0 and 1.

6. MAINTENANCE

INTRODUCTION

6.01 The FIOC contains the following maintenance capabilities:

- FIOC is designed such that most faults will cause it to halt in some state and no reply will be provided
- A maintenance order provides the capability for an FIOC to read out status information (sequence controller state register, parity checks, zero checks, first and last bit in the low and high shift register FA994) from its mate FIOC
- Operation of the sequence controller can be tested by a maintenance order which jams the sequence controller into various abnormal states. The results of these tests can then be read by the mate FIOC.

BUILT-IN MAINTENANCE CAPABILITY (SYSTEM)

6.02 When a trouble condition occurs, the sequence controller does not receive the necessary input to change its state. When the trouble condition has not been cleared after a third trial, the standby 3A CC, FIOC, and peripheral controllers are switched on-line. Once problems are detected, diagnosing the faulty peripheral controllers must be initated by a manual request.

6.03 The active 3A CC can transmit diagnostics to its associated on-line FIOC. The diagnostics send data patterns to the faulty (off-line) FIOC and direct the contents of the faulty FIOC to be read back to the active 3A CC. The diagnostic program identifies the fault in the FIOC and/or peripheral controller and calls for a TTY printout.

FIOC

6.04 The following maintenance capabilities may be used with the diagnostics:

- Mate FIOC reads contents of state registers in sequence controller of FIOC
- Mate FIOC checks FIOC for correct parity (RPK0), zero check (ZKL0 and ZKH0), and data okay (DOK0).

6.05 The mate FIOC can send a reset (RDOUT0) command which will cause the FIOC to reset to the PURGE or RECEIVE state depending on whether the shift register is non-zero (PURGE) or zero (RECEIVE). The FIOC receiver must be in the idle state for this to occur.

6.06 A message received on SCA (Figure 7) with a maintenance start and good parity and which has data bits 12 through 15 all ones will be recognized as a diagnose order. The normal transition to the GO0 state is suppressed. Data bits 0 through 4 of the message are loaded into the state register. Subsequent action (if any) is dependent on the state code loaded. For many state codes, no reply will be generated and the result must be read out by the mate FIOC.

6.07 The sequence controller has two additional states (as noted by the state registers) used for maintenance. The RDOUT (00010) state which allows the FIOC to reset the mate FIOC state register to clear an undesirable condition, and the READ (00100) state which allows the state of the mate FIOC to be loaded into the shift register.

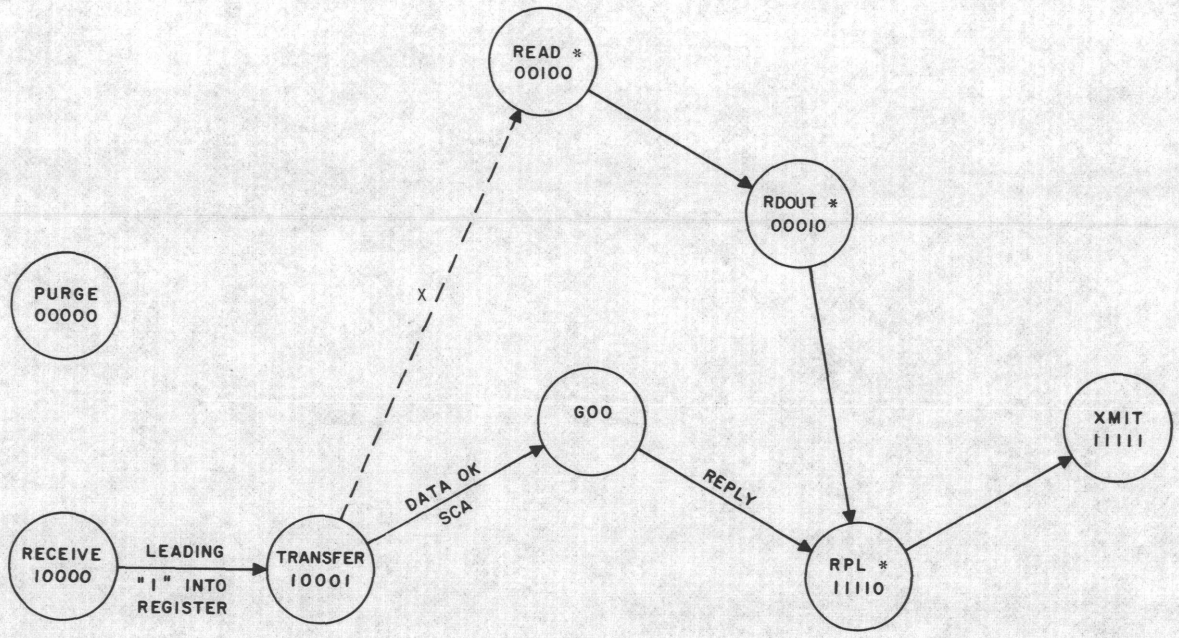
6.08 In addition to the state register and parity checks, the mate FIOC can also read the first and last bits (SRSTRT1 and SREND1, respectively) of the low shift register and the high shift register.

7. REFERENCES

7.01 The following list of Bell System Practices contains pertinent sections which are relevant to this section:

Section 233-110-100—3A Central Control Description

Section 233-110-200—3A Central Control Theory of Operation



* STATES MARKED * ARE TRANSITIONAL STATES, THE EXIT FROM WHICH IS DEPENDENT ONLY ON INTERNAL CONDITIONS
X LOADED STATE CODE RESULTS IN READ OUT BY MATE FIOC

Fig. 7—Maintenance Sequencer Controller State Flow Chart

Section 233-120-100—Switching Network Description and Theory of Operation

Section 233-121-100—Scanner Description and Theory of Operation

Section 233-121-105—Peripheral Pulse Distributor and Peripheral Decoder Description and Theory of Operation

Section 233-142-100—TOP Maintenance Volumes

Section 966-210-100—General Description No. 3 Electronic Switching System.

8. GLOSSARY

8.01 A glossary of terms is provided to aid in the understanding of definitive words in this section.

Latch Register A storage device that is fed data in parallel form and can maintain this data until it is changed

MLPWB Multilayer printed wiring board

Parity "The quality of being equal," that is each data word is to contain an odd or even number of 1 bits (including parity bit if used)

Shift Register A device that can shift digital data from one bit position to another and maintain the integrity of the original data pattern

Start Code (Input/Output) A 3-bit code used to notify a device of an input/ouput message and the type of input/output message - normal or maintenance.