

**PERIPHERAL UNIT DIAGNOSTICS
SOFTWARE SUBSYSTEM DESCRIPTION
NO. 3 ELECTRONIC SWITCHING SYSTEM**

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NOTICE

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C. Distributor Points (RT)	36	233-121-110	Frame Input/Output Controller Descriptive and Theory of Operation
1. GENERAL		233-153-140	Peripheral Unit Fault Recovery Software Subsystem Description
1.01 This section describes the operation of the No. 3 Electronic Switching System (ESS) peripheral unit diagnostic tests. A description of the software as well as the physical tests is included for the following peripheral units:		233-154-145	Pudal Diagnostic Language Software Subsystem Description
• Frame input/output controller		254-300-170	Tape Data Controller Descriptive and Theory
• Network controller		254-300-190	Teletypewriter and Teletypewriter Controller Descriptive and Theory of Operation.
• Peripheral pulse distributor			
• Ringing and tone plant			
• Scanner controller			
• Tape data controller			
• Teletypewriter controller.			
Instructions are included on execution of diagnostic tests and interpretation of the test results.			
1.02 Whenever this section is reissued, the reason for reissue will be listed in this paragraph.			
1.03 Table A is a list of abbreviations and acronyms that are applicable to this section.			
1.04 The following Bell System Practices provide background and more detailed information on some of the operations that are briefly described in this document.			
		1.05	The following programs implement the major portion of the peripheral unit diagnostics:
		(a)	Diagnostic Control Program (DCON), PR-3H266-01, is the monitor and control portion of the peripheral unit diagnostic tests (except for the tape data controller [TDC]) which are in table-driven form.
		(b)	Diagnostic Pudal Statement Execution Subroutines (DCNSUB), PR-3H265-01, contain the subroutines required to interpret the peripheral unit diagnostic language (PUDAL) macro statements.
		(c)	Frame Input/Output Controller Diagnostic (FIOCT), PR-3H267-01, contains the data tables pointing to interpretive routines in DCNSUB that are used to execute diagnostic tests of the frame input/output controller (FIOC).
		(d)	Network Controller Diagnostic (NTCT), PR-3H268-01, contains the data tables of

the table-driven diagnostics used to test the network controller.

- (e) Peripheral Pulse Distributor Diagnostic (PPDT), PR-3H269-01, contains the data tables required to generate the peripheral pulse distributor (PPD) diagnostic tests.
- (f) Scanner Controller Diagnostic (SCNT), PR-3H271-01, contains the data tables required to generate the scanner controller diagnostic tests.
- (g) Ringing and Tone Plant Diagnostic (RTPR), PR-3H270-01, contains the data tables required to generate the ringing and tone plant diagnostic tests.
- (h) Tape Data Controller Diagnostic (CTAPM), PR-1C958-02, contains the 3A Central Control (3A CC) coding required to test the TDC. It also contains its own monitor and diagnostic TTY message handler. The CTAPM program is coded for common system usage and does not utilize the PUDAL language.
- (i) The TTY Controller Diagnostic (TTYT), PR-3H272-01, contains the data tables required to generate the TTYC diagnostic test.

1.06 The peripheral unit diagnostic program interrelationships are shown in Fig. 1 (except for the TDC). This configuration contains the elements of a table-driven system, which is explained later in this section. The tape data controller diagnostic is a stand-alone program that can be utilized by any system using the 3A CC and tape system for memory backup.

2. PERIPHERAL UNIT DIAGNOSTIC TEST PHILOSOPHY

2.01 Peripheral unit diagnostic tests generally are not run automatically on the No. 3 ESS. The diagnostic tests must be requested manually except when run as part of the daily diagnostic routine. Brief descriptions of the fault detection, analysis, and recovery are included in the following paragraphs to demonstrate how the determination for manual diagnostics may be made.

FAULT DETECTION METHODS

2.02 When peripheral unit faults occur, they must be detected, isolated, and reported.

Several methods for detecting these faults are available to the active control unit:

- All-seems-well (ASW) response from the peripheral controller upon receipt of order
- No reply from a peripheral controller order
- Incorrect reply from a peripheral controller order
- All-zeros order for scan matrix column failures.

FAULT ANALYSIS

2.03 If a peripheral order is initiated and fails, it will be reinitiated to determine whether the failure is continuous or transient. If the order fails on the second attempt (indicating a hard failure), a system control (SYC) switch is performed. The same order is then tried using the mate controller. If the order passes, the failure could exist in the duplicated (peripheral controller) portion of the system (Fig. 2). If the order fails after the SYC switch, the failure could exist in the nonduplicated portion of the system (peripheral decoder, network fabric, or scanner matrix).

2.04 A transient error is defined where a peripheral order is initiated and fails but is executed correctly when retried. A peripheral controller is considered faulty if more than seven transient errors occur within an hour.

FAULT RECOVERY

2.05 When a peripheral controller fault is detected, the following system recovery steps occur automatically:

- A switch is made to the healthy SYC.
- The failure is recorded in the status table.
- The problem is displayed on the system status panel (SSP).
- The peripheral control frame out-of-service (OOS) lamp lights.
- A major alarm is given.

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- A TTY message denoting the faulty peripheral controller is printed.

By executing this procedure, the system is able to continue operating and informing the craft person of faults that require corrective action. The associated diagnostic test can then be manually initiated to aid in isolating the fault area. After corrective action is complete, the diagnostic test can be rerun to ensure that the fault is completely cleared.

2.06 Recovery from nonduplicated faults is dependent upon the fault location and type. In general, the fault is recorded in the known fault list and an alarm is given. A TTY message is printed to notify personnel of the area containing the existing fault.

REQUESTING PERIPHERAL UNIT DIAGNOSTICS

2.07 Peripheral controller diagnostics can be manually initiated via TTY input messages. The following message initiates diagnostic tests for the FIOC:

DGN:FIOC cs!

This input message initiates FIOC diagnostic tests that halt on the first detected failure. The variable **c** is used to denote the control frame (0 or 1) on which the FIOC is located. The system control (0 or 1), associated with the FIOC to be diagnosed, is specified by **s**.

2.08 The diagnostic test action can be modified by varying the input message:

DGN:FIOC cs, PH p, TST t; action-option!

The additional variables are:

p—defines the phase requested for the step or repeat mode.

t—is the test requested for step or repeat mode. It is an optional parameter for step or repeat mode.

Action options are:

RPT—Executes the requested diagnostic phase repetitively. To stop the diagnostic, depress the EXECUTE

key. To restart, depress the EXECUTE key again.

STEP—Executes the requested diagnostic phase whenever the EXECUTE key is depressed.

UCL—Unconditionally executes the entire diagnostic. However, some failure printouts can be lost due to overflowing the TTY message queue.

DETL—Unconditionally executes the entire diagnostic and prints all failures. This option will dramatically slow down the completion of the diagnostic since each failure is printed before execution continues.

Note: **DETL** is a 3E3 generic only option.

2.09 The system will respond to peripheral unit diagnostic requests with one of the following:

IP—The diagnostic request has been accepted and is in progress.

RI—A diagnostic is in progress or another multiscan function is in progress. Repeat the request later.

NG—The FIOC is not currently in the correct state to be diagnosed.

For information regarding diagnostic request messages for other peripheral controllers, refer to the No. 3 ESS Input Message Manual, IM-3H300-01, under DGN headings.

2.10 Controllers can be returned to service via the REQ key located on the peripheral control unit power panel (Fig. 3). When the REQ key is depressed, diagnostic tests are run on each peripheral controller. The TTY will respond with a message stating that the controller diagnosed and all tests pass (**DGN SC 00 ATP**) or test failed (if any). This message will be followed by a message stating that the peripheral controller restoral is complete (**M RST SC 00 COMPL**).

START-SMALL TEST PHILOSOPHY

2.11 The No. 3 ESS peripheral unit diagnostic tests are designed to avoid using circuitry

in a test that has not been tested previously. This "start-small" technique requires that circuits and paths be tested and validated prior to using these circuits and paths to access or transmit data to other points.

2.12 A general example of this technique is depicted in Fig. 4. Circuit 1 will be tested first. When it is proved to be operative, another test will be initiated to test circuit 2. Circuit 1 can now be utilized in the second test since it is known to be good. This accumulation of known good circuitry can progress until a fault is detected. When a test fails, the fault is isolated to that portion of the equipment being exercised by the failing test. This test method minimizes the possibility of erroneous fault locating.

2.13 This philosophy is applied to each individual peripheral controller and to the total diagnostic test if it is run completely; ie, the FIOC will be tested prior to tests of the other peripheral controllers. If individual peripheral controller tests are requested (via the DGN message), the FIOC must interface with the other controllers and must be functioning correctly. Diagnostic tests executed by the restore request (**RST:SC cs**) automatically will test the FIOC prior to diagnosing the referenced controller.

TABLE-DRIVEN PROGRAM STRUCTURE

2.14 Most No. 3 ESS peripheral unit diagnostics are table-driven programs. A table-driven program consists of three elements:

- (a) Data tables
- (b) Control program
- (c) Interpretive routines.

The relationship of the three elements is shown in Fig. 1. The control program (DCON) determines which data table is to be accessed to provide execution of the required diagnostic. When a data table entry is selected (controller diagnostic test), the 5-bit OP code denotes the interpretive routine (of a possible 32) required to interpret the data table entry and to execute the necessary machine operations. Upon completion of the task, the control program selects the next data table entry to be accessed and continues the sequence to completion.

2.15 Major advantages realized by using the table-driven program approach are:

- (a) A higher level program language is made available for generating the test code.
- (b) Once the diagnostic tests are generated, they can be used both for field testing and factory testing. An interpretive program equivalent to DCON was written for factory testing.

PAGING DIAGNOSTIC PROGRAMS INTO MEMORY

2.16 Peripheral unit diagnostic programs are not resident in the main store of the control unit as used in the No. 3 ESS. The diagnostic tests are stored on magnetic tape in order to conserve memory. When diagnostics are to be used, they are brought into main memory from the tape cartridge. A segment of main memory, known as the paging buffer, is reserved to accommodate programs that must be brought in from tape and that are not required on a high-usage basis.

2.17 When peripheral unit diagnostic tests are requested, program DCON, program DCNSUB, and phase 0 of the diagnostic test are loaded into the paging buffer (except the TDC diagnostic) for the duration of the peripheral unit diagnostic testing. The diagnostic tests, phases 1 through n (data tables), are brought in, one phase at a time, and stored (until executed) in that portion of the paging buffer reserved for diagnostic tests (Fig. 5). The size of the diagnostic test phase is limited by the area reserved within the paging buffer. This requirement ensures that the cartridge tape drive will not be exposed to excessive wear when a test phase is run in the repeat mode. If the program to be run exceeds the allowable memory size, portions must be read in separately from tape each time the test phase is executed.

3. PERIPHERAL UNIT DIAGNOSTIC TEST DESCRIPTIONS

FRAME INPUT/OUTPUT CONTROLLER

3.01 The FIOC is primarily an interface between the 3A CC and the other controllers. The FIOC receives serial data from the 3A CC on one of four subchannels (Fig. 6). The bipolar pulses are loaded into the 21-bit shift register until the first "1" is detected in the leading slot. When

this occurs, control steps to the next state (transfer) where the start code and parities are checked and data is loaded into the 19-bit latch register. After all functions are performed, the sequence controller advances into one of the four go states depending on which subchannel was used by the 3A CC to communicate with the FIOC. Subchannels 0 and 3 of the FIOC are used to communicate with the scanner controller (Fig. 2), while subchannel 1 of the FIOC enables the PPD and subchannel 2 of the FIOC communicates with the network controller.

3.02 The selected controller is then enabled to allow a reply, and data is gated in from the peripheral controller. When the ready signal is received, the FIOC steps to the next state, loads in parities, and then pulses the information back to the 3A CC. The control remains in this state until arrival of the next message. When the first pulse arrives, the control steps to the receive state if the shift register contains all zeros. If the shift register does not contain all zeros, the control is locked in the purge state where data is absorbed into the shift register, but control does not advance to another state during the cycle.

3.03 A special message, which is designed primarily to check the FIOC hardware, is provided. This message must be routed through subchannel 0 with good parities and the maintenance start code (first three bits, 101). Bits 12 through 15 must also be all ones. This is a maintenance order and allows the first five bits of the data to be used to control the 5-bit state register. The FIOC check word and sequence controller states are shown in Fig. 7. If the five low-order bits carry the message "00100," the FIOC control will enable the gating of the status of the mate FIOC, reset the mate FIOC, and return the information back to the 3A CC. If the five bits carry "00010," then the FIOC control resets the mate control and echoes the information received. If the message is "11110," the FIOC only echoes the information.

3.04 For normal controller communication, the FIOC gates in information from the controller and generates the parities and start code in accordance with the ASW bit. The echo order returns the mirror image of the received information. On the read status order, the status of the mate FIOC is returned to the 3A CC in the following format.

- Bits 0 through 4 indicate the contents of the state register.
- Bit 5, if zero, indicates that the upper half of the shift register is cleared.
- Bit 6, if zero, indicates that the lower half of the shift register is cleared.
- Bit 7 indicates a normal start and good parity or a maintenance start.
- Bit 8 is the lower half parity check bit of the data register (zero if correct parity).
- Bits 9 and 10 represent the contents of the least significant bit and most significant bit contained in the lower half of the shift register.
- Bit 11 is the upper half parity check bit of the data register (zero if correct parity).
- Bits 12 and 13 represent the contents of the least significant bit and most significant bit contained in the upper half of the shift register.
- Bits 14 and 15 are dummy 11 bits.

These normal and maintenance orders are used when the tests listed in paragraphs 3.05 through 3.21 are executed to determine the integrity of the FIOC.

3.05 *Homing Sequence:* (Phase 1 Test 0)

Resetting the FIOC to be diagnosed is attempted by issuing two maintenance orders with the five lower bits, "00100," through the mate FIOC. This should read the state of the FIOC and reset it. The returned data is masked since it is only desired to reset the FIOC. The sequence state registers should be in the transmit state (11111) since the data was transmitted (Fig. 7). Two subchannel echo orders are then initiated. These orders should also leave the FIOC in the reset state. An FIOC read state order is then issued to ascertain that the state registers are "11111" and that bit 7 is a one, which is the normal FIOC state between messages.

3.06 *Parity Check:* (Phase 1 Test 1) Parity checks are verified by a series of messages to the FIOC. The data is varied in half of the

message while the other half is held constant, and then the sequence is reversed. After each message, the state of the FIOC is checked for normal state via the mate FIOC.

3.07 Subchannel Verification: (Phase 1 Test 2) Subchannels 1 through 3 are verified by sending all zeros in turn to the PPD, network controller (NWC), and scanner controller (SC). The FIOC routes the information to each controller and depends on the ready signal from the controller to progress to the next state. The state of the FIOC is checked after each peripheral unit message is completed.

3.08 Reset Mechanism: (Phase 1 Test 3) The state register of the local FIOC is jammed to an illegal state (00111) using the FIOC maintenance order. The state of the FIOC is then read through the mate unit, which should also reset the register. A check is then made to ensure that the state register is reset. The recovery of the FIOC is initiated by inserting all zeros with the shift and data registers. The recovery action is then validated via the mate FIOC read message. The reset mechanism sequence is initiated again with the illegal state code 11101. These tests complete phase 1 of the FIOC diagnostics.

3.09 Illegal State Exercise: (Phase 2 Test 1) The homing sequence test is rerun at the beginning of phase 2 FIOC tests to ensure that the FIOC is in the normal state. Various illegal states are loaded into the state register using the special FIOC message. These states should cause the FIOC to stick. The FIOC status is checked for expected results, and then recovery action is initiated and confirmed.

3.10 Subchannel Activity Recorder: (Phase 2 Test 2) The FIOC order is used to set the state register into the regular dispatch go modes for subchannels 1, 2, and 3. The difference between the incoming subchannel (0) and the responding controller (1, 2, or 3) will cause the FIOC to stick. The expected results are determined through the mate FIOC.

3.11 Transfer and Receive Modes Exercise: (Phase 2 Test 3) The FIOC order is used to set the state register to the transfer state (10001) and then to the receive state (10000). The state register is verified in each case via the mate FIOC.

3.12 Looping: (Phase 2 Test 4) The state register is jammed first to the reply state (11110) and then to the readout state (00010) (Fig. 7) using the FIOC order. From these states, the FIOC should return the mirror image of the order. A check is made to determine that the FIOC is in the normal state after completion of each order. The looping test completes phase 2 of the FIOC diagnostic.

3.13 Reverse Read: (Phase 3 Test 1) As in other FIOC diagnostic phases, the homing sequence is executed to place the FIOC in the normal state. The reverse read test is then executed to determine the integrity of the FIOC to FIOC bus. The mate FIOC is jammed to various states, and the results are read through the local FIOC to verify correct operation of the FIOC to FIOC bus.

3.14 Unusual Sequences: (Phase 3 Test 2) The FIOC order is used to set the state register to the purge state (00000). This should leave the FIOC stuck at the illegal state (00001). The FIOC is then recovered from this state. The FIOC order is then used to set the state register to "01110." This should generate a normal scanner communication order, and the FIOC should return to the normal state after completion of the order.

3.15 Reset: (Phase 3 Tests 3 and 4) Two tests are executed to verify reset techniques. First, the state register is jammed to "00111." The FIOC is then reset by sending all zeros through the local FIOC and reading the status via the mate. The state register is then jammed to "11111." An RDOU0 order is then sent from the local controller and should reset the state register.

3.16 All-Zeros Checker: (Phase 3 Test 5) The FIOC contains all-zeros checkers, one that detects all zeros in the lower half of the shift register and one that detects all zeros in the upper half. When all zeros are detected (in either half), the state register is set to the receive state. Data is transferred to check the lower half zeros checker. The upper maintenance order must contain "1111" in the most significant bit positions.

3.17 Reset of Data Register: (Phase 3 Test 6) The data register is filled with all ones at the start of the test. Two data patterns are used to ensure that all data register bits can be reset to zero. Two data patterns are required

since the odd parity does not allow an all-zeros pattern.

3.18 Parity Loading: (Phase 3 Test 7) The mate FIOC is jammed to an illegal state. The local FIOC is then used to read the status of the mate. The status was set up to cause the parity bits to be inverted in the return message, thus checking the gating of the parity bit.

3.19 Data Register: (Phase 3 Test 8) The four upper leads of the data register are checked for a stuck-at-one condition. These bits denote the FIOC maintenance order. Each bit, in turn, is set to zero in an order. If the set-to-zero bit is stuck at one in the data buffer, the order is erroneously detected as an FIOC maintenance order.

3.20 FIOC Order Recognition: (Phase 3 Test 9) An FIOC order is sent through subchannel 3. A check is then made through the mate FIOC to ascertain that the order was not recognized as a maintenance order (maintenance orders are only valid in subchannel 0).

3.21 +3 Volt Power Alarm Test: (Phase 4 Test 1) A test unrelated to FIOC operation is now executed to ensure proper operation of the +3 volt power alarm test circuits. The associated power alarm scan points (in master scanner) are examined to ensure that they are in the normal state. Prior to issuing a PPD order to operate a power alarm test (PAT) relay, the ignore bits are set for all affected alarm ferros. This prevents generation of a real power alarm. The associated relay is then operated, and the associated ferrod is checked for saturation. The test is then cleared and checked for return to normal.

NETWORK CONTROLLER

3.22 The primary function of the No. 3 ESS network controller is to operate or release crosspoints in the network fabric. The controller must be able to select and enable one of nearly a million pulse paths through the first/second stage, third stage, or dummy load. The selection is determined by information in two 16-bit words received from the FIOC, with the exception of one dummy load path which is determined by a previous network order. A major function block diagram of network control is shown in Fig. 8.

3.23 The intent of the network controller diagnostic is to determine, as far as possible, if any of nearly a million possible, normal, or auxiliary orders will fail to execute. Due to obvious limits, all of the combinations cannot be included within the diagnostic test. Rather, the diagnostic test checks each component (level, switch, etc) by issuing at least one network order which requires that component to function properly. Functions, such as level selection, switch selection, etc, are tested by selecting each distinct level, switch, etc, at least once during the diagnostic test.

3.24 The network controller diagnostic test must be run on the off-line controller, as is the case with all controller diagnostics, in order not to interfere with call processing. To ensure no interference with call processing, the diagnostic is not allowed to operate or release any crosspoints. The off-line pulser is either dummy loaded or inhibited, or both, during the entire diagnostic sequence to implement this constraint (with the exception of one test in phase 5). The network controller diagnostic is divided into five phases. Each test contained within the five phases is described in the following paragraphs.

3.25 Initialization: (Phase 1 Test 0) The network controller is initialized to a known starting state by clearing the registers on the control logic and register (CLR) circuit pack. The dummy load and pulser inhibit flip-flops are set for protection against firing into the fabric. The power flip-flops are then set to enable the network controllers on both sides.

3.26 Power Enable Test: (Phase 1 Test 1) The two power flip-flops are inverted from the state set in initialization. This should leave both sides disabled. A check is made to ensure that the power enable load registers (LWEN1 and LWEN2) did not load erroneously. The off-line flip-flops are returned to their former state and the controller is cleared.

3.27 Maintenance Order Test: (Phase 1 Test 2) First, all maintenance flip-flops are cleared. A maintenance interrogation is then performed by sending an unused OP code, which verifies that no maintenance flip-flop sets when its OP code is not set. Three maintenance set orders are sent in sequence and examined for

correct operation of the associated flip-flop. The maintenance set orders are:

- (a) Dummy load
- (b) Group check bypass
- (c) Pulser inhibit.

3.28 OP Code Decoder Test: (Phase 1 Test 3) Six normal OP codes are sent in turn to the network controller. Only word 1 of each order is sent to ensure that no order execution will be attempted. Each order is followed by an interrogation with bits 2 through 7 of the response indicating the order received. The six normal OP codes are:

- (a) A—Close first and second stage
- (b) FCG—False cross and ground
- (c) HD—High and dry
- (d) RLS2—Open first and second stage
- (e) O3—Close third stage
- (f) R3—Open third stage.

3.29 Clear Pulser Inhibit Flip-Flop and Zero-Out-of-N Check: (Phase 1 Test 4)

When the maintenance order test is complete, the maintenance flip-flops are left in a nonnormal state. In preparation for further tests, the maintenance flip-flops are cleared and only the dummy load is set as confirmed by bit 2 of the reply. A 0/N is produced on group checks 1 through 7 simultaneously by sending a stage III operate order having illegal parity over bits 8 through 10 of word 1. This causes the system-generated, half-word parity to be inconsistent with the parity of bits 11 through 15, the OP code, and the steering bits. As a result, the OP code decoder produces no output and no group check decoding is done. This ensures that the seven detectors detect 0/N current.

3.30 Group Check 1, 2/N Check: (Phase 1 Test 6) A flip-flop in the input level and miscellaneous decoder circuit pack is set via a maintenance order to force stage III circuit level 0 on. Then a stage III operate order is sent that selects level 1, causing a 2/N on group check 1.

The remaining group checks should report normal 1/N conditions.

3.31 Group Check 2, 2/N Test: (Phase 1 Test 7) A flip-flop in the level decoder circuit pack is set via bit 7 of a maintenance order to force the stage III wire level 0 on. Then an operate order selecting level 1 is sent, which causes a 2/N on group check 2. Group check 1 should report a normal 1/N condition.

3.32 Group Check 3, 2/N Test: (Phase 1 Test 8) A maintenance flip-flop is set by bit 11 of a maintenance order to force the stage III switch 0 on. This is followed by an operate order, which addresses switch 1 and causes a 2/N on group check 3.

3.33 Group Checks 5 and 6, 2/N Test: (Phase 1 Test 9) A maintenance flip-flop on the level decoder circuit pack is set via bit 5 of a maintenance order to force the stage III group 0 on. An operate order addressing group 1 is sent, which causes a 2/N on group check 5. Since wire level and switch selection are also based on the same node lead, group checks 2 and 3 fail simultaneously. The maintenance order used in this test also sets a flip-flop, which forces high and dry input group A0 on. This draws another unit of current from source 6, causing group check 6 to fail also.

3.34 Group Check 7, 2/N Test: (Phase 1 Test 10) A maintenance flip-flop is set via bit 4 of a maintenance order, which forces the negative stage III group 0 on. An operate order addressing group 1 is sent, which causes a 2/N on group check 7. Since circuit level selection is based on nodes generated from the negative group selection, group check 1 fails also.

3.35 Group Check Bypass/Pulser Check: (Phase 1 Test 11) The dummy load and group check bypass maintenance flip-flops are set. A maintenance order forcing circuit level 0 is then sent. Following this is an operate order addressing level 1. Group check 1 should fail on 2/N; but because the bypass flip-flop is set, the pulser should fire into the dummy load. The interrogation without clear capability is verified on this test by sending two interrogative orders, the first without clearing (maintenance start code), and by looking for the same response on the second interrogation, except for bit 7 which is the clear indicator bit.

The maintenance flip-flops are then returned to their normal state in preparation for a possible looping of tests over this phase.

3.36 Power Down: (Phase 1 Test 12) The power enable flip-flop is inverted to disable the off-line network controller. All flip-flops are cleared. This completes phase 1 of the network controller diagnostic.

3.37 Stage III Access Tests: Phase 2 accesses each third-stage switch and each possible circuit and wire level for some switch in each half of each equipped switch group. The first test is an initialization, which is similar to the first test of phase 1 except that the pulser is not inhibited but is allowed to fire into the dummy load. Using a nested DOLOOP, selected operate and release orders are executed for stage III crosspoint selection. Figure 9 shows the No. 3 ESS stage III path selection.

3.38 The 4-digit test numbers in this phase are divided into three decimal fields. The most significant digit indicates the switch group (0 through 3) being accessed. The middle two digits indicate the switch number (00 through 15), and the least significant digit indicates the order, operate (1) or release (2). The levels selected are the same as the three low bits of the switch number for the operate order and the ones complement of the three low bits of the switch number for the release order.

3.39 Test number assignments for this phase access third-stage crosspoints in the following pattern for switch group 0.

TESTS	SWITCH	OPERATE LEVEL	RELEASE LEVEL
0001-0002	0	0	7
0011-0012	1	1	6
0021-0022	2	2	5
0031-0032	3	3	4
0041-0042	4	4	3
0051-0052	5	5	2
0061-0062	6	6	1
0071-0072	7	7	0

Tests 0081 through 0152 are assigned similarly for switches 8 through 15 of switch group 0. Tests 1001 through 1152 are assigned similarly for switch group 1. Tests 2001 through 2152 are assigned similarly for switch group 2. Tests 3001 through 3152 are assigned similarly for switch group 3.

3.40 The third-stage access test sequence of phase 2 issues an operate order to each crosspoint on the diagonal from level 0,0 to level 7,7 for every switch in an equipped group. The release orders are issued to crosspoints on the opposite switch diagonal. All order responses are verified, and no crosspoints are operated or released since the pulser is fired into the dummy load. Upon completion of the stage III access test, the power-down sequence is run to provide possible looping of phase 2 tests. This power-down sequence is identical to the power-down sequence at the end of phase 1.

3.41 Stages I and II Access Tests: Phase 3 of the network diagnostics accesses each equipped concentrator group, as determined from office data. The phase is in the form of a DOLOOP over all eight possible groups (maximum network frames per network controller) with the unequipped positions being skipped. Unlike previous phases, initialization and power turn-down routines are executed inside the loop, once for each equipped concentrator group.

3.42 The loop begins with high and dry orders since output levels or output switches are not involved. Next, false cross and ground and release orders are used to test output switch and level selection and no-test switch operation. Finally, A-link orders are used to access every input and output switch in the concentrator group.

3.43 A 4-digit coded test number is also used in this phase. The most significant digit indicates the concentrator group position (relative to the control frame being tested) being accessed. The tests applied to each concentrator group are identical, so only the three low digits will be used in the following test descriptions. An X will be used in the most significant position to indicate that a maximum of eight tests actually exist. Figure 10 represents a No. 3 ESS concentrator group and will be useful in understanding the following test description.

3.44 The *high and dry order* is performed for each level (0 through 7) of switch 0 of

each input group (A, B, and C) including operation and release of the cutoff. The hundreds digit of the test number specifies the group (A = 1; B = 2; C = 3). The tens digit specifies the level to be accessed (0 through 7), and the units digit specifies a cutoff state (0 for release; 1 for operate). For input switch group A, the test assignment is:

```
TESTS X100—X101: LEVEL 0,
                  RELEASE & OPERATE
TESTS X110—X111: LEVEL 1,
                  RELEASE & OPERATE
:
:
TESTS X170—X171: LEVEL 7,
                  RELEASE & OPERATE
```

Tests X200 through X271 and X300 through X371 are assigned similarly for groups B and C, respectively.

3.45 The preliminary false cross and group (FCG) test is performed for input switch 0 in each switch group (A, B, and C), using output switch 0 and output level 0 with no-test released. Test numbers are X180, X280, and X380 for input switch groups A, B, and C, respectively.

3.46 The false cross and ground (FCG) order is performed for switch 0 of each output group (A or B) for every level on the switch (0 through 7), including operation and release of the no-test. Switch 0 of input group A is used in every order to avoid using untested input circuitry. The hundreds digit of the test number specifies the output group being accessed (A = 4; B = 5). The tens digit indicates the output level (0 through 7) of switch 0 of the group being accessed, and the units digit indicates the state of the no-test (0 for released; 1 for operated). For output group A, the test number assignment is:

```
TESTS X400—X401: LEVEL 0,
                  RELEASE & OPERATE
TESTS X410—X411: LEVEL 1,
                  RELEASE & OPERATE
:
:
TESTS X470—X471: LEVEL 7,
                  RELEASE & OPERATE
```

Test numbers X500 through X571 are assigned similarly for the output group B tests.

3.47 The stage II release order test executes during the same DOLOOP that is used for the FCG test. The release order is also performed on the same output switch (0) for groups A and B and uses the same input switch (switch 0 of group A) as in the previous test. Test number assignments are X480 and X580 for output switch groups A and B, respectively.

3.48 The A-link test is also implemented by a DOLOOP statement, which simplifies the sequencing of repetitive tests through different equipment paths. To test input and output switch selection, A-link orders are sent involving every stage I and stage II switch. Each input switch (00 through 07 or 08 through 15) in each switch group (A through C) is paired with the corresponding output switch (00 through 07) in each concentrator. Each output switch is therefore accessed three times. Input and output level 0, with no-test and cutoff released, is used in all orders.

3.49 The hundreds digit of the test number specifies the input group being accessed (A = 6; B = 7; C = 8). The two low-order bits indicate the input switch (00 through 15) within the selected switch group. The output switch number selected is congruent to the input switch number, modulo 8. For group A, the test assignment numbers are:

```
TESTS X600—X607: INPUT SWITCH 0-7,
                  OUTPUT SWITCH 0-7,
                  CONCENTRATOR 0
```

```
TESTS X608—X615: INPUT SWITCH 8-15,
                  OUTPUT SWITCH 0-7,
                  CONCENTRATOR 0
```

Tests X700 through X715 and X800 through X815 are assigned similarly for input switch groups B and C, respectively. Test X900 is the power-down sequence and completes phase 3 of the network diagnostics.

3.50 Maintenance Flip-Flops: Some of the maintenance flip-flops on the 1A logic packs are used in phase 1 to force 2/N conditions on certain fields. The maintenance flip-flops used are related to third-stage orders since they can be executed without regard to the number of equipped concentrator groups. Phase 4 tests the remaining maintenance flip-flops related to concentrator group orders. The 2/N conditions are forced by first

setting the maintenance flip-flop and then executing the related concentrator order. All remaining maintenance flip-flops can be tested by accessing the first concentrator group or concentrator group 4, if equipped. Thus, test assignment numbers are 0001 through 4014. Initialization and power down are performed as in phase 3.

3.51 Phase 5: One bit in the response to every normal order is designated as the POK bit. This bit indicates whether the pulser current reached the desired 4-amp peak. Under dummy load, 4 amps is never reached, so faults in that lead cannot be detected. Also, a number of potential faults in the group selection access circuitry cannot be detected under dummy load. Therefore, phase 5 clears the dummy load flip-flop and issues high and dry orders with cutoff released to the lowest terminal equipment number (TEN) accessible from the control frame under test. For this purpose, TEN 1-0-0-0-0 is reserved on frame 0 and TEN 8-0-0-0-0 is reserved on frame 1. These terminals should not be assigned for normal office use. The two possible test numbers are 0001 and 1001. Initialization and power down are performed as in phase 3.

PERIPHERAL PULSE DISTRIBUTOR

3.52 The peripheral pulse distributor (PPD) performs the relay control function of the No. 3 ESS. In this application, the PPD receives information from the FIOC and passes either a one or a zero to the addressed peripheral decoder (PD). Seven such bits constitute a complete PD order, resulting in control of up to three relays, designated as a triplet. Four triplets are controlled by each PD as shown in Fig. 11. Two bits of the PD order make the one-of-four triplet selection. The three remaining bits control the operation or release for each of the three relays in the selected triplet. The first and last bits of the PD order are always ones and are used in control of the PD gating, etc.

3.53 The PD to be addressed is selected via a 16 by 16 transformer matrix. The data format for PPD control is shown in Fig. 12. Four bits are used for horizontal selection and four bits select the vertical. The polarity bit selects the transformer half to be pulsed, which determines whether a one or a zero is sent to the PD. The PDs do not provide a reply message to the PPD and cannot be checked without going through the

peripheral circuits. The PPD diagnostics verify only the PDD circuits and some FIOC circuits that cannot be completely checked during FIOC diagnostics. The individual PD circuits are checked during their respective diagnostics.

3.54 The structure of the PPD is shown in Fig. 13. Each physical unit is verified by one or more of the tests described in paragraphs 3.56 through 3.68. The PPD diagnostic tests are ordered in the following sequence:

- (1) Initialization
- (2) Power flip-flop
- (3) Reply register
- (4) State register
- (5) Current detectors
- (6) Vertical drivers
- (7) Horizontal drivers
- (8) Blocking diodes
- (9) Transformer paths
- (10) PPD-PD linkages.

Items (1) through (9) are executed during phase 1 of the PPD diagnostic tests, while (10) is executed during phase 2.

3.55 The following system requirements must be fulfilled in order for the PPD diagnostic test to execute.

- (a) All three vertical driver boards must be equipped.
- (b) Both horizontal driver boards must be equipped.
- (c) The transformer board (FC206) is an optional item, but the boards on verticals 1 and 15 must be equipped.
- (d) A 32-word PPD map is maintained by administrative software to show each transformer in the PPD outputting matrix that

is terminated by a PD board. During testing, any unterminated transformers will be skipped.

3.56 Initialization and Power Flip-Flop

Verification: Phase 1 of the PPD diagnostic test begins by initializing the power flip-flop with a power-off order. The status is checked by the intermediate level current detector. A power-on order is then issued. The power-on status is then checked by the intermediate level current detector.

3.57 Power Flip-Flop Gating Control: After the power flip-flop is turned off, a PPD power turn-on order is sent to the scanner through the same FIOC. Since the FIOC data register is shared by all controllers, a failure of the PPD gating control causes the power to be turned on. The current detector should indicate this failure. The power-on status is checked in a similar manner.

3.58 PPD Reset Mechanism: This test verifies the reset mechanism by setting each bit in the reply data register at least one time. The immediate reply order is used to determine that the flip-flops were reset properly.

3.59 Control Board Miscellaneous Check:

The state register is checked by forcing the controller to go through a complete cycle. The bits in the reply register are also checked by setting them at various operations. Current detectors are verified during the same process.

3.60 Vertical Driver Check: This test allows only the false vertical path to be on. The faults that cause any other vertical driver to be stuck high will be detected here.

3.61 Horizontal Drivers: Test 5 of phase 1 uses the false vertical and the current detectors to verify all the horizontal drivers. A blocked horizontal driver or an erroneous translation causes the current detector to fail.

3.62 Diode Check: This is test 6 of phase 1, the last test is phase 1. The threshold current detectors are used to check for shorted diodes. The presence of a shorted diode changes the expected current level, and a higher current level is detected by the next current level detector.

3.63 Vertical Drivers and Pull-Down Paths:

Tests 1 through 32 of phase 2 enable both the vertical driver and pull-down path and repeat

the operation for all the verticals. All driver, pull-down transistor, and translation failures will be detected.

3.64 Pulsing Path Verification (Polarity 0): Tests 1000 through 2515 of phase 2 verify all the polarity 0 pulse paths. The marginal current level pulse is used for all tests.

3.65 Pulsing Path Verification (Polarity 1): Tests 3000 through 4515 of phase 2 are used to verify all the polarity 1 pulse paths with a marginal current level. After each operation, seven zeros are passed to the addressed PD to clear its shift register.

3.66 Miscellaneous: Test 33 of phase 2 verifies that the horizontal parity bit can be set properly. A check is also made for a possible open M2 bit lead by forcing the controller to go through a complete cycle without firing a pulse into the transformer matrix.

3.67 PPD-PD Linkage Check (Polarity 0):

A normal level current is pulsed in turn through each polarity 0 transformer path. An open secondary fault will result in a high impedance. The current level detector is relied upon to indicate such a failure. Tests 1 through 16 execute these checks.

3.68 PPD-PD Linkage Check (Polarity 1):

Tests 17 through 32 verify all the PPD-PD polarity 1 linkages. The tests are identical to tests 1 through 16 with the addition of seven zeros being sent for PD shift register clear. Phase 2 of the PPD test is then completed by the same clean-up routine as utilized in phase 1.

RINGING AND TONE PLANT

3.69 The 881A ringing and tone plant in the No. 3 ESS provides continuous ringing, interrupted ringing, continuous call-progress tones, interrupted call-progress tones, and signaling interruption loops. The ringing and tone plant diagnostic test consists primarily of scanner orders to monitor the 25 master scan points dedicated to the ringing and tone plant and PPD orders to control the associated PD points. The scan points and distribute points associated with the ringing and tone plant are shown in Tables B and C. Two additional scan points are utilized to monitor the transfer of tone outputs from one side of the plant to the other, and six

points are used to monitor the +48 volt supply to the plant.

3.70 The ringing and tone plant diagnostic program (RTPT) consists of three phases. Phase 0 is used strictly to define the distribute points used by RTPT. Phases 1 and 2 each test one side of the duplicated ringing and tone plant (sides 0 and 1). The phases also test the nonduplicated receiver off-hook (ROH) generator, the distribution fuses, the bus transfer of tones into the network, and the +48 volt converter associated with the side being tested. The final test of each phase is utilized to test the +24 volt power alarm circuit even though it is not associated with the ringing and tone plant. The diagnostic request determines which phase (1 or 2) will execute. Each phase consists of an initialization, 15 tests, and a clean-up routine.

3.71 Fuse Test: The fuses associated with side 0 are checked by scanning the respective scan point.

3.72 Low Voltage Monitor and ROH

Generator Check: The low voltage monitor check circuits are verified for side 0 by operating the marginal check (MC) 0 relay and by releasing the MC1 relay. With the MC relay operated, simulated faults are generated at the monitor check circuit inputs. The following scan points are then checked to ensure correct operation of the monitor check circuits:

- (a) TOUCH-TONE® low voltage side 0
- (b) Call waiting low voltage side 0
- (c) Audible ring low voltage side 0
- (d) High tone low voltage side 0
- (e) Busy tone low voltage side 0
- (f) No voltage ROH generator.

The MC relays are restored at the end of the test.

3.73 Interrupter Check: For side 0, the 10 impulse per minute (IPM), 60-IPM, and 120-IPM interrupters are checked to see whether they can be operated. Each interrupter is then checked to determine if it will release and if it can be operated again. Verification of correct

operation is performed via the defective interrupter relay, side 0 scan point.

3.74 Output Transformer Ground Path

Checks: A ground detection monitor is provided in the ringing and tone plant and will initiate an alarm at the ground on tone output scan point if a load of 5000 ohms or less appears at any of the tone outputs. By operating combinations of distribute points GDT 1, GDT 2, and GDT 3, a ground of less than 5000 ohms is placed on the following tone outputs:

- (a) AR (10)
- (b) BT (120)
- (c) BT
- (d) ROH
- (e) HT
- (f) MT
- (g) TT.

Ground detection is verified via scan point GDO. The MC relays, RT relays, GDT tree, and interrupters are restored at the end of the test.

3.75 Ground Check Between the RTO Relay and the GDO Relay:

The GDO scan point is checked to determine if a ground exists throughout the plant.

3.76 Ground Test Between the Terminal Block and the GDO Relay:

Side 0 is activated using the RT relays. The GDO scan point is then checked to determine if a ground is present. Side 1 is reactivated at the end of test.

3.77 Emergency Manual Line Transfer

Test: The emergency manual line is tested via the no-voltage-on ringing output bus. The emergency manual line normally is not transferred.

3.78 Low Voltage Checks on Tones:

The low voltage checks are made by scanning the appropriate scan points with the MC relay in the normal state. This determines if the following tones have dropped 3 db below normal:

- (a) High tone

- (b) Low tone
- (c) Call waiting
- (d) TOUCH-TONE
- (e) Audible ring.

3.79 Receiver Off-Hook Generator Test: The ROH generator is tested via a dedicated scan point.

3.80 Overload Announcement Test: The overload announcement relay is checked to see if it can go through the transition of off to on to off again. The transitions are verified via the overload on BT (60 IPM) output scan point.

3.81 Ringing Distribution Fuse Alarm Test: The blown ringing fuse scan point is checked to determine if any ringing distribution fuses are blown.

3.82 Inverter 0 Test: This test first checks the inverter on side 1 using the no-voltage-on 20-Hz inverter, side 1 scan point. If this test fails, inverter 0 should not be checked because, if inverter 1 has lost its 105-volt line, the inverter 0 scan point (no-voltage-on 2-Hz inverter, side 0) will indicate a failure. If inverter 1 is found to be operational, the inverter 0 monitor is checked by using the MC relays and by scanning the associated scan point. The MC relays are then restored and inverter 0 is checked.

3.83 Bus Transfer Test: This test checks for proper operation of the bus transfer of tones to the network. The tones are transferred from side 1 to side 0 and back to side 1 using the RT relays. After each transfer, the bus transfer relays are checked via the BTA 0 and BTA 1 scan points.

3.84 Superimposed Ringing Test: The +48 volt converter is tested to determine whether it is manually off (using scan point P48OFO), has a fuse alarm (scan point P48FAO), or is a converter failure (scan point P48PAO).

3.85 +24 Volt Power Alarm Test: A test, unrelated to the ringing and tone plant operation, is now executed to ensure correct operation of the +24 volt power alarm circuit. The associated power alarm scan point is examined to determine

that the +24 volt converter is normal. A PAT order is then issued to ensure that a real power alarm is not generated. The alarm circuit is checked for a valid operation and then cleared and rechecked for normal operation. A clear routine is then executed to return the ringing and tone plant to a known state.

3.86 Ringing and Tone Plant, Phase 2:

Phase 2 of the ringing and tone plant diagnostic test is similar to phase 1 except that side 1 of the plant is diagnosed. The only variation in the test is the inverter test. The other side does not have to be verified prior to testing inverter 1 as is the case in the side 0 inverter test.

SCANNER CONTROLLER

3.87 The scanner performs the status observation function in the No. 3 ESS. The scanner consists of two main sections: (1) current-sensing ferrods that are wired to the observation points and (2) the SC that provides selection information necessary to interrogate the ferrod rows. The scan message is originated by the central control and routed through the FIOC via either subchannel 0 or 3 (Fig. 2) to the SC. The SC deciphers the message, makes a parity check on the address information, and interrogates the addressed row of ferrods.

3.88 The interface between the scanner controller and ferrod matrix is shown in Fig. 14. The redundant scanner controllers (SC00 and SC01) are capable of accessing eight 16 by 32 ferrod matrices. When office growth requires additional scanners, a second control frame is added to provide scanner controllers 10 and 11, which access scanners 08 through 15. The scanner controller diagnostic test requires that the office data area contain the number of the highest equipped logical scanner.

3.89 A scanner row is interrogated by enabling the appropriate transformer in the 16 by 16 interrogative transformer matrix (corresponding sensing detectors are also enabled). A bipolar pulse is then applied to the interrogative winding, which passes through 16 ferrods. The negative-half cycle of the bipolar pulse assures that the ferrite material is set to the maximum negative remanent state (if not in the saturated state). The positive-half cycle interrogates the ferrod. If the ferrod is not saturated (via the state coil), a pulse is coupled into the readout winding (indicating a

logical zero). If the ferrite material is saturated, no pulse will be present on the readout winding (indicating a logical one). The selected detectors collect the results of the interrogation and return a message to the central control (CC) via the FIOC. In addition to the 16-bit sensing reply, the reply message also includes an all-seems-well (ASW) bit. This bit determines whether a normal or a maintenance start code will be returned to the CC from the FIOC.

3.90 The scanner controller diagnostic test program (SCNT) consists of three phases. Phase 0 holds the variables and required office data information that will be loaded by the diagnostic control program prior to execution of the diagnostics. Phases 1 and 2 contain the scanner controller tests described in the following paragraphs.

3.91 Initialization and Power Flip-Flop

Verification: The first test of phase 1 initializes the power flip-flops to the diagnostic state on both the on-line and off-line sides. Power enable orders must be properly recognized to achieve this state. Power enabling logic is checked by the reply message. Gating control is checked by the reply of enable order POWER_BOT. Any detectors stuck low in bit groups 0 and 1 or 6 through 15 will be detected.

3.92 Power Registers: During this test, the power registers are set to various states and are verified. The coupling paths are checked fully during these tests. Upon completion, the power flip-flops are returned to the diagnostic state.

3.93 Order Decoder: The order decoder is exercised by issuing all the illegal orders. If these orders are correctly recognized to be illegal, the illegal pattern is echoed in bits 2 through 5. All the other bits in the reply message must be high, and the ASW bit must indicate a failure (high).

3.94 Subchannel 3 and Detectors: This test uses a power enabling order (POWER_TOP) to verify the current detectors in the subchannel group 3 (except for columns 2 through 5). The detectors for columns 2 through 5 in both subchannel groups are verified by normal orders addressing the reference point with inverted parities. A normal order opens the detector window at columns 2 through 5; however, the inverted parities inhibit

the scanner row selection. This allows the steady state status of the detectors at columns 2 through 5 of both subchannel groups to be observed.

3.95 Vertical Parity Check: A one in the steering bit inverts the parity bit and causes the parity checker to fail. This test verifies the checker against inverted parity by using all the vertical addresses. The first and second threshold current signals are checked by the ASW bit.

3.96 Horizontal Parity Check: The lower half-word parity bit is inverted by setting bits 2 and 3 of the sending message to 0 and 1, respectively. This test checks the horizontal parity checker by using all the horizontal addresses against the inverted parity. The scanner controller is now restored to the preferred state at the completion of phase 1 tests.

3.97 Timing Check: This test is the beginning of phase 2 of the scanner controller diagnostics. A regular pulse is fired through the addressed point. The threshold detector, which determines unit or no current (LE 1), should be turned low. This should detect an irregular timing sequence as well as faults that prevent the LE 1 detector from turning low.

3.98 LE 1 Detector: The ALT_VERT and ALT_HORIZ orders (test orders allowing zero or multiple selections) mask vertical or horizontal selections if vertical zero or horizontal zero is addressed, respectively. In this case, the LE 1 should remain high since no vertical or horizontal driver should be turned on. A zero reading from the LE 1 detector indicates a failure in one of the order decoders.

3.99 GR1 B Detector: The detector that detects multiple horizontal selections (GR1 B) is checked now. The ALT_HORIZ order is used to turn on two horizontal rows (including horizontal zero). The GR1 B detector should turn low indicating multiple selection.

3.100 GR1 A Detector: The multiple vertical selection detector (GR1 A) is checked. The ALT_VERT order is used to turn on two vertical columns (including column 0). The GR1 A detector should turn low indicating the multiple selection error.

3.101 Test Switch Failure Isolation: An all-zeros order with an odd vertical address is sent. The reply should be all ones. An all-zero reply indicates a test switch stuck low.

3.102 Current Detector: An all-zeros order forces the addressed current detector group to go low. If any bit in the reply remains high, it indicates that a current detector is stuck high or that the sensing path is open. If all bits remain high, the test switch on the test board is at fault.

3.103 Normal Order Recognition: Normal orders with correct parities are executed. The order decoder is verified by examination of the reply for expected results.

3.104 Power Cross Test: This test verifies the pulsing paths for possible shorts to power. In the scanner design, horizontal drivers serve as current sources, while vertical drivers serve as sinks. The current flowing through the matrix is sensed by the LE 1 detector at the sink side. Pulse path shorts to power are, therefore, detected by turning on the sink side but not the source. Here, the ASW order with inverted horizontal parity is used to achieve this purpose.

3.105 Pulsing Path Verification: These tests verify all the pulsing paths. If an interrogative path is open, it should introduce a high impedance into the pulsing path. These faults should be detected by the LE 1 detector.

3.106 Miscellaneous: If no power exists during the normal or ASW order, the no-power condition is flagged in bits 4 and 5 as well as the ASW bit. This feature is verified by turning down off-line controller power and then issuing an ASW order. If an ASW failure does not occur, the logic is not performing properly.

3.107 All-Zeros Blocking: For the all-zeros order, the interrogative signal is blocked by disabling the row translation. This feature is verified by issuing an all-zeros order with different row selections. If the reply does not contain a maintenance start code, the all-zeros blocking logic is faulty.

3.108 Order Isolation: Further orders are issued and the results examined to verify further features of the order decoder logic.

3.109 Power Order Gating: When the on-line scanner power is turned off and the off-line power is on, the A-bit in S2 is reset. An all-zeros order is issued to verify the action. At the successful completion of this test, the scanner controller is restored to the preferred state since the scanner controller diagnostic test is complete.

TAPE DATA CONTROLLER

3.110 The tape data controller (TDC) and minirecorder are used in the No. 3 ESS to provide memory backup and nonresident data required for system operation and maintenance. The tape data controller is depicted in Fig. 15.

3.111 The serial parallel interface (SPI) communicates serially with the 3A CC via an input/output subchannel. The SPI also establishes timing, control, and data signals over the parallel bus to the other TDC circuits.

3.112 The buffer provides two 1024-bit serial shift registers (BUF 0 and BUF 1) and associated counters and flags to temporarily store data being transferred between the 3A CC and tape cartridge. An intermediate transfer register (ITR) is provided to perform the parallel-to-serial conversion required to interface the shift registers with the common parallel bus.

3.113 The cartridge tape transport controller (CTTC) provides the interface with the minirecorder. The CTTC decodes commands from the 3A CC to initiate required sequencing of the control leads, providing proper tape motion, track selection, and data transfer between the read/write head and serial buffers.

3.114 The bus terminator (BT) provides the proper loading to electrically terminate the common parallel bus and serial buffer bus. It also generates the proper parity for status words originating from associated circuits and provides for maintenance checks on the common parallel bus.

3.115 As previously stated, the TDC diagnostic test program, unlike other peripheral unit diagnostics, is not written in the PUDAL 3 language. The TDC diagnostic program, CTAPM, contains its own TTY message handler and diagnostic monitor. There are six diagnostic tests for the TDC and minirecorder. Each test serves as a building block for the next; therefore, in order to ensure integrity

of the results, no test should be run without knowing that all previous tests have passed. The TDC and minirecorder diagnostic consists of the following sequence of tests:

- (1) SPI interface test
- (2) Buffer unit test
- (3) Cartridge tape transport controller test
- (4) Minirecorder read test
- (5) Minirecorder miscellaneous function test
- (6) Minirecorder write test.

All tests are written in common system code and are executed as described in the following paragraphs.

3.116 SPI Interface Test: A bad parity message is sent to the TDC. Bad serial parity should be detected by the SPI with a message returned indicating such. An SPI initialization order is sent to initialize the entire device. A check is then made to determine if the units were initialized and deselected.

3.117 An all-zeros order and then an all-ones order are sent to the BT. These orders should be *minimized* and returned intact. Sixteen orders that shift a one through a field of zeros are then sent and verified in sequence. These data patterns should also be returned intact. Successful execution verifies that data can be transferred through the STI to the ITR and to the BT and returned.

3.118 Buffer Unit Test: Test 2 checks the buffer unit of the TDC. An initialization order is first issued to set all states to a known level and deselect the tape unit to protect the tape cartridge. A check is made to verify that the buffers are in the idle state. A buffer order is then sent and verified to set the buffer in the load state, ready to receive data from the 3A CC.

3.119 The ability to correctly shift information through the 1024-bit shift registers is next tested. One register is half-filled with a checkerboard data pattern. The stuff order, which should shift the pattern to the upper half of the register, is then executed. The other buffer is then selected, and the complemented checkerboard pattern is used

to half-fill the register. The stuff order is executed for this register. The buffers are then unloaded and the received data patterns are verified.

3.120 The buffer ready (BR) flag, which denotes that a buffer is full and requires servicing, is now checked. An all-ones pattern is shifted into the first 32 words of each buffer. The buffer is switched on-line and the stuff order is executed. A check is made on the setting of the BR flag. Upon successful completion of this test, a clear order is executed to ensure that the BR flag can be reset.

3.121 Failure to service the two 1024-bit buffers in an adequate time should result in an overflow condition. Both buffers being full with more data coming off the tape unit causes the overflow bit to be set. This test simulates this condition by use of the fill order. The BR bit should become set at completion of the first buffer fill order, and the buffer overflow bit should become set after the second fill order. This occurs due to the BR bit remaining set after the first fill order. If this test completes successfully, a buffer initialization order is initiated to ensure that the buffer is reset to the idle state.

3.122 Shift counters are used to record how many bits have been loaded into the 1024-bit registers. A check is now made on these counters by loading half the buffer with all ones. A buffer initialization order is issued which should reset the counter. A 16-bit checkerboard pattern is then placed into the buffer, and the stuff order is issued to move the checkerboard pattern to the top of the register. The register is then unloaded and the checkerboard pattern should be detected first if the counters were reset properly.

3.123 Cartridge Tape Transport Controller Test: Fifteen of the 18 cartridge tape transport controller orders are issued. The response to each order is verified for correctness. The last test of the CTTC verifies the cyclic redundant check (CRC) hardware. When the CRC number is shifted through the CRC register, a zero remaining indicates correct transfer, whereas a non-zero indicates an error. Erroneous as well as correct CRC operations are performed and the expected results verified.

3.124 Minirecorder Read Test: This is the tape deck read diagnostic test. In order for the test to execute, the cartridge must be in

place and write-enabled. The read-a-block order is issued for each track. The block selected on each track is the first block that requires the backspace to function properly. The read continuous order is issued for one track only. An initialization order is then issued and the tape unit should return to the idle state.

3.125 *Minirecorder Miscellaneous Function*

Test: In this test, all non-read/write functions are tested. The tape is allowed to run until calculations indicate that it is closer to the EOT (end of tape) than to the BOT (beginning of tape). A fast reverse order is then issued; fast forward speed is tested next. From the fast forward speed, the stop command is executed. The BOT/EOT sensor is now tested. The tape is positioned 20 blocks out. The backspace order is issued 20 times, which should inch the tape toward block 0. One more backspace order is issued, and 3 seconds is allowed to detect BOT hole in the tape by the LED sensor. If not detected in the allotted time, the initialization order is given to position the tape in a safe region outside the BOT region.

3.126 *Minirecorder Write Test:* This is the final test of the TDC and minirecorder.

The test consists basically of reading a block from the mate unit, modifying it, writing it on the unit being tested, and then reading and verifying it. If the test passes, the data on the unit being diagnosed is rewritten correctly. The mate unit must be in service for this test to execute. Failure of this test might be due to the other TDC unit being out of service.

TTY CONTROLLER

3.127 *TTYC Status:* Only two tests exist to diagnose the TTYC. Test 1 consists of sending a TTYC status request. Successful completion verifies the 3A CC-to-TTYC communication link, valid reply start code, and parity.

3.128 *TTYC Parity:* The second test checks parity of the eight low bits using maintenance orders in order to prohibit a printout. Parity is checked via the TTYC return on orders. Orders are first issued to rotate a one through the eight low bits. Then another order generates an all-ones field; and finally, an order generates an all-zeros field.

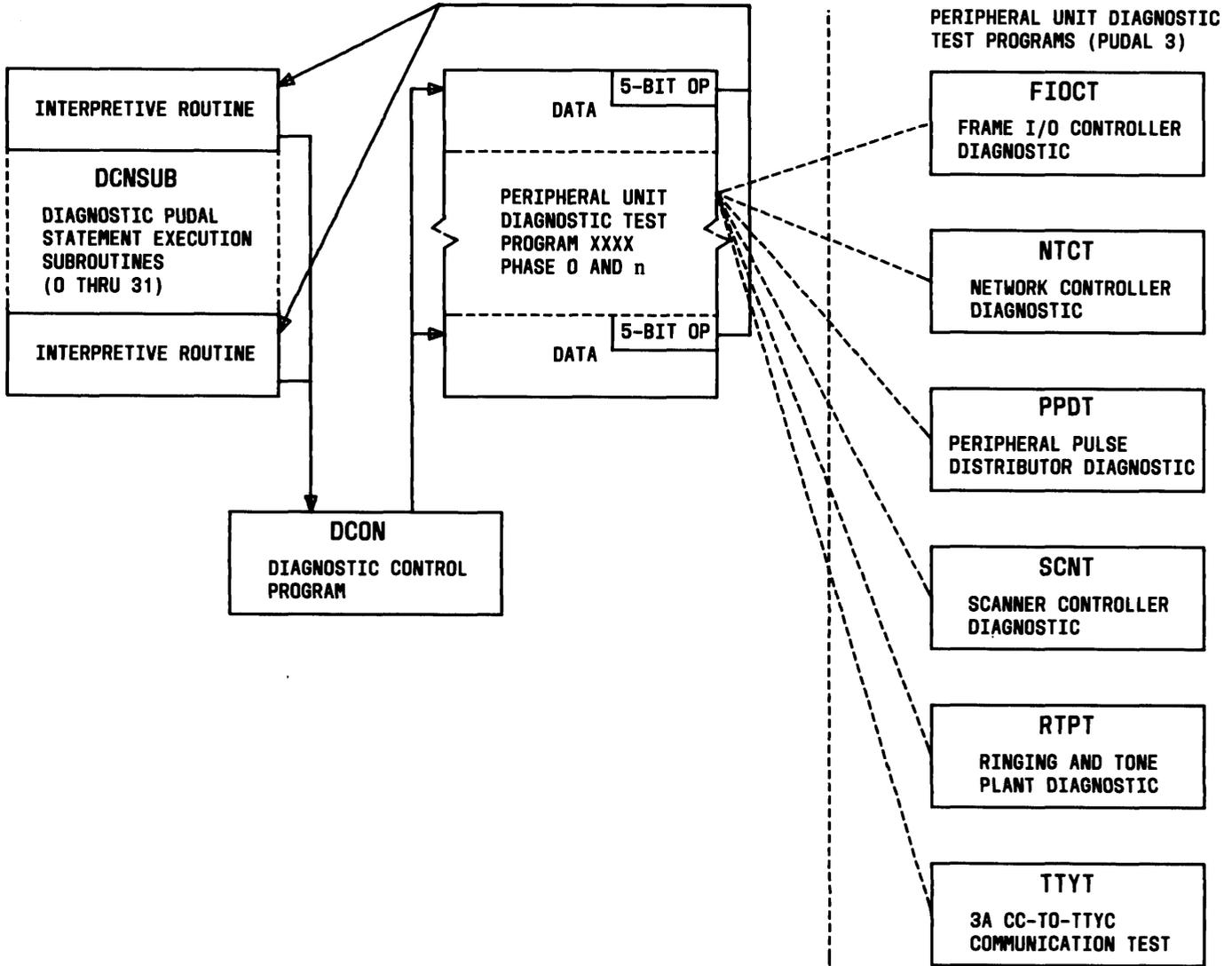


Fig. 1—Interrelationship of Peripheral Unit Diagnostic

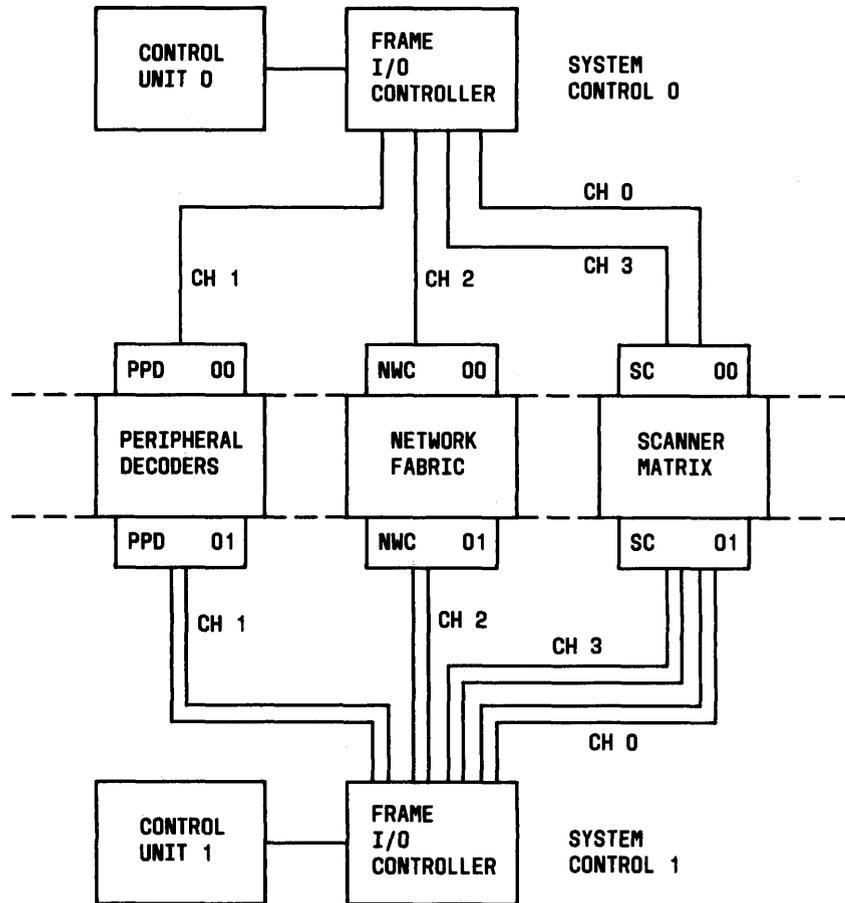


Fig. 2—Single Control Frame Office Configuration

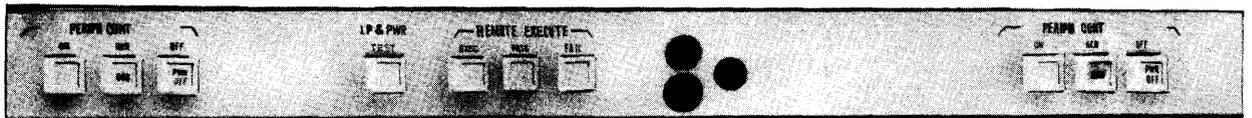


Fig. 3—Peripheral Control Unit Power Panel

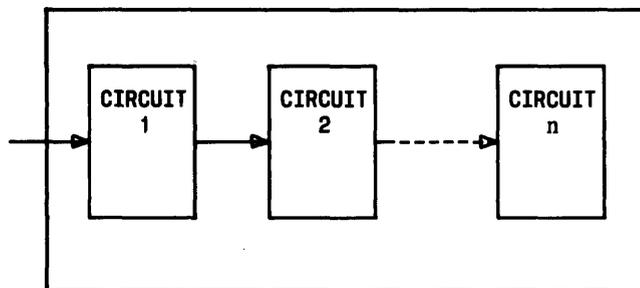


Fig. 4—Test Sequence

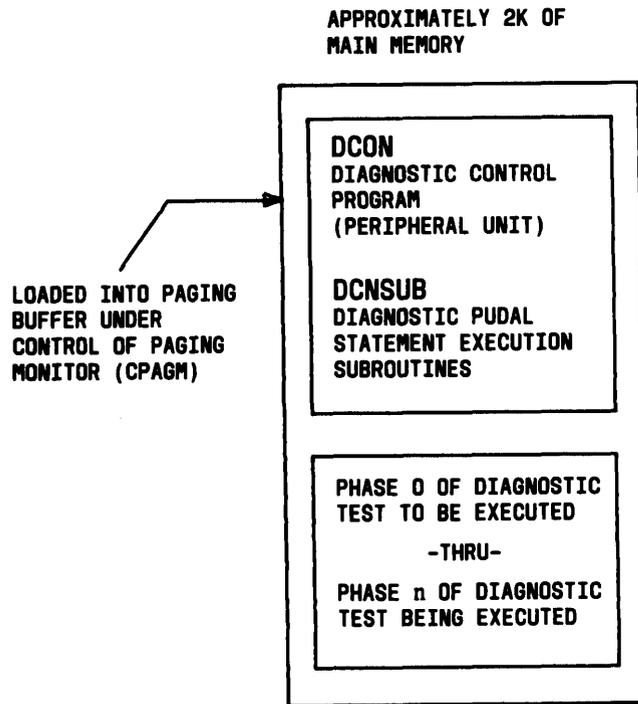


Fig. 5—Paging Buffer

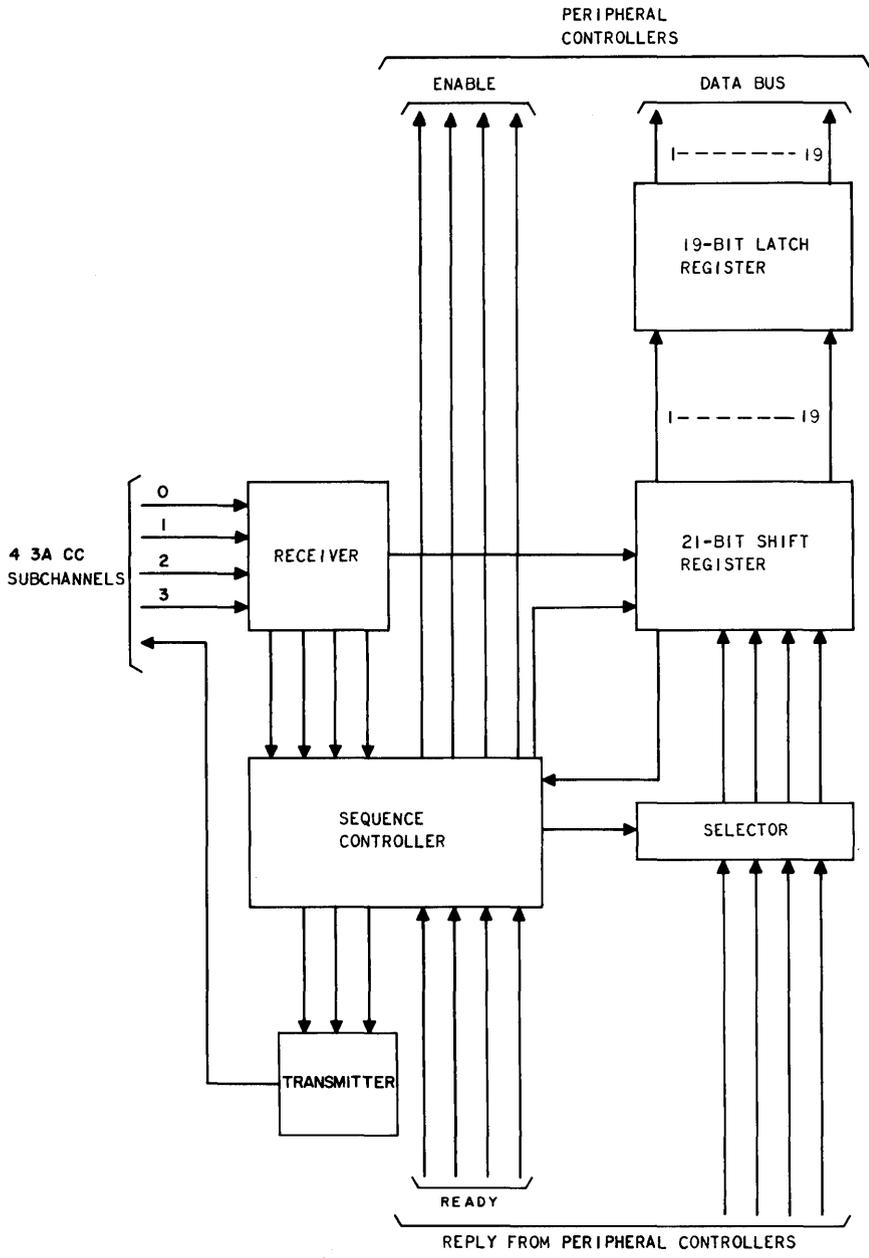
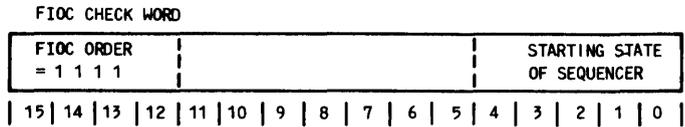
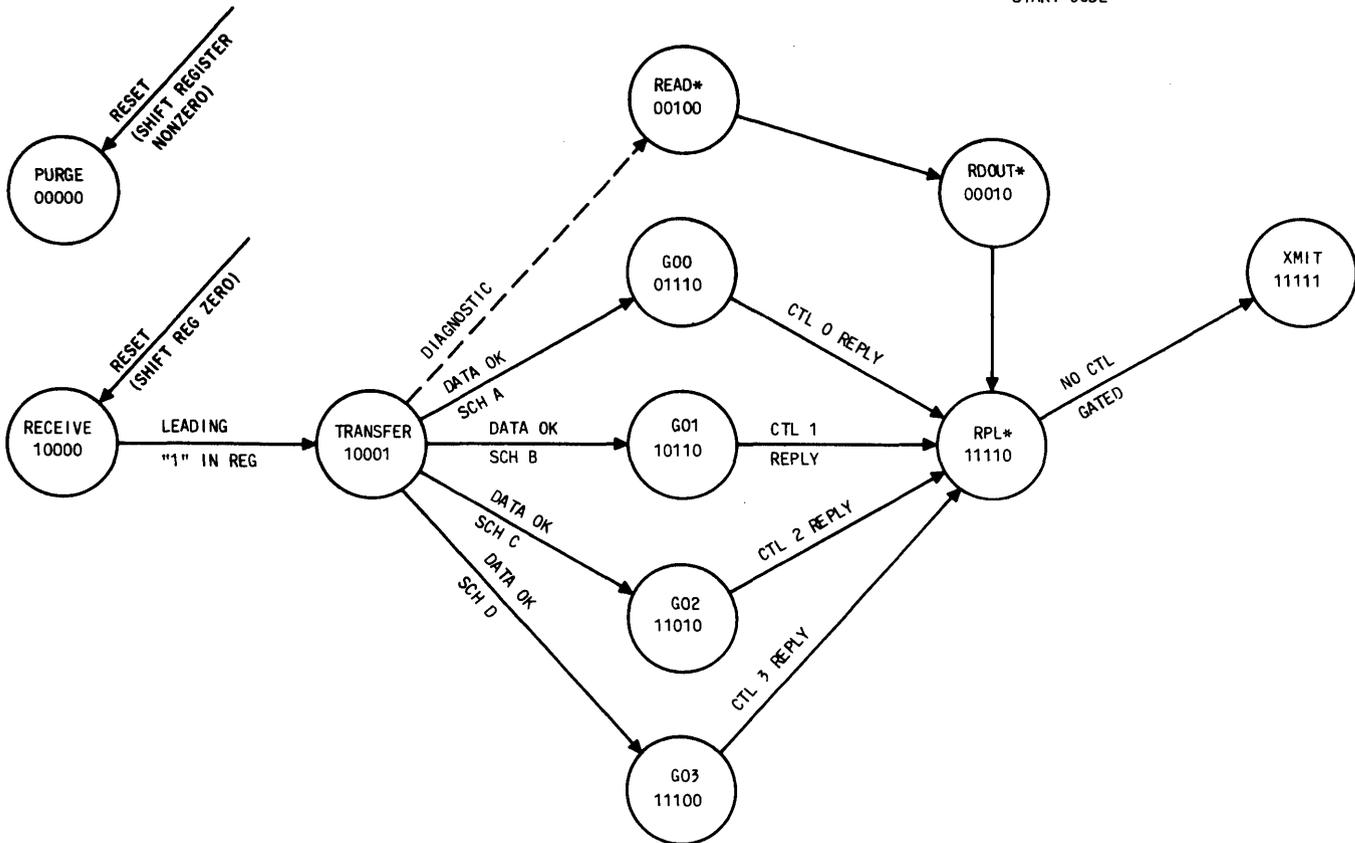


Fig. 6—FIOC Functional Diagram



NORMAL	0	1	1
MAINTENANCE	1	0	1

START CODE



NOTES:

1. THE 5-BIT CODE WITH EACH STATE REPRESENTS THE CONDITION OF THE STATE REGISTER (FLIP-FLOPS STA, STB, STC, STD, AND STE).
2. STATES MARKED * ARE TRANSITIONAL STATES, THE EXIT FROM WHICH IS DEPENDENT ONLY ON INTERNAL CONDITIONS.
3. "DATA OK" IS DEFINED AS A NORMAL START WITH GOOD PARITY OR A MAINTENANCE START WITH ANY PARITY.
4. A MESSAGE RECEIVED ON SCH A WITH A MAINTENANCE START AND GOOD PARITY AND WHICH HAS BITS 15-12="1111" WILL BE RECOGNIZED AS A DIAGNOSE ORDER. THE NORMAL TRANSITION TO STATE GOO IS SUPPRESSED AND INSTEAD, BITS 4-0 OF THE MESSAGE ARE LOADED INTO THE STATE REGISTER FLIP-FLOPS.
5. THE FIRST PULSE OF A NEW MESSAGE OR THE MATE FIOC ENTERING ITS "RDOUT" STATE WHEN NO SUBCHANNEL IS ACTIVE ON THIS FIOC WILL CAUSE A RESET TO "PURGE" OR "RECEIVE" DEPENDING ON WHETHER THE SHIFT REGISTER IS NONZERO OR ZERO, RESPECTIVELY.
6. FUNCTIONS OF THE STATES ARE AS FOLLOWS:
 "PURGE", "RECEIVE" - THE INCOMING BIT STREAM SHIFTED INTO THE SHIFT REGISTER.
 "TRANSFER" - THE CONTENTS OF THE SHIFT REGISTER ARE LOADED INTO THE OUTPUT LATCHES.
 "GO-" - THE ENABLE GATE TO THE SELECTED CONTROLLER IS ACTIVATED. REPLY DATA FROM THE SELECTED CONTROLLER IS LOADED INTO THE SHIFT REGISTER.
 "RPL" - LOAD PARITY INTO SHIFT REGISTER.
 "XMIT" - THE OUTPUT FROM THE SHIFT REGISTER IS TRANSMITTED TO THE CC. THE INCOMING BIT STREAM IS SHIFTED INTO THE SHIFT REGISTER.
 "READ" - THE STATE OF THE MATE FIOC IS LOADED INTO THE SHIFT REGISTER.
 "RDOUT" - THE MATE FIOC SEQUENCER IS RESET IF IT IS IDLE.

Fig. 7—FIOC Check Word and Sequence Controller Maintenance Steps

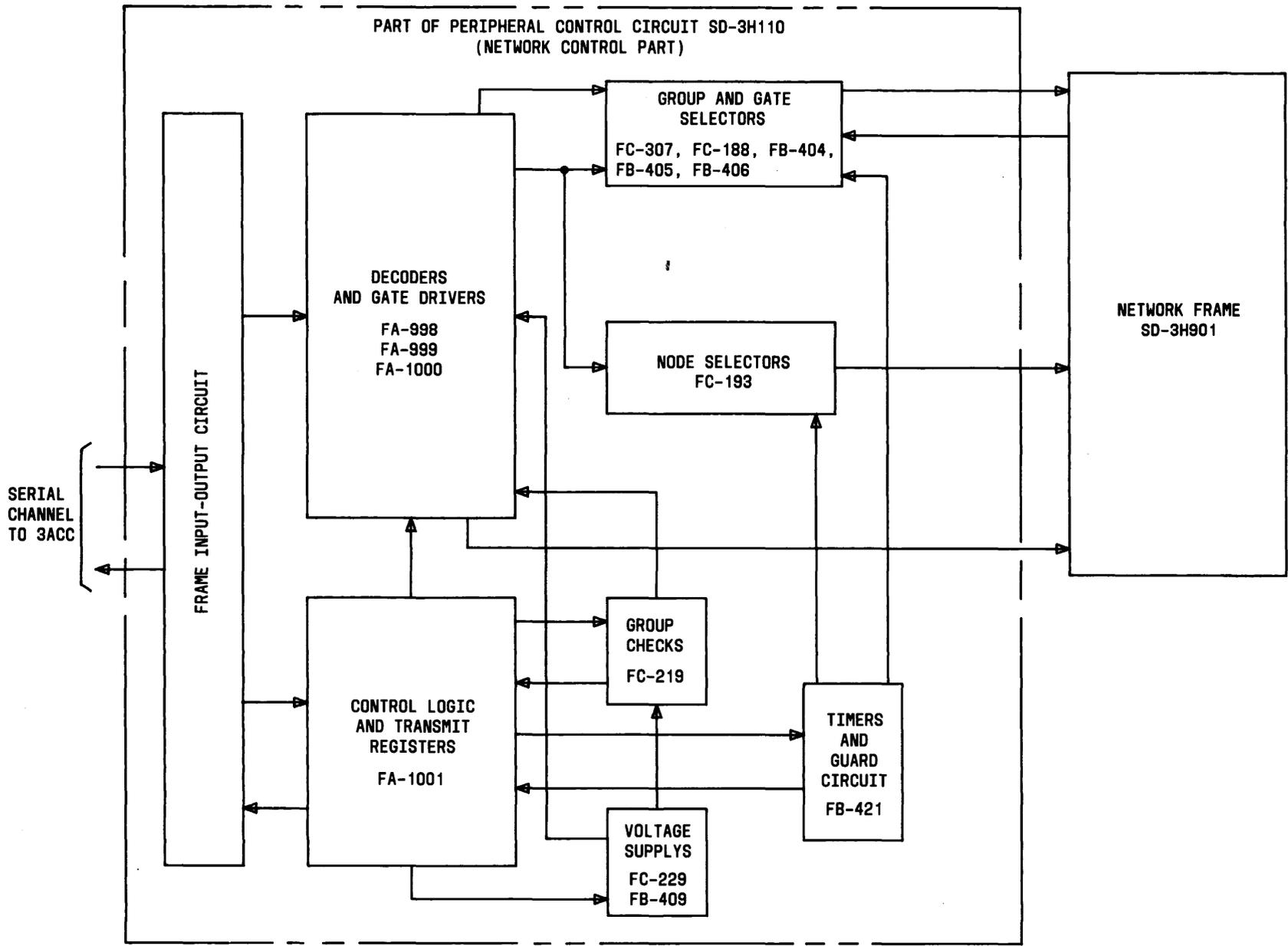


Fig. 8—Major Function Block Diagram of Network Control

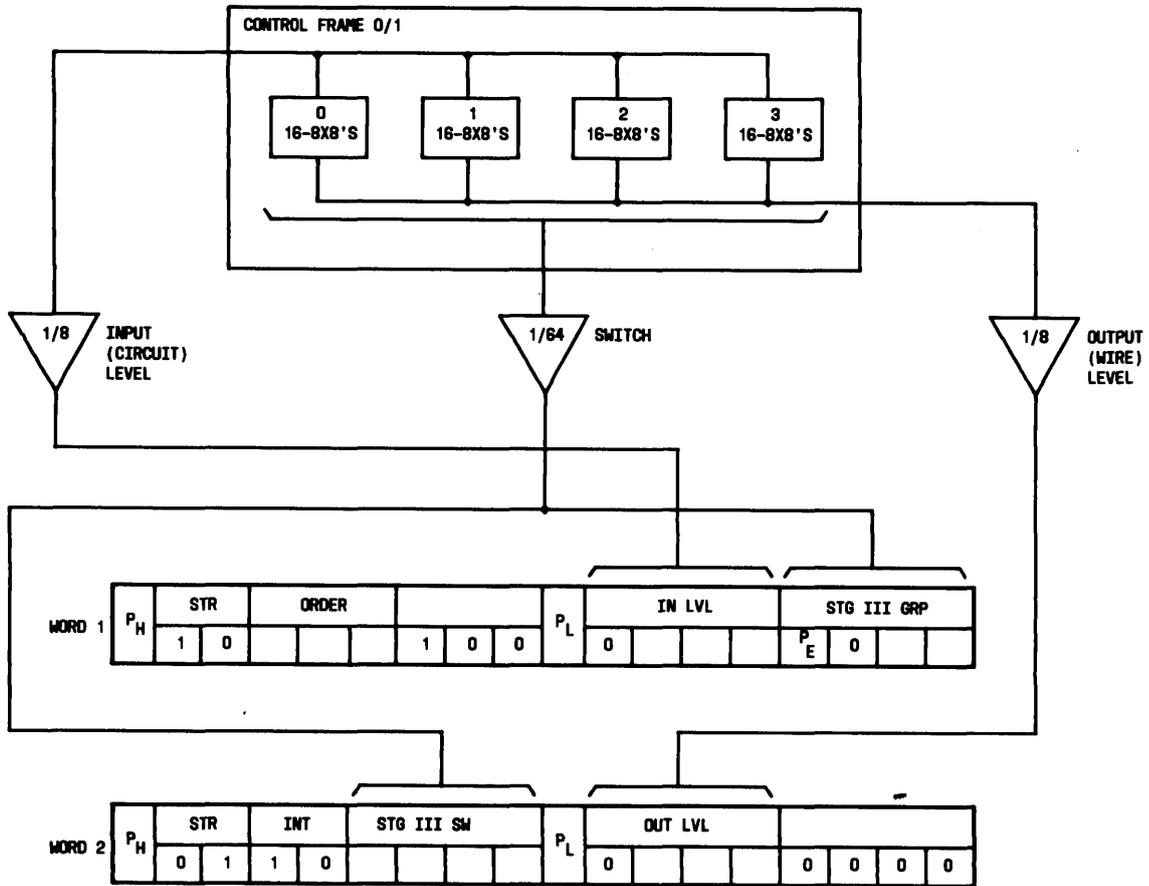


Fig. 9—No. 3 ESS Stage III Path Selection

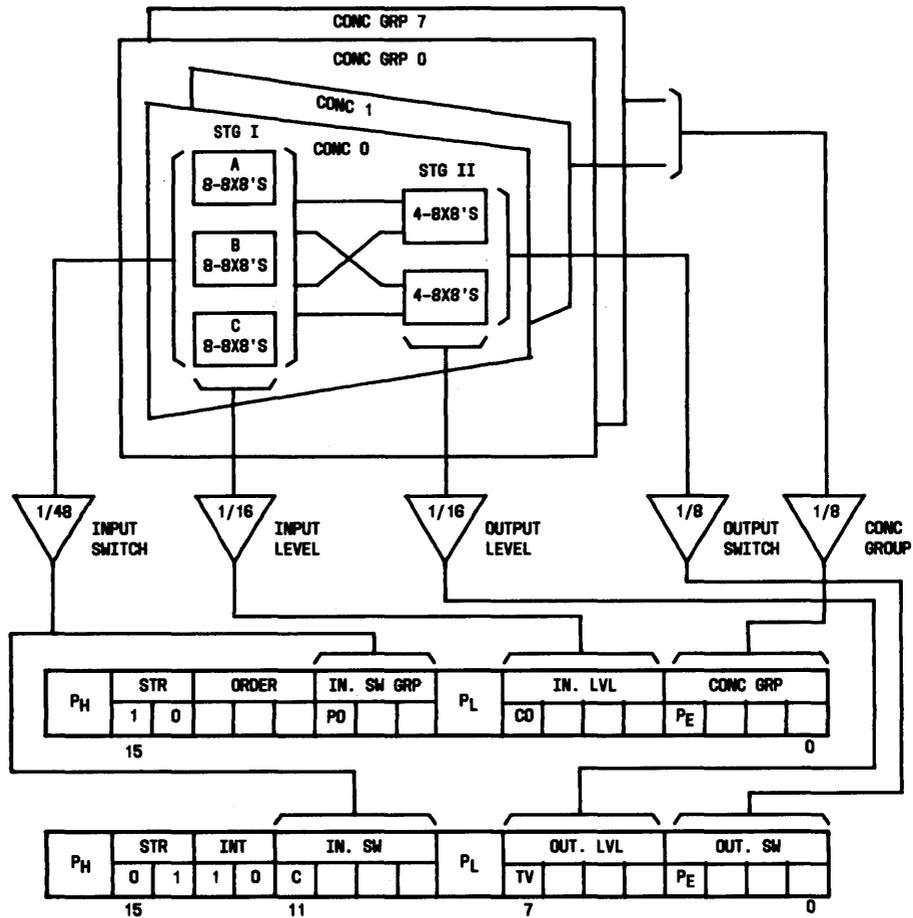


Fig. 10—No. 3 ESS Concentrator Selection

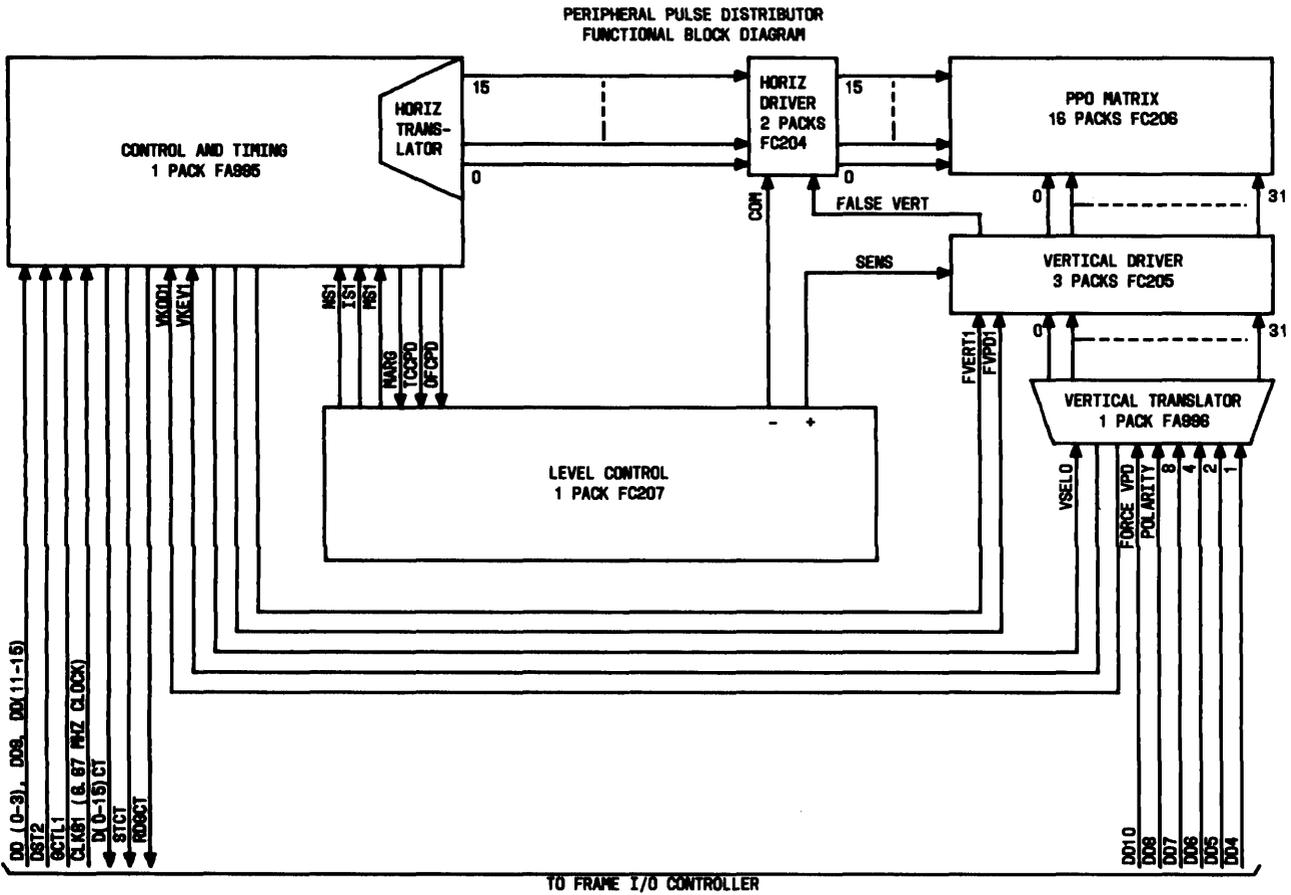
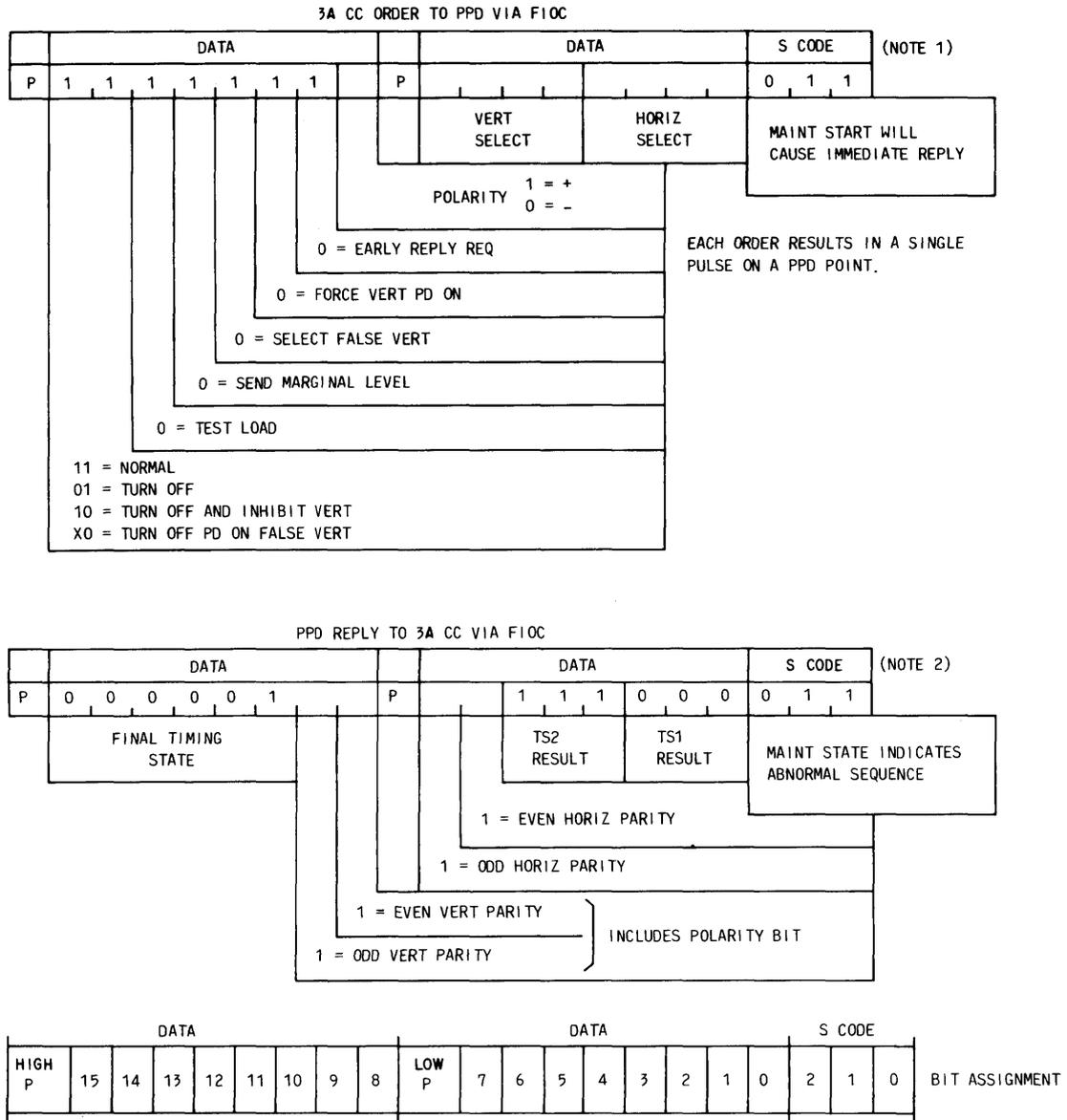


Fig. 11—Peripheral Decoder Functional Diagram



NOTES:

1. THE START CODE IS USED IN THE FIOC TO GENERATE THE DST2 OUTPUT TO THE PPD.
2. THE START CODE IS GENERATED IN THE FIOC USING THE STCT INPUT FROM THE PPD.

Fig. 12—Peripheral Pulse Distributor Data Format

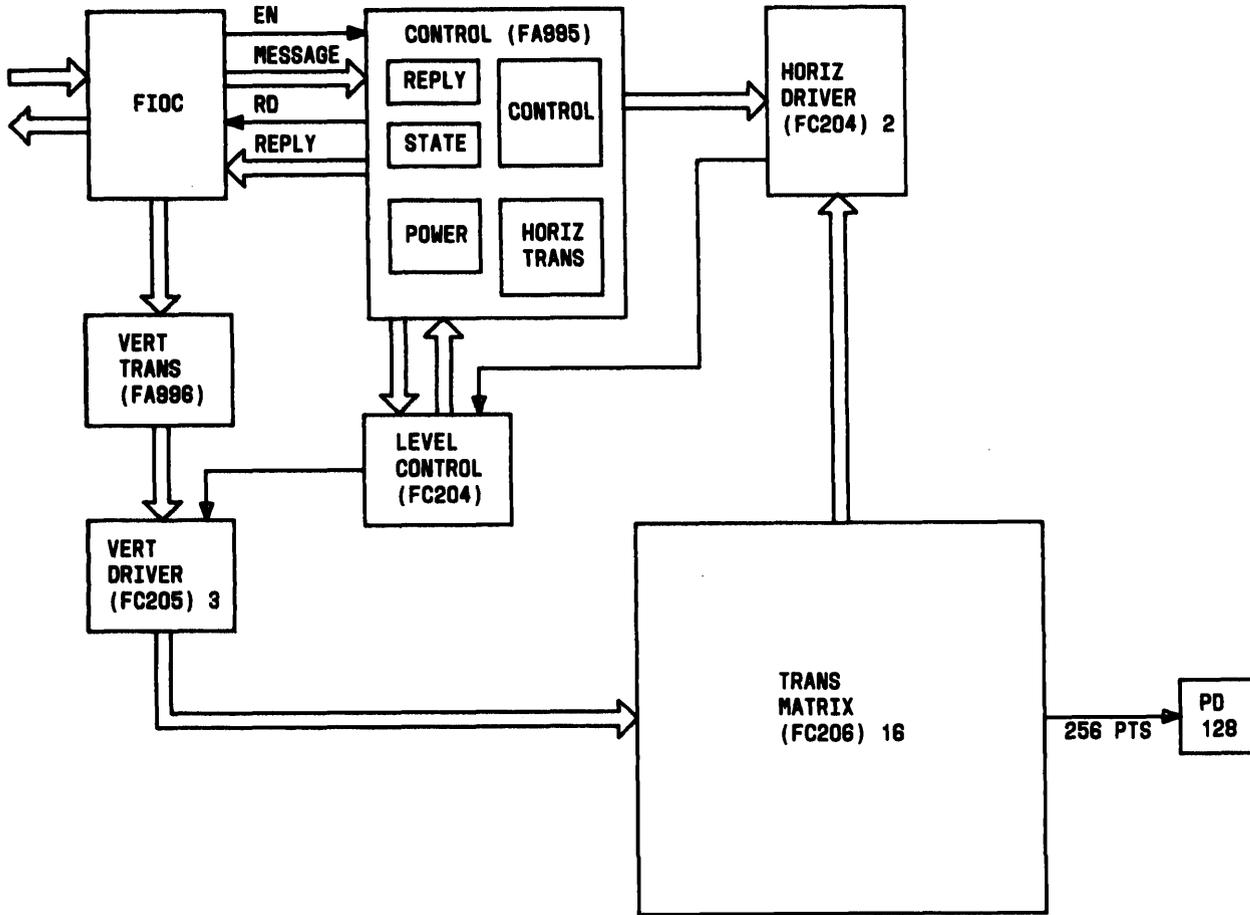


Fig. 13—PPD Structure

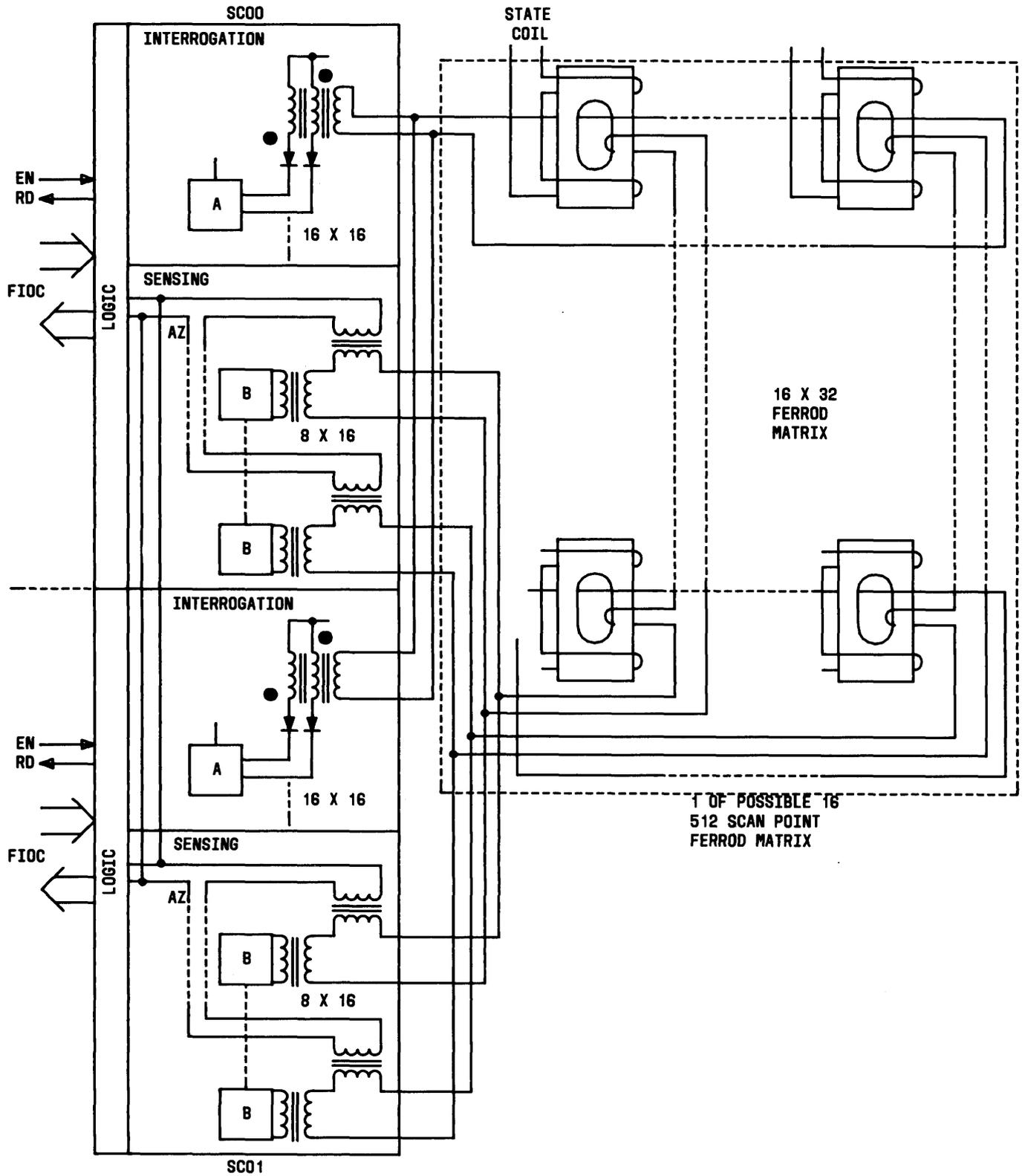


Fig. 14—Scanner Controller/Ferrod Matrix Interface

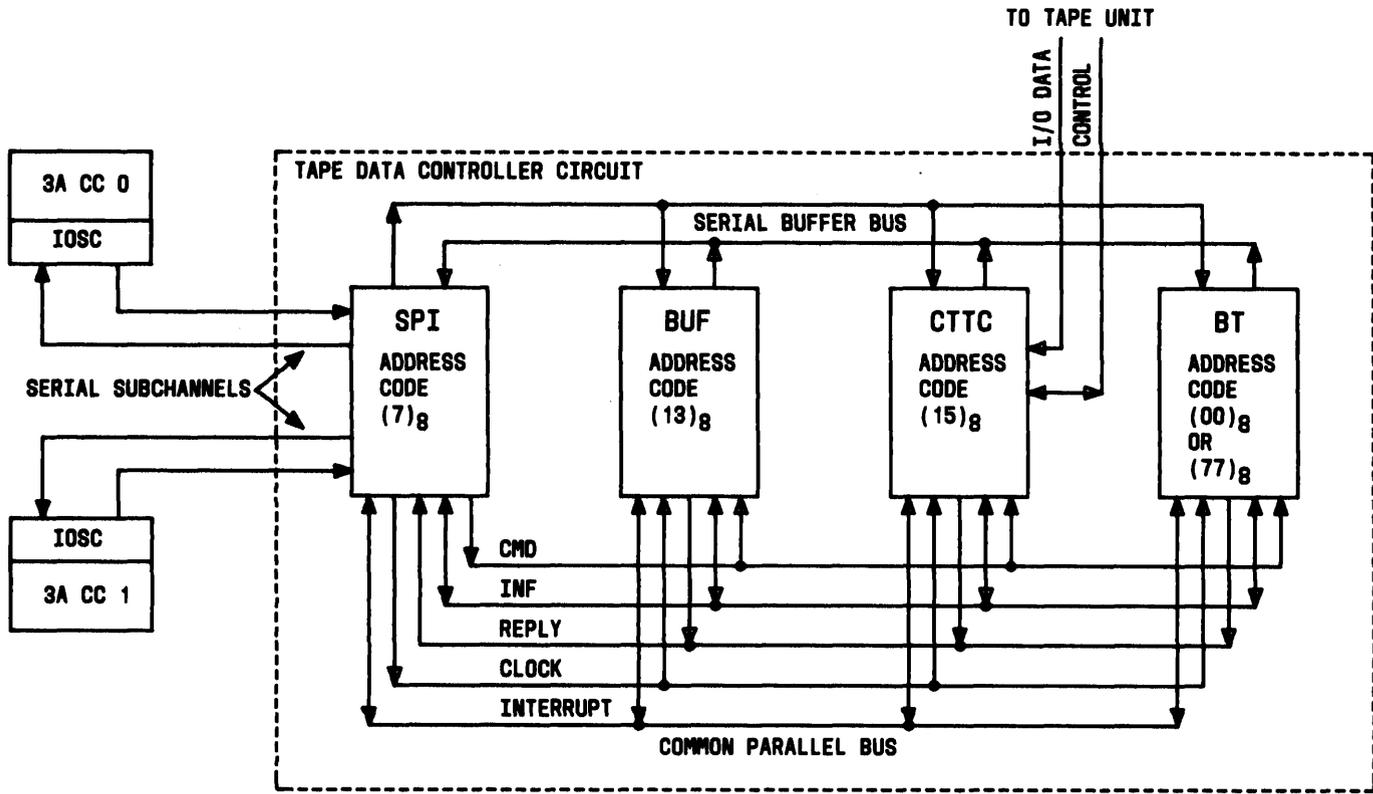


Fig. 15—Tape Data Controller Functional Diagram

TABLE A
ABBREVIATIONS AND ACRONYMS

ABBREVIATION	TERM
AR	Audible Ring
ASW	All-Seems-Well
BOT	Beginning of Tape
BR	Buffer Ready
BT	Bus Terminator
CLR	Control Logic and Register
CRC	Cyclic Redundant Check
CTAPM	Tape Data Controller Diagnostic
CTTC	Cartridge Tape Transport Controller
DCNSUB	Diagnostic Pудal Statement Execution Subroutines
DCON	Diagnostic Control Program
EOT	End of Tape
ESS	Electronic Switching System
FCG	False Cross and Ground
FIOC	Frame Input/Output Controller
FIOCT	Frame Input/Output Controller Diagnostic
GD	Ground Detector
HT	High Tone
IPM	Impulse Per Minute
ITR	Intermediate Transfer Register
MC	Marginal Check
MT	Call Waiting
NTCT	Network Controller Diagnostic
NWC	Network Controller
OOS	Out-of-Service
PAT	Power Alarm Test
PD	Peripheral Decoder
PPD	Peripheral Pulse Distributor
PPDT	Peripheral Pulse Distributor Diagnostic
PUDAL	Peripheral Unit Diagnostic Language
ROH	Receiver Off-Hook

TABLE A (Contd)

ABBREVIATIONS AND ACRONYMS

ABBREVIATION	TERM
RTPT	Ringing and Tone Plant Diagnostic
SC	Scanner Controller
SCNT	Scanner Controller Diagnostic
SPI	Serial Parallel Interface
SSP	System Status Panel
SYC	System Control
TDC	Tape Data Controller
TEN	Terminal Equipment Number
TT	TOUCH-TONE
TTY	Teletypewriter
TTYT	TTY Controller Diagnostic
3A CC	3A Central Control

TABLE B

SCAN POINTS (RT)

SCAN POINT (RT)	STATUS SIGNAL
01	Blown Ringing Fuse
02	No Voltage on 20-Hz Inverter Side 0
03	No Voltage on 20-Hz Inverter Side 1
04	No Voltage on Ringing Output Bus
05	TOUCH-TONE Low Voltage Side 0
06	Call Waiting Low Voltage Side 0
07	Audible Ring Low Voltage Side 0
08	High Tone Low Voltage Side 0
09	Busy Tone Low Voltage Side 0
10	TOUCH-TONE Low Voltage Side 1
11	Call Waiting Low Voltage Side 1
12	Audible Ring Low Voltage Side 1
13	High Tone Low Voltage Side 0
14	Busy Tone Low Voltage Side 1
15	No-Voltage ROH Generator
16	Defective Interrupter Relay Side 0
17	Defective Interrupter Relay Side 1
18	Power Off Side 0
19	Blown -48 or +48 Volt Fuse Side 0
20	Power Off Side 1
21	Blown -48 or +48 Volt Fuse Side 1
22	Overload on BT (60 IPM) Output
23	Ground on Tone Output Side 0
24	Ground on Tone Output Side 1
25	In-Service Status of Side 0 and Side 1

TABLE C

DISTRIBUTOR POINTS (RT)

DISTRIBUTOR POINTS (RT)	FUNCTION
A0	Operates IN10-0 Interrupter Relay
A1	Operates IN10-1 Interrupter Relay
B0	Operates IN120-0 Interrupter Relay
B1	Operates IN120-1 Interrupter Relay
C0	Operates IN60-0 Interrupter Relay
C1	Operates IN60-1 Interrupter Relay
D0	Operates GDT1 Ground Detection Relay
D1	Operates RT0-1 Ringing Transfer Relay
E0	Operates GDT2 Ground Detection Relay
F0	Operates GDT3 Ground Detection Relay
G0	Operates MC0 Marginal Check Relay
G1	Operates OA Overload Announcement Relay
H0	Operates MC1 Marginal Check Relay
K0	Lights OOS-0 Out-of-Service Lamp
K1	Lights OOS-1 Out-of-Service Lamp