Service Circuit System (SCS) Description
4ESS™ Switch

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1. Overview

1.01 This practice provides a description of the Service Circuit System (SCS) equipment. It is intended to serve as an overall reference for the planning, operation, and administration stages of the SCS for system engineering and the craftsperson associated with the system. The following subjects are included:

- Physical descriptions
- Functional descriptions
- Capacities
- Power requirements
- Maintenance philosophy.

1.02 This practice is being reissued to add information on Phase 2 of the optional Automatic Speech Recognition (ASR) feature. Information is also included on the new UN591 Executive Processor circuit pack.

1.03 This practice does not contain admonishments.

1.04 Your comments on this practice are welcome. Your comments will aid us in improving the quality and usefulness of documentation. Please use the Feedback Form provided in the back of this practice or call 1-888-LT INFO6 (584-6366).

1.05 Additional copies of this practice, associated appendixes, and all referenced practices may be ordered from the Lucent Technologies Customer Information Center as follows:

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- Complete Form INDI-80.80 and mail to:

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  Indianapolis, IN 46219-1999

1.06 Every effort was made to ensure that the information in this practice was complete and accurate at the time of printing. However, information is subject to change.

1.07 This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the installation manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

1.08 At the end of this practice, there is a list of the abbreviations and acronyms used in this practice.

1.09 This practice was developed by Lucent Technologies Network Systems Toll Switching, Voice & Signaling (TSVS) Information Development.

2. General

Purpose of the SCS

2.01 The SCS is a family of equipment cabinets that provides announcement and digit collection capabilities for the *4ESS*™ switch. SCS configurations include both software and firmware.

2.02 The SCS provides the following functions for telephone network services:

- Playing of recorded announcements that contain instructions or prompts to callers.
- Collection of various information by receiving touch-tone dialed signals.
- With the optional Automatic Speech Recognition (ASR) feature, collection of various information by receiving spoken responses. Two different ASR versions are provided: ASR Phase 1 and ASR Phase 2.

Differences between the two ASR versions are described throughout this practice.

2.03 The SCS incorporates the functions previously listed into the *4ESS* switch by harnessing the connection capabilities of the *4ESS* switch call processing logic. This means the *4ESS* switch can play announcements to both the caller and called party. It can also collect information from both the caller and called party.

2.04 With the SCS, critical buses and data links are duplicated. Also, critical circuit packs as well as the Hard Disk Units (HDUs) which store SCS announcements are duplicated. The SCS is designed so that no single point of failure will cause loss of service or degradation so severe that the system is unable to handle its usual load.

2.05 The SCS greatly improves the announcement and information collection capabilities of the *4ESS* switch with high reliability and performance. The result is a reduction of capital and operational expense involved with announcements and information collection. Another benefit is increased caller acceptance and sponsor satisfaction as a result of decreased call setup delays and decreased out-of-service time. Also, SCS increases the total number of available customized and generic announcements.

2.06 With the optional ASR feature, information collection capabilities are greatly improved and become more flexible by providing recognition of spoken responses such as digits (1, 2, 3, etc.) and simple words ("zero," "yes," "no," etc.). ASR also reduces expenses by decreasing required attendant services for customers that do not have touch-tone capability.

Equipment Characteristics

2.07 The main components of the SCS are the Service Circuit Controller (SCC), Service Circuit Unit (SCU), the HDU, and the Custom Data Services Unit (CDSU). The CDSU is provided only with the ASR feature. Each of these components is shown in Figure 1 and is discussed later in more detail. However, these main components are supported by many other components which are also described elsewhere in this practice.

2.08 The SCU is really the heart of the SCS. The SCU plays the announcements and asks for any digits that need to be collected. However, the SCU must be told what it needs to do by the *4ESS* switch. This is where the SCC comes in. The SCC translates messages between the 1B Processor Central Controller (CC) of the *4ESS* switch and the SCU so that they can understand each other. The SCU's announcements are stored in the HDUs.

2.09 The duplicated SCC serves as an interface between the *4ESS* switch 1B Processor CC and the SCU. In addition to translating messages between the 1B Processor CC and the SCU and routing these messages to the correct place, the SCC provides error detection and fault recovery capabilities for the SCU.

2.10 As shown in Figure 1, the SCC communicates with the 1B Processor CC via the Peripheral Unit Bus (PUB), which is shared with many other *4ESS* switch peripherals. The PUB is fully duplicated and has 24 data bits from the 1B Processor CC to the SCC and 24 data bits from the SCC to 1B Processor CC. There are also some dedicated control and response bits for specialized polling of peripherals by the 1B Processor CC, fault recovery, and error detection for a total of 64 transmit bits and 32 reply bits. A maximum of eight SCCs can be connected to a *4ESS* switch.

2.11 To allow polling of the SCC's buffers, **the SCCs must be placed on a PUB Branch (PUBB) with the extended buffer polling option**. The extended buffer polling option expands the 1B Processor CC's buffer polling capabilities on a specific PUBB. Replies to the extended buffer polling on the SCCs are on bits 8 through 15 of the Peripheral Unit Reply Bus (PURB). Additional information on extended buffer polling and its requirements can be found in 234-110-010, *Peripheral Unit Bus System Description 4ESS Switch*.

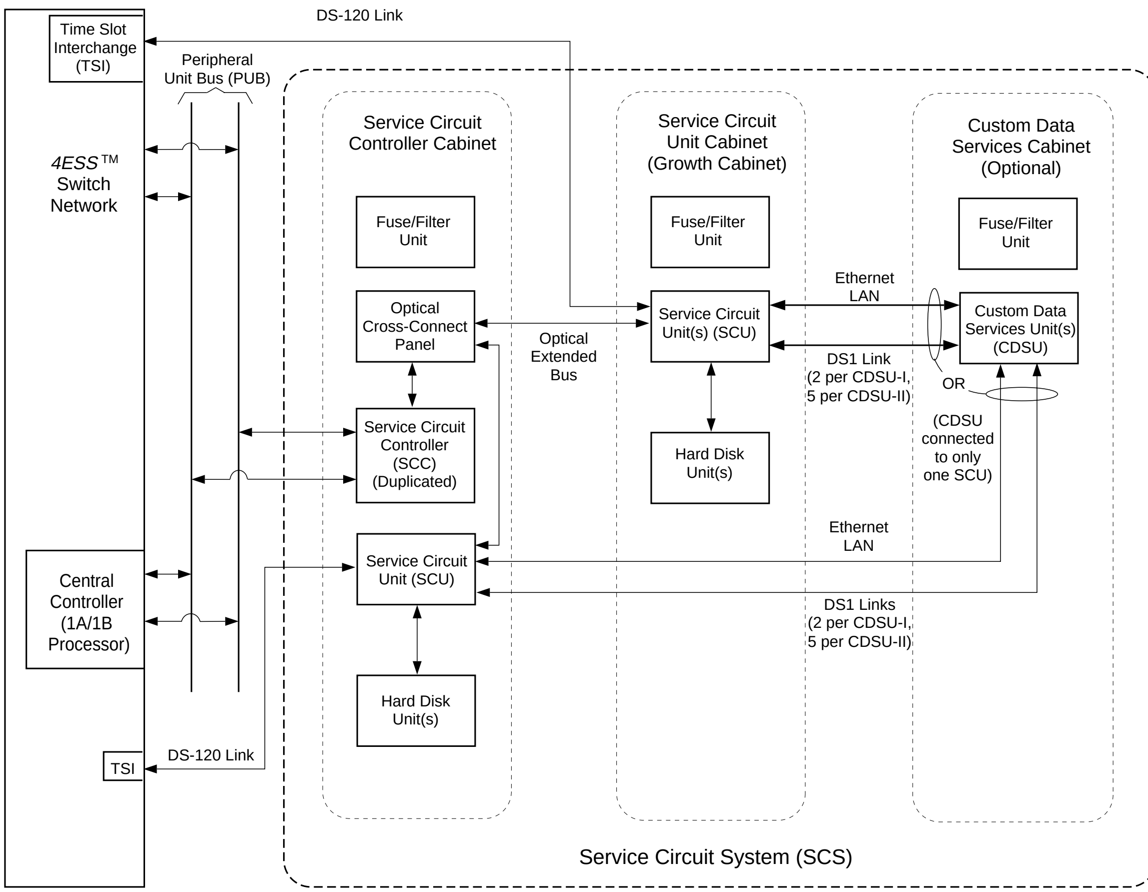

Figure 1. The SCS Interface

2.12 The SCC communicates with the SCU(s) through a duplicated optical Extended Bus (EB), which is discussed later in more detail. Each of the EB links (there can be as many as 16 per SCC) is controlled by the SCC. Each link can transfer data at 100 Mbps through the pair of optical fibers. The EB links are duplicated with one link from each half of the duplicated SCC going to each SCU it controls.

2.13 Each SCU has a bidirectional DS-120 link to the *4ESS* switch. Each link consists of a pair of coaxial cables. Digital data representing announcements and Dual Tone Multifrequency (DTMF) tones are sent serially on the DS-120 links with 120 voice terminations and 8 maintenance channels per link.

2.14 CDSUs provide ASR capabilities for the SCS. There are two different types of CDSUs available. The CDSU-I is used with the ASR Phase 1 feature. The CDSU-II is used with the ASR Phase 2 feature. The CDSUs are located in a separate Custom Data Services Cabinet (CDSC). There are also two different CDSCs available (a CDSC-I for ASR Phase 1 and a CDSC-II for ASR Phase 2).

2.15 A CDSC-I can contain as many as five CDSU-Is. One CDSC-I (with up to five CDSU-Is) is connected to each SCU with ASR capability. Two DS1 links connect the SCU to each CDSU-I (half of each link is used for ASR and the other half of each link is used for echo cancellation). An Ethernet Local Area Network (LAN) connection is provided between the SCU and the CDSU-Is as a control link. The LAN is connected to one CDSU-I, daisy-chained to each of the other CDSU-Is within the CDSC-I, then connected to the Smart HUB. See Figure 2 for SCU/CDSU-I/AAP connections.

2.16 A CDSC-II can contain as many as four CDSU-IIs. One CDSC-II (with up to four CDSU-IIs) is connected to up to two SCUs with ASR capability. Two CDSU-IIs are dedicated to each SCU. Five DS1 links connect each CDSU-II to the SCU. An Ethernet LAN connection is provided between the SCU and the CDSU-IIs as a control link. The LAN is connected to one CDSU-II, daisy-chained to the other CDSU-II associated with that SCU, then connected to the Smart HUB. See Figure 3 for SCU/CDSU-II/AAP connections.

2.17 Announcement administration for the SCU is provided by an Announcement Administrative Processor (AAP). The AAP communicates with SCUs over a dedicated LAN. The AAP also communicates with the CDSUs over a LAN via a Smart HUB.

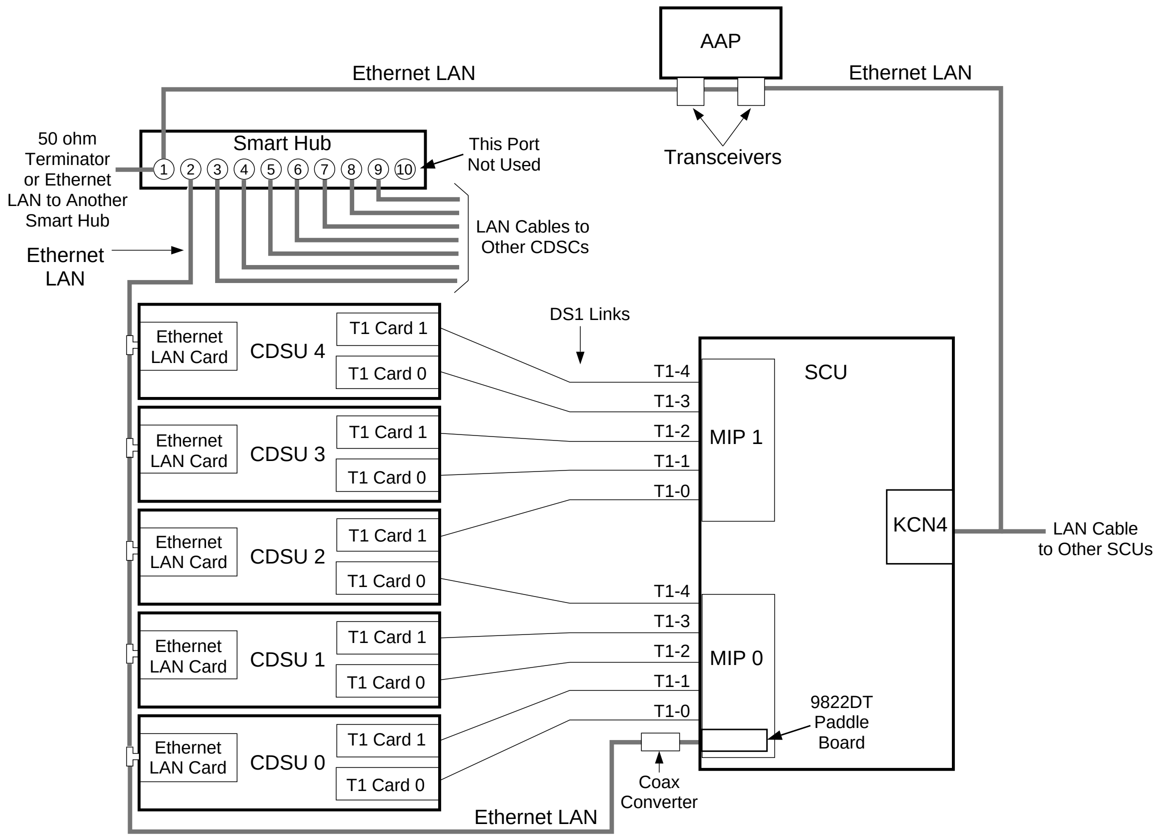

Figure 2. SCU/CDSU-I/AAP Connections

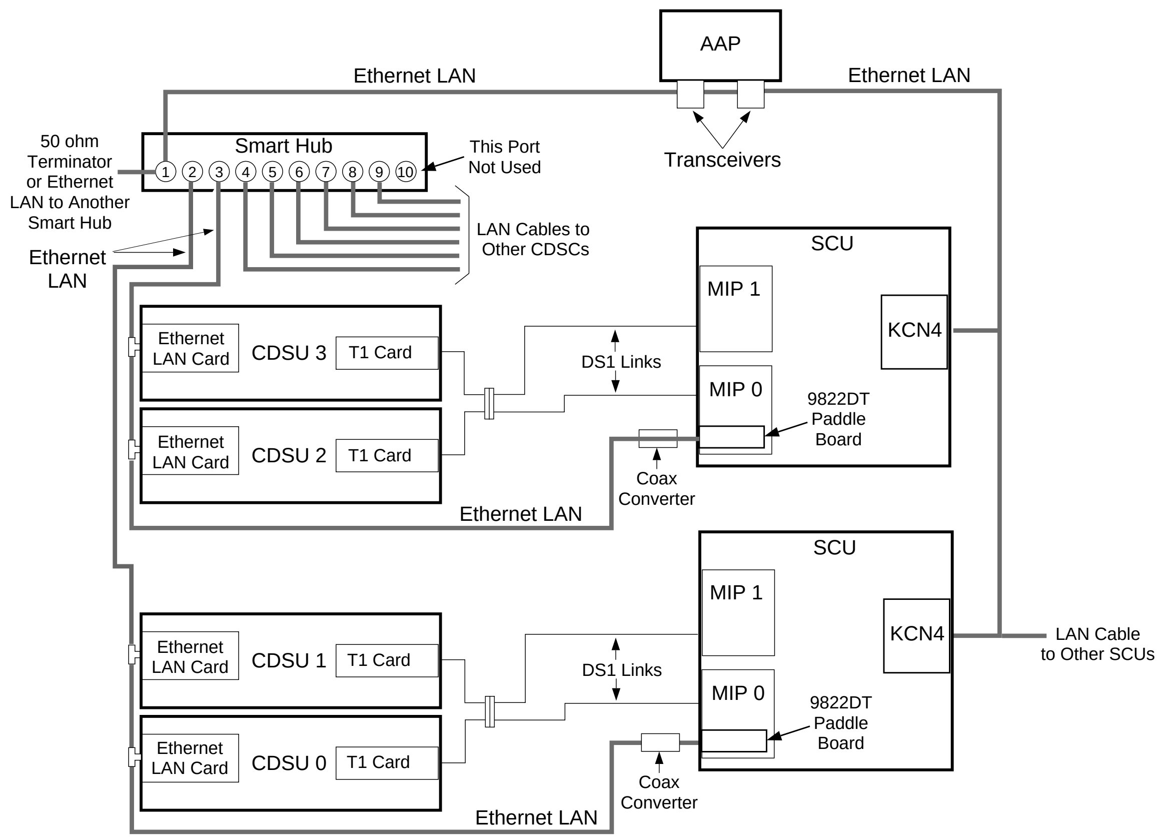

Figure 3. SCU/CDSU-II/AAP Connections

3. Physical Description

General

3.01 The equipment cabinets used for each SCS are 6 feet high, 2 feet 6 inches wide, and 24 inches deep. The equipment cabinets are the shielded type with double doors hinged at the edges of the cabinet. The units mounted in each SCC and SCU cabinet contain *FASTECH** circuit packs and backplanes. Integrated circuits of the dual in-line and surface mount variety and discrete components are both used in the circuit packs. Most power units are mounted in the same unit in which they are used and are adjacent to the circuit pack group served. Each circuit pack and power unit is labeled on designation strips to indicate its identity and boundaries. A 1-foot tall, 30-inch wide, and 24-inch deep cable cabinet is mounted on top of each cabinet.

Equipment Arrangements

3.02 Initially, each SCS consists of two or three cabinet types: the SCC cabinet (J4A024A-1), the SCU cabinet (J4A024B-1), and (optionally) the CDSC cabinet (J4A024C-1 or J4A024D-1). Initially, an SCS complex consists of one SCC cabinet and one SCU cabinet. A *4ESS* switch office can support up to eight SCS complexes.

The SCC Cabinet (J4A024A-1)

3.03 The SCC cabinet is the basic cabinet required in each SCS. The basic cabinet is equipped with each of the following units (Figure 4):

- One Fuse and Filter Panel (J5D003FJ-1)
- One Optical Cross-Connect Panel (J4A024AD-1)
- One SCC Unit 1 (J4A024AA-1)
- One SCU 0 (J4A024AB-1)
- One Fan Unit (J5D003FH-1)
- Up to two Hard Disk Units (J4A024AC-1).

* Registered trademark of Berg Electronics, Inc.

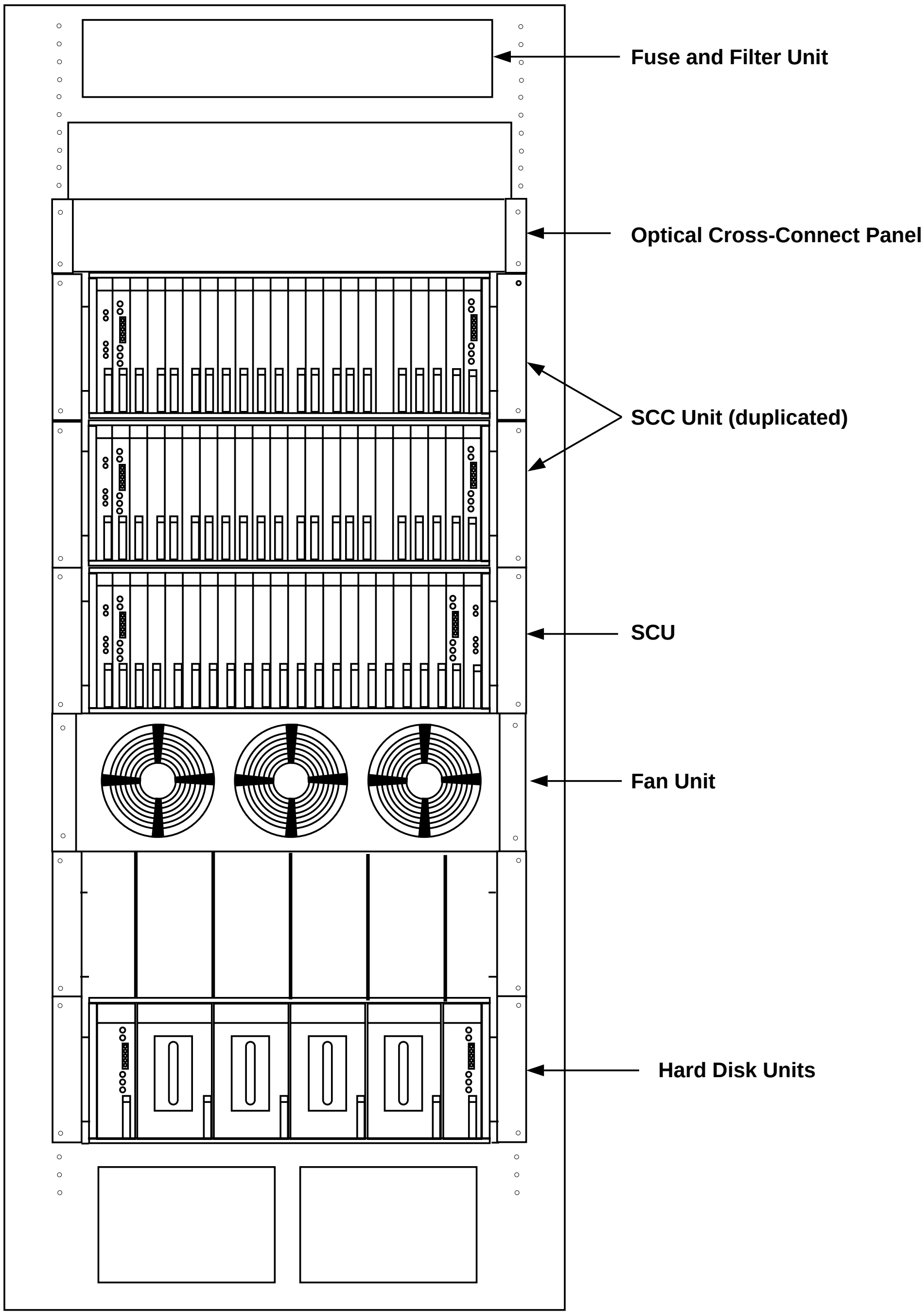

Figure 4. The SCC Cabinet (J4A024A-1) — Equipment Identification

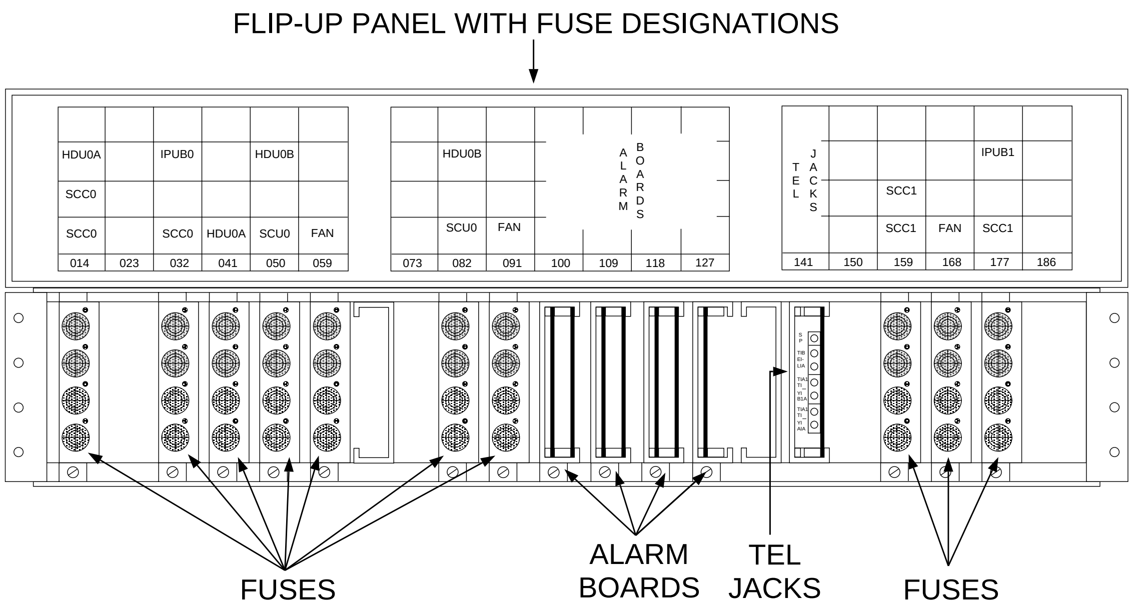

Figure 5. Fuse and Filter Panel for the SCC

A. Fuse and Filter Panel (J5D003FJ-1)

3.04 The SCC's fuse and filter panel has been arranged to accommodate the particular loads of the SCC cabinet. Figure 5 shows the front view of the panel and the designation strips located on the underside of the flip-up panel.

3.05 The fuse and filter panel has six input feeds from a Power Distribution Frame (PDF). These six input feeds supply the ten 4-position fuse blocks. Three alarm cards are provided, as well as one telephone jack card. The telephone jack card contains the following connectors/adapters:

SP 2-conductor bantam (.173 in.) male to 2-conductor bantam (.125 in.) female.

TEL 2-conductor twin bantam (.173 in.) male to 2-conductor twin longframe (.125 in.) female.

TTY 3-conductor twin bantam (.173 in.) male to 3-conductor twin longframe (.125 in.) male.

3.06 At the rear of the fuse and filter panel there are 12 possible inputs. Each input can accept a feed from a PDF. If used, an input consists of a capacitor, cables, connectors, other hardware, and at least one output fuse block at the front of the panel. The limit of fuse blocks that can be wired to a single feed depends on the total current through the feed and the available physical space in the panel for fuse blocks. Each capacitor assembly snaps in and out of the frame, and the fuse block holders and card holders are each removable. All wiring is connectorized and the various cards unplug from the card holder.

B. Optical Cross-Connect Panel (J4A024AD-1)

3.07 The SCCs and SCUs are interconnected by an optical EB. Both the SCCs and SCUs have Extended Bus (EB) circuit packs (discussed elsewhere in this practice). The optical cross-connect panel, located in the SCC cabinet, connects the optical fibers of the SCC's EB circuit packs to the optical fibers of the SCU's EB circuit packs.

3.08 Figure 6 shows the arrangement and assignment of the optical cable connectors located on the rear of the optical cross-connect panel. As shown in this figure, SCUs 0 through 7 are connected on row A. SCUs 8 through 15 are connected on row B. Each SCC has two connector appearances (one in row A and one in row B). This allows each SCC to access all SCUs in both rows A and B.

C. SCC Unit 1 (J4A024AA-1)

3.09 The SCC is a two-shelf unit consisting of two identical or duplexed controllers, each occupying a single shelf of the cabinet. The two controllers are stacked vertically with a common backplane.

3.10 The SCC (Figure 7) has six circuit pack types:

- Peripheral Unit Bus Driver/Receiver (UN349)
- Peripheral Unit Bus Interface (UN350)
- Executive Processor (UN351 or UN591)
- Global Random Access Memory (GRAM) (UN352)
- Extended Bus Interface (KCN3)
- Backplane Transceiver Logic (BTL) Bus Terminator (UN357).

3.11 The SCC has three power controller types:

- Integrated Power Controller (TN1671)
- Power Control (TN1984)
- Power Converter (410AA).

D. SCU 0 (J4A024AB-1)

3.12 The SCU is a single unit with one shelf of circuit packs. The SCU has up to 12 different circuit pack types:

- DS-120 Exchange and Interface (TN1588)
- Multifaceted Signal Processor (TN1589)
- Enhanced Peripheral Interface Controller (TN1976)
- Microstore (TN1977) or (TN9001)
- Small Computer System Interface (SCSI) Host Adapter (TN1978)
- Voice Processor (TN1979)
- Voice Processor Interface Controller (TN1980)
- Buffer Control (TN1981)
- Buffer Fabric (TN1982)
- Table RAM (TN1983) or (TN9002)
- Extended Bus and LAN Interface (KCN4)
- Multifunctional Interface Processor (TN4001) (used only with ASR).

3.13 The SCU has two power controller types:

- Power Control (TN1984)
- Power Converter (410AA).

E. Fan Unit (J5D003FH-1)

3.14 The bidirectional fan unit contains six fans (three located on the front of the unit and three located on the rear of the unit). The fan unit helps to cool the SCS cabinet.

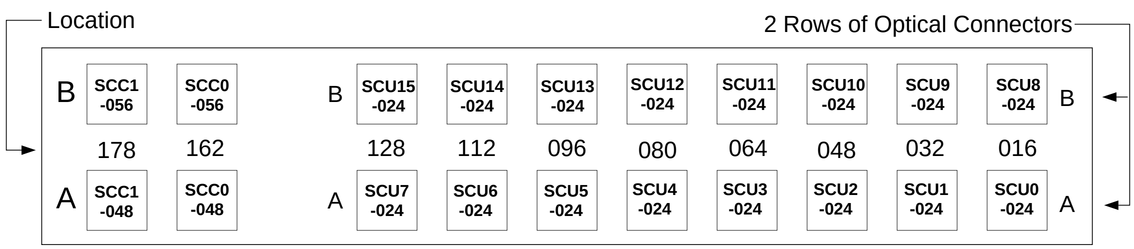

Figure 6. Optical Cable Connectors at Rear of Optical Cross-Connect Panel

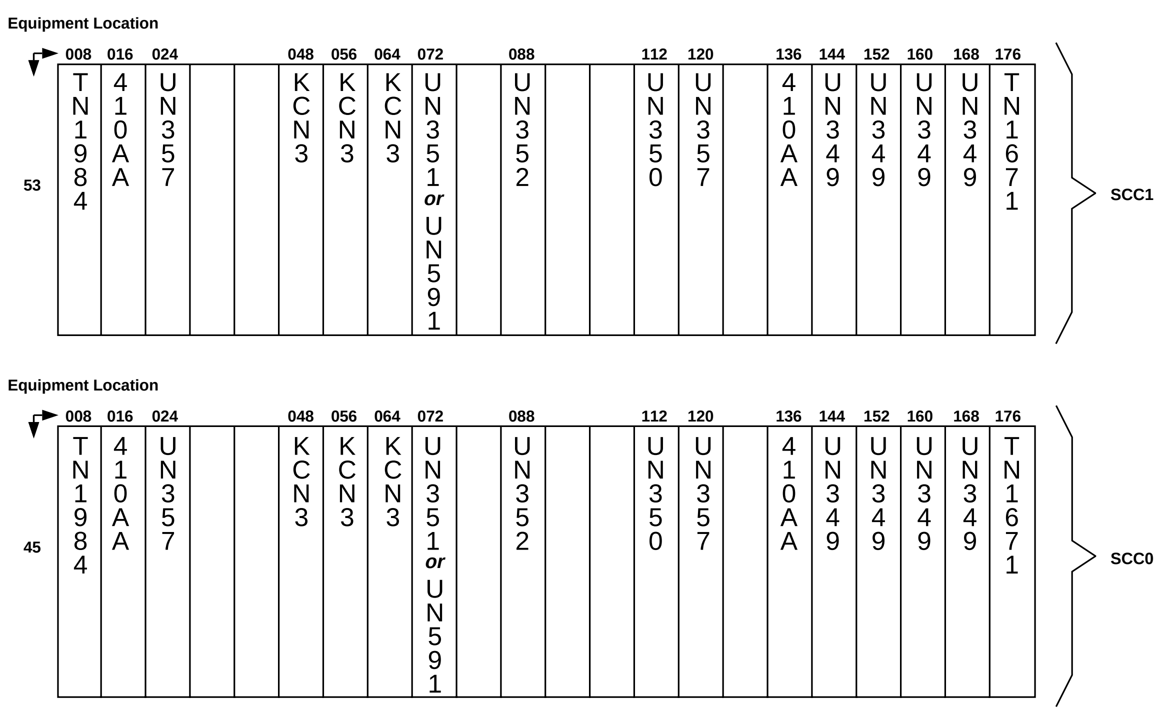

Figure 7. The SCC Unit - Circuit Pack Locations

F. Hard Disk Units (J4A024AC-1)

3.15 An HDU is comprised of two matched Hard Disk (HD) pairs and two power controllers. Each HDU takes up one shelf in the SCC cabinet. The SCC cabinet can be equipped with up to two HDUs (four matched pairs of hard disk circuit packs, all associated with SCU 0) for a total of two complete shelves. Each HDU uses up to four hard disk circuit packs (two pairs of hard disk circuit packs) and two UN356 disk power controller circuit packs. The hard disk circuit packs available are the TN1672 (420 MB), the TN1972 (2 GB), the TN4000 (4 GB), and the TN9000 (9 GB). The UN356 circuit pack supplies +12 V and +5 V to drive the hard disk circuit packs.

The SCU Cabinet (J4A024B-1)

3.16 The SCU cabinet is equipped with each of the following units (Figure 8):

- One Fuse and Filter Panel (J5D003FJ-1)
- Up to four SCUs (J4A024AB-1)
- One Fan Unit (J5D003FH-1)
- Up to two Hard Disk Units (four pairs of hard disk circuit packs; one pair for each SCU) (J4A024AC-1).

A. Fuse and Filter Panel (J5D003FJ-1)

3.17 The SCU's fuse and filter panel has been arranged to accommodate the particular loads of the SCU cabinet. Figure 9 shows the front view of the panel and the designation strips located on the underside of the flip-up panel.

3.18 The fuse and filter panel has four input feeds from a Power Distribution Frame (PDF). These four input feeds supply the seven 4-position fuse blocks. Three alarm cards are provided.

3.19 At the rear of the fuse and filter panel, there are 12 possible inputs. Each input can accept a feed from a PDF. If used, an input consists of a capacitor, cables, connectors, other hardware, and at least one output fuse block at the front of the panel. The limit of fuse blocks that can be wired to a single feed depends on the total current through the feed and the available physical space in the panel for fuse blocks. Each capacitor assembly snaps in and out of the frame, and the fuse block holders and card holders are each removable. All wiring is connectorized and the various cards unplug from the card holder.

B. The SCU(s) (J4A024AB-1)

3.20 Each SCU is a single unit with one shelf of circuit packs. Each SCU (Figure 10) has 12 circuit pack types:

- DS-120 Exchange and Interface (TN1588)
- Multifaceted Signal Processor (TN1589)
- Enhanced Peripheral Interface Controller (TN1976)
- Microstore (TN1977) or (TN9001)
- SCSI Host Adapter (TN1978)
- Voice Processor (TN1979)
- Voice Processor Interface Controller (TN1980)
- Buffer Control (TN1981)
- Buffer Fabric (TN1982)
- Table RAM (TN1983) or (TN9002)
- Extended Bus and LAN Interface (KCN4)
- Multifunctional Interface Processor (TN4001) (used only with ASR).

3.21 The SCU has two power controller types:

- Power Control (TN1984)
- Power Converter (410AA).

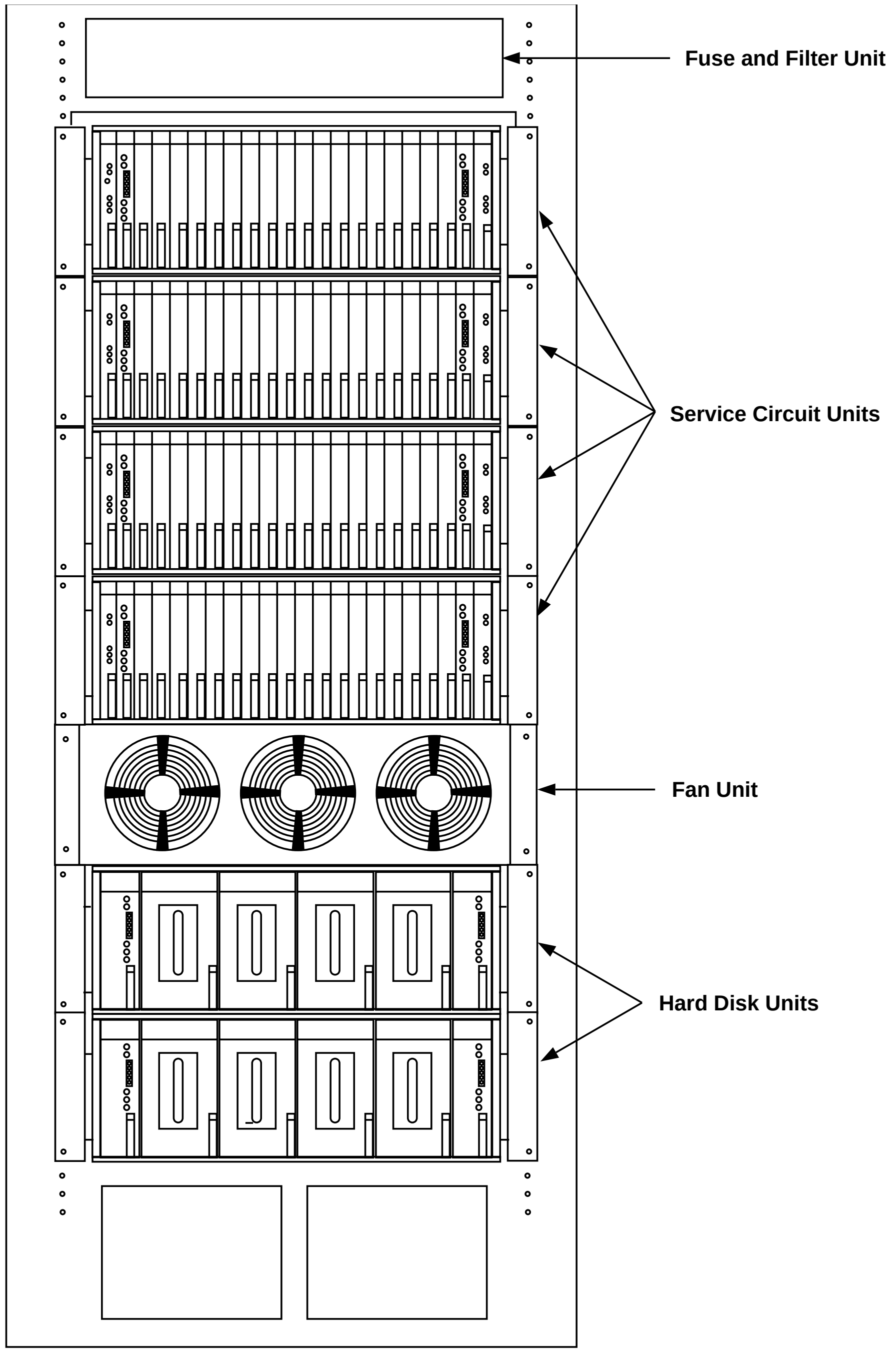

Figure 8. The SCU Cabinet (J4A024B-1) — Equipment Identification

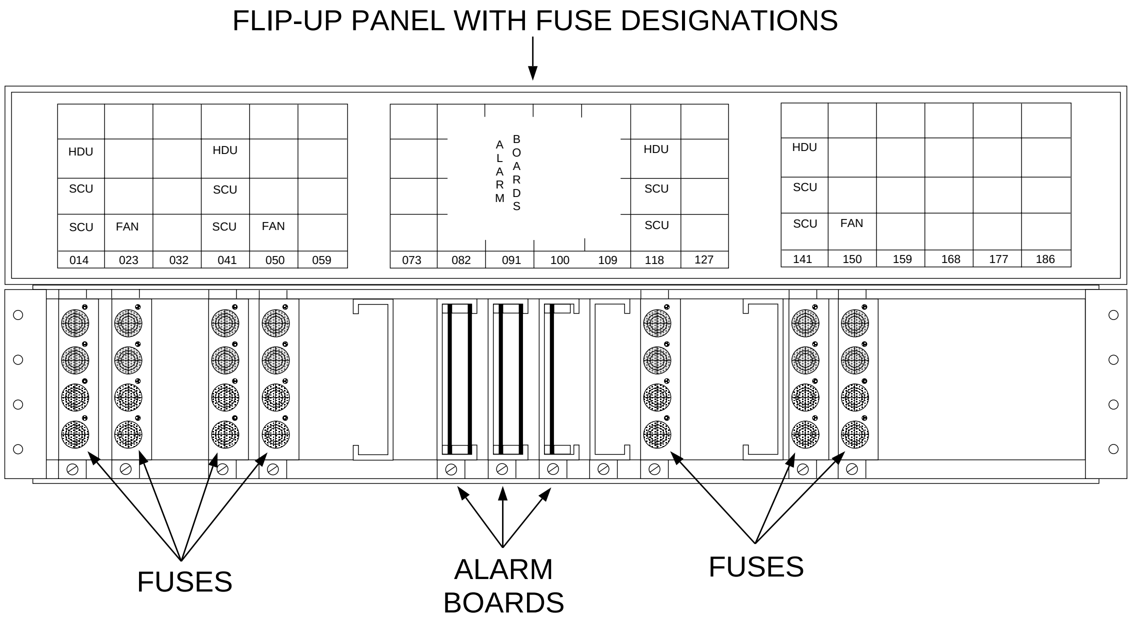

Figure 9. Fuse and Filter Panel for the SCU

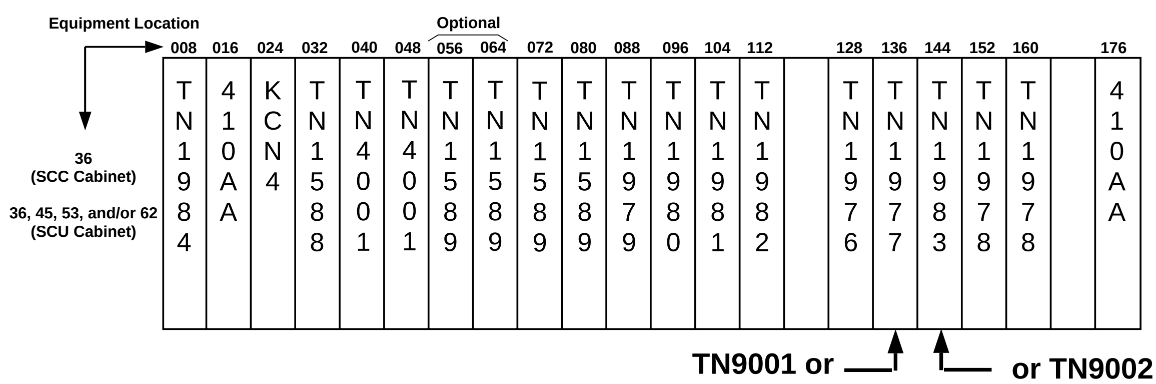

Figure 10. The SCU - Circuit Pack Locations

C. Fan Unit (J5D003FH-1)

3.22 The bidirectional fan unit contains six fans (three located on the front of the unit and three located on the rear of the unit). The fan unit helps to cool the SCU cabinet.

D. Hard Disk Units (J4A024AC-1)

3.23 Each HDU is comprised of two matched pairs of hard disk circuit packs and two power controllers. Each HDU takes up one shelf in the SCU cabinet. The SCU cabinet can be equipped with up to two HDUs (four matched pairs of hard disk circuit packs) (one pair of hard disk circuit packs associated with each SCU [Figure 8]) for a total of two complete shelves. Each HDU uses up to four hard disk circuit packs (two pairs of hard disk circuit packs) and two UN356 disk power controller circuit packs. The hard disk circuit packs available are the TN1672 (420 MB), the TN1972 (2 GB), the TN4000 (4 GB), and the TN9000 (9 GB). The UN356 circuit pack supplies +12 V and +5 V to drive the hard disk circuit packs.

The Custom Data Services Cabinet-I (CDSC-I) (J4A024C-1)

3.24 The CDSC-I is connected to an SCU to perform special signal processing functions. The cabinet contains up to five CDSU-Is. Each CDSU-I performs speech recognition for 24 channels. The CDSC-I is equipped with each of the following units (Figure 11):

- One Fuse and Filter Panel (J5D003FJ-1)
- Up to five CDSU-Is (J4A024CA-1)
- One Smart HUB (not in every CDSC-I; only one required for each set of eight CDSC-Is).

A. Fuse and Filter Panel (J5D003FJ-1)

3.25 The CDSU-I's fuse and filter panel has been arranged to accommodate the particular loads of the CDSU-I cabinet. Figure 12 shows the front view of the panel and the designation strips located on the underside of the flip-down panel.

3.26 The fuse and filter panel has five input feeds from a Power Distribution Frame (PDF). These five input feeds supply the five 4-position fuse blocks. Two alarm cards are provided, as well as one TTY card.

3.27 At the rear of the fuse and filter panel, there are 12 possible inputs. Each input can accept a feed from a PDF. If used, an input consists of a capacitor, cables, connectors, other hardware, and at least one output fuse block at the front of the panel. The limit of fuse blocks that can be wired to a single feed depends on the total current through the feed and the available physical space in the panel for fuse blocks. Each capacitor assembly snaps in and out of the frame, and the fuse block holders and card holders are each removable. All wiring is connectorized and the various cards unplug from the card holder.

B. The CDSU-I(s) (J4A024CA-1)

3.28 Each CDSU-I is a single unit occupying one shelf of the CDSC-I. Each CDSU-I (Figures 13, 14, and 15) consists of the following:

- One 486 Processor Card (WP-92304L301 CAT 1012) manufactured by Diversified Technology Inc.
- One Hard Disk Drive (WP-92304L304)
- One Ethernet LAN Interface Card (WP-92304L306)
- One Super Video Graphics Adapter (SVGA) Card (WP-92304L307)
- One SCSI Card (WP-92304L304)
- Twelve AYC50 Speech Processing Cards
- Two T1 Interface Cards (WP-92304L302)
- One Control Module
- One Power Module
- Three Fans.

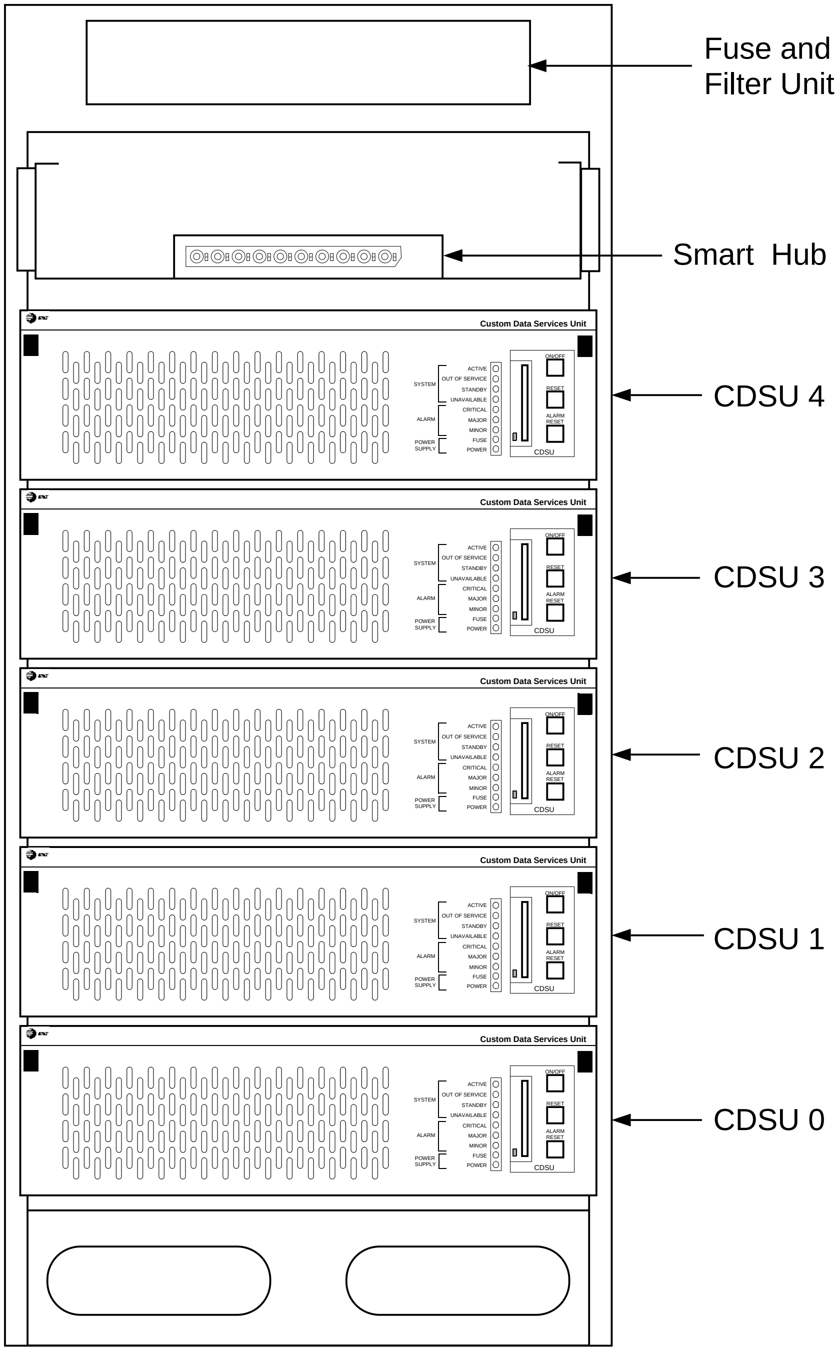

Figure 11. CDSC-I (J4A024C-1)

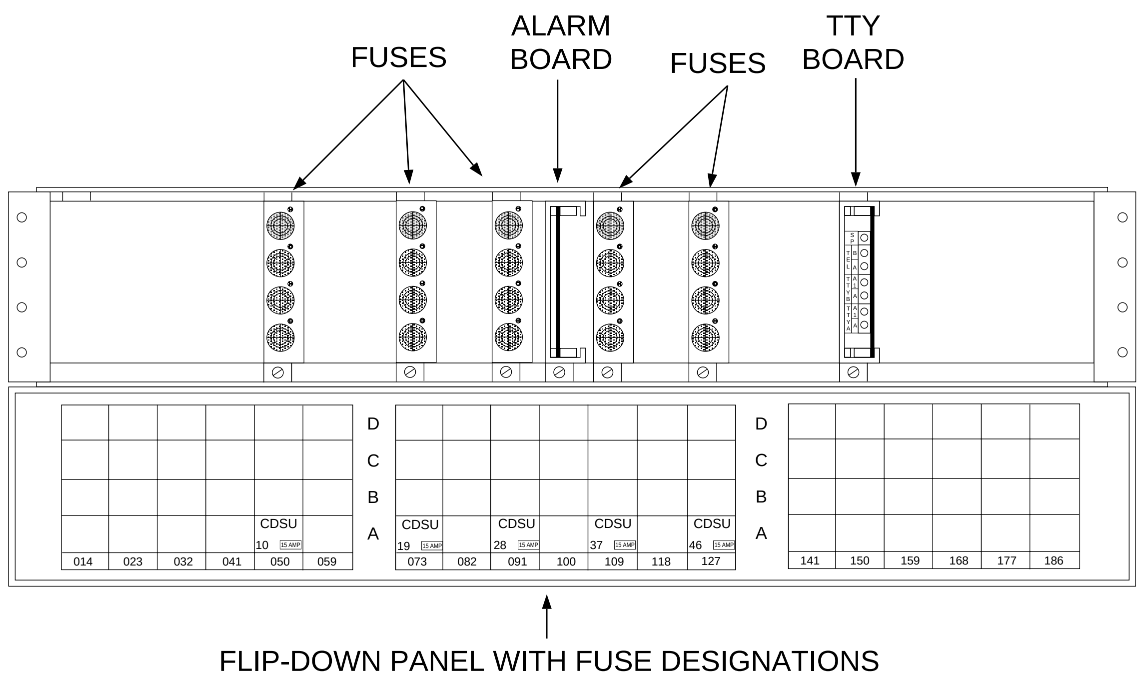

Figure 12. Fuse and Filter Panel for the CDSC-I

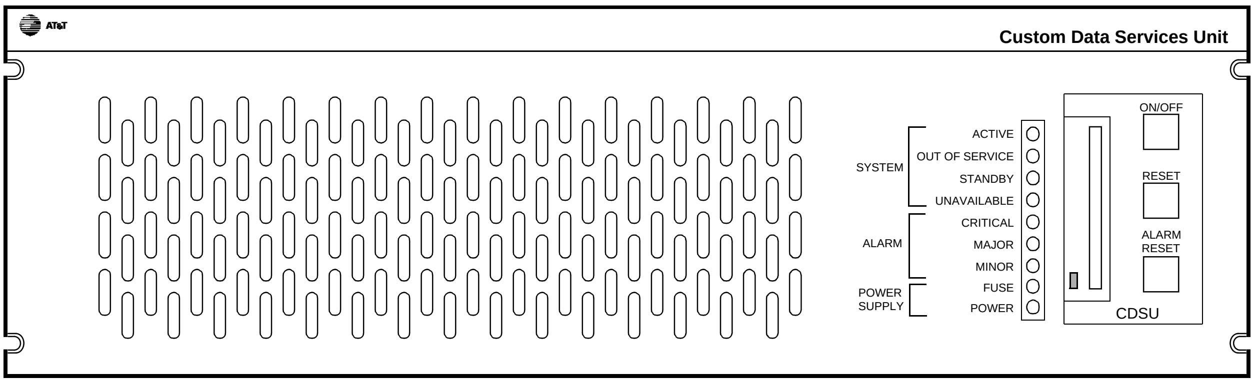

Figure 13. CDSU-I (Front View)

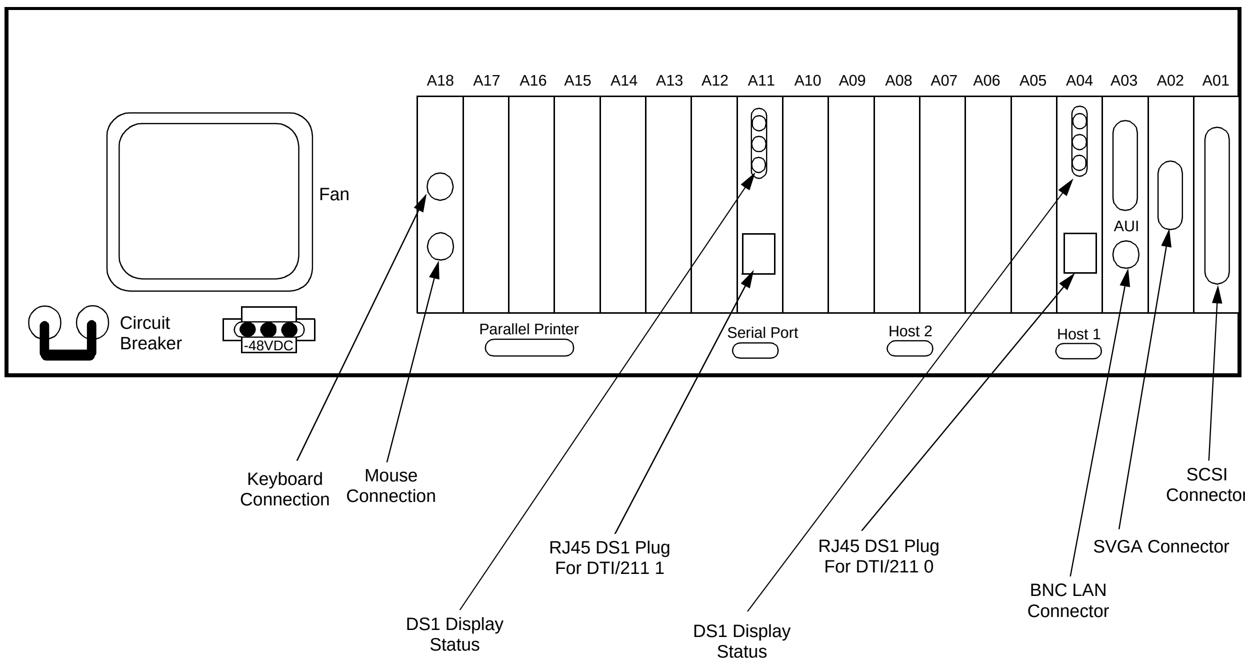

Figure 14. CDSU-I (Rear View)

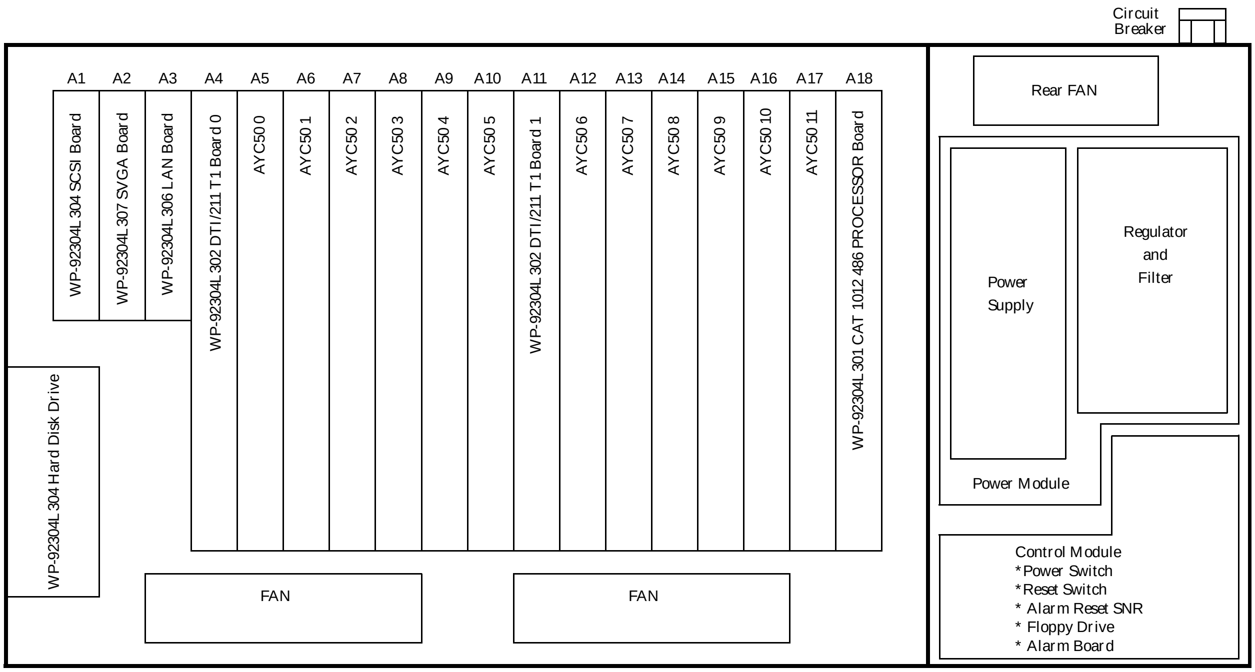

Figure 15. CDSU-I (Top View)

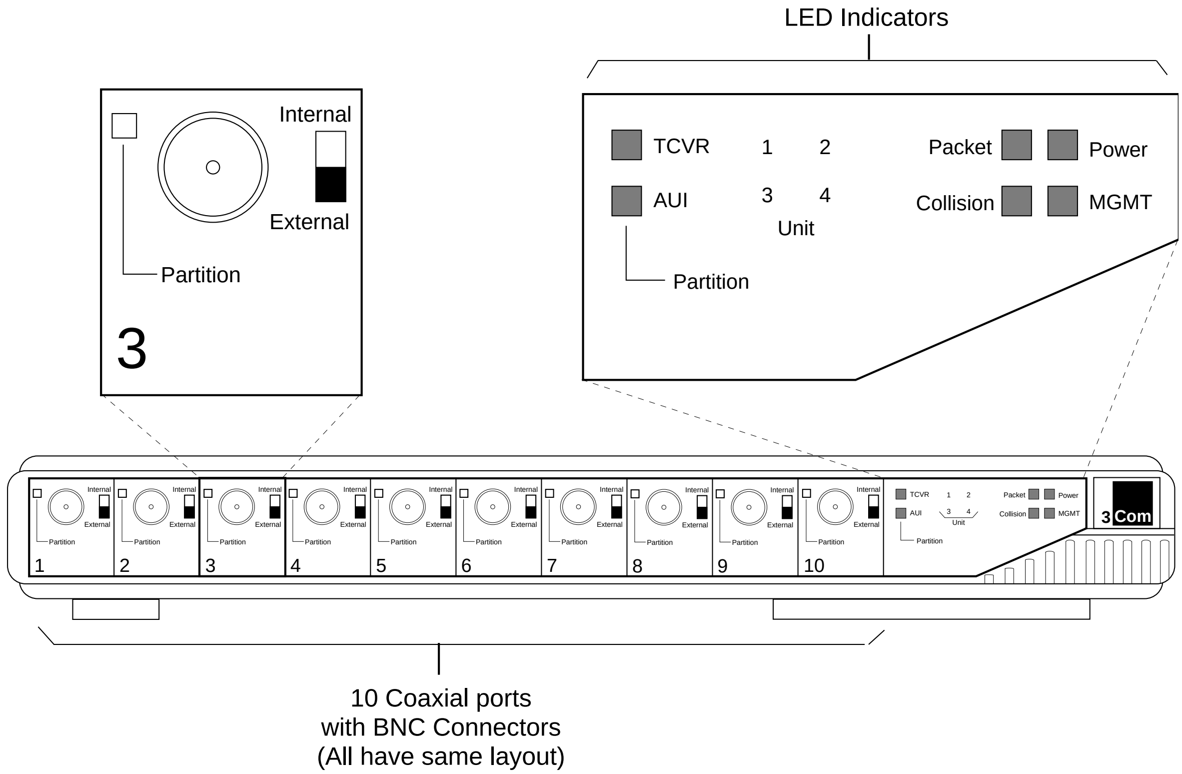

Figure 16. Smart HUB

C. Smart HUB

3.29 The Smart HUB (Figure 16) is a *LinkBuilder** Flexible Media Stack (FMS) Coaxial HUB. The Smart HUB, located in the CDSC-I, is used to connect the AAP to the CDSC-Is. The Smart HUB has various status Light Emitting Diodes (LEDs) and 10 Thin Ethernet ports on the front panel which are used to provide these connections. One of these ports is used for the AAP connection and optional connection to another Smart HUB. Eight of the ports can be used for CDSC-I connections. One port is not used. One Smart HUB port is used for each CDSC-I. Since one Smart HUB can be used to provide LAN connections to multiple CDSC-Is, a Smart HUB is not required at every CDSC-I.

3.30 The Smart HUB conforms to the Institute of Electrical and Electronics Engineers (IEEE) 802.3 standard for LAN repeaters and provides the following functions:

- Signal Retiming and Amplification
- Preamble Regeneration
- Fragment Extension
- Automatic Partition/Reconnection.

* Registered trademark of 3Com Corporation.

The Custom Data Services Cabinet-II (CDSC-II) (J4A024D-1)

3.31 The CDSC-II is connected to an SCU to perform special signal processing functions. The cabinet contains up to four CDSU-IIs. Each CDSU-II performs speech recognition for 60 channels. The CDSC-II is equipped with each of the following units (Figure 17):

- One Fuse and Filter Panel (J5D003FJ-1)
- Up to four CDSU-IIs (J4A024DA-1)
- One Smart HUB (not in every CDSC-II; only one required for each set of four CDSC-IIs).

A. Fuse and Filter Panel (J5D003FJ-1)

3.32 The CDSU-II's fuse and filter panel has been arranged to accommodate the particular loads of the CDSU-II cabinet. Figure 18 shows the front view of the panel and the designation strips located on the underside of the flip-down panel.

3.33 The fuse and filter panel has six input feeds from a Power Distribution Frame (PDF). Each of these six input feeds supplies a four-position fuse block. Four of these fuse blocks are used for the four CDSU-IIs. The other two fuse blocks are spares. Each fuse block has four fuse positions (A, B, C, and D). Only the "A" position is used. An alarm card is also provided, as well as a TTY card.

3.34 At the rear of the fuse and filter panel, there are 12 possible inputs. Each input can accept a feed from a PDF. If used, an input consists of a capacitor, cables, connectors, other hardware, and at least one output fuse block at the front of the panel. The limit of fuse blocks that can be wired to a single feed depends on the total current through the feed and the available physical space in the panel for fuse blocks. Each capacitor assembly snaps in and out of the frame, and the fuse block holders and card holders are each removable. All wiring is connectorized and the various cards unplug from the card holder.

B. The CDSU-II(s) (J4A024DA-1)

3.35 Each CDSU-II is a single unit occupying one shelf of the CDSC-II. Each CDSU-II (Figures 19, 20, and 21) consists of the following:

- One *Pentium** Enhanced Industry Standard Architecture (EISA)/Peripheral Controller Interface (PCI) Processor Board
- One Hard Disk Drive
- One Ethernet LAN Interface Board
- One PCI SVGA Video Board
- One PCI SCSI Interface Board
- Five BYC51 Speech Processing Cards
- One AYC52 T1 Interface Card
- One AYC53 Echo Cancellation Card
- One Control Module
- One Power Module
- Three Fans.

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* Registered trademark of Intel Corporation.

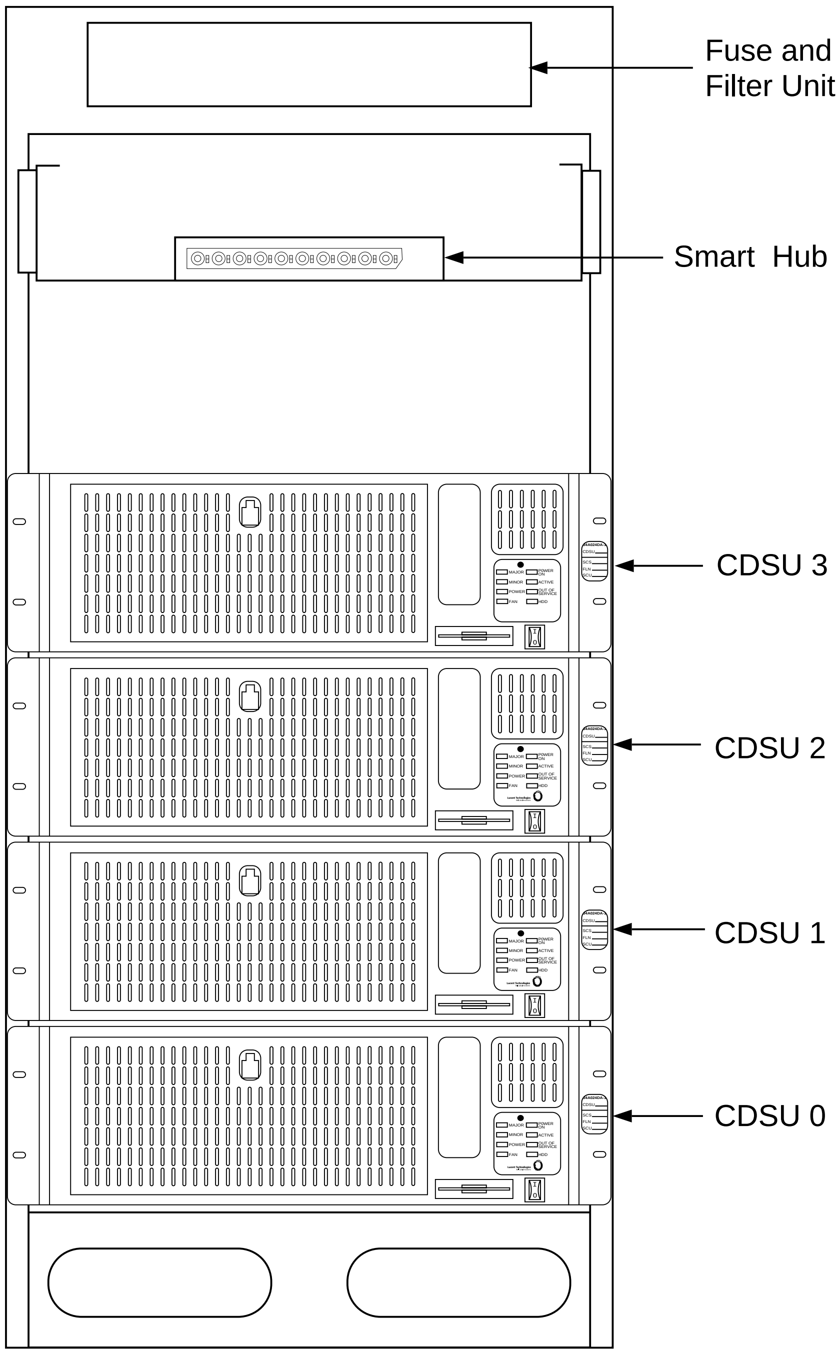

Figure 17. CDSC-II (J4A024D-1)

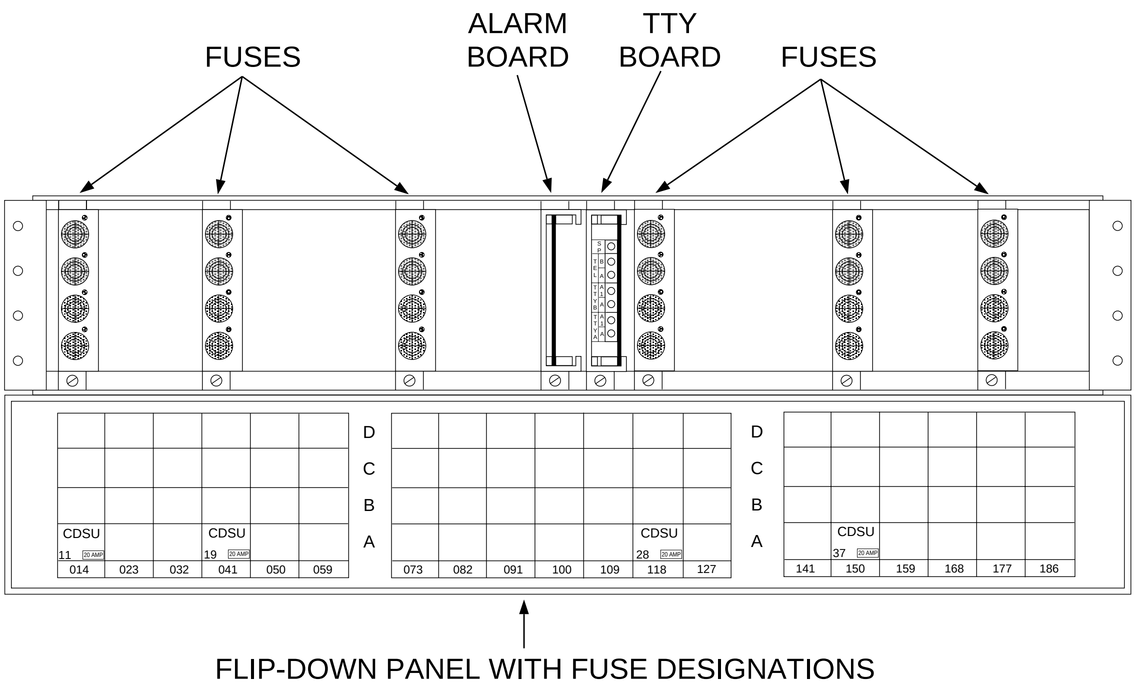

Figure 18. Fuse and Filter Panel for the CDSC-II

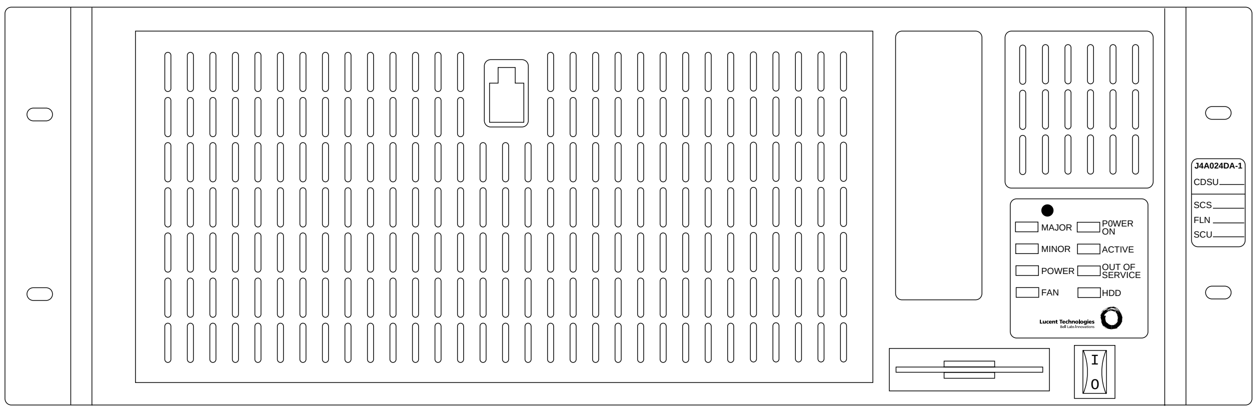

Figure 19. CDSU-II (Front View)

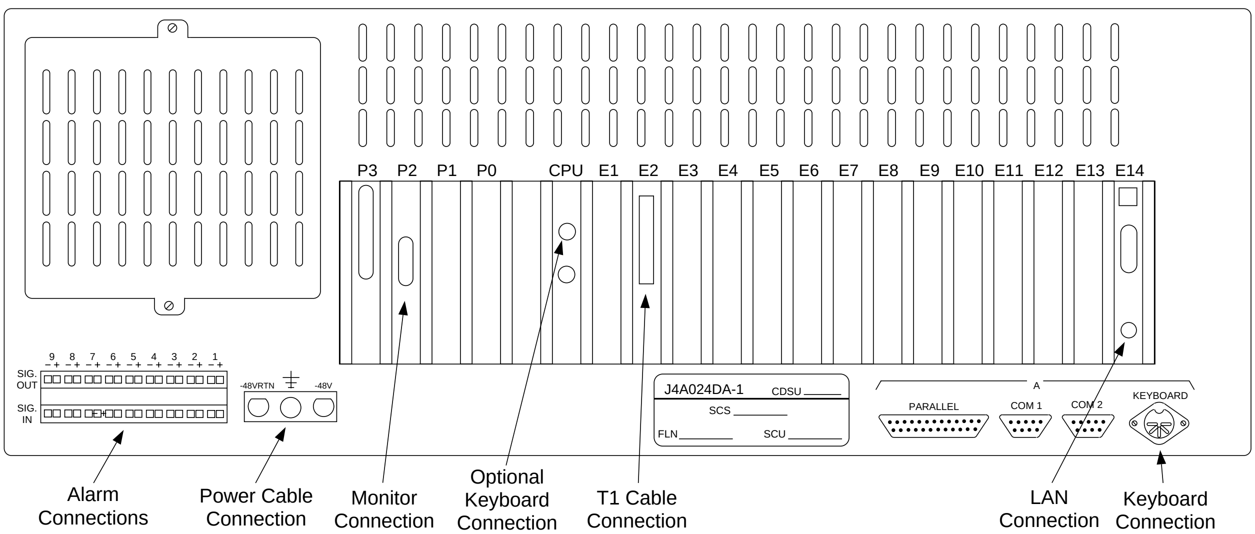

Figure 20. CDSU-II (Rear View)

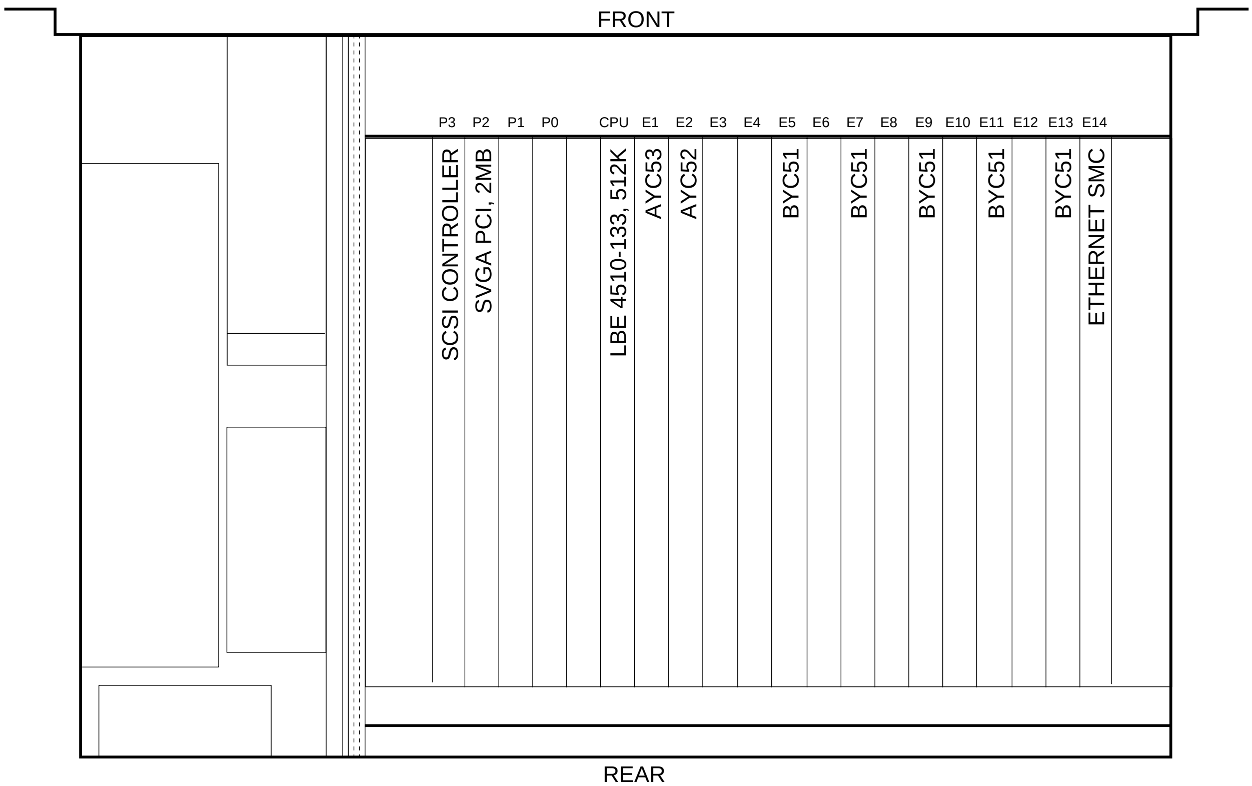

Figure 21. CDSU-II (Top View)

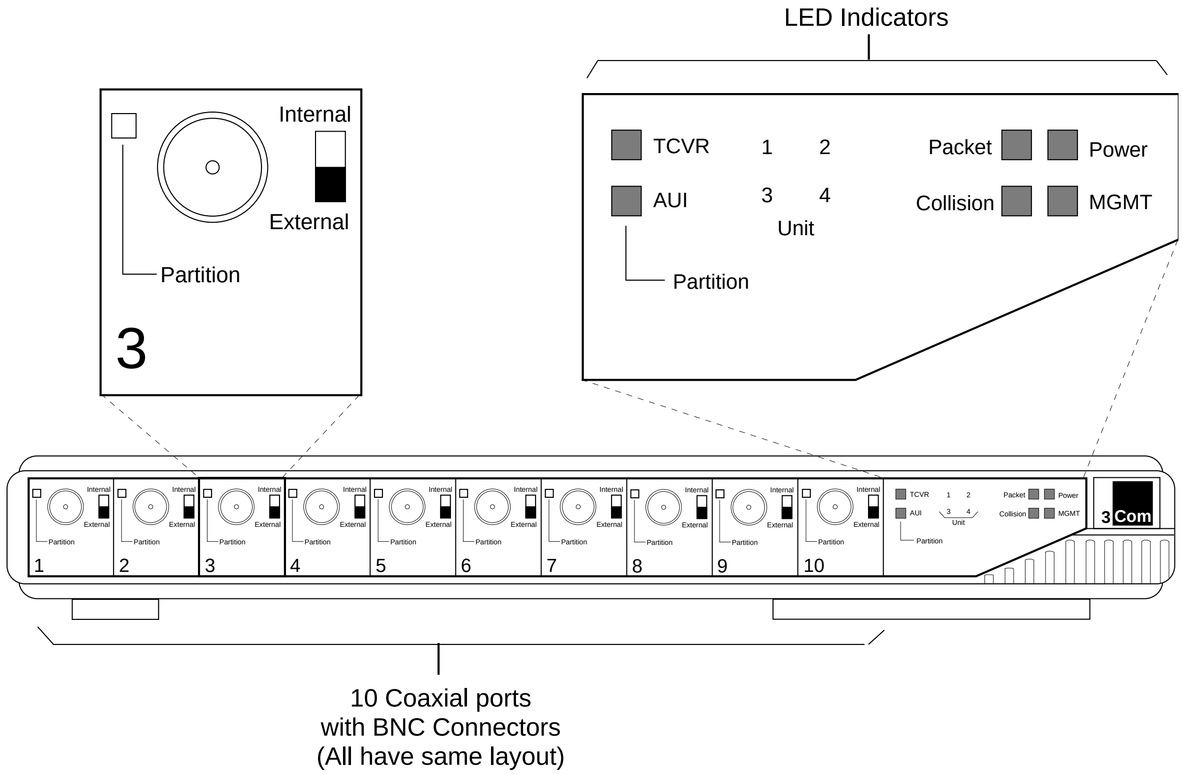

Figure 22. Smart HUB

C. Smart HUB

3.36 The Smart HUB (Figure 22) is a *LinkBuilder* Flexible Media Stack (FMS) Coaxial HUB. The Smart HUB, located in the CDSC-II, is used to connect the AAP to the CDSC-IIs. The Smart HUB has various status LEDs and 10 Thin Ethernet ports on the front panel which are used to provide these connections. One of these ports is used for the AAP connection and an optional connection to another Smart HUB. Eight of the ports can be used for CDSC-II connections. One port is not used. One Smart HUB port is used for each pair of CDSU-IIs. Therefore, two Smart HUB ports can be used for each CDSC-II. Since one Smart HUB can be used to provide LAN connections to multiple CDSC-IIs, a Smart HUB is not required at every CDSC-II.

3.37 The Smart HUB conforms to the IEEE 802.3 standard for LAN repeaters and provides the following functions:

- Signal Retiming and Amplification
- Preamble Regeneration
- Fragment Extension
- Automatic Partition/Reconnection.

4. Functional Description

Introduction

4.01 This section provides a functional description of the SCS cabinets and units housed within the frames. The following subjects are included in this section:

- General description of SCS functions
- Functional description of SCS cabinets, units, and circuit packs.

General

4.02 As more customer features are implemented, expanded, and improved on the *4ESS* switch, more announcement and information collection capability is needed. The SCS, as an adjunct to the *4ESS* switch, is designed to provide these announcements and information collection functions. In addition, the SCS provides these functions with high reliability and performance, at a relatively low cost.

4.03 As described previously in the "Physical Description" section of this practice, the SCS is composed of two or three cabinet types: the SCC cabinet (shown in Figure 4), the SCU cabinet (shown in Figure 8), and (optionally) the CDSC-I (shown in Figure 11) or the CDSC-II (shown in Figure 17). Each cabinet has various units which may occupy one or more shelves in the cabinet. Each unit contains a variety of circuit packs. For the location of the various units and circuit packs, see the "Physical Description" section of this practice.

4.04 The remainder of this section describes how the various units and their corresponding circuit packs function.

Service Circuit Controller Unit (J4A024AA-1)

4.05 The SCC is basically a fast, microprogrammed processor that performs instruction decoding, buffering, interrupt service, and control register operations. Its main task is to translate between the format of the messages that the CC sends over the PUB and the format that the SCUs require. The SCC then routes the resulting messages to the correct destination. The SCC also provides error detection and some fault recovery for the SCUs.

4.06 The SCC microword has 64 bits (plus 8 parity bits) divided into 17 control fields. Three 32-bit buses (two source and one destination) carry data to and from the Arithmetic/Logic Unit (ALU). Up to 64 registers can be accessed by the SCC's UN351 or UN591 Executive Processor (EXEC) circuit pack.

4.07 Figure 23 shows the SCC unit architecture. As shown in Figure 23, all SCC subsystems are duplicated for fault tolerance purposes. A pair of system buses interconnects all the subsystems. Interfaces are connected to the buses to allow the connection of the PUB, the optical EB, and future control interfaces. Some RAM is available on each UN351 or UN591 EXEC circuit pack, and much larger Global RAMs are connected to the bus.

4.08 The SCC contains the following circuit pack types:

- Peripheral Unit Bus Driver/Receiver (UN349)
- Peripheral Unit Bus Interface (UN350)
- Executive Processor (UN351 or UN591)
- Global RAM (UN352)
- Extended Bus Interface (KCN3)

- BTL Bus Terminator (UN357)
- Integrated Power Controller (TN1671)
- Power Control (TN1984)
- Power Converter (410AA).

A. Executive Processor (UN351)

4.09 The executive processor circuit pack is the SCC's main processor. A block diagram of the executive processor is shown in Figure 24. Three 32-bit buses carry operands between the various sources and destinations. These buses are protected by four parity bits each, for a total bus width of 36. The top portion of Figure 24 is the data path of the control processor, the center is the memory control subsystem, and the bottom is the sequencing logic.

4.10 In addition to the paths shown to the three main 32-bit buses, many side paths exist to carry operands during special operations like subroutine calls and interrupt service. Control signals from the sequencer logic direct the latching of data from the buses, selection of registers, memory access modes, and condition code select. Other control signals drive the ALU opcode and shifter control inputs. The individual bit fields in the microword are directed as control signals to the rest of the processor.

4.11 The ALU, which is duplicated on each UN351 circuit pack, is a single chip manufactured by Monolithic Memories Inc. The 29332 chip is a large combinational logic element that can perform many arithmetic and logic functions on two 32-bit operands and can generate a 32-bit result in a single instruction.

4.12 In addition to the ALU, the data path includes several registers that have full access to the buses. Memory offset fields in the microword select which register(s) is to be read and/or written.

4.13 Fifteen scratch registers are available to store global values that the processor needs to access quickly at all times.

4.14 The timer register can be read and cleared by the processor, and is automatically decremented by the system clock (or an external time base). If the timer reaches zero, an interrupt is generated. Watchdog timer functions and the scheduler's software clock use the timer register.

4.15 Two different types of hardware interrupts are processed through the interrupt register; one of these summarizes the 128 interrupts originating on the Peripheral Unit Bus Interface (PUBI) circuit pack that corresponds to the set of opcodes received in messages from the 1B Processor CC. A second type provides a synchronized interrupt when hardware errors occur. There are two ways to temporarily disable all interrupts (hardware and PUBI): by setting a global interrupt disable bit in the interrupt register or by setting a bit in the microword, allowing the creation of sequences of uninterruptible instructions.

4.16 A control and status register has some readable/writable bits and some read-only bits. Status signals that reflect many conditions in the controller are read through this register. Setting special bits in the control and status register simulate SCC error conditions, such as parity errors in order to test the parity checkers. The interrupt vector is latched during an interrupt in the control and status register so that it is readable by software. Spare bits can be used in the future as general purpose input/output bits.

4.17 The executive processor's local RAM is used as a register file to implement the 15 scratch registers for local variables and for stack operations. Since the local RAM is located on the same circuit pack as the ALU and data path, it can be accessed quickly. See Figure 26 for details of the local RAM control circuits. The executive processor also controls the Global RAM which is discussed later in more detail.

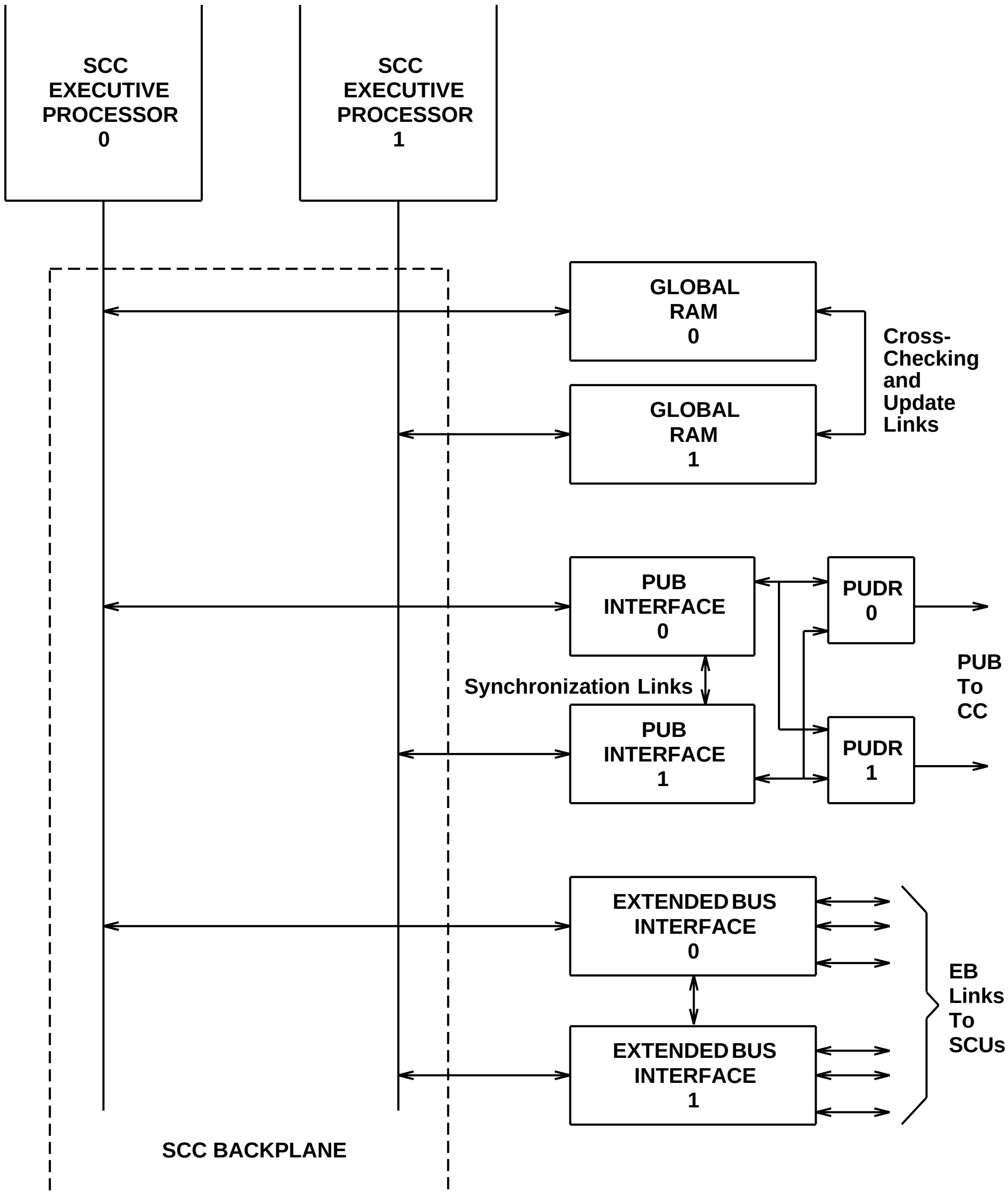

Figure 23. The SCC Architecture

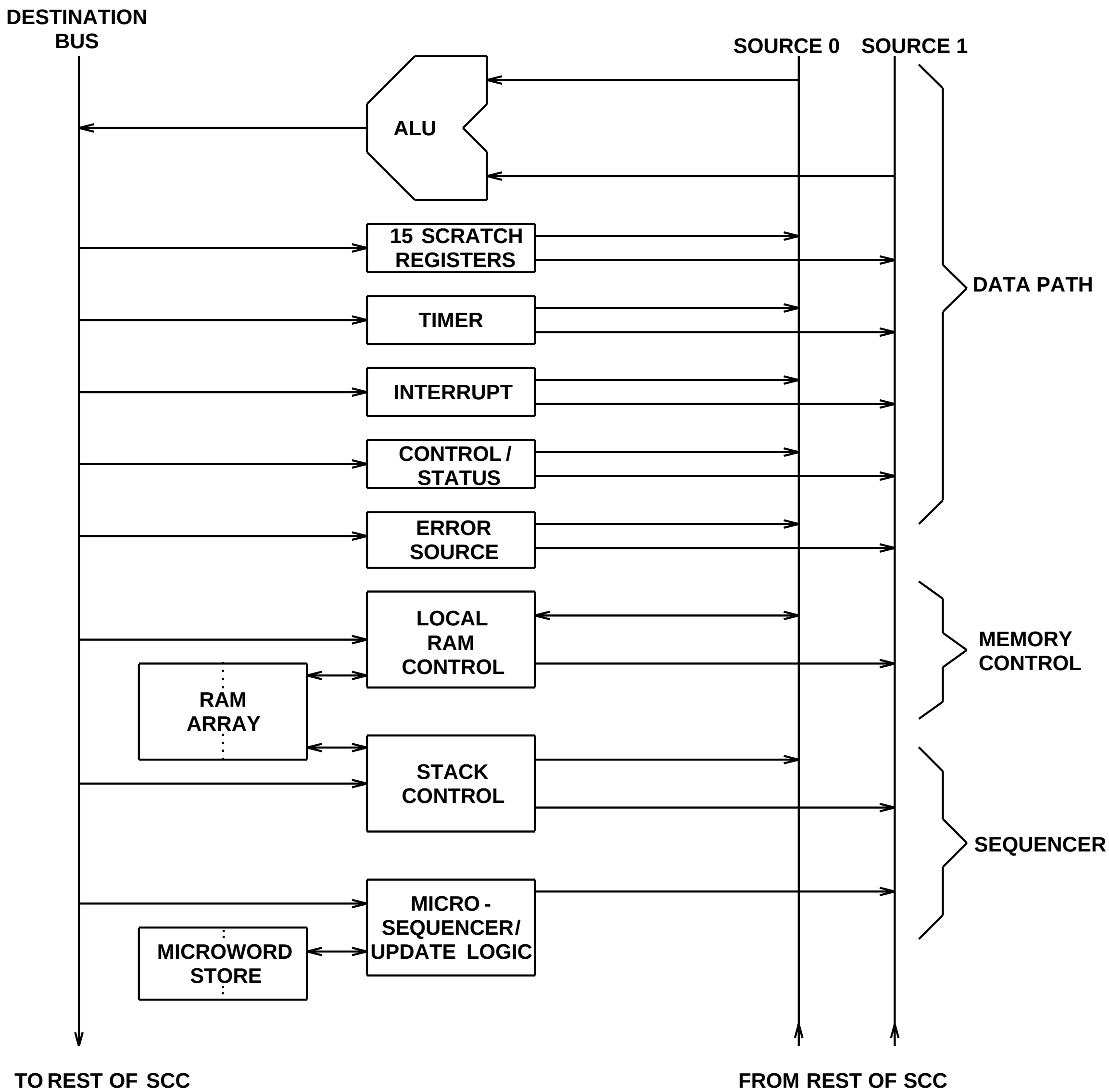

Figure 24. Executive Processor (UN351)

4.18 The microsequencer section of the controller is responsible for providing the timing and branch control. A microaddress register generates an address to a 64 K by 64-bit wide micro-RAM. The first 16 K by 64-bit wide portion of the micro-RAM is initialized from Read Only Memory (ROM) chips at power-up or hard reset. The remaining 48 K by 64-bit portion of the micro-RAM must be initialized from the SCU disk or the other SCC before it can be used. Eight additional bits provide parity to the microword. Microinstructions from the micro-RAM are decoded into bit fields and distributed as control signals to the rest of the controller.

4.19 There are two different interrupt vector tables. One starts at micro-RAM address 0 and runs for 256 instructions. The other is in the highest addressable 256 words of micro-RAM. A bit in the control/status register determines which interrupt vector table is to be used. Power cycling or a hard reset of the controller causes the table at address 0 to be used.

4.20 The three operand buses and their parity bits, along with mode and offset signals, are directed to the SCC backplane. Registers in the interface boards installed in the SCC access these signals to provide read/write paths to the controller. Some circuit pack locations in the backplane receive all three operand buses, while others receive only the destination bus and source bus A. Circuit packs installed in slots of the later type can only be addressed to read data to the A bus.

B. Executive Processor (UN591)

4.21 The UN591 along with the UN352 Global RAM circuit pack and various I/O packs makes up the processor complex needed to decode orders arriving on the PUB from the central controller, and manage the entire operation of the TSI. The UN591 has the ability to operate in lockstep as a duplex pair, to locate faults when they develop, and to undergo repairs to a faulty processor in the pair while its mate continues to process calls.

4.22 The UN591 (Figure 25) is a three-bus microcoded machine. On the UN591, a 64-bit microword controls the datapaths. The three data buses are each 32 bits wide, and have 4 parity bits each. The source A and source B buses bring operands to the ALU. A destination bus carries the results of the arithmetic and logical operations from the ALU to the rest of the system. Seven bits of the microword control which operation the ALU will perform. Additional bits in the microword control subroutine calls, branching, and access to the RAMs and immediate data.

C. Peripheral Unit Bus Driver/Receiver (UN349) and Peripheral Unit Bus Interface (UN350)

4.23 Connections between the SCC backplane buses and the PUB are made by the PUBI circuit pack and the Peripheral Unit Bus Driver/Receiver (PUDR) circuit packs. Each of the duplicated PUBs is terminated on its own set of four PUDR circuit packs. The PUDR circuit packs have coupling transformers, bus drivers and bus receivers, as well as configuration control logic. The signals are sent over the backplane to one PUBI circuit pack in each half of the SCC. Crossover signals in the backplane connect PUDR signals between controllers, so the system remains operational if either a PUB or a PUDR circuit pack fails.

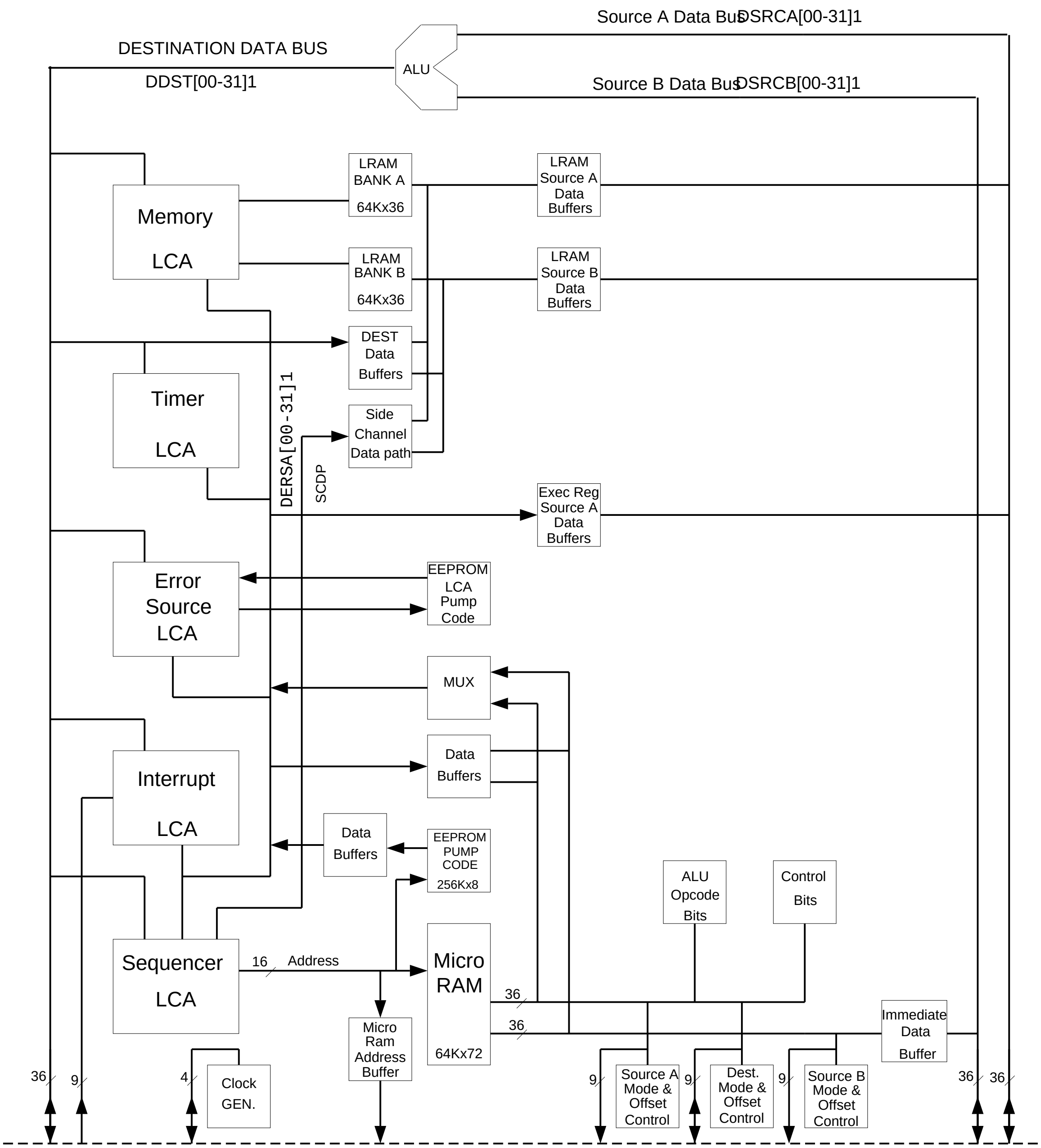

Figure 25. Executive Processor (UN591)

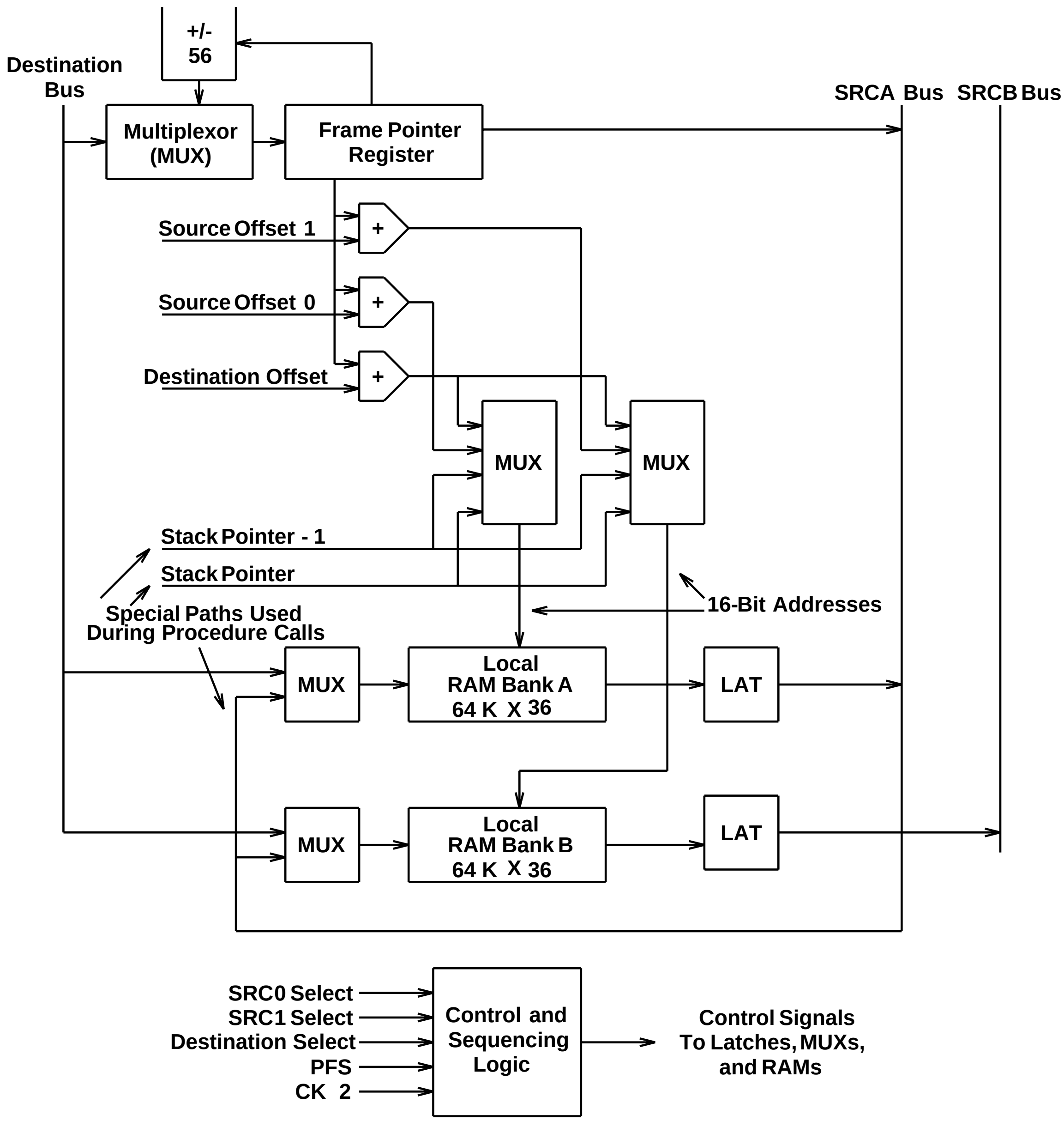

Figure 26. Local RAM Control Logic

4.24 The PUBI circuit pack contains logic to recognize when the SCC is being addressed by the 1B Processor CC. The PUBI circuit pack also contains much of the SCC's error processing circuitry and the registers that allow the 1B Processor CC to perform maintenance and configuration control.

4.25 The PUDR circuit packs are powered from a separate power supply, so the PUB power domain is isolated from the SCC. The PUBs loop through the SCC backplane, so backplane-mounted series resistors ensure that the PUBs remain electrically connected if a PUDR is pulled for repair.

4.26 To allow polling of the SCC's buffers, **the SCCs must be placed on a PUBB with the extended buffer polling option**. The extended buffer polling option expands the 1B Processor CC's buffer polling capabilities on a specific PUBB. Replies to the extended buffer polling on the SCCs are on bits 8 through 15 of the PURB. Additional information on extended buffer polling and its requirements can be found in 234-110-010, *Peripheral Unit Bus System, Description, 4ESS Switch*.

D. Global RAM (UN352)

4.27 Two different memory systems exist in the SCC. One is called local RAM, and is located on the executive processor circuit pack. The other is the much larger Global RAM, which is on the UN352 Global RAM circuit pack connected to the PUB. The Global RAM is used to hold tables and other data structures. Global RAM capacity is 256 K 32-bit words with byte parity.

4.28 The Global RAM circuit pack includes a parity checker for the destination bus that detects backplane faults. It also has parity checkers for the mode and offset addressing fields for all three buses. Zero drivers on the Global RAM circuit pack ensure that the backplane is driven with correct idle states when no data is being sent on the source buses.

4.29 The Global RAM circuit pack is also the location of the cross-checking logic between controllers. In normal operation, the two SCCs making up a duplex controller are running independently, but in lockstep. Checking logic on the Global RAM circuit packs compares a set of 8 syndrome bits that are calculated by both SCCs, and detects any mismatches. These mismatches usually indicate a hardware fault and require the performance of diagnostic tests.

4.30 Once the diagnostics have been run and the system is repaired, crossover logic on the Global RAM circuit pack assists in restoring the lockstep state between the two controllers. The destination bus on the good controller is crossed over to the newly repaired half through the backplane. All writes on the good half also drive the destination bus on the other controller, effectively writing all results to both SCCs. The good controller performs a background read and write-back of the micro-RAM that is not initialized from ROM chips, all of its local RAM, Global RAM, and registers. The crossover effectively copies the context of the good controller to the restored controller. In a few seconds, the background copy is complete, the good controller has still been processing calls and updating context in the other controller, so all the storage on both processors should be identical.

4.31 Global RAM control logic is shown in detail in Figure 27.

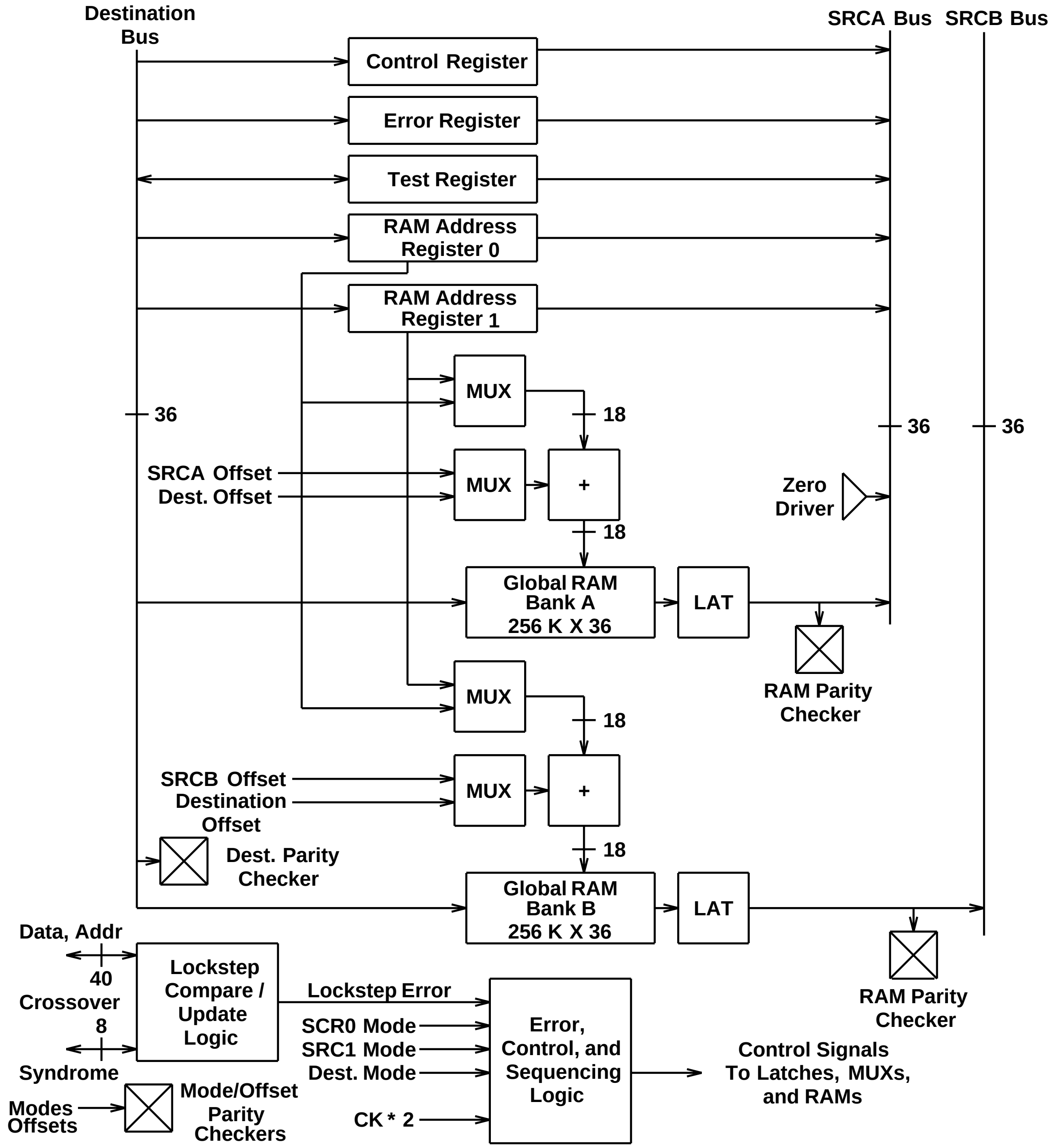

Figure 27. Global RAM (UN352)

E. Extended Bus Interface (KCN3)

4.32 High-speed extended buses interconnect the SCC unit with the SCUs. Initially, eight channels of the extended bus are terminated on each Extended Bus Interface (EBI) circuit pack. With two circuit packs per SCC, this gives 16 EB channels per SCC for a total of 32 links on a duplex SCC. This bus is a bidirectional, fiber-optic, point-to-point link operating at 100 Mbps.

4.33 Several registers are found on the EBI circuit pack. There are two data registers, one to receive 32-bit data from the SCC controller and one to buffer data received from the SCUs. A control register holds addressing and command information that is transmitted along with the 32-bit data to the SCU. A status register holds error bits to report parity and protocol violation errors, sequencer control bits, and SCU status information.

4.34 An address register is written to control to which one of the EBI channels the other registers will refer. This register exists on both EB boards, but is active only on the EB board in the first backplane slot. This means that when the SCC processor reads or writes the address register, only the register on the board in that first slot will respond. A narrow bus running from this board to the other EB board provides the other board with the address contained in this register. Backplane straps determine which EB board has the active address register; both EB boards are identical.

F. The Backplane Transceiver Logic (BTL) Bus Terminator (UN357)

4.35 The UN357 provides backplane termination for the BTL that is employed by the SCC. The SCC backplane is made up of 139 BTL signals. There are three 45-bit buses (32 bits of data, 8 bits of address and 5 bits for parity) and 4 clock signals.

4.36 Each BTL signal is terminated at both ends of the bus with a single 39-ohm resistor connected to an active voltage source of 2.1 volts. The power supply load resistors supply a constant 10 percent load to the 2.1 volt power supply. This load is needed for the power supply to behave properly when transitioning from no load to full load.

4.37 The UN357 has two voltage sensing resistors. When the UN357 is inserted into the SCC unit, a 147-ohm resistor is placed in parallel with the other UN357 circuit pack and the UN352 GRAM circuit pack to provide a 49-ohm load. The TN1984 power control pack uses this to sense and correct the 2.1 voltage at the power converter. At the same time, a 100-ohm resistor is placed in parallel with the other UN357 circuit pack to provide a 50-ohm load that the TN1984 power control pack uses as an input for its voltage monitoring lead.

4.38 Three capacitor types are used in the UN357. The 0.1 μF capacitors are used to filter higher frequency components out of the supply voltage. The 47 μF capacitors are used to filter midrange frequency components out of the supply voltage. The 220 μF capacitors are used for bulk storage of energy that is needed when the supply load has a large transition. These capacitors provide about 4000 μF of capacitance for the circuit pack.

4.39 The power requirement for the UN357 circuit pack is approximately 10 watts.

G. Integrated Power Controller (TN1671)

4.40 The TN1671 integrated power controller circuit pack provides +24 volts and +5 volts to the four UN349 PUDR circuit packs in each SCC unit. The TN1671 has onboard voltage monitors that detect out-of-range voltages, protecting the wiring of both the UN349 and the backplane. If a fault occurs, the TN1671 shuts down within milliseconds while reporting status via scan leads to the *4ESS* switch. The design enables the user to power the unit up or down, and remove or restore the unit to service. Onboard diagnostics may be activated on the front panel or invoked by software from the *4ESS* switch.

H. Power Control (TN1984)

4.41 The TN1984 power control circuit pack provides a means of powering an SCC up or down and reporting power status via scan leads to the *4ESS* switch. The design has provisions for monitoring eight 15-amp current branches with two 410AA power converter circuit packs as the source. Each branch is monitored for overcurrent protection and will trigger an alarm if this condition exists. The TN1984 offers programmable current monitoring by simply shorting designated pins on the backplane. It also offers over and under voltage monitoring for out-of-range voltage conditions. In addition to controlling eight 5-volt branches, the circuit pack also has a 2-volt, onboard converter, supplying branch terminator power to the SCC. Onboard diagnostics may be exercised manually or via software from the *4ESS* switch. The TN1984 also generates alarms for the SCC and SCU.

I. Power Converter (410AA)

4.42 The 410AA power converter circuit pack is a 5-volt converter capable of supplying 60 amps from a -48 volt input. A remote on/off circuit may be used if a controller, such as a TN1984 is used in conjunction with the 410AA. The 410AA also has programmable overcurrent protection along with an overvoltage shutdown circuit.

Service Circuit Unit (J4A024AB-1)

4.43 An SCS can have up to 16 SCUs. Each SCU provides the following capabilities:

- 120 channels of service circuits
- Eight maintenance channels
- Either 420 MB, 2 GB, 4 GB, or 9 GB of storage (disk based)
- 65,535 announcement numbers
- Announcements up to 261 seconds long in 1.024-second increments
- The ability to concatenate/queue up to 32 announcements together
- Short, high use announcements can be stored in RAM in increments of 0.128 seconds
- At least 512 seconds of RAM-based announcement storage for short and frequently used announcements
- Announcements that are interruptible on customer input
- Announcements that are continuously played (such as phased announcements)
- Average announcement latency of less than 0.5 seconds
- Multifaceted Signal Processor (MSP) based digit receiver hardware with software downloadable algorithms
- DTMF receivers that use Linear Predictive Coding (LPC) techniques to maximize talk-off immunity (the ability to avoid falsely recognizing DTMF digits during conversations)
- Dedicated buffer memory for each voice channel for playing announcements, so separate channels can have different announcements playing simultaneously
- Hardware to increase system reliability, such as a sanity timer, parity bits, and so forth.

4.44 Figure 28 shows the SCU architecture. The SCU receives control messages from the SCC over the EB fiber-optic cables. The messages are buffered on a KCN4 Extended Bus and Lan Interface (EBLI) circuit pack. The SCU processor copies the messages to table RAM, then carries out the requested operation. If an announcement playback is requested, a disk controller circuit pack starts a seek operation to locate the ADaptive Pulse Code Modulation (ADPCM) encoded announcement on one of the disk drives. The announcement data is then transferred from the disk drive to a buffer memory.

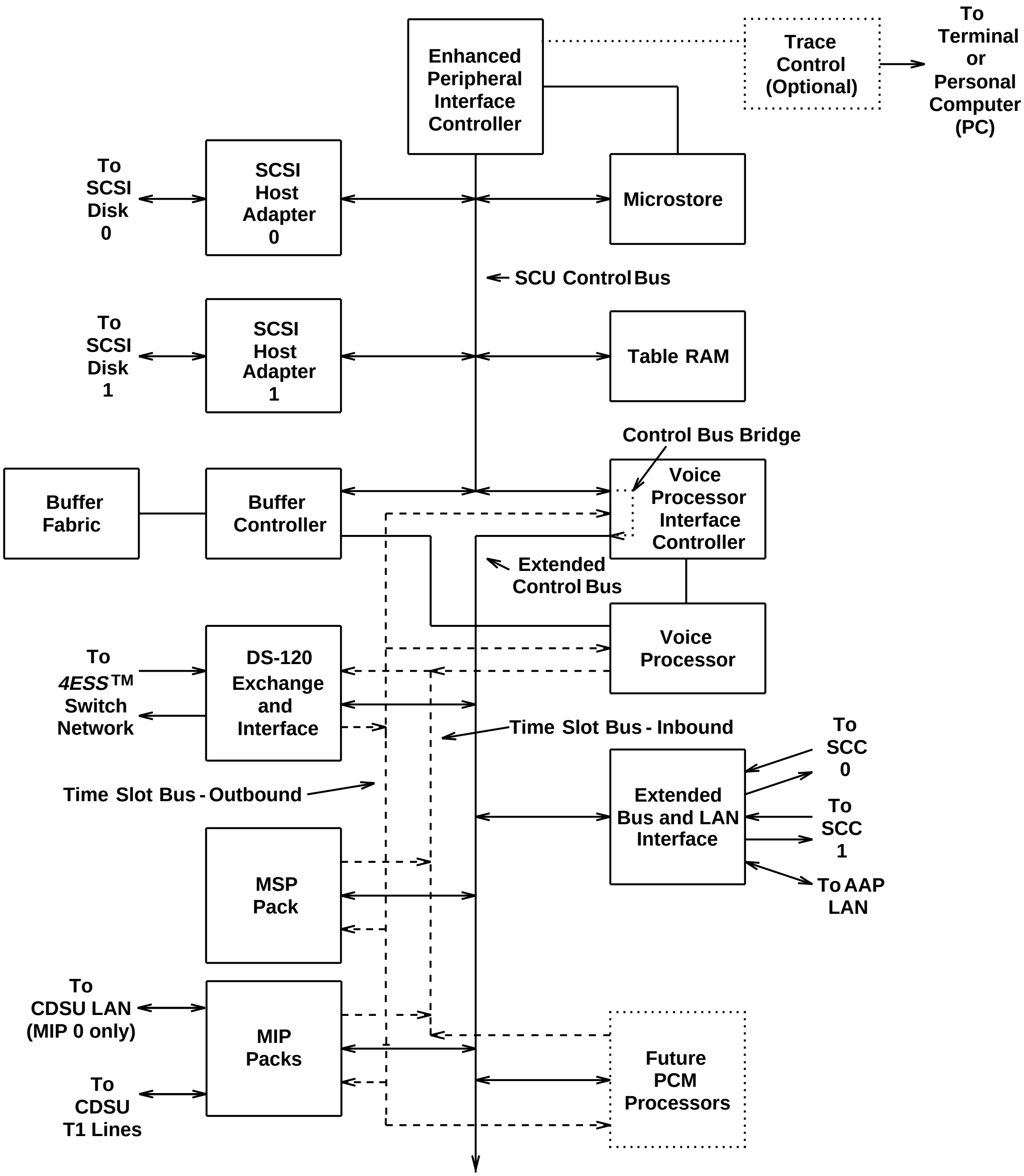

Figure 28. The SCU Architecture

A voice processor reads the data from the buffer memory, converts it from ADPCM to Pulse Code Modulation (PCM), and sends it at a predefined time over a time slot bus in the SCU to a DS-120 interface. The DS-120 interface then transmits the announcement to the *4ESS* switch network.

4.45 If a digit collection operation is specified in the message from the SCC, the PCM encoded signal is routed through the DS-120 interface to the time slot bus and then to an MSP circuit pack. This circuit pack runs a fast algorithm that decodes the tones into digits, which the control processor formats into messages and sends to the SCC through the EBI.

4.46 If speech recognition collection (associated with the ASR feature) is specified in the message from the SCC, the PCM encoded signal is routed through the DS-120 interface to the time slot bus and then to a Multifunctional Interface Processor (MIP) circuit pack. (It is still also routed to the MSP as before for DTMF collection.) The MIP circuit pack routes the PCM encoded data over a DS1 (T1) interface channel to an adjunct CDSC where speech recognition is performed. Control messages to/from the CDSC, as well as messages indicating the speech recognized, are sent over a 10 MBs Ethernet LAN interface between the CDSC and the MIP circuit pack. If an announcement playback is requested on the channel at the same time, echo cancellation is performed on the incoming speech to provide reliable speech recognition. Instead of the PCM encoded announcement being sent directly to the DS-120 interface, it is sent to the CDSC over a second DS1 (T1) channel where it is used by the CDSC to perform echo cancellation. The announcement playback data is then returned by the CDSC back to the SCU where it is once again sent to the DS-120 interface.

4.47 If announcement data needs to be written on the HDU, the control processor locates free disk space. The ADPCM announcement data is transmitted from the AAP over a local area network through an AAP interface. The data is temporarily stored in the table RAM, and the processor instructs the disk controller to write the announcement to the disk.

A. The DS-120 Exchange and Interface (TN1588)

4.48 The DS-120 circuit pack connects the links coming from the *4ESS* switch network and the SCU's local time slot bus. It includes a cable driver/receiver, a buffer register, a framer, a timing generator, a Time Slot Interchanger (TSI), and control logic to drive the local time slot bus. A special serial interface conforming to the V.35 specification allows the diversion of a single time slot to a future signaling processor. The DS-120 interface is the master of the time slot bus that connects through the SCU backplane to all other SCU circuit packs that need PCM data. The bus is comprised of an inbound section and an outbound section. The inbound section is 8 bits of parallel data that is time multiplexed between 256 time slots. The outbound section is also 8 bits parallel, with 256 time slots. A parity bit is sent with each of these buses. A block diagram of the DS-120 circuit pack is shown in Figure 29.

4.49 The DS-120 links in the *4ESS* switch each carry 120 voice signals and 8 maintenance channels over a 128 time slot serial bus in each direction. A pair of coaxial cables carry the bidirectional DS-120 link from the *4ESS* switch network to connectors on paddle boards on the backplane of the SCU directly behind the DS-120 interface circuit pack. Framing logic decodes the timing from the DS-120 signal and generates a start-of-frame reference and other timing signals. A shift register on the DS-120 interface converts between the serial format of the DS-120 and an 8-bit parallel format. A shadow register resynchronizes the parallel data and presents it to the input of a TSI on 128 of the 512 possible incoming time slots. Another 256 time slots appearing on the TSI input port are filled with data from the announcement playback logic that arrives on the inbound time slot bus. The unused time slots at the TSI input are filled with idle code.

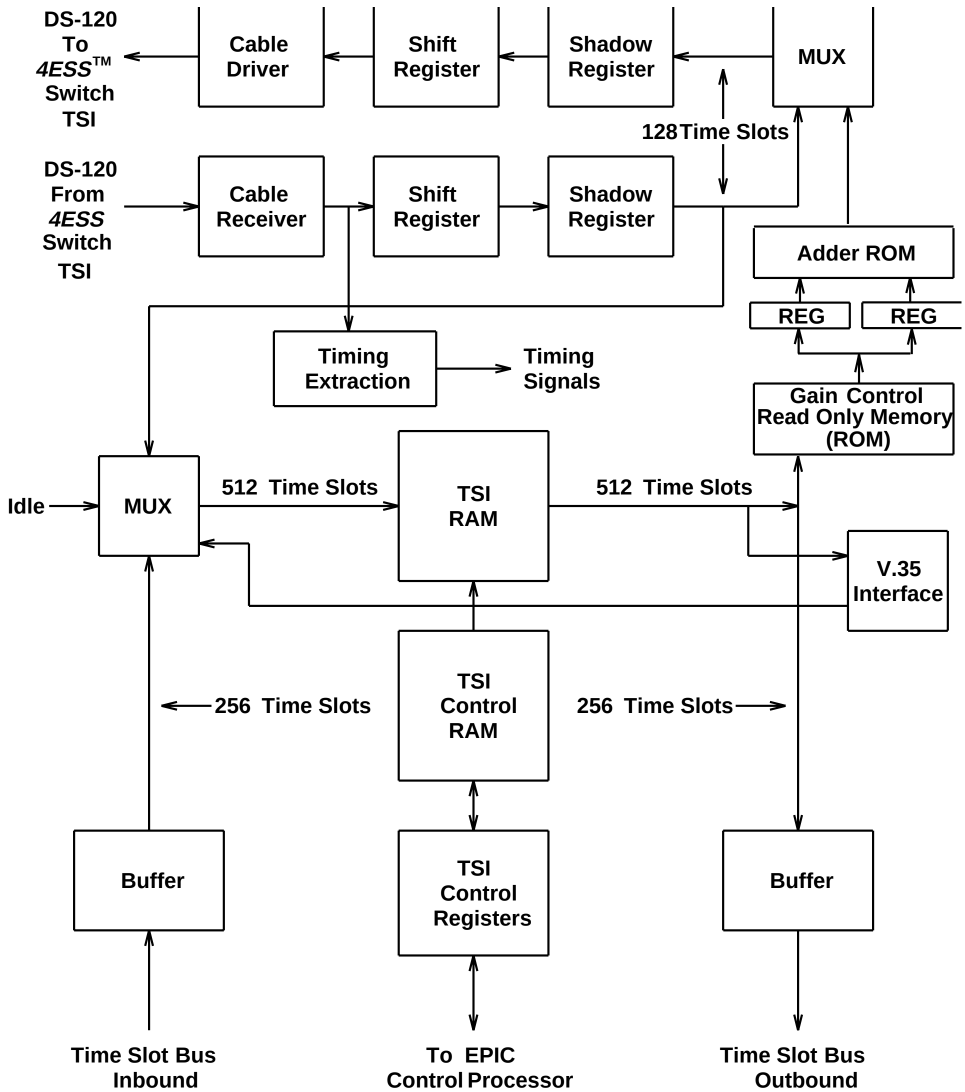

Figure 29. The DS-120 Interface

4.50 The TSI is a dual-ported memory with a write port and a read port. The 512 time slots of incoming data are written to the dual-port RAM sequentially addressed by the time slot count. A controller reads a time slot map RAM and decides from which data RAM address a given outgoing time slot's data will be read. Once the data emerges from the TSI, it is written to one of the following: one of 256 time slots on the outbound local time slot bus, eventually destined for the SCU circuit packs that require PCM data, or to alternating ports of an adder that combine two time slots into a single PCM stream destined for the outgoing DS-120 link. The combined time slots are routed through a gain control stage, a shadow register, and a shift register, and are driven to the outgoing DS-120 link. The adder and gain control stages could be used for teleconferencing.

B. The SCSI Host Adapter (TN1978)

4.51 A pair of TN1978 SCSI host adapter circuit packs are the interface to two SCSI buses per SCU. They contain control registers, First-In-First-Out (FIFO) registers, and SCSI controller chips. The SCSI standard allows up to seven device controllers to be connected to each host adapter. The device controllers are an integral part of the disk drives.

C. Voice Processor (TN1979) and Voice Processor Interface Controller (TN1980)

4.52 The voice processor complex is responsible for conversion between the 32-kbps ADPCM format used to store the announcements on the disks and the 64-kbps PCM format used in the network. It also performs announcement buffering and various timing functions.

4.53 The TN1979 voice processor circuit pack reads the announcement data from a buffer, does the format conversion to PCM, and sends the announcement to the DS-120 interface over the SCU time slot bus. A Voice Processor Interface Controller (VPIC) circuit pack (TN1980) manages the timing of the voice processor circuit pack.

D. Buffer Control (TN1981) and Buffer Fabric (TN1982)

4.54 The TN1981 buffer control circuit pack manages the timing of the buffer memory that stores the announcement prior to and during playback.

4.55 The TN1982 buffer fabric circuit pack provides 8 MB of storage to hold a complete announcement segment per channel. This data is read off the disk drives or from Cache Memory, transferred to the buffer fabric, then played back through the buffer control, VPIC and voice processor circuit packs.

E. Extended Bus and LAN Interface (KCN4)

4.56 The EBLI for the SCU is very similar to the SCC EBI. A fiber-optic transceiver converts optical signals to electronic signals for each of the two EB links (one from each of the duplicated SCCs). A block diagram of the EBI is shown in Figure 30.

4.57 The EB links are duplicated so the system can continue to function in the presence of a failure in an SCC or a single EB link. For fault isolation purposes, the EB links are considered a part of the SCC to which they connect. If one side of an SCC fails, the EBI on the SCU reconfigures under SCC direction to the other link and thus the other SCC.

4.58 In normal operation, with both sides of the SCC working, the SCU sends response messages to both sides of the SCC simultaneously. This is required to provide both SCCs with identical input so that the SCC sides stay in synchronization, and the matchers that monitor the SCC for faults detect no mismatches.

4.59 Diagnostics are provided to determine the health of both sets of EB links. The active SCC controller can loop messages to each SCU to completely test the path between the active controller and the SCU. The standby EB link is disconnected from the receiver on the SCU, so special circuitry can monitor the standby link for errors, which causes an error bit to be set. This capability helps isolate errors between the nonactive SCC and the SCU.

4.60 The AAP interface also resides on the EBLI circuit pack. A standard Ethernet chip set is used to implement the LAN interface to the AAP. This chip set performs all the standard Ethernet packetization and depacketization processes, media access control, buffering, and transceiver functions. Also, error counts are maintained and loopback testing modes can be invoked from the chip set.

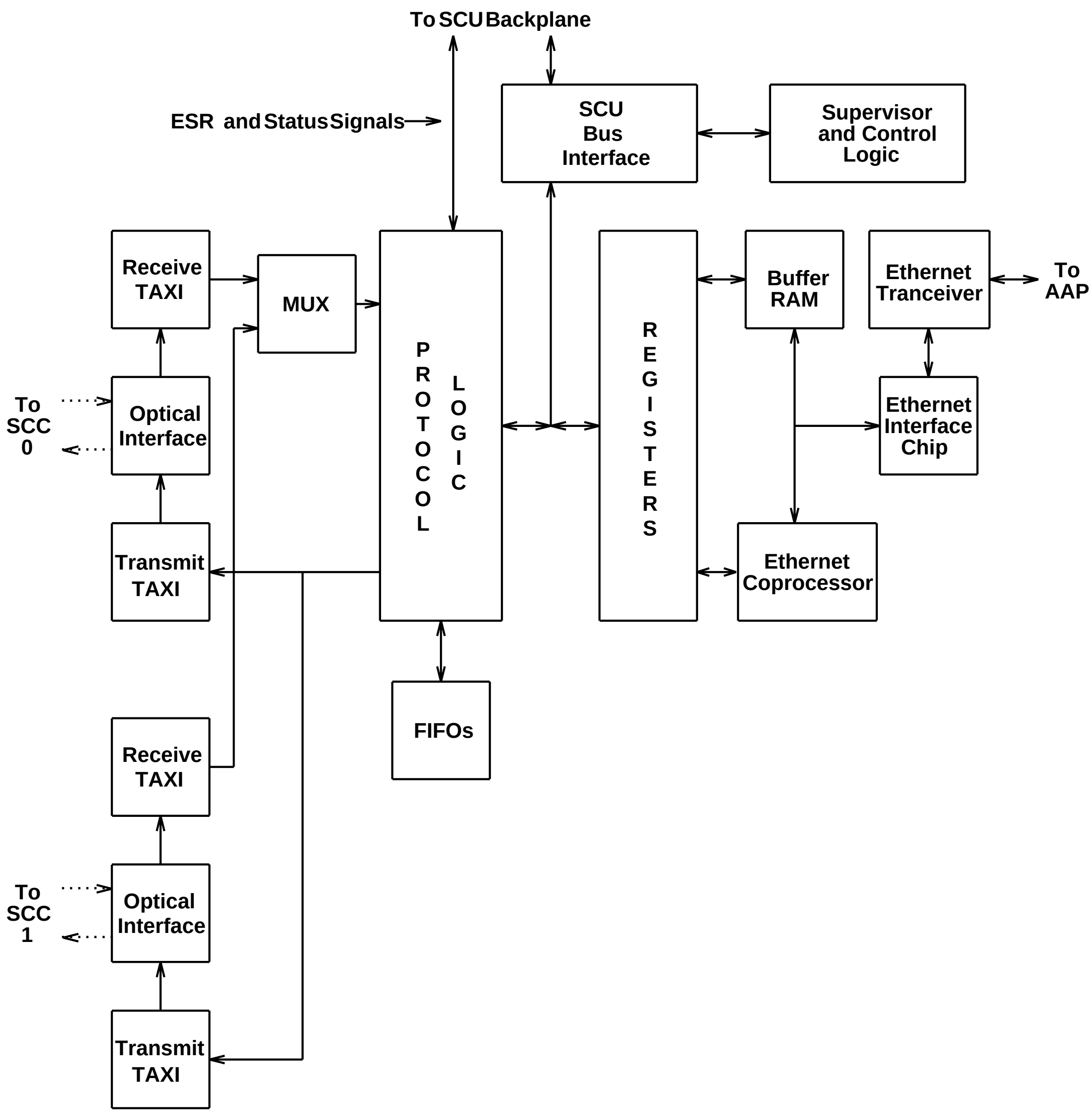

Figure 30. Extended Bus and LAN Interface

F. Table RAM (TN1983) or TN9002

4.61 The TN1983 Table RAM circuit pack provides 1 M words of general purpose memory. The TN9002 Table Ram circuit pack provides 1.5 M words of general purpose memory and is required for the announcement expansion feature.

G. Enhanced Peripheral Interface Controller (TN1976)

4.62 The Enhanced Peripheral Interface Controller (EPIC) circuit pack is a 16-bit microsequencer. It is programmed in assembly language with tasks being handled in a base cycle loop. Each task returns control to the base cycle loop scheduler via WAIT, EXEC, or EXIT system calls.

4.63 Interrupts are reserved for errors. In general, when the EPIC detects a serious error it sets a bit in the Error Source Register (ESR) and stops the operations. It is up to the SCC to notice the error (it can read the ESR without EPIC assistance) and report it to the 1B Processor CC. The 1B Processor CC then issues appropriate commands to resolve the problem (for example, run diagnostics, restore the SCU, and so forth).

H. Multifaceted Signal Processor (TN1589)

4.64 A block diagram of the MSP is shown in Figure 31. The MSP circuit pack contains five DSP-32C Digital Signal Processor (DSP) chips. The circuit pack also provides RAM to support the algorithms that are run on the DSPs, steering logic to direct any time slot from the SCU backplane buses to any DSP and an interface to allow the EPIC processor to communicate with all DSPs.

4.65 A single MSP circuit pack recognizes DTMF tones on all 128 incoming DS-120 time slots (120 operational and 8 maintenance) simultaneously. Customer-dialed digits encoded as DTMF tones and further encoded as PCM are placed on the SCU time slot bus by the DS-120 interface circuit pack. The MSP circuit pack accesses the time slot bus and routes each of the incoming time slots to one of the circuit pack's DSPs. Each DSP has support logic to interface with the time slot bus and to select the time slots that a particular DSP will decode. Interfaces to the SCU controller are used by each DSP to report its status and the values of any collected digits to the SCU processor.

I. Microstore (TN1977) or TN9001

4.66 The TN1977 or TN9001 microstore circuit pack is used with the TN1976 EPIC circuit pack. The program memory on the TN1977 or TN9001 is 16 K by 40 bits of Eraseable Programmable Read Only Memory (EPROM) and 32 K by 40 bits of RAM. The program RAM is writable and readable by the EPIC. Parity generation and checking are provided for the program memory. The TN1977 or TN9001 also contains the clock generation and synchronization circuitry for the EPIC. The instruction speed can be programmed to be from 183 to 610 nanoseconds. The TN9001 is required with the TN9002 for the announcement expansion feature.

J. Power Control (TN1984)

4.67 The TN1984 power control circuit pack provides a means of powering an SCU up or down and reporting power status via scan leads to the *4ESS* switch. The design has provisions for monitoring eight 15-amp current branches with two 410AA power converter circuit packs as the source. Each branch is monitored for overcurrent protection and will trigger an alarm if this condition exists. The TN1984 offers programmable current monitoring by simply shorting designated pins on the backplane. It also offers over and under voltage monitoring for out-of-range voltage conditions. Onboard diagnostics may be exercised manually or via software from the *4ESS* switch. The TN1984 also generates alarms for the SCC and SCU.

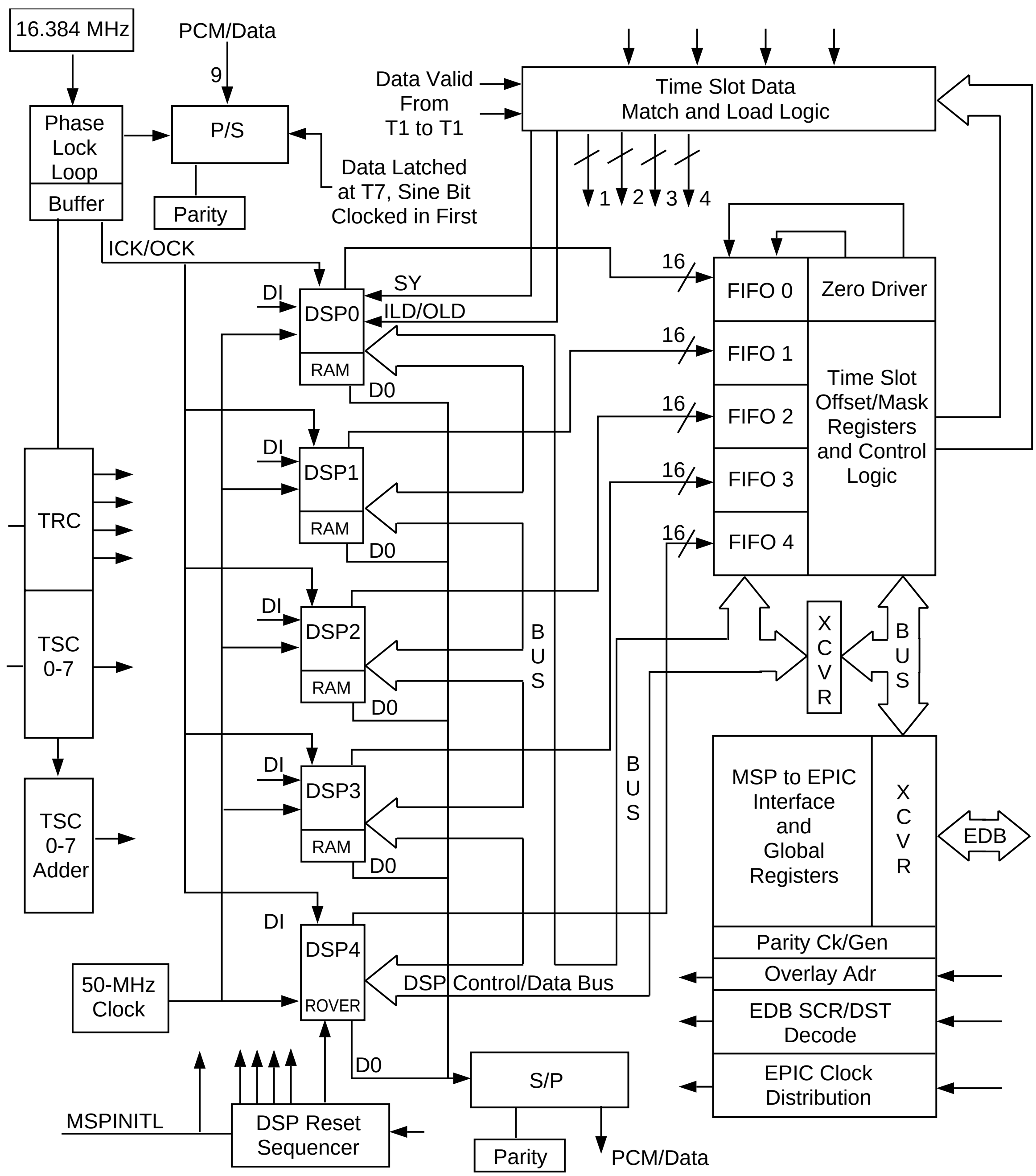

Figure 31. Multifaceted Signal Processor

K. Power Converter (410AA)

4.68 The 410AA power converter circuit pack is a 5-volt converter capable of supplying 60 amps from a -48 volt input. A remote on/off circuit may be used if a controller such as a TN1984 power control circuit pack is used in conjunction with the 410AA. The converter also has programmable overcurrent protection along with an overvoltage shutdown circuit.

L. Multifunctional Interface Processor (TN4001)

4.69 The MIP circuit pack contains a local processing device to administer the Ethernet LAN connection and the five T1 interfaces. The processor consists of a *Motorola** 68360 QUad Integrated Communications Controller (QUICC) device with volatile and nonvolatile support memory as well as an interface to the SCU TN1976 EPIC circuit pack, Ethernet LAN, RS-232, and five T1/DSX1 devices. MIP local processing hardware is summarized as follows:

- The 68360 QUICC device is a versatile, one-chip, integrated microprocessor and peripheral combination that contains the following features:
  - — CPU32+ processor running at 24 MHz that is configured with an external 16-bit data bus.
  - — Reduced Instruction Set Computer (RISC) controller that performs low-level protocol for the Ethernet LAN interface and three RS-232 asynchronous serial interfaces. The LAN interface supports an Ethernet IEEE 802.3 Access Unit Interface (AUI). A backplane paddle board at the rear of the MIP then provides an IEEE 802.3 10Base2 (Cheapernet) interface. The three RS-232 asynchronous interfaces have a programmable baud rate and format.
  - — Miscellaneous parallel interface registers.
  - — Programmable chip selects.
  - — Four general purpose timers.
  - — Baud rate generator.
  - — Background Debug Mode (BDM) that allows connection to a PC-based development system for program debugging (for example, program downloading, program tracing, program breakpoints, register dumps, etc.).
- Nonvolatile program memory is provided by 1 MB flash memory. Volatile memory is provided by 768-KB static RAM.
- Communication between the 68360 processor and the SCU EPIC processor is provided by a First-In-First-Out (FIFO) memory arrangement. An 8-KB FIFO is provided for each transmission direction to support full duplex communication. A MIP Status/Control register is also provided for the EPIC to perform various direct circuit control functions (such as reset).
- An 8-bit interface is provided to the five T1 devices. The 68360 can configure the T1 devices as well as monitor them for alarm conditions.

Hard Disk Unit (J4A024AC-1)

4.70 The SCU's announcements are stored in the HDUs. Each HDU is comprised of two matched pairs of hard disk circuit packs and two power controllers. Each HDU takes up one shelf in the SCC and/or SCU cabinet. The SCC and SCU cabinets can each be equipped with up to two HDUs (two matched pairs of hard disk circuit packs). In the SCU cabinet, one pair of hard disk circuit packs is associated with each SCU. The hard disk circuit packs available are the TN1672 (420 MB), the TN1972 (2 GB), the TN4000 (4 GB), and the TN9000 (9 GB). The TN4000 contains two disk drives. A pair of TN4000 circuit packs is

* Registered trademark of Motorola, Inc.

equivalent to two pairs of TN1972 hard disk circuit packs.

4.71 Each pair of hard disk circuit packs in the SCU cabinet is connected to an SCU by a pair of SCSI buses (bus 0 and bus 1). As shown in Figure 32, **two pairs of hard disk circuit packs in the SCC cabinet are connected to the same SCU**. Note that in each pair of hard disk circuit packs one pack is connected to SCSI bus 0 and the other pack is connected to SCSI bus 1. As shown in Figure 33, **each pair of hard disk circuit packs in the SCU cabinet is connected to a different SCU**. Figure 33 shows the pair of hard disk circuit packs to which each SCU is connected. Again, note that in each pair of hard disk circuit packs, one pack is connected to SCSI bus 0 and the other pack is connected to SCSI bus 1. Each hard disk circuit pack is separately accessible by the **init** and **copy** commands.

4.72 When an announcement playback is requested by the SCU, a disk controller circuit pack starts a seek operation to locate the ADPCM encoded announcement on one of the disk drives. The announcement data is then transferred from disk to a buffer memory. A voice processor reads the data from buffer memory, converts it from ADPCM to PCM, and sends it at a predefined time over a time slot bus in the SCU to a DS-120 interface. The DS-120 interface then transmits the announcement to the *4ESS* switch network.

4.73 Announcement data stored on the HDUs originates at a single central location for all *4ESS* switches in the network. Each *4ESS* switch office has an AAP to receive and buffer updates to the announcement set and to send the announcement data to all SCUs in the office.

4.74 If announcement data needs to be written on the disks, the SCU's control processor locates free disk space. The ADPCM announcement data is transmitted from the AAP over a local area network through an AAP interface. The data is temporarily stored in the table RAM, and the processor instructs the disk controller to write the announcement to the disk.

Custom Data Services Unit-I (CDSU-I)

4.75 Up to five CDSU-Is are provided in a CDSC-I. All CDSU-Is within the same CDSC-I are connected to the same SCU and provide Automatic Speech Recognition (ASR) capabilities for the DS-120 channels associated with that SCU. Each CDSU-I provides ASR capabilities for 24 DS-120 channels. Each CDSU-I (Figures 13, 14, and 15) consists of the following:

- One 486 Processor Card (WP-92304L301 CAT 1012)
- One Hard Disk Drive (WP-92304L304)
- One Ethernet LAN Interface Card (WP-92304L306)
- One SVGA Card (WP-92304L307)
- One SCSI Card (WP-92304L304)
- Twelve AYC50 Speech Processing Cards
- Two T1 Interface Cards (WP-92304L302)
- One Control Module
- One Power Module
- Three fans.

A. 486 Processor Card (WP-92304L301 CAT 1012)

4.76 The 486 Processor Card is based on an 80486DX2 processor operating at 66 MHz with 8 Kb internal cache, 256 Kb secondary cache and 32 Mb of onboard Dynamic RAM.

4.77 Peripheral ports on this card include two serial ports, a parallel port, a floppy drive interface, Imbedded Drive Electronics (IDE) interface, and a PS/2 mouse port.

B. Hard Disk Drive (WP-92304L304)

4.78 The hard disk drive is a SCSI hard drive.

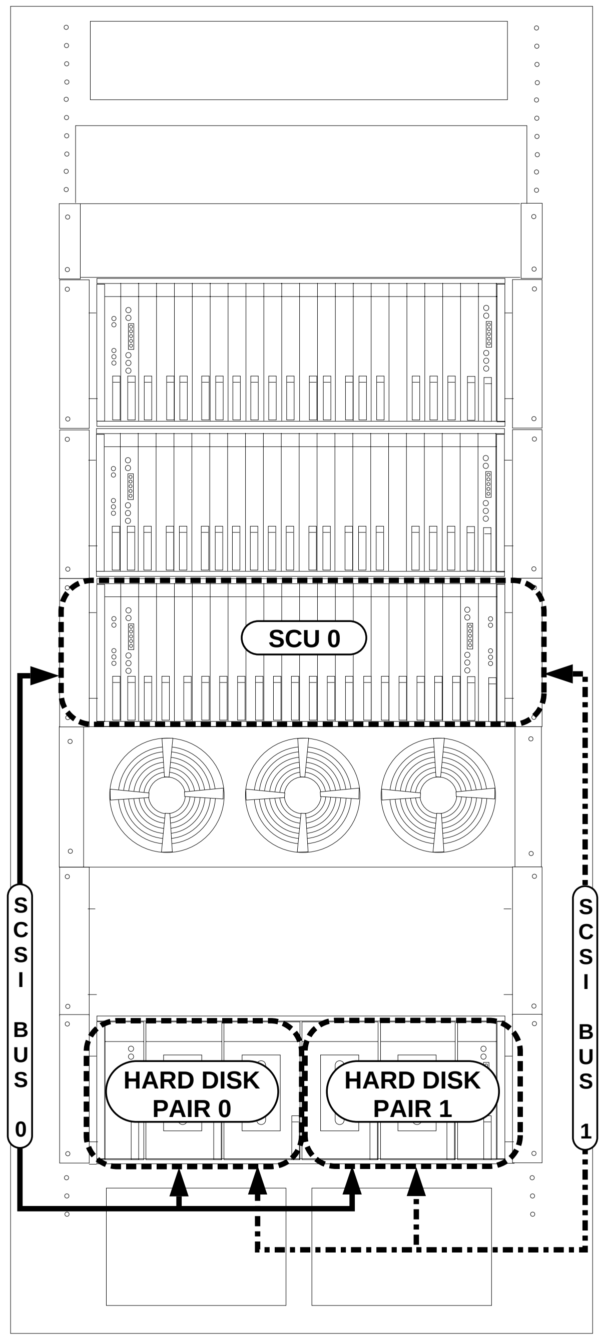

Figure 32. Hard Disk to SCU Connections in the SCC Cabinet

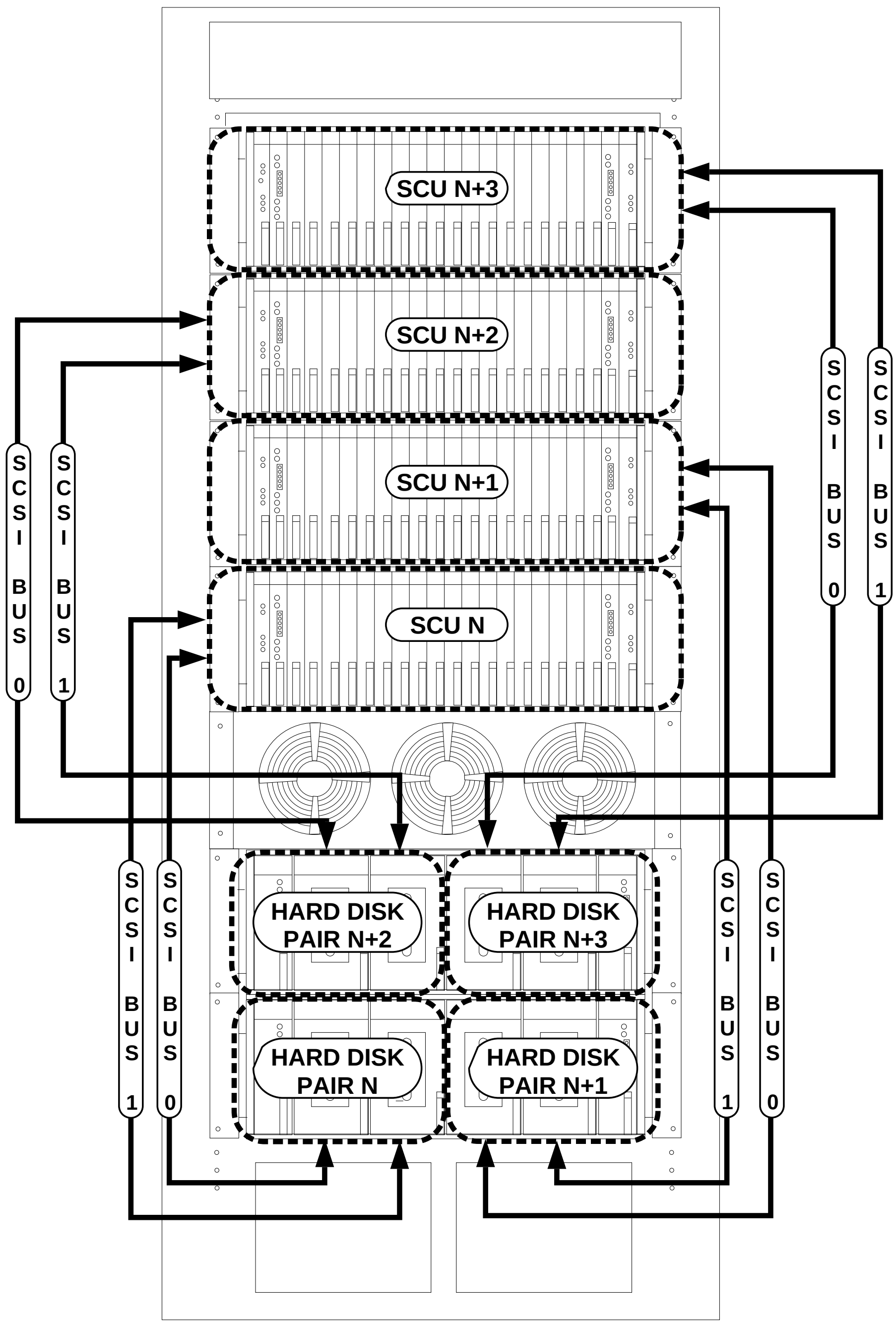

Figure 33. Hard Disk to SCU Connections in the SCU Cabinet

C. Ethernet LAN Interface Card (WP-92304L306)

4.79 The Ethernet adapter is the SMC Elite 16 Combo. It provides a datalink connection between the Multifunctional Interface Processor (MIP) and the CDSU-I.

D. SVGA Card (WP-92304L307)

4.80 The WP-92304L307 is a SVGA video card.

E. SCSI Card (WP-92304L304)

4.81 The SCSI card is an Adaptec* 1542C host adapter card.

F. AYC50 Speech Processing Cards

4.82 The AYC50 Speech Processing Card is a 16-bit Industry Standard Architecture (ISA) bus-based speech processing board. The board has four DSP32C processors running at 50 MHz. Each processor has 1 megabyte of private Static RAM and can share 256 Kbs of common memory. It has an I/O board to interface to the PCM Expansion Bus (PEB).

G. T1 Interface Cards (WP-92304L302)

4.83 Each CDSU-I has two T1 Interface Cards. These DTI/211 T1 Interface Cards allow interconnection of T1 time slots and AYC50s via the PEB. The DTI/211 allows the connection of individual T-1 voice channels or time slots without any external channel bank or trunk conversion equipment.

4.84 Each DTI/211 provides a 24-channel digital interface to 6 AYC50 Speech Processing Cards. Each CDSU-I uses 2 DTI/211 cards for a total of 48 channels.

4.85 Signaling and maintenance functions for the DTI/211 board are controlled and monitored by the CDSU-I 486 Processor Card. Each DTI/211 board has an RJ-48C connector which is used to transmit and receive voice/data to and from SCU TN4001 MIP circuit pack.

H. Control Module

4.86 The Control Module (Figure 34) consists of a control panel, a floppy drive, and a status display with the following LED indicators:

- System Status Indicators:
  - — ACTIVE — Remains lighted while the LAN link to the SCU's MIP circuit pack is established.
  - — OUT OF SERVICE — Lighted during CDSU-I software initialization (following a power-on or reset), up to the point where the CDSU-I is ready to establish a LAN connection to the MIP. The status then changes to UNAVAILABLE.
  - — STANDBY — This indicator is not used.
  - — UNAVAILABLE — Indicates that CDSU-I software is running, but no LAN link to the SCU's MIP circuit pack is currently established.
- Alarm indicators:
  - — CRITICAL — Indicates a critical alarm.
  - — MAJOR — Indicates a major alarm.
  - — MINOR — Indicates a minor alarm.

  The CDSU-I also uses error report messages to communicate any detected error conditions, along with the appropriate alarm level, to the SCU's MIP circuit pack via the Ethernet LAN.
- Power Supply Indicators:
  - — FUSE — Remains lighted during normal operation.

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* Registered trademark of Adeptec, Inc.

— POWER — Remains lighted during normal operation.

During normal in-service operation, the ACTIVE LED will be lighted.

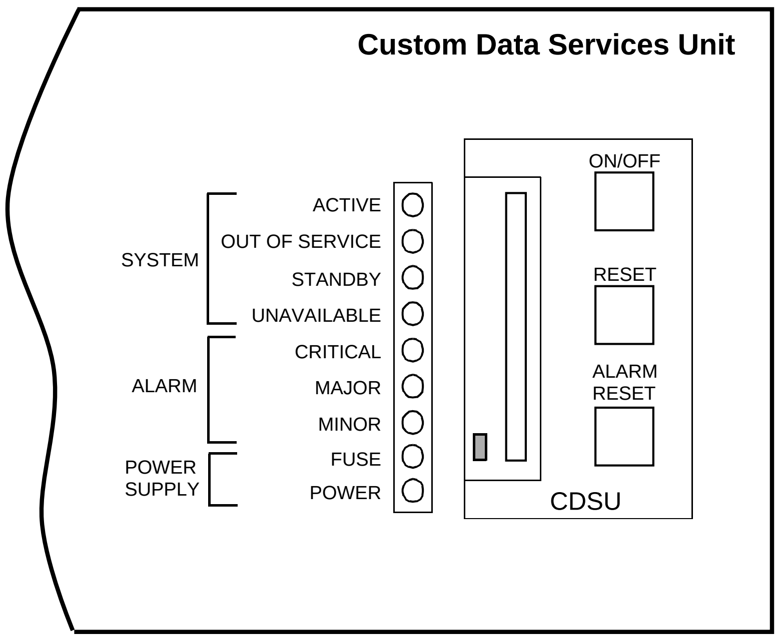

Figure 34. The CDSU-I Control Panel

I. Smart HUB

4.87 The Smart HUB, located in the CDSC-I, is used to connect the AAP to the CDSU-Is for remote login to the CDSU-Is. This allows Broadcast Warning Messages (BWMs) and Software Updates (SUs) to be sent to the CDSU-Is from the AAP. Software updates that can be applied via the AAP include the following:

- ASR Unit Operating Software
- ASR Application Software.

4.88 The LAN connections provided by the Smart HUB also provide access to the CDSU-Is by various support organizations. This allows the support organizations to perform the following operations on the CDSU-Is remotely.

- Execute BWM/SU operations, such as APPLY, BLOCKOUT, BOLO, PERM, RMV, VFY, and DISPLAY.
- Log into the UNIX* system.
- Upload and download CDSU-I files (such as log files, error files, etc.).
- List and display BWM/SU status of CDSU-Is.
- Add any deleted CDSU-Is from the list serviced by the AAP.

Custom Data Services Unit-II (CDSU-II)

4.89 Up to four CDSU-IIs are provided in a CDSC-II. Two of the four CDSU-IIs within the same CDSC-II are connected to one SCU. The other two CDSU-IIs are connected to a different SCU. The CDSU-IIs provide ASR capabilities for the DS-120 channels associated with that SCU. Each CDSU-II provides ASR capabilities for 60 DS-120 channels. Each CDSU-II (Figures 19, 20, and 21) consists of the following:

- One *Pentium*** EISA/PCI Processor Board
- One SCSI 2.1-GB Hard Drive
- One Ethernet LAN Interface Board
- One PCI SVGA Video Board
- One PCI SCSI Interface Board
- Five BYC51 Speech Processing Cards
- One AYC52 T1 Interface Card
- One AYC53 Echo Cancellation Card
- One Control Module
- Two Power Supplies.

4.90 The main hardware components of the CDSU-II (BYC51, AYC52, AYC53, and Control Panel) are described in the following paragraphs.

A. Speech Processing Card (BYC51)

4.91 Each BYC51 Speech Processing Card provides speech recognition for 12 DS-120 channels. The BYC51 has a total of 48 MB of Dynamic RAM. A daughter card connects the five BYC51 cards to the SCSA PCM bus which is also connected to the AYC52 and AYC53 cards.

B. T1 Interface Card (AYC52)

4.92 Each CDSU-II has one AYC52 T1 Interface Card. The AYC52 supports five T1 spans (120 channels). The AYC52 provides interconnection of T1 time slots and five BYC51s. The AYC52 also provides connection to the AYC53 card for echo cancellation. The AYC52 allows the connection of individual T-1 voice channels or time slots without any external channel bank or trunk conversion equipment.

C. Echo Cancellation Card (AYC53)

4.93 The AYC53 is connected to the AYC52 card and the five BYC51 cards. The AYC53

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* UNIX is a registered trademark in the United States and other countries, licenced exclusively through X/Open Company Limited.

** Registered trademark of Intel Corporation.

provides echo cancellation for each of the 60 DS-120 channels supported by the BYC51 cards.

D. Control Panel

4.94 The Control Panel (Figure 35) consists of a control panel, a floppy drive, and a status display with the following LED indicators:

- System Status Indicators:
  - — ACTIVE — Remains lighted while the LAN link to the SCU's MIP circuit pack is established (normal in-service operation).
  - — OUT OF SERVICE — Lighted during CDSU-II software initialization (following a power-on or reset), up to the point where the CDSU-II is ready to establish a LAN connection to the MIP (software is running, but no LAN link to the MIP is established).
  - — HDD — Lights when the system's hard disk is being read to or written from.
- Alarm indicators:
  - — MAJOR — Indicates a major alarm.
  - — MINOR — Indicates a minor alarm.
  - — POWER — Indicates a shortage of power to the unit.
  - — FAN — Indicates that one or more fans have stopped running.

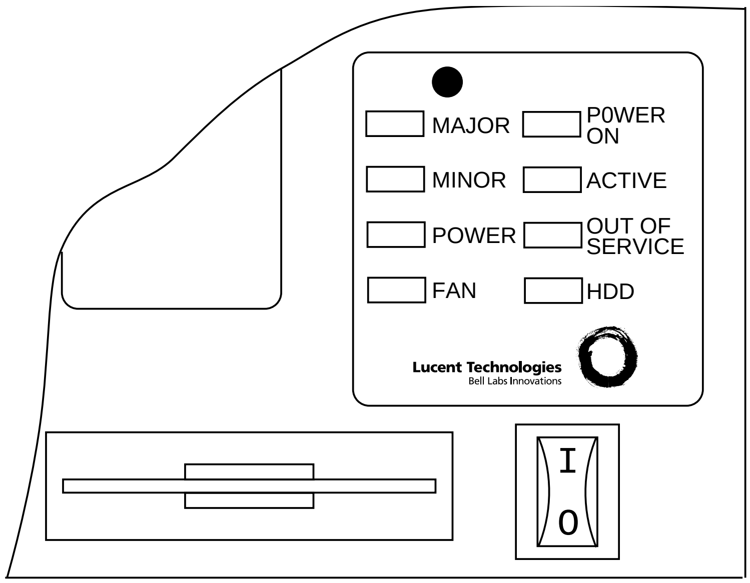

Figure 35. The CDSU-II Control Panel

The CDSU-II also uses error report messages to communicate any detected error conditions, along with the appropriate alarm level, to the SCU's MIP circuit pack via the Ethernet LAN.

- Power Supply Indicator:
  - — POWER ON — Remains lighted while power switch is in the **ON** position.

During normal in-service operation, the ACTIVE LED will be lighted.

E. Smart HUB

4.95 The Smart HUB, located in the CDSC-II, is used to connect the AAP to the CDSU-IIs for remote login to the CDSU-IIs. This allows Broadcast Warning Messages (BWMs) and Software Updates (SUs) to be sent to the CDSU-IIs from the AAP. Software updates that can be applied via the AAP include the following:

- ASR Unit Operating Software
- ASR Application Software.

4.96 The LAN connections provided by the Smart HUB also provide access to the CDSU-IIs by various support organizations. This allows the support organizations to perform the following operations on the CDSU-IIs remotely:

- Execute BWM/SU operations, such as APPLY, BLOCKOUT, BOLO, PERM, RMV, VFY, and DISPLAY.
- Log into the UNIX system.
- Upload and download CDSU-II files (such as log files, error files, etc.).
- List and display BWM/SU status of CDSU-IIs.
- Add any deleted CDSU-IIs from the list serviced by the AAP.

5. SCS Capacities

5.01 Each SCU supports 120 channels of simultaneous operation (either announcement playback and/or digit collection).

5.02 Each pair of hard disk circuit packs using the TN1672 hard disk circuit packs can store up to 95,000 announcement seconds (approximately). Each pair of hard disk circuit packs using the TN1972 hard disk circuit packs can store up to 490,000 announcement seconds (approximately). Each pair of hard disk circuit packs using the TN4000 hard disk circuit packs can store up to 980,000 announcement seconds (approximately). Each pair of hard disk circuit packs using the TN9000 hard disk circuit packs can store up to 2,136,000 announcement seconds (approximately).

5.03 Each SCU supports up to 65,535 announcement numbers. Announcement number "0" is invalid. Announcement numbers from 2001 to 2020 are reserved for SCU internal use (for maintenance tones and diagnostics).

5.04 The system supports announcements between 1.024 seconds and 261.12 (255 x 1.024) seconds in length, inclusive, in 1.024 second increments. Half-second (0.512 seconds) announcements are also supported.

5.05 The system supports up to 512 seconds of RAM resident announcements (Cache Memory) in increments of 0.128 seconds. This allows more efficient use of the disk by avoiding short disk reads and decreases the delay before the start of announcement playback.

5.06 Each SCU supports the concatenation of up to 32 announcement numbers.

5.07 Each SCU can collect an exact number of digits (up to 63 with a single PUB command), or it can collect an unspecified number of digits and let the 1B Processor CC tell the SCU when to stop. The SCU sends DTMF digits one at a time to the 1B Processor CC in either case.

5.08 Each SCC can have up to 16 SCUs, including spares.

5.09 Each SCU can have up to five associated CDSU-Is (located within the same CDSC) to provide ASR Phase 1 capabilities.

5.10 Each SCU can have up to two associated CDSU-IIs (located within the same CDSC) to provide ASR Phase 2 capabilities.

5.11 A CDSC-I can house up to five CDSU-Is.

5.12 A CDSC-II can house up to four CDSU-IIs.

5.13 Each CDSU-I provides ASR for 24 DS-120 channels.

5.14 Each CDSU-II provides ASR for 60 DS-120 channels.

5.15 Up to eight duplex SCCs are allowed in a single office.

5.16 The total service circuit capacity of this system is 15,360 ports (120 x 16 x 8).

6. SCS Maintenance

Introduction

6.01 There is a strict division of responsibility between the 1B Processor CC and the AAP regarding maintenance of the SCS. The 1B Processor CC is responsible for exercising, diagnosing, and reconfiguring the duplex SCCs and all SCUs. The LAN and the AAP itself are controlled from the AAP and its craft interface. However, the LAN is diagnosed from the SCS. The 1B Processor CC controls audits within an SCU (including announcement audits), while the AAP controls inter-SCU announcement audits. The AAP can also request intra-SCU announcement audits.

6.02 The 1B Processor CC is basically in charge of SCS maintenance, but some of the details of reconfiguration and diagnostics are distributed to simplify the 1B Processor CC actions. For example, the 1B Processor CC makes the decision to remove and restore an SCU, but some details of initializing an SCU are hidden down in the SCU.

Announcement Integrity

6.03 The following sections describe the methods used to ensure the integrity of announcements.

A. Checks During Announcement Update

6.04 The following methods are used to guarantee the integrity of announcements during the update process:

- Error detection code during transmission from Centralized Announcement Update System (CAUS) to the local AAP and from the AAP to SCUs.
- Announcement version numbers provided by the CAUS to detect different versions of the same announcement and to help keep track of updates during SCU outages, so they can be applied when the SCU is restored. These version numbers are also used by the CAUS to check which announcement is actually stored in an office.
- Optional Automatic Gain Control (AGC) for recording user announcements combined with caller verification. This can be done either at the CAUS or in the AAP.

6.05 No disk time stamp is used in the SCS. Instead, flags are used to indicate whether a centralized announcement update is in progress on a disk pair with copies on both disks. This flag is only set when an SCU is in the process of being restored to service and the AAP is applying updates which were queued while the SCU was out of service. A different value for this flag indicates that this is the destination disk for a copy operation now in progress. Other flags are also used by the SCS to do the following:

- Identify an SCU which is the source of copy data for a disk copy.
- Identify an SCU which is the destination of copy data for a disk copy.
- Indicate that a disk initialization is in progress.

B. Audits Internal to the SCU

6.06 The following checks are done within an SCU to detect corrupted announcements. The first check is done at initialization time only. The second and third checks are single copy announcement checks. The last check is a multiple copy announcement check. All checks are done as a low priority routine exercise (normally in the order shown) and upon demand by the 1B Processor CC or AAP, providing that no disk update or copy operation is in progress.

- Verification that the state of both disks is set to normal operation, and that the last announcement updated on both is the same. The disk state can be normal operation, copy in progress, formatted, or various announcement update in progress states.
- Verification of the error detection code for each announcement by reading the entire announcement from disk, recalculating the code value, and comparing it to the stored value on that disk.
- Verification of any RAM copy of the announcement by recalculating the error detection code over the RAM copy and comparing it to the value for the corresponding disk copy of the announcement.
- Comparison of the two (or more) copies of the announcement (two disk copies and possibly a RAM copy) by comparing their error detection code values, their size, their version numbers, and their state (if there is more than one nonidle state).

C. Audits Between SCUs

6.07 The AAP controls the auditing of copies of announcements between SCUs. Periodically, the AAP audits all copies of an announcement set. To each SCU with the announcement set, the AAP sends a request for the error detection code, the version number, and the announcement length for one announcement number. If a number is not in use, the SCU indicates that in the response. This is repeated for every possible announcement number in the set.

6.08 Mismatches in individual announcements on different SCUs are not corrected automatically. This prevents one bad copy with a mistakenly large version number from destroying all good copies in the office. Instead, the AAP has each SCU run its local audits for just that announcement. If a correctable local error is found, the error is corrected by the AAP. Otherwise, manual action is required to fix the mismatch.

6.09 When a mismatch is found, the AAP issues an error report through its own craft interface. The 1B Processor CC is not made aware of any problem as long as local audits in each SCU pass.

6.10 Updates, both normal and during the restoration of an SCU, are allowed during the audit of an announcement set. However, if the update is for the set being audited, the update waits until the audit finishes with an announcement number. After reaching a safe stopping point, the audit is suspended until the update is completed.

6.11 Maintenance actions (such as "disk copy") caused by the 1B Processor CC may also interfere with this audit. Such actions cause the SCU to drop out of the audit. If this causes the number of SCUs in the audit to fall below two, the audit is aborted.

Copying Announcements Between SCUs

6.12 Copying announcements between SCUs is only done in response to a manual request, perhaps to correct an audit failure. A single announcement, a range of announcements, or an entire disk can be copied. Copying an entire disk could take several hours, and is only done as a last resort.

6.13 To copy an announcement, the AAP sends an announcement verify message to the source SCU, which reads the announcement(s) off of a disk and sends it over the LAN to AAP. The AAP then does an announcement update to the SCU(s) needing the announcement.

6.14 To prevent interference between the copy and the update of the announcement set, normal updates are not allowed to announcements while they are being copied.

Copying an Entire Disk Between SCUs

6.15 An entire hard disk can be copied between SCUs from the 1B Maintenance (MTC) Terminal, with the following requirements:

- The source SCU can be in or out of service.
- The destination SCU must be out of service.
- Announcement updates are not allowed to the source SCU while the copy is in progress. (This must be manually inhibited.)

Updating Announcements in a Nonactive SCU

6.16 Announcement updates can occur in an office when one or more SCUs are not active, provided an AAP is active and there is at least one active SCU. In this situation, the AAP adds the update to the list of needed updates maintained for each SCU. When the 1B Processor CC restores the SCU, this list is used to perform the needed updates.

6.17 The 1B Processor CC may not do a disk copy in an SCU where a special update is in progress. If the 1B Processor CC needs to do a disk copy before the update finishes, it resets the SCU first. This causes the AAP to time out and abort the special update process. The AAP keeps any updates not completely finished on the pending update list.

LAN Routine Exercises

6.18 The AAP is responsible for routine exercises of the LAN. It does this by looping test messages over the LAN to each SCU. It loops a single test message to each SCU, one to each multicast group (one per announcement set), and broadcasts one to all SCUs, checking for the expected reply(s) in each case. If any of these tests fail, the AAP reports the problem using its local craft interface.

6.19 The AAP keeps a database of all valid SCU and multicast addresses. If the multicast or broadcast tests show that there is some SCU on the LAN that is not in this database, an error report is printed on the AAP craft interface. The AAP does not update its database to correct this error, since it does not know what announcement set(s) is in the unknown SCU. By leaving it out of the database, the AAP guarantees that no update can occur until this SCU gets included in the database. If the AAP cannot communicate with any SCU, it runs loopback diagnostics.

6.20 The SCUs do not test the LAN unless there is some indication of a LAN problem. Demand diagnostics can be invoked by the 1B Processor CC to run LAN loopback diagnostics on the SCU.

Removing/Restoring an SCC

6.21 The removal and restoration of the new SCC is similar to that for existing PUB controllers. Pumping from the SCU disk is different from any existing equipment.

Removing an SCU

6.22 Only the 1B Processor CC can remove an SCU from service. The SCU or the SCC detects errors implicating the subunit, then the SCC signals the CC that there is a problem. The normal 1B Processor CC response to an SCU error is to remove the SCU from service.

Restoring an SCU

6.23 The 1B Processor CC controls the restoration of an SCU. It first resets the SCU by writing a bit in its status register. This reset causes the SCU firmware to initialize the SCU and to pump the RAM program from disk. After the reset, the 1B Processor CC waits 2 seconds before checking for successful initialization. This is done by checking the ESR for initialization errors.

6.24 After the reset is finished, the 1B Processor CC sends an Equipment Configuration Data (ECD) order to the SCU via the SCC. This causes the firmware to jump into the operational program in RAM. The operational program, without further prompting, initializes its copy of the ECD from values in the message, copies the announcement tables from disk to RAM, and loads any RAM-resident announcements into the RAM buffers. The 1B Processor CC then sends an initialize DSP order, causing the SCU to pump the DSPs with the correct disk program. The last SCU action is to query the AAP for deferred updates. When all of these initialization steps are finished, the CC sets the in-service bit in the SCU status register, completing the restore.

Removing/Restoring a CDSU

6.25 Removing and restoring a CDSU is done manually at the CDSC. The SCU associated with the CDSU is removed from service automatically by the 1B Processor CC when a CDSU problem is detected. In this case, the SCU detects errors implicating the CDSU, then the SCC signals the CC that there is a problem. The normal

1B Processor CC response to a CDSU error is to remove the SCU associated with the CDSU from service.

Reliability

6.26 The SCS is connected to the office alarm grid.

6.27 The SCS has the capability to be removed and restored to service by command of the 1B Processor CC.

6.28 The SCS has the capability to format disks and copy the contents of a disk on one SCU to a disk on another SCU when both SCUs are homed on the same SCC (4E18 only, and only with the TN1672 disk). The SCS is also capable of responding to 1B Processor CC requests to read/write RAM or disk and system status/error registers.

6.29 The SCS has operational error checking such as hardware parity checks, a sanity timer, matching (when applicable), software self-checks, audits, and input command consistency checks. Errors detected by these checks are reported to the 1B Processor CC. Even though specific maintenance functions may be performed by the system components, the 1B Processor CC has full responsibility for recovery and configuration of the SCS.

6.30 Each component in the SCS has a software diagnostic which tests to see if the component is working satisfactorily. The diagnostics run reasonably fast (generally less than 3 minutes) and detect more than 95 percent of all service affecting faults. Manual diagnostic phases may take longer.

6.31 Faults are isolated to no more than an average of two and a maximum of ten circuit packs.

6.32 The Mean Time To Repair (MTTR) for any disk in the system is less than 4 hours, including the diagnostic run time and disk copy time. The MTTR for any other component in the system is less than 2 hours, including the diagnostic run time and restore time.

6.33 The Mean Time To Failure (MTTF) of an individual SCU including the disks, is more than 2,500 hours (3.5 months). The MTTF of an individual SCC (one side) is greater than 20,000 hours (2.3 years).

6.34 The SCS should be unavailable for service due to hardware faults no more than 1 minute per year.

6.35 Calls cutoff due to a SCS failure should be less than 1 in 100,000.

Alarms

A. SCS Alarms

6.36 Alarms for the SCS are reported via scan leads tied to the *4ESS* switch. Each of the TN1984 and TN1671 power control circuit packs report individual alarm status through a dedicated set of scan leads. A major alarm is activated at the cabinet if a power fault or fan failure occurs and is reported to the *4ESS* switch alarm grid.

B. CDSU-I Alarms

6.37 CDSU fuse alarms, power failures and component failures, including fan alarms, are not reported to the office alarm grid but are reported to the 1B processor via an SCU interject message sent on the LAN. This interject causes the SCU/CDSU to be removed from service and an SCU/CDSU diagnostic to be initiated. Diagnostic phases then detect and report the CDSU failure via the appropriate output message. To aid maintenance personnel in identifying the specific CDSC that has failed, labels are attached to the SCUs and CDSCs to cross-reference their physical locations in the office. Also, diagnostic software provides the floor identification code of the CDSC when a fault has been detected.

C. CDSU-II Alarms

6.38 For major and minor alarms, the CDSU-II software will send error report messages along with the appropriate alarm level (interject or BLM) to the MIP via the LAN. This interject causes the SCU/CDSU to be removed from service and an SCU/CDSU diagnostic to be initiated. Diagnostic phases then detect and report the CDSU failure via the appropriate output message. To aid maintenance personnel in identifying the specific CDSC that has failed, labels are attached to the SCUs and CDSCs to cross-reference their physical locations in the office. Also, diagnostic software provides the floor identification code of the CDSC when a fault has been detected.

6.39 In addition to the interjects and BWMs that may be generated, office alarms may also be triggered. One relay for major office alarms is provided in the CDSU-II via scan point connections.

6.40 In addition to the system fans, each BYC51 has three processor fans (one per Power PC chip). These fans are not alarmed, but each Power PC chip has a thermal sensor which will report overheating of the chip. This error is reported to the ACU as an interject via the LAN.

7. Power

Introduction

7.01 The majority of the SCS units share a common power design that provides the following major features:

- Power is derived from –48 V using *FASTECH* power unit circuit packs.
- Power units are automatically shut down for fault protection.
- Each unit (or functional unit group) has an individual power switch and control circuit pack.
- Each unit's power control circuit communicates power status to the *4ESS* switch processor.
- Each unit's power control circuit provides clamping outputs to protect the SCS common buses during unit fault and power cycling intervals.
- Indicators are provided to help localize any detected power fault.

SCS Power Requirements

7.02 Each SCC cabinet requires six –48 V power feeders from a J86334B-1 or J86334C-1 power distribution frame. The J86334B-1 power distribution frame is required for use with –48 V battery plants. The J86334C-1 power distribution frame is required for use with +140 V to –48 V converter plants.

7.03 Each of the SCU cabinets require four –48 V power feeders from the power distribution frame. The power feeders to each frame are connected to a fuse panel via a filter unit located at the top of the frame. The –48 V is then distributed to the various DC-to-DC power converter units within the frame via alarm-type fuses in the fuse panel.

7.04 Each CDSC requires one –48 V power feeder from the power distribution frame for each CDSU in the cabinet. These power feeders must be from the same power bus (A or B) that is connected to the associated SCU. If the CDSC-II is used, feeders from both A and B power buses may be required if the two SCUs connected to the CDSC-II use different power buses. The power feeders to each frame are connected to a fuse panel via a filter unit located at the top of the frame. The –48 V is then distributed to the various DC-to-DC power converter units within the frame via alarm-type fuses in the fuse panel. Also, a 120 V AC outlet is required in each CDSC with a Smart HUB, to provide power for the Smart HUB.

Power Dissipation

7.05 Power dissipation for the main cabinet with the duplex SCC and one SCU with four pairs of hard disk circuit packs is 2,250 watts. A fully equipped side cabinet with four SCUs, each with one pair of hard disk circuit packs, dissipates 2,600 watts. A fully equipped CDSC-I (five CDSU-Is) dissipates 2275 watts (455 watts per CDSU-I). A fully equipped CDSC-II (four CDSU-IIs) dissipates 2400 watts (600 watts per CDSU-II).

Abbreviations and Acronyms

8.01 This section defines the abbreviations and acronyms used in this practice.

AAP	Announcement Administrative Processor
ADPCM	Adaptive Pulse Code Modulation
AGC	Automatic Gain Control
ALU	Arithmetic/Logic Unit
ASR	Automatic Speech Recognition
BDM	Background Debug Mode
BNC	Bayonet Neill-Concelman
BWM	Broadcast Warning Message
BTL	Backplane Transceiver Logic
CAUS	Centralized Announcement Update System
CC	Central Controller (1B Processor)
CDSC	Custom Data Services Cabinet
CDSU	Custom Data Services Unit
DSP	Digital Signal Processor
DTMF	Dual Tone Multifrequency
EB	Extended Bus
EBI	Extended Bus Interface
EBLI	Extended Bus and LAN Interface
ECD	Equipment Configuration Data
EISA	Enhanced Industry Standard Architecture
EPIC	Enhanced Peripheral Interface Controller
EPROM	Eraseable Programmable Read Only Memory
ESR	Error Source Register
EXEC	Executive Processor
FMS	Flexible Media Stack
FIFO	First-In-First-Out
GRAM	Global Random Access Memory
HD	Hard Disk
HDU	Hard Disk Unit
IDE	Imbedded Drive Electronics
IEEE	Institute of Electrical and Electronics Engineers
ISA	Industry Standard Architecture
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Linear Predictive Coding
MIP	Multifunctional Interface Processor
MSP	Multifaceted Signal Processor
MTC	Maintenance
MTTF	Mean Time To Failure
MTTR	Mean Time To Repair
PCI	Peripheral Controller Interface
PCM	Pulse Code Modulation
PDF	Power Distribution Frame
PEB	PCM Expansion Bus
PUB	Peripheral Unit Bus
PUBB	Peripheral Unit Bus Branch
PUBI	Peripheral Unit Bus Interface

PUCB	Peripheral Unit Control Bus
PUDR	Peripheral Unit Bus Driver/Receiver
PURB	Peripheral Unit Reply Bus
QUICC	QUad Integrated Communications Controller
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
SCC	Service Circuit Controller
SCCC	Service Circuit Controller Cabinet
SCS	Service Circuit System
SCSI	Small Computer System Interface
SCU	Service Circuit Unit
SCUC	Service Circuit Unit Cabinet
SVGA	Super Video Graphics Adapter
TSI	Time Slot Interchanger
VPIC	Voice Processor Interface Controller

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