



# 4ESS™ Switch

## Digital Interface Frame-Export 1 (DIF-E1) Description

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## 1. General

### Introduction

**1.01** This document describes the Digital Interface Frame-Export 1 (DIF-E1) that is used in the 4ESS™ switch in North America. The document includes the following information for these frames:

- Physical description
- Functional description
- Power requirements
- Maintenance considerations.

**1.02** This document is reissued to support generic programs up through 4E21. The following revisions are included in the update of the document.

- Add a description of the 64 Clear Channel Capability (64CCC) feature.
- Add a description of the Per-Call-Control (PCC) feature.
- Revise the method of identifying digital interface unit (DIU) hardware and functions.
- Clarify Figures 1, 6, 7, 8, 9, 10, and 11.
- Make minor revisions

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## Development of DIF-E1

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**1.08** The DIF (digital interface) frame was developed for the 4E5 generic. This combined the functions of the signal processor 2 (SP) and digroup terminal complexes to provide a digital transmission interface for the 4ESS switch. The DIF-E1 was developed for the 4EE1 generic for use in the international market. The DIF-E1(D), J-5X059B-2, is a modified DIF-E1 for use in the 4E8 generic program and only in North America. The DIF-E1(MF), developed from a DIF-E1(D) for the 4E9 generic program, provides 64 MF digital service circuits. In the 4E10 generic program, the DIF-E1(DTMF,4-ST,IADC,CSDC) and DIF-E1(MF,4-ST,CSDC,IADC) frames provide 64 dual-tone multiFrequency (DTMF) (touch-tone) digital service circuits in a separate frame from MF service circuits. Both frames also have 4-State signaling, customer switched digital connect (CSDC) signaling, and integrated access digital connect (IADC) signaling capabilities on the DS1-line, using the SM8 DS1-line circuit pack. The SM8 was superceded by the SM9 DS1-line circuit pack in the 4E11 generic program. This added the 64kb Clear Channel Capability (64CCC) feature. The SM10 DS1-line circuit pack was introduced in the 4E14 generic program to add per call control (PCC). The original DS1-line circuit pack SM1B is still available, along with the SM9 and SM10, the SM8 circuit pack has been discontinued. The CSDC and IADC signaling features are no longer available within the 4ESS switch. The generic software has been modified to prevent feature activation. This document uses the term DIF-E1 when referring to subject matter common to the following DIF-E1 types.

- DIF-E1(D)
- DIF-E1(MF)
- DIF-E1(DTMF,4-ST)
- DIF-E1(MF,4-ST).

**1.09** In the 4E11 generic program, a SM9 T1-line circuit pack provides the 64CCC feature. The SM10 T1-line circuit pack adds the PCC functionality with the 4E14 generic program.

## Purpose

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**1.10** The DIF-E1 functions as a transmission and signaling interface between transmission facilities and the 4ESS switch. The DIF-E1 terminates and multiplexes DS-1 digital signals into DS-120 digital signals suitable for the 4ESS switching equipment. There are five DS-1 lines for every one DS-120 line. A total of 160 DS-1 lines provide 32 DS-120 lines. Digital interface units in the DIF-E1 process DS-1 framing and signaling formats, signaling translations, and zero code treatment. digital interface service units replace some of the DIUs in the DIF-E1 to provide the MF and DTMF services.

**1.11** The DIF-E1 (MF) has the same capabilities as a DIF-E1 (D) and provides up to 64 digital service circuits that receive and transmit MF signaling and 480 Hz operator tone.

**1.12** The DIF-E1 (DTMF,4-ST) has the same capabilities as a DIF-E1 (D) and provides up to 64 digital service circuits that receive and transmit DTMF signaling along with dial tone for each receiver circuit. The DTMF service circuits allow the 4ESS to provide direct connections to private branch exchange (PBX) customers.

**1.13** The 4-state signaling used by the DIF allows the 4ESS switch to provide CCITT 5 international signaling for international calls on a single DS-1 line

## Equipment Characteristics

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**1.14** The DIF-E1 (J-5X059B-2) is capable of replacing up to four digroup terminals and a signal processor 2 and is located in the DT/SP2 area of the office. This space saving is accomplished by the DIF-E1 through its use of large scale integrated circuits, metal oxide semiconductors, and bit-sliced microcontrollers instead of the hard-wired logic used in the DT and SP circuits. Transmission interfacing, dial-pulse digit reception/outputpulsing, and supervisory

scanning and distributing are basic DIF-E1 functions. The DIF-E1 does not provide pulse points, miscellaneous scan, and signal distribution points. Functions associated with these capabilities are provided by a standard SP in the office.

**1.15** The DIF-E1(MF) provides the MF signaling capability for roughly half the cost of that provided by analog MF service circuits. A controlling SP is not needed in the DIF-E1(MF); therefore, more SP/DIF member numbers can be allocated to trunk terminations rather than service circuits. This increases the trunk termination capacity of the toll office. Recent advances in the development of digital signal processor chips have made possible these digital MF service circuits (SM6 packs) in the DIF-E1(MF). The DIF-E1(MF) can contain SM6 packs in four of its digital interface units (DIUs).

**1.16** The DIF-E1(DTMF) is derived from and is very similar to the DIF-E1(MF). The DIF-E1(DTMF) can contain DTMF service circuits (SM7 packs) in four of its DIUs. The SM7 circuit pack has four DTMF transmitters and receivers and a dial tone generator. There are four SM7 packs per DIU for a total of 16 DTMF transmitters and receivers. This allows a maximum of 64 DTMF transmitters and receivers per DIF-E1 frame. The DTMF/4ST feature uses a TM377 pack in the digital interface controller (DIC). This pack replaces the TM376 pack used with the MF feature. The TM377 allows 4ST DIUs to be identified and diagnosed.

**1.17** Four-state signaling is accomplished by a DS-1 circuit pack either SM9 or SM10 and TM377. Before the SM9 and TM377 were available the 4ESS switch used two DS-1 lines—one for customer voice and the A bit part of the signaling. The other DS-1 line is used for the B bit part of the four state signaling. The generic call processing software reads two areas of signaling memory within the DIF-E1 to get the A and B signaling bits for each customer's call. With the SM9/10 and TM377 circuit pack hardware, the A and B signaling bits are derived from one DS-1 line

and sent to the TM377. The TM377 is equipped with a four-state register, and when activated for particular even DIU(s), the TM377 reads both A and B signaling bits from the DIU(s); otherwise, the A signaling bit is read.

**1.18** The network/digital multiplex interface (N/DMI) available with the 4E11 generic program provides a DS-1 connection between the 4ESS switch and a compatible PBX. The SM9 is a microprocessor based programmable interface circuit pack capable of terminating DS-1 connections with a variety of line format characteristics. One of these formats is the BOS (bit oriented signaling). With this new format, twenty-three 64 kb/s clear channels are provided. The 24th channel is used for BOS over the other 23 channels. The SM9 also provides an extended superframe framing format and B8ZS code suppression.

**1.19** There are 34 operational DIUs in the DIF-E1. The DIU 32 remains looped on itself until switched in to replace any DIUs numbered 0 through 15. Also, DIU 33 remains looped on itself until switched in to replace any DIU numbered 16 through 31.

**1.20** Each of the 32 in-service DIUs processes five DS-1 formatted digroups ( $5 \times 24 = 120$  channels) at 1.544 megabits per second (Mb/s). After buffering, the five digroups are multiplexed to a common time-shared, parallel format containing 128 time slots. Only 120 of the 128 time slots are used for working channels. The remaining eight time slots (called virtual trunks) are used for internal maintenance. For transmission to the time slot interchange (TSI), the 120-channel parallel format is converted to an 8.192 Mb/s (16.384 megabaud/second) serial bit stream (DS-120 format). The switched 16.384 megabaud/second bit stream is an input to the outgoing portion of the DIU where demultiplexing of the DS-120 and conversion to DS-1 format at 1.544 Mb/s takes place. The DS-1 signals are distributed to five digroups in the transmission facilities. Each of the in-service DIUs also performs the functions of signaling extraction and insertion.

**1.21** Supervisory scanning and distributing functions and dial pulse digit reception/outpulsing are executed by the signal processor in the DIC. A maintenance microprocessor (MMP) is used in the exchange of maintenance data between the DIUs and the DIC.

**1.22** Timing for the DIF-E1 is sent to the DIC over four coaxial cables from the TSI known as master timing links (MTL). Timing cables are limited to a maximum length of 1000 feet plus or minus one foot of each other. On the switch side, the DS-120 cables to and from the DIF-E1 are restricted to a length equal to the clock cable length plus or minus 60 feet. On the facility side, the DS-1 cable length is restricted to within 655 feet from the DSX-1 or a collocated LT-1 connector. Three different equalizer networks are available for proper operation of the DIF-E1 with various DS-1 cable lengths. The equalizers accommodate the following cable lengths.

- 1 to 220 feet (SJ5 circuit pack)
- 220 to 440 feet (SJ6 circuit pack)
- 440 to 655 feet (SJ7 circuit pack).

**1.23** Extensive use of large scale integration in the DIF-E1 makes it possible to duplicate certain parts of the DIC within a simplex controller. This is done for fault detection on the hardware that is not easily maintainable.

**1.24** The digital interface signal processor (DISP) and the MMP in the DIF-E1 consist of random access memory (RAM). The MMP also consists of 2K bytes of hardcore read only memory (ROM); however, the bulk of the MMP program store memory (52K bytes) consists of RAM. The DISP state translation memory consists of 12K × 18 RAM.

**1.25** The 4ESS switch has recommended limits for its operating environment. The temperature should generally range between 4 and 38 degrees centigrade. The humidity level should range between 20 and 55 percent.

## **2. Physical Description**

### **Digital Interface Description**

**2.01** The DIF-E1 is a 3-bay complex (double bay with single bay [Figure 1]). All bays are 7 feet high and 12 inches deep. The double bay is 6 feet 6 inches wide, and the single bay is 3 feet 3 inches wide. The bays are numbered 0, 1, and 2, from left to right. The left and right sides of each bay are mirror images of each other for ease of wiring. A fully equipped DIF-E1 contains the following:

(a) ED-5X400-30, G1 Double Bay

BAY 1:

- Peripheral unit bus (PUB) interface circuitry
- Fully duplicated DIC
- Telephone and teletypewriter jack assembly
- Two working DIUs (DIU 0 and DIU 16)
- Power unit assembly
- Fuse and alarm panel assembly
- Filter assembly.

BAY 0:

- Input/output (I/O) and protection switch assembly
- 15 working DIUs (DIUs 1 through 15)
- 1 spare DIU (DIU 32).

(b) ED-5X400-30, G2

BAY 2:

- I/O and protection switching assembly

- 15 working DIUs (DIUs 17 through 31)
- One spare DIU (DIU 33).

## Printed Wiring Board Design

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**2.02** The printed wiring boards (PWB) used in the DIUs are 8 inches high and 9 inches long. These PWBs can either be double sided or of the multilayer type. A similar type of PWB is also used in the protection switch circuitry and the controller. The original backplane for the Interface for Peripher Unit Bus (IPUB) was a 4-inch high by 9-inch depth. The new multi-layered PWB backplane for the controllers includes the IPUB backplane. This new multilayered PWB controller backplane consists of two large panels for each controller (total of 4 printed wiring boards) and contains most of the original first level wiring, and minimizes some of the long wiring runs.

## Digital Interface Connectorization

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**2.03** The DIF-E1 has been modularized into replaceable plug-in circuit packs and power units. The plug-in units slide into guided channels on the mounting shelves and make electrical connections with pins in the backplane. Connections between the DIUs and DICs are made with flat ribbon cables that plug into connectors in the center of each bay. This type of connectorization reduces the amount of wiring in the rear of the frame.

### Bay 1 (P/O 5X059B)

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**2.04** The following paragraphs describe the equipment contained in Bay 1 which is located in the center of the DIF-E1 complex.

#### A. Peripheral Unit Bus Interface

**2.05** The IPUB, located at vertical positions 74 through 84, contains the plug-in circuit packs needed to interface the PUB and the DIC. The

PUB is connectorized and plugged in to the wire-wrap pins at vertical position 84. The associated PUB interface power circuit packs, power unit, and power switch are below the interface circuitry at vertical position 74 (Figure 2). A TG-4 circuit pack has a LED display to indicate out-of-tolerance voltages (Table A) on the PUB interface circuitry.

#### B. Digital Interface Controller— ED-5X401-30, G1

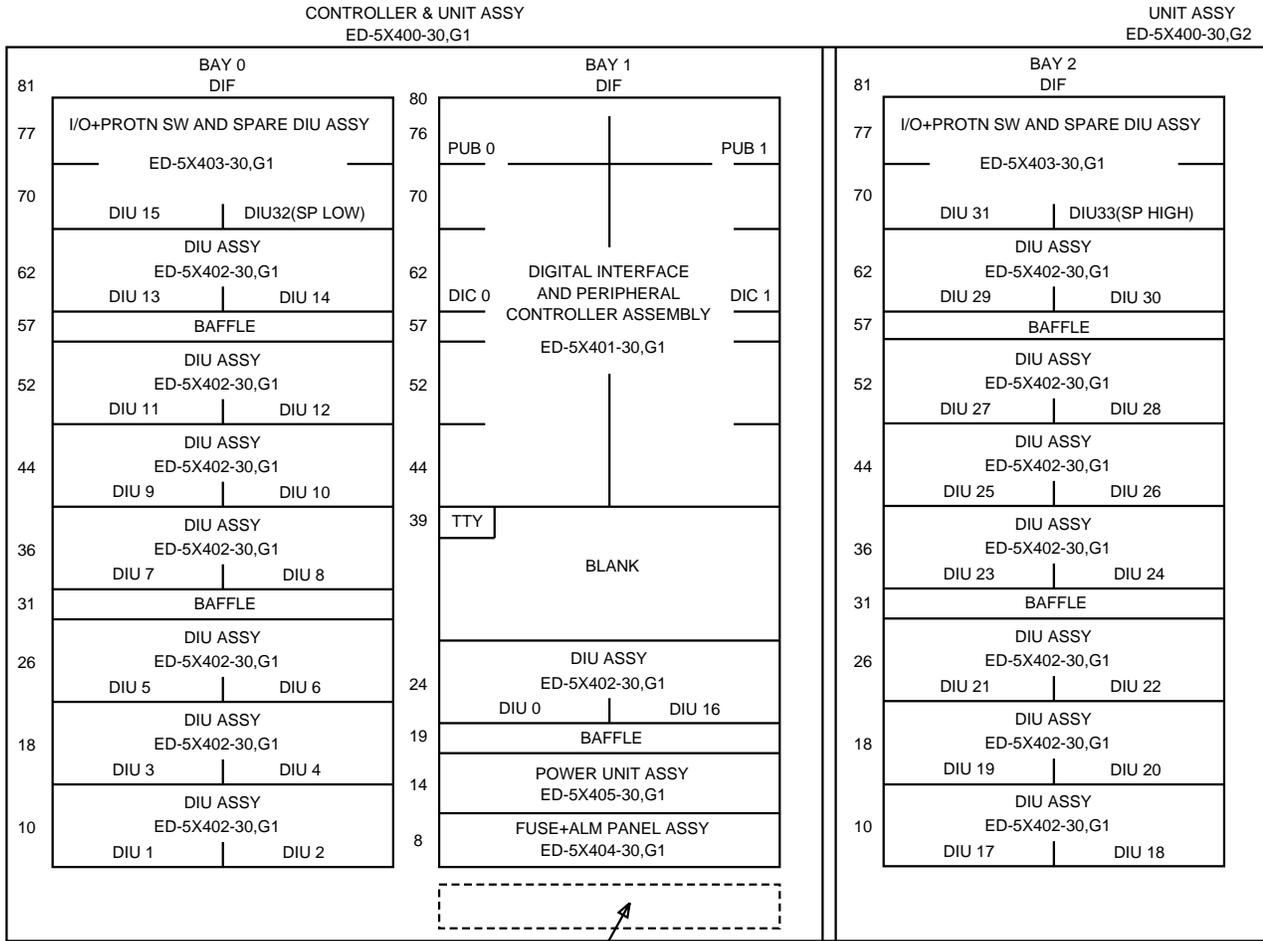
**2.06** Four shelves of circuit packs at vertical positions 40 through 74 make up the DIC. At position 59 is the controller power switch; at vertical position 64 is a LED display to indicate overcurrent, overvoltage, and undervoltage conditions in the DIC (Figure 3). Below the left side of the controller is a TEL and TTY jack unit to provide telephone and beltline TTY communications within the 4ESS switch.

#### C. Digital Interface Units— ED-5X402-30, G1

**2.07** The DIUs 0 and 16 are located in Bay 1 at vertical position 24. These DIUs are collocated in a space 38-inches wide, 8-inches high, and 11.84-inches deep. Each DIU is equipped with digroup (SM1, SM1B, SM9, SM10) circuit packs, an SM2, an SM3, an SM4, and an SM5 circuit pack. Each DIU is also equipped with a 141C or 140L power unit, a 140E power unit, and an LED to indicate when the DIU is in the maintenance mode.

#### D. Digital Interface Service Units— ED-5X400-01, G1

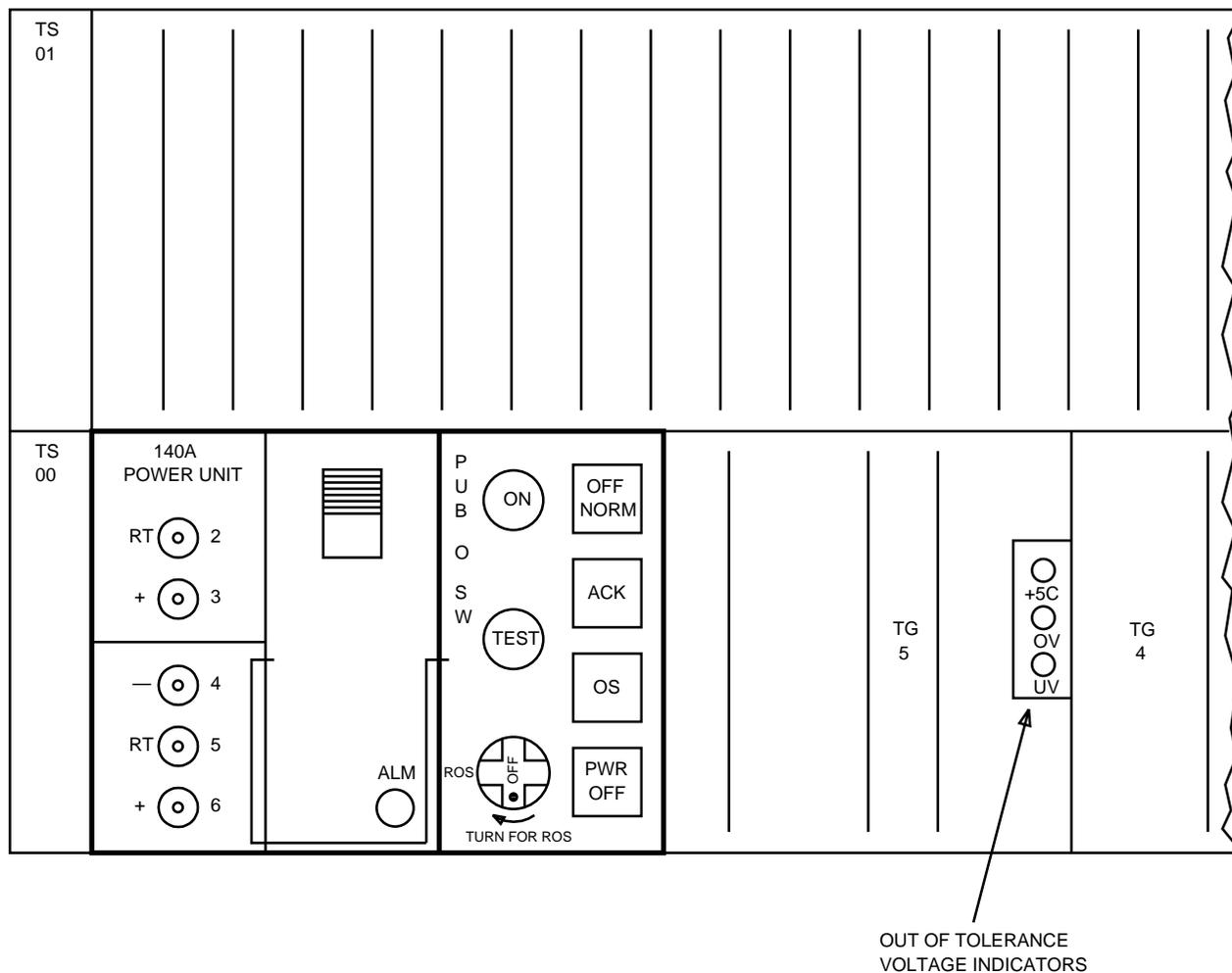
**2.08** A DIF-E1 complex can be equipped with four MF DISUs or four DTMF DISUs to provide 64 MF service circuit trunk appearances or 64 DTMF service circuit trunk appearances to the switching network. These DISUs are located in Bay 0 and Bay 2 at vertical positions 10 and 44. The DISUs occupy DIU positions 1, 18, 9, and 26. Each DISU is also equipped with a 141C power unit and an LED to indicate when the DISU is in the maintenance mode.



**LEGEND:**  
 ASSY - ASSEMBLY  
 DIC - DIGITAL INTERFACE CONTROL  
 DIU - DIGITAL INTERFACE UNIT  
 I/O - INPUT/OUTPUT  
 PROTN - PROTECTION  
 SW - SWITCH

FILTER UNIT ASSY  
 ED-5X406-30,G1

**Figure 1. DIF-E1 Equipment Layout**



**Figure 2. PUB Interface Assembly**

**E. Power Unit Assembly—  
ED-5X405-30, G1**

**2.09** The power unit shelf, located at vertical position 14, contains the 245B and 140F power units for both controllers (Figure 4). The

245B power unit supplies +5 volts to the +5 V dc bus. The 140F power unit supplies -5 volts to the -5 V dc bus.

**Table A. Controls and Indicators**

<b>Name</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
Controller Current Monitor	Over Current A/B 70 62 52 44	LED (red)	LED is lighted when current is too high for safe operation.
Controller Voltage Monitor	Voltage +5C Under +5 -5 +12	LED (red)	Lighted when +5C voltage is less than operating range (power switch voltage). +5 voltage is less than operating range (power switch voltage). -5 voltage is less than operating range (power switch voltage). +12 voltage is less than operating range (power switch voltage).
Controller Voltage Monitor	Voltage +5C Over +5 -5 +12	LED (red)	Lighted when +5C voltage is more than safe operating range (power switch voltage). +5 voltage is more than safe operating range (power switch voltage). -5 voltage is more than safe operating range (power switch voltage). +12 voltage is more than safe operating range (power switch voltage).
Power Units	ALM	LED (red)	Lighted when power unit fails.
PUB Interface Voltage Indicators	+5C +5 Over +5 Under	LEDs (red)	Lighted when +5C voltage fails (power switch voltage). +5 volts is more than safe operating range. +5 volts is less than operating range.
Maintenance Mode Indicator	MM	LED (green)	Lighted when DIU is in a maintenance mode protection switched state.

See footnote at end of table.

**Table A. Controls and Indicators (Contd)**

<b>Name</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>
Diagnostic Switch	*LAMP TEST	Pushbutton Key	When depressed, all lamps associated with the DIUs except the power failure lamp are lighted.
	*ROS/NORM	Rotary Key	When rotated to ROS position, a diagnostic test is requested for the out-of-service DIUs. The MM LED is lighted on out-of-service DIU.
	*OFF	Lamp (white)	Lighted when ROS/NORM key is in ROS position.
	*ACK	Lamp (white)	When lighted, indicates that the program has recognized a request for diagnostic test.
	*OS	Lamp (yellow)	When lighted, indicates the program has taken one or more units out of service.
	OFF NORM	Lamp (white)	When lighted, indicates that a request has been made to take equipment out of service, PWR OFF and OFF NORM lamps both lighted indicates power has been removed manually from the DIC or PUB interface.
	ACK	Lamp (white)	When lighted, indicates the program has recognized the request for out of service or that diagnostic tests made following a request for frame or unit restore to service are in progress.
	OS	Lamp (yellow)	When lighted, indicates the program has taken associated equipment out of service.
DIC/PUB Interface Power Switch	PWR OFF	Lamp (red)	When lighted, indicates power has been removed from DIF controller or PUB interface. If PWR OFF lamp is lighted and OFF NORM lamp is extinguished, power was removed from the DIF controller or PUB interface under fuse alarm (FA) conditions.

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See footnote at end of table.

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**Table A. Controls and Indicators (Contd)**

Name	Name	Type	Function
	OFF	Rotary pushbutton (OFF and ON pushbuttons are part of same switch)	When rotated clockwise (OFF on face of switch is horizontal), a request is made to the program to remove DIF controller or PUB interface from service. If OS lamp lights, OFF pushbutton may be depressed to remove power from frame or unit on which switch is mounted.

\*One key or indicator is provided per 17 DIUs.

#### **F. Fuse and Alarm Panel— ED-5X404-30, G1**

**2.10** The fuse and alarm panel, located at vertical position 8, contains fuses for +140 volts and +24 volts to the DIC and PUB interface, +140 volts to the DIUs, and +24 volts to the protection switch relays (Figure 5). The +140 volt and +24 volt power feeders have A and B distributions to the frame. This panel also contains alarm relay and relays to operate the power supplies.

**2.11** The filter unit is needed to filter the +140 volt and +24 volt power feeders. The unit is behind the bottom kickplate on Bay 1.

#### **Bays 0 and 2 (J5X059A)**

**2.12** Bays 0 and 2 are on either side of Bay 1 and contain identical equipment, except the submember designations are different.

#### **A. Input/Output and Protection Switch Shelf—ED-5X403-30, G1**

**2.13** The T1 lines are terminated in a connector assembly at vertical position 81 (top) in Bays 0 and 2 (Figure 6). The protection switch relay shelf is at vertical position 77. The protection switch relay packs have coaxial connectors to terminate the TSI cables.

#### **B. Digital Interface Units (Vertical Positions 6 Through 74)— ED-5X402-30, G1**

**2.14** Bays 0 and 2 each contain 15 working DIUs and 1 spare DIU located at vertical positions 6 through 74. These DIUs are used for protection switching (Figure 7). Two other working DIUs are in Bay 1, as stated earlier. Each unit has a 141C or 140L power unit, a 140E power unit, and a unit switch with a LED to indicate when the unit is in a maintenance mode. The remainder contains SM1 or SM1B, SM2, SM3, SM4, and SM5 circuit packs to interface DS-1 and DS-120 signals.

**2.15** The DIU next to the spare (protection switch) DIU is equipped with a diagnostic switch similar in appearance to a power switch. The diagnostic switch is used to request CC to diagnose a DIU which is looped on itself (off-line).

**2.16** In the DIF-E1(MF) frame, DIUs 1, 18, 9, and 26 may be either standard DIUs or MF DIUs (that is, DIUs which contain digital MF receiver and transmitter circuits). These digital MF service circuits are on SM6 circuit packs. Each SM6 circuit pack contains 4 MF receiver circuits and 4 MF transmitter circuits. The SM6 packs are in digroup positions 1 through 4 of an MF DIU. A normal trunk circuit pack (SM1B) is always in digroup position 5. The SM6 circuit packs require more power than the SM1B circuit packs that they

replace. Therefore, the 141C power converter replaces the 140L power converter in MF DIUs.

**2.17** In the DIF-E1(DTMF) frame, DIUs 1, 18, 9, and 26 may be either standard DIUs or DTMF DIUs (that is, DIUs which contain digital DTMF receiver and transmitter circuits). These digital DTMF service circuits are on SM7 circuit packs. Each SM7 circuit pack contains 4 DTMF receiver circuits and 4 DTMF transmitter circuits. The SM7 packs are in digroup positions 1 through 4 of a DTMF DIU. A normal trunk circuit pack (SM1B) is always in digroup position 5. The SM7 circuit packs require more power than the SM1B circuit packs that they replace. Therefore, the 141C power converter replaces the 140L power converter in DTMF DIUs.

**2.18** Four-state feature DIUs can only reside in even numbered DIUs, starting with 0. A DIU using E and M signaling cannot reside in the odd numbered DIU immediately after a 4S feature DIU. The only restriction on the placement of IADC and CSDC feature DIUs, is that they may not reside after a 4S feature DIU. The SM8 circuit pack provides the 4S, CSDC, and IADC features. However, the SM8 cannot provide these three features simultaneously.

## Growth

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**2.19** The DIF-E1(D) can either be provided at an office cutover or grown into the operating office if office data requirements for the DIF-E1(D) have been included for the growth interval. Digital service associated with an existing DIF-E1(D) can also be grown to the point where 32 DIUs along with two spare (protection switch) DIUs are being used. One spare (protection switch) DIU is required for up to 16 DIUs.

**2.20** A change to add a wiring option (frame list G) must be applied to DIF-E1(D) frames before they can be converted to DIF-E1(MF) frames. A special in-office growth procedure is then followed for this conversion. The conversion can only take place during an office data assembler (ODA) retrofit.

## 3. Functional Description

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### Introduction

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**3.01** The DIF-E1 provides a digital transmission interface to the 4ESS switch that was previously provided by the DT/SP2. Figure 8 shows possible arrangements for the DIF-E1. On the transmission side, DS-1 signals are cabled to the DIF-E1 from the DSX-1, and LT-1 connector, or a D4 channel bank. On the switch side, DS-120 signals are cabled to the TSI. An echo suppressor terminal can be connected between the DIF-E1 and TSI if the office requires echo suppression. The DIF-E1 is capable of providing dial pulse digit reception/outputting and supervisory scan and signal distribution functions.

**3.02** The DIF-E1 functions are as follows:

- Conversion between DS-1 and DS-120 formats
- Supervisory scanning and signal distribution
- Dial pulse digit reception
- Dial pulse digit outputting
- T1 facility monitoring
- Frame diagnostics and fault recovery.

An additional function provided by the DIF-E1(MF):

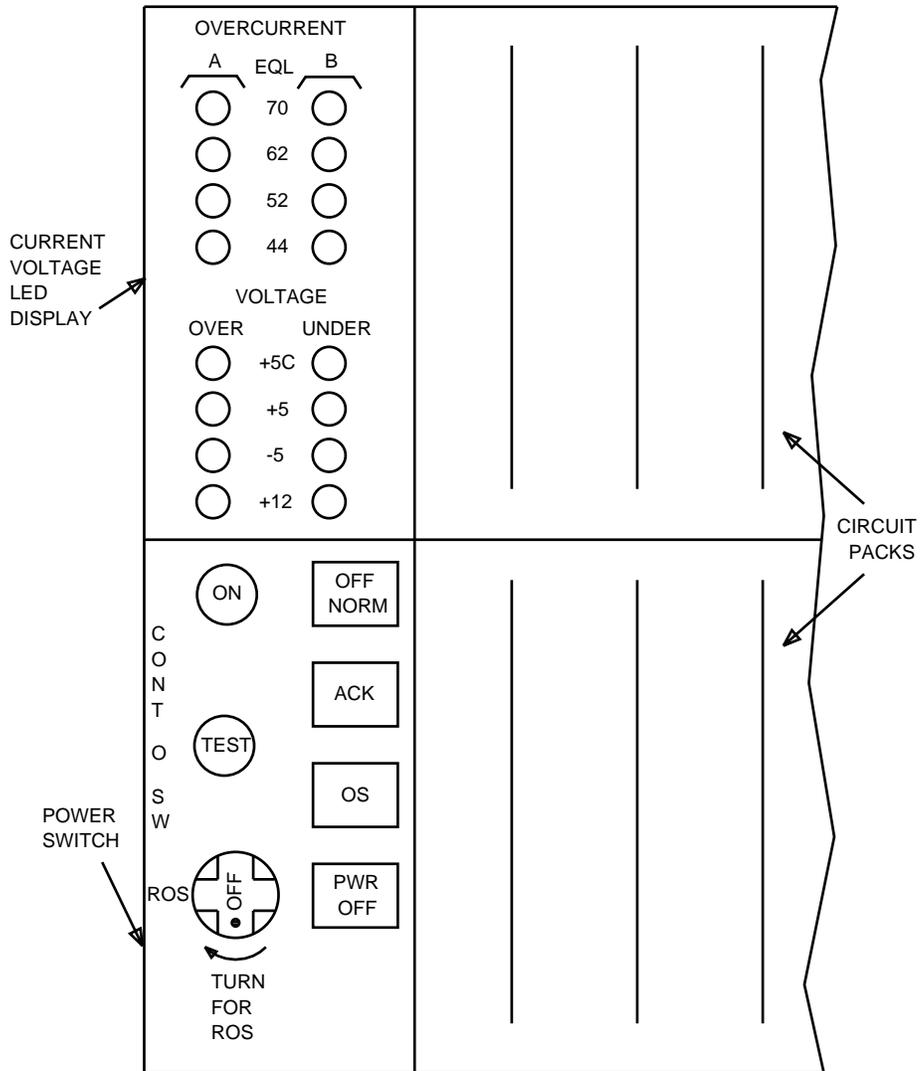
- Multifrequency digit reception/outputting.

Additional functions provided by the DIF-E1(DTMF) are:

- DTMF digit reception/outputting
- Dial tone outputting.

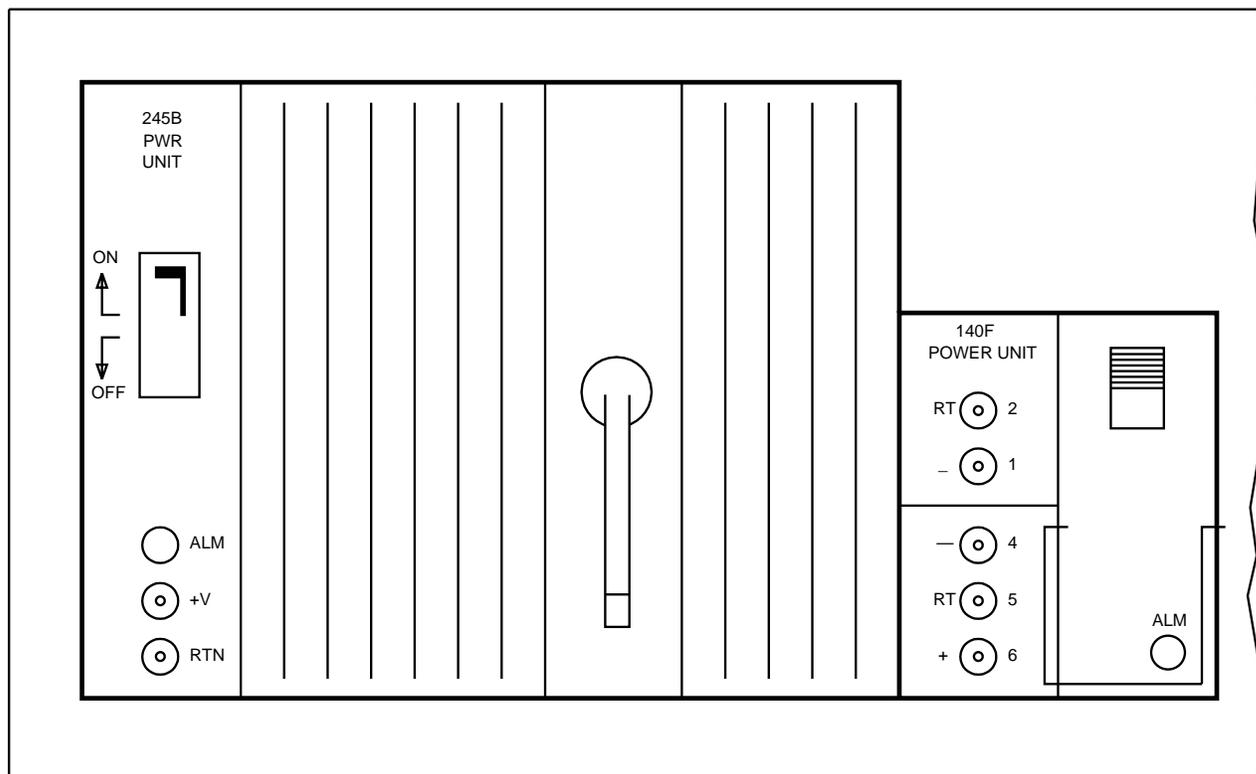
Additional features provided by 4S feature signaling:

- CSDC
- IADC.



NOTE: Right and left sides of the shelf are mirror images of each other.

Figure 3. Power Switch and LED Display



**NOTE:** Right and left sides of the shelf are mirror images of each other.

**Figure 4. Power Unit Shelf**

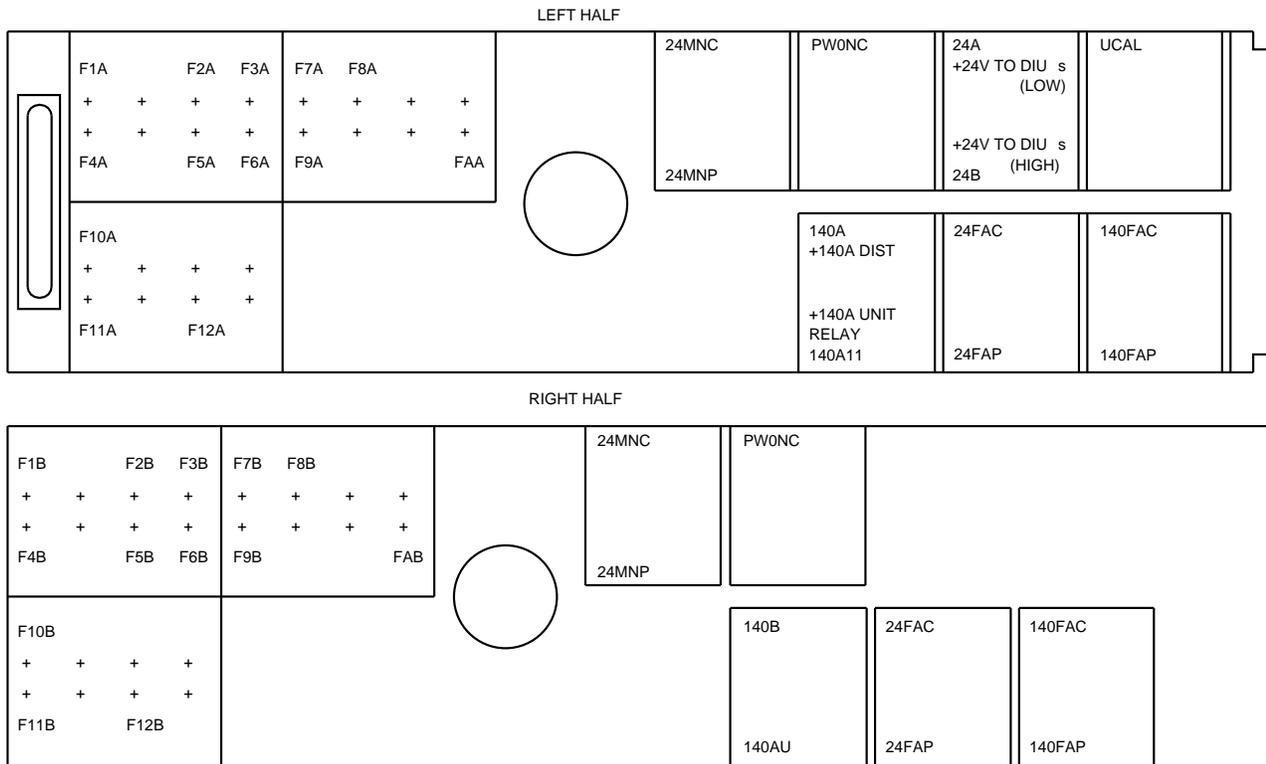
**3.03** Additional features provided by the N/DMI feature are as follows:

- Framing format
- Zero code suppression
- Signaling format
- Signaling translation.

**3.04** A digital interface functional block diagram is shown in Figure 9. This diagram illustrates how the various components of the DIF-E1 are

connected. The functions of these various components are covered in detail in the following paragraphs.

**3.05** The portion of the DIF-E1 that provides a transmission interface is the DIU. The portion of the DIF-E1 that provides a signaling interface, and a control interface, and autonomously maintains the frame is the DIC.



**Figure 5. Fuse and Alarm Panel**

**3.06** A brief discussion of the DIC architecture is necessary before describing the DIC functions. The DIC (Figure 10) is comprised of the following entities:

- (a) **Peripheral unit bus(PUB) Interface:** Transfers control data between DIC and PUB which interfaces the CC.
- (b) **Internal bus (IB):** Transfers control data to/from the PUB. The IB also serves as the communication link between all functional entities of the DIC.
- (c) **Executive controller (EXEC):** Sequences and controls the execution of peripheral orders and controls routing of intra-DIC data.
- (d) **Digital interface signal processor (DISP):** Executes supervisory scan and signal distribution and reception/outputpulsing of dial pulse (DP) digits. It also performs multifrequency digit reception/outputpulsing in

the DIF-E1(MF) and DTMF digit reception/outputting in the DIF-E1(DTMF).

- (e) **Buffer random access memory (RAM):** Contains buffer space for four DISP operational buffers and a maintenance report buffer. The four operational buffers are incorporated in the same way as their SP2 counterparts.
- (f) **Maintenance microprocessor (MMP):** A microprocessor employed for DIU maintenance functions, fault recovery, and diagnostics.
- (g) **Internal Registers:** Various registers are provided for configuration control and error status reporting, such as the status register, error-source registers, pest register, exercise register, protection switch register, and the controller primary error-source register.
- (h) **Message Accounting Processor (MAP):** A hardware sequencer that is used only in the DIF-E1(D) to generate periodic pulses with programmable rates. The MAP interfaces with the DISP as shown in Figure 11.

## Controller Functions

**3.07** The DIC is fully duplicated and has an active role in call processing and control of fault reconfiguration, fault recovery, and maintenance. The DIF-E1(D) has the same type of peripheral identification number as the SP1s and SP2s and uses exactly the same CC commands for all processing. Therefore, the CC does not have to distinguish between the DIF-E1(D) or DIF, SP1, and SP2 when sending signaling orders on the related PUB. However, the CC must distinguish between the DIF-E1(MF) and other frames when sending newly defined orders for controlling digital MF service circuits. Also, there are newly defined orders for the DIF-E1(DTMF) and the 4S features.

### A. Internal Bus

**3.08** A simplex controller is a combination of processors, sequencers, and buffers

interconnected by the internal bus (IB). Data on the IB is sequenced and routed by the EXEC. All functional entities of the DIC have ports on the IB. The PUB receive/reply logic provides 1A/1B processor read/write access to the DIC. The MMP and DISP can also initiate actions on the IB. Routine maintenance and/or initialization of controller functional entities are MMP associated activities. The reports of the DISP are managed by the EXEC and read by CC after CC buffer polling. The controller can also function in the maintenance mode where the MMP and EXEC are used to exercise the DISP.

**3.09** The PUB terminates in the PUB access circuitry in the DIC. Both PUB 0 and PUB 1 can be used by either DIC 0 or DIC 1. This is the standard 4ESS switch full bus access. Real-time clock is supplied to the DIC by two duplicated master timing links from a TSI. Each controller derives and distributes clock signals to drive the DIU functions.

### B. Executive Controller

**3.10** The EXEC, a bit-sliced microprocessor, sequences distribution of intra-DIC operational orders. In addition, the EXEC controls the operation of the DISP. When a controller is in the standby mode, the EXEC and MMP can be coupled to execute maintenance checks on the DIF-E1. In addition, the EXEC administers the SP generated trunk reports.

### C. Digital Interface Signal Processor

**3.11** The DISP is a read-modify-write structure and is primarily used for scanning and distributing supervision data for the trunks connected to the DIF and DIF-E1. Each status word represents the present state of the associated trunk. The SP state translation store (STS) is a RAM resident state table description of all the call states which the SP is programmed to interpret. Every DIF-E1 trunk is processed once every 10 milliseconds. A state table look-up technique is used to update the current state of the trunk. If the updating state is a report state, the SP sends a report interrupt to the EXEC. The EXEC, in turn,

reads the pending report and loads it to the appropriate call activity buffer in buffer RAM.

**3.12** The DISP provides the following signaling functions:

- Continuous scanning and reporting of incoming trunk signaling
- State changes (supervisory scanning)
- Control of outgoing trunk signaling states (signal distribution)
- Dial pulse digit reception
- Dial pulse digit outpulsing
- MF digit reception/outpulsing on digital MF service circuits.
- DTMF digit reception/outpulsing on digital DTMF service circuits.

**3.13** Signaling in the DIF-E1 is treated on a 128-trunk basis with 120 voice trunks and 8 virtual trunks for exercise and internal maintenance. The DISP serially processes signaling during regularly scheduled intervals.

**3.14** The E-lead information scanned (every 10 milliseconds) by the DISP involves two functional units, the E-scanner and the E-store. A 1 Mb/s bit stream carries E-data for up to 32 working DIUs and two spare (protection switch) DIUs to the E-store. The E-store is continually updated by the E-scanner. The E-scanner is maintained by circuitry which is duplicated and matched within a simplex controller and by looped M-data to E-data on virtual trunks (time slots 120 through 127).

**3.15** The DISP autonomously writes M-data into the M-store for all trunks on the DIF-E1, and the CC controls supervisory states with direct write orders. The M-distribution supplies all DIUs (including protection switch spares) by a single serial bit stream from the M-store. Each DIU link is protected by parity over the bit stream and looping of M-data to E-data on the virtual trunks.

**3.16** The per channel inhibit signal (PCIS) function inhibits M-signaling on a per-channel basis. The function of inhibiting M-signaling is designed for use with data transmission or with a nailed-up connection (reserved or predetermined electrical path). When M-signaling is inhibited by an order from the CC, the 4ESS switch becomes transmission transparent to the trunk(s) involved except with zero code suppression.

**3.17** Buffer space is reserved in the DIC for the DISP operational buffers (seizure, digit, high- and low-priority) and a maintenance reporting buffer.

**3.18** In the DIF-E1(MF) and DIF-E1(DTMF), the EXEC can access six bits of the E, M, and PCIS stores simultaneously. In the MF/DTMF DIUs, these six bits are used to control and communicate with an MF/DTMF receiver/transmitter pair.

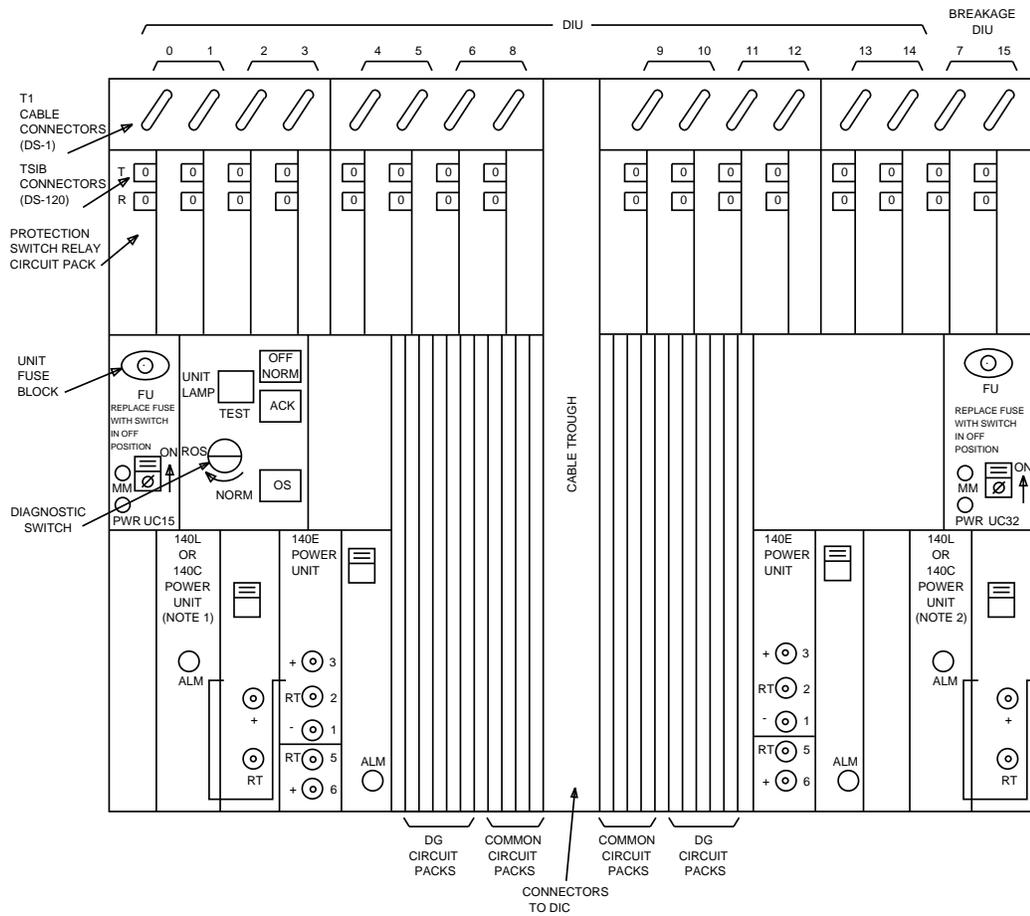
**3.19** The format of the MF/DTMF orders is different from the format used in the DIF-E1(D). Therefore, "frogging" (internal bus bit manipulation) is utilized in order to manipulate the bits or fields into their proper positions on the DIC internal bus.

**3.20** A shadow memory of the E-store provides the ability to do multiple E-bit reads as well as maintain access to the E-store when the MF DIU is protection switched.

**3.21** In MF/DTMF DIUs, 96 of the 128 available M, PCIS, and E data bits are used for communication between the DISP and the digital service circuits.

## D. Maintenance Microprocessor

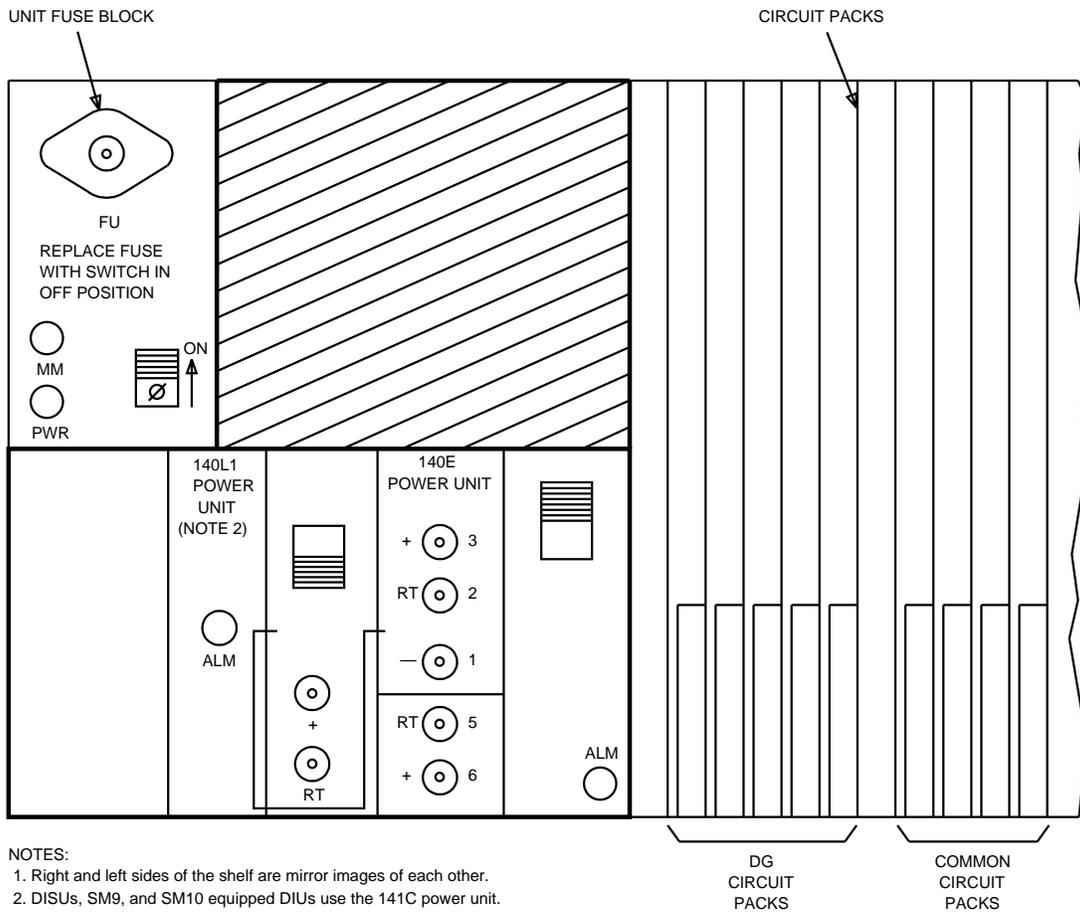
**3.22** The 24-bit internal bus provides functions as a communications interface for all intracontroller functions. This bus is controlled by the EXEC. The MMP uses this bus to communicate with the remainder of the controller. On the other hand, the MMP uses serial data links to communicate with the DIUs. Unit maintenance functions performed by the MMP are as follows:



- Notes:
1. The DIUs equipped SM9 and SM10 use the 141C power unit
  2. The protect switch spare DIU's SM9, and SM10 equipped DIU's use the 141C power unit.

**LEGEND:**  
 ALM - ALARM  
 COMMON - SM2-5  
 DG - DIGROUP  
 DIC - DIGITAL INTERFACE CONTROL  
 DMI - DIGITAL MULTIPLEX INTERFACE  
 FU - FUSE  
 MM - MAINTENANCE MODE  
 OS - OUT OF SERVICE  
 PWR - POWER  
 RT - RETURN  
 SM - S-TYPE CONNECTOR, M-TYPE BOARD  
 TSIB - TIME-SLOT INTERCHANGE 'B'

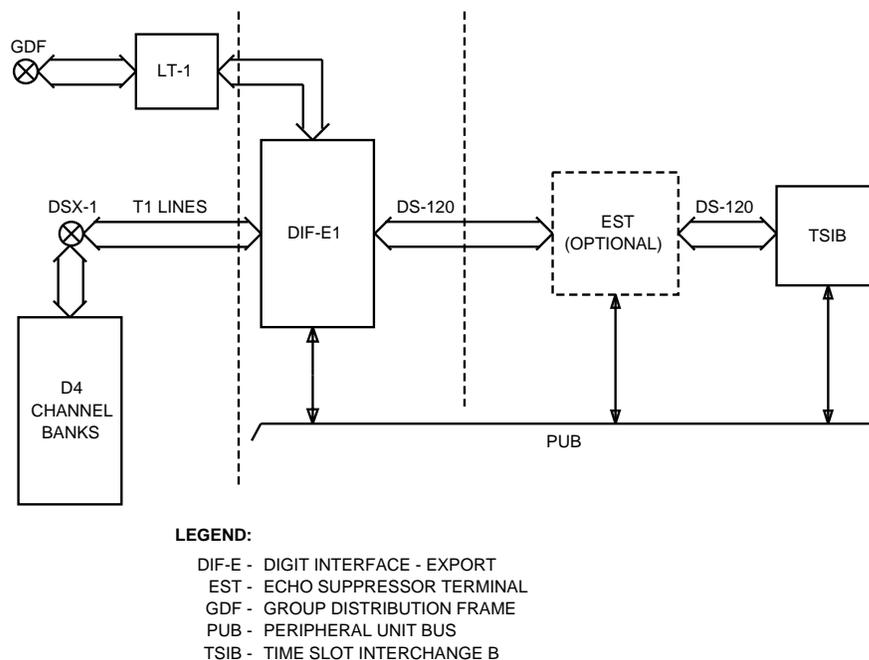
**Figure 6. Input/Output Protection Switch Relay and Digital Interface Unit Shelf**



NOTES:  
 1. Right and left sides of the shelf are mirror images of each other.  
 2. DISUs, SM9, and SM10 equipped DIUs use the 141C power unit.

**LEGEND:**  
 ALM - ALARM  
 COMMON - SM2-5  
 DG - DIGROUP  
 DISU - DIGITAL INTERFACE SERVICE UNIT  
 DIU - DIGITAL INTERFACE UNIT  
 FU - FUSE  
 MM - MAINTENANCE MODE  
 PWR - POWER  
 RT - RETURN  
 SM - S-TYPE CONNECTOR, M-TYPE BOARD

**Figure 7. Digital Interface Unit**



**Figure 8. Interface with 4ESS™ Switch**

- Unit error-source scanning [error-source register (ESR) monitoring]
- Hit timing
- Collecting and reporting of facility reports (out-of-frame, slips, etc.)
- Routine exercise of DIUs
- Audits of MAP and SP data stores — DIF-E1(D)
- Audits of MMP and SP program stores — DIF-E1(D).

**3.23** Status reports are continuously sent from the DIUs to the MMP in a multiplexed bit stream. The MMP generates the data to be sent on the unit maintenance bus (UMB). The UMB message formatter (located on the MMP external bus) receives messages from the MMP. The

messages are reformatted and retimed from parallel to serial format before being sent to the DIUs on the UMB. The unit scanner/preprocessor receives DIU ESR and report-function raw data from all the DIUs. The data is then multiplexed, reformatted into 8-bit parallel format, and delivered to the appropriate part of the MMP memory for processing.

#### **E. Internal Registers**

**3.24** Various internal registers in the DIC function as the following:

- Status registers
- Reply registers
- Error source registers

- Receive registers
- Exercise registers
- Protection switch registers.

## Digital Interface Unit Functions

**3.25** The DIUs (Figure 12) provide the same type of transmission interface as the digroup terminal units. In addition to the usual tasks of line clock recovery, signal regeneration, and framing, the DIU:

- Synchronizes each T1 line to the network clock
- Extracts and inserts signaling information (does not update signaling when framing errors, out-of-frames, or slips are detected)
- Detects digroup failure alarms
- Detects framing errors which indicate T1 line performance
- Monitors slips and slip polarity
- Provides maintenance exercise access and ESRs to readily detect failures
- Provides necessary multiplexing and demultiplexing of data
- In the DIF-E1(MF) (up to four of the DIUs) may also be used to provide digital MF service circuits
- In the DIF-E1(DTMF) (up to four of the DIUs) may also be used to provide digital DTMF service circuits
- Provides 4S features (CSDC and IADC).

**3.26** The DIU performs several functions on a per-digroup basis that the digroup terminal unit treats as common control functions. This allows use of large scale integration. Maintenance complexity is reduced because the per-digroup arrangement eliminates the need for many reference signals and vector generators.

**3.27** The DS-1 receive section of the DIU terminates five incoming T1 lines, recovers line timing, extracts signaling, and converts the incoming data into a form suitable for multiplexing into a DS-120 signal.

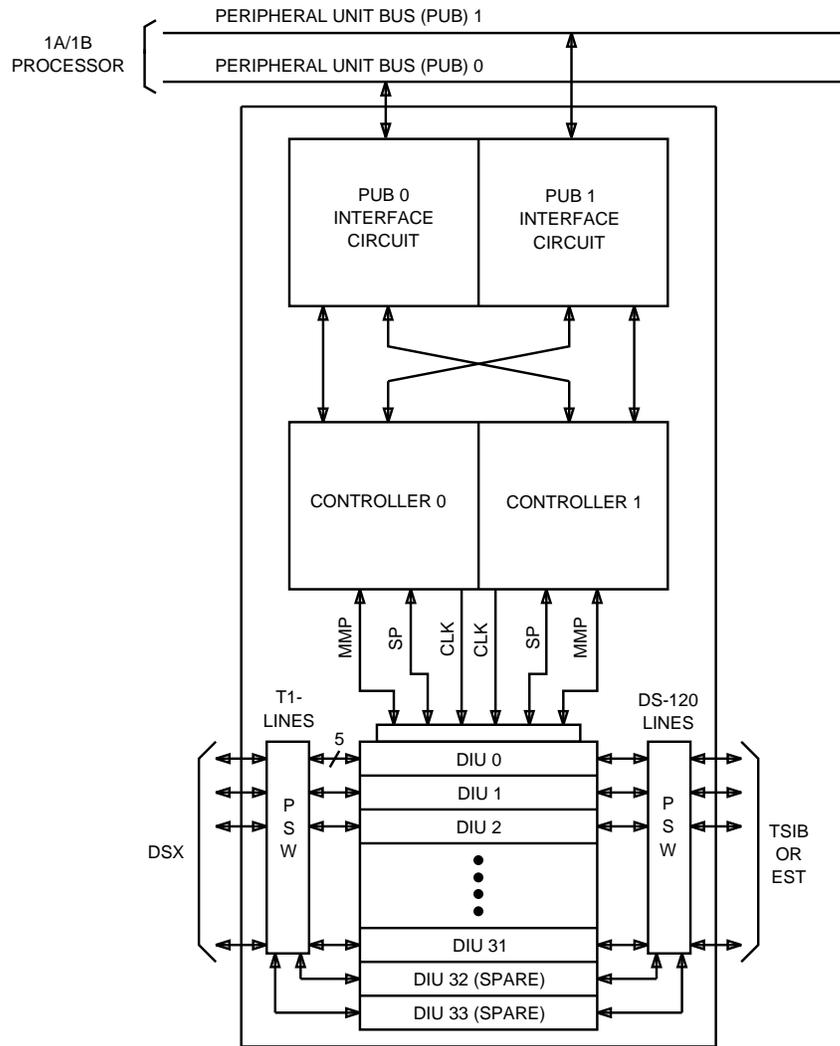
**3.28** In the DIF-E1(MF)/(DTMF) DIUs, only one T1 line is terminated. The remainder of the DIU is dedicated to providing MF/DTMF signaling.

**3.29** Also, the DS-1 transmit section receives parallel data from the DS-120 interface. This data is demultiplexed into digroups and converted to a 1.544 Mb/s serial signal with proper framing information. Part of the conversion process inserts signaling information.

**3.30** The DS-120 receive section terminates the TSI coaxial cables, amplifies the pulse code modulation data from the TSI, and converts the serial bit stream to parallel format. The data signal framing is determined and the parallel data is sent to the DS-1 interfaces.

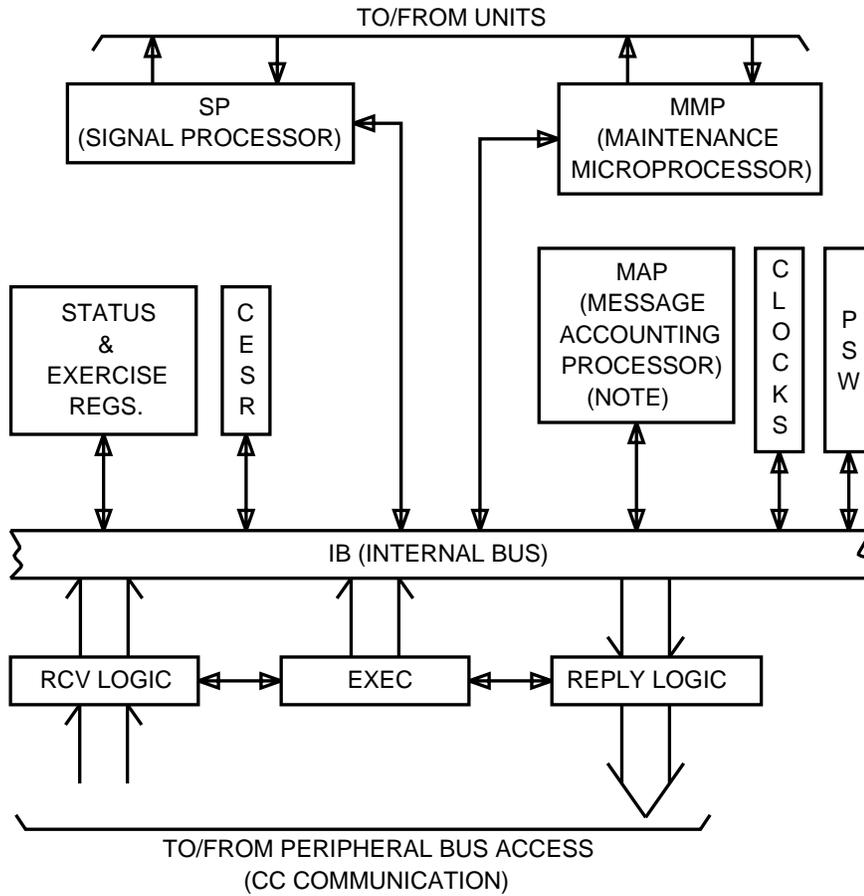
**3.31** The DS-120 transmit section receives parallel formatted data from the DS-1 interface. This parallel data is reclocked and reformatted into a 16.384 megabaud/second serial bit stream before being sent to the TSI.

**3.32** The two output data streams from the DIU go through the control interface circuit pack SM2. The first data output is the E-signaling data stream from the T1-lines. This data consists of repeating 128 bits every 125 usec and data is sent to both DISPs. The second data output is the maintenance bit stream. It is also a repeating 128 bits every 125 usec and goes to both MMPs. The E-signaling bits contain five digroups of 24 bits each plus 8 virtual bits that are the repeats of the M-data virtual or the PCIS-data virtual bits. The report data of the maintenance bit stream contain five digroups of 24 bits of ESRs plus 8 common alarm bits. The ESR of each digroup has 6 bits of hardware detected errors, 12 bits of T1-line status, and 6 bits of hardware status. For details on these bits, refer to LTP 234-310-107, *Lucent Technologies Practices, 4ESS™ Switch, Maintenance Reference Handbook*.



**LEGEND:**  
 EST - ECHO SUPPRESSOR TERMINAL  
 DIU - DIGIT INTERFACE UNIT  
 PSW - PROTECTION SWITCH  
 TSIB - TIME SLOT INTERCHANGE B

**Figure 9. Digital Interface Functional Block Diagram**

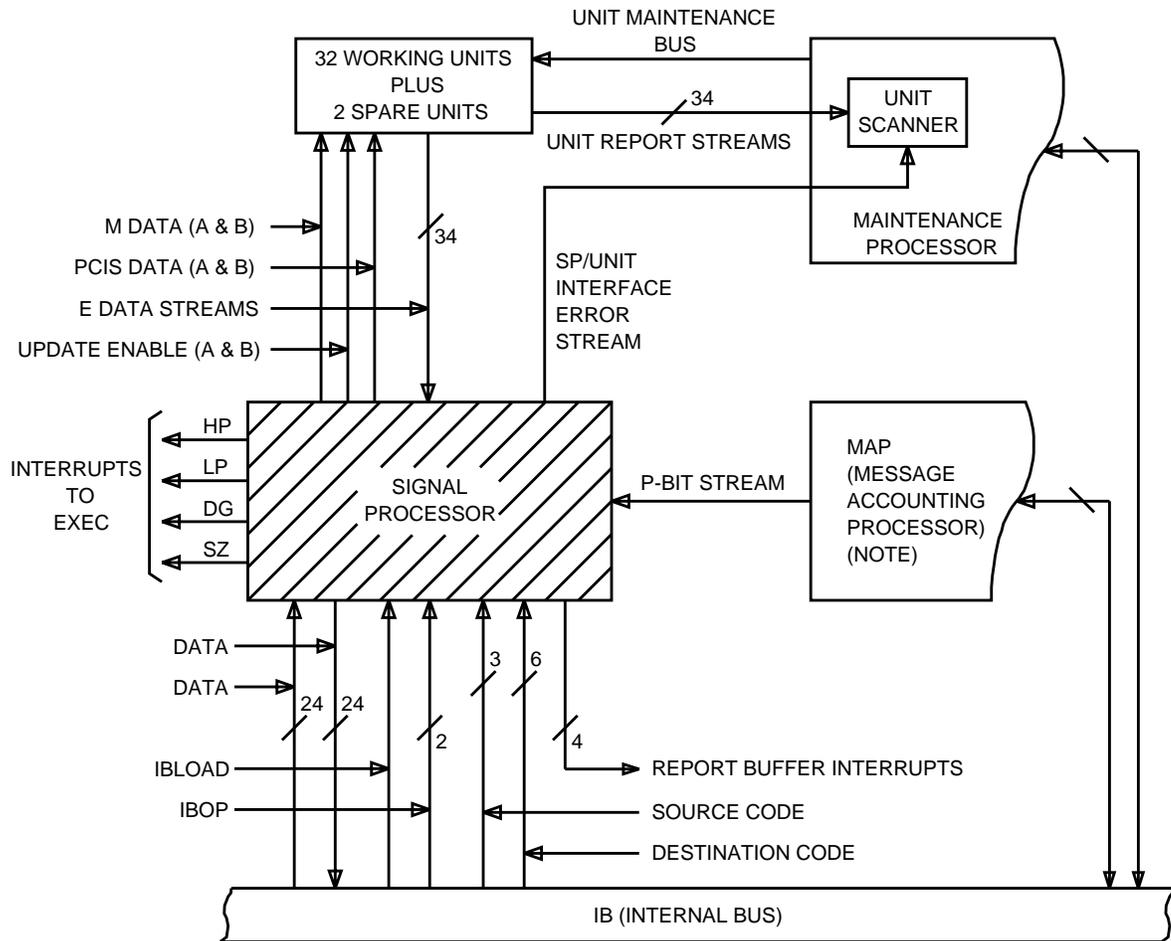


**NOTE:** The MAP complex is used only in the DIF-E1 and DIF-E1(D).

**LEGEND:**

CESR - CONTROL ERROR SOURCE REGISTER  
 PSW - PROTECTION SWITCHES  
 RCV - RECEIVE

**Figure 10. Digital Interface Controller — Block Diagram**



**NOTE:** The MAP complex is used only in the DIF-E1 and DIF-E1(D).

**LEGEND:**  
 IBOP - INTERNAL BUS OPERATION  
 PCIS - PER CHANNEL INHIBIT SIGNAL

**Figure 11. Signal Processor Input/Output — Block Diagram**

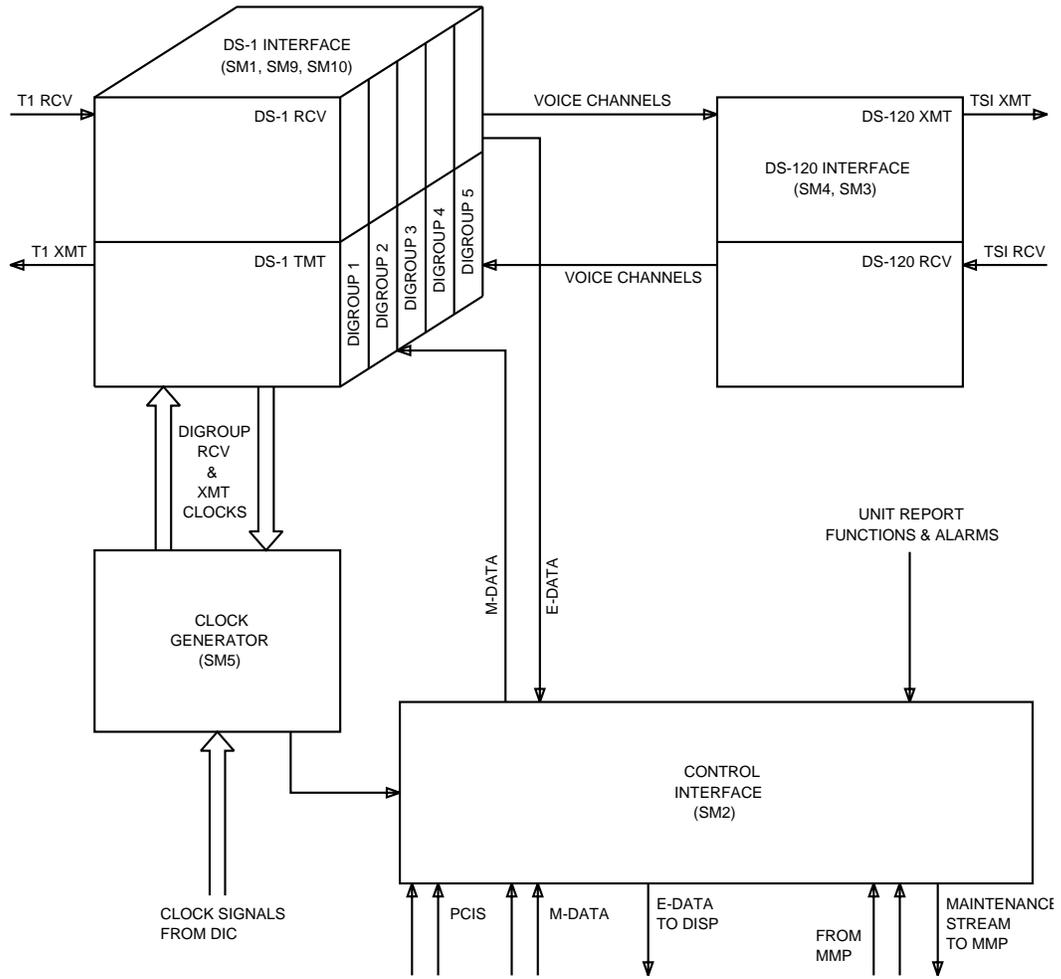


Figure 12. Digital Interface Unit — Block Diagram

**3.33** The SM1B, SM9, and SM10 circuit packs perform the T1-line interface. The SM1B (and also SM1) circuit packs only handle T1-lines in the superframe (SF) framing format, robbed bit (RB) signaling format, 2-state (2-ST) signaling translation, and zero code suppression (ZCS). The SM9 circuit pack, introduced in 4E11 generic to replace the SM1B circuit pack, can be configured to 50 different T1-line modes.

**3.34** The SM9 can handle extended superframe (ESF) framing format, network digital multiplexed interface with bit oriented signaling (N/DMI) format, 4-State (4-ST), customer switched direct connect (CSDC) and integrated access direct connect (IADC) signaling translations, and bipolar with 8 zero substitution (B8ZS) and no zero code suppression (noZCS) zero code treatment. The SM9 provides two additional modes. These modes are 64 clear channel capability (64CCC) in both the SF and ESF framing formats.

**3.35** The DIU equipped with SM9 circuit packs can be configured to any one of 50 different modes. Each mode has a specific combination of T1 facility characteristics which are chosen from the following options:

- Framing Format: Either superframe or extended superframe format can be selected.
- Zero code Suppression: All zero octets are suppressed, and zero code suppression can be completely disabled.
- Signaling Format: Bit oriented signaling can be encoded as either RB bit or N/DMI.
- Signaling Translation: Bit oriented signaling translations can be performed to provide 4-S, 4-S CSDC and IADC.

**3.36** The SM10 provides PCC for enabling/disabling echo cancellers and A/u-Law converters on a single call basis. The PCC function operates on top of the 64CCC mode only in the ESF framing format and now makes 51 different modes. The echo cancelers and A/u-Law converters are located in an advanced switchable signaling and echo canceling terminal (ASSET) in a

4ESS International Switching Center (ISC). Another transmission frame called the universal services echo canceler (USEC) terminal interfaces between the 4ESS and the long distance network only providing an integrated voice/data digital network in North America.

**3.37** The SM10 communicates with the ASSET and USEC via the 4-Kbit facility data link (FDL) with-in the framing bits of the ESF format. The protocol used for communicating is a simplified Link access procedure on the D-Channel (LAPD) only using the unacknowledged information transfer facilities. Details of the LAPD can be found in the *CCITT Red Book Volume VI, "Fascicle VI.9, Digital access signaling system; Geneva, 1985"*.

**3.38** The DS-120 line between the DIF-E1 and the TSI is a 4ESS exclusive interface and is a 16.384 Mhz signal with 120 customer trunks plus 8 trunks of maintenance.

**3.39** A description of a T1-line can be found in the latest version of *American National Standard for Telecommunications "Digital Hierarchy" "Electrical Interfaces"*. The following gives explanation of the T1-line:

- Framing Format
  - (1) SF: 1.5 msec 12 frames  
frame = 24, eight-bit channels + framing bit
  - (2) ESF: 3 msec 24 frames
- Signaling Translation
  - (1) 2-State
  - (2) 4-State
  - (3) CSDC
  - (4) IADC
- Zero Code Treatment
  - (1) ZCS: setting bit 7 in a channel containing a 8-bit zero word

- (2) B8ZS: causing 2 bipolar violations within a channel containing a 8-bit zero word
- (3) noZCS: do nothing when an 8-bit zero is to be transmitted

- T1-line Maintenance

- (1) Red Alarm: when an Out-Of-Frame condition exists for 2.5 secs +/- .5 sec.
- (2) Yellow Alarm: a message received from the far-end that they are in a red alarm state
- (3) Performance Monitoring: slips, Fe, and CRC

- Facility Data Link on SM9 and SM10

**3.40** The SM8 circuit packs were available with the 4E9 generic to the 4E14 generic to provide the 4-ST, CSDC, and IADC signaling translation on a SF framing format. These packs were recalled in 1989 so programming code could be made available in the MMP.

## Digital Interface Timing

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### A. Digital Interface Controller Timing Chain

**3.41** The DIC timing chain is illustrated in Figure 13. The MTL and 16.384 megabaud/second clock are sent from the equalizer to the framer. The framer uses MTL data to establish framing. Framing information is then sent to controller clock chains A and B and the T1 clocks. From the T1 clocks, the framing information is sent to all the DIUs. The local clock ESR receives parity information from the clock chain and reports to the primary control ESR.

**3.42** The following are clock signals provided to the DIC by clock chains A and B:

- GBCs (generated bit codes) — divide each time slot into 16 phases, define EXEC cycle time, and define read/write cycle of DISP random access memory.
- GWCs (generated word codes) — enabled by last phase of GBC counter, supply time cycle to define each time slot.
- GGCs (generated granularity codes) — enabled by the end of the GWC cycle, supply lowest rate of timing to DIUs and MMP.
- 10-Millisecond Clock — a 7-stage clock used as a timer for DISP real-time interrupts and enabled at the end of the GGC cycle.
- GBC, GWC, and GGC Parity — used to maintain the clock chains.

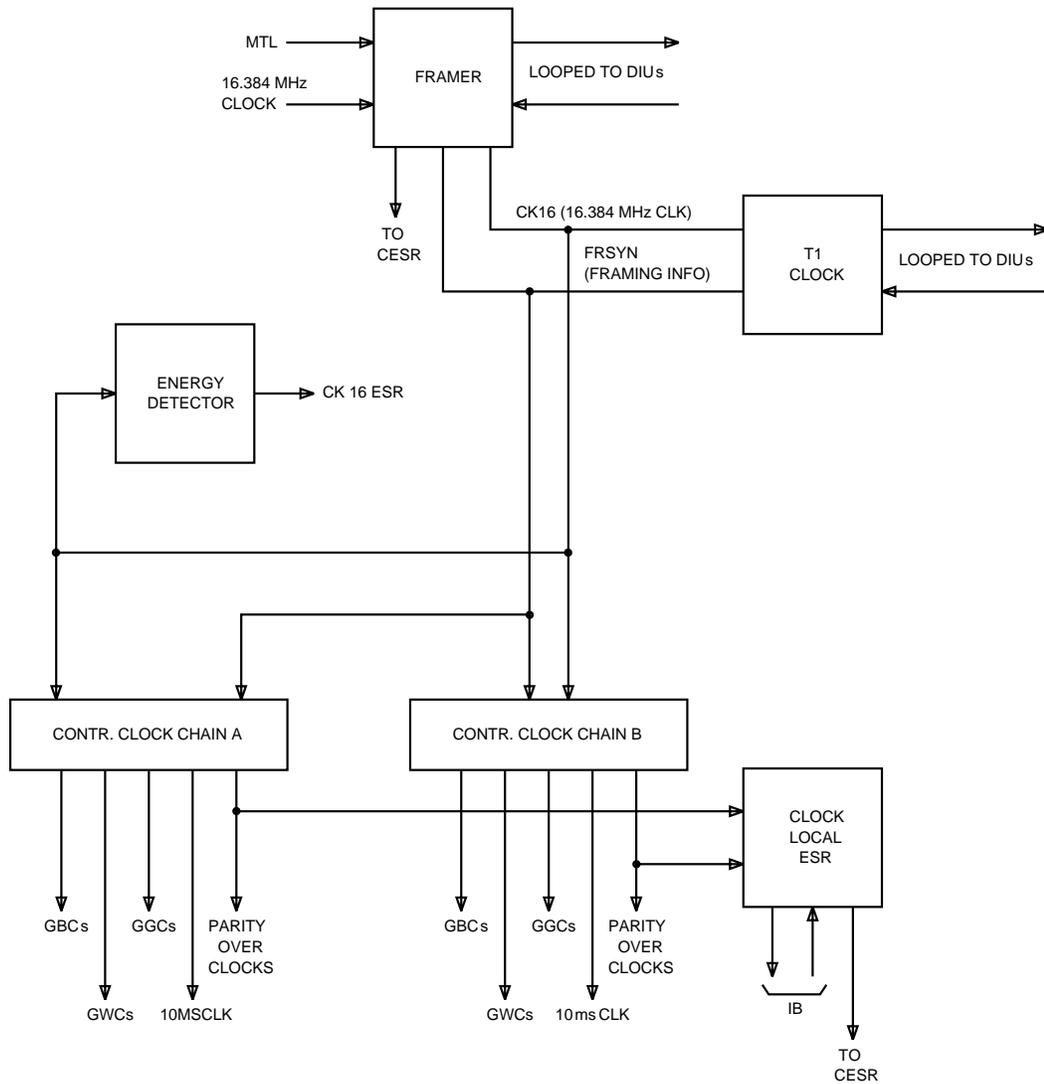
**3.43** The T1 clock chain provides clocks to the DIUs for the following functions:

- Synchronism between DIU local clocks with the DIC clocks
- DIU maintenance of local GGC clocks
- 1.544-MHz clock for DS-1 interface output
- Super frame pattern synchronizing (which identifies framing and signaling channels in DS-1 format).

### B. Clock Synchronization Between DICs

**3.44** Duplex operation of the DIC requires the clock chains in one controller to be synchronized to that of the mate controller. The GBC and GWC counters are automatically synchronized to the data of the MTLs. Clocks with cycle times greater than the GWC counter can only be synchronized to the counterparts in the mate controller.

**3.45** One controller is defined as a master and the other controller, the slave; the slave controller can be synchronized to the master controller.



**Figure 13. Digital Interface Controller Timing Chain**

**3.46** All counters duplicated within a simplex controller need to be synchronized. Upon order of the CC, all duplicated counters (with cycle times greater than the GWC counter) are jam set to the same state.

**3.47** Cross-controller synchronization is done with signals from the GGC clock, 10-millisecond clock, and the super frame pattern generator. These signals are sent to their counterparts in the mate controller. After 64 milliseconds, the slave is synchronized with the master, and the cross-controller connections are removed.

**3.48** Once cross-controller synchronization is established, each signal sent to the mate is matched against the locally generated signal in the mate. When a mismatch occurs, an indicator is marked in the local clock ESR which, in turn, reports to the control error source register (CESR).

## 4. Power

### Power Requirements

**4.01** The power requirement for the DIF-E1 is approximately 2400 watts. This is equal to one-third of the requirement for a DT/SP complex.

**4.02** Each DIF-E1 is supplied with duplicated +140 volt and +24 volt power feeders (A and B distributions) for the basic input power. The 140-volt power feeder is used to supply power to the power units that provide integrated circuits with +12 V dc or  $\pm 5$  V dc. The 24-volt feeder provides power for alarm relays, power control circuitry, IPUB drivers, indicator lights, and protection switch relays. The power feeders are filtered, then fused on the fuse and alarm panel at the bottom of Bay 1.

**4.03** Power for the DIC (Bay 1) is distributed from the fuse and alarm panel as follows (Figure 14):

- +140 volt feeder fused to power unit shelf
- 140F (-5 volts) and 245B (+5 volts) power units to DIC circuits via bus bars and printed backplane wiring panels
- 140A (+5 volts) power unit distributed to PUB interface circuits
- +24 volts to power sequencing circuit, power switches, and LEDs.

**4.04** The DIUs Power (Bays 0 and 2) is distributed from the fuse and alarm panel as follows (Figure 15):

- Distribution A supplies power to all odd numbered (0 through 31) DIUs.
- Distribution B supplies power to all even numbered (0 through 31) DIUs and spare protection switch DIUs (32 and 33).
- +140 volts are supplied to DIUs in each bay by FAUL, FBUL, FBUH, and FAUH master fuses.
- Each DIU is fused in a fuse block at the side of the shelf designated FU.
- Two power units are associated with the DIUs; a 141C or 140L (+5 volts), and 140E (+12, -5 volts).
- Each fuse and power unit is tied to the office alarm.
- A blown fuse activates the minor alarm.

All fuses used in the DIF-E1 are indicator fuses that trigger an alarm when blown. The maximum current drain for a fully equipped DIF-E1 is:

- +140 volts (A) 8.3 amps
- +140 volts (B) 8.3 amps
- +24 volts (A) 1.7 amps
- +24 volts (B) 1.7 amps.

The maximum +24 volt current drain is not a function of office activity. This current drain

depends on the maintenance status of a frame. When a DIU is protection switched (in the maintenance mode), more current is drawn than when the frame is in a normal state. Therefore, it is unlikely that all the DIF-E1s in the office will draw maximum current at the same time.

## Power Control and Alarms

**4.05** Four power entities, DIC 0, PUB 0 interface, DIC 1, and PUB 1 interface, are separately controlled. All entities work similarly for powering up and down, power sequencing, and alarming. The DIC 0 and differences among other entities are discussed in the following paragraphs.

**4.06** The DIC 0 incorporates a power control switch, power control and alarm circuit, LED display, a pair of scan points, and SD points to the base of the office. The power switch uses a closure to start the power-up procedure. The power control and alarm circuit performs a self-check on its voltage and current monitors before allowing power to turn on. While power is on, all voltages and the +5 volt circuit currents are continuously monitored. Detection of any voltage or current out of limits causes the power units to shut down and an appropriate alarm to be given. Two scan points give the power switch the capability of reporting in four different states:

- Power on
- Power off
- ROS (request out of service)
- Power alarm.

**4.07** A power alarm exists whenever the controller loses power without being manually powered down. This condition is caused by a blown +24 volt or +140 volt fuse to a power unit or detection of out-of-limit current or voltage.

**4.08** Two SD points light the lamps on the power switch to indicate that the CC acknowledges a ROS request or an out-of-service controller. The following are definitions for the major (MJ) and minor (MN) alarms for the DIF-E1:

- MJ alarm — failures affecting controller service — power unit shutdowns and fuse failures on major control hardware
- MN alarm — nonservice-affecting failures — fuse failures in power leads for lamps or LEDs and loss of +24 volt to protection switch circuits and +140 volt to a unit.

## Power Sequencing

**4.09** Each power entity has a power sequencing circuit. Controller and bus interface entities have different requirements for power sequencing. A power entity in any state (powering up or down) does not adversely affect the operation in the other three power entities, the DIUs, protection switching circuits, or generated autonomous peripheral unit failure or autonomous peripheral unit trouble alarms.

(a) When powering down the bus entity:

- The power switch is turned off.
- The +24 volts to the associated cable drivers is removed before PUB interface power unit primary is opened.

(b) When powering up a bus entity, +5 volt power is applied before the +24 volt power is applied to the cable drivers.

(c) When powering down a controller:

- The power switch is turned off.
- The PUB interface leads are disabled.
- The select leads to the DIUs are disabled.

(d) When powering up a controller:

- The power switch is on — starts power unit outputs.
- The select leads remain disabled.
- The controller is released from cut-off state.

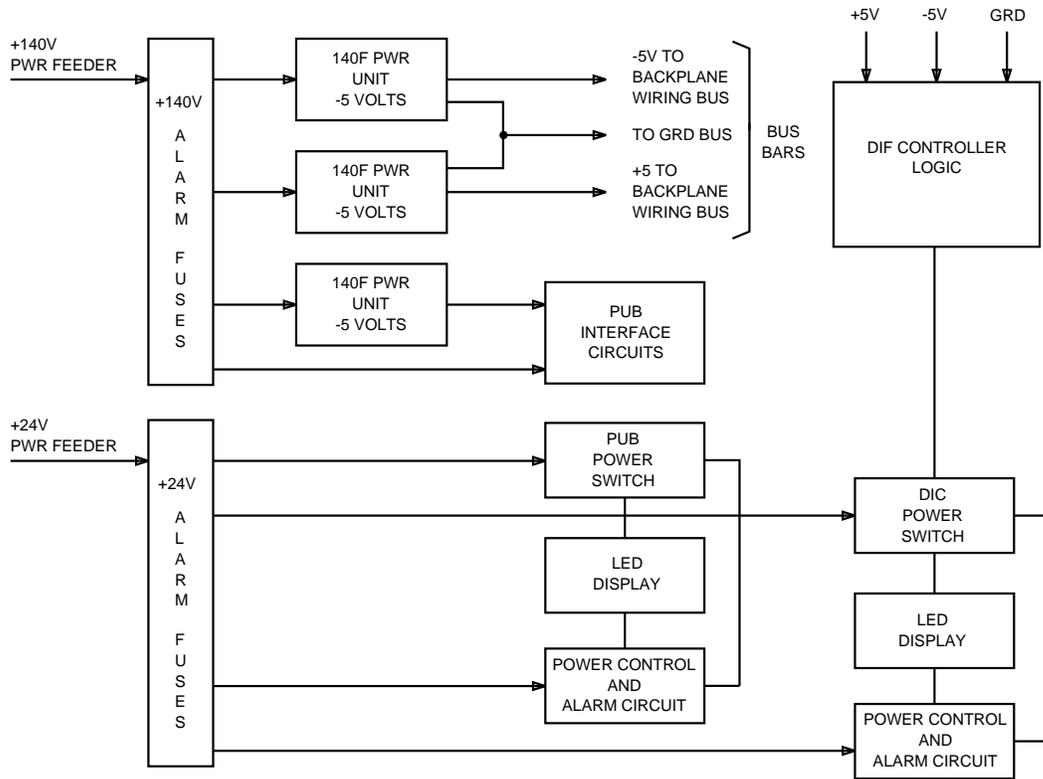
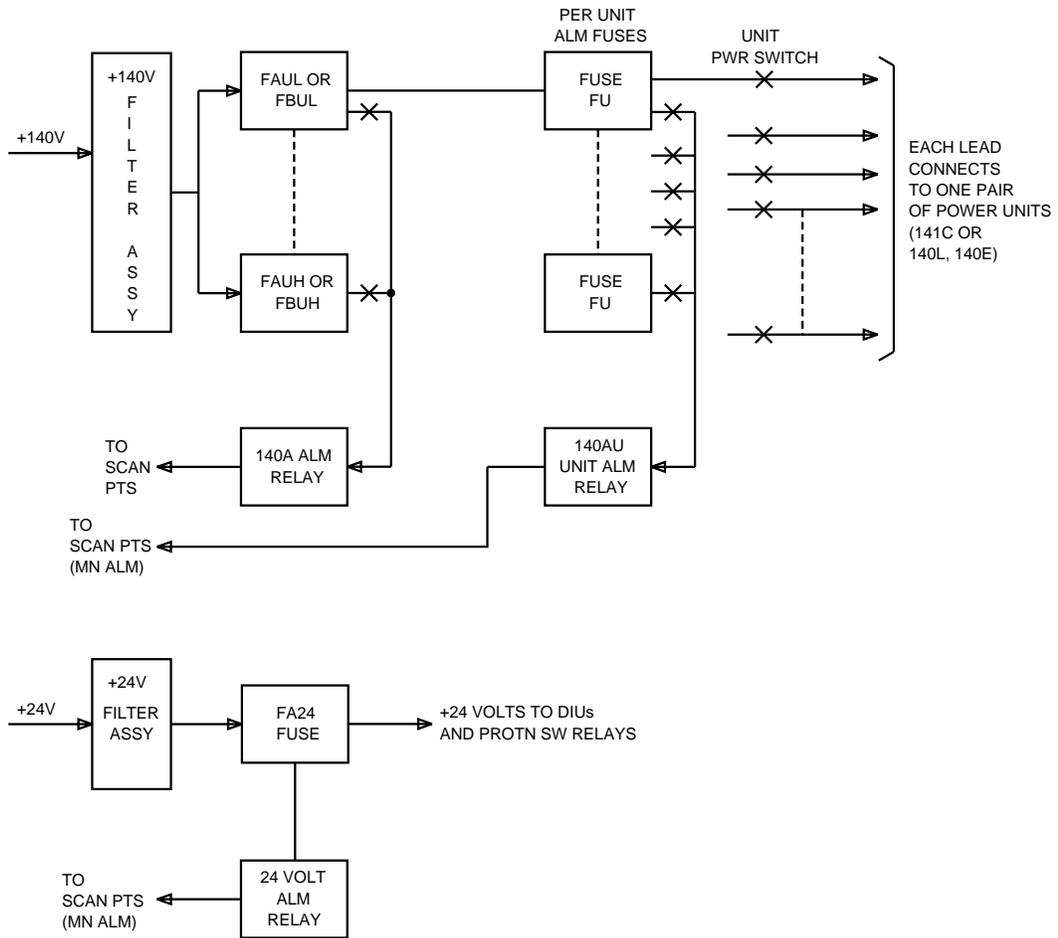


Figure 14. Digital Interface Controller Power Distribution



**NOTE:**  
 1. The +140 and +24V power distributions are each duplicated.  
 The A distribution powers the odd numbered DIUs plus DIU0  
 and the B distribution powers the even numbered DIUs plus  
 the two spare DIUs (32 and 33).

**Figure 15. Digital Interface Unit Power Distribution**

## 5. Maintenance

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### Introduction

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**5.01** The large capacity of the DIF-E1 (3840 trunks) requires rigid reliability and maintenance standards. Primarily, each DIC must be fully capable of stand-alone operation. This is true for maintenance and operational functions. In addition, the controllers must be independently maintainable, implying minimal cross-controller matching.

**5.02** Faults which affect the normal response of scan or SD processing are automatically detected by the maintenance logic within the switching center. Faults which affect T1 terminations and unit processing are automatically detected by the DIF-E1. Both types of faults can be diagnosed, repaired, verified good for service, and restored to normal operation.

**5.03** All DIF-E1 hardware is modularized with clearly defined boundaries for easy fault recognition and quick repair. Unequipped portions of the DIF-E1 should not cause any failure modes that would interfere with normal operation.

### Maintenance Software

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**5.04** The maintenance and recovery strategy used by 4ESS switch equipment is separated into five levels. These levels are phase, interrupt, interject, base, and diagnostic isolation. The phase level is the most severe since it can cause a service interruption. Phase levels are caused when a failure seriously hinders operation or if reinitialization of part or all of the system is required for recovery. The interrupt level is the second most serious level. The F-level interrupt is used by the DIF-E1 to notify the 1A/1B Processor of failures associated with the controller. The third and fourth most serious levels are the interject and the base. These levels are reserved for DIU failures. A base level has less effect on the system than an interject. Diagnostics is the lowest level

and it is used to specifically determine which circuitry, if any, has failed. Diagnostic levels are separated into phases, and each phase is responsible for checking a specific part of DIF-E1 circuitry. Phases used by the diagnostic level should not be confused with a phase level (most serious of the five levels being discussed).

**5.05** Software controlled diagnostics and fault detection coupled with microprocessor and large scale integration technology give the DIF-E1 a large degree of autonomy. For example, DIU faults are detected from data sent to the MMP on a multiplexed data bus.

**5.06** Exercises are used to periodically test error-source registers and matchers in the unit. The DIU exercise routines can test digroup equipment when the DIU is protection switched. The DIC has a set of exercise routines to test the ability of the DIUs to do the following:

- Detect framing errors
- Reframe
- Detect forced D2 (second bit of a pulse code modulated data stream used to stimulate the yellow alarm)
- Send forced D2 (yellow alarm)
- Transmit/receive signaling
- Detect errors from digital MF/DTMF service circuits in the DIF-E1(MF)/(DTMF).

**5.07** Faults capable of generating hardware maintenance interrupts or interjects are diagnosed by the DIF-E1 diagnostic software package. The objective of this software is to diagnose the fault down to a minimum number of circuit packs. The average number of circuit packs that the fault is diagnosed to is four.

**5.08** The DIF-E1 hardware is designed to have minimal impact on existing call processing software. Since the DIF-E1 does not have a supplementary matrix (for miscellaneous scan and SD functions), the correspondence between DIF-E1s and SPs is not exact. Also, implementation of the unit signaling processor is different from that

function in the SP2, resulting in minor changes in the data response of certain peripheral orders. Two new MF orders are implemented for use with the digital MF service circuits.

**5.09** The DIF-E1 diagnostic software follows the standard guidelines for peripheral diagnostics used with a 4ESS switch. The DICs can be diagnosed independently of the DIUs. The diagnostics are separated into demand phases, which are manually initiated, and routine phases, which are run on a scheduled basis by the CC. Any service-affecting tests are demand phases to minimize service degradations when diagnostics are being run.

### **Facility Fault Recovery**

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**5.10** The MMP detects errors in a facility and reports to the fault recovery software which then gathers the data and puts it into the proper format to report to trunk maintenance. Two new facility alarms have been added to support the N/DMI-BOS feature. These are the LSA (local subframing alarms) and the RSA (remote subframing alarms). Also, the following software modifications have been added to support SM9 circuit packs:

- Interface between MMP and fault recovery software to process LSA and RSA state changes.
- Interface between trunk maintenance and fault recovery software to transfer LSA and RSA status
- Memory in unit status to maintain LSAs and RSAs
- Increase in time limit for DIU initialization during various DIU configurations.

### **Digital Interface Unit Fault Recovery**

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**5.11** Unit exercise data and facility reports are sent to the MMP in a serially multiplexed bit stream. Signaling data is reported to the DISP. When a fault affecting 120 trunks is found in a DIU,

an autonomous peripheral unit trouble or maintenance report is sent to the CC. The CC interrogates the MMP for the identity of the faulty DIU. If a spare is available, the CC orders the DIC to execute a protection switch. While the protection switching relays are operating, the MMP loads the faulty unit number into the spare image number register. The spare image number register allows the spare to receive the switched unit trunk status information. To remove a protection switch, the enable bit in the protection switch register is reset. When an MF/DTMF DIU is protection switched, the spare DIU cannot perform the MF/DTMF function.

### **Digital Interface Controller Fault Recovery**

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**5.12** When a DIC fails, the standby controller goes on line as a stand-alone controller until the faulty controller is repaired. Data is sent from both DICs to all the DIUs. A pulse point is operated to isolate the faulty DIC from the DIUs, and a peripheral unit write order is used to activate the standby controller.

### **Timing Chain Maintenance**

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**5.13** Maintenance of the timing is provided at various points throughout the clock chain. Clock ESRs are used to detect the first indications of clock failures. These indications are then reported to the controller ESR.

**5.14** The next level of maintenance is done at the outputs of the controller clock chains and T1 clock chains. The clock signals from each controller clock chain are maintained by matching against the corresponding signals in the mate controller.

**5.15** Timing distributed to the DIUs is maintained by looping back and checking the clocks. An energy detector is used to check for the presence of the 16.384-MHz clock and framing information. Direct matching is used for the rest of the DIU clock signals.

## **Abbreviations and Acronyms**

4S

Four State

64CCC

64 Clear Channel Capability

### **A**

**ASSET**Advanced Switchable Signaling and Echo  
Canceling Terminal

### **B**

**B8ZS**

Bipolar with 8 Zero Substitution

**BOS**

Bit Oriented Signaling

### **C**

**CC**

Central Control

**CCC**

Clear Channel Capability

**CESR**

Control Error Source Register

**CSDC**

Circuit Switched Digital Capability

### **D**

**DIC**

Digital Interface Controller

**DIF**

Digital Interface

**DIF-E1**

Digital Interface - Export

**DIF-E1(D)**

Digital Interface - Export (Domestic)

**DIF-E1(DTMF)**Digital Interface - Export (Dual Tone  
Multifrequency)**DIF-E1(MF)**

Digital Interface - Export (Multifrequency)

**DISP**

Digital Interface Signaling Processor

**DISU**

Digital Interface Service Unit

**DIU**

Digital Interface Unit

**DMI**

Digital Multiplexed Interface

**DP**

Dial Pulse

**DSX-1**

Digital Cross-Connect Frame

**DT**

Digroup Terminal

**DTMF**

Dual Tone Multifrequency

### **E**

**ESF**

Extended Superframe Framing

**ESR**

Error Source Register

**EST**

Echo Suppressor Terminal

**EXEC**

Executive Controller

### **F**

**FDL**

Facility Data Link

**G****GBC**

Generated Bit Code

**GGC**

Generated Granularity Code

**GWC**

Generated Word Code

**I****I/O**

Input/Output

**IADC**

Integrated Access Digital Capability

**IB**

Internal Bus

**IPUB**

Interface for Peripheral Unit Bus

**ISC**

International Switching Center

**L****LAPD**

Link Access Procedure on D-Channel

**LED**

Light Emitting Diode

**LSA**

Local Subframing Alarms

**M****MAP**

Message Accounting Processor

**Mb/s**

Megabits per Second

**MF**

Multifrequency

**MJ**

Major

**MMP**

Maintenance Microprocessor

**MN**

Minor

**MTL**

Master Timing Link

**N****N/DMI**

Network/Digital Multiplexed Interface

**NoZCS**

No Zero Code Suppression

**O****ODA**

Office Data Assembler

**P****PBX**

Private Branch Exchange

**PCC**

Per Call Control

**PCIS**

Per Channel Inhibit Signal

**PLS**

Pulsed Line Signaling

**PUB**

Peripheral Unit Bus

**PWB**

Printed Wiring Board

**R****RAM**

Random Access Memory

**RB**

Robbed Bit

**ROM**

Read Only Memory

**ROS**  
Request Out of Service

**RSA**  
Remote Subframing Alarms

**S**

**SF**  
Superframe Framing

**SP**  
Signal Processor

**STS**  
State Translation Store

**T**

**TSIB**  
Time Slot Interchange

**U**

**UMB**  
Unit Maintenance Bus

**USEC**  
Universal Services Echo Canceler

**Z**

**ZCS**  
Zero Code Suppression

# How Are We Doing?

Document Title: **4ESS™ Switch Digital Interface Frame-Export 1 (DIF-E1) Description**

Document No.: 234-112-015

Issue 4

Date: June 1996

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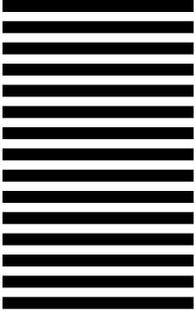
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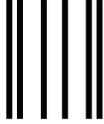
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