Task Oriented Practice
(TOP)

4ESS™ SWITCH

—— 1A PROCESSOR ——

OUTPUT MESSAGE ANALYSIS
(AUDITS, INTERJECTS, AND INTERRUPTS)
MAINTENANCE

Developed by
Customer Information Development and Business Translations Organization

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TITLE PAGE	000

FIND YOUR JOB IN THE LIST BELOW . . . . . THEN GO TO

FIND YOUR JOB IN THE LIST BELOW . . . . . THEN GO TO

No acceptance test procedures are required

MAINTENANCE PHILOSOPHY

General

The Maintenance Operation Center (MOC) Output Message Analysis volume has been developed to extend the trouble-clearing strategy in the MOC beyond the limits of the Diagnostic (DGN) programs. Output message analysis is performed in response to specific TTY printouts, AUDIT CALL AT, REPORT; INTERJECT, and REPORT: INTERRUPT usually when no DGN: or DGN: ATP printout has been generated. However, it is possible to perform output message analysis after fault isolation using DGN: has failed (Trouble Locating Programs (TLP), Raw Data Analysis, and, to some extent, interactive diagnostics using looping techniques) if the appropriate output messages are printed out. As a result of output message analysis, a suspect pack list is identified, but no directions to or how to replace the suspect packs are provided within this volume. Circuit pack replacement procedures can be accessed through the index of the individual frame volumes. Verification of success in clearing problems may require monitoring the system, subsystem, and frame operation over a lengthy period of time. This is especially true when the problem is sporadic or intermittent. It is assumed that all instructions and decisions are performed correctly.

Audits

Audits are performed to correct data errors. The occurrence of an audit is not cause for trouble clearing. The TAPs provided for analyzing audits should only be used when the audit is repetitive, indicating a probability of a hardware error or when the AUDIT CALL AT printout is accompanied by a REPT: SYSTEM TROUBLE: AUDIT UNABLE TO CORRECT TROUBLE printout. For this reason, the printout should be checked for all messages related to the audits performed, before determining which TAP to access.

Interjects and Interrupts

Interjects and interrupts are analyzed utilizing printouts generated by the malfunction. These printouts provide several segments of information that must be analyzed. These segments are Heading Information, Level Data providing the contents of CC Registers, Fault Recognition Results, Error Analysis Recent History Table and Internal Registers also known as Critical Registers (CREG). Analyzation of this information may follow different approaches. One, a step-by-step approach takes the user (craft) through a bit-by-bit examination of these registers, eliminating fault possibilities with each examination until a group of candidate (suspect) packs are identified. Examples of printouts are provided to aid in location and identification of words (registers) and bits; and tables are used to relate to suspect packs and suspect leads and to provide trouble-clearing tips. In other procedures, analyzation is conducted in a procedural approach which utilizes the Point of Maximum Definition (PMD) to implicate the suspect circuits, packs, and leads. The method used is based upon the sophistication of the PMD relationship to the fault recognition program-generated printout. The level of interject or interrupt is an indication of the equipment involvement. Levels A, B, and C indicate Central Control (CC) or configuration involvement. Level D reflects Call Store (CS) or auxiliary unit (FS, TU, DUS) involvement, and Level E implicates the Program Store (PS). An interject is a less critical indication of a problem. It should not be ignored because of the tendency toward escalation into a more serious problem.

SUMMARY	
Using AUDIT AT and AUX= addresses, determine PIDENT that called for message print and failure point calling for AUDIT. Using starting address of PIDENT, convert the addresses above to relative addresses. Using PIDENT,	locate relative addresses and scan program listing backward from address points for comments related to AUDIT CALL, data structures passed to AUDITS, and data in CC REGs at time of AUDIT CALL. Decode data structures and CC REGs to determine possible cause of AUDIT AT message

```
05  AUDIT CALL AT 16150430 AUX= 16150430 CLIENT= MTC
    MISCELLANEOUS DATA INVALID
    MAC SYSTEM TROUBLE DETECTED
    CC REGS
    L=00000077  F=77767777  G=00140000  J=16140734
    K=00012022  X=00031046  Y=00000002  Z=00000002
    SHADOW REGS
    L=00004172  F=77767777  G=00140000  J=16140734
    K=00012022  X=00000072  Y=00000001  Z=00000071
    DATA:
    16143006  16140736
    12/15/88   08:03:17
    #431
```

AUDIT AT AND AUX= ADDRESSES WHEN THEY ARE DIFFERENT: NOTE BOTH

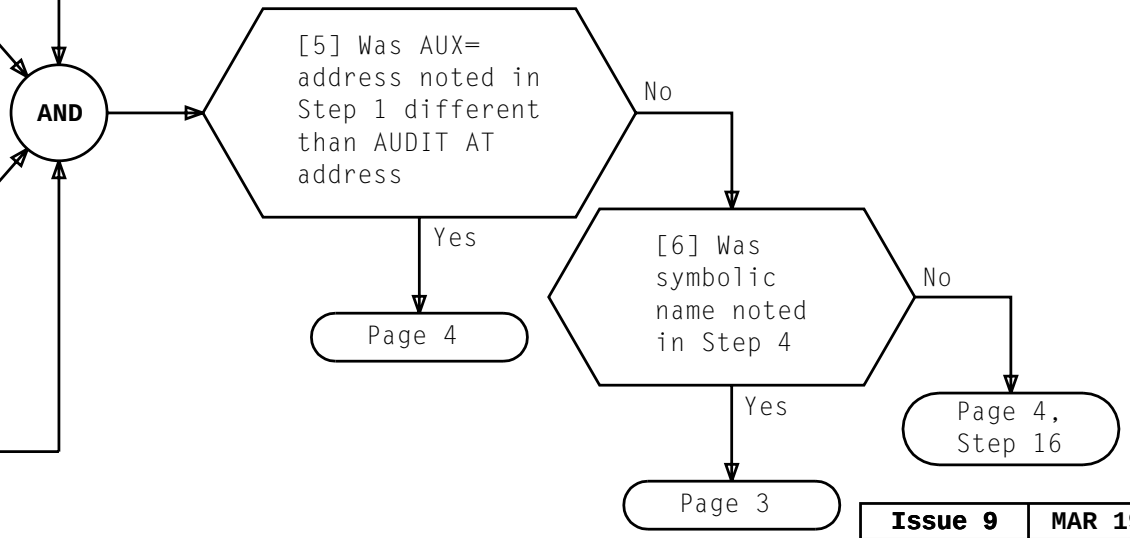
FIG. 1 - Sample of the Audit Call at Message

[1] Using loader map, identify, then obtain PIDENTs containing AUDIT AT and AUX= addresses from printout [FIG. 1]

[2] Convert AUDIT AT and AUX=addresses to relative addresses within PIDENTs [DLP-514]

[3] In PIDENT containing AUDIT AT address, scan backward from the relative address of AUDIT AT address to entry point of audit call [FIG. 2]

[4] Note comments indicating reason for AUDIT CALL, entry point symbolic name (if there is one), CC REGs listed and contents, and data structures passed to AUDITS [FIG. 2]



ANALYZE AUDIT AT MESSAGE

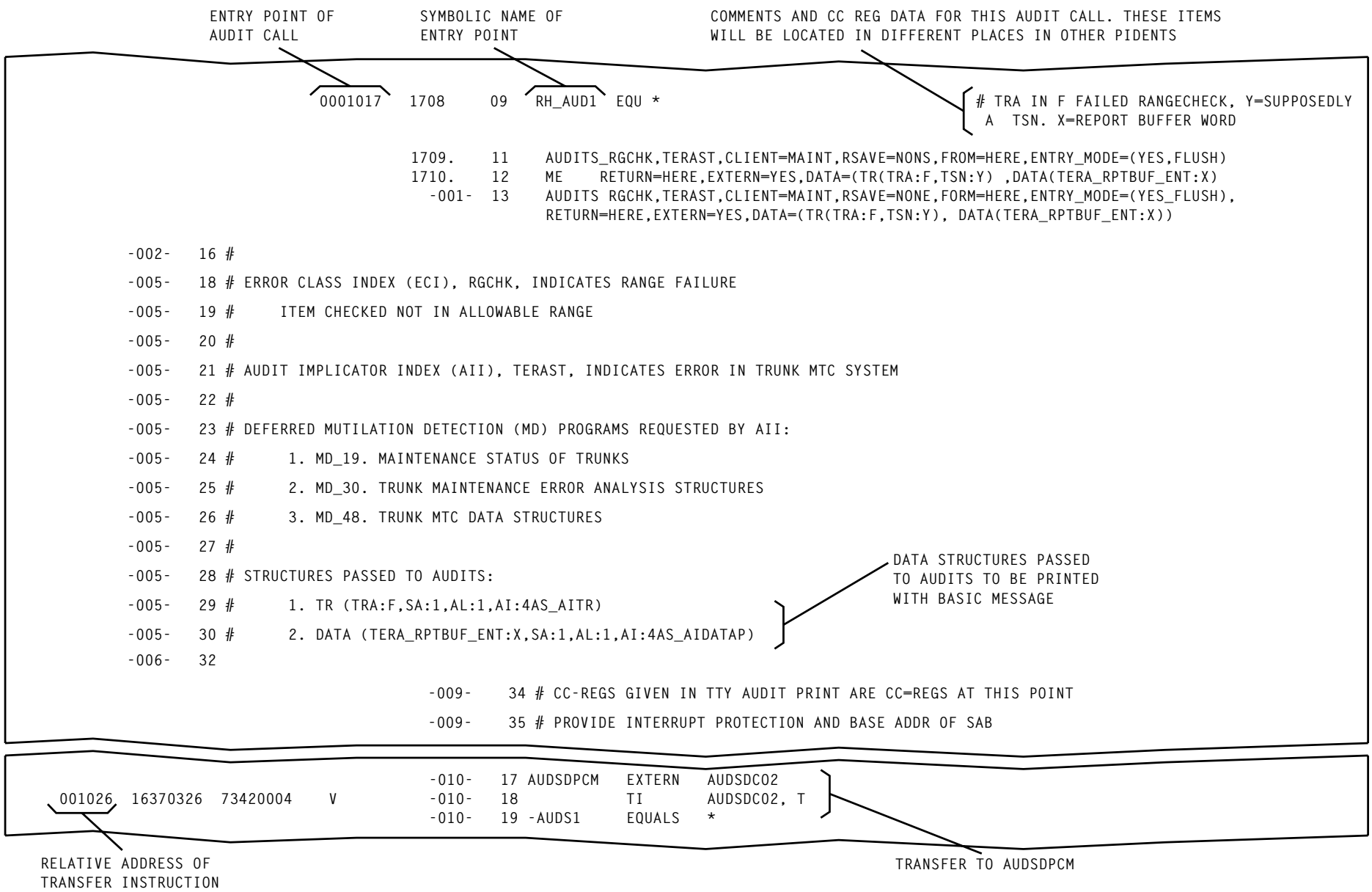
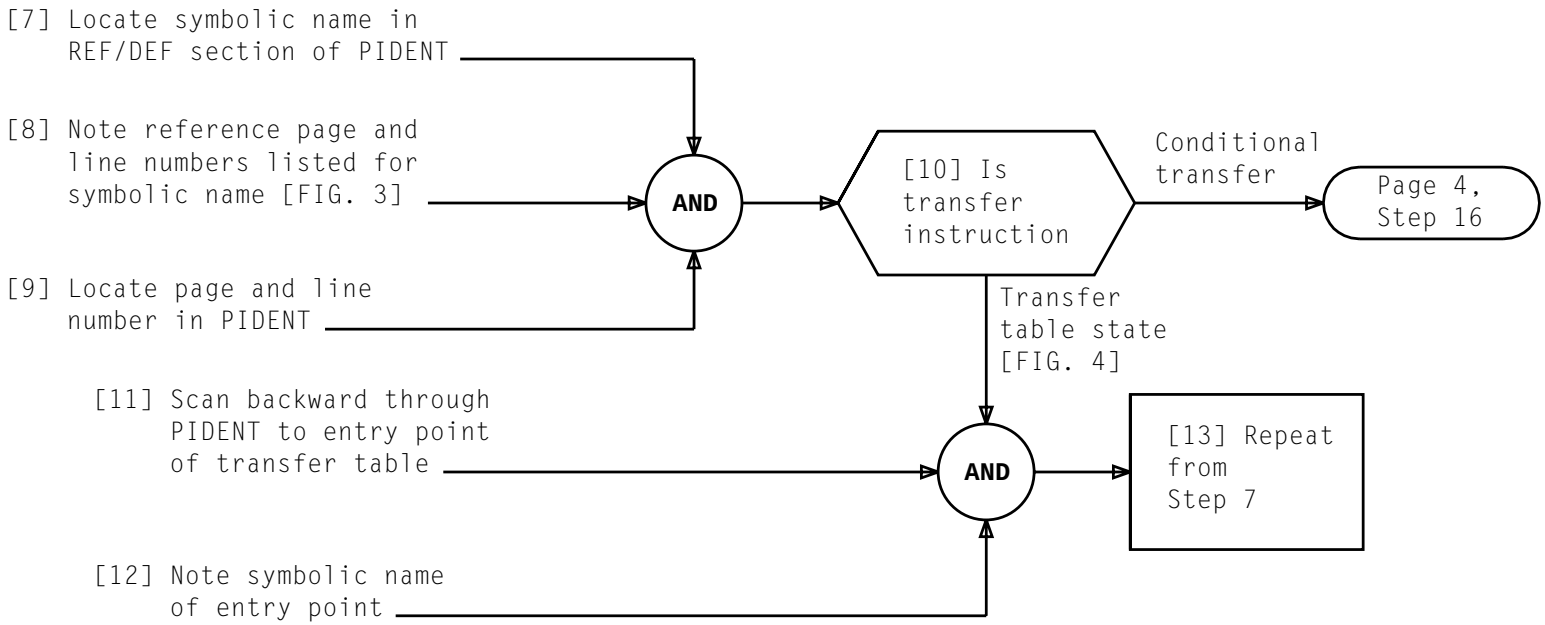


FIG. 2 — Sample of PIDENT Audit Call Expansion

ANALYZE AUDIT AT MESSAGE



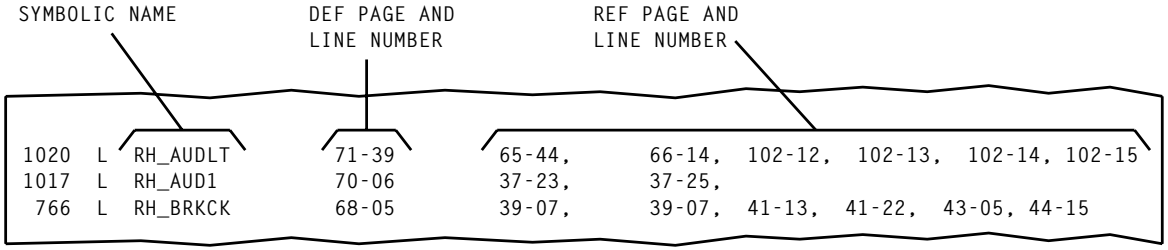


FIG. 3 — Example From PIDENT REF/DEF Section

```
007175    15605703   63400200   007375    -003-    22      T     AUDODOT    # STATE 0 IS UNASSIGNED ( )
007176    15605704   77400400              -003-    23      T     O(TI)      # STATE 1=4CROGT_AUD1 (AUDIT STATE_
                                                                              IGNORE REPORT
007177    15605705   63400176   007375    -003-    25      T     AUDODOT    # STATE 2 IS UNASSIGNED ( )
007200    15605706   63400175   007375    -003-    26      T     AUDODOT    # STATE 3 IS UNASSIGNED ( )
```

FIG. 4 — Sample From PIDENT Transfer Table

[14] In PIDENT containing AUX= address, locate line of relative address found in Step 2

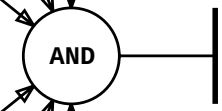
[15] Back up one instruction line and note transfer instruction to AUDIT CALL

[16] Scan backward through PIDENT noting what program was doing when audit was called [FIG. 5]

[17] Note data being checked or compared and location recorded

[18] Analyze CC REGs and/or data structures noted

[19] Determine source of data in error



ANALYZE AUDIT AT MESSAGE

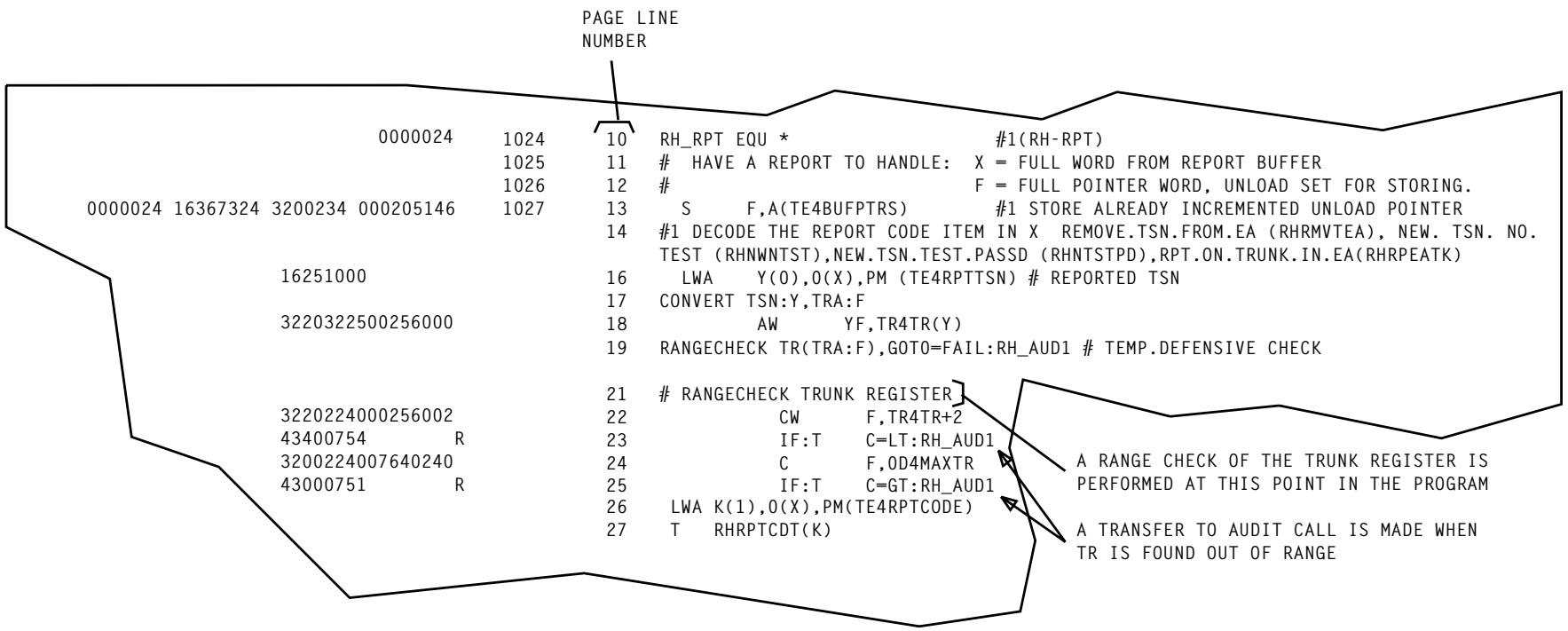


FIG. 5 — Sample of Error Condition Transfer to Audit Call

SUMMARY

Using **AUDIT AT** output message, determine FS IDTAG NUM. If message indicates **UNRESOLVED FAILURE** and FS IDTAG NUM is not 02 or 13, perform TAPE AUDIT (SAST) with appropriate system backup tape [TABLE A]. If FS IDTAG NUM is 13, copy office data onto tape (TWRP). If FS IDTAG NUM is 02, type **INIT:LIBSYS** message. If **UNRESOLVED FAILURE** is not indicated, analyze data and look for possible cause of errors

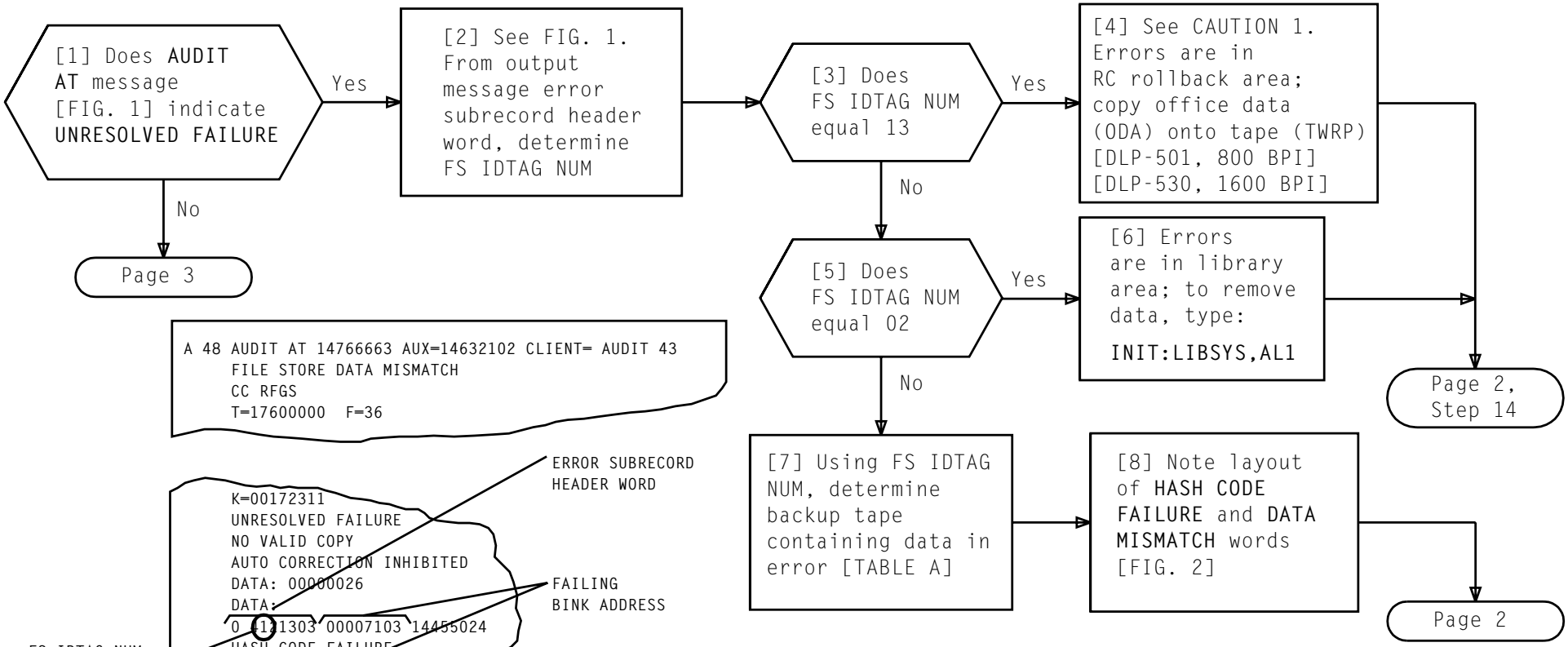
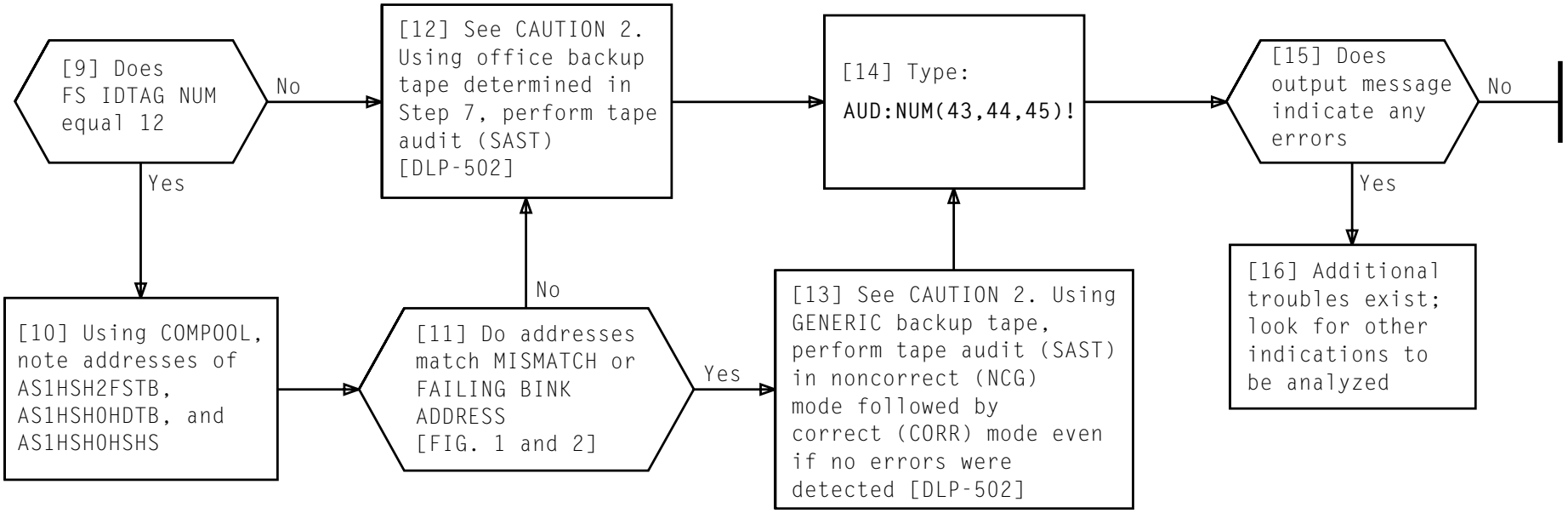


FIG. 1 - Sample of (Partial) Saws Audit Error Message

CAUTION 1
Writing new ODA tape affects rollback ability. Notify MAC before proceeding

ANALYZE AUDIT 43, 44, AND 45 ERRORS



HASH CODE FAILURE
DATA:
aaaaaaaa bbbbbbbb cccccccc dddddddd eeeeeeee ffffffff
DATA MISMATCH
DATA:
aaaaaaaa bbbbbbbb cccccccc dddddddd eeeeeeee ffffffff

WORD	FOR HASH CODE FAILURE	FOR DATA MISMATCH
a	ERROR SUBRECORD HEADER	ERROR SUBRECORD HEADER
b	FAILING BINK ADDRESS	MISMATCH ADDRESS
c	CORE-RESIDENT STORE HASH SUM	FILE STORE ADDRESS
d	COMPUTED FS 1 HASH SUM	FS 1 DATA
e	COMPUTED FS 0 HASH SUM	FS 0 DATA
f	COMPUTED CORE HASH SUM	CORE DATA

FIG. 2 — Layout of Hash Code Failure and Data Mismatch Words

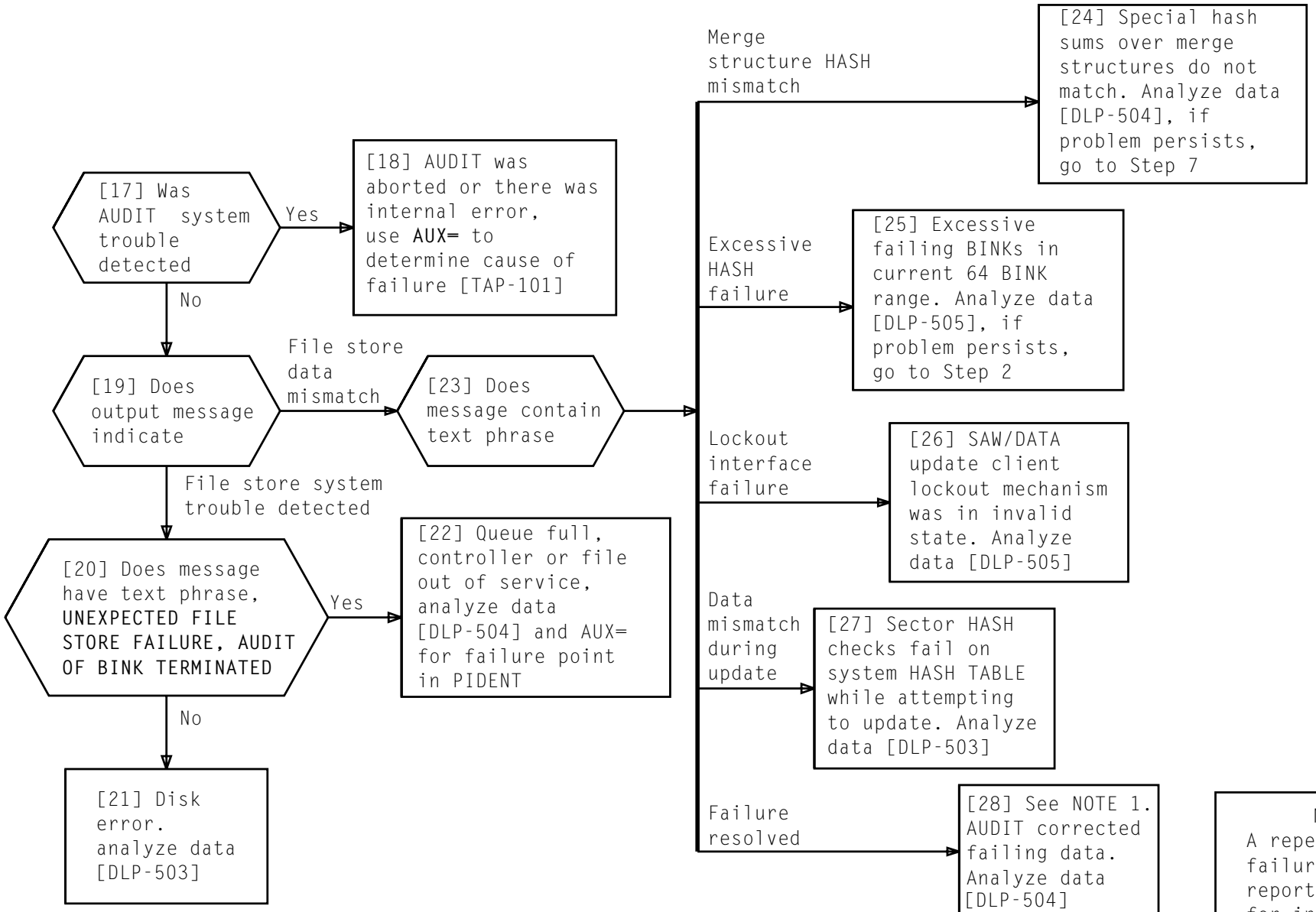
TABLE A

FS ID TAG NUM	FS AREA NAME	OFFICE BACKUP TAPE TO USE
01	GENERIC PROGRAM	GENERIC*
03	OFFICE DATA	ODA*
07	NETWORK MANAGEMENT	NTWK MGT
12	MERGE:FOR CORE—DISK AND HASH TBL	GENERIC*
14	TRAFFIC/PLANT MEASUREMENT	TR/PLT MEAS

*Use SR tape if generic and ODA are combined on one tape

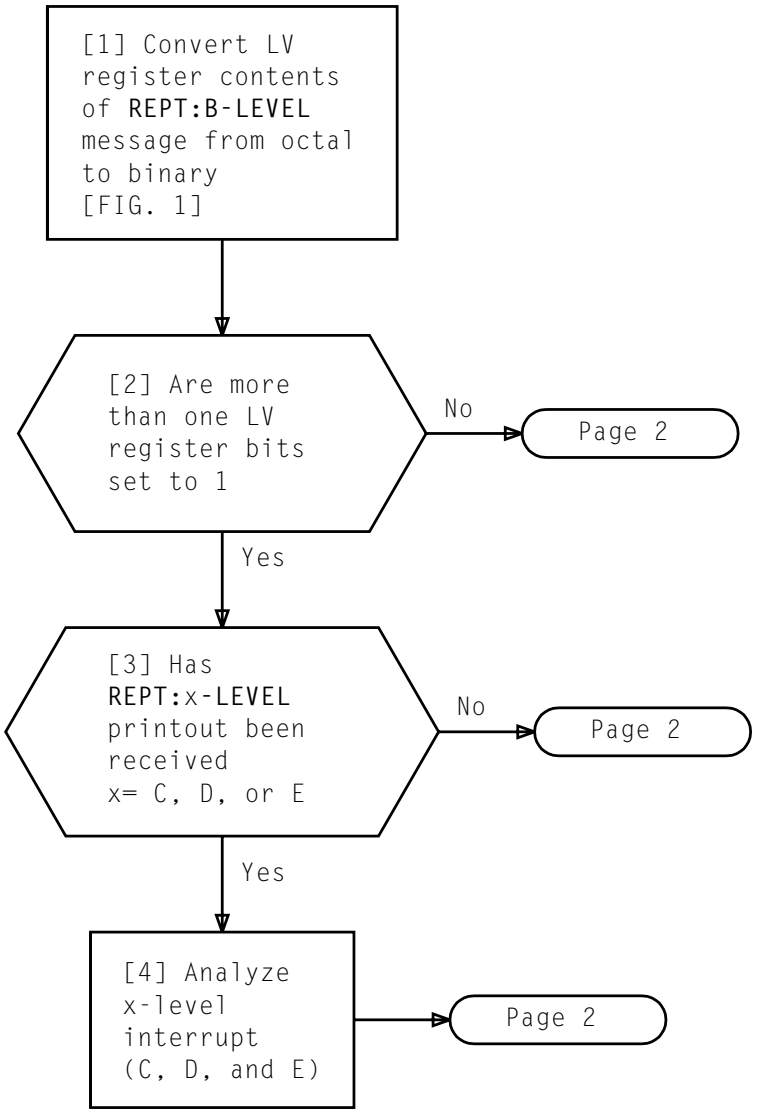
CAUTION 2
Software change packages (SCPs), entered since last backup tape was written, are lost at this point and must be reentered

ANALYZE AUDIT 43, 44, AND 45 ERRORS



NOTE 1
A repetitive data failure should be reported to NTAC for investigation

ANALYZE AUDIT 43, 44, AND 45 ERRORS




```
A 50 REPT: B-LEVEL  @04723444 MFNUM=00000040 MICON=00000021  COMPLETED
     LV=0002 D0=00001001 D1=00000000 D2=00000000 D3=00000000

     PCRV CONFIGURED

     DATA:  B-LEVEL
     00000015 00000000 04723445 01000000 01000000 00117275
     00020475 00014543 01200000 04723444 00000402 04723443
     00117275 00000001 17410020 62005757 00060302 00001400

     DATA:  PCRV TEST RUN AND HASH SUM RESULTS
     04151602 00000000 00400000

     DATA:  BLEV STANDBY CC REGISTERS
     00000000 00000000 00000000 00000000 00000000 00000000
     00000000 00000000 00000000 00000052 00000000 00000026
     00000000 02000000 77637777 00035746 00065701 00000000
     000000  00:50:32
     #162
```

B-LEVEL (BLEV)

IN1FR	IN1GR	IN1JR	IN1KR	IN1LR	IN1XR
IN1YR	IN1ZR	IN1BR	IN1CAR	AC1ILA	AC1SCA
AC1SDA	AC1INS	AC1INH	AC1CSC	AC1PCR	AC1SAT

PCRV TEST RUN AND HASH SUM RESULTS (PCRVHS)

			COUPLETS		
PCRVPADDR	PC1HISTORY	PC1OVERRIDE	M-ADDR	M-DATA	M-ADDR
M-DATA	M-ADDR	M-DATA	M-ADDR	M-DATA	M-ADDR

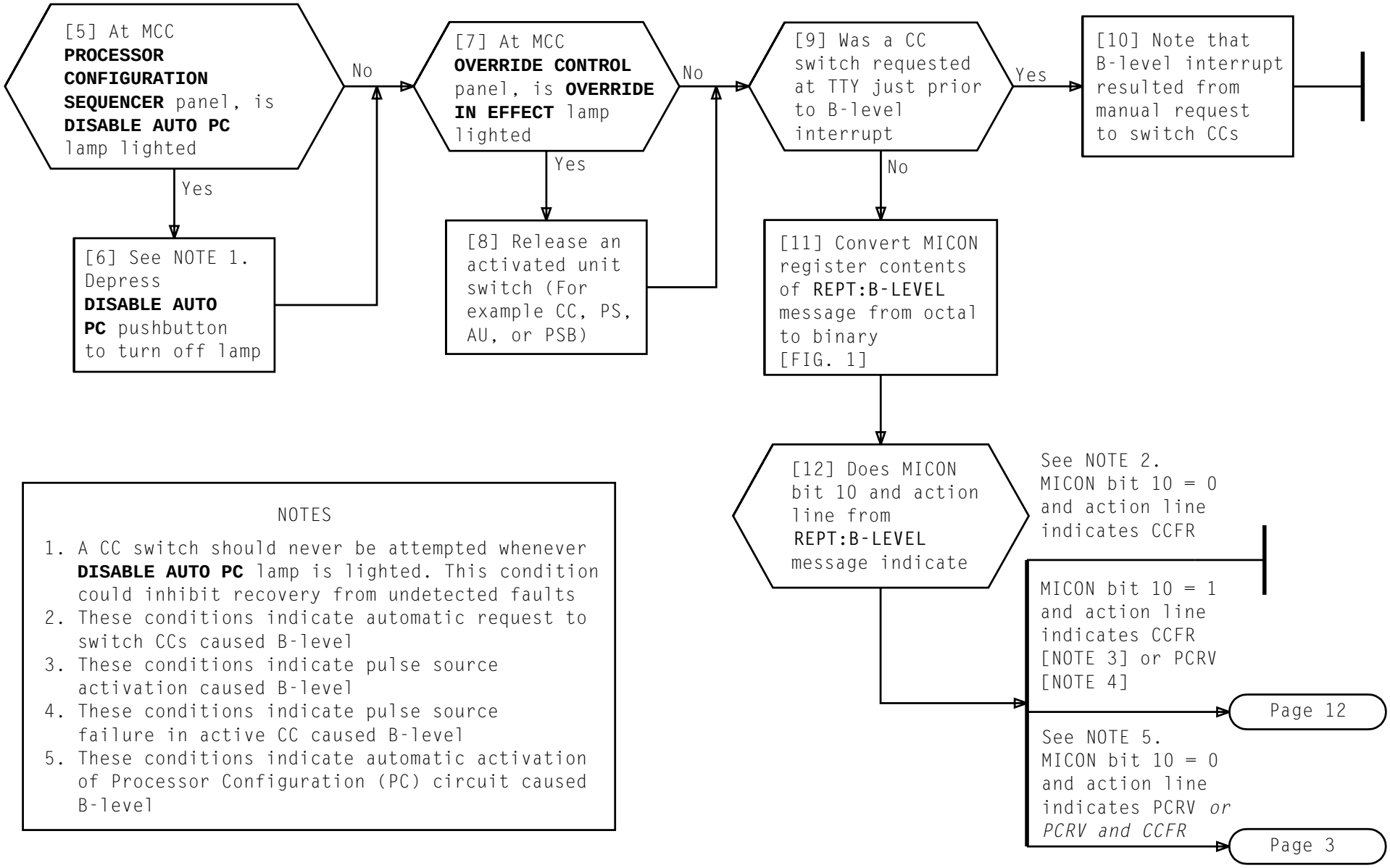
M-ADDR/DATA IS OPTIONAL

PCRV STANDBY CC REGISTERS (PCRVST)

ST1FR	ST1GR	ST1JR	ST1KR	ST1LR	ST1XR
ST1YR	ST1ZR	ST1BR	ST1CAR	ST1ILA	ST1SCA
ST1SDA	ST1INS	ST1INM	ST1CSC	ST1PCR	ST1SAT

FIG. 1 — Sample of B-Level Printout and Register Location

ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTES

1. A CC switch should never be attempted whenever **DISABLE AUTO PC** lamp is lighted. This condition could inhibit recovery from undetected faults
2. These conditions indicate automatic request to switch CCs caused B-level
3. These conditions indicate pulse source activation caused B-level
4. These conditions indicate pulse source failure in active CC caused B-level
5. These conditions indicate automatic activation of Processor Configuration (PC) circuit caused B-level

ANALYZE B-LEVEL INTERRUPT MESSAGE

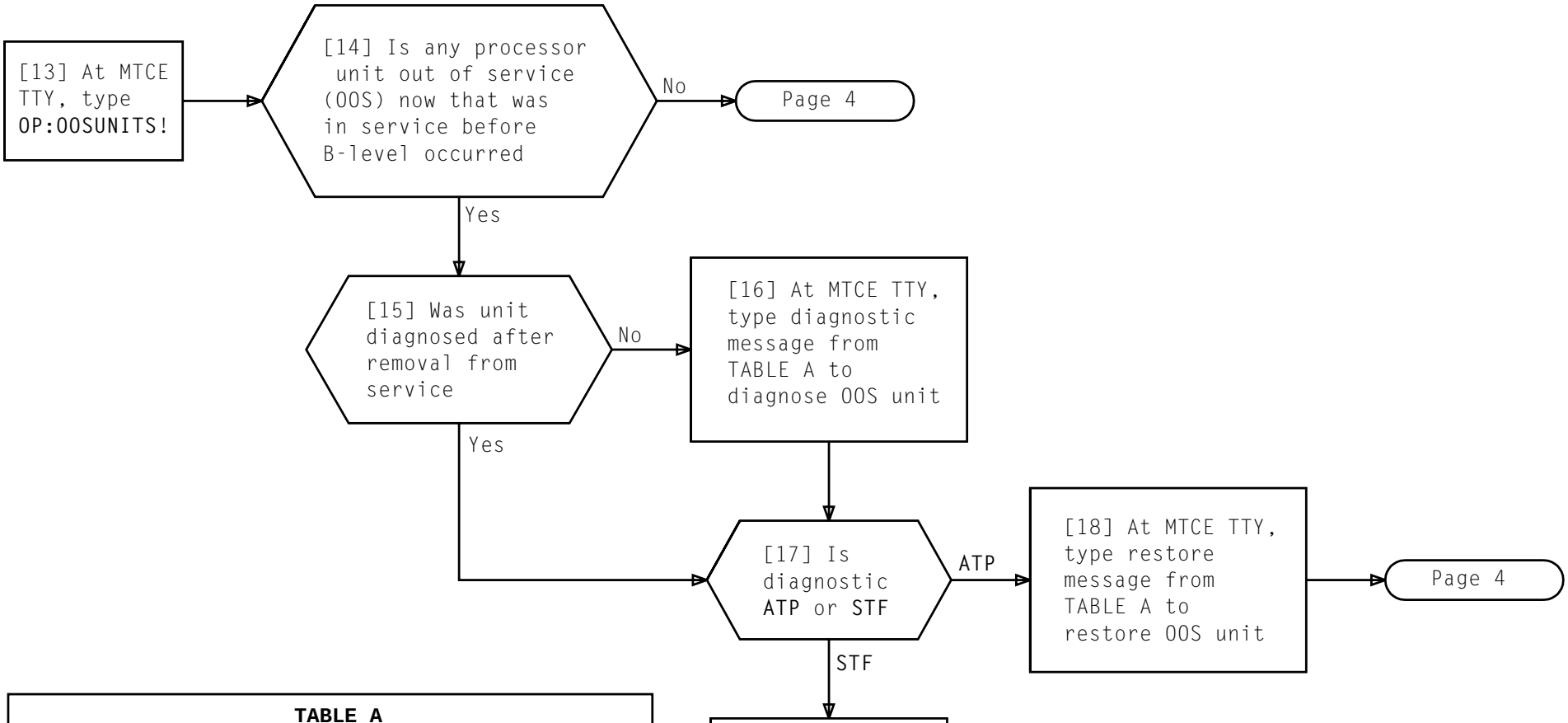
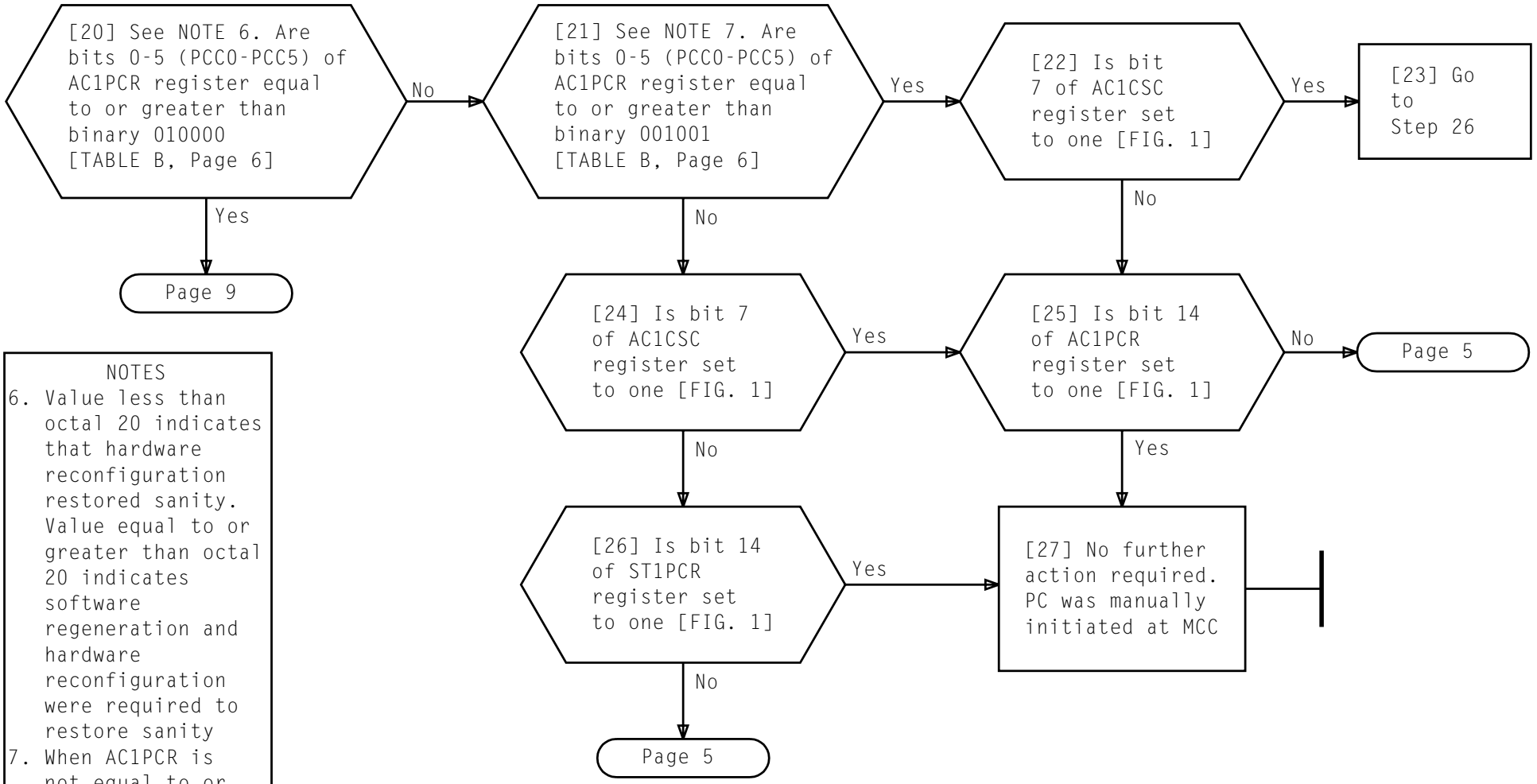


TABLE A

UNIT	DIAGNOSTIC MESSAGE	RESTORE MESSAGE	TOP VOLUME
CC	DGN:CC a:TLP!	RST:CC a!	254-251-001
PS	DGN:PS a:TLP!	RST:PS a!	254-251-005
PSB	DGN:PSB a!	RST:PSB a!	254-251-005
CS	DGN:CS a:TLP!	RST:CS a!	254-251-005
CSB	DGN:CSB a!	RST:CSB a!	254-251-005
AUB	DGN:AUB a!	RST:AUB a!	254-251-010
FS	DGN:FS a:TLP!	RST:FS a!	254-251-015

a = member number

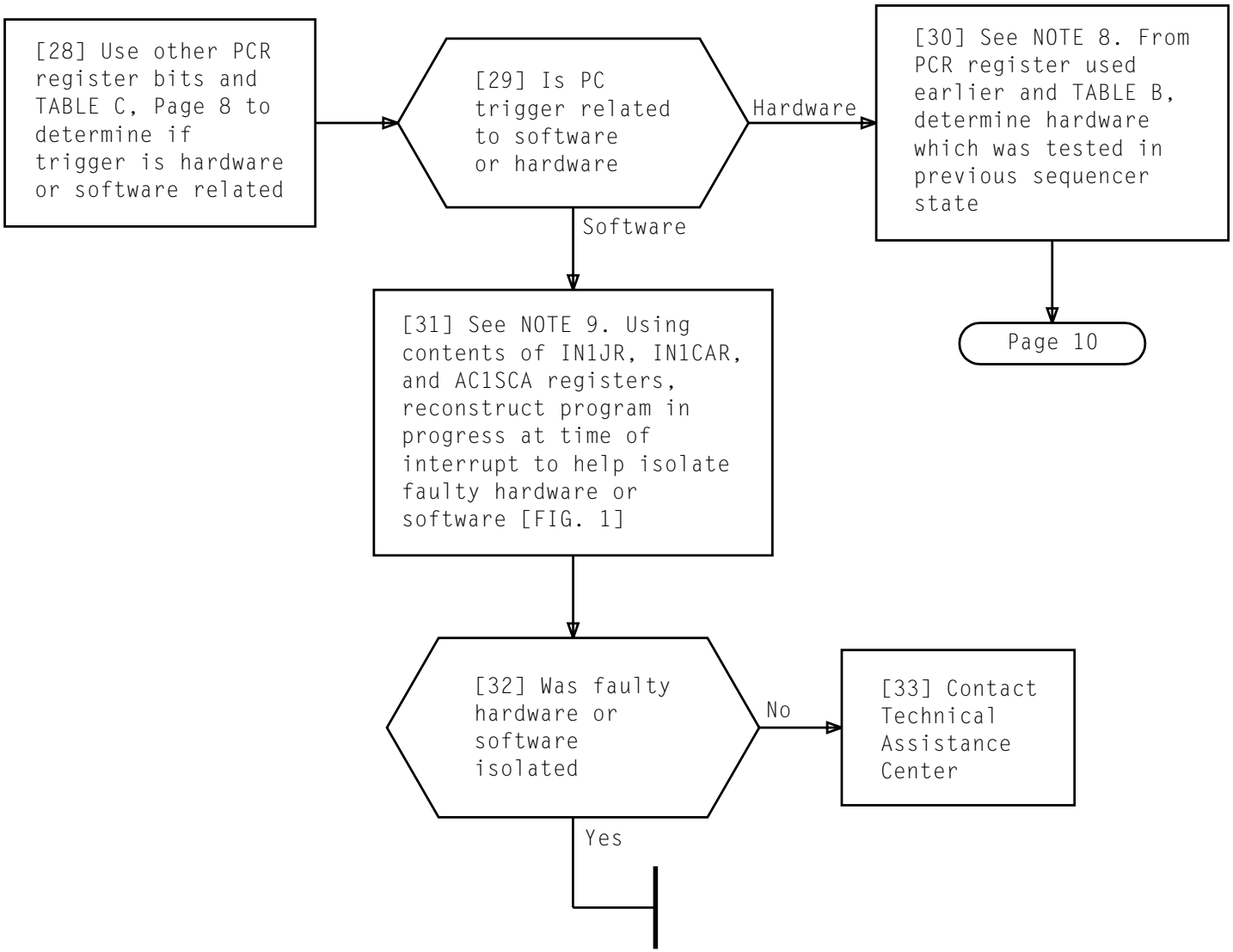
ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTES

6. Value less than octal 20 indicates that hardware reconfiguration restored sanity. Value equal to or greater than octal 20 indicates software regeneration and hardware reconfiguration were required to restore sanity
7. When AC1PCR is not equal to or greater than octal 11, CC was not switched a second time. Standby CC registers are frozen on interrupt

ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTES

8. If this is level 1 PC (PC states 0-15) and rover store is not assigned K-code 20, it will advance to next higher state. This is normal since level 1 use of rovers is limited to only backup K-code 20 (block 0)
9. Programmer notes in PR may be helpful. It may be necessary to request assistance from SMCC, TAC, or PECC per local practice. J register is used to store address (J) returns. SCA register is used to store address where program is coming from (where program was interrupted in standby CC). CAR register contains address where program is/was going

ANALYZE B-LEVEL INTERRUPT MESSAGE

TABLE B
HARDWARE CONFIGURATIONS DURING PROCESSOR CONFIGURATION (PC) STATES

PC STATE	PC STATE COUNTER						STATES OF PC STATE COUNTER IN LEVEL 1 PC									PC STATE	PC STATE COUNTER						STATES OF PC STATE COUNTER IN LEVEL 2 PC (PUMP)								
	PCC5	PCC4	PCC3	PCC2	PCC1	PCC0	CC SWITCH	RECONFIGURE	PUMP	PROGRAM STORE SELECTED	PS BUS SELECTED	FSC SELECTED	NO CHANGE	BYPASS CC SANITY CHECK	BYPASS HASH CHECK OF DATA	BYPASS STORE MAINTENANCE CHECK		PCC5	PCC4	PCC3	PCC2	PCC1	PCC0	CC SWITCH	RECONFIGURE	PUMP	PROGRAM STORE SELECTED	PS BUS SELECTED	FSC SELECTED	NO CHANGE	BYPASS CC SANITY CHECK	BYPASS HASH CHECK OF DATA	BYPASS STORE MAINTENANCE CHECK
0	0	0	0	0	0	0							X				16	0	1	0	0	0	0								X				
*1	0	0	0	0	0	1	X										17	0	1	0	0	0	1	X										
2	0	0	0	0	1	0		X		PS 0	BUS 0						18	0	1	0	0	1	0		X	X	PS 0	BUS 0	0				
3	0	0	0	0	1	1		X		PS 0	BUS 1						19	0	1	0	0	1	1		X	X	PS 0	BUS 1	0				
4	0	0	0	1	0	0		X		ROV 0	BUS 0						20	0	1	0	1	0	0		X	X	ROV 0	BUS 0	0				
5	0	0	0	1	0	1		X		ROV 0	BUS 1						21	0	1	0	1	0	1		X	X	ROV 0	BUS 1	0				
6	0	0	0	1	1	0		X		ROV 1	BUS 0						22	0	1	0	1	1	0		X	X	ROV 1	BUS 0	0				
7	0	0	0	1	1	1		X		ROV 1	BUS 1						23	0	1	0	1	1	1		X	X	ROV 1	BUS 1	0				
8	0	0	1	0	0	0							X				24	0	1	1	0	0	0								X				
9	0	0	1	0	0	1	X										25	0	1	1	0	0	1								X			
10	0	0	1	0	1	0		X		PS 0	BUS 0						26	0	1	1	0	1	0		X	X	PS 0	BUS 0	1				
11	0	0	1	0	1	1		X		PS 0	BUS 1						27	0	1	1	0	1	1		X	X	PS 0	BUS 1	1				
12	0	0	1	1	0	0		X		ROV 0	BUS 0						28	0	1	1	1	0	0		X	X	ROV 0	BUS 0	1				
13	0	0	1	1	0	1		X		ROV 0	BUS 1						29	0	1	1	1	0	1		X	X	ROV 0	BUS 1	1				
14	0	0	1	1	1	0		X		ROV 1	BUS 0						30	0	1	1	1	1	0		X	X	ROV 1	BUS 0	1				
15	0	0	1	1	1	1		X		ROV 1	BUS 1						31	0	1	1	1	1	1		X	X	ROV 1	BUS 1	1				

* State 1 switch is dependent on CC trouble F/F TCC reset

TABLE B (Contd)

HARDWARE CONFIGURATIONS DURING PROCESSOR CONFIGURATION (PC) STATES

PC STATE	PC STATE COUNTER PCC5	PCC4	PCC3	PCC2	PCC1	PCC0	STATES OF PC STATE COUNTER IN LEVEL 2 (PUMP) INCLUDING REPEATED PC (32-63 REPEAT AFTER 63) CC SWITCH	RECONFIGURE	PUMP	PROGRAM STORE SELECTED	PS BUS SELECTED	FSC SELECTED	NO CHANGE	BYPASS CC SANITY CHECK	BYPASS HASH CHECK OF DATA	BYPASS STORE MAINTENANCE CHECK
†32	1	0	0	0	0	0							X			
33	1	0	0	0	0	1	X									
34	1	0	0	0	1	0		X	X	PS 0	BUS 0	0				
35	1	0	0	0	1	1		X	X	PS 0	BUS 1	0				
36	1	0	0	1	0	0		X	X	ROV 0	BUS 0	0				
37	1	0	0	1	0	1		X	X	ROV 0	BUS 1	0				
38	1	0	0	1	1	0		X	X	ROV 1	BUS 0	0				
39	1	0	0	1	1	1		X	X	ROV 1	BUS 1	0				
40	1	0	1	0	0	0							X			
41	1	0	1	0	0	1							X			
42	1	0	1	0	1	0		X	X	PS 0	BUS 0	1				
43	1	0	1	0	1	1		X	X	PS 0	BUS 1	1				
44	1	0	1	1	0	0		X	X	ROV 0	BUS 0	1				
45	1	0	1	1	0	1		X	X	ROV 0	BUS 1	1				
46	1	0	1	1	1	0		X	X	ROV 1	BUS 0	1				
47	1	0	1	1	1	1		X	X	ROV 1	BUS 1	1				
48	1	1	0	0	0	0							X	X	X	X
49	1	1	0	0	0	1	X							X	X	X
50	1	1	0	0	1	0		X	X	PS 0	BUS 0	0		X	X	X
51	1	1	0	0	1	1		X	X	PS 0	BUS 1	0		X	X	X
52	1	1	0	1	0	0		X	X	ROV 0	BUS 0	0		X	X	X
53	1	1	0	1	0	1		X	X	ROV 0	BUS 1	0		X	X	X
54	1	1	0	1	1	0		X	X	ROV 1	BUS 0	0		X	X	X
55	1	1	0	1	1	1		X	X	ROV 1	BUS 1	0		X	X	X
56	1	1	1	0	0	0							X	X	X	X
57	1	1	1	0	0	1							X	X	X	X
58	1	1	1	0	1	0		X	X	PS 0	BUS 0	1		X	X	X
59	1	1	1	0	1	1		X	X	PS 0	BUS 1	1		X	X	X
60	1	1	1	1	0	0		X	X	ROV 0	BUS 0	1		X	X	X
61	1	1	1	1	0	1		X	X	ROV 0	BUS 1	1		X	X	X
62	1	1	1	1	1	0		X	X	ROV 1	BUS 0	1		X	X	X
63	1	1	1	1	1	1		X	X	ROV 1	BUS 1	1		X	X	X

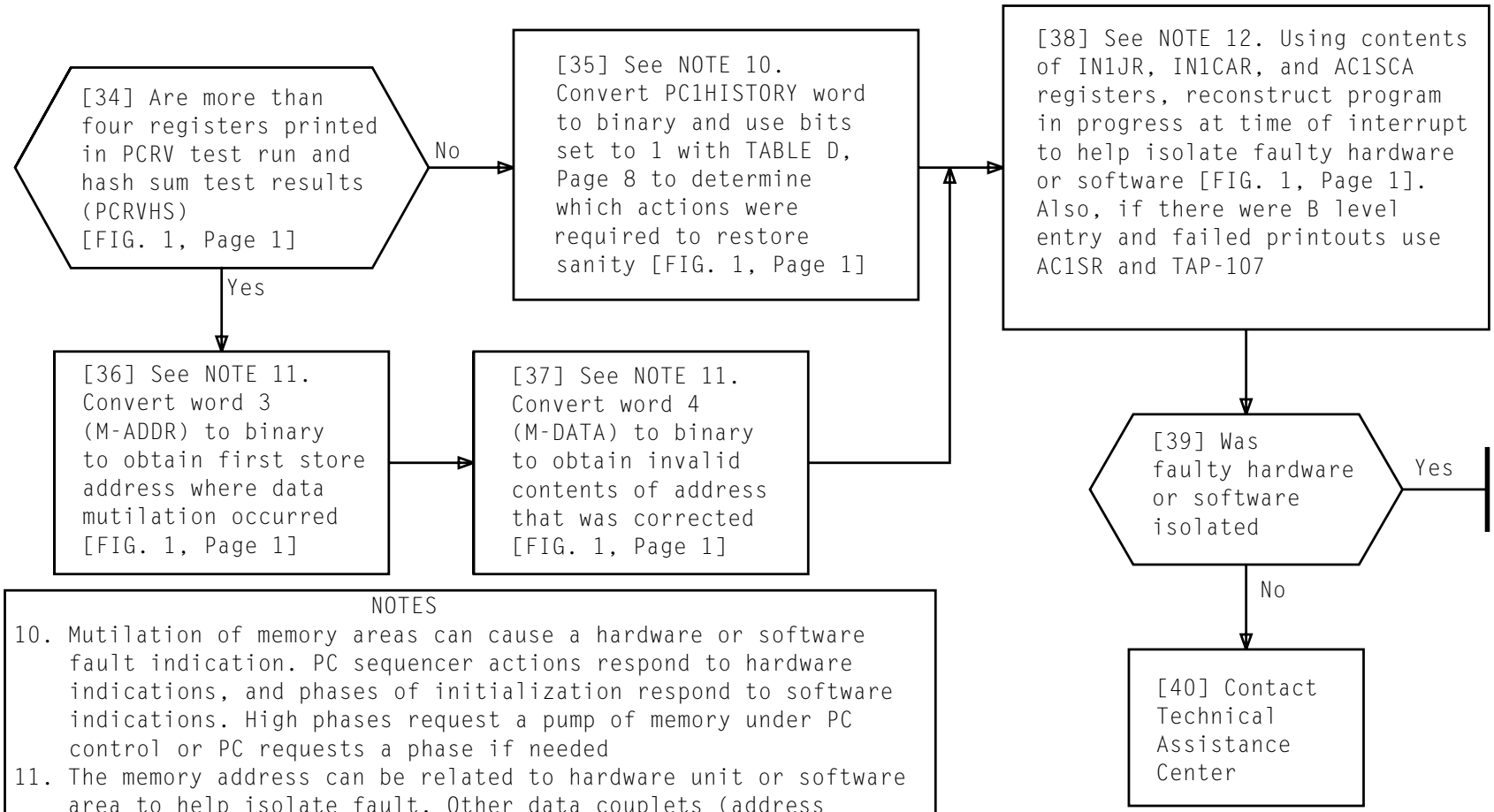
† When PCC5 becomes set, it remains set. Repeat PC cycles through states 48 through 63; then 32 through 47; then 48 through 63, etc

‡ Modified recovery actions remain in effect during repeat PC

TABLE C		
AC1PCR OR ST1PCR BIT	TRIGGER EXPLANATION	TRIGGER IS RELATED TO
8 = 1	PROGRAM SANITY TIMER: program sanity timer time-out, program insanity (execution took too long, loop, PST fault)	Software
9 = 1	PC SANITY TIMER: PC sanity timer time-out, configuration assembled in last state failed sanity or access tests	Hardware
10 = 1	Program request activated PC sequencer	Software
11 = 0		Hardware
12, 11 = 01	ANALOG TIMER TIME-OUT: fault recognition, recovery check failure, loss of CC clock, clock errors	Software or Hardware
12, 11 = 11	Act-Act, Sby-Sby check failure. Both CCs marked Act or Sby clock fault, CC hardware	Hardware
13 = 1	CCs were switched. When bit 13 equals 1 and no other trigger bits are set, marginal CC fault may exist	Hardware

TABLE D	
PC1HISTORY WORD BIT NUMBER	ACTION REQUIRED TO RESTORE SANITY
2, 12, or 13 = 1	Transient data was zeroed. Expect phase printouts before or after this interrupt
7 = 1	Hash totals were mutilated. Expect phase printouts before or after this interrupt
3 = 1	Interrupt is part of System Reinitialization (SR). SR data should have printed prior to this interrupt. Following an SR, B-level interrupt, printout can be expected
14 = 1	Pump actions have been expected due to: • Manual request (activate override) • Phase • Fault recovery required PC
15 = 1	PHASE ENTRY: phase printout should precede or follow interrupt
17 = 1	Phase entry to hash or pump all backed up memory and return to calling program
16 = 1	Phase entry, PC inhibited
18 = 1	PU Loop-around test failed
20 = 1	Active API switched
4 = 1	CS booted
5 = 1	PS booted
6 = 1	AU Bus system boot strapped
8 = 1	AU Bus was forced
9 = 1	Bad CS found during AU test
10 = 1	Bad PS found during AU test

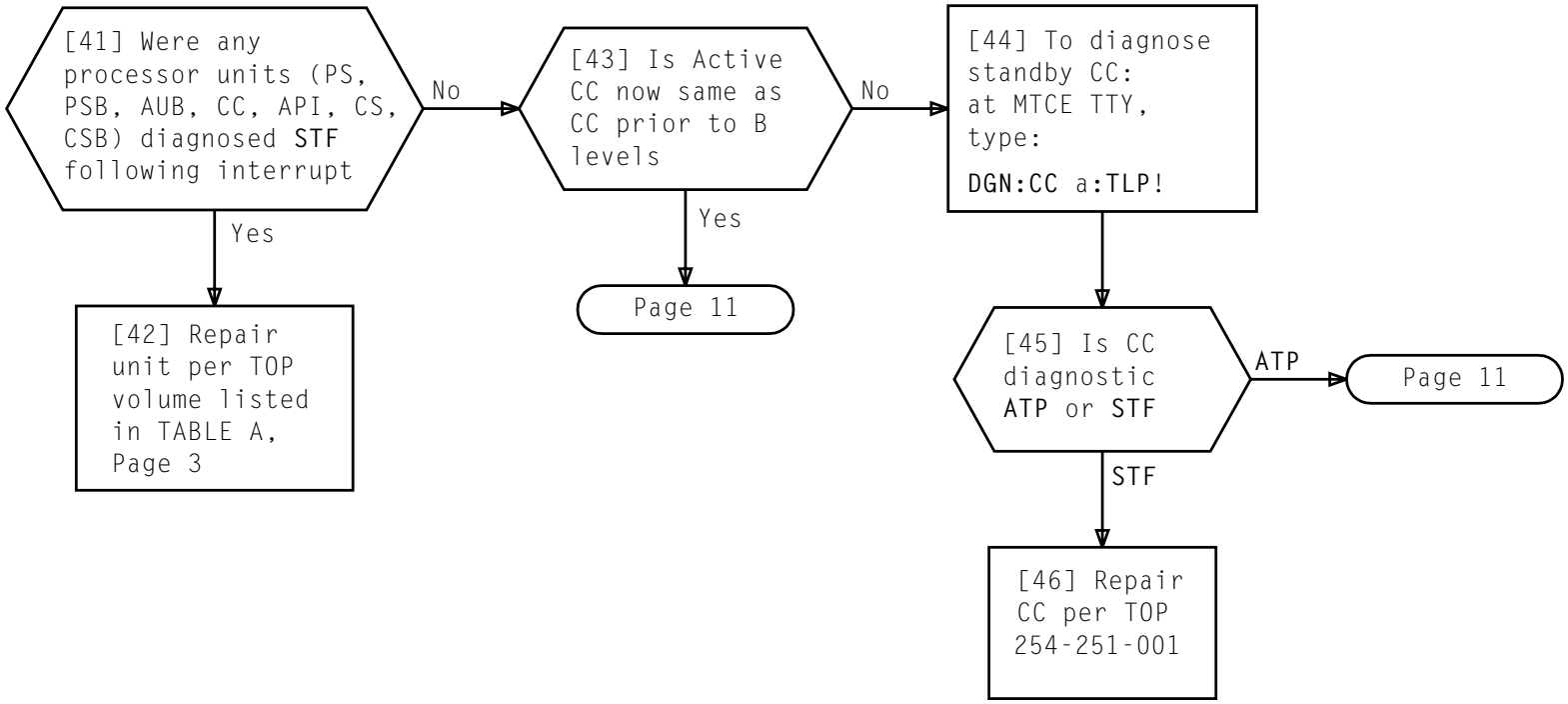
ANALYZE B-LEVEL INTERRUPT MESSAGE



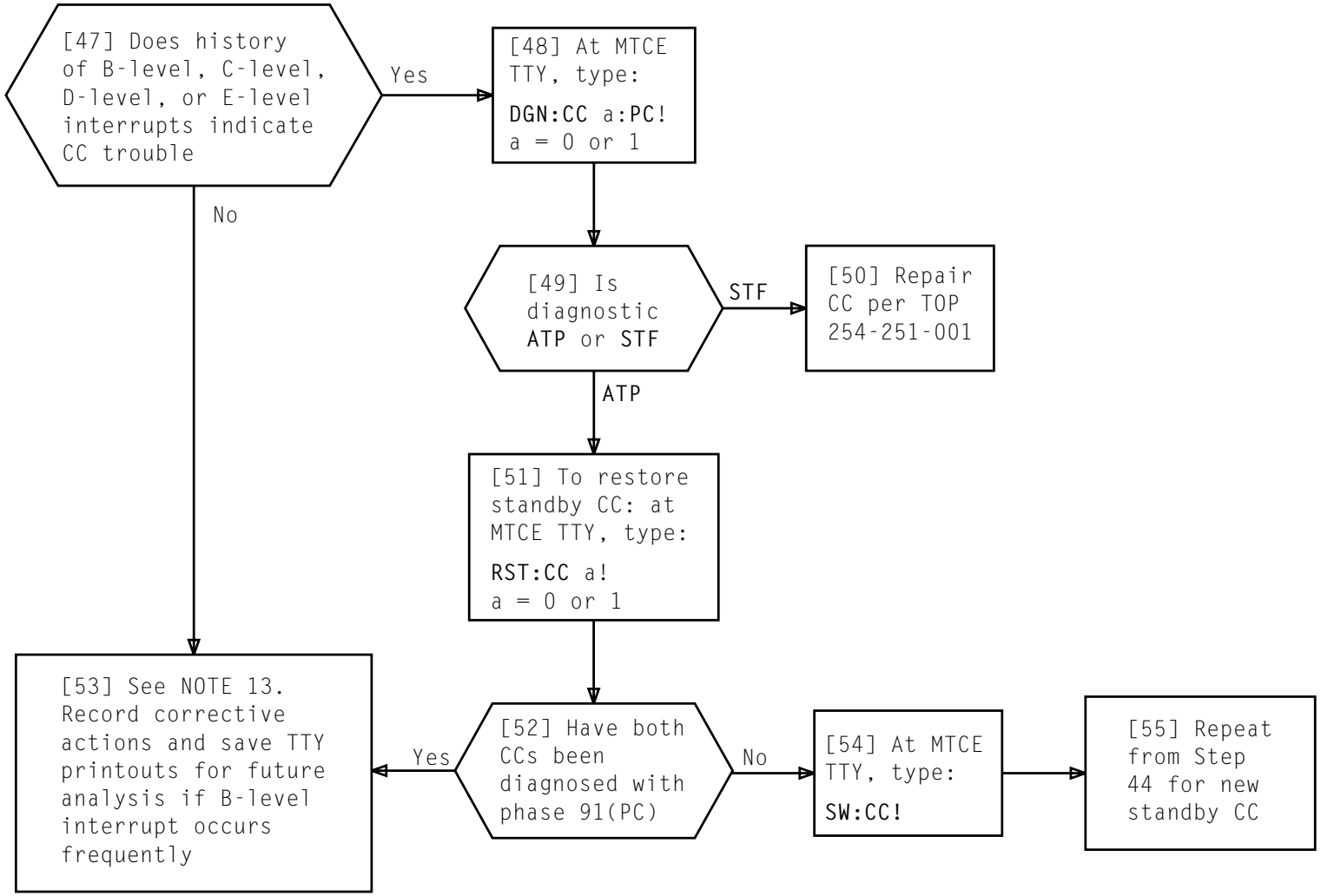
NOTES

10. Mutilation of memory areas can cause a hardware or software fault indication. PC sequencer actions respond to hardware indications, and phases of initialization respond to software indications. High phases request a pump of memory under PC control or PC requests a phase if needed
11. The memory address can be related to hardware unit or software area to help isolate fault. Other data couplets (address word - data word), if any, can be analyzed like words 3 and 4 to help isolate fault
12. Programmer notes in PR may be helpful. It may be necessary to request assistance per local practice. J register is used to store address (J) returns. SCA register is used to store address where program is coming from (where program was interrupted in standby CC). CAR register contains address where program is/was going

ANALYZE B-LEVEL INTERRUPT MESSAGE

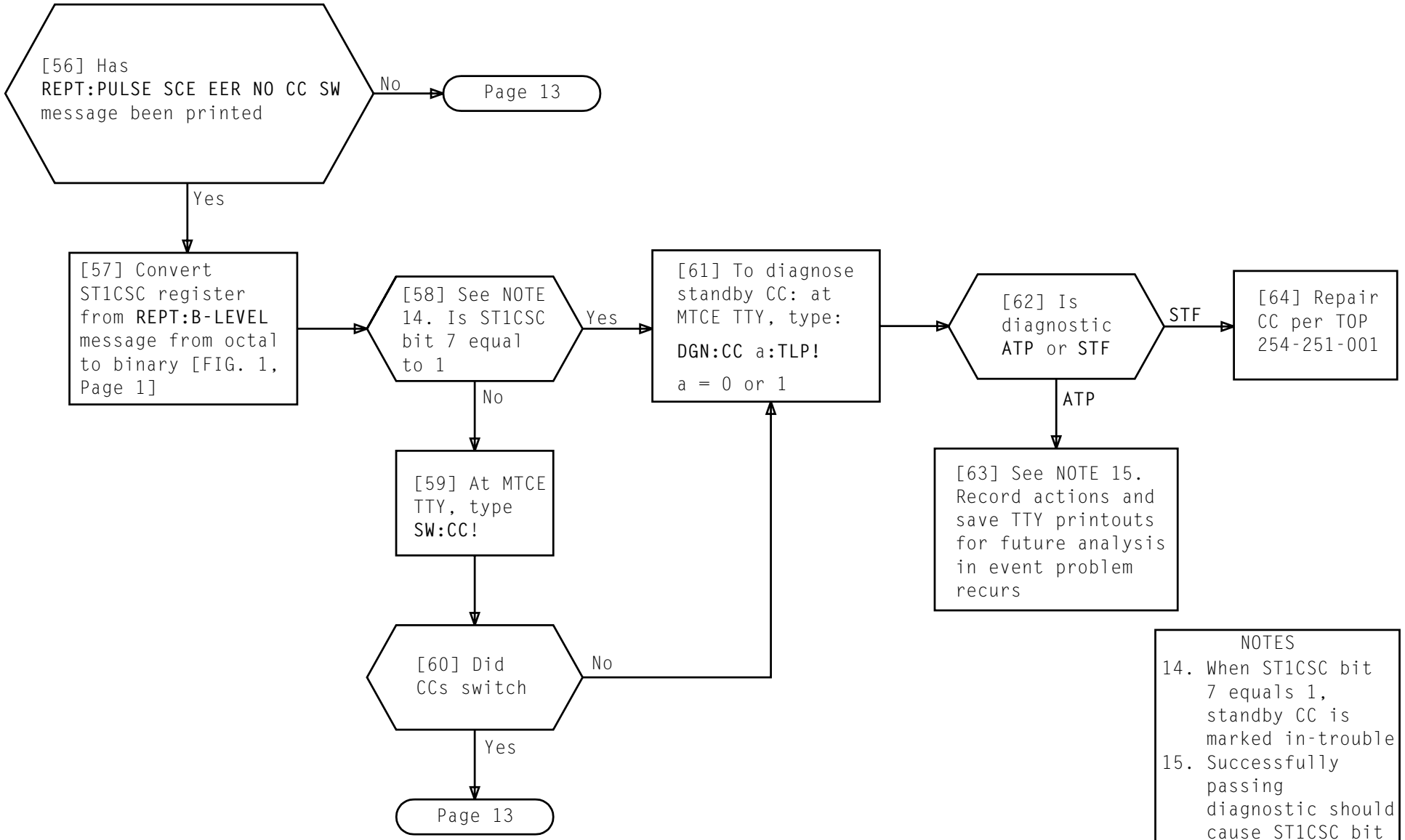


ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTE 13
It may be necessary to request technical assistance per local practice

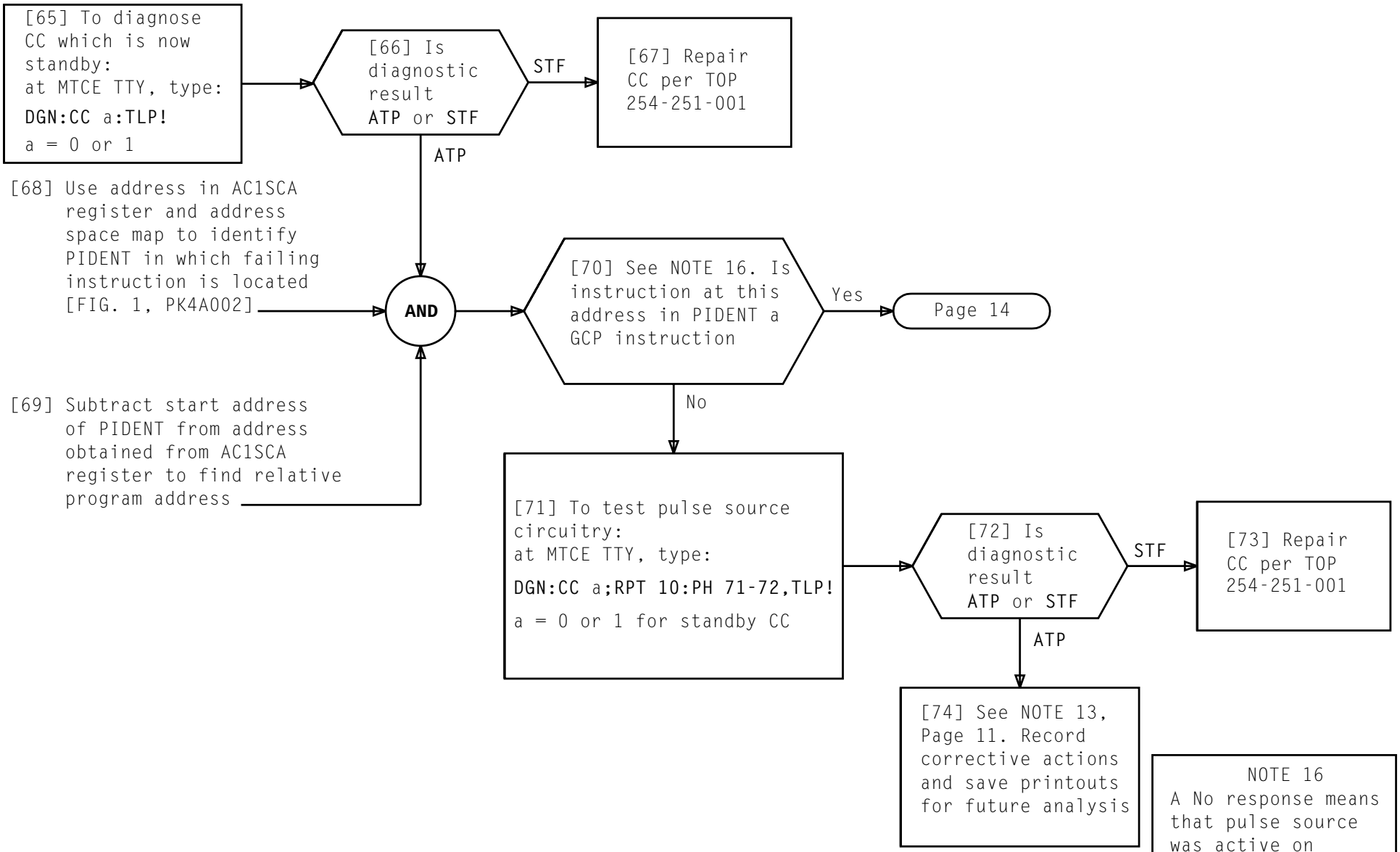
ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTES

14. When ST1CSC bit 7 equals 1, standby CC is marked in-trouble
15. Successfully passing diagnostic should cause ST1CSC bit 7 to be reset to 0

ANALYZE B-LEVEL INTERRUPT MESSAGE



NOTE 16
A No response means that pulse source was active on non-GCP instruction

ANALYZE B-LEVEL INTERRUPT MESSAGE

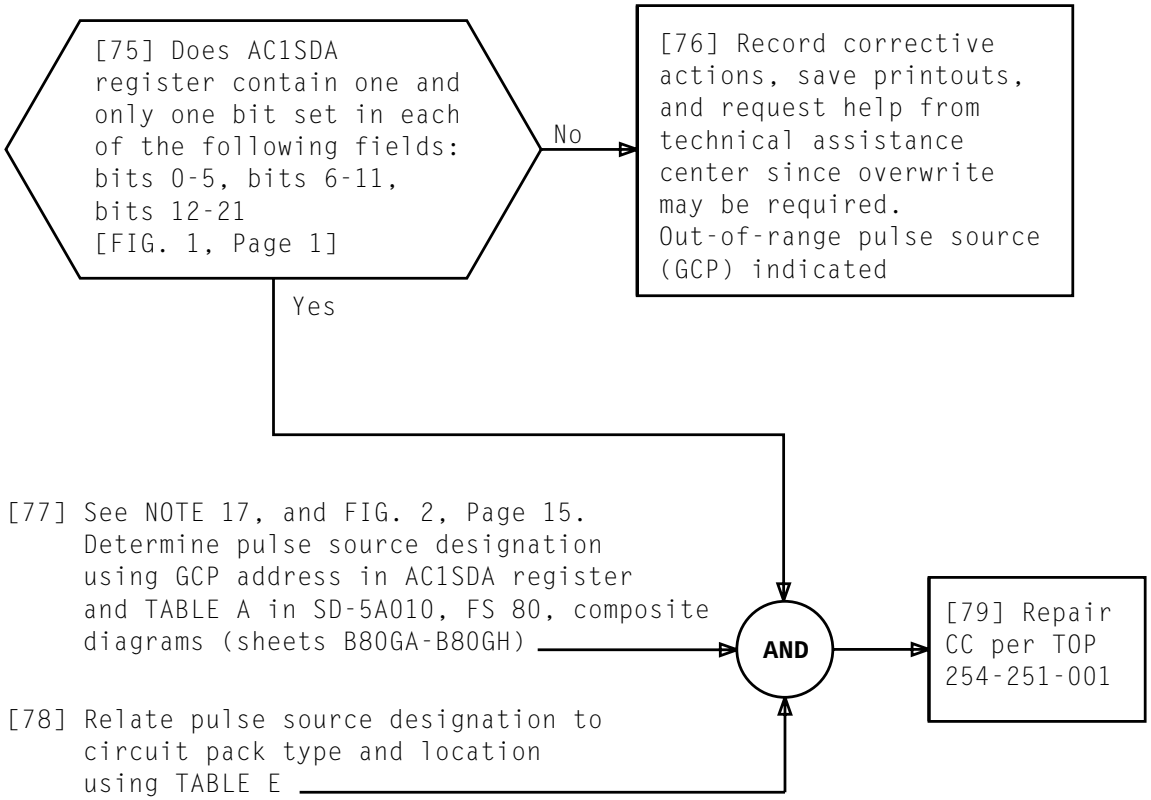


TABLE E
PULSE SOURCE DESIGNATION TO CP LOCATION CROSS REFERENCE

PULSE SOURCE DESIGNATION	CIRCUIT PACK TYPE	CIRCUIT PACK LOCATION
PSCS1	**FA183**	72-46
PSCS2	**FA183**	72-47
PSCS3	**FA183**	72-48
PSPS1	**FA183**	72-49
PSCU1	**FA183**	72-50
PSPU1	**FA183**	72-43
PSPU2	**FA183**	72-44
PSPU3	**FA183**	72-45
PSCC1	**FA183**	62-44
PSCC2	**FA183**	62-45

NOTE 17

Failure is likely due to multiple or no pulses being generated on a GCP instruction

ANALYZE B-LEVEL INTERRUPT MESSAGE

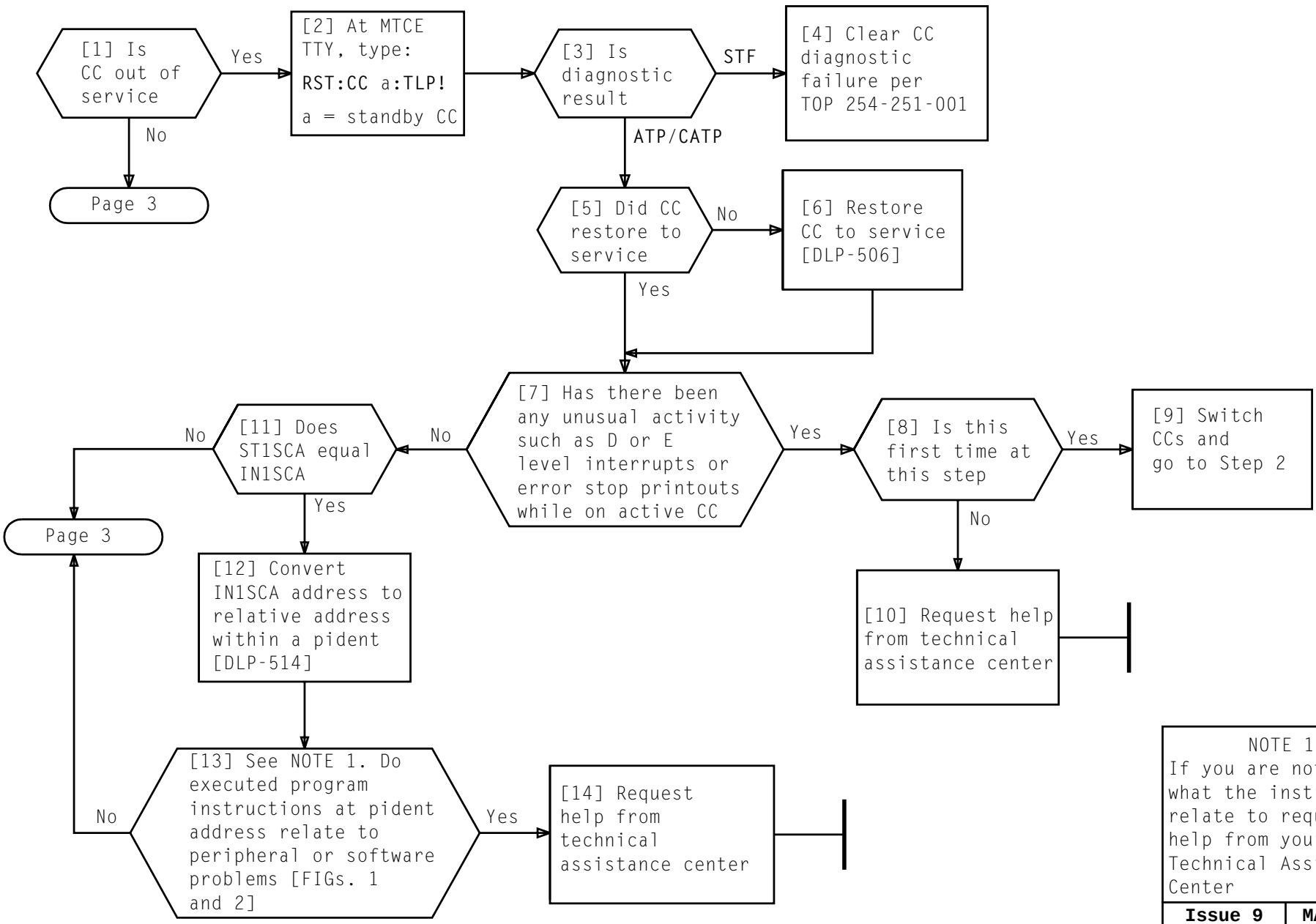
GCP ADDRESS FROM AC1SDA REGISTER

PULSE SOURCE DESIGNATION

TABLE A
PULSE SOURCES (CC GROUP 1 = PSCC1)

PULSE SOURCE	OCTAL ADDRESS	CC PULSE POINTS CONTROLLED BY GCP INSTRUCTION	PULSE SOURCE	OCTAL ADDRESS	CC PULSE POINTS CONTROLLED BY GCP INSTRUCTION
	04000101	SPARE	PGOPUCM	04001001	EXECUTE PU ORDER (MAINTENANCE, CPD ENABLED)
	0102	SPARE	PGOPUCN	1002	EXECUTE PU ORDER (NORMAL, CPD ENABLED)
PSSLPS	0104	SET FORCE PROGRAM STORE TO APPEAR SLOW	PGOPUKM	1004	EXECUTE PU ORDER (MAINTENANCE, CODED ENABLED)
PSSLCS	0110	SET FORCE CALL STORE TO APPEAR SLOW	PGOPUKN	1010	EXECUTE PU ORDER (NORMAL, CODED ENABLED)
PCSPCS	0120	CLEAR FORCE CALL AND PROGRAM STORE TO APPEAR SLOW	PFCG	1020	FALSE-CROSS-AND-GROUND TEST
PSOFPS	0140	SET OTHER CC ACCESSED AS FAST PROGRAM STORE	PRESET	1040	RESET NETWORK CONTROLLER (CPD)
PCOFPC	0201	CLEAR OTHER CC ACCESSED AS FAST CALL PROGRAM STORE	PCFAUA	2001	CLEAR FORCE AU ADDRESS FF
PSOFCS	0202	SET OTHER CC ACCESSED AS FAST CALL STORE	PSFAUA	2002	SET FORCE AU ADDRESS FF
PULAX1	0204	PU LOOP-AROUND EXECUTE BUS 1	PCTOLL	2004	CLEAR TOLL FF
PULAM21	0210	PU LOOP-AROUND MAPPING 2, BUS 1	PSTOLL	2010	SET TOLL FF
PULAM11	0220	PU LOOP-AROUND MAPPING 1, BUS 1	PCPUBR	2020	CLEAR PUBR FF
PULAM01	0240	PU LOOP-AROUND MAPPING 0, BUS 1	PSPUBR	2040	SET PUBR FF
PULAX0	0401	PU LOOP-AROUND EXECUTE BUS 0	PCPUBT	4001	CLEAR PUBT FF
PULAM20	0402	PU LOOP-AROUND MAPPING 2, BUS 0	PSPUBT	4002	SET PUBT FF
PULAM10	0404	PU LOOP-AROUND MAPPING 1, BUS 0	PCPUBA	4004	CLEAR PUBA FF
PULAM00	0410	PU LOOP-AROUND MAPPING 0, BUS 0	PSPUBA	4010	SET PUBA FF
PSCSRS	0420	START MAINTENANCE CLOCK IN SYNC	PCPUBO	4020	CLEAR PUBO FF
PSCSPS	04000440	STOP OPERATIONAL AND MAINTENANCE CLOCK	PSPUBO	04004040	SET PUBO FF

FIG. 2 – Sample of Pulse Source Table From FS 80, SD-5A010



NOTE 1
If you are not sure what the instructions relate to request help from your Technical Assistance Center

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ANALYZE C-LEVEL INTERRUPT MESSAGE

```
A 29 REPT: C-LEVEL @04172645 MFNUM=00000407 MICON=00000023  COMPLETED
     LV=0004 D0=00001001 D1=00000000 D2=00000000 D3=00000000

     CCFR REMOVED CC 1

     DATA: C-LEVEL
     00000006 00001132 04167306 00006000 00177777 00000010
     04171474 04172717 00301500 04172645 00000404 04172643
     00021711 04172646 62005455 00004003 01620002 00450003
     00021711 00021711 00000000 00000000 00000000 00000000
     00000000 00000000 00000000 00000000 00177777 00000000
     04172643 00021711 04172646 00301500

     (POSSIBLE MAC CONTROL DATA TO BE CONSIDERED)

     DATA: ACTIVE CC REGISTERS
     00177777 77250777 00000006 00000000 00001132 35250000
     00006000 00000001 00000010 42120206 04171474 00000000
     04172717 00000001 04167306 00140000 00301500 00000000
     00301500 20000401 04217762 77777777 00021711 00000000
     00000000 77777777 00000000 00177777 00000000 00450003
     01620002 00000000 00000000 06000000 00000000 00000000
     01004000 10040404 00000000 07410022 34000000 00004003
     70125477 00004001 00020200 62005455 00000003 00014000
     17600001 00000002 00013400 03400000 26660000 00000000
     00000000 00000000 00140000 00000000 00000000 00000000
     00000000 00000040 07000001 00000000 00000000 00000000

     DATA: STANDBY CC REGISTERS
     00177777 77250777 00000006 00000000 00001132 35250000
     00006000 00000001 00000010 42120206 04171474 00000000
     04172717 00000001 04167306 00140000 00201600 00000000
     00201600 04000401 04217762 77777777 00000000 00021711
     00000000 77777777 00000000 00000000 00000000 00450003
     02610002 00000000 00000000 06000000 00010000 00000000
     00002200 10440400 00000000 07410022 34000000 00004003
     31020644 00010001 00020200 42005055 06003003 00014004
     17600001 00000002 00213400 43400000 26660000 00000000
     00000000 00000000 00140000 00000000 00000000 00000000
     00000000 00000040 07000000 00000000 00000000 00000000
```

FIG. 1 - Sample of C-Level Interrupt Printout

DATA: C-LEVEL

1	IN1FR	IN1GR	IN1JR	IN1KR	IN1LR	IN1XR
2	IN1YR	IN1ZR	IN1BR	IN1CAR	IN1ILA	IN1SCA
3	IN1SDA	IN1SPA	IN1CSC	IN1INS	IN1MSR	IN1MMR
4	IN1MIO	ST1MEO	IN1CMO	IN1MI1	ST1ME1	IN1CM1
5	ST1MIO	IN1MEO	ST1CMO	ST1MI1	IN1ME1	ST1CM1
6	ST1SCA	ST1SDA	ST1SPA	ST1BR		

DATA: ACTIVE CC REGISTERS

1	AC1LR	AC1LRS	AC1FR	AC1FRS	AC1GR	AC1GRS
2	AC1KR	AC1KRS	AC1XR	AC1XRS	AC1YR	AC1YRS
3	AC1ZR	AC1ZRS	AC1JR	AC1JRS	AC1ER	AC1PRM
4	AC1PRL	AC1RR	AC1SR	AC1BCO	AC1MIO	AC1MEO
5	AC1CMO	AC1BC1	AC1MI1	AC1ME1	AC1CM1	AC1MMR
6	AC1MSR	AC1MOR	AC1M1R	AC1MCP	AC1MCO	AC1MCD
7	AC1CES	AC1ILA	AC1ILR	AC1INH	AC1INJ	AC1INS
8	AC1BCS	AC1PES	AC1PCR	AC1CSC	AC1PSC	AC1MDF
9	AC1DE	AC1SC	AC1LPA	AC1UPA	AC1ABK	AC1SVG
10	AC1AAS	AC1AMB	AC1AMC	AC1RIG	AC1RQG	AC1ARR
11	AC1AWF	AC1EVG	AC1AMA	AC1AWS	AC1EBG	AC1VRG

DATA: STANDBY CC REGISTERS

1	ST1LR	ST1LRS	ST1FR	ST1FRS	ST1GR	ST1GRS
2	ST1KR	ST1KRS	ST1XR	ST1XRS	ST1YR	ST1YRS
3	ST1ZR	ST1ZRS	ST1JR	ST1JRS	ST1ER	ST1PRM
4	ST1PRL	ST1RR	ST1SR	ST1BCO	ST1MIO	ST1MCO
5	ST1CMO	ST1BC1	ST1MI1	ST1ME1	ST1CM1	ST1MMR
6	ST1MSR	ST1MOR	ST1M1R	ST1MCP	ST1MCO	ST1MCD
7	ST1CES	ST1ILA	ST1ILA	ST1INH	ST1INJ	ST1INS
8	ST1BCS	ST1PES	ST1PCR	ST1CSC	ST1PSC	ST1MDF
9	ST1DE	ST1SC	ST1LPA	ST1UPA	ST1ABK	ST1SVG
10	ST1AAS	ST1AMB	ST1AMC	ST1RIG	ST1RQG	ST1ARR
11	ST1AWF	ST1EVG	ST1AMA	ST1AWS	ST1EBG	ST1VRG

FIG. 2 - C-Level Interrupt Printout Register Identification

ANALYZE C-LEVEL INTERRUPT MESSAGE

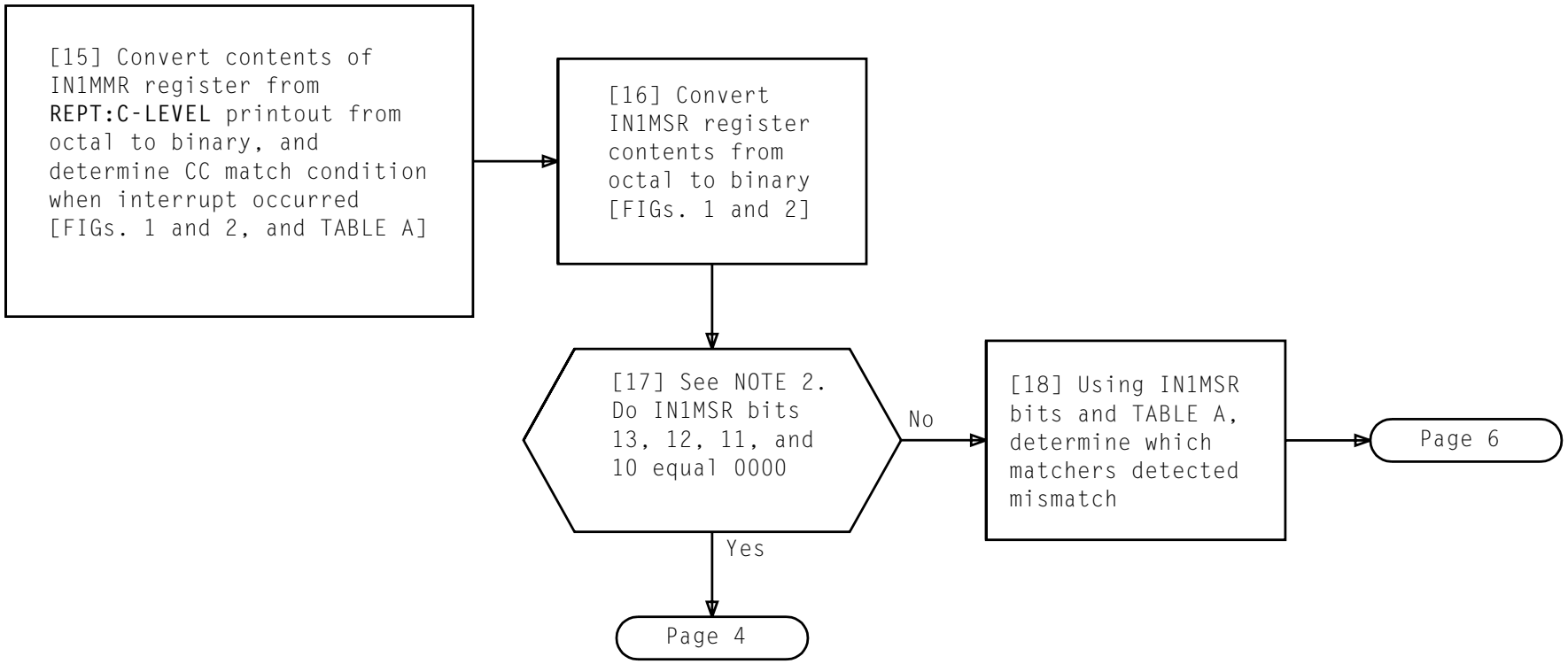
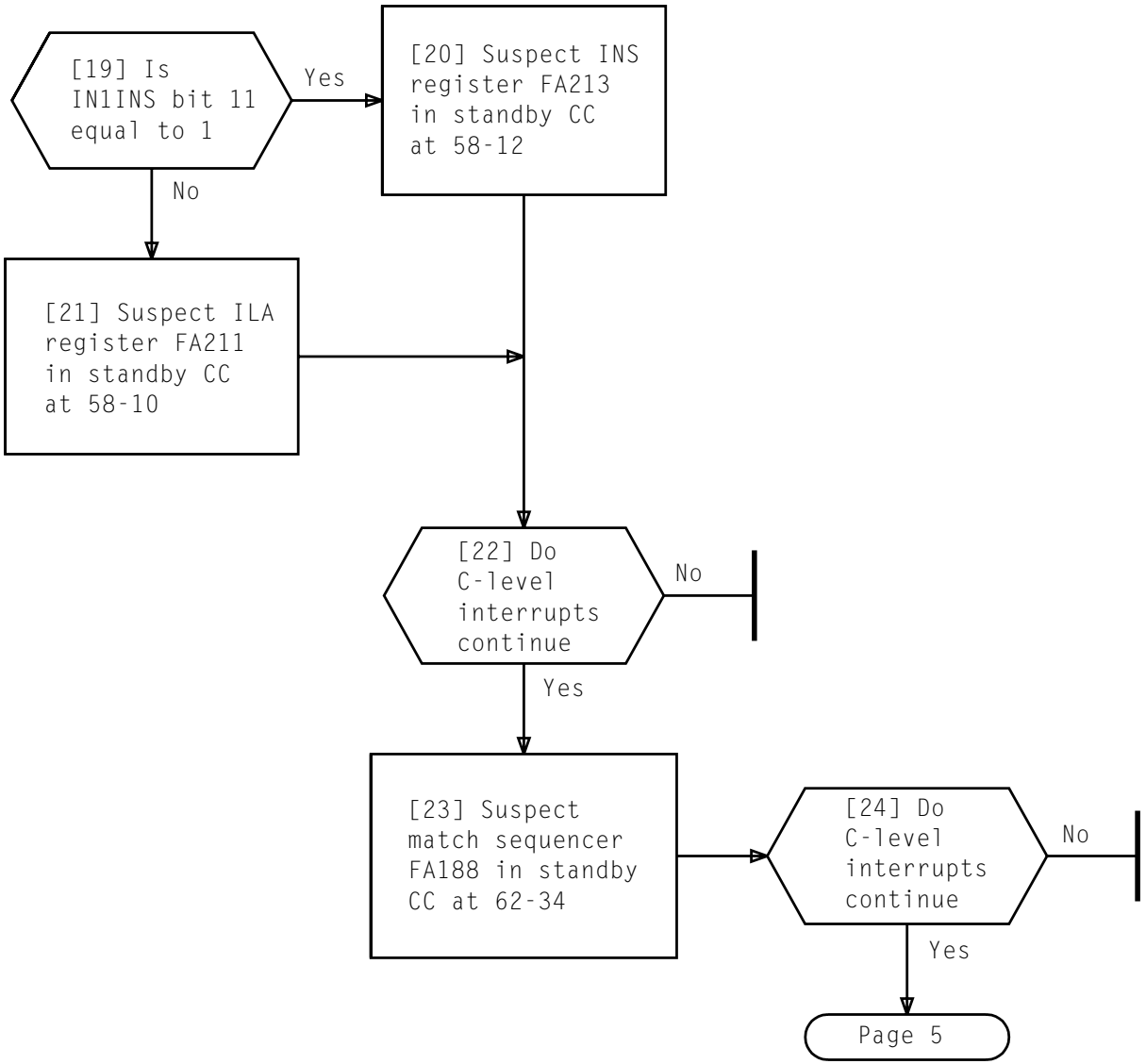


TABLE A
IN1MMR AND IN1MSR BIT INTERPRETATION FOR MATCHING TYPE

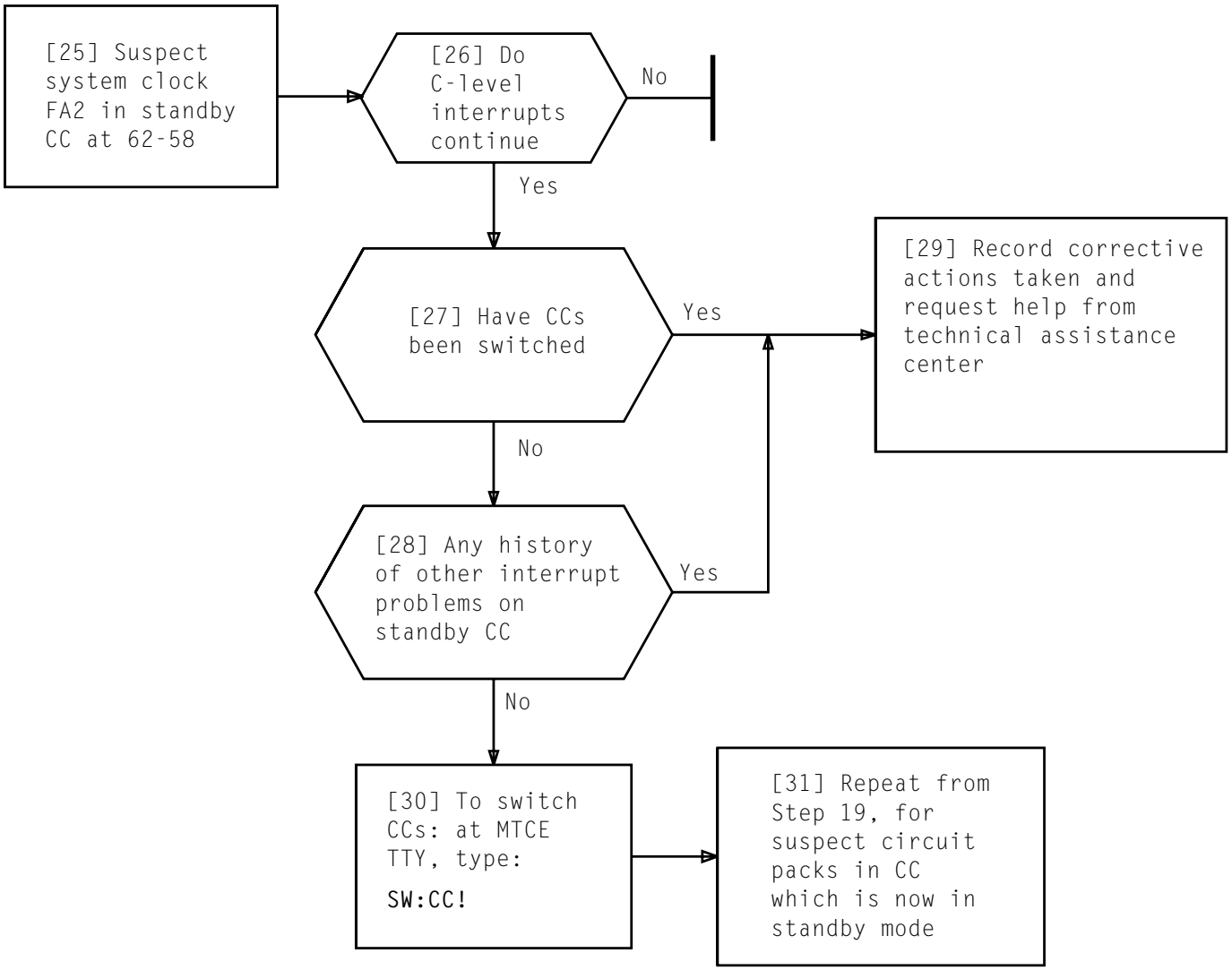
STATE OF IN1MM BITS 1,0	CC MATCH CONDITION	MATCHER WHICH DETECTED MISMATCH
01	Active CC Routine Matching	IN1MSR Bit 10 = 1:IN1MI0 ≠ ST1ME0 Active CC — Matcher 0 IN1MSR Bit 12 = 1:IN1MI1 ≠ ST1ME1 Active CC — Matcher 1
10	Standby CC Routine Matching	IN1MSR Bit 11 = 1:ST1MI0 ≠ IN1ME0 Standby CC — Matcher 0 IN1MSR Bit 13 = 1:ST1MI1 ≠ IN1ME1 Standby CC — Matcher 1
11	Both CCs Routine Matching	IN1MSR Bit 10 = 1:IN1MI0 ≠ ST1ME0 Active CC — Matcher 0 IN1MSR Bit 11 = 1:ST1MI0 ≠ IN1ME0 Standby CC — Matcher 0 IN1MSR Bit 12 = 1:IN1MI1 ≠ ST1ME1 Active CC — Matcher 1 IN1MSR Bit 13 = 1:ST1MI1 ≠ IN1ME1 Standby CC — Matcher 1

NOTE 2
IN1MSR bits 13, 12, 11, and 10 equaling 0000 indicates no mismatch was detected. Interrupt was triggered by other means

ANALYZE C-LEVEL INTERRUPT MESSAGE



ANALYZE C-LEVEL INTERRUPT MESSAGE



ANALYZE C-LEVEL INTERRUPT MESSAGE

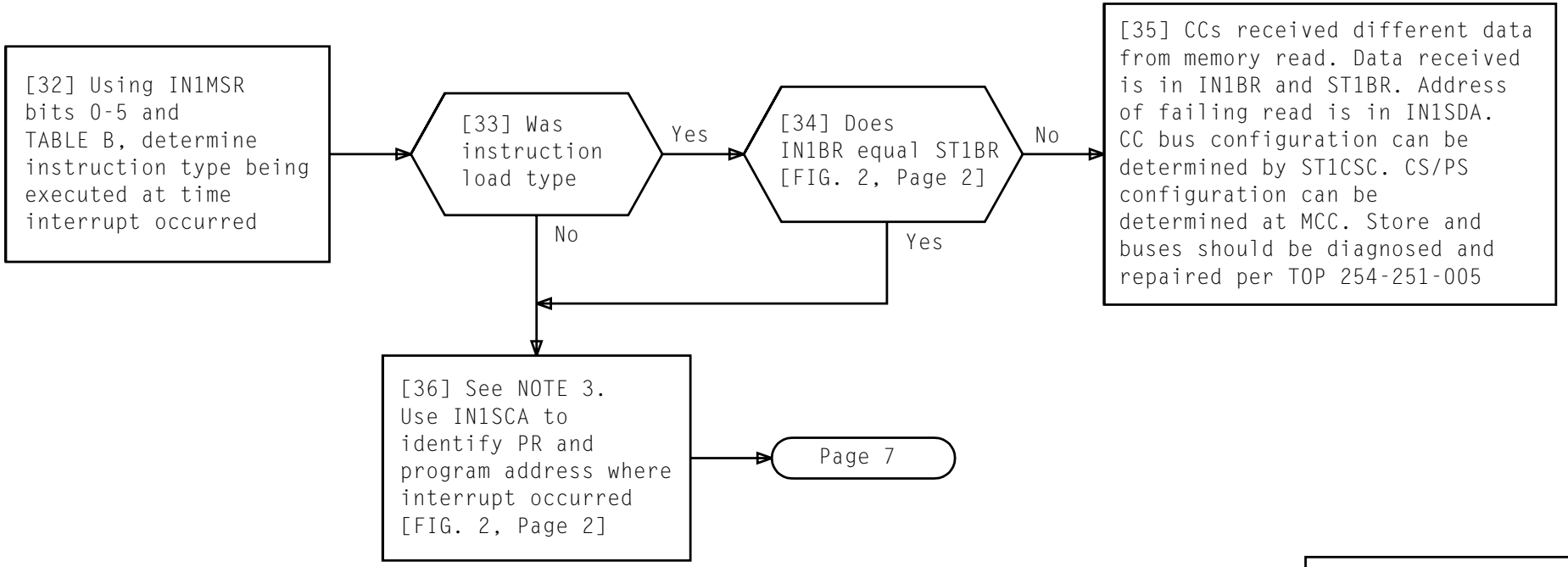


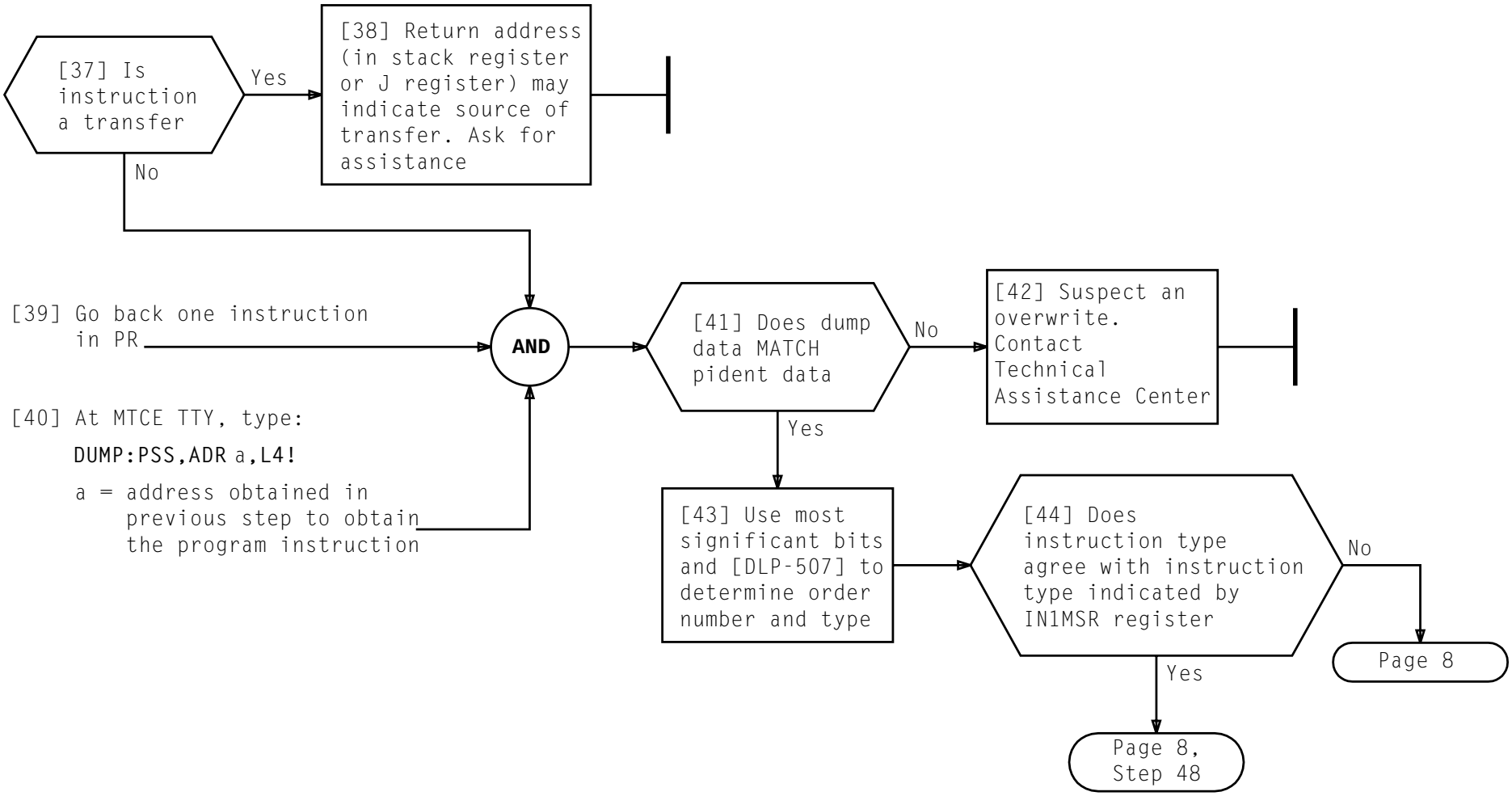
TABLE B

IN1MSR BITS 5, 4, 3, 2, 1, 0 =	INSTRUCTION TYPE
000001	Transfer
000010	Load
000100	Store
001000	Word
010000	Miscellaneous
100000	Push/Pop

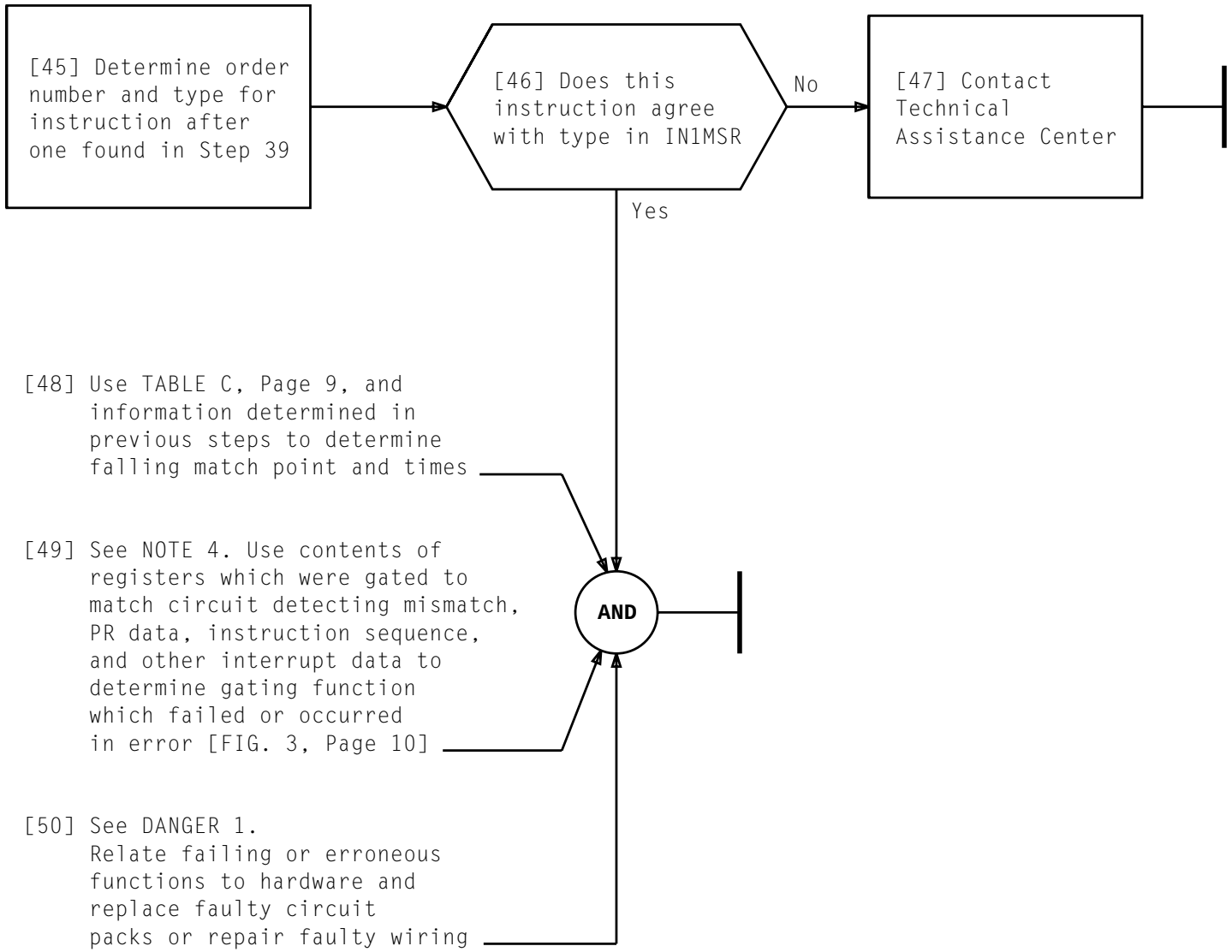
NOTE 3

Failing instruction may be either instruction pointed to by IN1SCA or instruction previous to that one. Final decision on which instruction failed depends on instruction type, number of cycles used by instruction, and whether IN1SCA points to an obvious entry point into program

ANALYZE C-LEVEL INTERRUPT MESSAGE



ANALYZE C-LEVEL INTERRUPT MESSAGE



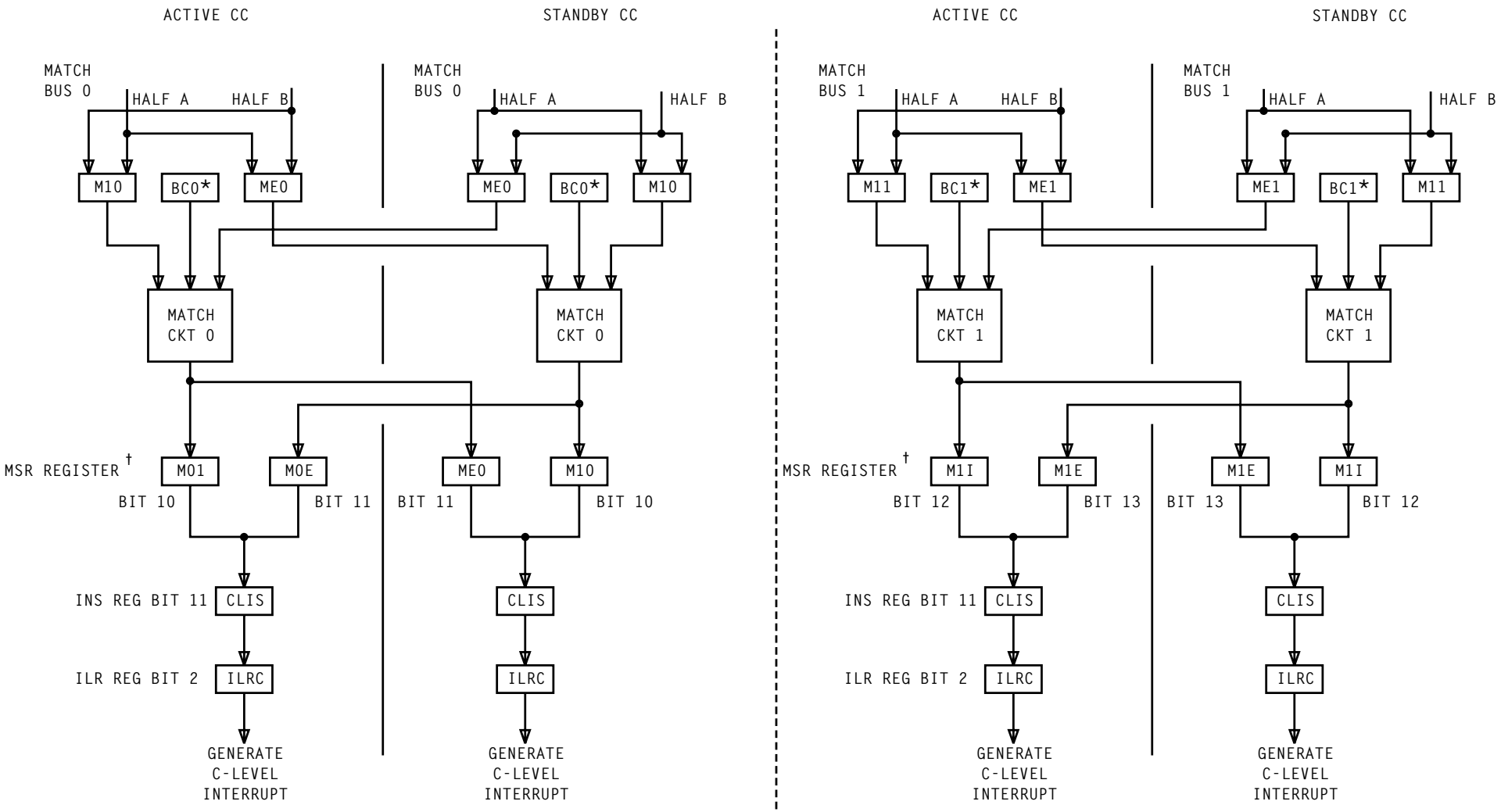
NOTE 4
SD5A010 SC2 can be used to determine number of machine cycles used by this instruction

DANGER 1
Presences of −48V and +24V power constitutes personal hazard

ANALYZE C-LEVEL INTERRUPT MESSAGE

TABLE C
DATA SELECTION FOR ROUTINE MATCHING (MATCH POINTS AND TIMES)

			INSTRUCTION TYPE													
			MSR BITS						MISMATCH DETECTED IN ACTIVE CC				MISMATCH DETECTED IN STANDBY CC			
	MMR BITS		5	4	3	2	1	0	MATCHER 0		MATCHER 1		MATCHER 0		MATCHER 1	
	1	0	PUSH / POP	MISC	WORD	STORE	LOAD	TRANS	MSR BIT 10 = 1		MSR BIT 12 = 1		MSR BIT 11 = 1		MSR BIT 13 = 1	
	RS	RA							POINT	TIME	POINT	TIME	POINT	TIME	POINT	TIME
BOTH CCs ROUTINE MATCHING	1	1	0	0	0	0	0	1	PAR	4T8	BR	0T4	SC	8T0	MB	4T8
	1	1	0	0	0	0	1	0	DAR	8T0	MB	0T4	MB	4T8	MB	8T0
	1	1	0	0	0	1	0	0	DAR	8T0	BR	0T4	MB	4T8	MB	8T0
	1	1	0	0	1	0	0	0	DAR	8T0	MB	8T0	MB	4T8	UB	4T8
	1	1	0	1	0	0	0	0	PAR	4T8	BR	0T4	SC	8T0	DAR	8T0
	1	1	1	0	0	0	0	0	SC	8T0	BR	0T4	DAR	8T0	MB	8T0
ACTIVE CC ONLY ROUTINE MATCHING	0	1	0	0	0	0	0	1	PAR	4T8	BR	0T4				
	0	1	0	0	0	0	1	0	DAR	8T0	MB	0T4				
	0	1	0	0	0	1	0	0	DAR	8T0	BR	0T4				
	0	1	0	0	1	0	0	0	DAR	8T0	MB	8T0				
	0	1	0	1	0	0	0	0	PAR	4T8	BR	0T4				
	0	1	1	0	0	0	0	0	SC	8T0	BR	0T4				
STANDBY CC ONLY ROUTINE MATCHING	1	0	0	0	0	0	0	1					PAR	4T8	BR	0T4
	1	0	0	0	0	0	1	0					DAR	8T0	MB	0T4
	1	0	0	0	0	1	0	0					DAR	8T0	BR	0T4
	1	0	0	0	1	0	0	0					DAR	8T0	MB	8T0
	1	0	0	1	0	0	0	0					PAR	4T8	BR	0T4
	1	0	1	0	0	0	0	0					SC	8T0	BR	0T4
MSR = IN1MSR MMR = IN1MMR			Y	X	W	S	L	T	MISMATCH BETWEEN IN1MI0 AND ST1ME0		MISMATCH BETWEEN IN1MI1 AND ST1ME1		MISMATCH BETWEEN ST1MI0 AND IN1ME0		MISMATCH BETWEEN ST1MI1 AND IN1ME1	



*BCO BIT CONTROL REGISTER 0
BCO REGISTER PROVIDES A MASK. ONLY THE BITS WHERE ONES APPEAR IN BCO ARE MATCHED. FOR ROUTINE MATCHING, THE BIT CONTROL REGISTERS ARE WRITTEN TO ALL "ONES"

†INDICATES A MISMATCH WHEN SET

*BC1 BIT CONTROL REGISTER 1
BC1 REGISTER PROVIDES A MASK. ONLY THE BITS WHERE ONES APPEAR IN BC1 ARE MATCHED. FOR ROUTINE MATCHING, THE BIT CONTROL REGISTERS ARE WRITTEN TO ALL "ONES"

†INDICATES A MISMATCH WHEN SET

FIG. 3 — CC Matchers 0 and 1

ANALYZE C-LEVEL INTERRUPT MESSAGE

Guidelines for further analysis of TTY printouts are provided below. The level of action taken is determined by the resulting indications from the analysis.
CAUTION: Do not perform indicated maintenance until equipment considerations are met

See FIG. 1.

1. Use contents of CRO1 (ACT,STB) [TABLE A] register for status of monitored leads, especially TAPF, TWEF, TDPF, and TRFDPF1 [FIG. 2]

2. Determine system configuration at time of interrupt. During normal duplex operation, D LEVEL IN1CSC register bits 0-5 identify system configuration. However, for D-level interrupt only, one CC may indicate the error. Therefore, determine state of standby CC by examining state of bit 7 in CSID SYSSTAT register. If bit 7 is one, standby CC is in service, and bits 0-5 identify system configuration. If bit 7 is zero, standby CC is out of service (OOS), and bits 0-5 of CSID IBUSSTAT register should be used to identify system configuration [FIG. 3]

3. Analyze contents of D LEVEL IN1CES and ST1CES registers for pertinent error summaries relating to system configuration [FIG. 4]

4. Compare contents of D LEVEL IN1BR register with contents of C (FAILING ADDRESS) register. Verify results by use of PR listing at the address where D-level occurred [FIG. 5]

5. Use ERAP to collect error summary results on D-level interrupts

TABLE A

PS/CS (ID) CRO1 REG		
CRO1	CSID REG	PSID REG
ACT	23	27
STBY	30	34

D-LEVEL

IN1FR	IN1GR	IN1JR	IN1KR	IN1LR	IN1XR
IN1YR	IN1ZR	IN1BR	IN1CAR	IN1ILA	IN1SCA
IN1SDA	IN1SPA	IN1CSC	IN1INS	IN1INH	IN1SC
IN1SR	IN1INJ	IN1CES	ST1CES		

FIG. 1 — D-Level Register Layout

GUIDELINES FOR D/E LEVEL INTERRUPT ANALYSIS, SEMICONDUCTOR STORE

MODE = READ
ADDRESS = 6100001

CONTROL READ 01

COMPOOL MNEMONIC = DRW01
SD 5A040-01
GATEOUT ENABLE: SCR1
GATEOUT SELECT: CR010

(32406010) BIT	SAMPLE	FUNCTION NAME	COMPOOL ALIAS	SD	FS/SYM	LEAD DESIG	CPS REG/GATE NAME	DESCRIPTION
00	0	ANS01		40	1/3	ANS01	ANS0	OUTPUT OF ANSWER ON BUS 0 FF
01	0	ANS11		40	1/3	ANS11	ANS1	OUTPUT OF ANSWER ON BUS 1 FF
02	0	R01		40	1/3	OR01	R0	FANOUT FROM R0 FF
03	1	R00		40	1/3	OR00	R0	FANOUT FROM R0 FF
04	0	N001		40	1/3	N001	N00	OUTPUT OF VARIABLE NAME REGISTER BIT 0
05	0	N011		40	1/3	N011	N01	OUTPUT OF VARIABLE NAME REGISTER BIT 1
06	0	N021		40	1/3	N021	N02	OUTPUT OF VARIABLE NAME REGISTER BIT 2
07	0	N031		40	1/3	N031	N03	OUTPUT OF VARIABLE NAME REGISTER BIT 3
08	0	N041		40	1/3	N041	N04	OUTPUT OF VARIABLE NAME REGISTER BIT 4
09	0	UPDT		40	1/3	UPDT1	UPDT	OUTPUT OF STORE UPDATE FF
10	1	TWF1		40	1/3	TWF1	TWF	OUTPUT OF TWF FF
11	1	FRH0		40	1/3	FRH0	FRH	OUTPUT OF FRH FF
12	0							UNUSED RESPONSE
13	0							UNUSED RESPONSE
14	0							UNUSED RESPONSE
15	0							UNUSED RESPONSE
16	0							UNUSED RESPONSE
17	1	TRFDPF1		40	1/3	TRFDPF1	TRFDPF	OUTPUT OF TRFDPF FF
18	0	TDPF1		40	1/3	TDPF1	TDPF	OUTPUT OF TDPF FF
19	1	TWEF1		40	1/2	C190	TWEF	DATA BIT 19 OF CONTROL READ OPERATION*
20	0	TAPF1		40	1/2	C200	TAPF	DATA BIT 20 OF CONTROL READ OPERATION*
21	1	CRI0		40	1/3	CRI0	CRI	OUTPUT OF CRI FF
22	1	MTCE1		40	1/3	MTCE1	MTCE	OUTPUT OF MTCE FF
23	0	TME1		40	1/2	C230	TME	DATA BIT 21 OF CONTROL READ OPERATION*

* OUTPUTS OF THE TWEF, TAPF, AND TME FFS ARE NOT DIRECTLY ACCESSIBLE FROM CIRCUIT-PACK PINS

MODE = READ
ADDRESS = 6100001

INDICATED RESPONSES

BIT 20 - NO TAPF1
BIT 19 - TWEF
BIT 18 - NO TDPF1
BIT 17 - TRFDPF1

FIG. 2 — Analyze Printouts to Identify Read Results — CTRLR1

1. MODE=READ
ADDRESS=160

CENTRAL CONTROL STATUS FFS

SAMPLE

COMPOOL MNEMONIC = CSC = 00001657

SD5A010-01 OR -02

GATEOUT ENABLE = CSCBRO

BIT	OP	FUNCTION NAME	COMPOOL ALIAS	SD	FS/SYM	LEAD DESIG	CPS REG/GATE NAME	DESCRIPTION
1	00	PBO		10	1/1	BRBAA000	PBAO(A)	PS BUS CONTROL - ACTIVE SEND ON BOTH
1	01	PBA		10	1/1	BRBAA010	PBAO(B)	PS BUS CONTROL - ACTIVE BUS
1	02	PBT		10	1/1	BABAA020	CPB(A)	PS BUS CONTROL - STANDBY BUS TROUBLE
1	03	CBO		10	1/1	BRBAA030	CPB(B)	CS BUS CONTROL - ACTIVE SEND ON BOTH
0	04	CBA		10	1/1	BRBAA040	CTA(A)	CS BUS CONTROL - ACTIVE BUS
1	05	CBT		10	1/1	BRBAA050	CTB(B)	CS BUS CONTROL - STANDBY BUS TROUBLE

SAMPLE

2. SYSSTAT = 00000057 ## SYSTEM STATUS AT TIME OF INTERRUPT

SYSSTAT LAYOUT ABC:DEF:GHI:JKL:MNO:PQR:STU:VWX

X	PRTBKZP	ITEM	N	# INDICATES KCODE 20 HAS BEEN PUMPED
0	CCS	ITEM	Q	# STATE OF CC1CCS AT INTERRUPT
1	ST1CBT	ITEM	S	# CBT OF STANDBY CC AT ENTRY TO INTERRUPT
0	ST1CBA	ITEM	T	# CBA OF STANDBY CC AT ENTRY TO INTERRUPT
1	ST1CBO	ITEM	U	# CBO OF STANDBY CC AT ENTRY TO INTERRUPT
X	ST1PBT	ITEM	V	# PBT OF STANDBY CC AT ENTRY TO INTERRUPT
X	ST1PBA	ITEM	W	# PBA OF STANDBY CC AT ENTRY TO INTERRUPT
X	ST1PBO	ITEM	X	# PBO OF STANDBY CC AT ENTRY TO INTERRUPT

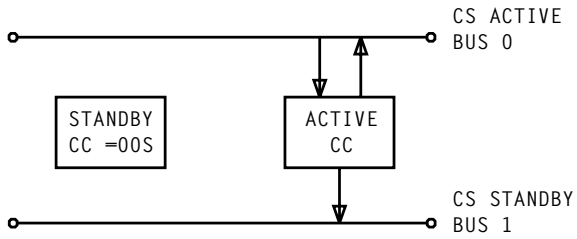
SAMPLE

3. IBUSSTAT = 04000050 ## BUSSTAT AT INTERRUPT ENTRY

IBUSSTAT LAYOUT ABC:DEF:GHI:JKL:MNO:PQR:STU:VWX

1	CBT	ITEM	S	# BOTH CCS WILL RECEIVE FROM THE # ACTIVE BUS WHEN SET. CS ONLY
0	CBA	ITEM	T	# DEFINES THE BUS USED BY THE ACTIVE # CC. BUS 1 IS ACTIVE WHEN SET. CS ONLY
1	CBO	ITEM	U	# WHEN SET, ACTIVE CC SENDS OVER # BOTH BUSES. (SET BY INTERRUPT # SEQUENCER). CS ONLY
0	REGEN	ITEM	V	# WHEN SET, MUST SET STORE REGEN # FOR MARP AND MCC. CS ONLY
0	OFLC	ITEM	W	# USED TO INDICATE TO CALCONFIG THAT # THE CS COMMUNITY IS TO BE SET UP IN AN # OFF LINE CONFIGURATION. CS ONLY
0	NDLEV	ITEM	X	# NON D LEVEL ENTRY FLAG. CS ONLY

4. CONFIGURATION CBO = 1, CBA = 0, CBT = 1;



SYSTEM CONFIGURATION (SEE BIT DESCRIPTION)	NOTES
1. CSC: CBO = 1 CBA = 0 CBT = 1	Indicated configuration may be incorrect for simplexed CCs
2. SYSTAT: CBO = 1 CBA = 0 CBT = 1 CCS = 0	Indicated configuration may be incorrect since bit 7 (Q) is 0, and standby CC is OOS
3. IBUSSTAT: CBO = 1 CBA = 0 CBT = 1	Indicated configuration is considered as valid. In this case, all configurations agree

FIG. 3 — Analyze Printouts to Identify System Configuration

MODE=WRITE
ADDRESS=140

CENTRAL CONTROL ERROR SUMMARY

COMPOOL MNEMONIC = CES
SD5A010-01 OR - 02
COMMON CLEAR = CLCESOA (BITS 07-10, 18-19),
CLCESOB (BITS 11-17, 20-23)
GATEIN ENABLE = BRCESOA (BITS 07-10, 18-19),
BRCESOB (BITS 11-17, 20-23)

SAMPLE: ST1CES 00000240	IN1CES 03302540	FUNCTION BIT	OP	COMPOOL NAME	ALIAS	SD	FS/SYM	LEAD DESIG	CPS REG/GATE NAME	DESCRIPTION
0	0	00	E	EWPTY		10				ENABLE WRITE INTO CES PARITY BITS*
0	0	01		SCOP						UNUSED
0	0	02		DPWEFCS						UNUSED
0	0	03		DPWEFPS						UNUSED
0	0	04		OAPC		10	33/5	BR040B	OACP(B)	ODD ADDRESS PARITY CONTROL
1	1	05		DPM	DPKA	10	33/5	BR050B	MDPP(B)	ODD DATA ADDRESS PARITY MEMORY
0	1	06		PPM	PPKA	10	33/5	BR060B	MDPP(A)	ODD PROGRAM ADDRESS PARITY MEMORY
1	0	07		PPR1		10	28/3	BR070A	CBSCB(B)	AUX BUFFER ORD WORD CHECK BIT PR1
0	1	08		PPR2		10	28/4	BR080A	CBSCB(B)	AUX BUFFER ORD WORD CHECK BIT PR2
0	0	09		PPL1		10	28/1	BR090A	CBSCB(B)	AUX BUFFER ORD WORD CHECK BIT PL1
0	1	10		PPL2		10	28/2	BR100A	CBSCB(B)	AUX BUFFER ORD WORD CHECK BIT PL2
0	0	11		ASWEP		10	105/1	BR110D	PSASWE(A)	PROG STORE ALL SEEMS WELL ERROR
0	0	12		ASWFP		10	105/1	BR120D	PSASWE(B)	PROG STORE ALL SEEMS WELL FAILURE
0	0	13		PFPSR		10	105/1	BR130D	PSPF(A)	PROG STORE PARITY FAIL RIGHT
0	0	14		PFPSL		10	105/1	BR140D	PSPF(B)	PROG STORE PARITY FAIL LEFT
0	1	15		ASWEC		10	105/1	BR150D	CSASWE(A)	CALL STORE ALL SEEMS WELL ERROR
0	1	16		ASWFC		10	105/1	BR160D	CSASWE(B)	CALL STORE ALL SEEMS WELL FAILURE
0	0	17		PFCS		10	105/1	BR170D	DARPFCS(A)	CALL STORE PARITY FAILURE
0	1	18		DP1	CP1	10	33/5	BR180B	DP(B)	BUFFER REGISTER DATA CHECK BIT P1
0	1	19		DP2	CP2	10	33/5	BR190B	DP(A)	BUFFER REGISTER DATA CHECK BIT P2
0	0	20		PFAU		10	105/1	BR200D	ASWPFAUE(A)	AUXILIARY UNIT PARITY FAILURE
0	0	21		ASWEAU		10	105/1	BR210D	ASWPFAUE(B)	AUXILIARY UNIT ALL SEEMS WELL ERROR
0	0	22		MTCCS		10	105/1	BR220D	MTCPSCS(A)	CALL STORE MAINTENANCE MODE CONTROL
0	0	23		MTCPS		10	105/1	BR230D	MTCPSCS(B)	PROG STORE MAINTENANCE MODE CONTROL

* LOCK PARITY CHECK (LOKP) FLIP-FLOP IS CLEARED ON ALL CES WRITES (FS105)

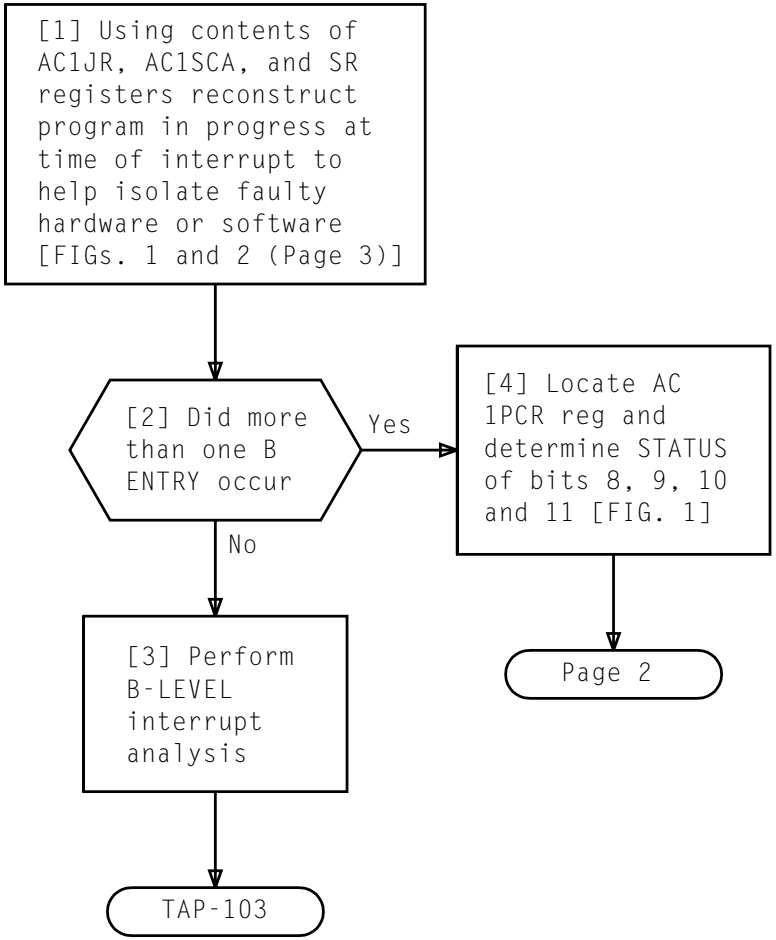
INDICATED RESPONSE

IN1CES (ACTIVE CC): ASWEC (BIT 15) AND ASWFC (BIT 16)
ST1CES (STANDBY CC); NO SIGNIFICANT RESPONSES - OOS

FIG. 4 — Analyze IN1CES and ST1CES Registers for Configuration Responses

COMPARE CONTENTS OF REGISTERS		NOTES
IN1BR	= 00000000	
C(FAILING ADDRESS)	= 00000000	CONTENTS OF BOTH REGISTERS AGREE, INDICATING CAUSE OF INTERRUPT IS IN SEMICONDUCTOR STORE
SBR	= 00000000	CONTENTS OF SBR ALSO AGREES WITH IN1BR
D-LEVEL OCCURRENCE	= 04200000	WHEN RESULTS DISAGREE, REFER TO PR LISTING FOR ADDRESS TO DETERMINE MODE OF OPERATION WHEN INTERRUPT OCCURRED

FIG. 5 — Compare Contents of IN1BR and C(FAILING ADDRESS) Registers



PCRV: FAILED

AC1BR	AC1FR	AC1GR	AC1JR	AC1KR	AC1LR
AC1XR	AC1YR	AC1ZR	AC1FRS	AC1GRS	AC1JRS
AC1KRS	AC1LRS	AC1XRS	AC1YRS	AC1ZRS	AC1SR
AC1SC	PC1HISTORY	PC1OVER-RIDE	JOB-FLGS	INH-FLGS	AC1PCR

PCRV: B-LEVEL ENTRY

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR	AC1CAR	AC1ILA	AC1SCA
AC1SDA	AC1INS	AC1INH	AC1CSC	AC1PCR	AC1SAT
AC1SR	AC1MCO	AC1MCP	AC1MCD	IB1B_PCR	IB1B_SAT

PCRV: FAIL

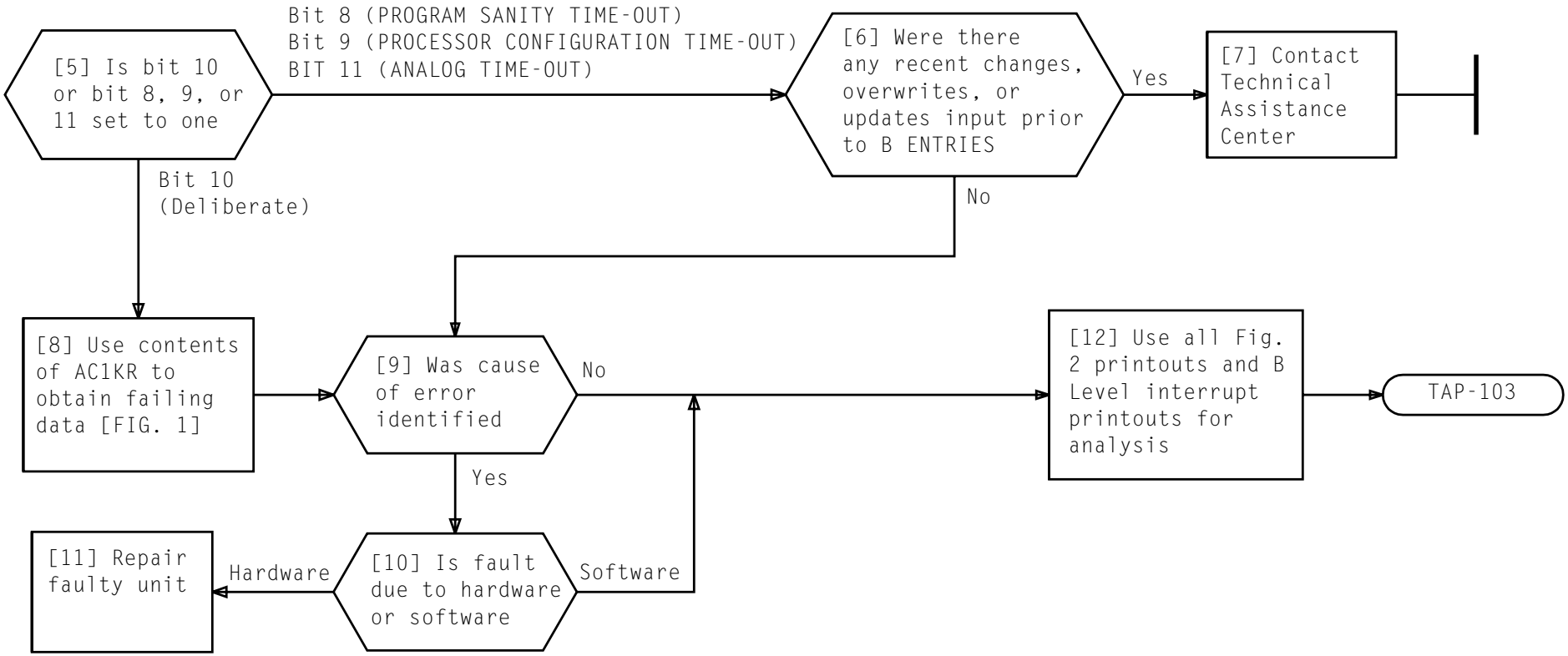
AC1JR	AC1KR	AC1SR	PC1HIS	PC1OVER-RIDE	JOB-FLGS

PCRV: B REQ

AC1JR	AC1KR	AC1SCA	AC1CSC	AC1PCR	AC1SR

FIG. 1 - B-Level Printout Register Locations

ANALYZE B-ENTRY/B-FAILED INTERRUPT



ANALYZE B-ENTRY/B-FAILED INTERRUPT

```
TOTAL TA

*C PCRV: FAILED
 00000034 14065436 00000075 14262433 00000000 00000037
 07700000 00100000 77777777 00000001 00000006 40000007
 54353235 00040000 37777777 00037401 00000000 14777221
 00000001 04000000 00000000 00000000 07700000 00000000

*C PCRV: BENTRY
 00000010 77777767 14262433 00000000 00000400 00000030
 00000130 77777631 00000010 54063131 00404012 14063131
 77777765 04002503 57637777 23031477 00022301 00001400
 14777221 00010000 06000000 00000000 00022301 00001200

*C PCRV: BENTRY
 00000010 77777767 14065347 00000105 00000400 00000001
 25252525 00000000 44021012 54021012 00444002 14063131
 77777765 00002503 77637777 23031555 00037023 00000000
 14064655 00010000 06000000 00000000 00037323 71340405

*C PCRV: FAILED
 14064655 00000000 00000000 14067576 00000105 00000500
 17600000 00047107 00000105 20077777 00000000 14115367
 25252525 01400000 17600000 25252525 00000000 14064655
 00000001 02020220 00000000 00000020 10000000 00037023

*C PCRV: BENTRY
 00000010 77777767 14067576 00000105 00000400 00000030
 00000130 77777631 00000010 54063131 00404002 14063131
 77777765 00002503 57637777 23031577 00037024 00000000
 14064655 00010000 06000000 00000000 00037324 51040404

*C PCRV: FAIL
 14067576 00000105 14064655 02020020 00000000 00000020

*C PCRV: B REQ
 14067576 00000105 14063131 23031555 00037025 14064655

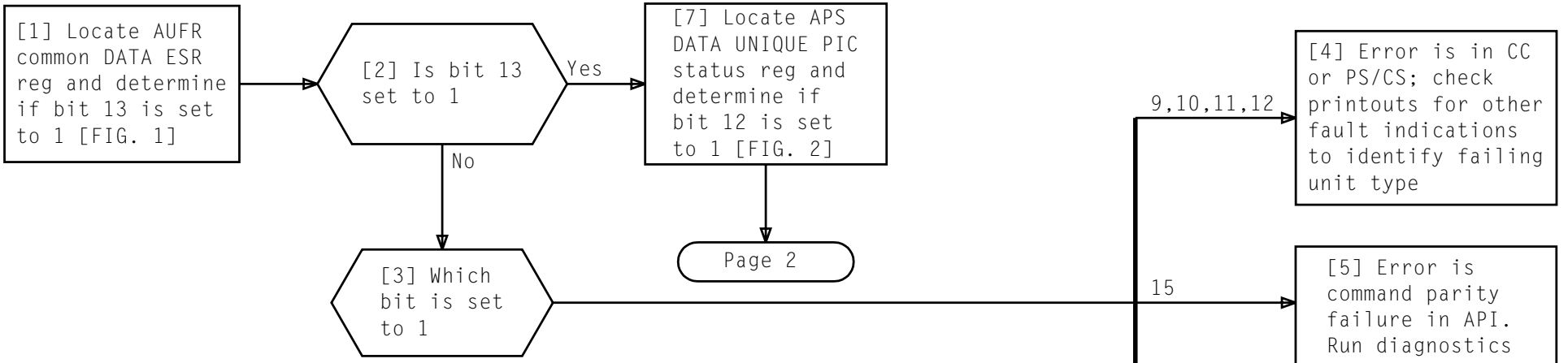
                           ¦
                           ¦
                           ¦

*C PCRV: FAIL
 14262433 00000000 14420666 22070264 00000000 00000000

*C PCRV: B REQ
 14262433 00000000 14063131 22031455 00022045 14420666
```

FIG. 2 — B-Entry/B-Failed Printout

ANALYZE B-ENTRY/B-FAILED INTERRUPT

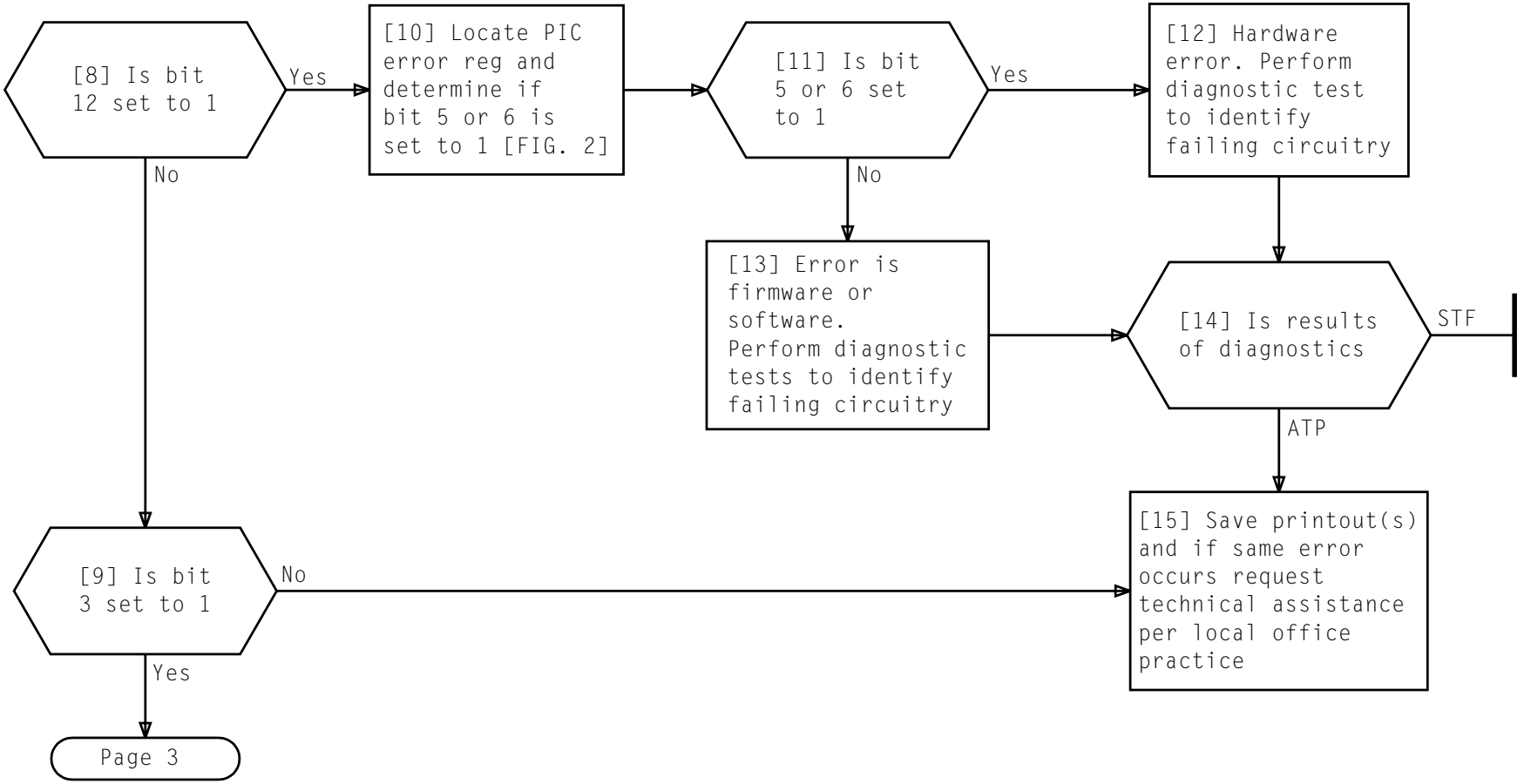


COMMON AUXILIARY UNIT DATA

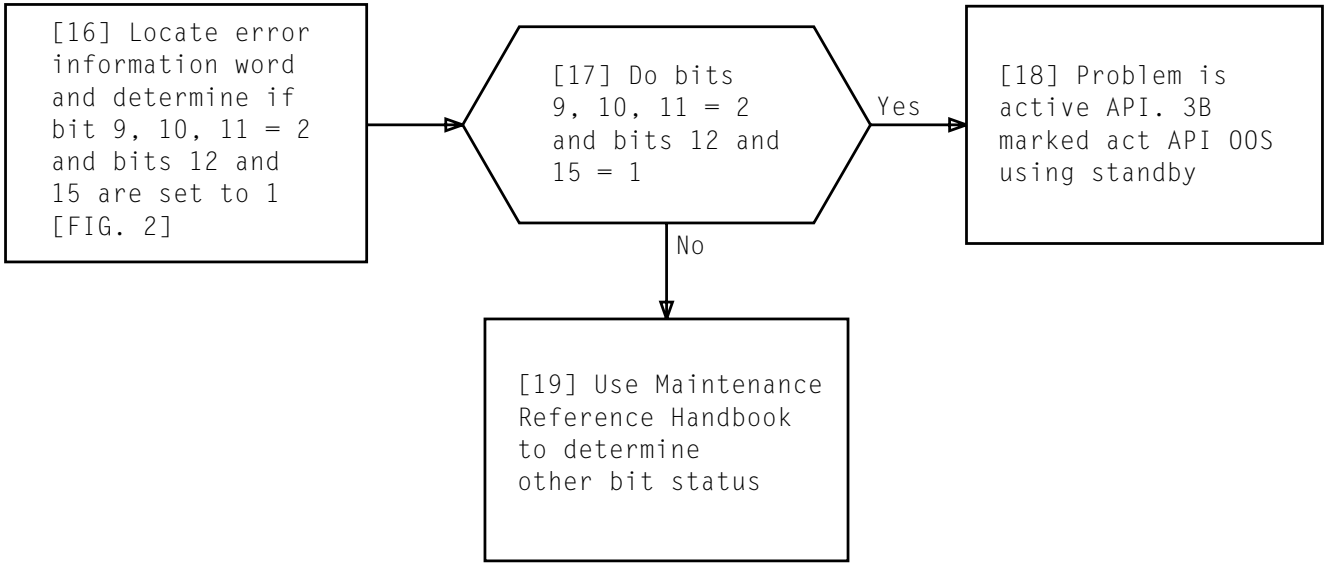
RBSTAT#	RSTAT0#	RSTAT1#	RSTAT2#	RSTAT3#	RSTAT4#
RSTAT5#	RSTAT6#	RSTAT7#	RSTAT8#	RSTAT9#	RSTAT10#
RSTAT11#	RSTAT12#	RSTAT13#	RSTAT14#	RSTAT15#	AC1AMC
AC1AMB	AC1RIG	AC1RQG	AC1EVG	AC1EBG	AC1SVG
AC1VRG	AC1ABK	AC1AMA	AC1AAS	AC1ARR	AC1AWF
AC1AWS	ST1AMC	ST1AMB	ST1RIG	ST1RQG	ST1EVG
ST1EBG	ST1SVG	ST1VRG	ST1ABK	ST1AMA	ST1AAS
ST1ARR	ST1AWF	ST1AWS	RSAVKCD#	RCPSR#	ESR0#
RPSR#	RCFA#	RCFD#	RSFA#	RSFD#	RFAPF#
RFARQ#	RFEVB#	RSYSW#	RPGWD#	RFSAVG#	RFSAVJ#
RFSAVX#	RFSAVF#	RSFSAVY#	RFSAVK#	RPSCES#	RJRAB#
RBSTAT#	RSTAT0#	RSTAT1#	RSTAT2#	RSTAT3#	RSTAT4#
RSTAT5#	RSTAT6#	RSTAT7#	RSTAT8#	RSTAT9#	RSTAT10#
RSTAT11#	RSTAT12#	RSTAT13#	RSTAT14#	RSTAT15#	AC1CSC

FIG. 1 - D-Level Interrupt Printout Common Auxiliary Unit Data

ANALYZE APFR D-LEVEL INTERRUPT/INTERJECT



ANALYZE APFR D-LEVEL INTERRUPT/INTERJECT



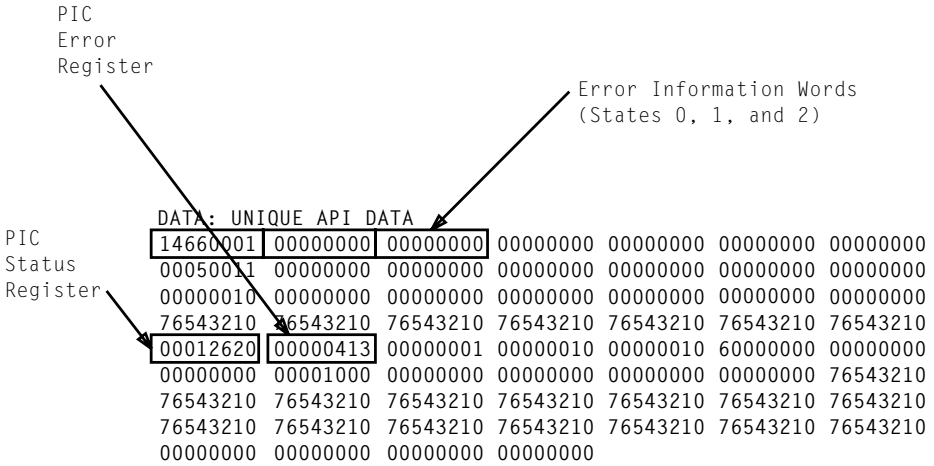


FIG. 2 — D-Level Interrupt Printout Unique API Data

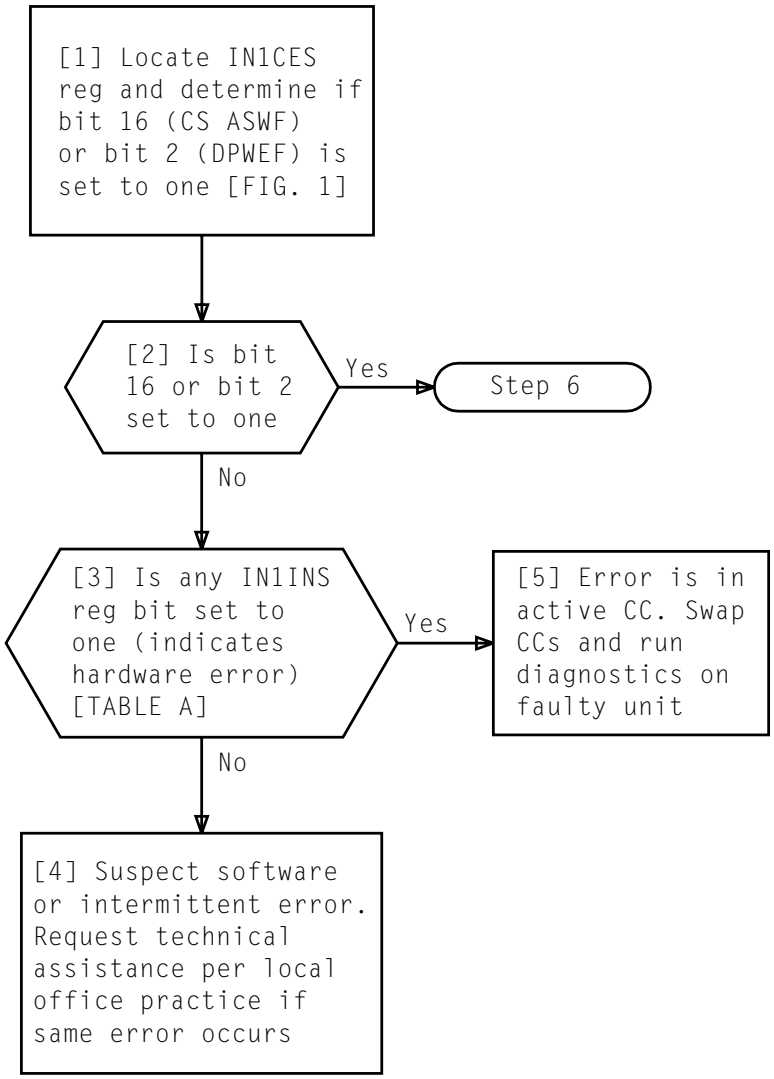
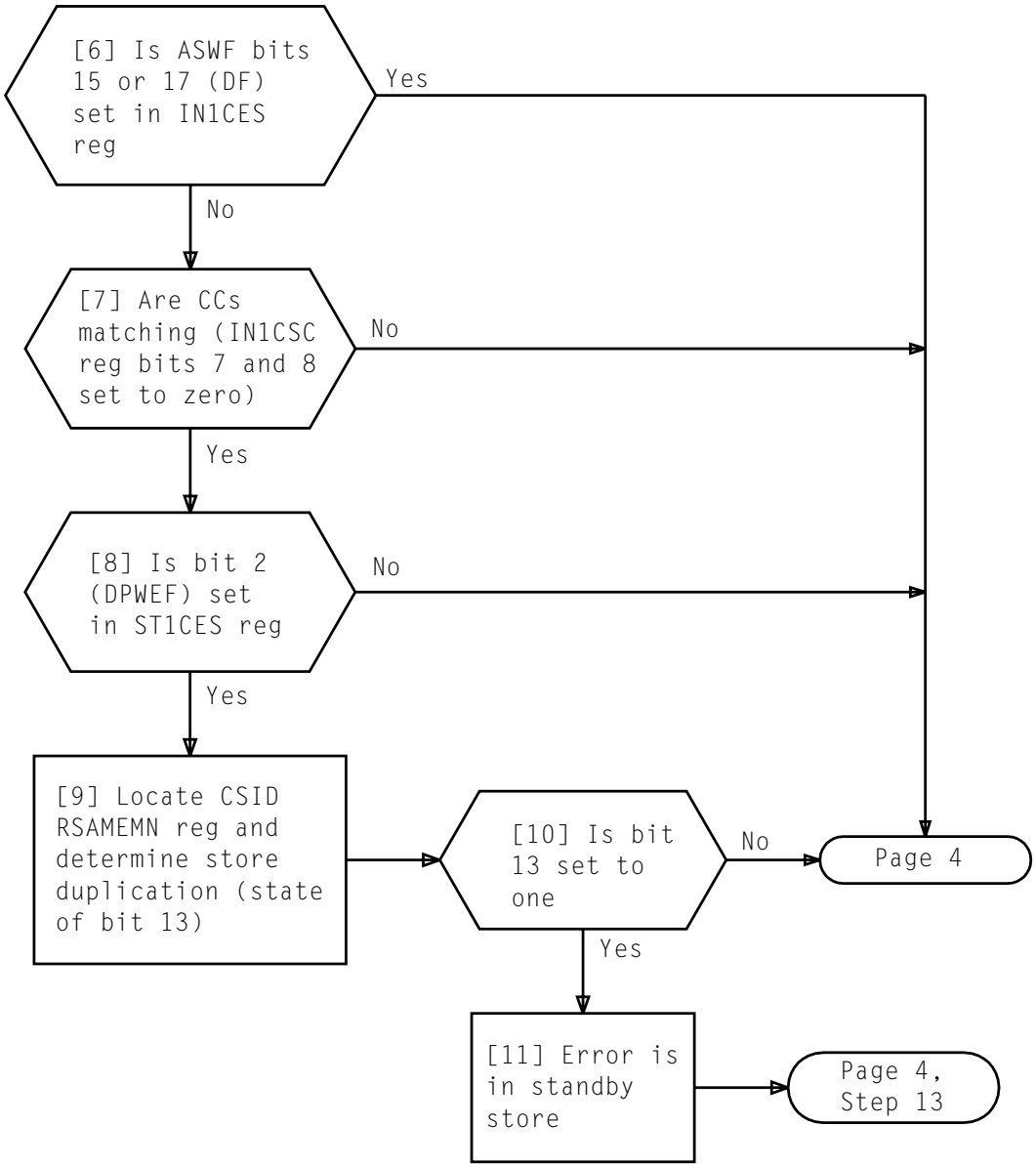


TABLE A

256K STORE					64K STORE	
BITS	MEMORY PLANE	SUSPECT PACK		LOC	SUSPECT PACK	LOC
		SLOW ONLY	SLOW OR FAST			
0-3	1	**FE66**	**FE68**	-01	**FE10**	-31
4-7	2	**FE66**	**FE68**	-03	**FE10**	-33
8-11	3	**FE66**	**FE68**	-05	**FE10**	-35
12-15	4	**FE66**	**FE68**	-07	**FE10**	-37
16-19	5	**FE66**	**FE68**	-09	**FE10**	-39
20-23	6	**FE66**	**FE68**	-11	**FE10**	-41
24-25	7	**FE67**	**FE69**	-13	**FE9**	-43

ANALYZE D-LEVEL INTERRUPT, CALL STORES



ANALYZE D-LEVEL INTERRUPT, CALL STORES

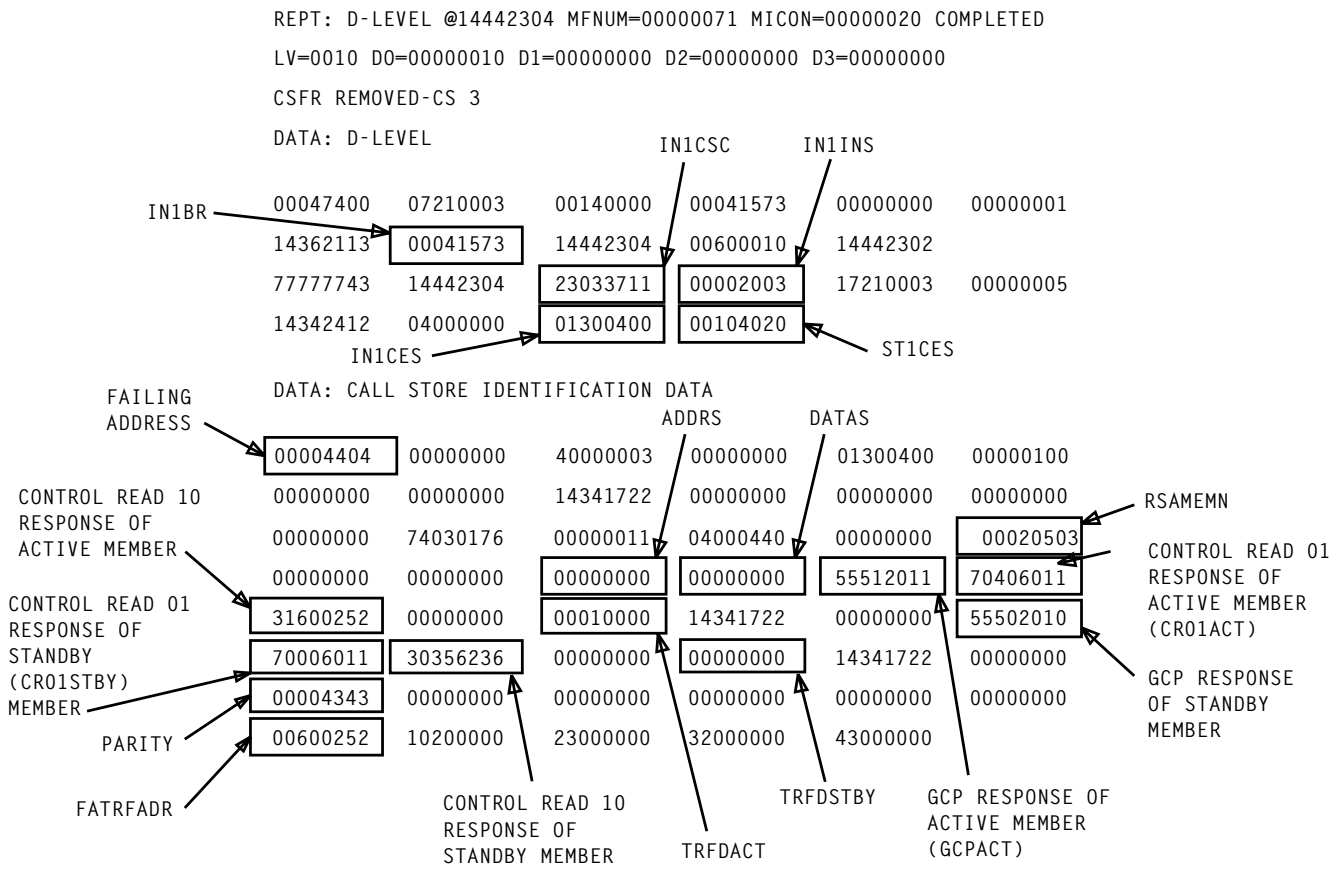
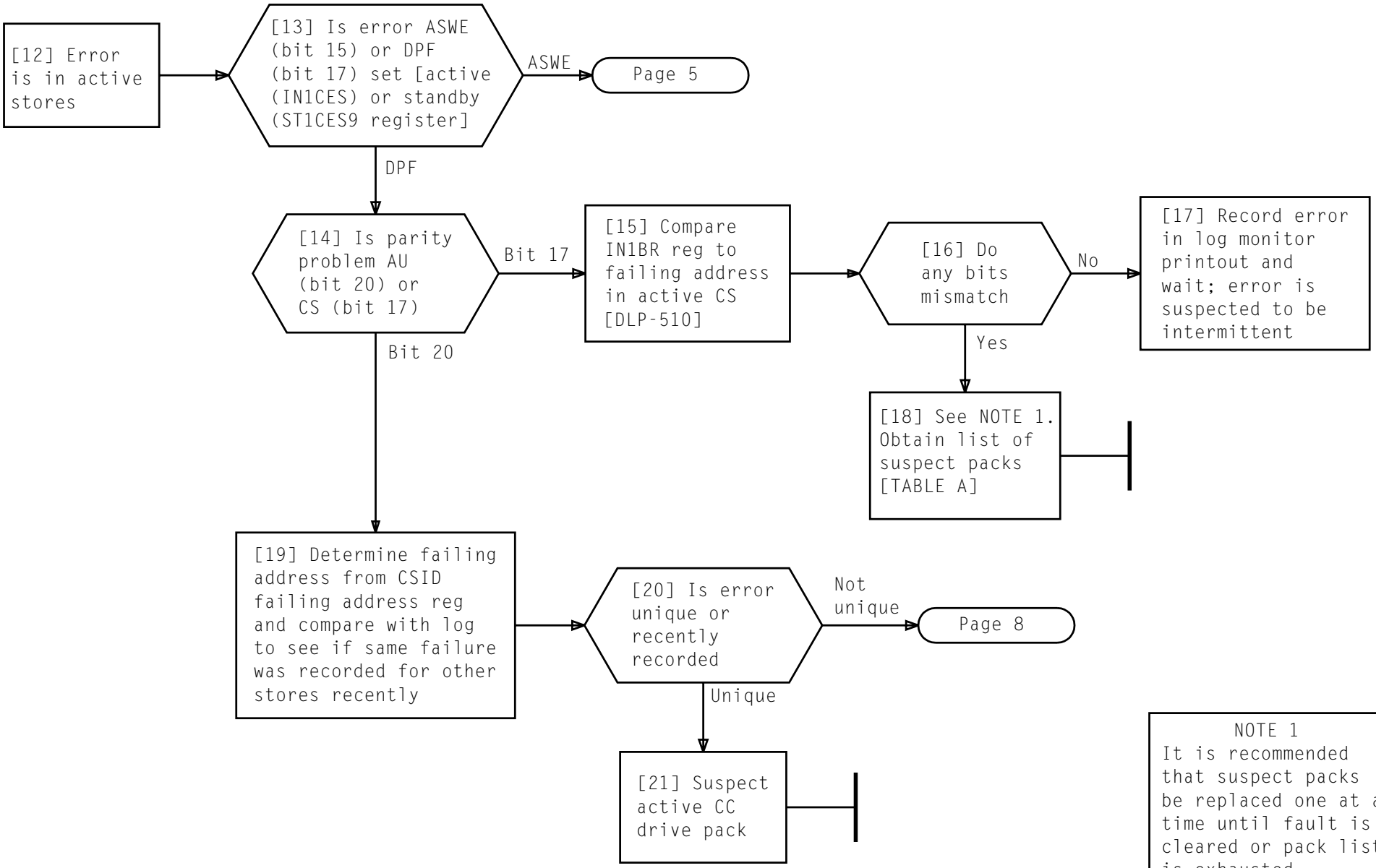


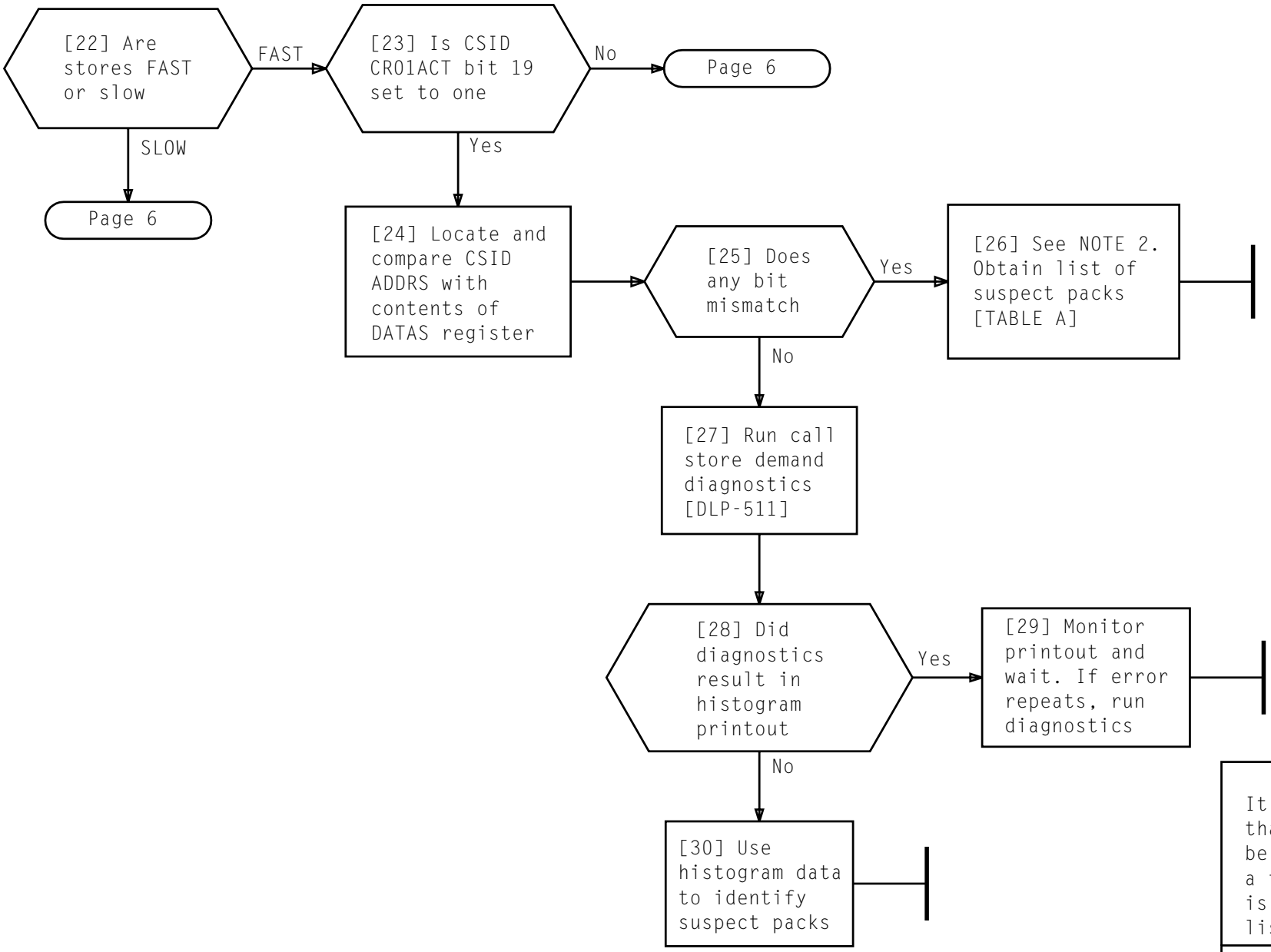
FIG. 1 – D-Level Interrupt Printout

ANALYZE D-LEVEL INTERRUPT, CALL STORES



NOTE 1
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE D-LEVEL INTERRUPT, CALL STORES



NOTE 2
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE D-LEVEL INTERRUPT, CALL STORES

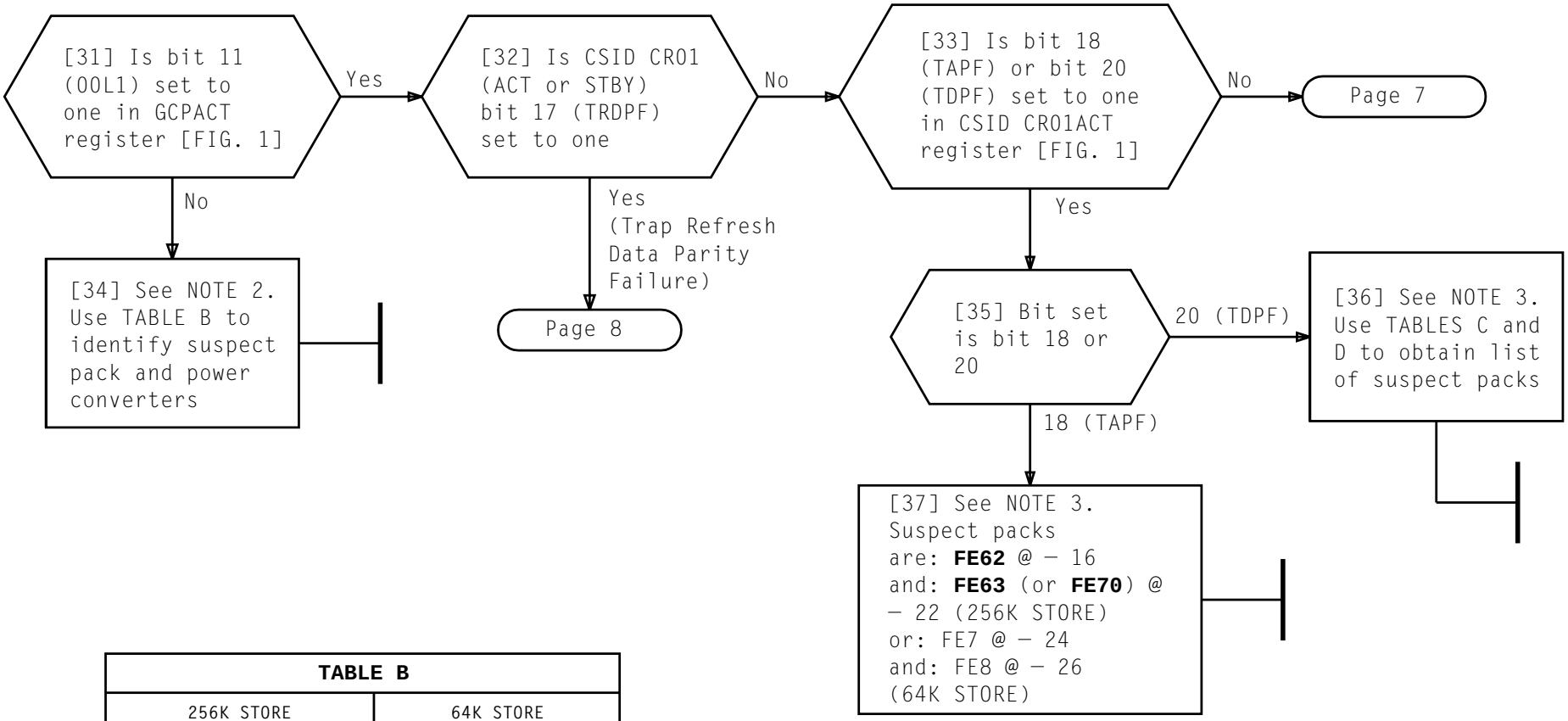


TABLE B

256K STORE		64K STORE	
CKT PACK	HORIZONTAL LOCATION	CKT PACK	LOCATION
FE71	-24	**FE6**	-20
		FE7	-22
PWR UNIT		**POWER UNIT**	
136J	-26 thru -30	**136D**	-00 thru -06
136L	-26 thru -30	**136E**	-00 thru -06

NOTE 3
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE D-LEVEL INTERRUPT, CALL STORES

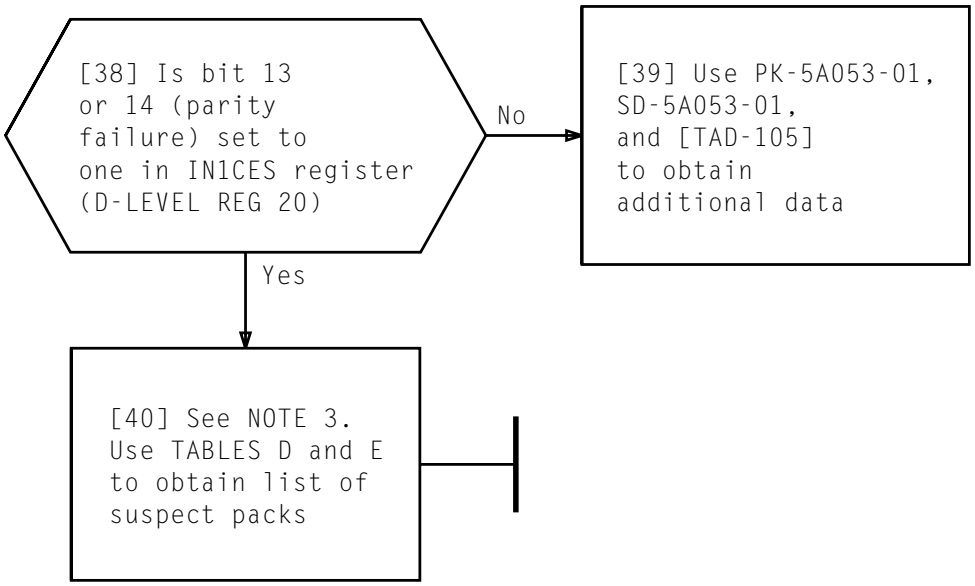


TABLE C

256K STORE		64K STORE	
CKT PACK	LOCATION	CKT PACK	LOCATION
FE65	–20	**FE3**	–24
FE63 (or **FE70**)	–22	**FE8**	–26

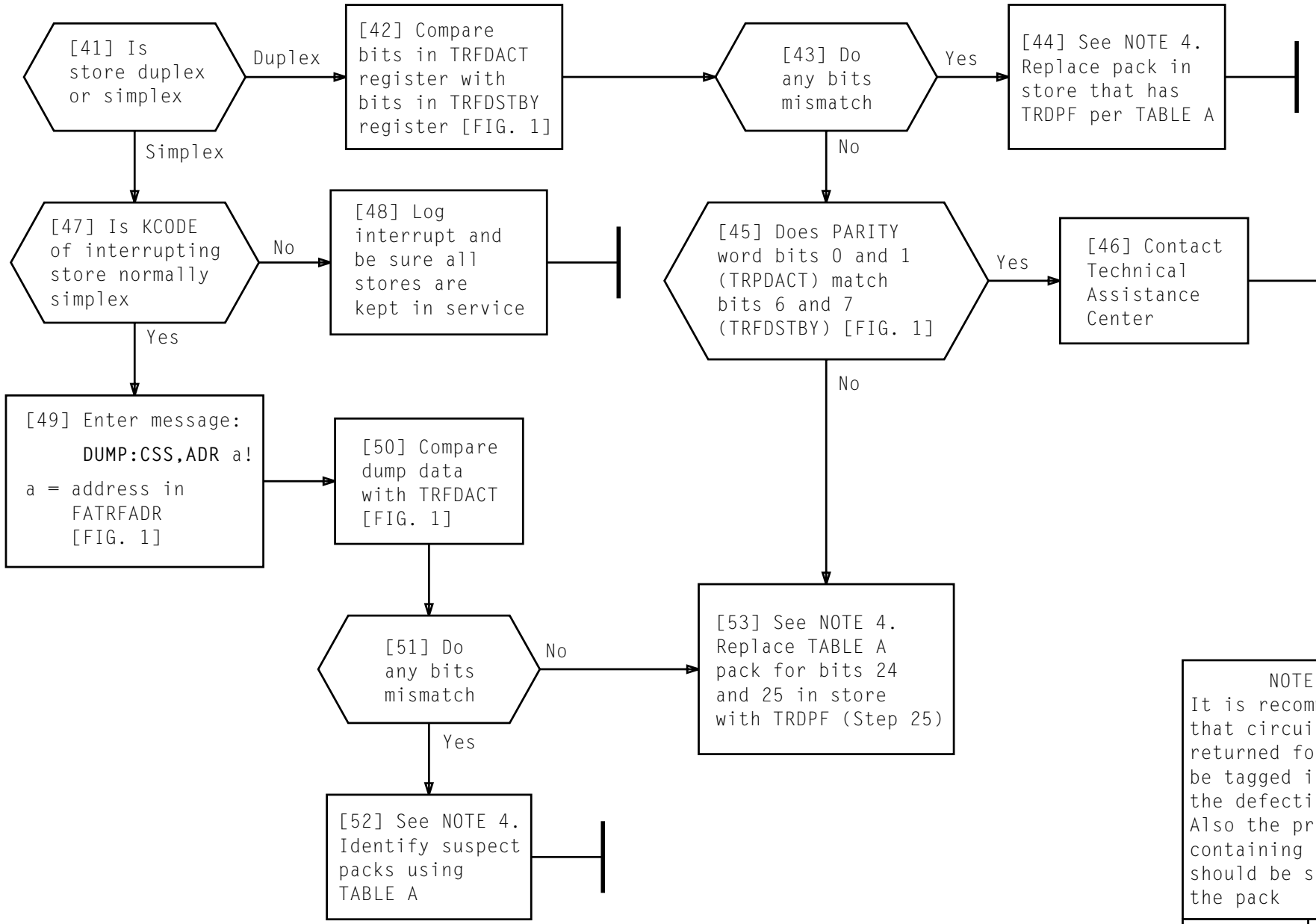
TABLE D

256K STORE			64K STORE		
CKT PACK	MEMORY PLANE	LOCATION	CKT PACK	MEMORY PLANE	LOCATION
FE67 **FE69**	7	–13	**FE9**	7	–43
All **FE66** or **FE68** packs in TABLE B			All **FE10** packs in TABLE A		

TABLE E

256K STORE		64K STORE	
LOGIC PACK	LOCATION	LOGIC PACK	LOCATION
FE62	–16	**FE7**	–28
FE64	–18	**FE5**	–22
FE65	–20	**FE6**	–20
FE63	–22	**FE3**	–24
		FE8	–26

ANALYZE D-LEVEL INTERRUPT, CALL STORES



NOTE 4
It is recommended that circuit packs returned for repair be tagged identifying the defective bit. Also the printout containing the error should be sent with the pack

ANALYZE D-LEVEL INTERRUPT, CALL STORES

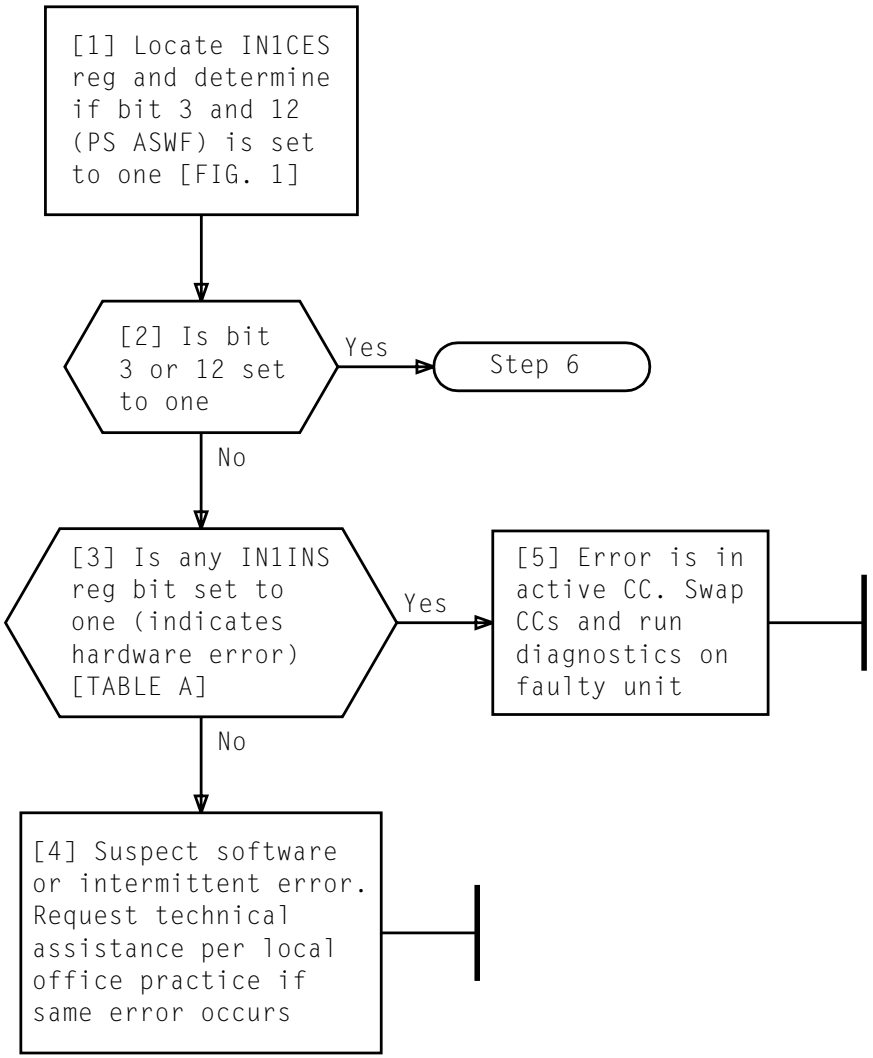
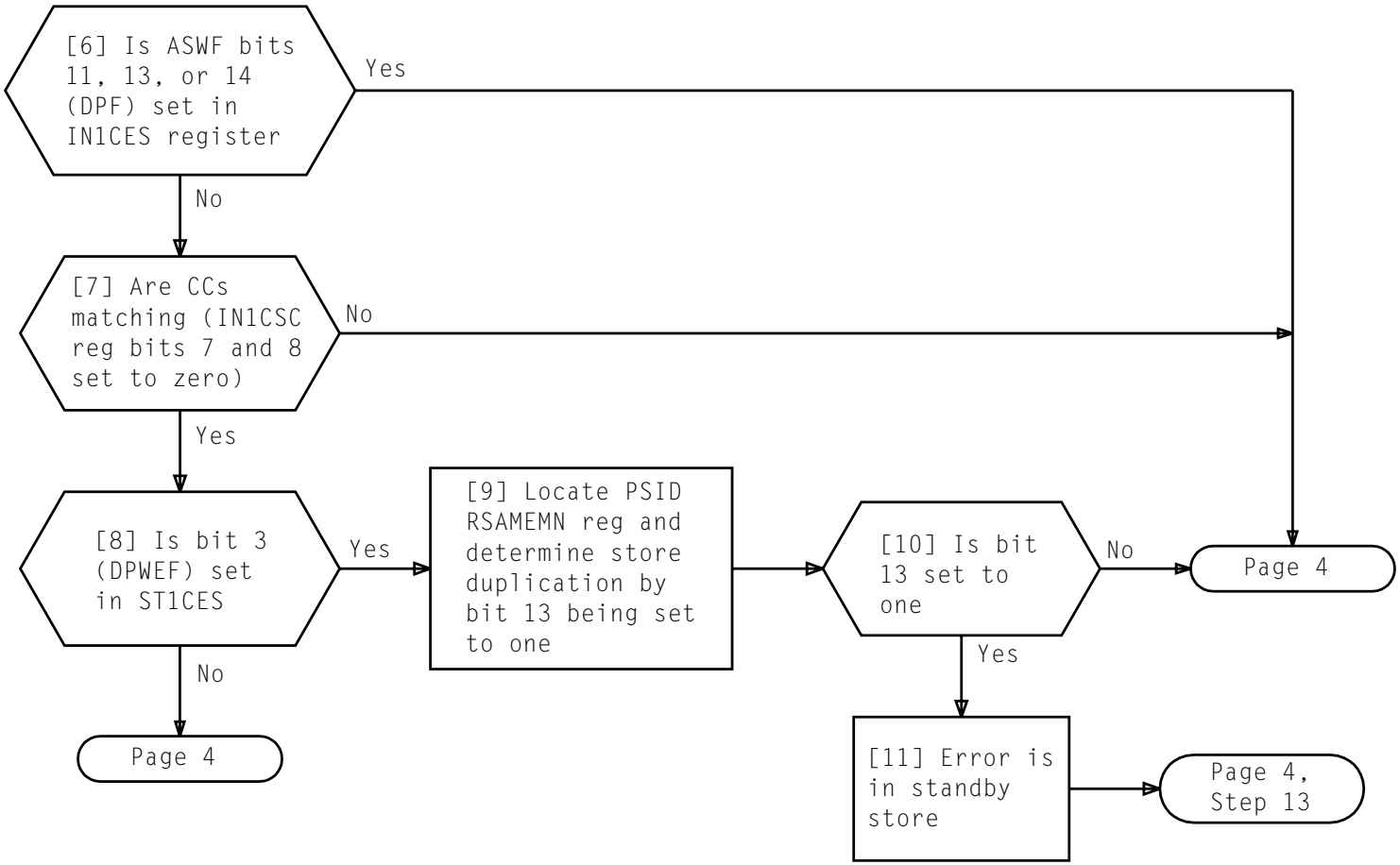


TABLE A

256K STORE					64K STORE	
BITS	MEMORY PLANE	SUSPECT PACK		LOC	SUSPECT PACK	LOC
		SLOW ONLY	SLOW OR FAST			
0-3	1	**FE66**	**FE68**	-01	**FE10**	-31
4-7	2	**FE66**	**FE68**	-03	**FE10**	-33
8-11	3	**FE66**	**FE68**	-05	**FE10**	-35
12-15	4	**FE66**	**FE68**	-07	**FE10**	-37
16-19	5	**FE66**	**FE68**	-09	**FE10**	-39
20-23	6	**FE66**	**FE68**	-11	**FE10**	-41
24-25	7	**FE67**	**FE69**	-13	**FE9**	-43

ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES



ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES

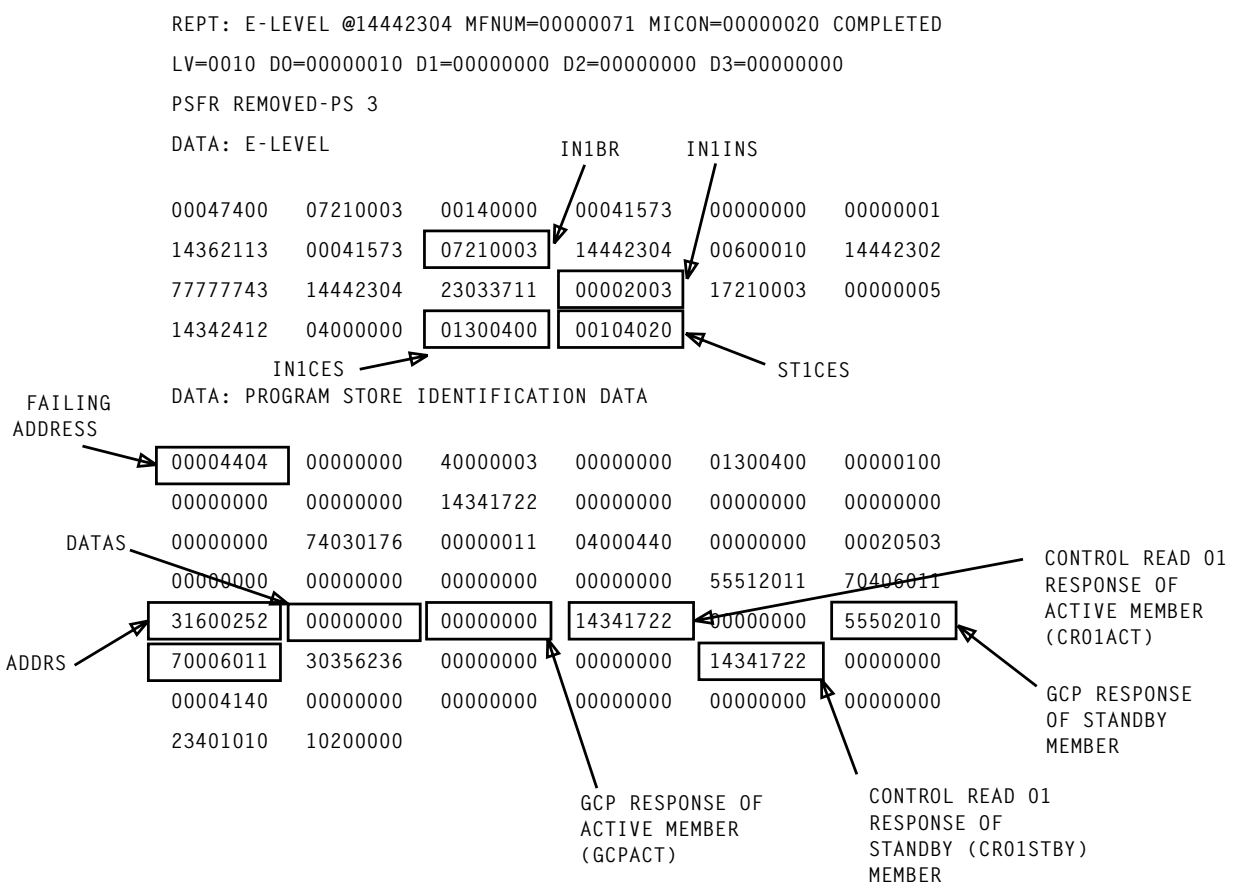
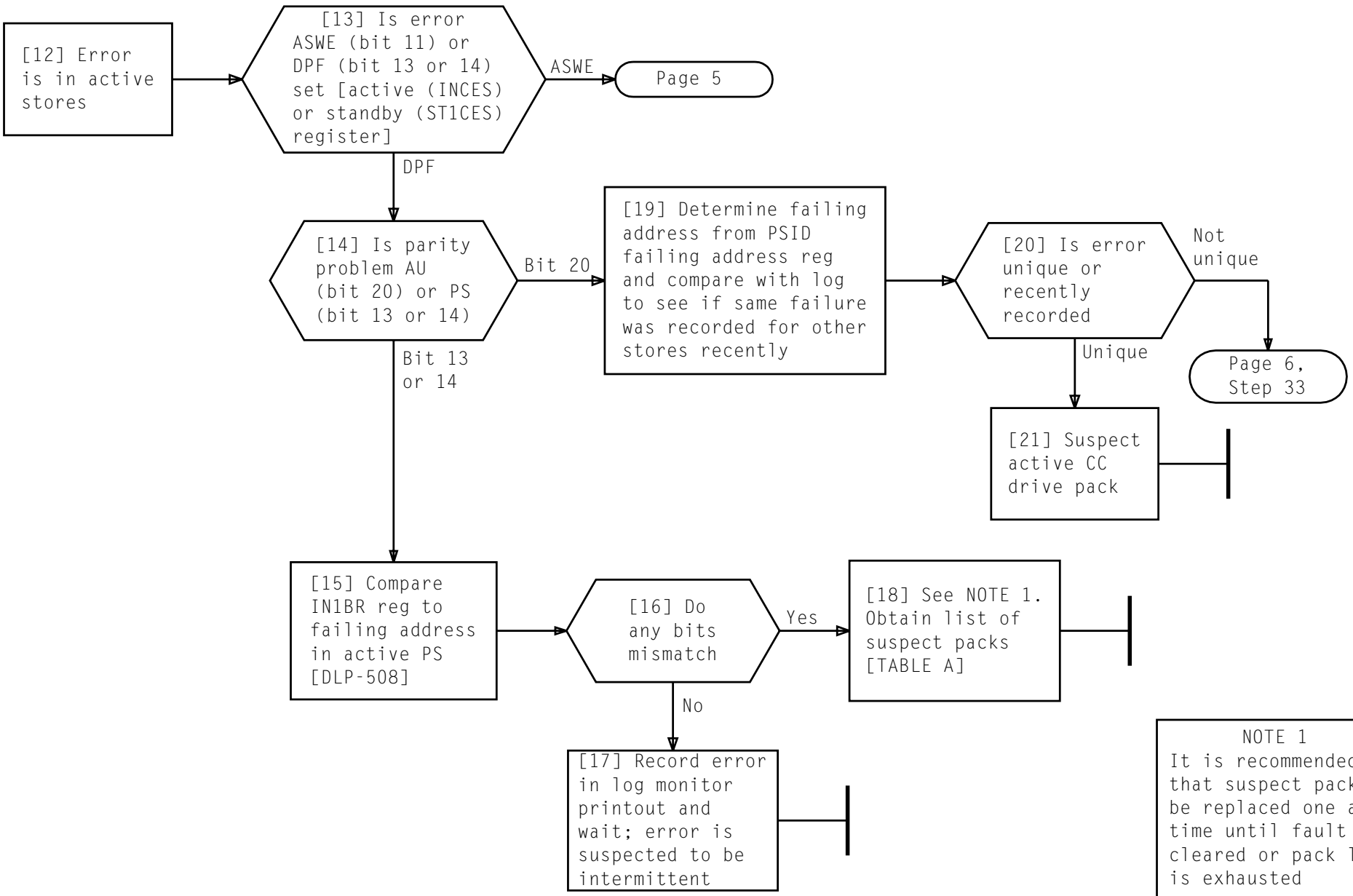
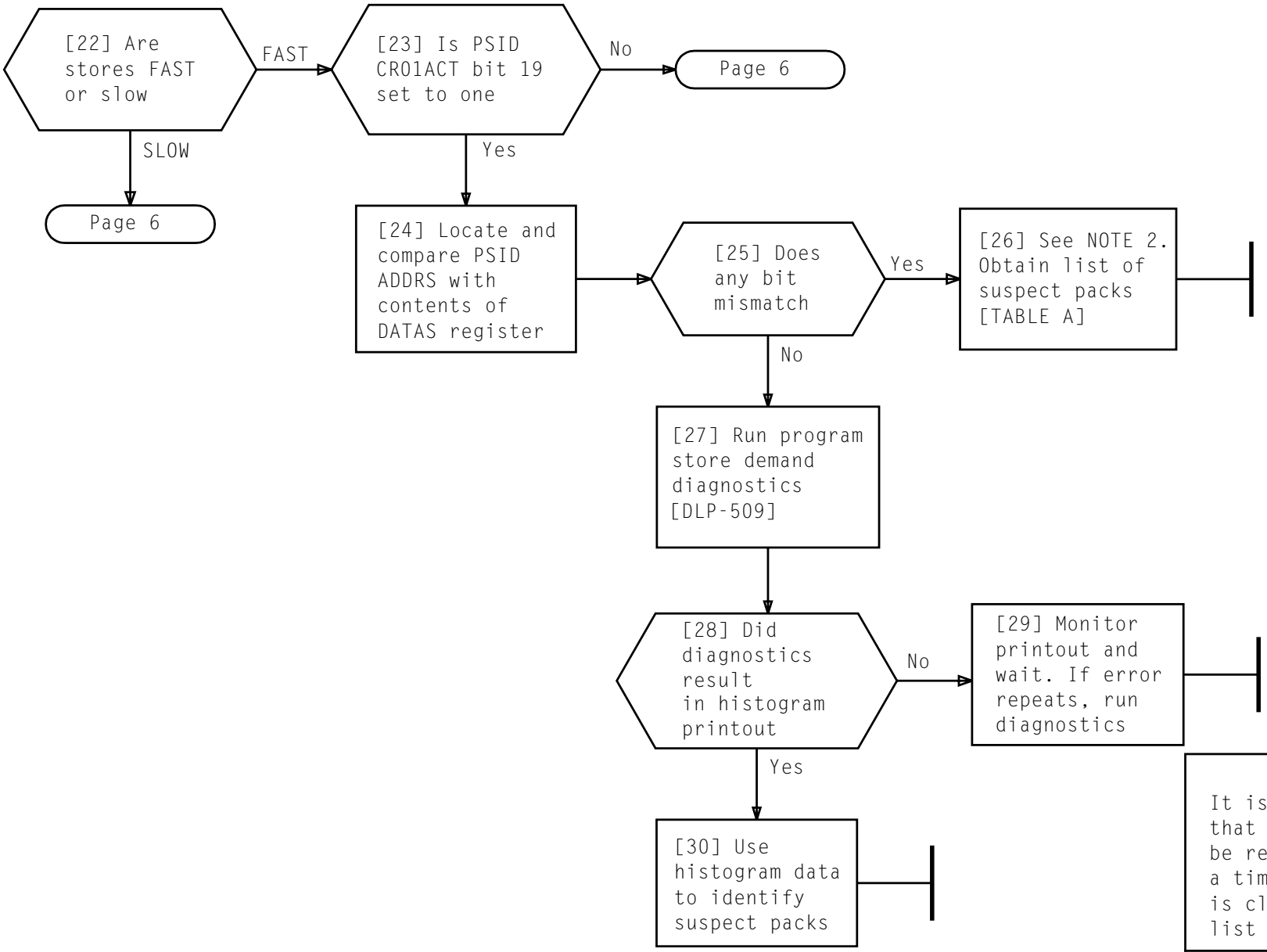


FIG. 1 — E-Level Interrupt Printout



NOTE 1
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES



NOTE 2
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES

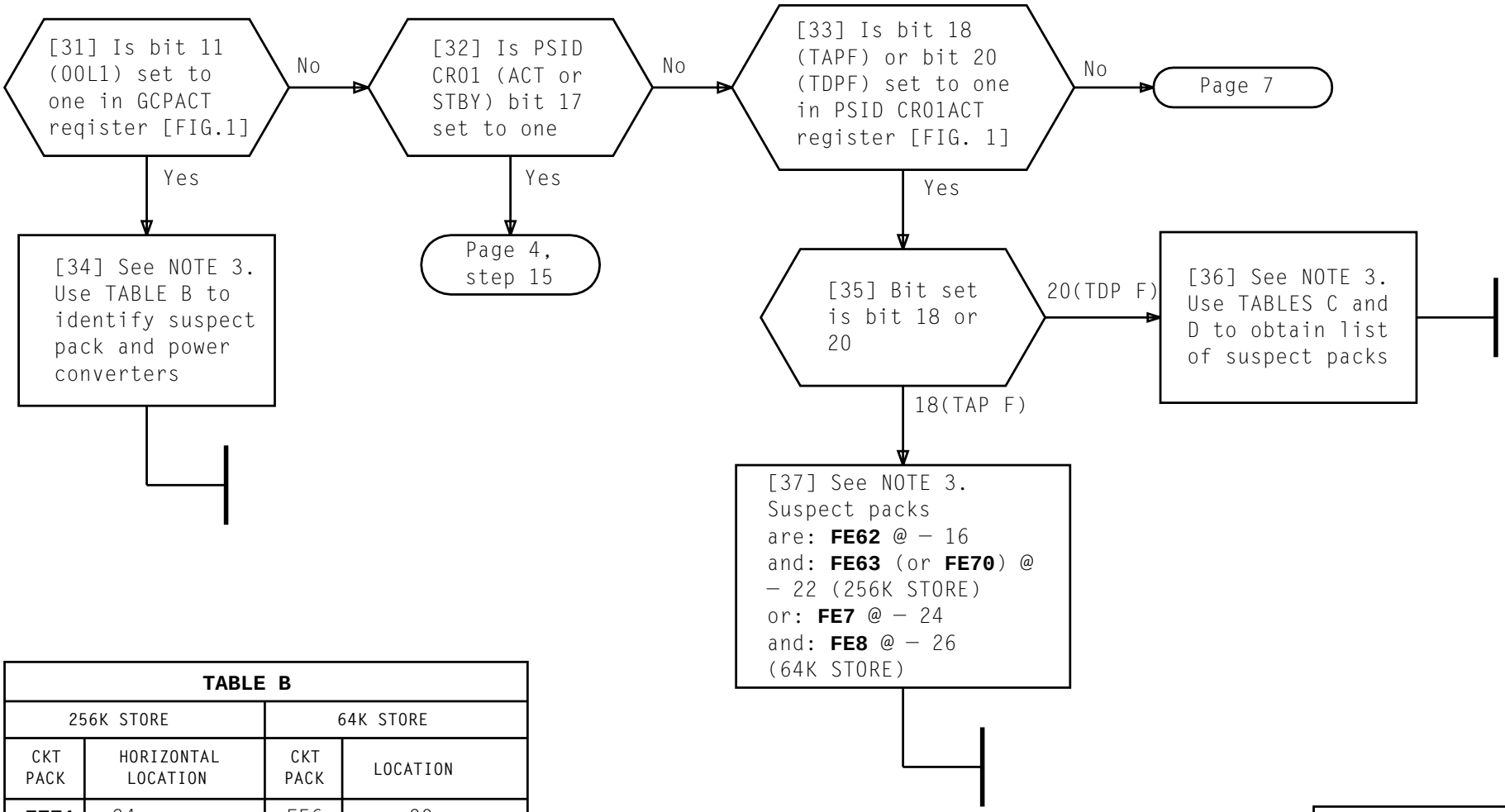


TABLE B

256K STORE		64K STORE	
CKT PACK	HORIZONTAL LOCATION	CKT PACK	LOCATION
FE71	-24	FE6 FE7	-20 -22
PWR UNIT		**POWER UNIT**	
136J 136L	-26 thru -30 -26 thru -30	136D 136E	-00 thru -06 -00 thru -06

NOTE 3
It is recommended that suspect packs be replaced one at a time until fault is cleared or pack list is exhausted

ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES

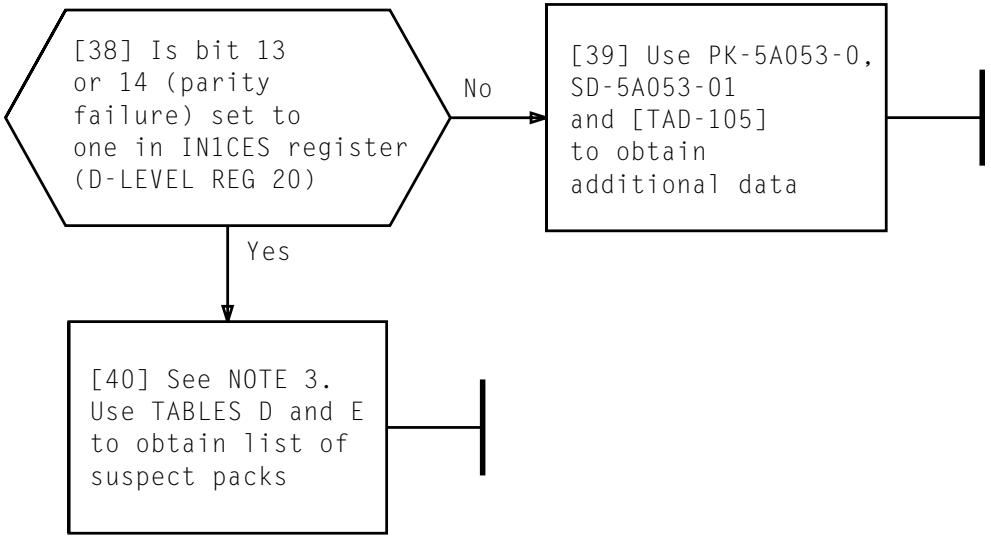


TABLE C			
256K STORE		64K STORE	
CKT PACK	LOCATION	CKT PACK	LOCATION
FE65	–20	**FE3**	–24
FE63 (or FE70)	–22	**FE8**	–26

TABLE D					
256K STORE			64K STORE		
CKT PACK	MEMORY PLANE	LOCATION	CKT PACK	MEMORY PLANE	LOCATION
FE67 FE69	7	–13	**FE9**	7	–43
All **FE66** or **FE68** packs in TABLE B			All **FE10** packs in TABLE A		

TABLE E			
256K STORE		64K STORE	
LOGIC PACK	LOCATION	LOGIC PACK	LOCATION
FE62	–16	**FE7**	–28
FE64	–18	**FE5**	–22
FE65	–20	**FE6**	–20
FE63	–22	**FE3**	–24
		FE8	–26

ANALYZE E-LEVEL INTERRUPT, PROGRAM STORES

[1] Using FIG. 1, obtain Point of Maximized Definition (PMD) from **FAULT RECOGNITION ISOLATION DATA** word 2 (rightmost three octal digits)

[2] Access PMD dictionary to obtain description of software actions and analysis of this error [DLP-515]

AND

[3] Was Error Analysis (ERAT) resolution used (from header)

Yes

[4] A nonunique error has occurred. Mate unit may be at fault

No

[5] Unique error has occurred. Unit identified in test printout is suspected faulty

[6] Is CREG 2 [FIG. 2] bit position 0 set to

1 (ASW) failure

Page 5

0 (Autonomous Interrupt [AINT] occurred)

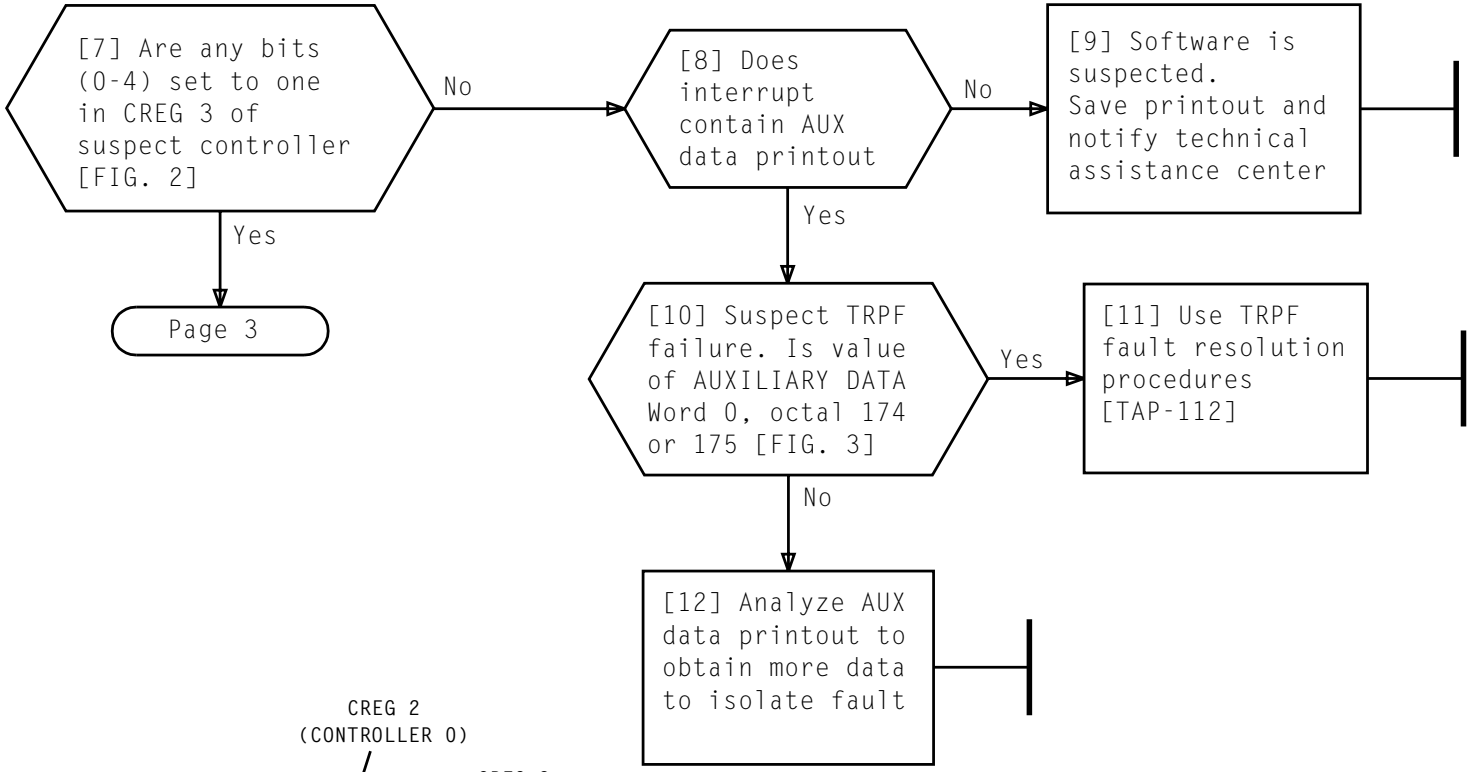
Page 2

PMD NUMBER

```
A 39 REPT: F-LEVEL 014764301 MFNUM=00004303 MICON=00000020  MSG COMPL
     LV=0040 D0=00000000 D1=04000000 D2=00000017 D3=00000000
     DATA: PERIPHERAL SYSTEM DATA
     03020102 00000000 00000001 00000000 00000000 00000104
     00000112 00000004 00000012 03600001 03600001 03600001
     03600001
     DATA: INTERRUPT SOURCE DATA
     00002400 14130667 03552000 00000020 00002000
     DATA: FAULT RECOGNITION ISOLATION DATA
     00000020 00002000 00000237 00000000 00000003 00000000
     DATA: ERROR ANALYSIS STRATEGY DATA
     01664210 00000001 00000001 00000001 00000001 00000000
     00000001
     04/29/83 11:38:49
     #822
```

FIG. 1 - Part of TNFR Printout

ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT USING PMD



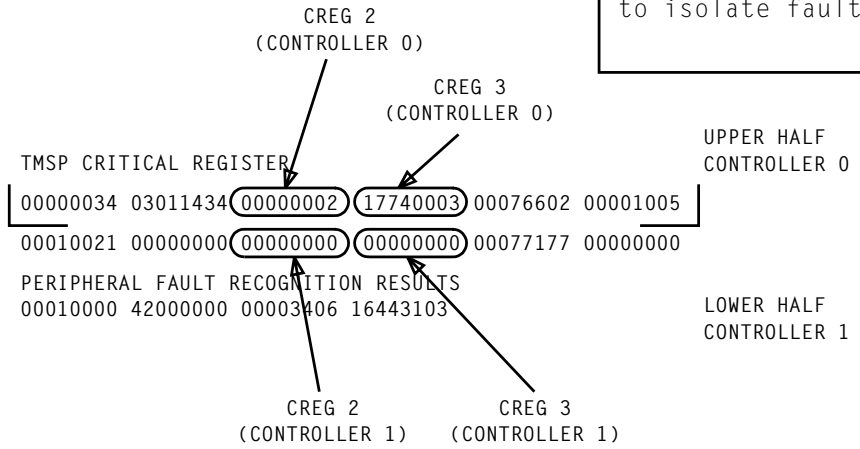


FIG. 2 — TMS Critical Registers

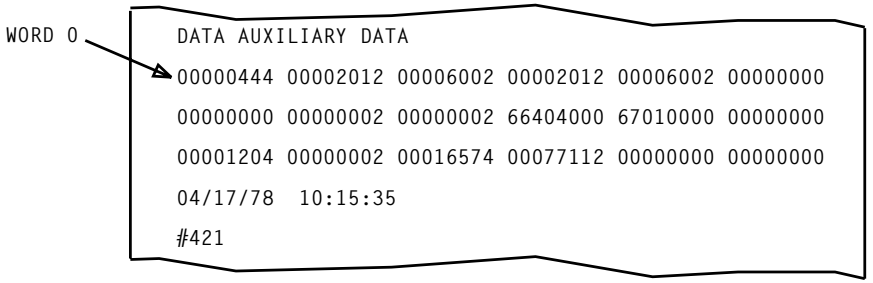


FIG. 3 — Auxiliary Data Registers

ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT USING PMD

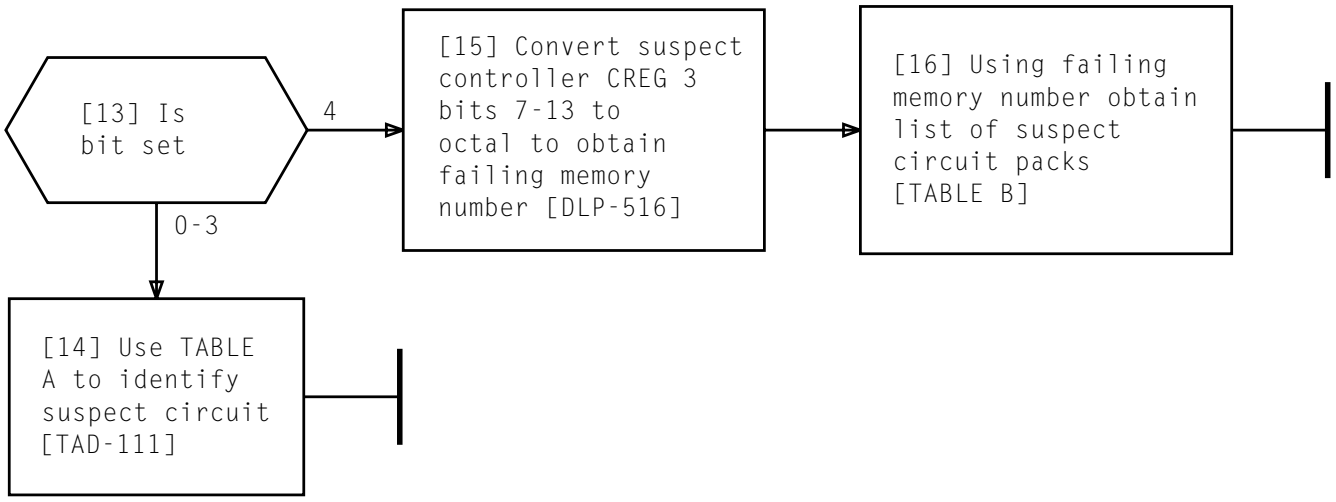


TABLE A
TMS–AINT, BITS 0–3

Significance of bit and reference to SD-4A026 for TMS-A and SD-4A088 for TMS-B appear below. Determine next step for error source bits set

ESR1 BIT	NAME	LEAD	FS/SYMBOL	IMPLICATION	SUSPECT PACKS	TMS-A	TMS-B
0	CE	ECE0	15/1	Internal clock error. Suspect clock circuit	FA527 FB225	072–21 072–22	(0,1)68–37
1	TSSC	ETSSC0	13/1	Time slot sequence. Check suspect time slot counter circuit	FA532	072–23	(0,1)68–39
2	TSCMM	ETSMM0	14/1	Time slot counter mismatch. Suspect time slot counter, match circuit, or mate controller	FA532 FA527 MATE CONTR	072–23 072–21 –	(0,1)68–39 (0,1)68–37 –
3	CMM	DESB030	15/1	Clock mismatch. Suspect clock match circuit or mate controller	FA527 MATE CONTR	072–23	(0,1)68–37

ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT USING PMD

TABLE B — TMS MEMORY NUMBERS			
HORIZONTAL PACK LOCATION			
FAILING MEMORY NUMBER	TMS-A FA632 MEMORY PACK	TMS-A FA520 MEMORY REGISTER PACK	TMS-B FA1199 MEMORY PACK
0, 20, 40, 60, 100, 120, 140, 160,	−05	−09	−25
1, 21, 41, 61, 101, 121, 141, 161	−06		
2, 22, 42, 62, 102, 122, 142, 162	−07	−10	−27
3, 23, 43, 63, 103, 123, 143, 163	−08		
4, 24, 44, 64, 104, 124, 144, 164	−21	−17	−28
5, 25, 45, 65, 105, 125, 145, 165	−20		
6, 26, 46, 66, 106, 126, 146, 166	−19	−16	−30
7, 27, 47, 67, 107, 127, 147, 167	−18		
10, 30, 50, 70, 110, 130, 150, 170	−24	−28	−46
11, 31, 51, 71, 111, 131, 151, 171	−25		
12, 32, 52, 72, 112, 132, 152, 172	−26	−29	−44
13, 33, 53, 73, 113, 133, 153, 173	−27		
14, 34, 54, 74, 114, 134, 154, 174	−40	−36	−43
15, 35, 55, 75, 115, 135, 155, 175	−39		
16, 36, 56, 76, 116, 136, 156, 176	−38	−35	−41
17, 37, 57, 77, 117, 137, 157, 177	−37		
VERTICAL PACK LOCATION			
0 Through 17	Bay 0, Vertical 36		*24
20 Through 37	Bay 0, Vertical 44		*28
40 Through 57	Bay 0, Vertical 52		*36
60 Through 77	Bay 0, Vertical 60		*40
100 Through 117	Bay 1, Vertical 36		*48
120 Through 137	Bay 1, Vertical 44		*52
140 Through 157	Bay 1, Vertical 52		*60
160 Through 177	Bay 1, Vertical 60		*64
* = Controller 0 or 1			

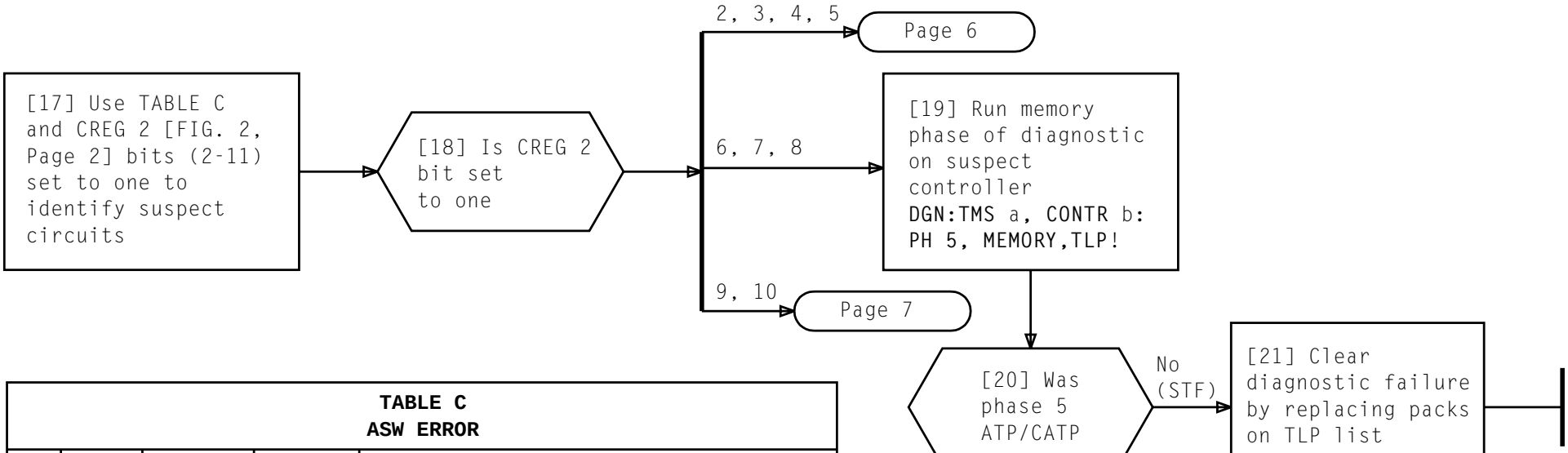
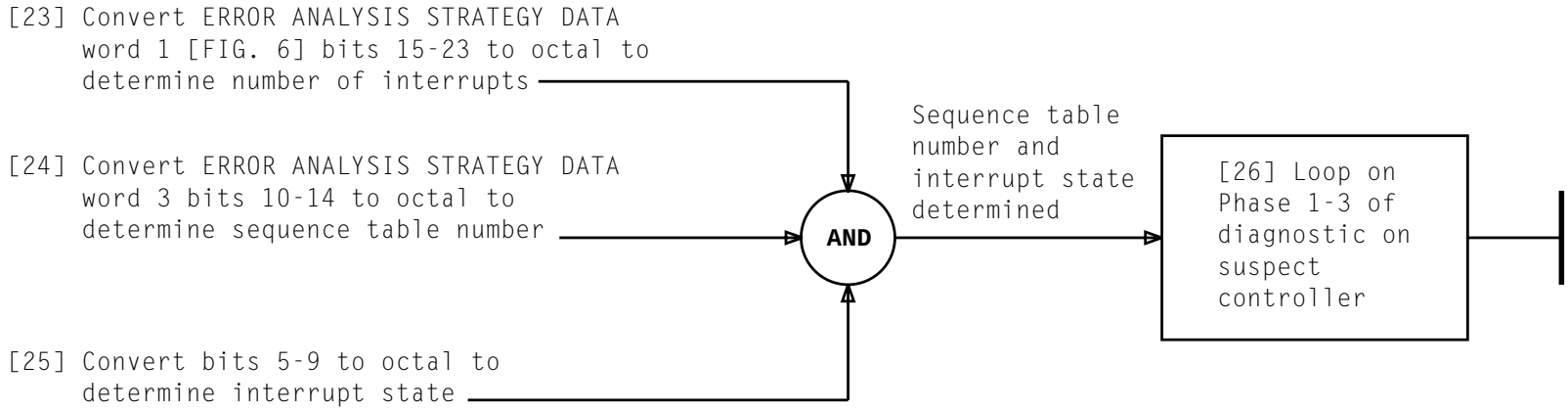


TABLE C
ASW ERROR

ESR1 BIT	NAME	LEAD	FS/SYMBOL	IMPLICATION
0	ASRF	EASRM0	16/11	All seems well failure summary
1	AINT	—	—	Autonomous interrupt failure summary
2	PFE	EPFE0	3/3	Bus parity failure — even bits
3	PFO	EPFB0	3/1	Bus parity failure — odd bits
4	MODE	EMB00	16/10	Mode failure
5	SEQCK	ESEQCK0	16/11	Suspect output decoder problem in controller
6	MAF	EMAF0	16/9	Suspect a memory problem
7	TSPF	EMPFB0	12/5	Suspect a memory problem
8	AUDIT	EAU00	16/6	Suspect software or a memory problem
9	TSAMM	ETSMM0	14/1	Mismatch error
10	MTMM	EMSH0	10/1	Mismatch error
11	ABORT	EABORT0	16/11	

ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT USING PMD



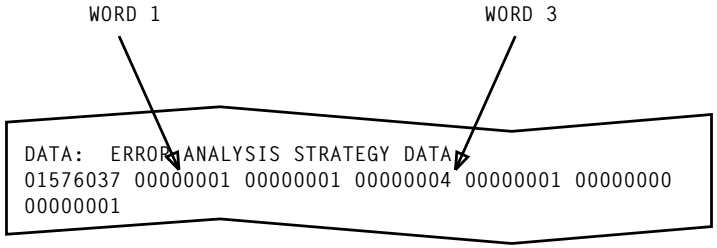
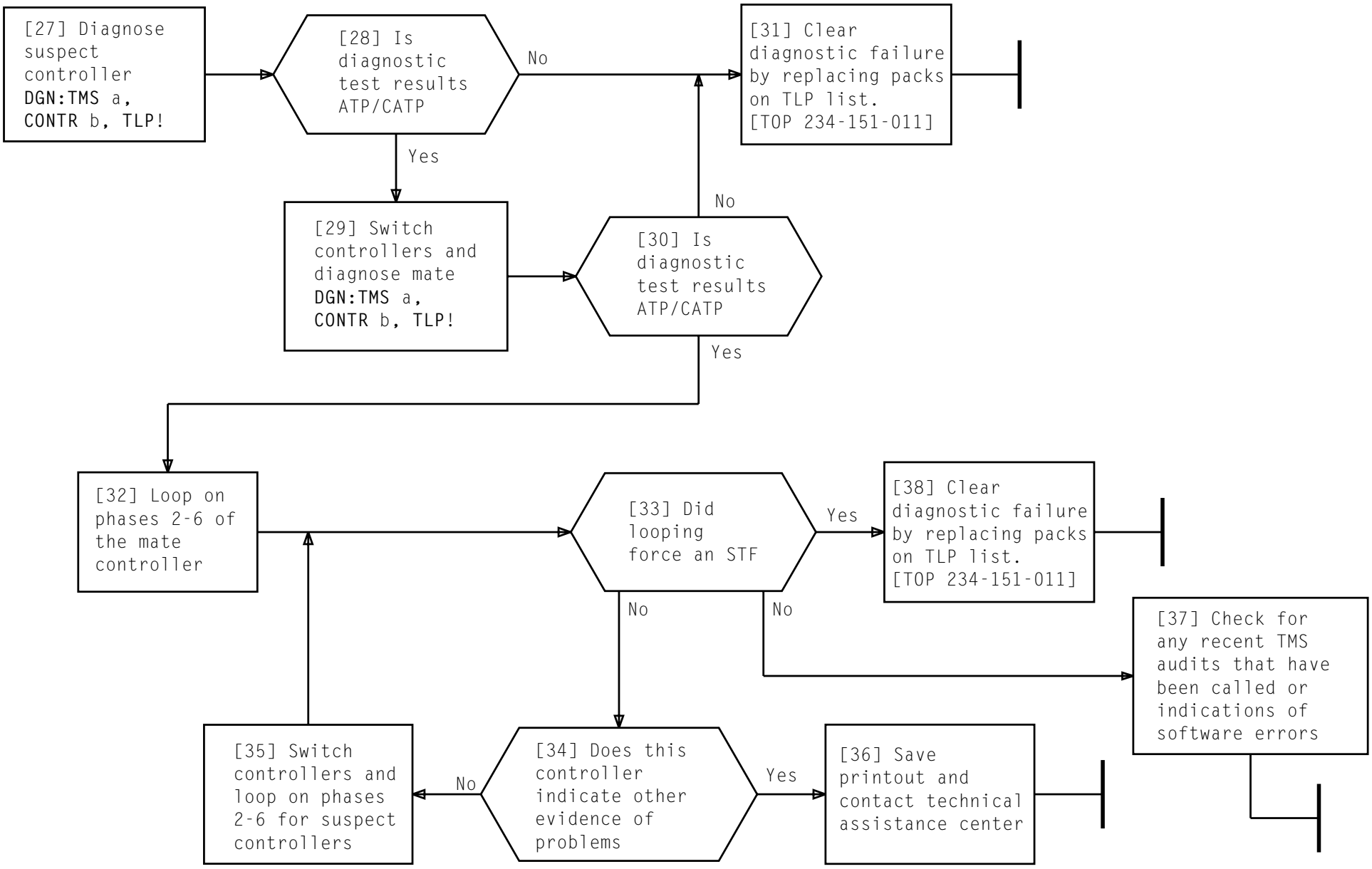
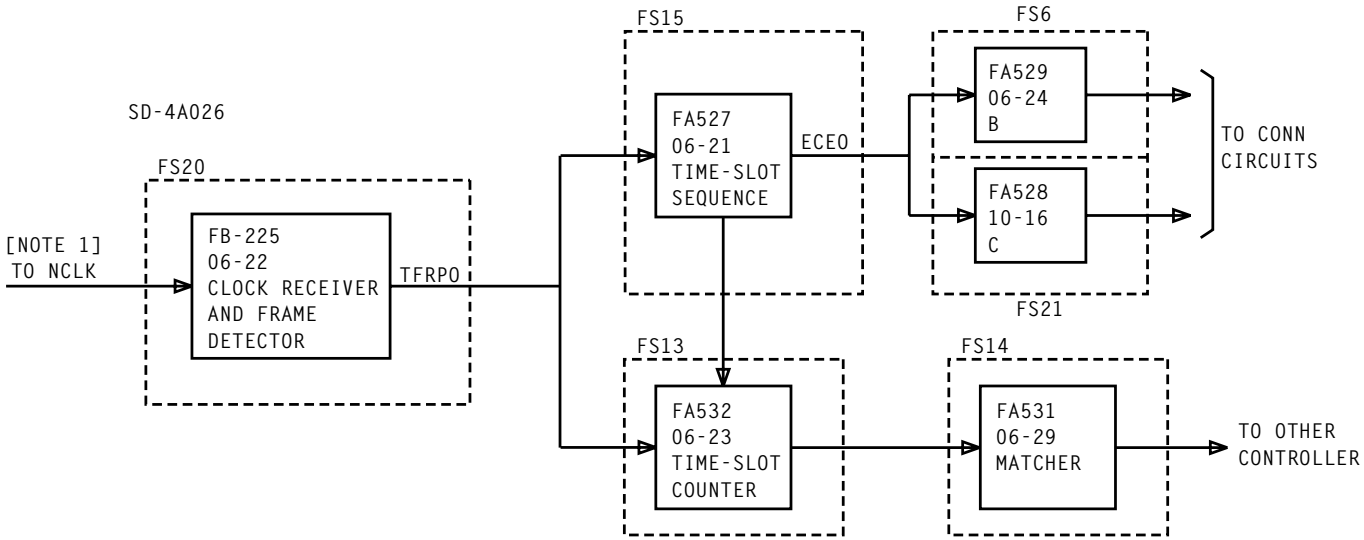


FIG. 6 - Error Analysis Strategy Data



ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT USING PMD

A simplified block diagram for AINT bits 0-3 in CREG 3 register is provided as an aid for trouble isolation of clock problems in the TMS frame



NOTE 1
Verify NCLK frame is providing good clock before checking packs

AUTONOMOUS INTERRUPT (AINT) CLOCK BITS 0-3, TIME MULTIPLEXED SWITCHING

At TCC terminal:

[1] Type:

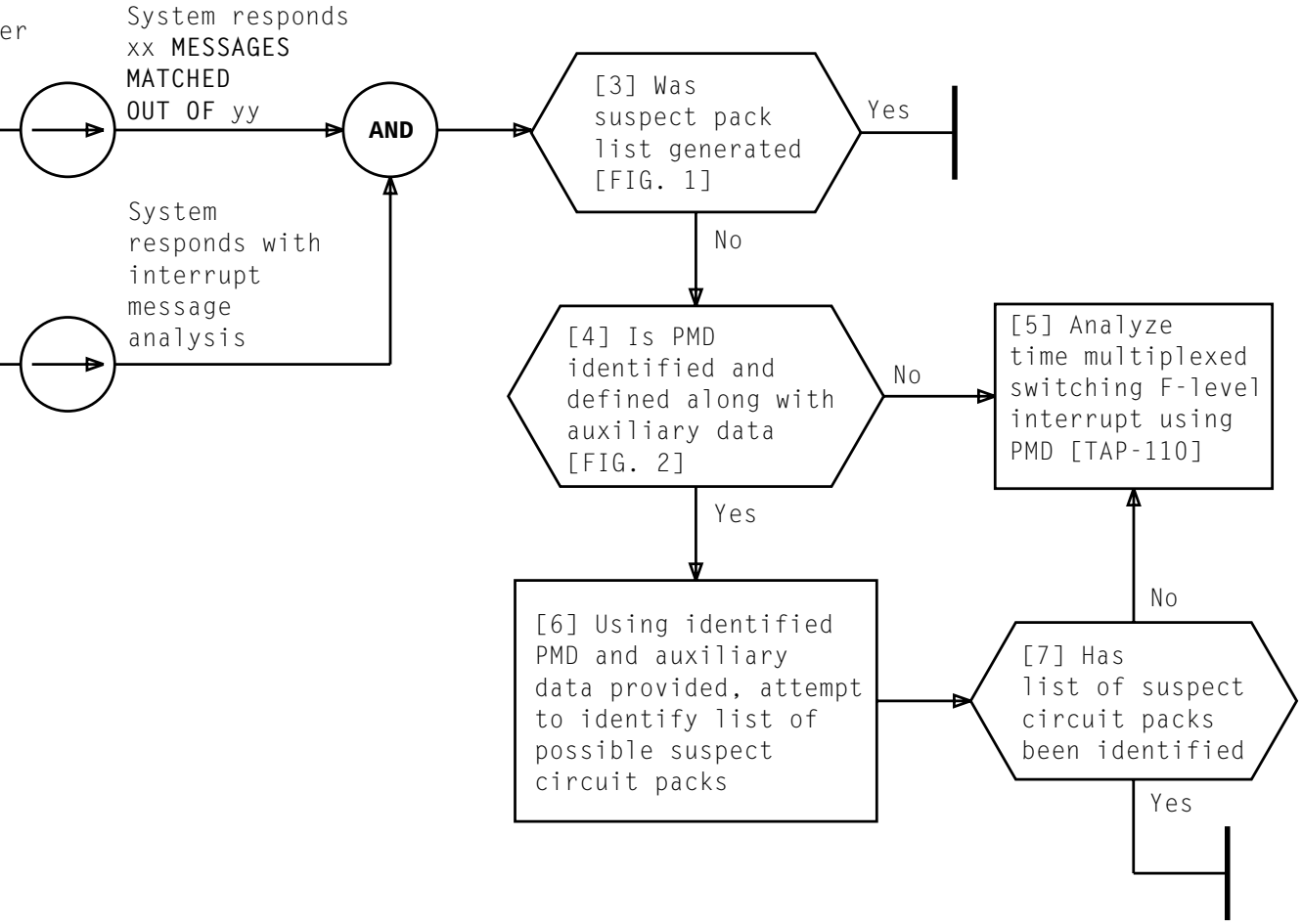
F: a;PAT b, {FROM c, TO d,} RDT e!

a = office code
b = desired interrupt pattern
c = month, day, and time filter is to begin
d = month, day, and time filter is to end
e = file name interrupt data is to be directed to

[2] Type:

ANAL:TRPF;CHANNEL a;RDT b!

a = office code
b = file name interrupt data was directed to



ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT

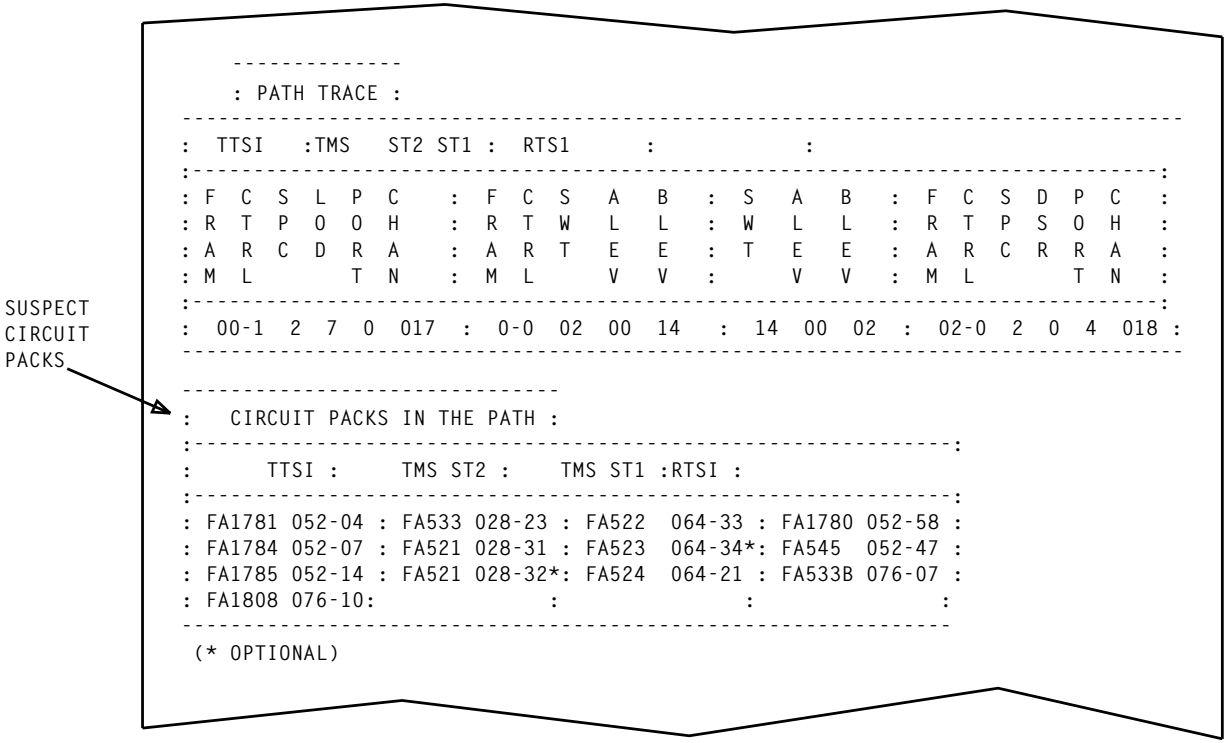


FIG. 1 - Sample Interrupt Message Analysis (Partial)

ANALYZE TIME MULTIPLEXED SWITCHING F-LEVEL INTERRUPT

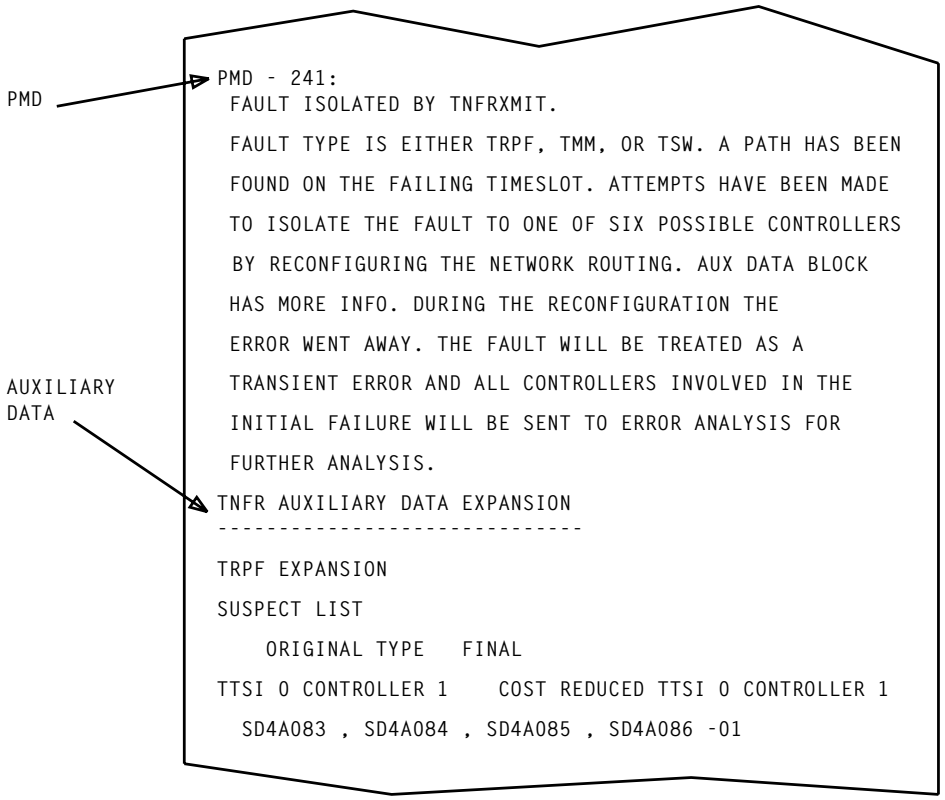
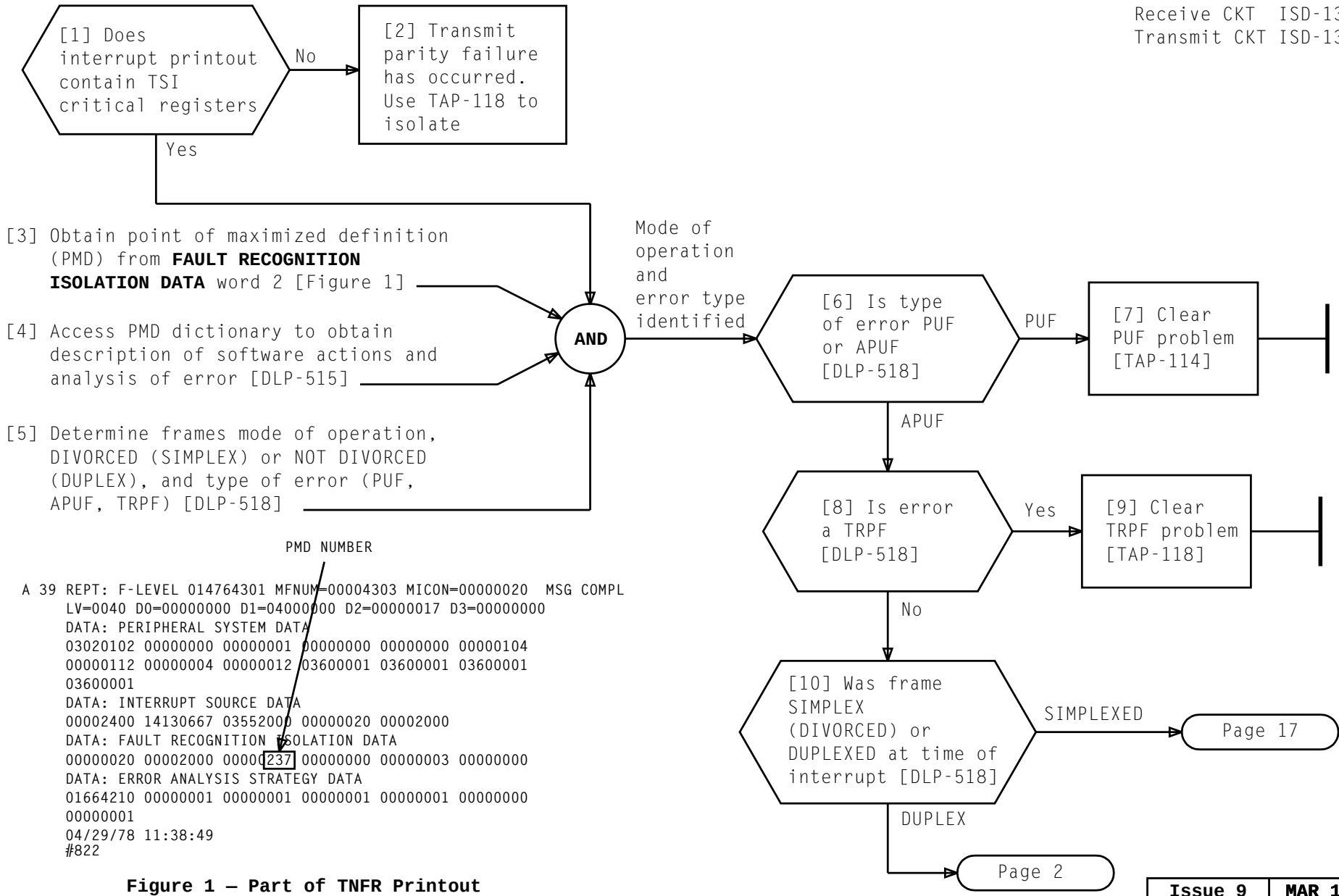


FIG. 2 - Sample Interrupt Message Analysis (Partial)

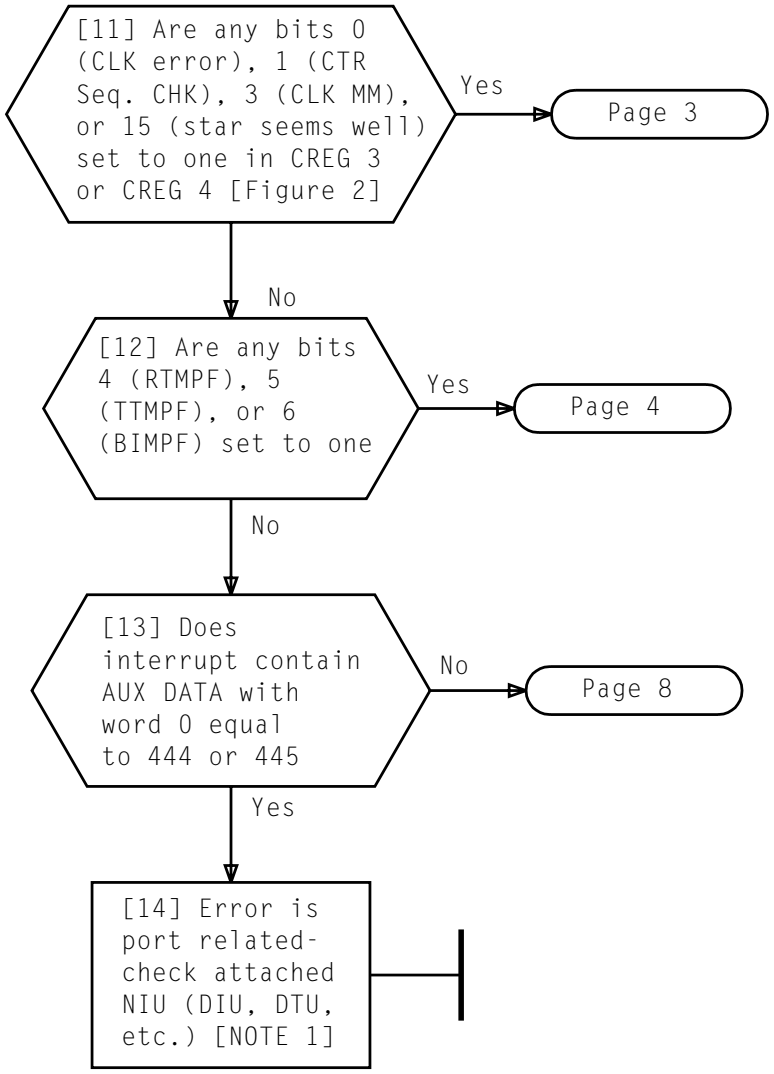


PMD NUMBER

```
A 39 REPT: F-LEVEL 014764301 MFNUM=00004303 MICON=00000020  MSG COMPL
     LV=0040 D0=00000000 D1=04000000 D2=00000017 D3=00000000
     DATA: PERIPHERAL SYSTEM DATA
     03020102 00000000 00000001 00000000 00000000 00000104
     00000112 00000004 00000012 03600001 03600001 03600001
     03600001
     DATA: INTERRUPT SOURCE DATA
     00002400 14130667 03552000 00000020 00002000
     DATA: FAULT RECOGNITION ISOLATION DATA
     00000020 00002000 00000237 00000000 00000003 00000000
     DATA: ERROR ANALYSIS STRATEGY DATA
     01664210 00000001 00000001 00000001 00000001 00000000
     00000001
     04/29/78 11:38:49
     #822
```

Figure 1 – Part of TNFR Printout

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE



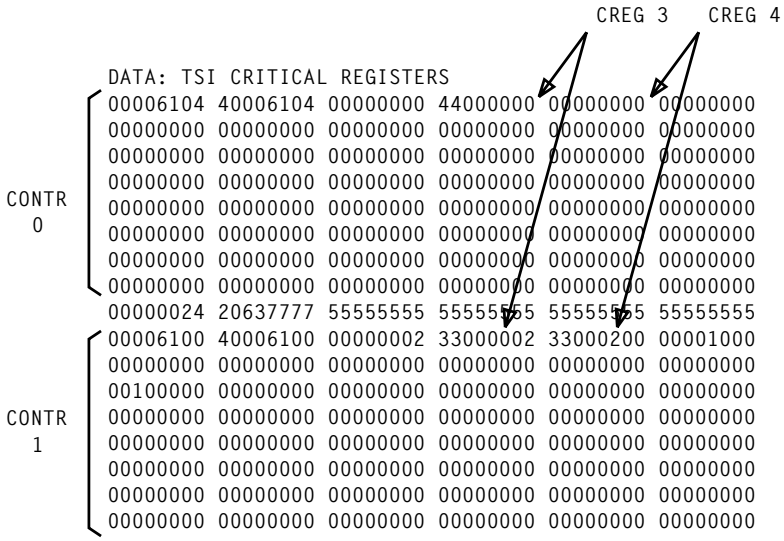


Figure 2 — TSI CREGs

NOTE 1
Table G can be used to determine port. Use CREG 22 and 23 (RSW). If zero look at CREG 12 and 13 (BMAPF).

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

[15] Use TABLE A to obtain suspect pack list for set bits 0, 1, 3, or 15, use [TAD-117] for general strategy, and use Figure 3 and Example 1 for frame type

TABLE A
CLOCK BITS

FRAME TYPE	SET BIT	PACK TYPE	LOCATION
TSI-A1 [SD-4A023-01]	0,1,3	FA562	56-36
		FB225	56-35
		FB224	56-37
		FA552	56-30
		FA553	56-33
		FA554	56-34
	15	FB220	56-39
		FB225	56-35
TSI-A2 [SD-4A023-02]	0,1,3	FA562	56-36
		FC463	56-35
		FA552	56-30
		FA553	56-33
		FA554	56-34
TSI-B [SD-4A083-01]	0,1,3	FA1798	72-29
		FA1233	72-31
		FA1234	72-30
		FC464	72-27

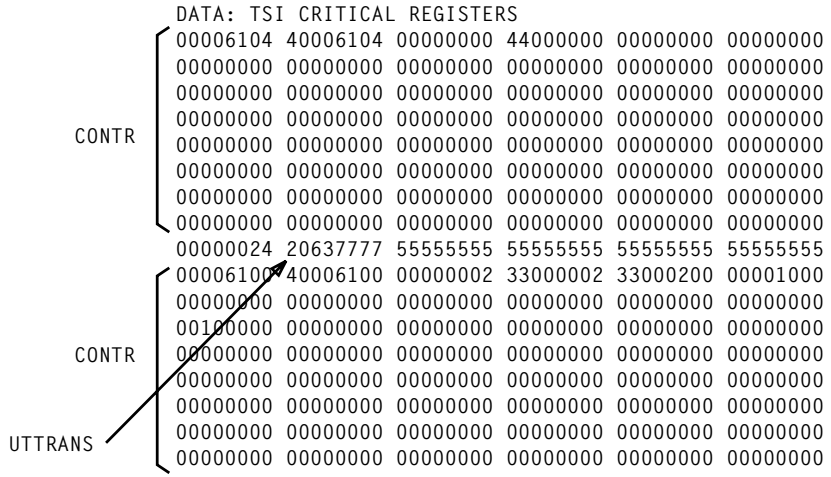
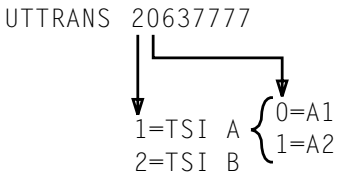


Figure 3 – TSI CREGs



EXAMPLE 1

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

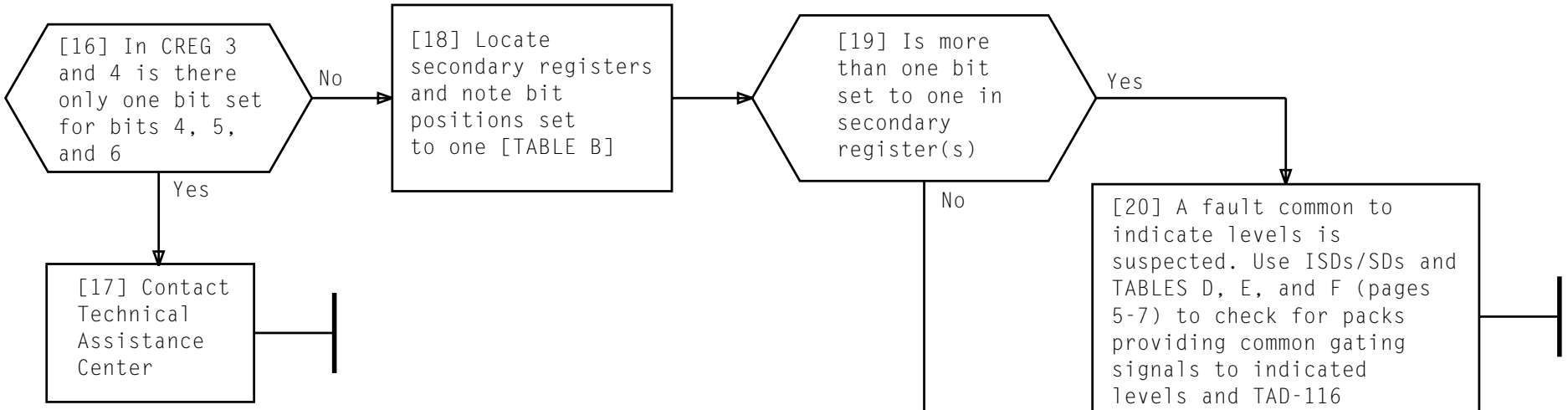


TABLE B
SECONDARY REGISTERS FOR SET ESR BIT

ASSOCIATED SECONDARY REGISTERS		
CREG 3, 4 ERROR SOURCE BIT	**ORIGINAL TSI FRAME (SD-4A011-01) OR NEAR TERM TSI FRAME (SD-4A011-02)**	**COST REDUCED TSI FRAME (SD-4A083-01)**
4(RTSMP)	CREG 6	CREG 6, CREG 7
5(TTSMP)	CREG 8	CREG 8, CREG 9
6(BIMPF)	CREG 10	CREG 10, CREG 11

TABLE C
SPC AND LEVEL

CREG	SPC								SPC							
6,8,10 7,9,11	1 3								0 2							
BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

TABLE D — SUSPECT PACK LIST FOR ESR BIT 4										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA632(B)	42-29	42-28	42-27	42-26	42-24	42-23	42-22	42-21
		FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
	TSI-A2 SD4A011-02	FA632B	42-29	42-28	42-27	42-26	42-24	42-23	42-22	42-21
		FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
	TSI-B SD4A083-01	FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
1	TSI-A1 SD4A011-01	FA632(B)	64-29	64-28	64-27	64-26	64-24	64-23	64-22	64-21
		FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
	TSI-A2 SD4A011-02	FA632B	64-29	64-28	64-27	64-26	64-24	64-23	64-22	64-21
		FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
	TSI-B SD4A083-01	FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
2	TSI-B SD4A083-01	FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC — all levels)										

TABLE E — SUSPECT PACK LIST FOR ESR BIT 5									
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA632(B)	42-44	42-43	42-42	42-41	42-39	42-38	42-37	42-36
		FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
	TSI-A2 SD4A011-02	FA632B	42-44	42-43	42-42	42-41	42-39	42-38	42-37	42-36
		FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
	TSI-B SD4A083-01	FA1781*	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
1	TSI-A1 SD4A011-01	FA632(B)	64-44	64-43	64-42	64-41	64-39	64-38	64-37	64-36
		FA541	68-44	68-43	68-42	68-41	68-40	68-39	68-38	68-37
	TSI-A2 SD4A011-02	FA632B	64-44	64-43	64-42	64-41	64-39	64-38	64-37	64-36
		FA541	68-44	68-43	68-42	68-41	68-40	68-39	68-38	68-37
	TSI-B SD4A083-01	FA1781*	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
2	TSI-B SD4A083-01	FA1781*	52-24	52-23	52-19	52-17	52-10	52-07	52-05	52-04
3	TSI-B SD4A083-01	FA1781*	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
* FA1781 or FA1817 (wide band option on SPC — all levels)										

TABLE F — SUSPECT PACK LIST FOR ESR BIT 6										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6*	7*
0 or 1	TSI-A1 SD4A011-01	FA633(B)	N/A	N/A	N/A	N/A	N/A	N/A	42-53	64-53
		FA556							42-52	64-52
		FA555							56-38	56-38
	TSI-A2 SD4A011-02	FA633B	N/A	N/A	N/A	N/A	N/A	N/A	42-53	64-53
		FA556							42-52	64-52
		FA555							56-38	56-38
0	TSI-B SD4A083-01	FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
1	TSI-B SD4A083-01	FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
2	TSI-B SD4A083-01	FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
3	TSI-B SD4A083-01	FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
* For TSI-A1 and TSI-A2 this column is bit 6 and 7 not level 6 and 7										

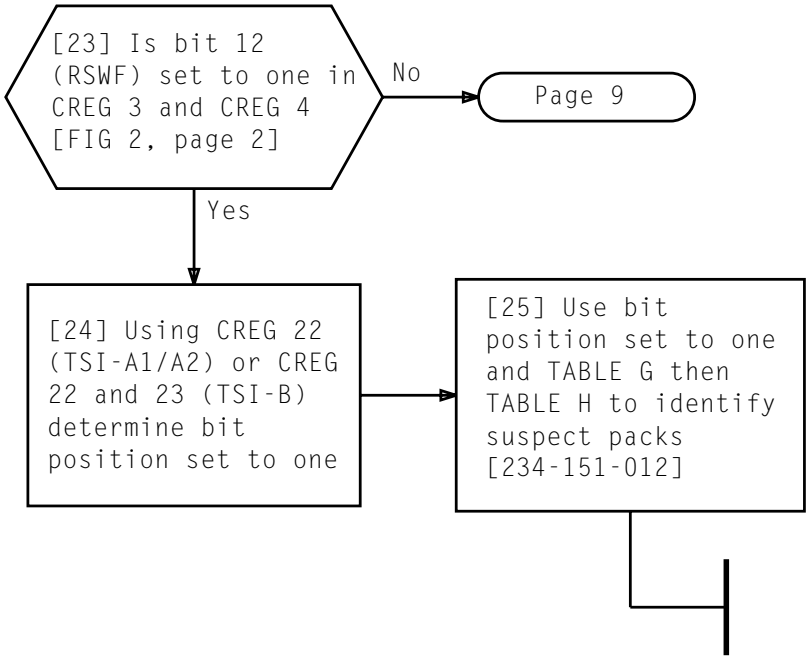


TABLE G
IDENTIFICATION OF SPC AND LEVEL

(EVEN NUMBERED SECONDARIES)																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
1								0								SPC

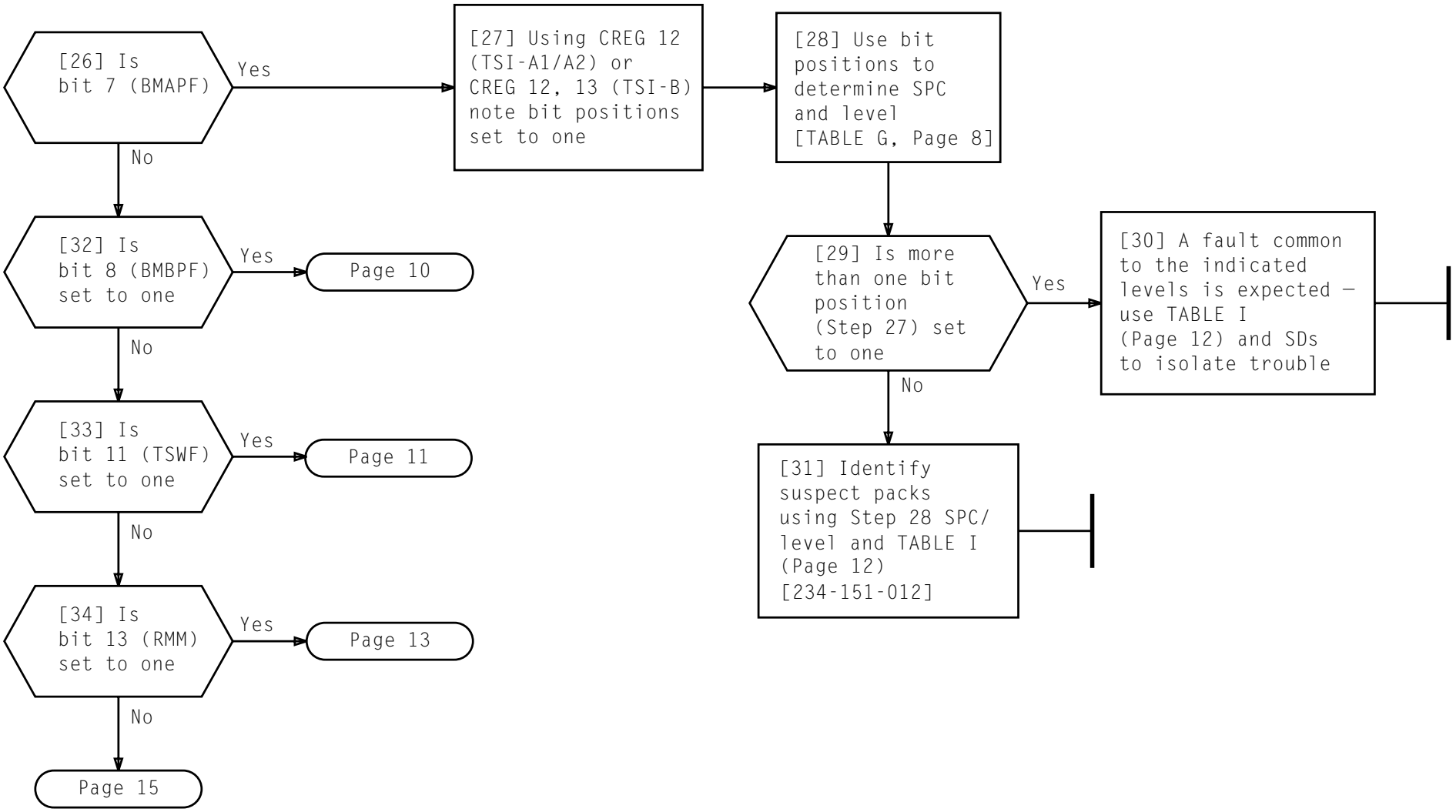
* (ODD NUMBERED SECONDARIES)																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
3								2								SPC

* For TSI-B

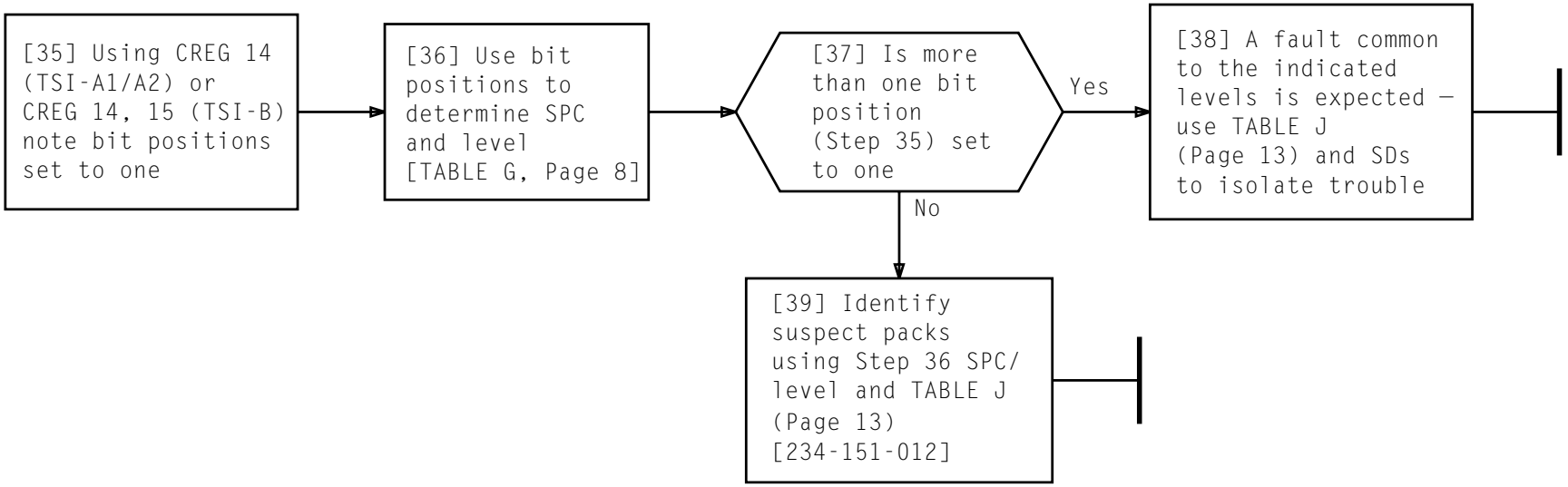
TABLE H
SUSPECT PACKS FOR CREG 3/4 BIT 12

	TSI (SD-4A011-01, 02)			TSI (SD-4A083-01)				
LEVEL	CIRCUIT PACK TYPE	SPC 0	SPC 1	CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
0	FB221(B) FA567 FA569	38-23 38-19 38-11	60-23 60-19 60-11	FB221B FA1791 FA1782	*24-69 *24-68 *24-66	*36-69 *36-68 *36-66	*48-69 *48-68 *48-66	*60-69 *60-68 *60-66
1	FB221(B) FA567 FA569	38-23 38-18 38-10	60-23 60-18 60-10	FB221B FA1791 FA1782	*24-69 *24-65 *24-63	*36-69 *36-68 *36-63	*48-69 *48-68 *48-63	*60-69 *60-68 *60-63
2	FB221(B) FA567 FA569	38-22 38-17 38-09	60-22 60-17 60-09	FB221B FA1791 FA1782	*24-61 *24-60 *24-58	*36-61 *36-60 *36-58	*48-61 *48-60 *48-58	*60-61 *60-60 *60-58
3	FB221(B) FA567 FA569	38-22 38-15 38-08	60-22 60-15 60-08	FB221B FA1791 FA1782	*24-61 *24-56 *24-54	*36-61 *36-56 *36-54	*48-61 *48-56 *48-54	*60-61 *60-56 *60-54
4	FB221(B) FA567 FA569	38-21 38-14 38-07	60-21 60-14 60-07	FB221B FA1791 FA1782	*24-52 *24-51 *24-49	*36-52 *36-51 *36-49	*48-52 *48-51 *48-49	*60-52 *60-51 *60-49
5	FB221(B) FA567 FA569	38-21 38-13 38-06	60-21 60-13 60-06	FB221B FA1791 FA1782	*24-52 *24-47 *24-45	*36-52 *36-47 *36-45	*48-52 *48-47 *48-45	*60-52 *60-47 *60-45
6	FB221(B) FA567 FA569	38-20 38-12 38-05	60-20 60-12 60-05	FB221B FA1791 FA1782	*24-43 *24-41 *24-39	*36-43 *36-41 *36-39	*48-43 *48-41 *48-39	*60-43 *60-41 *60-39
7				FB221B FA1791 FA1782	*24-43 *24-38 *24-37	*36-43 *36-38 *36-37	*48-43 *48-38 *48-37	*60-43 *60-38 *60-37

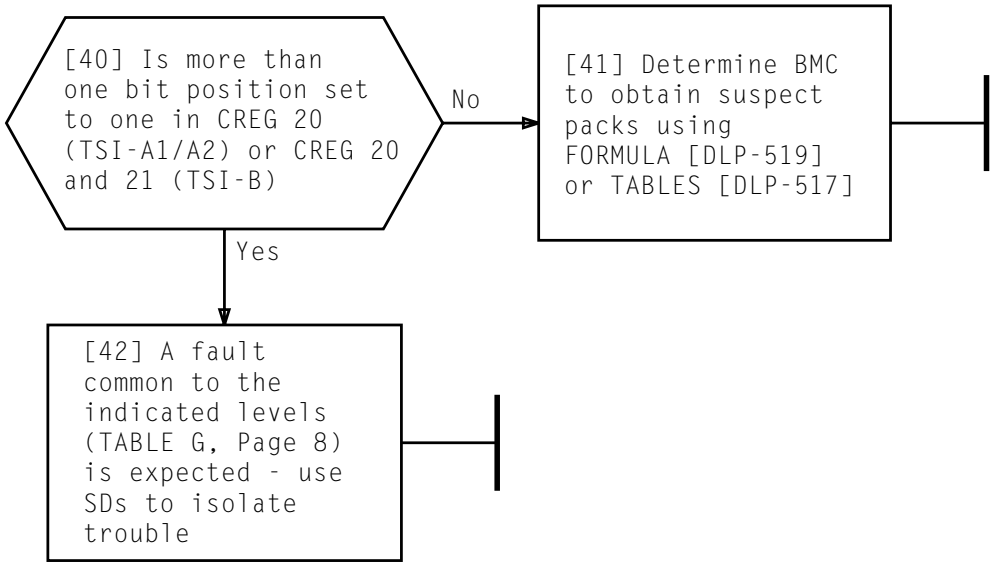
* Bay 0 or 1 same as suspect controller



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

TABLE I — SUSPECT PACK LIST FOR ESR BIT 7										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA633(B)	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	42-15, 42-14 (Address Select)				42-13, 42-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	24-68	24-65	24-60	24-56	24-51	24-47	24-41	N/A
		FA1782	24-66	24-63	24-58	24-54	24-49	24-45	24-39	N/A
1	TSI-A1 SD4A011-01	FA633(B)	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	36-68	36-65	36-60	36-56	36-51	36-47	36-41	36-38
		FA1782	36-66	36-63	36-58	36-54	36-49	36-45	36-39	36-37
2	TSI-B SD4A083-01	FA1791	48-68	48-65	48-60	48-56	48-51	48-47	48-41	48-38
		FA1782	48-66	48-63	48-58	48-54	48-49	48-45	48-39	48-37
3	TSI-B SD4A083-01	FA1791	60-68	60-65	60-60	60-56	60-51	60-47	60-41	60-38
		FA1782	60-66	60-63	60-58	60-54	60-49	60-45	60-39	60-37

TABLE J — SUSPECT PACK LIST FOR ESR BIT 8										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA633(B)	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA544	50-26	50-25	50-24	50-23	50-22	50-21	50-20	50-19
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA1198	50-26		50-24		50-22		50-20	
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	28-45	28-45	28-45	28-45	28-45	28-45	28-45	28-45
		FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
1	TSI-A1 SD4A011-01	FA633(B)	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA544	72-26	72-25	72-24	72-23	72-22	72-21	72-20	72-19
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA1198	72-26		72-24		72-22		72-20	
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	40-45	40-45	40-45	40-45	40-45	40-45	40-45	40-45
		FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
2	TSI-B SD4A083-01	FA1786	52-45	52-45	52-45	52-45	52-45	52-45	52-45	52-45
		FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1786	64-45	64-45	64-45	64-45	64-45	64-45	64-45	64-45
		FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC - all levels)										

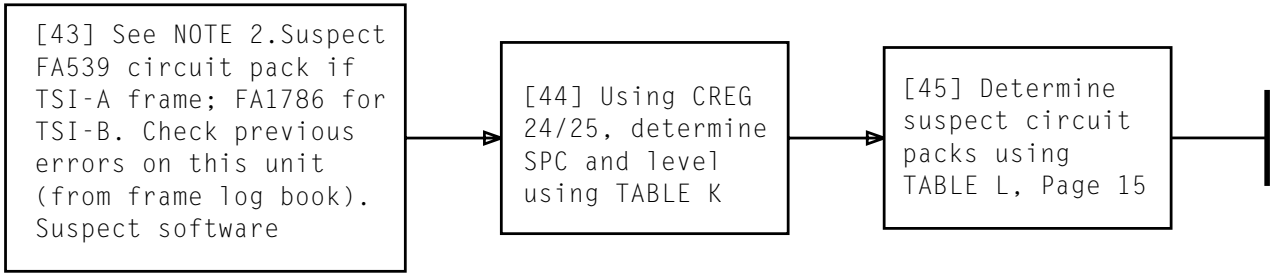


TABLE K
LEVEL AND SPC

CREGs		SPC								SPC							
RMM 24 25	TMM 26 27	1 3								0 2							
BIT		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

NOTE 2
An RMM mismatch has occurred. Either controller may be suspect. Other interrupts with unique errors should be used to select suspect

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

TABLE L
SUSPECT RMM — CIRCUIT PACKS FOR ESR BIT 13

FRAME TYPE	SPC	CIRCUIT PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 (SD-4A011-01) or TSI-A2 (SD-4A011-02)	0	FA542	46-09	46-07	46-08			46-06	46-04	46-05
		FA633*	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	
		FA539	—	—	—	—	—	—	—	—
	1	FA542	68-09	68-07	68-08		68-06	68-04	68-05	
		FA633*	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	
		FA539	—	—	—	—	—	—	—	—
SD-4A083-01	0	FA1780	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
		FA1786	← 28-45 →							
	1	FA1780	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
		FA1786	← 40-45 →							
	2	FA1780	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
		FA1786	← 52-45 →							
	3	FA1780	64-68	64-56	64-54	64-51	64-43	64-41	64-39	64-37
		FA1786	← 64-45 →							

* TSI-A2 (SD4A011-02) has FA633B pack, TSI-A1 (SD4A011-01) could have FA633B pack.

[46] See NOTE 3. Using CREG 26/27 and TABLE K, Page 14 determine SPC and level

→ [47] Determine suspect packs using TABLE M [234-151-012]

TABLE M
SUSPECT TMM-CIRCUIT PACKS FOR ESR BIT 14

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A023-01] or TSI-A2 [SD-4A023-02]	0	FA539	38-56	38-55	38-54	38-53	38-52			
		FA633*	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
	1	FA539	60-56	60-55	60-54	60-53	60-52			
		FA633*	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
TSI-B [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1787	← 28-29 →							
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1787	← 40-29 →							
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1787	← 52-29 →							
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1787	← 64-29 →							

* TSI-A2 has FA633B pack, TSI-A1 could have FA633B pack.

NOTE 3
Bit 14 is set indicating a TMM mismatch has occurred. Either controller may be suspect. Other interrupts with unique errors should be used to select suspect

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

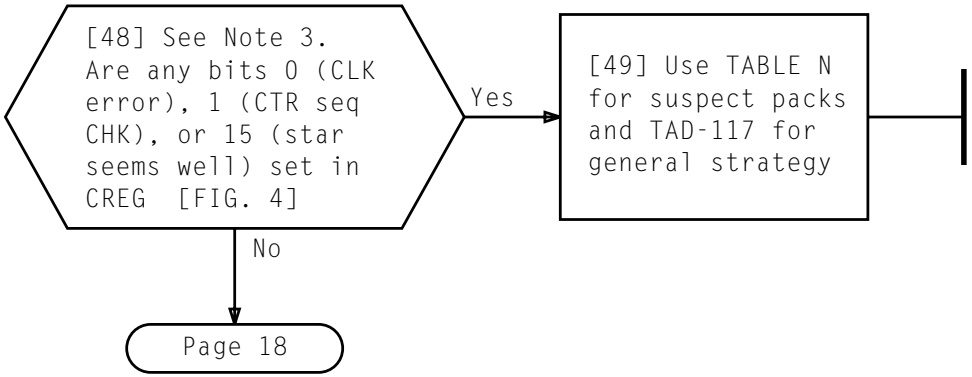


TABLE N
CLOCK BITS

FRAME TYPE	SET BIT	PACK TYPE	LOCATION
TSI-A1 [SD-4A023-01]	0,1,3	FA562 FB225 FB224 FA552 FA553 FA554	56-36 56-35 56-37 56-30 56-33 56-34
	15	FB220 FB225	56-39 56-35
TSI-A2 [SD-4A023-02]	0,1,3	FA562 FC463 FA552 FA553 FA554	56-36 56-35 56-30 56-33 56-34
TSI-B [SD-4A083-01]	0,1,3	FA1798 FA1233 FA1234 FC464	72-29 72-31 72-30 72-27

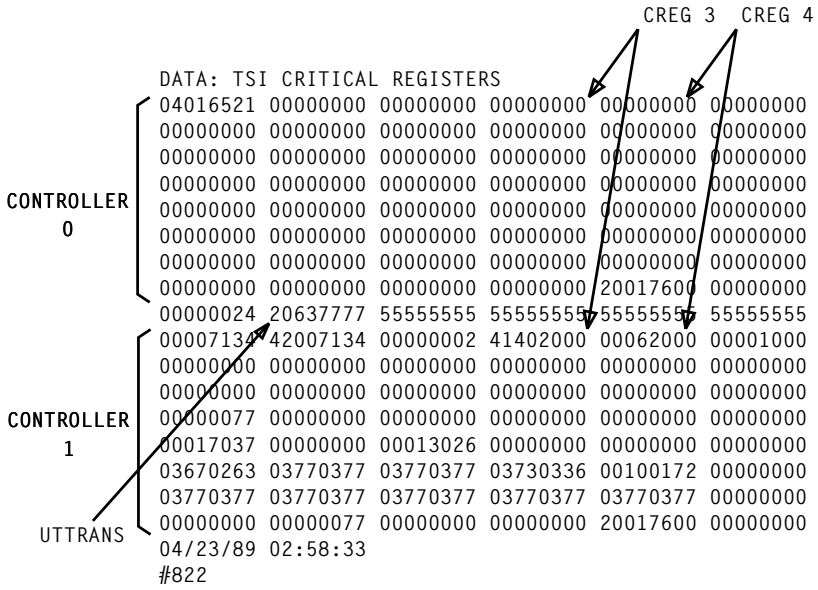
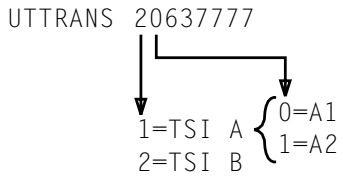


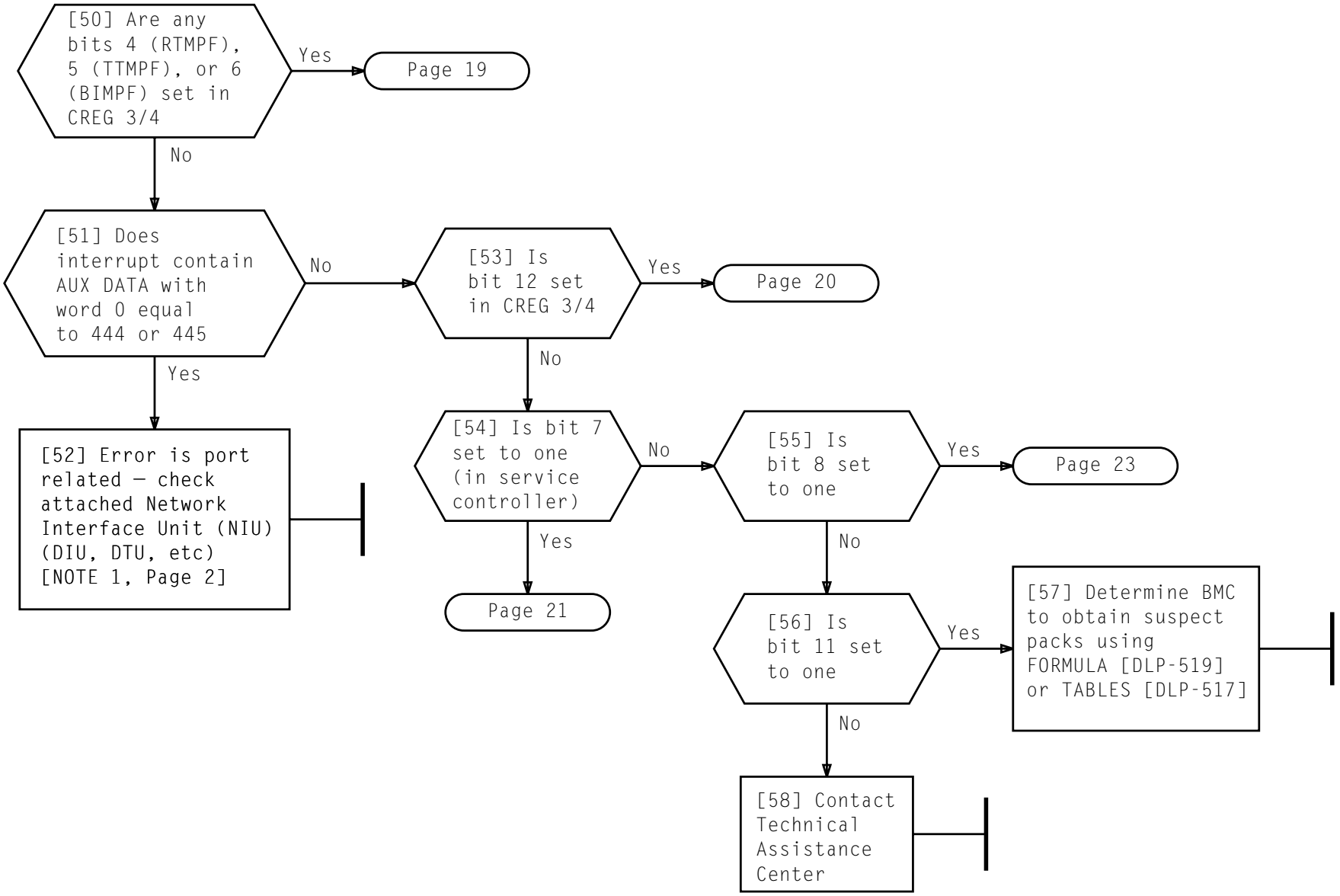
Figure 4 – TSI CREGs



EXAMPLE 2

NOTE 3
Analysis is for a simplex unit interrupt. Information is less conclusive than a duplex unit interrupt

ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

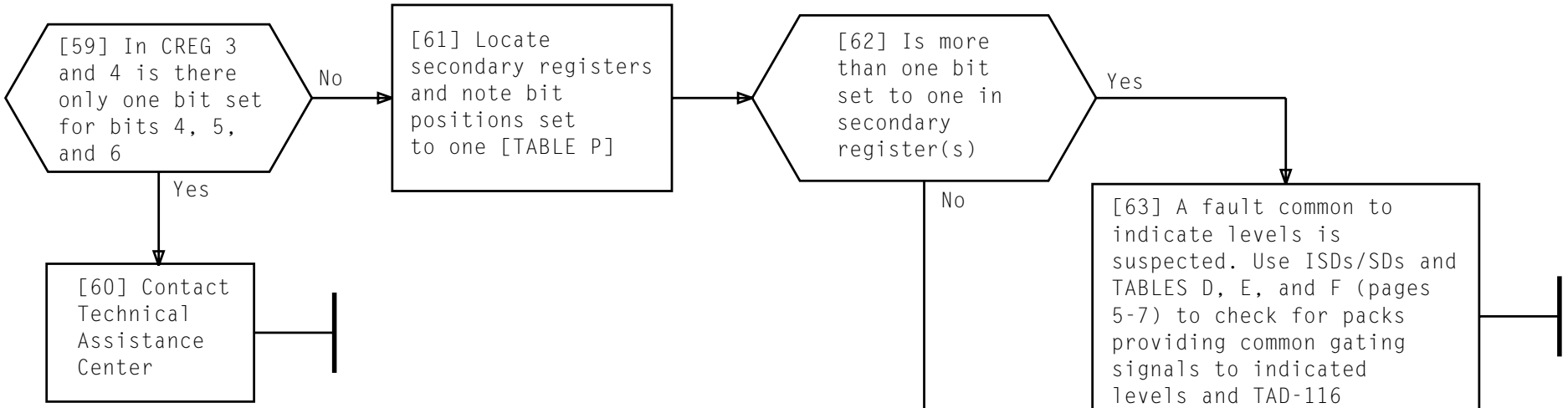


TABLE P
SECONDARY REGISTERS FOR SET ESR BIT

ASSOCIATED SECONDARY REGISTERS		
CREG 3, 4 ERROR SOURCE BIT	**ORIGINAL TSI FRAME (SD-4A011-01) OR NEAR TERM TSI FRAME (SD-4A011-02)**	**COST REDUCED TSI FRAME (SD-4A083-01)**
4(RTSMP)	CREG 6	CREG 6, CREG 7
5(TTSMP)	CREG 8	CREG 8, CREG 9
6(BIMPF)	CREG 10	CREG 10, CREG 11

TABLE Q
SPC AND LEVEL

CREG	SPC								SPC							
6,8,10 7,9,11	1 3								0 2							
BIT	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

[66] Using CREG 22 (TSI-A1/A2) or CREG 22 and 23 (TSI-B) determine bit position set to one [See Figure 4 and Example 2 for frame type (Page 17)]

↓

[67] Use bit position set to one and TABLE R then TABLE S to identify suspect packs [234-151-012]

TABLE R
IDENTIFICATION OF SPC AND LEVEL

(EVEN NUMBERED SECONDARIES)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
1								0								SPC

*** (ODD NUMBERED SECONDARIES)**

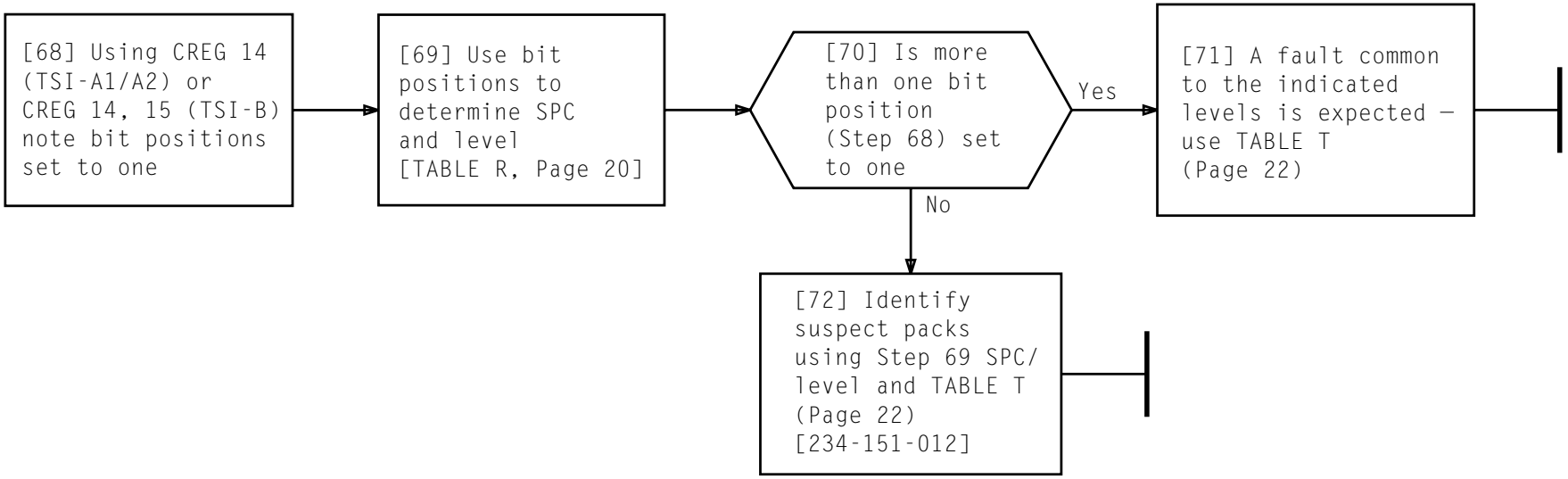
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																BIT POSITION
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	LEVEL
3								2								SPC

* For TSI-B

TABLE S
SUSPECT PACKS FOR CREG 3/4 BIT 12

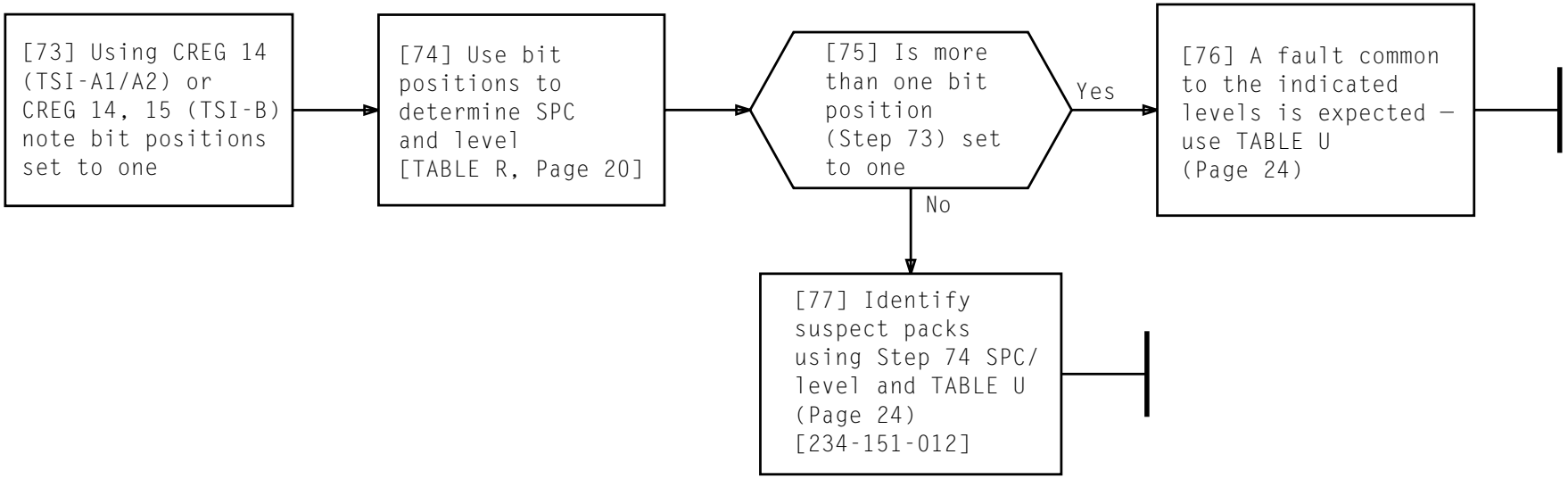
	TSI (SD-4A011-01, 02)			TSI (SD-4A083-01)				
LEVEL	CIRCUIT PACK TYPE	SPC 0	SPC 1	CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
0	FB221 FA567 FA569	38-23 38-19 38-11	60-23 60-19 60-11	FB221B FA1791 FA1782	*24-69 *24-68 *24-66	*36-69 *36-68 *36-66	*48-69 *48-68 *48-66	*60-69 *60-68 *60-66
1	FB221 FA567 FA569	38-23 38-18 38-10	60-23 60-18 60-10	FB221B FA1791 FA1782	*24-69 *24-65 *24-63	*36-69 *36-68 *36-63	*48-69 *48-68 *48-63	*60-69 *60-68 *60-63
2	FB221 FA567 FA569	38-22 38-17 38-09	60-22 60-17 60-09	FB221B FA1791 FA1782	*24-61 *24-60 *24-58	*36-61 *36-60 *36-58	*48-61 *48-60 *48-58	*60-61 *60-60 *60-58
3	FB221 FA567 FA569	38-22 38-15 38-08	60-22 60-15 60-08	FB221B FA1791 FA1782	*24-61 *24-56 *24-54	*36-61 *36-56 *36-54	*48-61 *48-56 *48-54	*60-61 *60-56 *60-54
4	FB221 FA567 FA569	38-21 38-14 38-07	60-21 60-14 60-07	FB221B FA1791 FA1782	*24-52 *24-51 *24-49	*36-52 *36-51 *36-49	*48-52 *48-51 *48-49	*60-52 *60-51 *60-49
5	FB221 FA567 FA569	38-21 38-13 38-06	60-21 60-13 60-06	FB221B FA1791 FA1782	*24-52 *24-47 *24-45	*36-52 *36-47 *36-45	*48-52 *48-47 *48-45	*60-52 *60-47 *60-45
6	FB221 FA567 FA569	38-20 38-12 38-05	60-20 60-12 60-05	FB221B FA1791 FA1782	*24-43 *24-41 *24-39	*36-43 *36-41 *36-39	*48-43 *48-41 *48-39	*60-43 *60-41 *60-39
7		N/A	N/A	FB221B FA1791 FA1782	*24-43 *24-38 *24-37	*36-43 *36-38 *36-37	*48-43 *48-38 *48-37	*60-43 *60-38 *60-37

* Bay 0 or 1 same as suspect controller



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

TABLE T — SUSPECT PACK LIST FOR ESR BIT 7										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	TSI-A1 SD4A011-01	FA633	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	42-11	42-10	42-09	42-08	42-07	42-06	42-05	42-04
		FA542	(46-09, 46-08, 46-07)				(46-06, 46-05, 46-04)			
		FA569	38-11	38-10	38-09	38-08	38-07	38-06	38-05	N/A
		FA567	38-19	38-18	38-17	38-15	38-14	38-13	38-12	N/A
		FA540	42-15, 42-14 (Address Select)				42-13, 42-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	24-68	24-65	24-60	24-56	24-51	24-47	24-41	N/A
		FA1782	24-66	24-63	24-58	24-54	24-49	24-45	24-39	N/A
1	TSI-A1 SD4A011-01	FA633	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	64-11	64-10	64-09	64-08	64-07	64-06	64-05	64-04
		FA542	(68-09, 68-08, 68-07)				(68-06, 68-05, 68-04)			
		FA569	60-11	60-10	60-09	60-08	60-07	60-06	60-05	N/A
		FA567	60-19	60-18	60-17	60-15	60-14	60-13	60-12	N/A
		FA540	64-15, 64-14 (Address Select)				64-13, 64-12 (Address Select)			
	TSI-B SD4A083-01	FA1791	36-68	36-65	36-60	36-56	36-51	36-47	36-41	36-38
		FA1782	36-66	36-63	36-58	36-54	36-49	36-45	36-39	36-37
2	TSI-B SD4A083-01	FA1791	48-68	48-65	48-60	48-56	48-51	48-47	48-41	48-38
		FA1782	48-66	48-63	48-58	48-54	48-49	48-45	48-39	48-37
3	TSI-B SD4A083-01	FA1791	60-68	60-65	60-60	60-56	60-51	60-47	60-41	60-38
		FA1782	60-66	60-63	60-58	60-54	60-49	60-45	60-39	60-37



ANALYZE TNFR, F-LEVEL INTERRUPT, TIME-SLOT INTERCHANGE

TABLE U — SUSPECT PACK LIST FOR ESR BIT 8										
SPC	FRAME TYPE	PACK TYPE	LEVEL							
			0	1	2	3	4	5	6*	7*
0	TSI-A1 SD4A011-01	FA633	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA544	50-26	50-25	50-24	50-23	50-22	50-21	50-20	50-19
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	50-18	50-17	50-15	50-14	50-13	50-12	50-11	50-10
		FA1198	50-26		50-24		50-22		50-20	
		FA540	46-18, 46-17 (Address Select)				46-15, 46-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	28-45	28-45	28-45	28-45	28-45	28-45	28-45	28-45
		FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
1	TSI-A1 SD4A011-01	FA633	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA544	72-26	72-25	72-24	72-23	72-22	72-21	72-20	72-19
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
	TSI-A2 SD4A011-02	FA633B	72-18	72-17	72-15	72-14	72-13	72-12	72-11	72-10
		FA1198	72-26		72-24		72-22		72-20	
		FA540	68-18, 68-17 (Address Select)				68-15, 68-14 (Address Select)			
	TSI-B SD4A083-01	FA1786	40-45	40-45	40-45	40-45	40-45	40-45	40-45	40-45
		FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
2	TSI-B SD4A083-01	FA1786	52-45	52-45	52-45	52-45	52-45	52-45	52-45	52-45
		FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
3	TSI-B SD4A083-01	FA1786	64-45	64-45	64-45	64-45	64-45	64-45	64-45	64-45
		FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
* FA1780 or FA1816 (wide band option on SPC - all levels)										

[1] See NOTE 1. Using FIG. 1, locate CREG 2 for suspect controller and determine if bit 0 is set to one [DLP-518]

[2] Is bit 0 set to one

Yes

[3] Are any bits 2-13 set to one in CREG 2

Yes

[4] See NOTE 2. Are any bits 5-13 set to one in CREG 2

Yes

Page 3

No

No

No

Page 2

[5] No error was detected by TSI unit. Analyze CC F LEVEL registers to determine CC, BUS, and unit configurations [TAP-115]

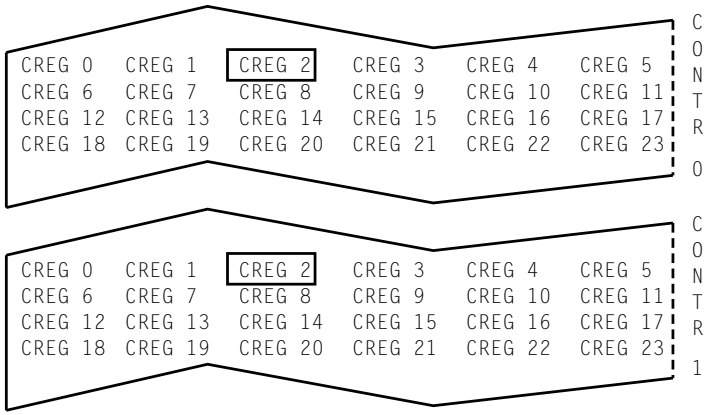
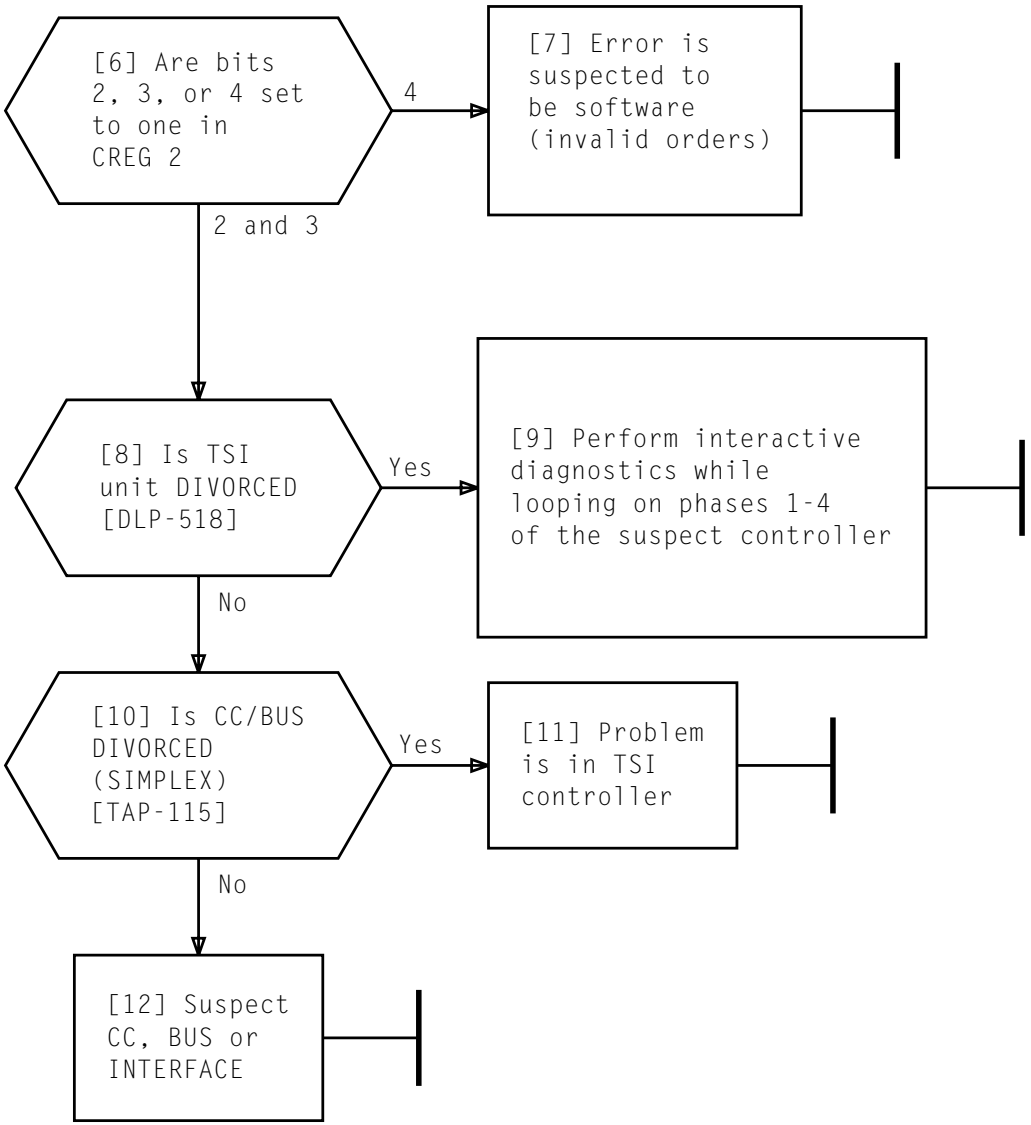


FIG. 1 — TSI CREGs

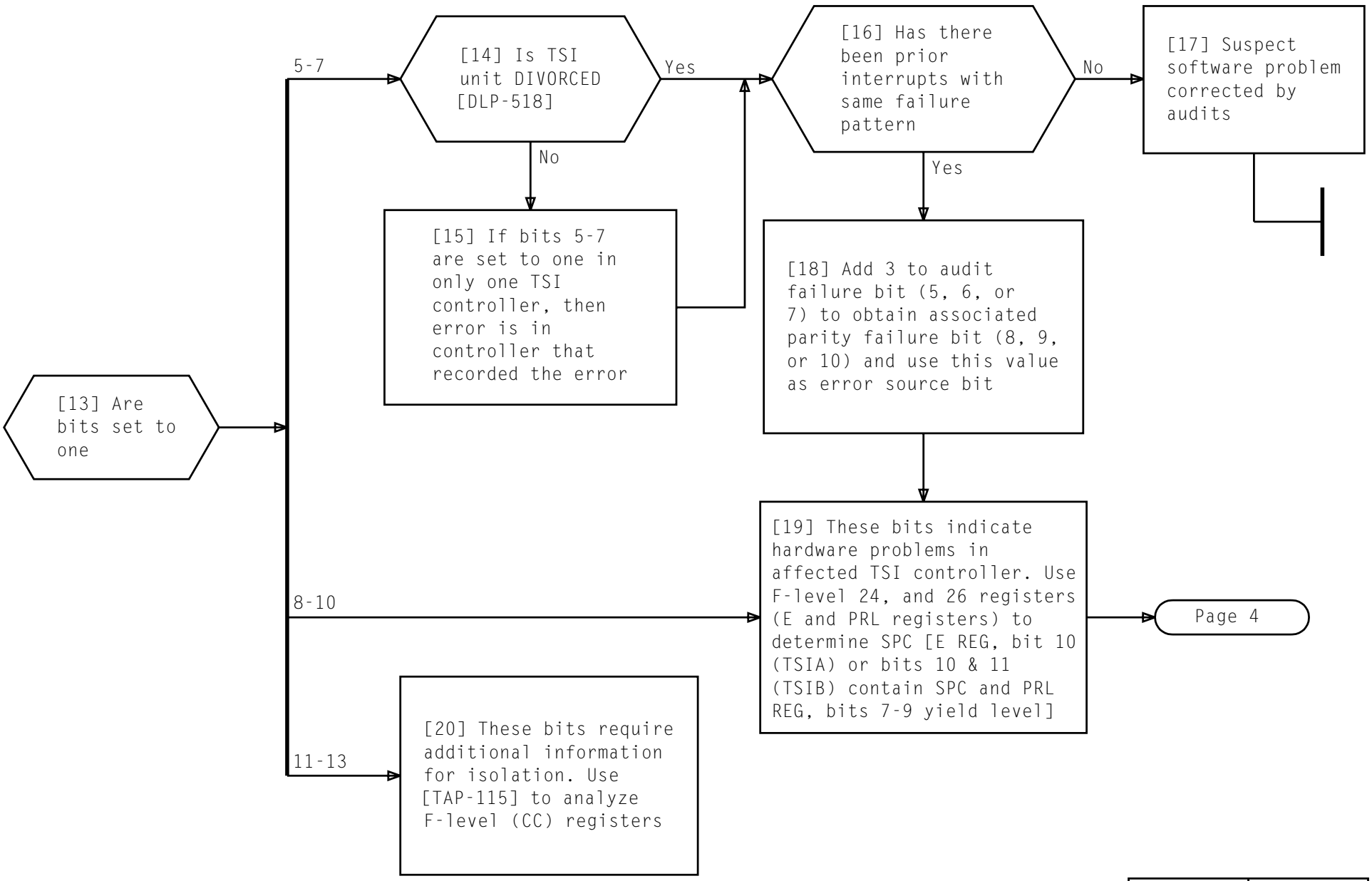
NOTES

1. In-service TSI unit should only be considered.
2. If any bit 5—7 is **only** bit(s) set, then printout should be saved and NESAC should be notified of possible software error

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME SLOT INTERCHANGE



ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME SLOT INTERCHANGE



ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME SLOT INTERCHANGE

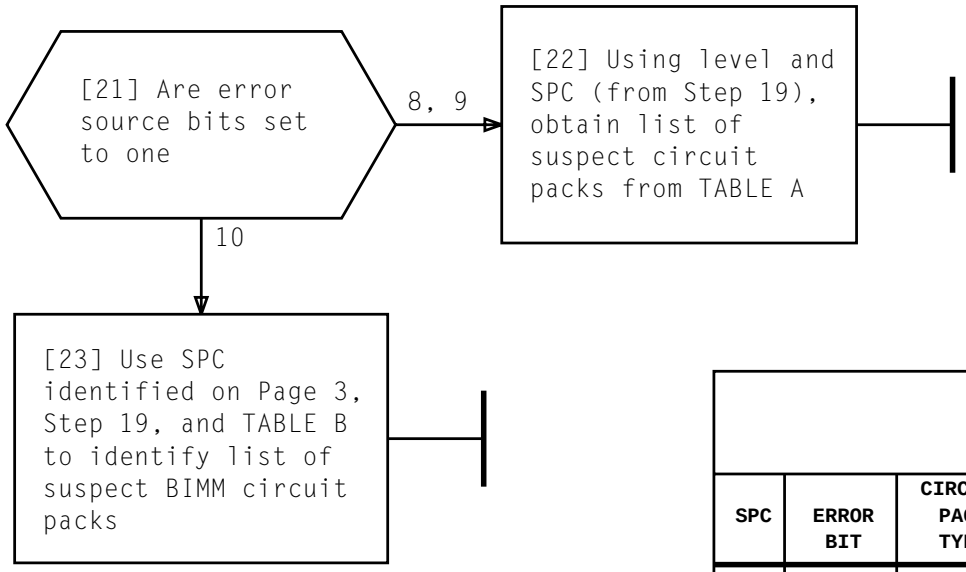


TABLE B
BIMM SUSPECT PACKS
(SD-4A023-01, 02); (SD-4A083-01)

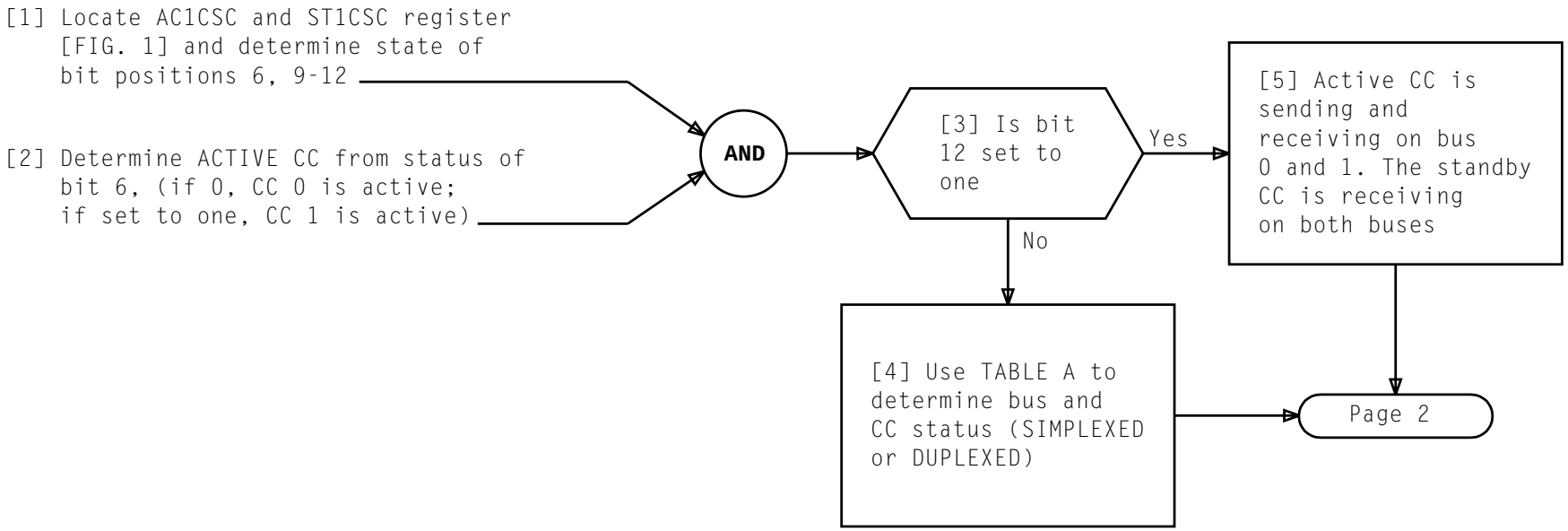
CIRCUIT PACK TYPE	SPC 0	SPC 1	SPC 2	SPC 3
FA556	42-52	64-52	NA	NA
FA555	56-38			
FA1783	28-28	40-28	52-28	64-28

TABLE A
SUSPECT TSM MEMORY PACKS
SD-4A023-01,02

SPC	ERROR BIT	CIRCUIT PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
0	8	FA543	46-26	46-25	46-24	46-23	46-22	46-21	46-20	46-19
	9	FA541	46-44	46-43	46-42	46-41	46-40	46-39	46-38	46-37
1	8	FA543	68-26	68-25	68-24	68-23	68-22	68-21	68-20	68-19
	9	FA541	68-44	68-43	68-42	68-41	68-39	68-38	68-37	68-36
SD-4A083-01										
0	8	FA1780*	28-58	28-56	28-54	28-51	28-43	28-41	28-39	28-37
	9	FA1781†	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
1	8	FA1780*	40-58	40-56	40-54	40-51	40-43	40-41	40-39	40-37
	9	FA1781†	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
2	8	FA1780*	52-58	52-56	52-54	52-51	52-43	52-41	52-39	52-37
	9	FA1781†	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
3	8	FA1780*	64-58	64-56	64-54	64-51	64-43	64-41	64-39	64-37
	9	FA1781†	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04

* May be FA1816
† May be FA1817

ANALYZE TNFR F-LEVEL INTERRUPT, PERIPHERAL UNIT FAULT (PUF), TIME SLOT INTERCHANGE




```
F-LEVEL

AC1FR        AC1GR        AC1JR        AC1KR        AC1LR        AC1XR
AC1YR        AC1ZR        AC1BR        AC1CAR       AC1ILA       AC1SCA
AC1SDA       AC1SPA       AC1CSC       AC1INS       AC1INH       AC1SC
AC1SR        AC1INJ       AC1PES       AC1PSC       AC1DE        AC1RR
AC1ER        AC1PRM       AC1PRL       ST1LR        ST1PES       ST1PSC
ST1DE        ST1RR        ST1ER        ST1PRM       ST1PRL       ST1INS
ST1CSC       ST1INH       AC1LR_S      PU1RFLC00    PU1RFLC01    PU1RFLC02
PU1RFLC03    PU1RFLC04    PU1RFLC05    PU1RFLC06    PU1RFLC07

PU1RFLC00                    CONTROLLER 0 PULSE POINT REPLY
       01                                1   "     "     "
       02                                0 STATUS REGISTER
       03                                1   "       "
       04                                0 ERROR SOURCE REGISTER
       05                                1   "       "       "
                                         FAIL TEST
       06                                FAIL DATA
       07
AC1 - ACTIVE CC REGISTER
ST1 - STANDBY CC REGISTER
```

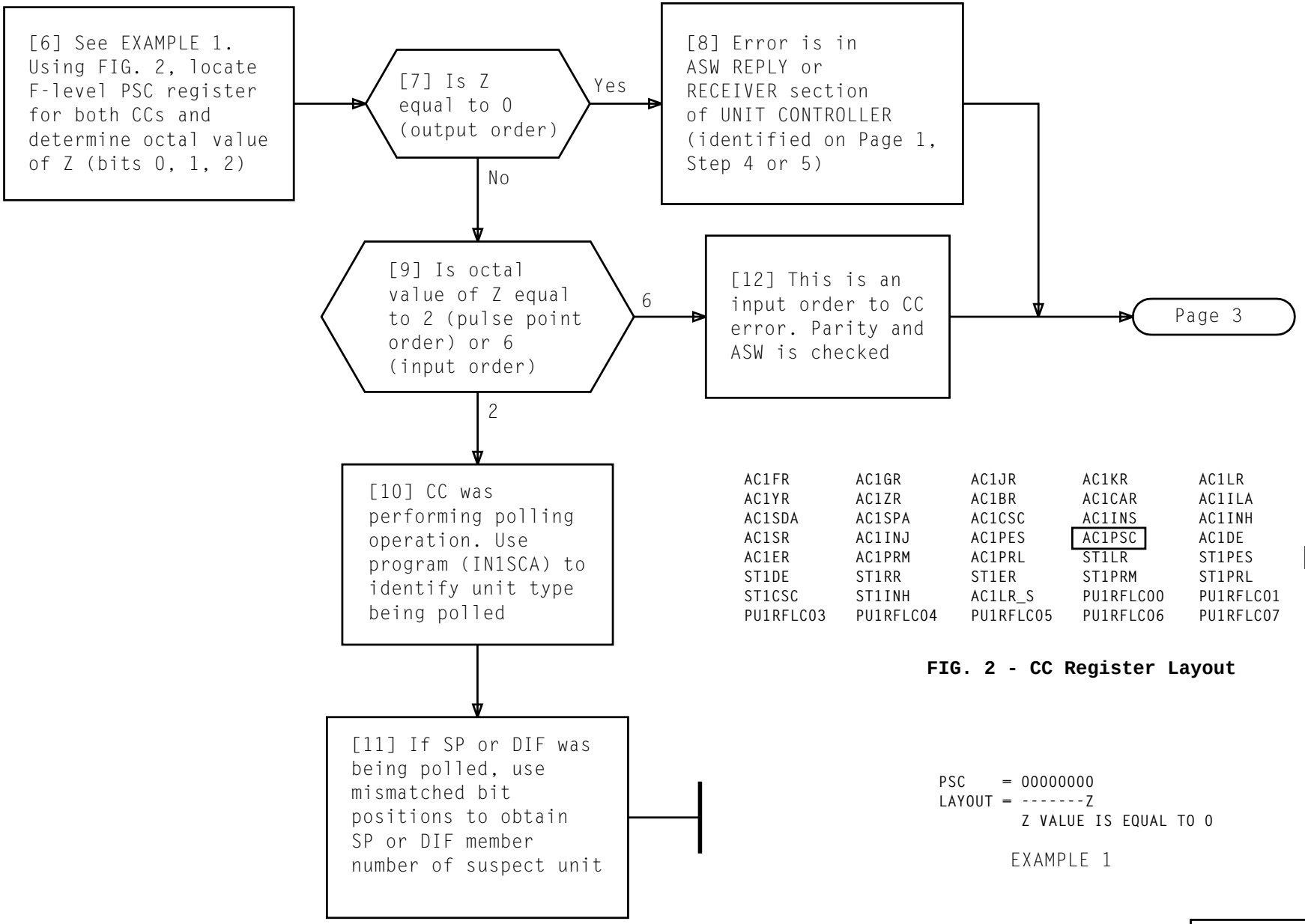
FIG. 1 - CC Register Layout

TABLE A
CSC REGISTER

BIT VALUE			ACTIVE CC		STANDBY CC	
PUBT 11	PUBA 10	PUBO 09	ENABLE/ WRITE	REPLY (RECEIVE)	ENABLE/ WRITE	REPLY (RECEIVE)
0	0	0	0	0	1	1
0	1	0	1	1	0	0
1	0	0	0	0	X	0
1	1	0	1	1	X	1
0	0	1	0&1	0	X	1
0	1	1	0&1	1	X	0
1	0	1	0&1	0	X	0
1	1	1	0&1	1	X	1

X = Idle, bus receives only

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS



AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR	AC1CAR	AC1ILA	AC1SCA
AC1SDA	AC1SPA	AC1CSC	AC1INS	AC1INH	AC1SC
AC1SR	AC1INJ	AC1PES	AC1PSC	AC1DE	AC1RR
AC1ER	AC1PRM	AC1PRL	ST1LR	ST1PES	ST1PSC
ST1DE	ST1RR	ST1ER	ST1PRM	ST1PRL	ST1INS
ST1CSC	ST1INH	AC1LR_S	PU1RFLC00	PU1RFLC01	PU1RFLC02
PU1RFLC03	PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07	

FIG. 2 - CC Register Layout

```
PSC    = 00000000
LAYOUT = -------Z
         Z VALUE IS EQUAL TO 0
```

EXAMPLE 1

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS

[13] Using FIG. 3, locate F-LEVEL PES register for both CCs and determine if bit 6 and/or 7 set to one

[14] Bit(s) set to one

6 only or 6 and 7

7 only

[15] Locate F-LEVEL WORD AC1ER [FIG. 3] and convert bit positions 10-21 to binary

[16] Identify unit being addressed by CC [TABLE C]

[17] Does your office have this unit type member

Yes

No

[18] Does register PU1RFLC04 or PU1RFLC05 have bits set to one [FIG. 3]

No

Yes

[21] Suspect write or enable bus problem to that unit type or unit type member

[20] Is unit type I/O

No

Yes

[23] Analyze units error(s) as indicated in both PU1RFLC04 and PU1RFLC05 [TABLE F]

[19] This is a software problem. Get help from technical assistance center

[22] Analyze using bits set to one in PU1RFLC04. See TABLE E

[24] Using TABLE B, compare state of bit 7 for both CCs and note indication given in table for future use

[25] Using FIG. 3, locate AC1LR and ST1LR and determine bit positions with mismatching state

Page 5

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	AC1BR	AC1CAR	AC1ILA	AC1SCA
AC1SDA	AC1SPA	AC1CSC	AC1INS	AC1INH	AC1SC
AC1SR	AC1INJ	AC1PES	AC1PSC	AC1DE	AC1RR
AC1ER	AC1PRM	AC1PRL	ST1LR	ST1PES	ST1PSC
ST1DE	ST1RR	ST1ER	ST1PRM	ST1PRL	ST1INS
ST1CSC	ST1INH	AC1LR_S	PU1RFLC00	PU1RFLC01	PU1RFLC02
PU1RFLC03	PU1RFLC04	PU1RFLC05	PU1RFLC06	PU1RFLC07	

FIG. 3 - CC Register Layout

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS

TABLE B — PES BIT 7		
CC0	CC1	INDICATION
0	0	No error detected by CC. Peripheral unit reply problem. Use configuration to resolve error (CC, BUS, CONTR) and other indications (prior interrupts, growth activity, power sequencing, etc)
0 1	1 0	Bus related problem
1	1	A simplexed controller is suspected to contain error. Request technical assistance, if necessary

TABLE C — E-REGISTER LAYOUTS

BITS →	21	20	19	18	17	16	15	14	13	12	11	10
MCC	0	0	0	0	1	1	1	1	0	1	1	0
SP/DIF	0	0	0	1	0	Member number					MTX	
SCLK	0	0	0	1	1	Member number						
TMS	0	0	1	0	0						MEM NO	
TSI	0	0	1	0	1	Member number						SPC
TGR	0	0	1	1	0	Member number						
IOUS	0	0	1	1	1	Member number					IOUC	
EST	0	1	0	0	1	Member number						
SCS	0	1	0	1	1	Member number				SCU NUMBER		
BITS →	21	20	19	18	17	16	15	14	13	12	11	10

TABLE D — CONSIDERATIONS FOR ISOLATION	
CONSIDERATION NUMBER	CONSIDERATION
1	If only one unit is involved
2	If multiple bits are set rather than same bits
3	If error occurs on same branch pair of PUB
4	After several days, CC is independent or dependent of error dependent of error
5	The integration of change versus no change (that is, after a period of time, does the error follow a pattern with different bus, controller, and/or CC configurations; or does it occur only with certain configurations)

TABLE E — I/O F LEVELS	
REGISTER	DESCRIPTION
PU1RFLC00	PLSRPLY (MA PULSE REPLY)
PU1RFLC01	USOFT-STAT (UNIT SOFT STATUS)
PU1RFLC02	UHARD-STAT (UNIT HARD STATUS)
PU1RFLC03	SU-STAT (SUBUNIT STATUS)
PU1RFLC04	ESR (ERROR SUMMARY)
PU1RFLC05	ACTION (RECOVERY ACTION)
PU1RFLC06	CSR (CHANNEL STATUS REGISTER)
PU1RFLC07	TSTRSLT (TEST RESULT FLAGS)

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS

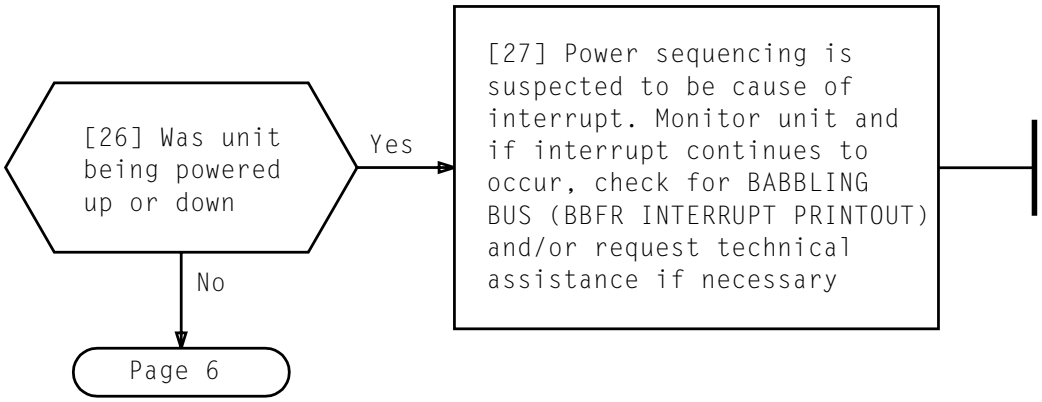
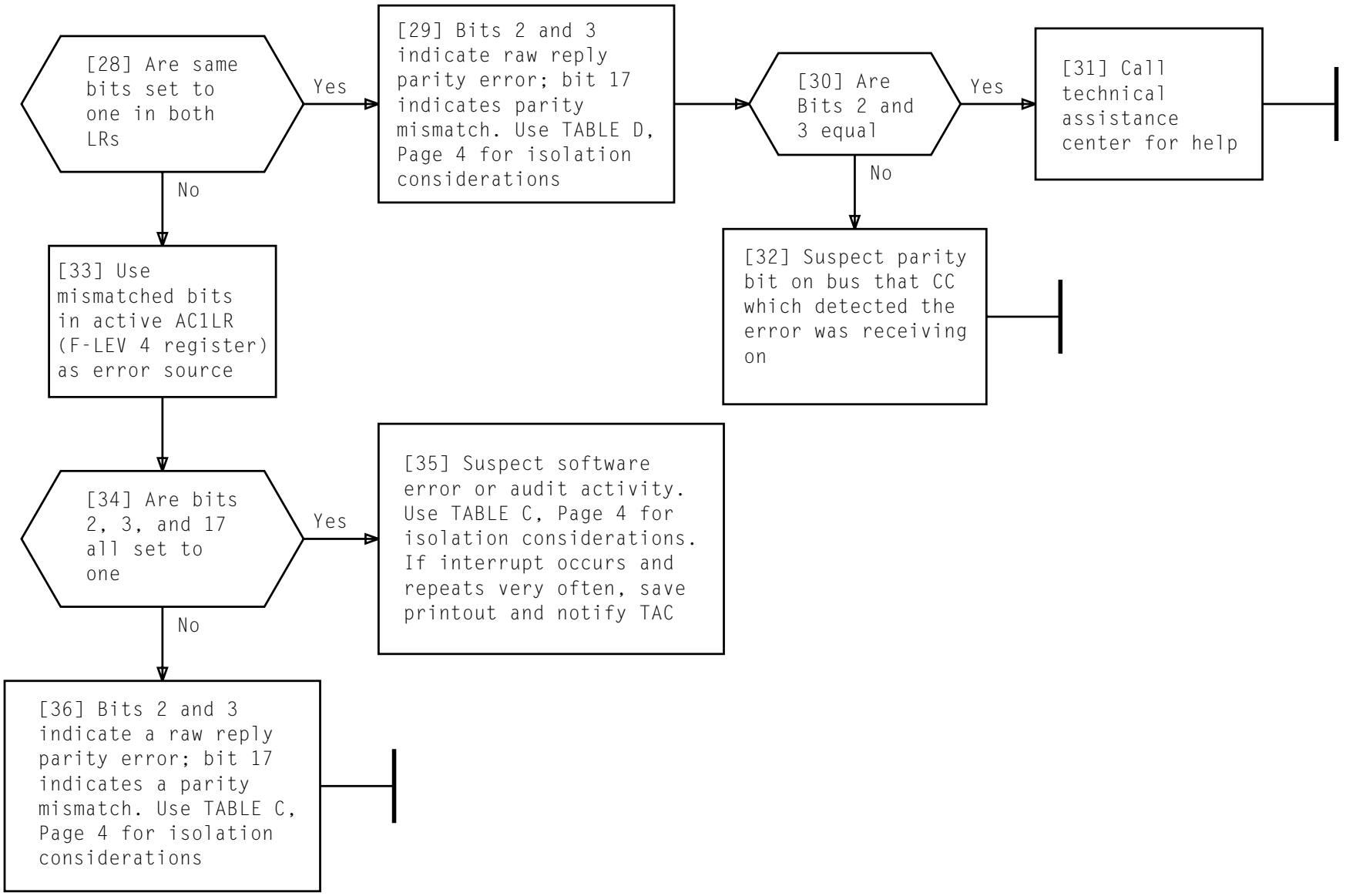


TABLE F — CRITICAL REGISTERS

UNIT TYPE	PU1RFLC04 (CONTR 0)	PU1RFC05 (CONTR1)
DIF	CESR	CESR
EST	CESR1	CESR1
TMS	TG4ESR+0	TG4ESR+0
TSI	ASESR (ESR0)	ASESR (ESR0)
SP	SP4ESR1	SP4ESR1
SCLK	HESR	HESR
CCIS	ESR	ESR

ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS



ANALYZE F-LEVEL INTERRUPT, (CC) REGISTER ANALYSIS

This data formulates the strategy to be used when multiple bits are set in bit positions 4 through 14 of TSI controller error source registers (ESR+1)

1. Use ERAP data and attempt to locate a repeating pattern or common unit
2. Check prior printouts for audit activities that may have been involved with an interrupt
3. Investigate clock problems external to TSI frame
4. Use FIG. 1 to check bits 4-7 (implicate cable/bus as suspect) in PERIPHERAL SYSTEM DATA WORD 1
5. Analyze F-level Registers
6. Check SDs and attempt to locate a common circuit pack

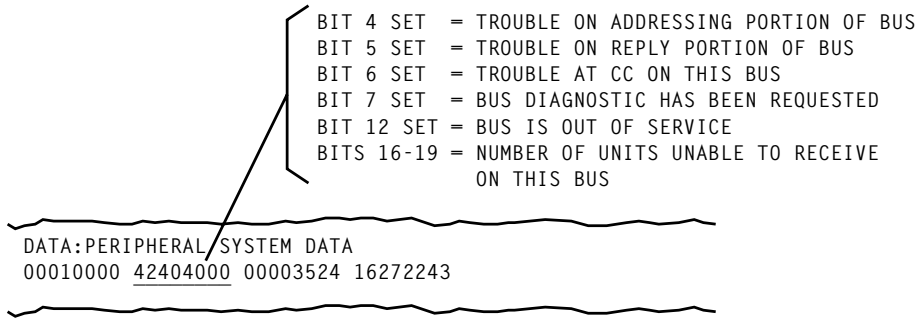


FIG. 1 — Cable/Bus Implication

F-LEVEL INTERRUPT, TSI MULTIPLE FAULT INDICATIONS STRATEGY

CAUTION: Maintenance on a simplexed unit is complicated by the system's inability to reconfigure and could cause a directed phase one.

The following stratagems are provided as general guidelines for analyzing faults in a simplexed TSI.

1. Check to see if maintenance activities may have caused problem (that is, powering down or up of mate unit)

2. Analyze bits 4, 5, 6 in CREG 3 register as one bit (starting with bit 4) and try to resolve error using duplex path

3. Analyze bits 7, 8, 12 (starting with bit 12) as in Step 2 except that resolution internal or external to the unit cannot be made (suspect clock problems in attached unit, power sequencer, etc)

4. Resolution of a TSWF (bit 11) to the determination of which side contains the error should not be attempted

5. Try to determine why unit is simplexed and if error is related to simplexed condition

6. Use ERAP data to determine if a pattern exists

7. Use TABLE A (TSI-A), Page 2 or TABLE B (TSI-B) page 3 for additional information (bits set to one in CREG 3)

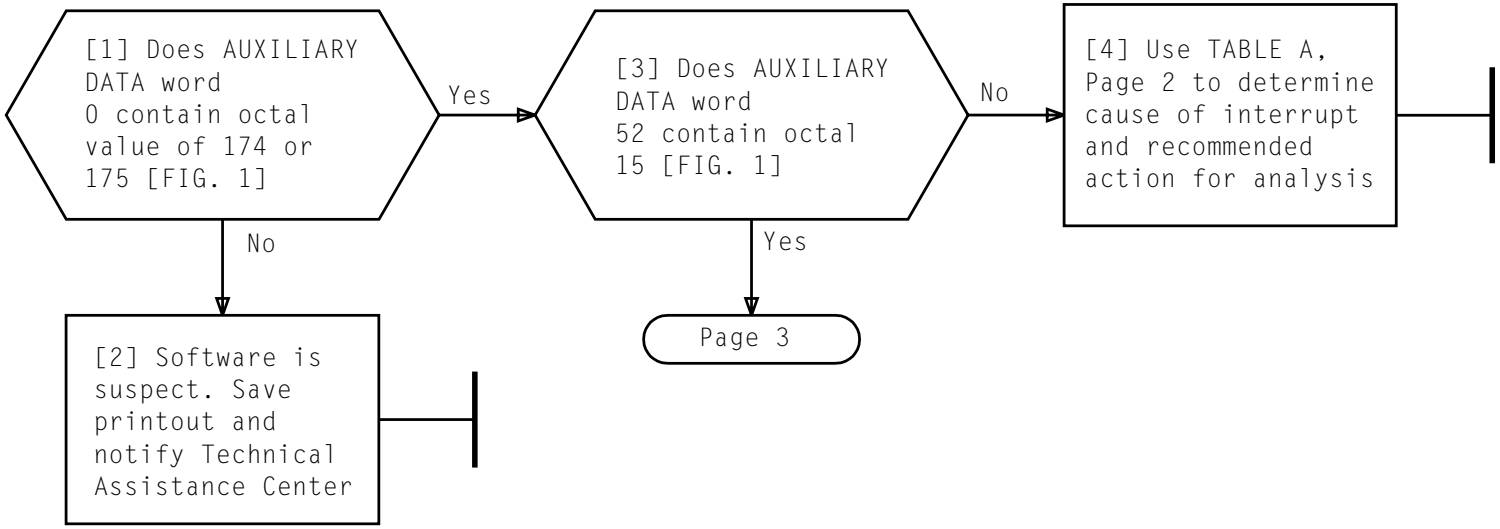
F-LEVEL INTERRUPT, SIMPLEXED TSI STRATEGY

TABLE A
TSI A BIT IDENTIFICATION APUF, CREG 3)

BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION
0	CE	CCESTRCO	4A023	4/1	Internal clock error. Suspect clock circuit
1	TSSC	ERESTSCO	4A023	5/3	Time slot sequence check. Suspect time slot counter circuit
2	TSCMM	METRCMMO	4A023	4/1	Time slot counter mismatch
3	CMM	ETRCMMO	4A023	4/1	Clock mismatch. Suspect clock match circuit or mate controller
4	RTMP	0EPRRO | 7EPRRO	4A024	11/1 | 11/8	Receive time slot memory (TSM) parity failure
5	TTMP	0ERTPO | 7ERTPO	4A024	17/1 | 17/8	Transmit TSM parity failure
6	BIMP	ERMPO	4A024	23/5	Busy idle map memory (BIMM) parity failure
7	BMAPF	0ERPHAO 1ERPHAO 2ERPHAO 3ERPHAO 4ERPHAO 5ERPHAO 6ERPHAO 7ERPHAO	4A024	5/1 5/1 5/2 5/2 5/4 5/4 5/5 5/5	Buffer memory A parity failure
8	BMBPF	0ERSPO | 7ERSPO	4A024	8/1 | 8/8	Buffer memory B parity failure
9	—	—	—	—	Not used
10	TRPF	0EPLOO | 7EPLOO	4A024	20/1 | 20/8	Transmission parity failure
11	TSWF	0EBTO 1EBTO 2EBTO 3EBTO 4EBTO 5EBTO 6EBTO	4A024	25/5 25/5 25/6 25/6 25/7 25/7 25/8	Transmit seems well failure
12	RSWF	0ERBO | 6ERBO	4A024	1/1 | 1/7	Receive seems well failure. Suspect VIU/ DTU failure or receive box failure
13	RMM	0ECOLO | 4ECOLO	4A024	6/1 | 6/5	Receive mismatch. Suspect: 1. decorrelator or buffer A 2. mismatch circuit 3. mate controller
14	TMM	0ECRO | 4ECRO	4A024	24/1 | 24/5	Transmit mismatch. Suspect: 1. decorrelate circuit 2. match circuit 3. mate controller
15	SSWF	ECLKO	4A023	9/1	Suspect clock circuit

TABLE B
TSI B BIT IDENTIFICATION (APUF, CREG 3)

BIT	NAME	LEAD(S)	SD	FS/SYMBOL	IMPLICATION
0	CE	(Internal)	4A085	16/1	Twisted Ring Counter Error.
1	TSSC	ETSCPTYO	4A085	17/1	Time slot sequence check. Suspect time slot counter circuit.
2	—	—	—	—	Not Used
3	TRCMM	TTRCOM TTRCIM (From mate)	4A085	16/1	Twisted ring counter mismatch. Suspect clock match circuit or mate controller.
4	RTSMPF	ERMEMPO	4A084	2/1-8	Receive time slot memory (TSM) parity failure.
5	TTSMPF	ETMEMPO	4A084	6/1-8	Transmit TSM parity failure.
6	BIMMF	EBIMMO	4A084	7/1	Busy/Idle map memory parity failure.
7	BMAPF	ODSBMAO | 7DSBMAO	4A084	12/1-8	Buffer memory A parity failure.
8	BMBPF	ERBMPO	4A084	2/1-8	Buffer memory B parity failure.
9	—	—	—	—	Not Used.
10	TRPF	ETRPFO	4A084	5/1-4	Leading one detector parity failure.
11	TSWF	ETSWFO	4A084	14/1-8	Transmit seems well failure.
12	RSWF	ERSWO	4A084	11/1,3, 5,6,9, 11,13,15	Receive seems well failure. Suspect VIU/DTU failure or receive box failure.
13	RMM	EBMMTCHO	4A084	2/1-8	Receive mismatch. Suspect: 1. Decorrelator buffer A and same port receiver. 2. Mismatch circuit and receiver. 3. Mate controller.
14	TMM	ETMMO	4A084	8/1	Transmit mismatch. Suspect: 1. Decorrelator circuit. 2. Match circuit. 3. Mate controller.
15	—	—	—	—	Not Used



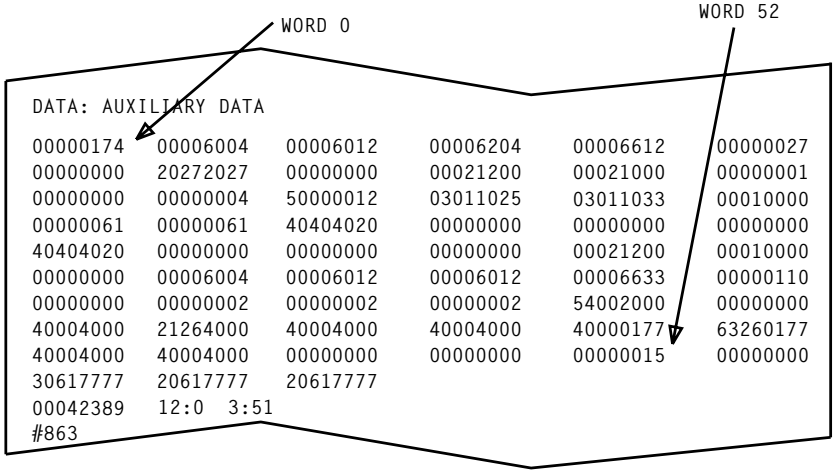


FIG. 1 - AUXILIARY DATA Registers

ANALYZE TNFR F-LEVEL INTERRUPT TRPF FAILURE, TIME SLOT INTERCHANGE/TIME MULTIPLEXED SWITCH

TABLE A PATH RESULTS		
AUX DATA WORD 52 VALUE	**ERROR DESCRIPTION**	**RECOMMENDED ACTION**
0	T-TSI routing failure	Run diagnostics on suspect TSI — should result in STF (if not, notify SMCC, TAC, PECC)
1	TTSI no data	Suspect Leading One Detector or TTSM register associated with the failing level.
3	T-TSI data mismatch	Contact Technical Assistance Center
5	TMS mismatch failure	
6	TMS software	
7	R-TSI duplex failure	
12	R-TSI data mismatch	
13	R-TSI software error	
14	R-TSI network mismatch	
4	TMS access failure	Run diagnostic on suspect unit; should result in STF. This TRPF is first indication that a unit has stopped working
10	R-TSI access failure	
11	R-TSI routing failure	Same as for value 0 above
16	TMS duplex failure	Contact Technical Assistance Center

See NOTE 1.

[5] Using AUXILIARY DATA words 5, 11, 17, 29, 51 [FIG. 2] and TABLE B, determine TRPF path data

[6] Use TABLE C and AUXILIARY DATA word 51 to identify controllers involved in TRPF path

[7] Use ISDs, SDs, or ERAP to isolate TRPF and identify suspect circuit packs

AND

```
A 14 REPT: F-LEVEL @14204313 MFNUM=00135364 MICON=00000020
     LV=0040 D0=00000000 D1=04000000 D2=00000037 D3=00000000
     DATA: INTERRUPT SOURCE DATA
     00002640  00000000 01402000 00000020 00000020
     DATA: FAULT RECOGNITION ISOLATION DATA
     00000030 00000001 00000241 00000001 00000014 00000000
     DATA: ERROR ANALYSIS STRATEGY DATA
     04026344 00000004 00000004 00000030 00000004 00000000
     00000000
     DATA: AUXILIARY DATA                                    AUX DATA WORDS
     00000174 00002004 00006012  00002004 00006012 20101166  5
     00000003 25662566 00000000  00021204 00021002 02000104 11
     00000000 50000004 00000012  03011025 03011033 02041000 17
     00000064 00000064 23402640  40614031 40404020 00000000
     23402640 40615031 40404020  00000000 00021242 21045027 29
     00000000 00002004 00006012  00002025 00006033 00000110
     00000000 00000002 00000002  01402000 01402000 00000000
     01772622 01770177 64270177  01770177 01772622 01770177
     64270177 01770177 00000000  00000052 00000015 00000052 53
     30617777 20617777 20617777
     032889   12:12:51                                  51
     #938
```

FIG. 2 - Auxiliary Data Registers

TABLE B
TRPF PATH DATA

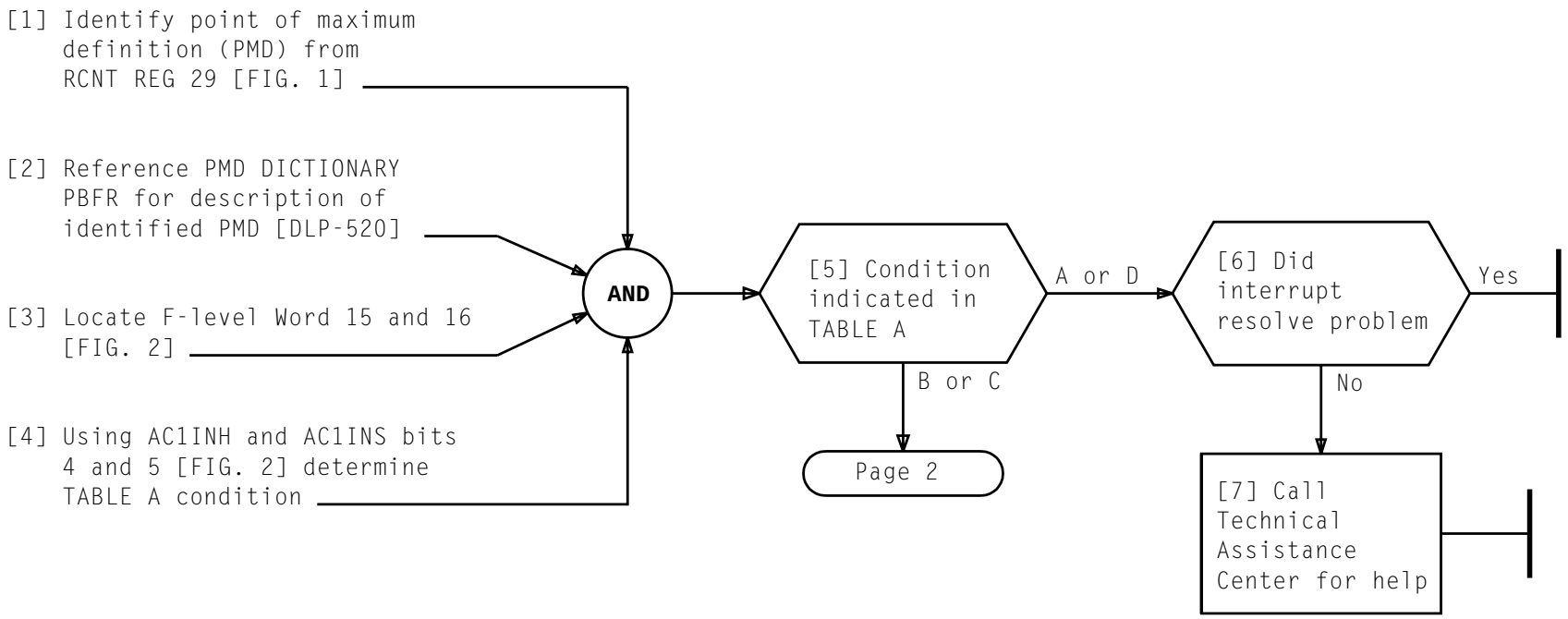
AUX DATA REGISTER	HARDWARE PATH					
	CHANNEL	LEVEL	SPC	MEMN	TERMINATING SWITCH LEVEL	
05 (T-TSI)	Bits 0-6	Bits 9-11	Bit 12	Bits 13-18	Bits 21-23	ISD-133
11 TMS ST2	B-LINK	A-LINK		SWITCH	TMSP	
	Bits 0-3	Bits 6-9		Bits 12-15	Bits 19,18	
17 TMS ST1	Bit layout is same as ST2SW					
29 (R-TSI)	CHANNEL	LEVEL	SPC	MEMN	ORIGINATING SWITCH LEVEL	
	Bits 0-6	Bits 9-11	Bit 12	Bits 13-18	Bits 21-23	ISD-134

TABLE C
AUX DATA 53

	T-TSI	TMS	R-TSI
	BITS SET TO ONE		
CONTR 0	Bit 0	Bit 2	Bit 4
CONTR 1	Bit 1	Bit 3	Bit 5

NOTE 1
ISD applies to TSI-B only

ANALYZE TNFR F-LEVEL INTERRUPT TRPF FAILURE, TIME SLOT INTERCHANGE/TIME MULTIPLEXED SWITCH




```
ERROR ANALYSIS RECENT HISTORY TABLE
00241030 10401630 00000000 00000000 00000000 00000000
00000003 00000001 00010000 77777776 00000000 00000001
30602040 00000000 40001604 00000002 00000003 00000000
00000000 00000044 00000052 00000004 00000012 00241030
00402040 00000000 00000000 00000000 00076010 20000201
00025673 00025673 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 00000000
00100001 00011702 00000101 00000000 00000000 00000000
00000000 00000000 03471371 00000000 00000001 00000000
04000151 00000000 10000252 00000000 00000000 00000000
00000000 00000000 00000000 20637777
123088  02:02:33
#247
```

PMD NUMBER

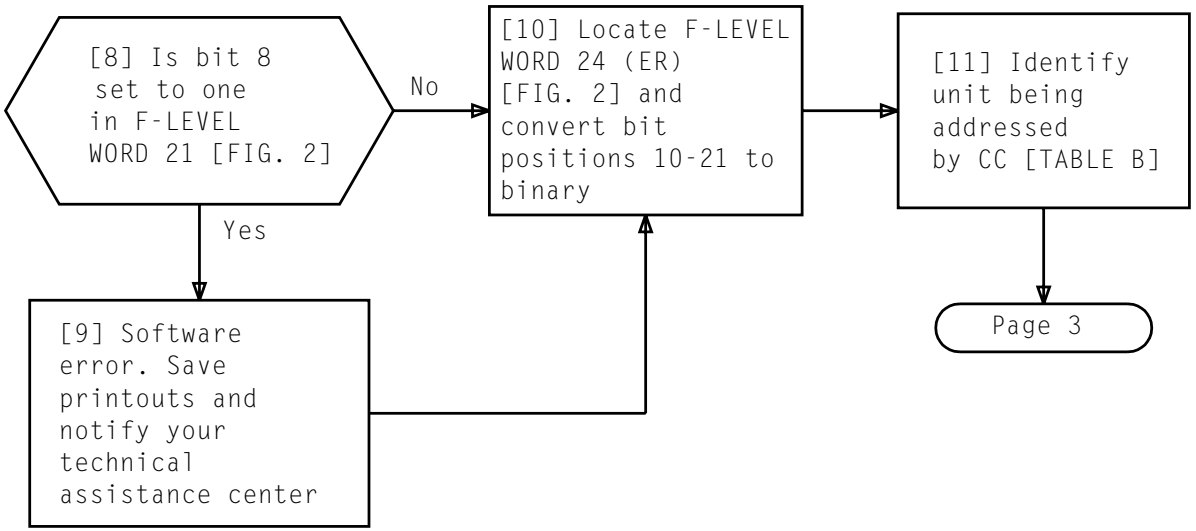
FIG. 1 - RCNT Register Printout

TABLE A

AC1INH		AC1INS		CONDITION
BIT 4	BIT 5	BIT 4	BIT 5	
0	DC	1	0	A
0	0	1	1	B
1	0	DC	1	C
0	1	1	DC	D

DC = Don't Care

ANALYZE PBFR F-LEVEL INTERRUPT



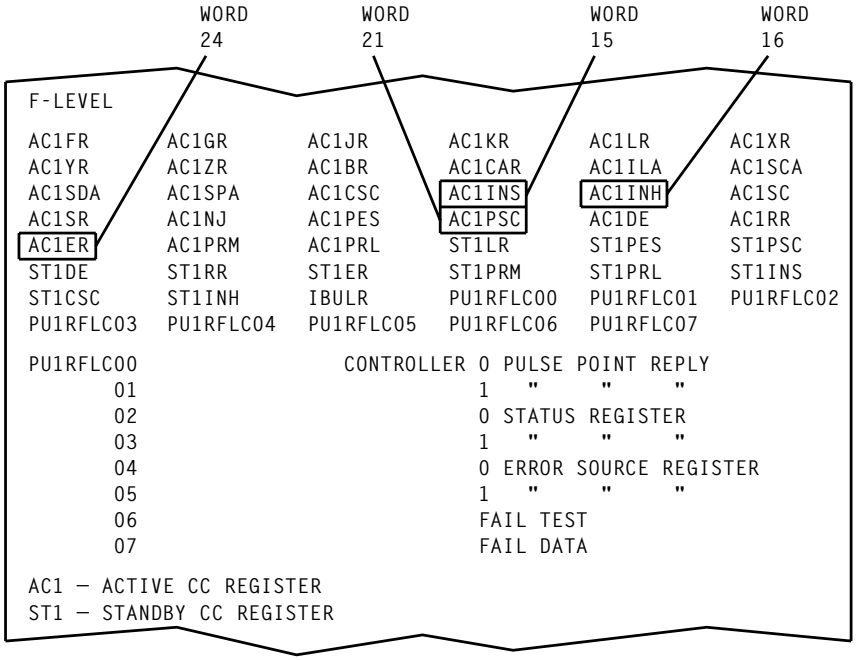


FIG. 2 — CC Register Layout

TABLE B — E-REGISTER LAYOUTS

BITS →	21	20	19	18	17	16	15	14	13	12	11	10
MCC	0	0	0	0	1	1	1	1	0	1	1	0
SP/DIF	0	0	0	1	0	Member number						MTX
SCLK	0	0	0	1	1	Member number						
TMS	0	0	1	0	0							MEM NO
TSI	0	0	1	0	1	Member number						SPC
TGR	0	0	1	1	0	Member number						
IOUS	0	0	1	1	1	Member number				IOUC		
EST	0	1	0	0	1	Member number						
SCS	0	1	0	1	1	Member number			SCU number			
BITS →	21	20	19	18	17	16	15	14	13	12	11	10

ANALYZE PBFR F-LEVEL INTERRUPT

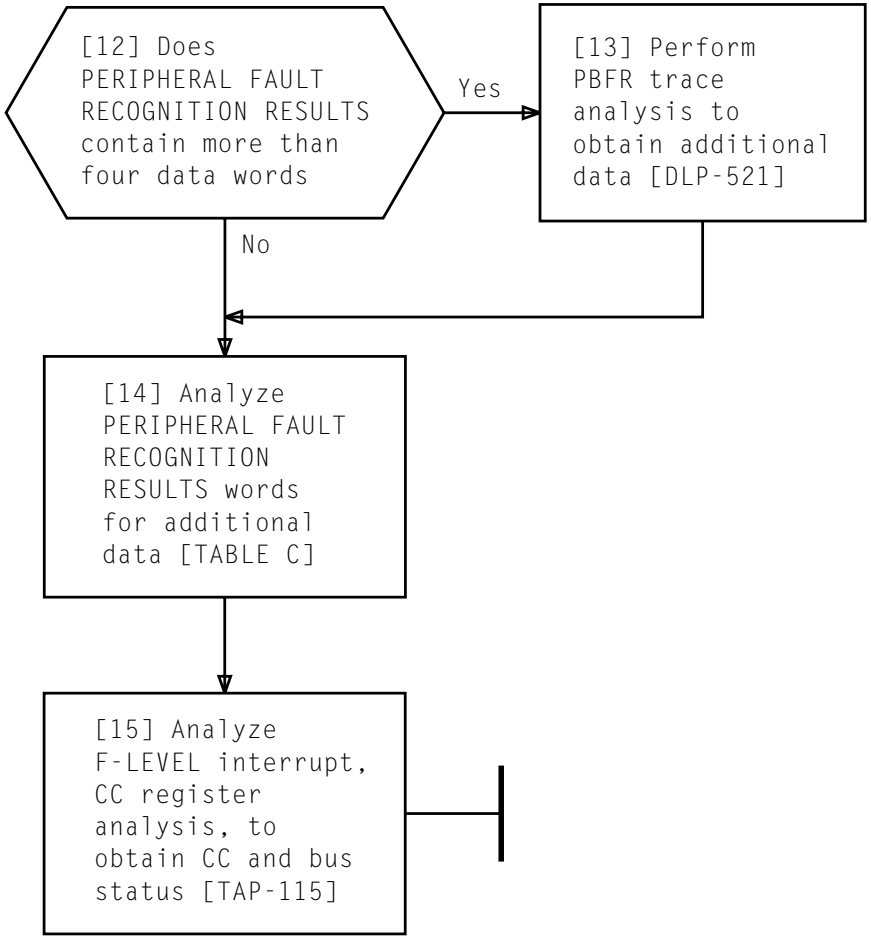


TABLE C
PERIPHERAL FAULT RECOGNITION RESULTS

IDENTIFICATION OF REGISTERS IN RESULTS TABLE OF F-LEVEL MESSAGES

PU4RESULT PU4UTMNO PU4FRPMD PU4FRJRG

PU4RESULT ----------NMLKJIHGFEDCBA

BIT		
	0	A = CC0 found faulty
	1	B = CC1 found faulty
	2	C = Controller 0 found faulty
	3	D = Controller 1 found faulty
	4	E = PU bus 0 found faulty
	5	F = PU bus 1 found faulty
	6	G = PU bus 0 at unit found faulty
	7	H = PU bus 1 at unit found faulty
	8	I = Faulty unit or subunit to be removed and diagnosed
	9	J = Faulty unit or subunit to be removed
	10	K = Fault recognition was unable to find the fault
	11	L = Fault recognition found that a software error caused the F-level
	12	M = Fault recognition found that a transient caused the F-level
	13	N = Signal processor matrix found faulty

PU4UTMNO DDDDDDDCCCCCCCBAAAAAAA--

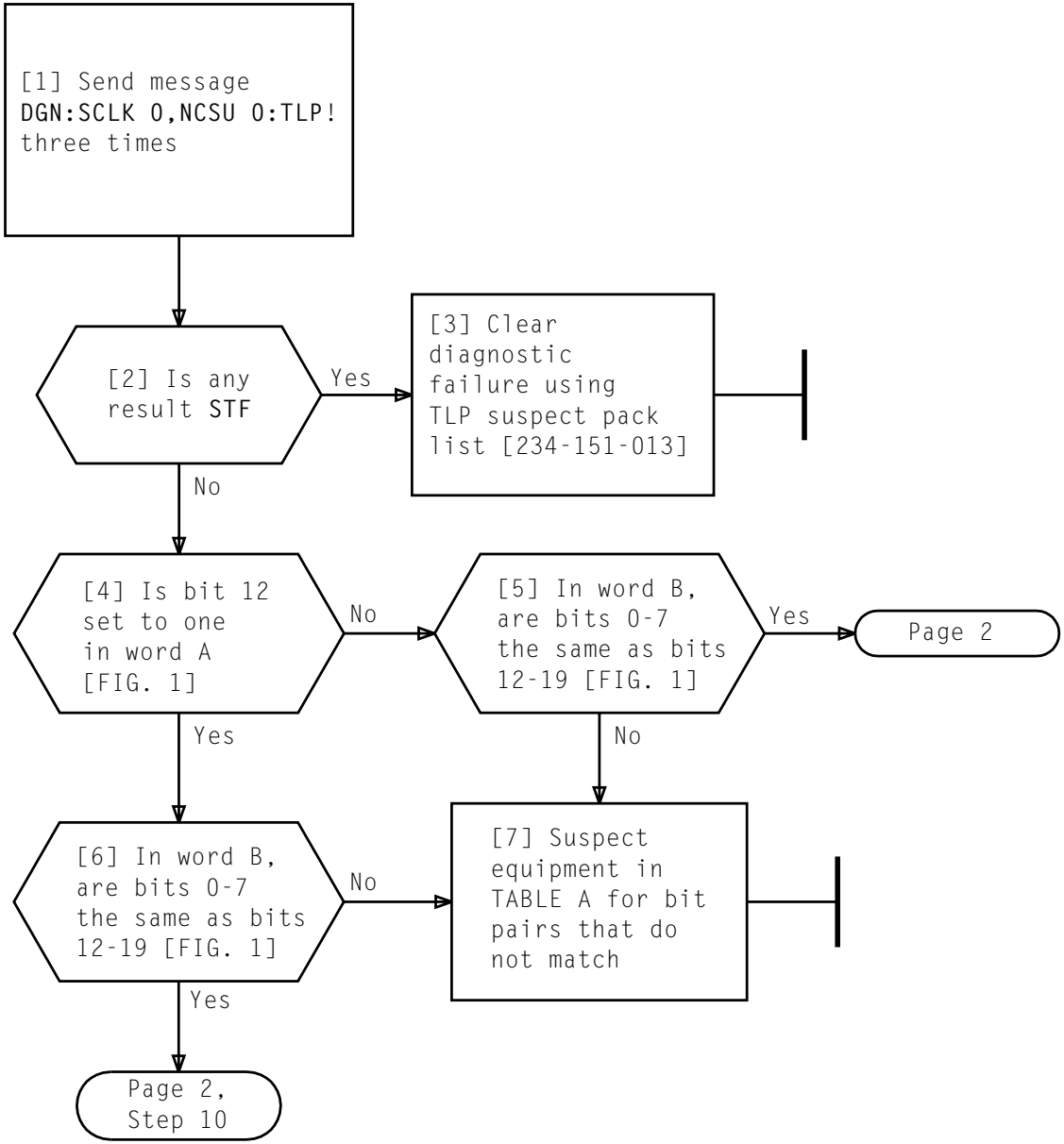
BIT		
	2-8	A = Submember found faulty (if any)
	9	B = Set if submember found faulty
	10-16	C = Member number found faulty
	17-23	D = Unit type found faulty

PU4FRPMD --CCCCCCCBBBBBBBAAAAAAA

BIT		
	0-7	A = Point of Maximum Definition MACRO number relative to an FR program
	8-14	B = Fault recognition decision code
	15-21	C = Error analysis action code

PU4FRJRG = FR program address where error was located

ANALYZE PBFR F-LEVEL INTERRUPT



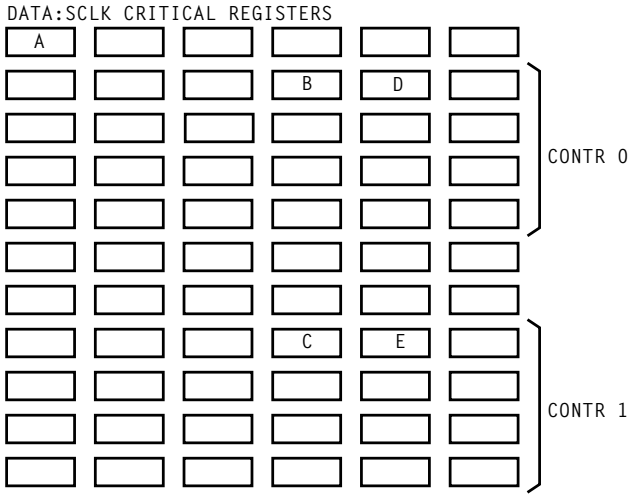
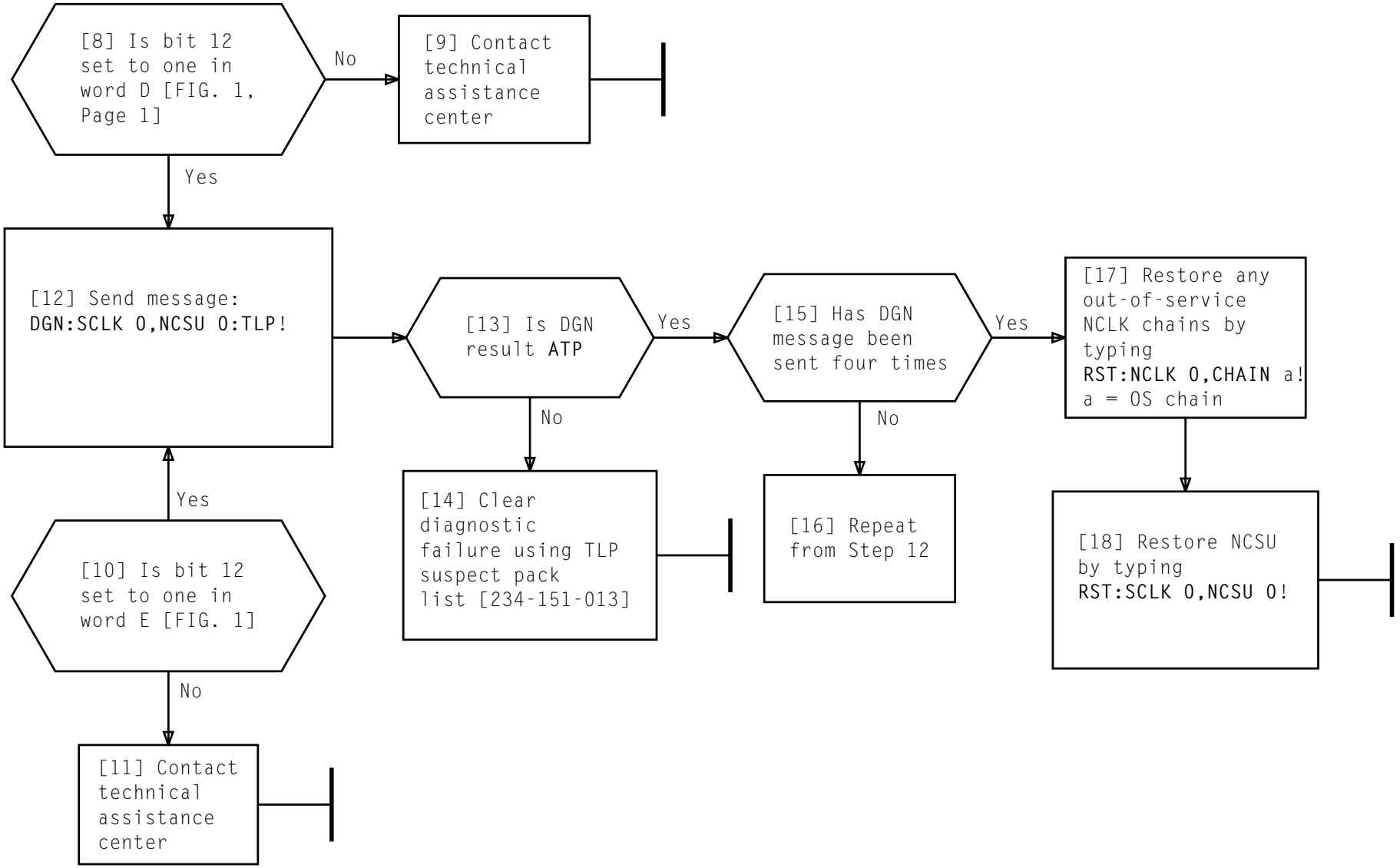


FIG. 1 — Part of Base Level Printout

TABLE A
BASE 0 ESR (WORD B)

BIT PAIR	BIT DESCRIPTION	SUSPECT EQUIPMENT
0,12	Oscillator out of range	Suspect NCLK oscillator indicated. Clear phase error [234-151-013]. If more than one oscillator indicated, suspect lower numbered oscillator first
1,13	Oscillator 0	
2,14	Oscillator 1	
2,15	Oscillator 2	
4,16	Oscillator 3	
5,17	BSRF outage	Office timing reference outage
6,18	DS1A outage	
7,19	DS1B outage	

ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) BASE LEVEL INTERRUPT



ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) BASE LEVEL INTERRUPT

[1] Using FIG. 1, identify suspect controller from TEXT HEADER

[2] Using FIG. 1, obtain Point of Maximum Definition (PMD) from DATA:ERROR ANALYSIS RECENT HISTORY TABLE WORD 29

[3] Define PMD dictionary nodes to obtain description of software analysis and action taken [DLP-522]

[4] Using FIG. 1 and TABLE A, determine frame mode of operation; that is, SIMPLEX, DUPLEX

AND

Page 2

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A 12 REPT: F-LEVEL  @14703410 MFNUM=00001336 MICON=00000020     COMPLETED
     LV=0040 D0=00000000 D1=60020000 D2=00000000 D3=00000000
     VCFR RESTORED VIF 1 VIU 3                          <- SUSPECT UNIT
     DATA:  F-LEVEL
     00100025 07210003 14450162 45710325 00000300 00000040
     00000012 14703410 03270062 14703410 00000040 14450216
     00004012 14703410 02026102 00000020 07210003 00000000
     16305272 04001000 00010000 00000000 60000000 00000000
     01402000 00002700 00000000 00000300 00010000 00000000
     60000000 00000000 01402000 00002700 00000000 00000020
     02025102 07210003 00000300 00000000 00000000 00000000
     00000000 00000000 00000000 00000000 00000000
     DATA:  VIF CRITICAL REGISTERS
CREG 0 ->    00210047 00206004 00000000 00000000 00000000 00000000
     00000000 00006007 00100010 00177777 00004000 00003503
CREG 12/13
CONTROLLER 0 -> 00000000 00000000 00000000 00000000 00000000 00000000
CREG 1 ->    00000000 00006007 00000411 00000000 00004000 00003746
CREG 12/13
CONTROLLER 1 -> 00000000 00000204 00000400 00000150 00000000 00000000
     DATA:  PERIPHERAL FAULT RECOGNITION RESULTS
     00000000 00000000 00000023 10121656
     DATA:  ERROR ANALYSIS RECENT HISTORY TABLE
     04605403 27000601 00000000 00000000 00000000 00000000
     00006103 00000400 00000002 00000300 00040004 50050406
     20444140 00000000 00001604 00000000 00000000 00002204
     00000000 00000411 00000000 00206004 00210047 04505403
     00044140 00000000 00000000 00000000 00110010 20000023   <- PMD
     00001336 00001336 00000003 00000000 00000000 00000000
     00000000 00000000 00000000 00000000 00002403 00000000
     00100004 00010002 00000101 00000000 00000000 00000010
     00000000 00000000 35363321 00000000 00000001 00000000
VIU ERROR
SOURCE
REGISTERS -> 00000000 00000000 00000000 20000000 00000000 00000000
     00000000 00000000 00031520 00000000
     07/14/79  08:11:51
     #514
```

FIG. 1 – VIF Interrupt Printout

TABLE A			
	CREG 0	CREG 1	MODE OF OPERATION
State of bit 12	0	0	FRAME is DUPLEXed
	0	1	Controller 1 is OOS
	1	0	Controller 0 is OOS
	1	1	DUPLEX FAILURE

ANALYZE VCFR, F-LEVEL INTERRUPT

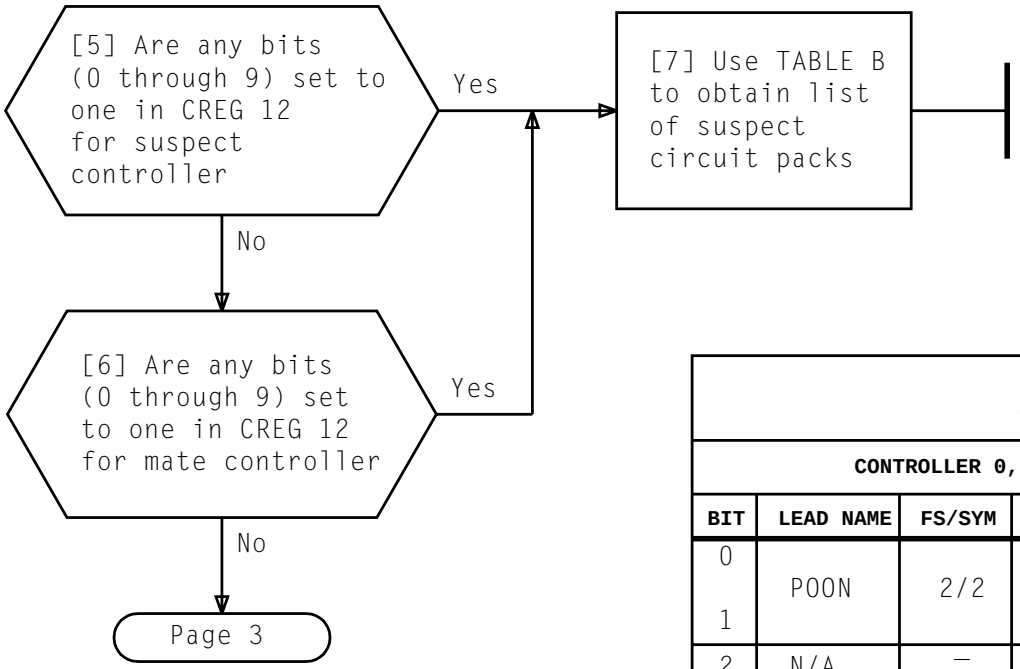
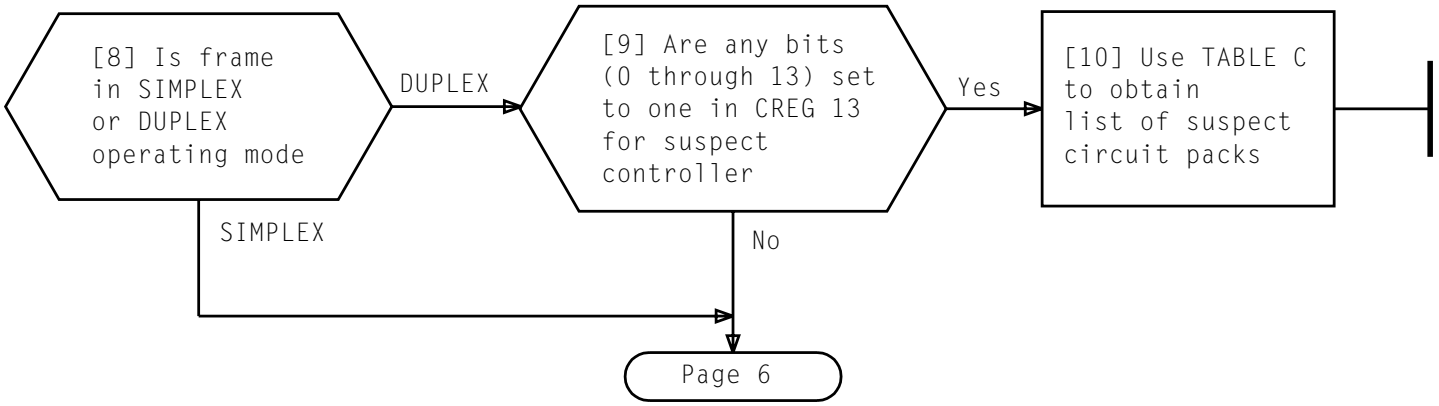


TABLE B
CREG 12 CIRCUIT PACKS — (SD56158-01)

CONTROLLER 0, ESR BITS				CONTROLLER 1, ESR BITS			
BIT	**LEAD NAME**	**FS/SYM**	**SUSPECT PACK/LOC**	**BIT**	**LEAD NAME**	**FS/SYM**	**SUSPECT PACK/LOC**
0 1	P0ON	2/2	FA741 @ 148-11 FA740 @ 148-12 FA742 @ 148-05	0 1	P01N	2/5	FA741 @ 148-26 FA740 @ 148-25 FA742 @ 148-32
2	N/A	—		2	N/A	—	
3	00FN0	8/2	FA747 @ 144-08 FB481 @ 144-07 FA748 @ 144-09	3	00FN1	8/6	FA747 @ 144-29 FB481 @ 144-31 FA748 @ 144-28
8	CC0N0			8	CC0N0		
4	TC0N	12/1	FA754 @ 156-12	4	TC0N	12/1	FA754 @ 156-12
5	TC1N	12/2	FA754 @ 156-13	5	TC1N	12/2	FA754 @ 156-13
6	TC2N	12/3	FA754 @ 156-14	6	TC2N	12/3	FA754 @ 156-14
7	TC3N	12/4	FA754 @ 156-15	7	TC3N	12/4	FA754 @ 156-15
9	CC1N0	8/4	FA748 @ 144-09 FA747 @ 144-08 FA481 @ 144-07	9	CC1N1	8/8	FA748 @ 144-28 FA747 @ 144-29 FA481 @ 144-31

ANALYZE VCFR, F-LEVEL INTERRUPT



ANALYZE VCRF, F-LEVEL INTERRUPT

TABLE C
CREG 13 CIRCUIT PACKS — (SD-5G158-01)

CONTROLLER 0, ESR BITS				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
0	MMICFN0	8/3	INDICATOR CHECK FRAME MISMATCH	FA749 @ 144-10 FA748 @ 144-09 FA747 @ 144-08
1	MMESMN0	2/2	MISMATCH ENABLE SELECT MODE ON INPUT REGISTER	FA741 @ 148-11 FA740 @ 148-12
2	MMREPN0	6/1	INPUT TO REPLY REGISTER MISMATCH	FA760 @ 152-18 FS 2, 3, 13 PACKS
3	MMMUXN0	11/5	INDICATOR MULTIPLEXER MISMATCH	FA757 @ 144-14 FA756 @ 144-17 FA756 @ 144-18 FA756 @ 148-17 FA756 @ 148-18
4	MMSMN0	11/5	STATUS MEMORY MISMATCH	FA757 @ 144-14 FA758 @ 144-16 *FA758 @ 144-21 FS 3 PACKS
5 6	MMP10 MMP20	10/2	VIU CONTROL BUFFER PARITY VIOLATION 1, VIOLATION 2	FA753 @ 148-03 *FA753 @ 148-34 FA747 @ 144-08
7	MMPSLN0	6/1	PROTECTION SWITCH LOGIC FUNCTION CODE MISMATCH	FA760 @ 152-18 FA755 @ 148-06 *FA755 @ 148-31

CONTROLLER 0, ESR BITS (Contd)				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
8	MMDSGN0	9/3	DIGITAL SIGNAL GENERATOR MISMATCH	FA750 @ 144-12 *FA750 @ 144-25 FA748 @ 144-09 FA749 @ 144-10
9	RRPEN0	4/1	REPLY REGISTER PARITY VIOLATION	FA744 @ 152-17 FA745 @ 152-16
10	MM11BN0	6/1	ERROR SOURCE REGISTER MISMATCH	FA760 @ 152-18 FA743 @ 148-07 FS 3 PACKS
11	POON	2/2	REMOTE INPUT PARITY VIOLATION	FA741 @ 148-11 FA740 @ 148-12 FA742 @ 148-05 *FA741 @ 148-26
12	CCON0	8/2	REMOTE TIMING RECEIVER CODE VIOLATION	FA747 @ 144-08 FA481 @ 144-07 FA748 @ 144-09 FA741 @ 144-11
13	CC1N0	8/4	REMOTE FRAME COUNTER VIOLATION	FA748 @ 144-09 FA747 @ 144-08 FA749 @ 144-10

* This pack is in Controller 1

TABLE C
CREG 13 CIRCUIT PACKS — (SD-5G158-01) (Contd)

CONTROLLER 1, CREG 13 ESR BITS				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
0	MMICFN1	8/7	INDICATOR CHECK FRAME MISMATCH	FA749 @ 144-27 FA748 @ 144-28 FA747 @ 144-29
1	MMESMN1	2/5	MISMATCH ENABLE SELECT MODE ON INPUT REGISTER	FA741 @ 148-26 FA740 @ 148-25
2	MMREPN1	6/2	INPUT TO REPLY REGISTER MISMATCH	FA760 @ 152-19 FS 2, 3, 13 PACKS
3	MMMUXN1	11/13	INDICATOR MULTIPLEXER MISMATCH	FA757 @ 144-23 FA756 @ 144-19 FA756 @ 144-20 FA756 @ 148-19 FA756 @ 148-20
4	MMSMN1	11/13	STATUS MEMORY MISMATCH	FA757 @ 144-23 FA758 @ 144-21 *FA758 @ 144-16 FS 3 PACKS
5 6	MMP11 MMP21	10/4	VIU CONTROL BUFFER PARITY VIOLATION 1, VIOLATION 2	FA753 @ 148-34 *FA753 @ 148-03 FA747 @ 144-08
7	MMPSLN1	6/2	PROTECTION SWITCH LOGIC FUNCTION CODE MISMATCH	FA760 @ 152-19 FA755 @ 148-31 *FA755 @ 148-06

CONTROLLER 1, CREG 13 ESR BITS (Contd)				
BIT	LEAD NAME	FS/SYM	ERROR IDENTIFICATION	SUSPECT PACK/LOC
8	MMDSGN1	9/6	DIGITAL SIGNAL GENERATOR MISMATCH	FA750 @ 144-25 *FA750 @ 144-12 FA748 @ 144-28 FA749 @ 144-27
9	RRPEN1	4/3	REPLY REGISTER PARITY VIOLATION	FA744 @ 152-20 FA745 @ 152-21
10	MM11BN1	6/2	ERROR SOURCE REGISTER MISMATCH	FA760 @ 152-19 FA743 @ 148-30 FS 3 PACKS
11	PO1N	2/5	REMOTE INPUT PARITY VIOLATION	FA741 @ 148-26 FA740 @ 148-25 FA742 @ 148-32 *FA741 @ 148-11
12	CCON1	8/6	REMOTE TIMING RECEIVER CODE VIOLATION	FA747 @ 144-29 FA481 @ 144-31 FA748 @ 144-28 FA741 @ 741-26
13	CC1N1	8/8	REMOTE FRAME COUNTER VIOLATION	FA748 @ 144-28 FA747 @ 144-29 FA749 @ 144-27

* This pack is in Controller 0

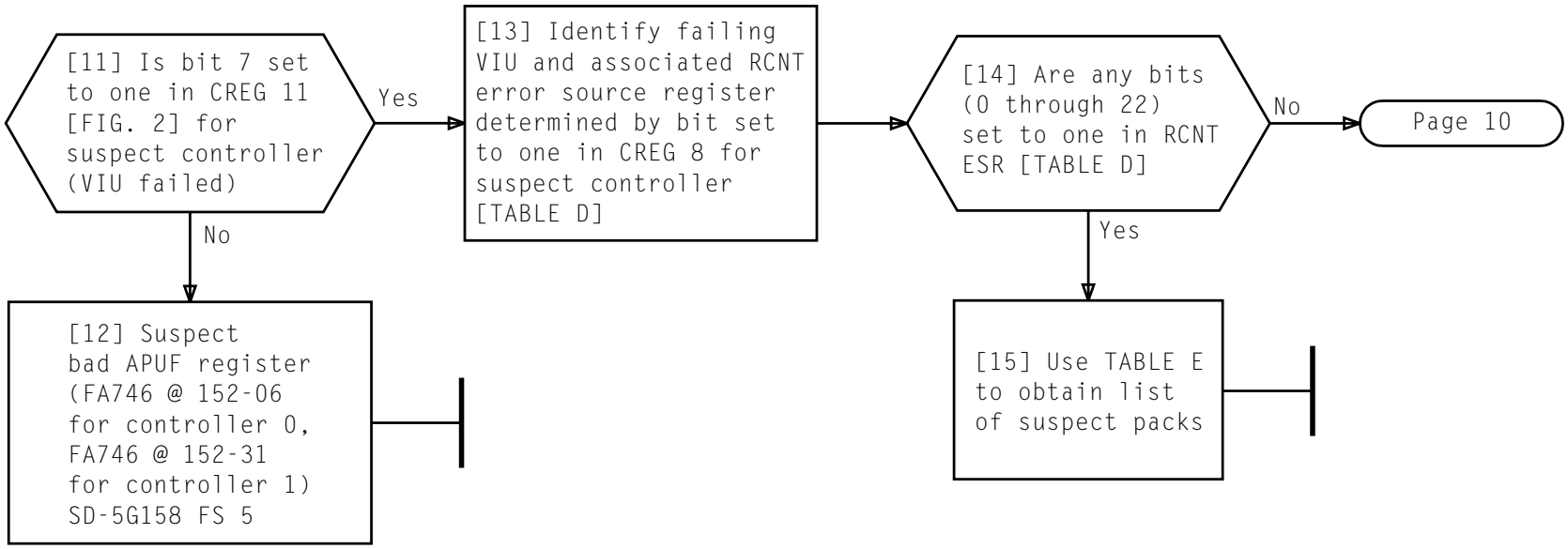


TABLE D

CREG 8 SET BIT	FAILING VIU	ASSOCIATED ERROR SOURCE REGISTER
0	0	RCNT+54
1	1	RCNT+55
2	2	RCNT+56
3	3	RCNT+57
4	4	RCNT+58
5	5	RCNT+59
6	6	RCNT+60
7	7	RCNT+61

ANALYZE VCFR, F-LEVEL INTERRUPT

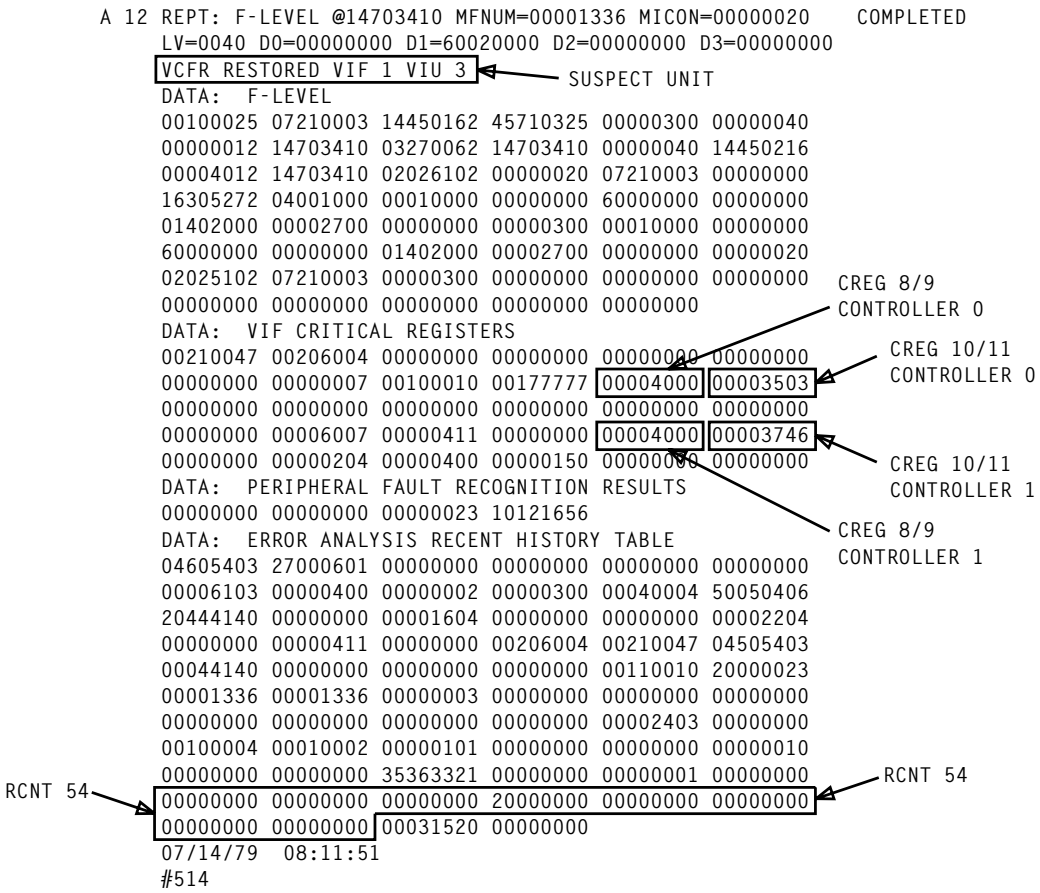


FIG. 2 — VIF Interrupt Printout

ANALYZE VCFR, F-LEVEL INTERRUPT

TABLE E
RCNT+54 THROUGH RCNT+61 (SD-5G157)

SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC
0	S3	7/2	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 125	JA3 @ 09-02 JA6 @ 09-03 JA7 @ 09-25 JA5 @ 09-26 JA4 @ 09-29 FA724 @ 03-19 FA731 @ 09-11
1	S2	7/1	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 127	JA3 @ 09-02 JA6 @ 09-03 JA7 @ 09-25 JA5 @ 09-26 JA4 @ 09-30 FA724 @ 03-19 FA723 @ 15-11 FA731 @ 09-11
2	S1	7/2	SIGNAL ALARM IN BLOCK CONTAINING TRUNK 126	JA3 @ 09-04 JA6 @ 09-05 JA7 @ 09-27 JA5 @ 09-28 JA4 @ 09-29 FA724 @ 03-20 FA723 @ 15-11 FA723 @ 15-13 FA731 @ 09-11
3	S0	7/1	SIGNAL ALARM IN BLOCK CONTAINING	JA3 @ 09-04 JA6 @ 09-05 JA7 @ 09-27 JA5 @ 09-28 JA4 @ 09-30 FA724 @ 03-20 FA723 @ 15-13 FA731 @ 09-11
4	P2	5/5	DECODER I/P PROCESSOR PARITY FAIL ALARM	FA726 @ 03-18 FA728 @ 03-16 FA729 @ 15-19 FA730 @ 15-17 FA731 @ 03-11 FA733 @ 03-16
5	P1	4/12	PARITY OVER DATA PASSED BETWEEN PACKS FA727, FA571, FB220	FB220 @ 15-21 FA731 @ 03-11 FA571 @ 15-17 FA727 @ 15-15 FA729 @ 15-19
6	D3	7/2	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 125	JA3 @ 09-02 JA6 @ 09-03 JA7 @ 09-25 JA5 @ 09-26
7	D2	7/1	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 127	JA3 @ 09-02 JA6 @ 09-03 JA7 @ 09-25 JA5 @ 09-26
8	D1	7/2	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 126	JA3 @ 09-04 JA6 @ 09-05 JA7 @ 09-27 JA5 @ 09-28
9	D0	7/1	HIGH DISTORTION IN BLOCK CONTAINING TRUNK 0	JA3 @ 09-04 JA6 @ 09-05 JA7 @ 09-27 JA5 @ 09-28
10	P4	6/2	CONTROL ACCESS PARITY M/M	FA732 @ 03-13 FA731 @ 03-11

ANALYZE VCFR, F-LEVEL INTERRUPT

TABLE E (Contd)
RCNT+54 THROUGH RCNT+61 (SD-5G157)

SET BIT	LEAD NAME	FS/SYM	ERROR INDICATION	SUSPECT PACK/LOC
11	P3	5/5	DECODER I/P PROCESSOR PARITY FAIL	SAME AS BIT 4
12	TRU	2/4	OUTPUT CLOCK ERROR ALARM	FA721 @ 15-22 FA729 @ 15-19 FA731 @ 03-11
13	TRL	2/5	OUTPUT CLOCK ERROR ALARM	FA721 @ 03-22 FA729 @ 15-19 FA731 @ 03-11
14	TTU	2/2	OUTPUT CLOCK ERROR ALARM	FA721 @ 15-09 FA729 @ 15-19 FA731 @ 03-11
15	TTL	2/3	OUTPUT CLOCK ERROR ALARM	FA721 @ 03-09 FA729 @ 15-19 FA731 @ 03-11
16	P6	6/1	PARITY VIOLATION (CONTROL)	FA731 @ 03-11 SD-5G156-01
17	P5	5/3	PARITY ERROR IN SERIAL/ RETIMING	FA733 @ 03-16 FA730 @ 03-17 FB480 @ 03-15
18	PWR	8/1	80A OR 81A PWR SUPPLY FAILURE	80A @ 09-08 81A @ 09-23
19	CST	2/1	STATE OF VIU CLOCK	NOT USED
20	CSO	2/1	ALARMS WHEN CLOCK SELECT AND BUFFER SWITCH FROM CONTR 0 TO 1 OR 1 TO 0	FA729 @ 15-19 FA731 @ 03-11 SD-5G156-01
21			NOT USED	
22	REF	5/2	FAILURE TO FRAME ON PCM DATA	FA733 @ 03-16 FB480 @ 03-15 FA730 @ 03-17 TSI PROBLEM, COAX PROBLEM

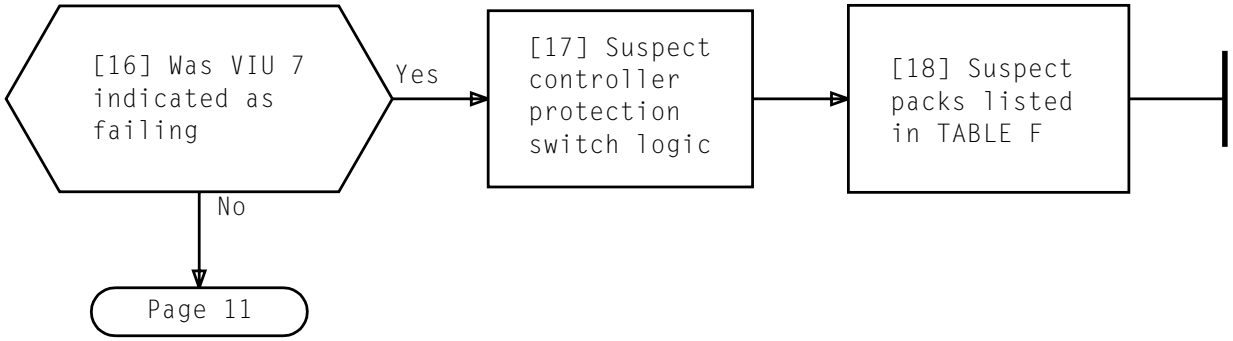


TABLE F	
CIRCUIT PACK	**LOCATION**
FA 755	148-06
FA 755	148-31
FC 195	156-21
FC 195	156-24

ANALYZE VCRF, F-LEVEL INTERRUPT

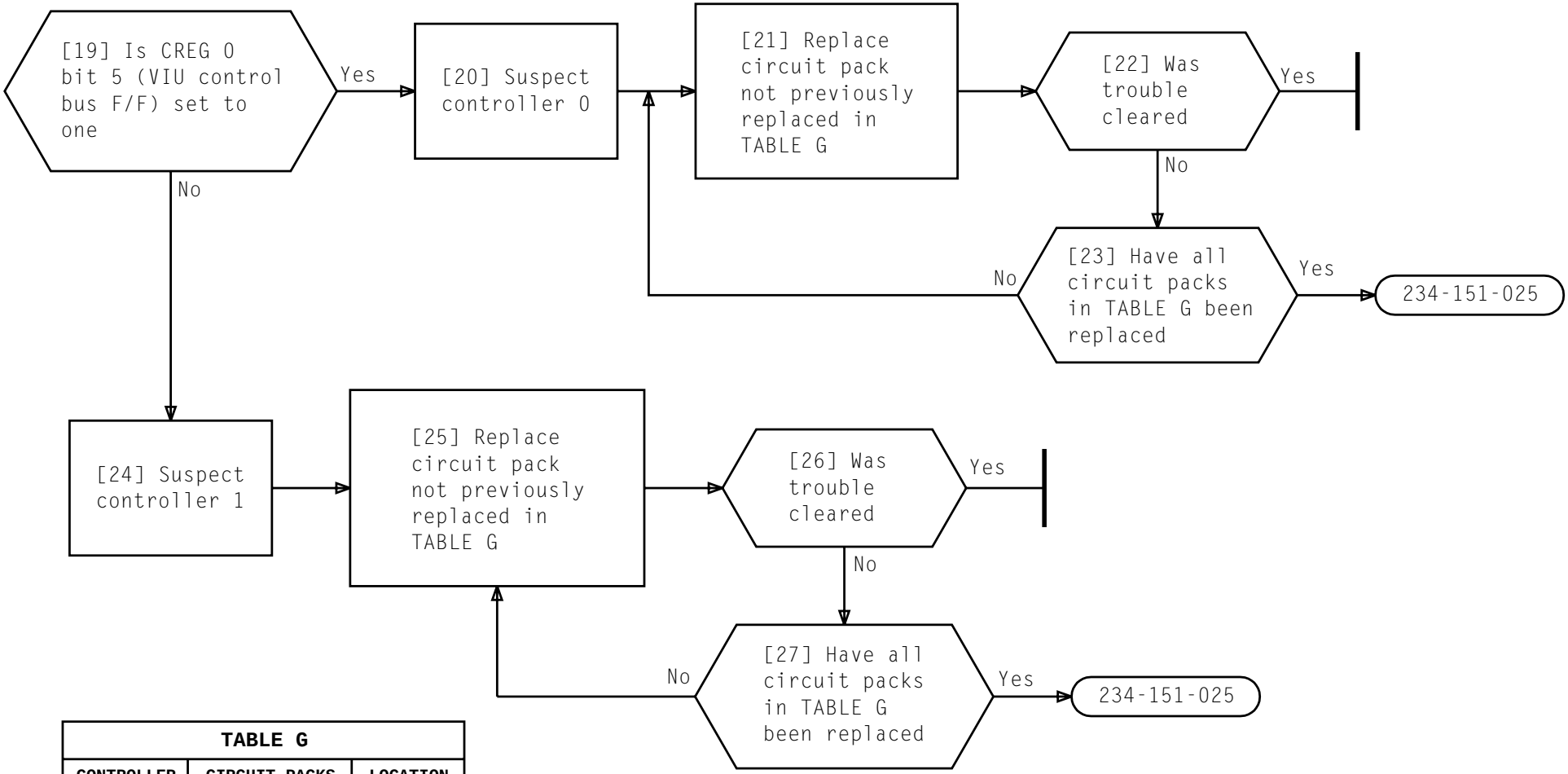


TABLE G		
CONTROLLER	**CIRCUIT PACKS**	**LOCATION**
0	FA 732	003-11
	FA 732	003-13
1	FA 731	103-11
	FA 732	103-13

ANALYZE VCRF, F-LEVEL INTERRUPT

See FIG. 1:
[1] Identify VIU where error was detected

[2] Locate and note contents of register associated with VIU where error was detected

See FIG. 2:
[3] Convert contents of associated VIU register from octal to binary

[4] Determine rightmost set bit

AND

Page 2

```
A 39 REPT: INTERJECT  @14207170 MFNUM=00001321 MICON=00000000  COMPLETED
     LVDATA=0400 SRDATA=00000000 FRDATA=60000000

     VCFR RESTORED VIF 12   VIU 4

     INTERJECT
     06020000

     PERIPHERAL FAULT RECOGNITION RESULTS
     00000000 00000000 00000036 16465532

     ERROR ANALYSIS RECENT HISTORY TABLE
     04645430 00000000 00000000 20000000 00000400 00000000
     00002003 00000400 00010000 20000000 00000000 00000000
     04146040 00000000 00001604 00000000 00000000 00000000
     00000000 00010020 00000000 00002000 00004160 04645430
     00046040 00000000 00000000 00000000 00076210 20000036
     04641321 00001321 00000024 00000000 00000000 00000000
     00000000 00000000 00000000 00000000 00000000 00000000
     00100004 00012001 00000101 00000000 00000200 00000000
     00000000 00000000 74416516 00000000 00000001 00000000
     00000000 00000000 00000000 00000000 00000014 00000000
     00000000 00000000 00000000 00000000 00000000 00000000
     07/28/88  03:39:25
     #115
```

VIU WHERE ERROR WAS DETECTED

VIU0
VIU6
VIU5
VIU
REGISTERS
VIU1
VIU7
VIU2
NOT USED
VIU3
VIU4 (FIG. 2)

FIG. 1 – VCFR Interject Printout

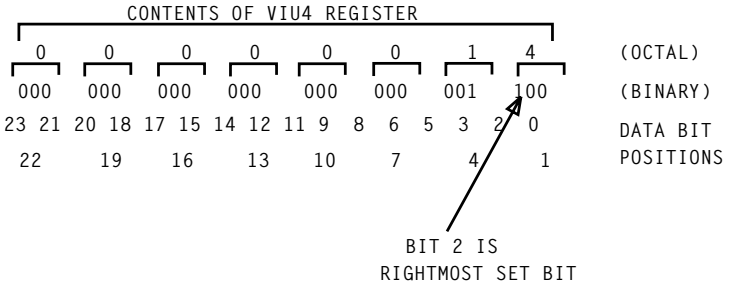
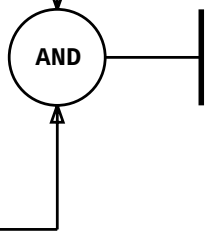


FIG. 2 - Example of Rightmost Set Bit

ANALYZE VCFR INTERJECT

[5] Determine type of error associated with rightmost set bit [TABLE A]



[6] Locate type of error in TABLE B. Identify and list all associated suspect circuit packs [NOTES 1 and 2]

TABLE A
TYPE OF ERROR PER BIT POSITION

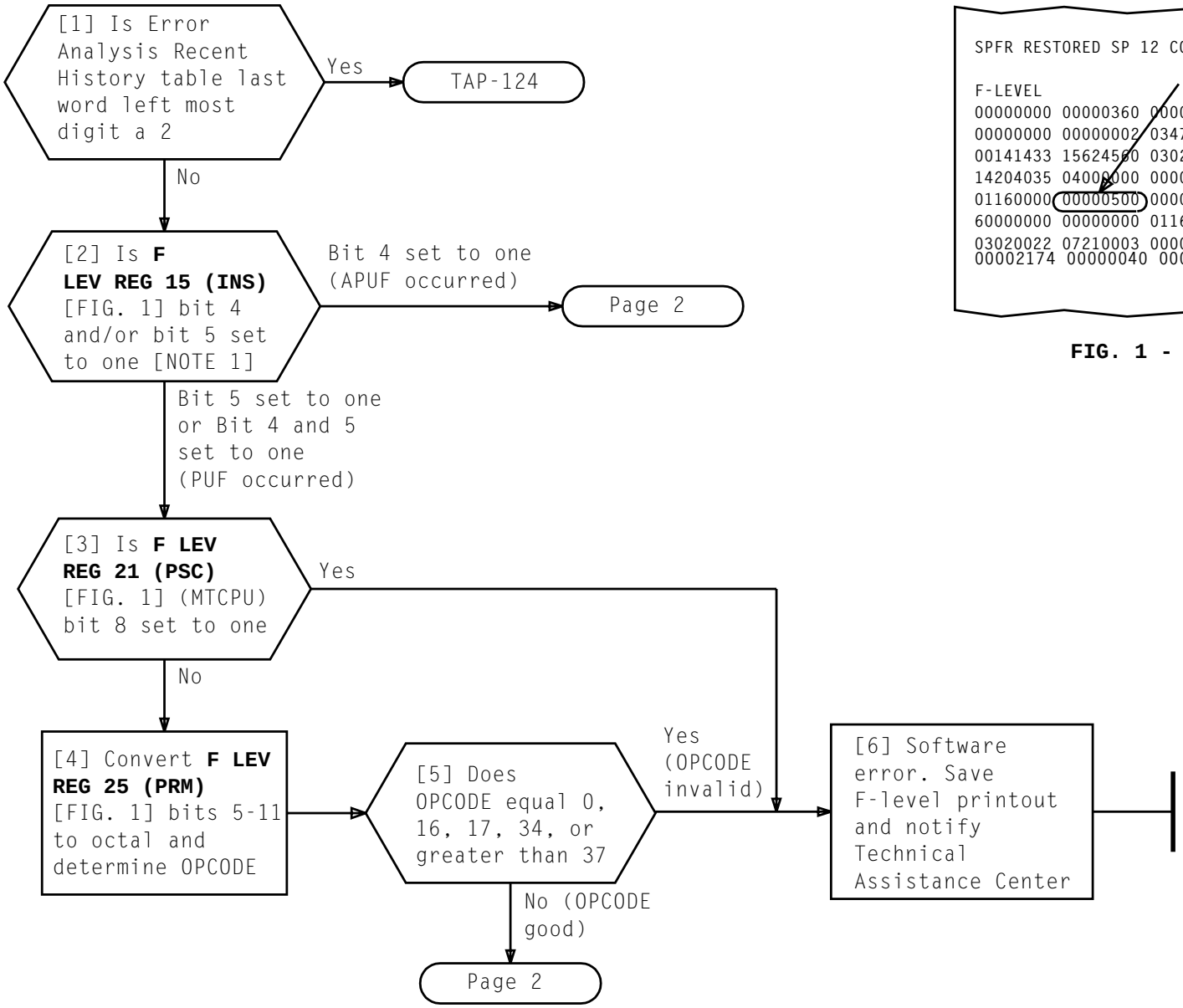
DATA BITS	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TYPE OF ERROR		REF		CSO	CST	PWR	P5	P6	TTL	TTU	TRL	TRU	P3	P4	D0	D1	D2	D3	P1	P2	S0	S1	S2	S3

NOTES
1. All possibilities of troubles are not covered in TABLE B. Any troubles found that are not listed should be added to TABLE B
2. Numbers in parenthesis are circuit pack locations

ANALYZE VCFR INTERJECT

TABLE B
SUSPECT CIRCUIT PACKS ASSOCIATED WITH TYPE OF ERROR

SUSPECT CIRCUIT PACKS	TYPE OF ERROR																						
	S3	S2	S1	S0	P2	P1	D3	D2	D1	D0	P4	P3	TRU	TRL	TTU	TTL	P6	P5	PWR	CST	CSO		REF
JA 3 (09-02)	X	X					X	X															
JA 6 (09-03)	X	X					X	X															
JA 3 (09-04)			X	X					X	X													
JA 6 (09-05)			X	X					X	X													
JA 7 (09-25)	X	X					X	X															
JA 5 (09-26)	X	X					X	X															
JA 7 (09-27)			X	X					X	X													
JA 5 (09-28)			X	X					X	X													
JA 4 (09-29)	X		X																				
JA 4 (09-30)		X		X																			
FA724(03-19)	X	X																					
FA724(03-20)			X	X																			
FA723(15-11)		X	X																				
FA723(15-13)	X	X																					
FA571(15-17)						X																	
FA733(03-16)																							X
FB480(03-15)																							X
FA730(03-17)																							X
FA731(03-11)	X	X	X	X																			
FA732											X												
FB220(15-21)						X																	



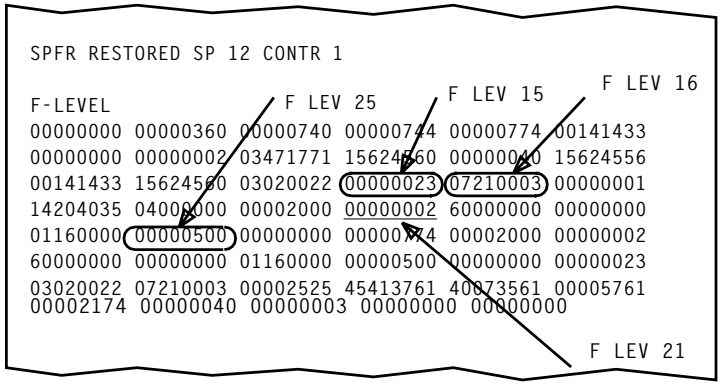


FIG. 1 - F-Level Register Printout

NOTE 1
If both bits are set, then use PUF path

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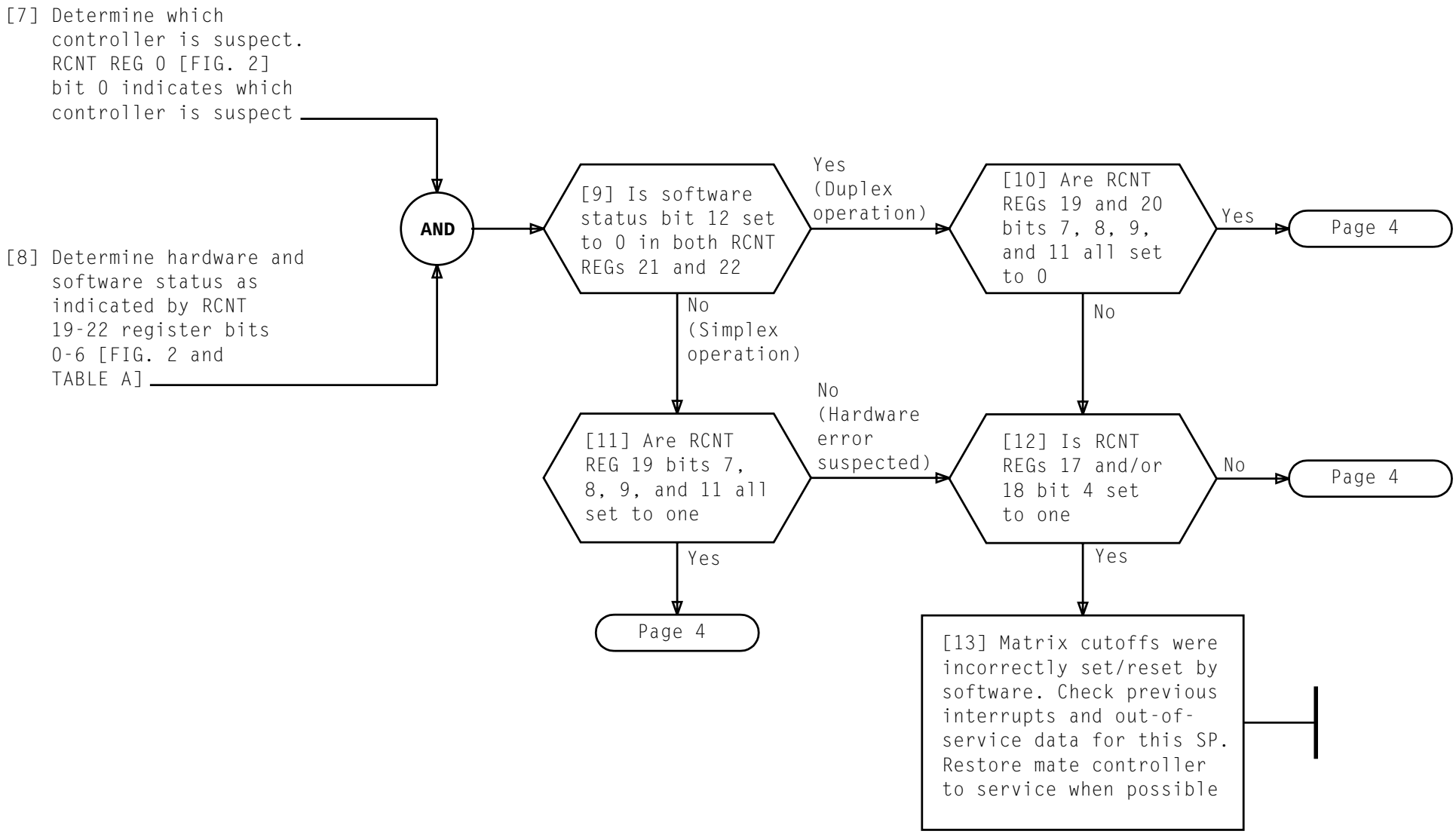
ANALYZE SP F-LEVEL INTERRUPT



ANALYZE SP F-LEVEL INTERRUPT

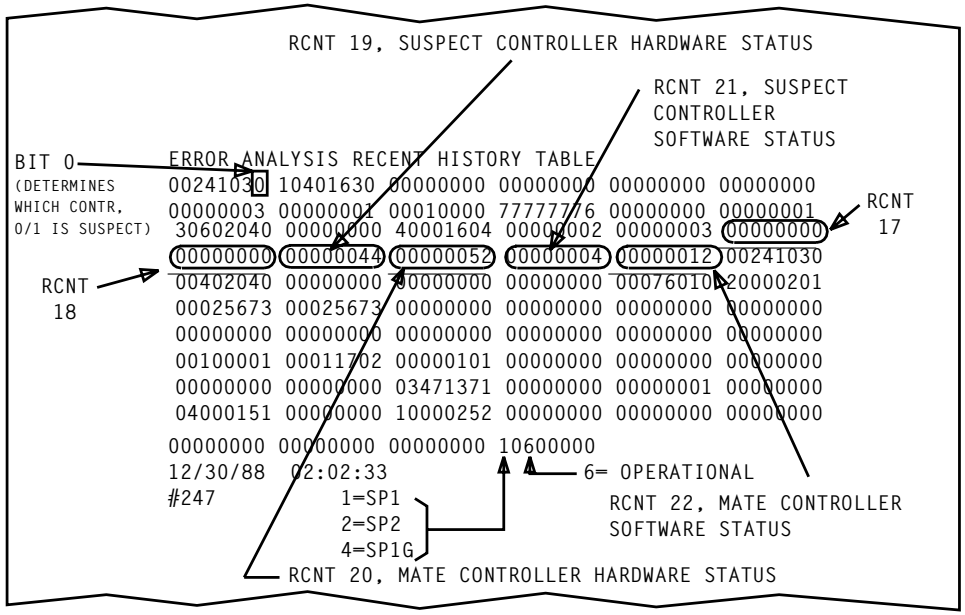
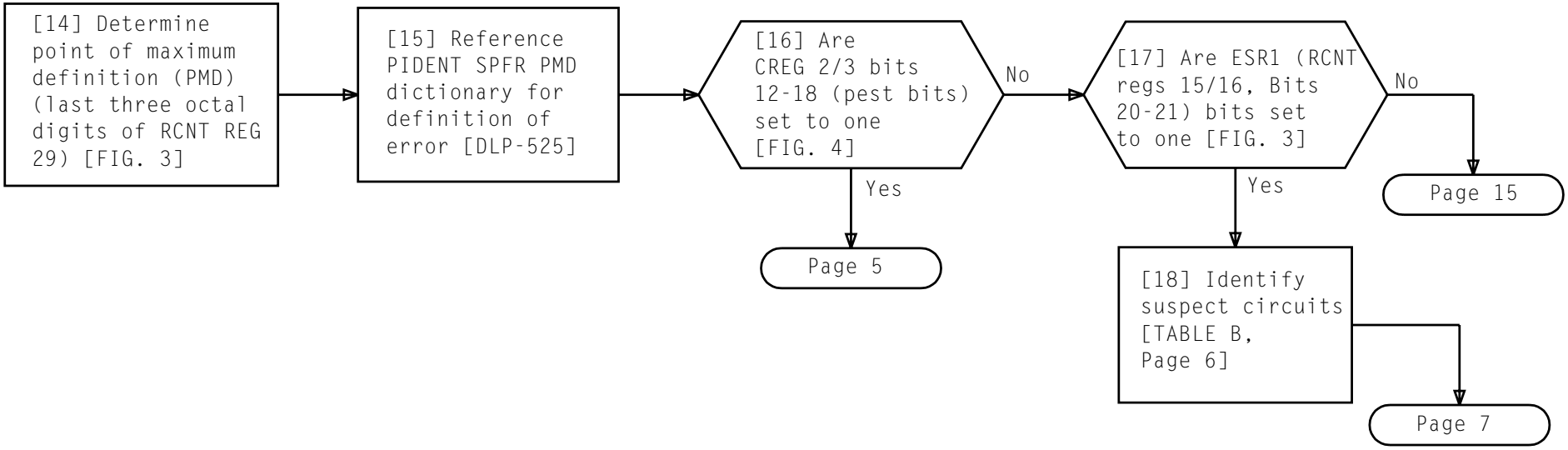


FIG. 2 - RCNT Register Printout

TABLE A
RCNT 19-22, HARDWARE/SOFTWARE STATUS

BIT	NAME	STATE	IMPLICATION
0	MA	0	Operational mode
		1	Maintenance mode
1	RO	0	Receiving on Bus 0
		1	Receiving on Bus 1
2	SO	0	Not sending on Bus 0
		1	Sending on Bus 0
3	S1	0	Not sending on Bus 1
		1	Sending on Bus 1
4	DIV	0	DUPLEX
		1	SIMPLEX — should be set in both controllers
*5	STOP	0	SP not stopped
		1	Stopped for out-of-service or interrupt (only set in out-of-service controller in hardware status)
6	CA	0	Using clock from controller 0
		1	Using clock from controller 1 Both controllers should be using the same clock. If the frame is SIMPLEX, it should be the in-service controller

*Bit 5 (RCNT REGs 19 and 20) is always set on an F-level interrupt printout



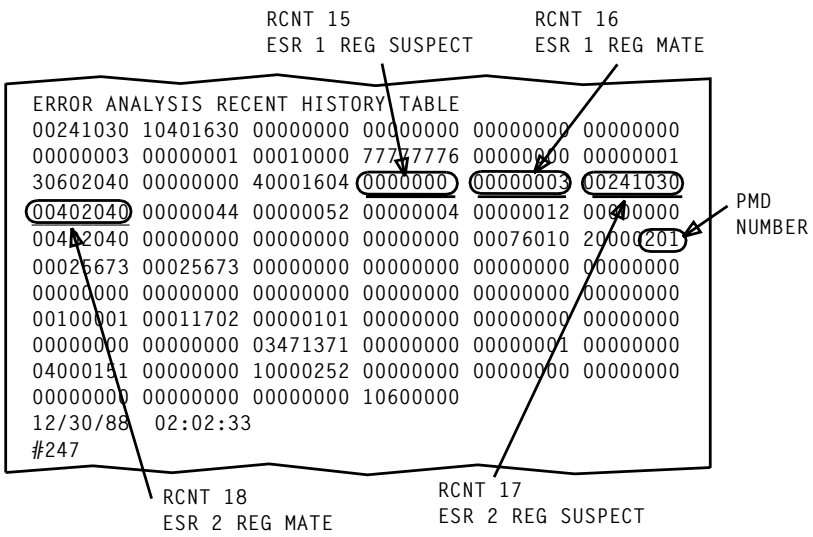


FIG. 3 - RCNT Register Printout

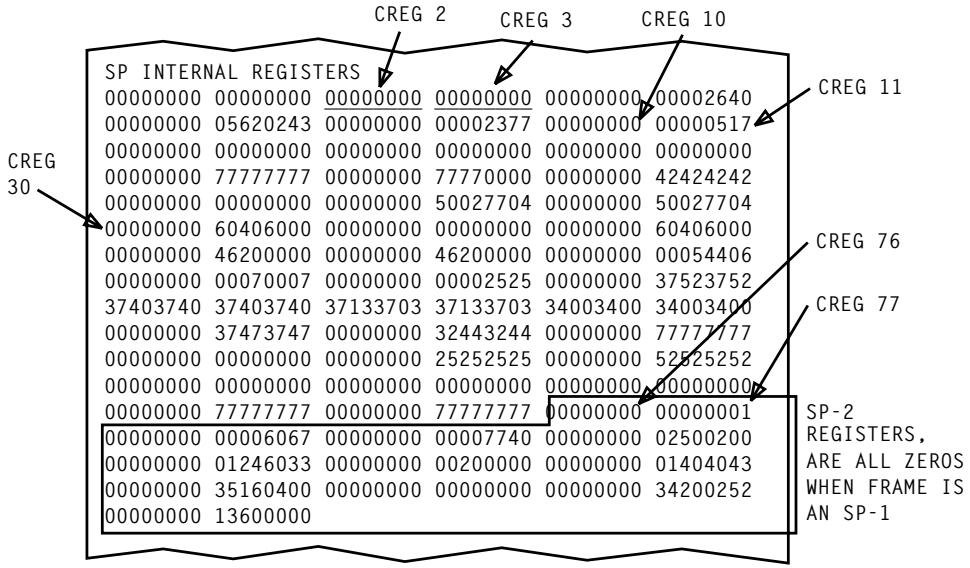
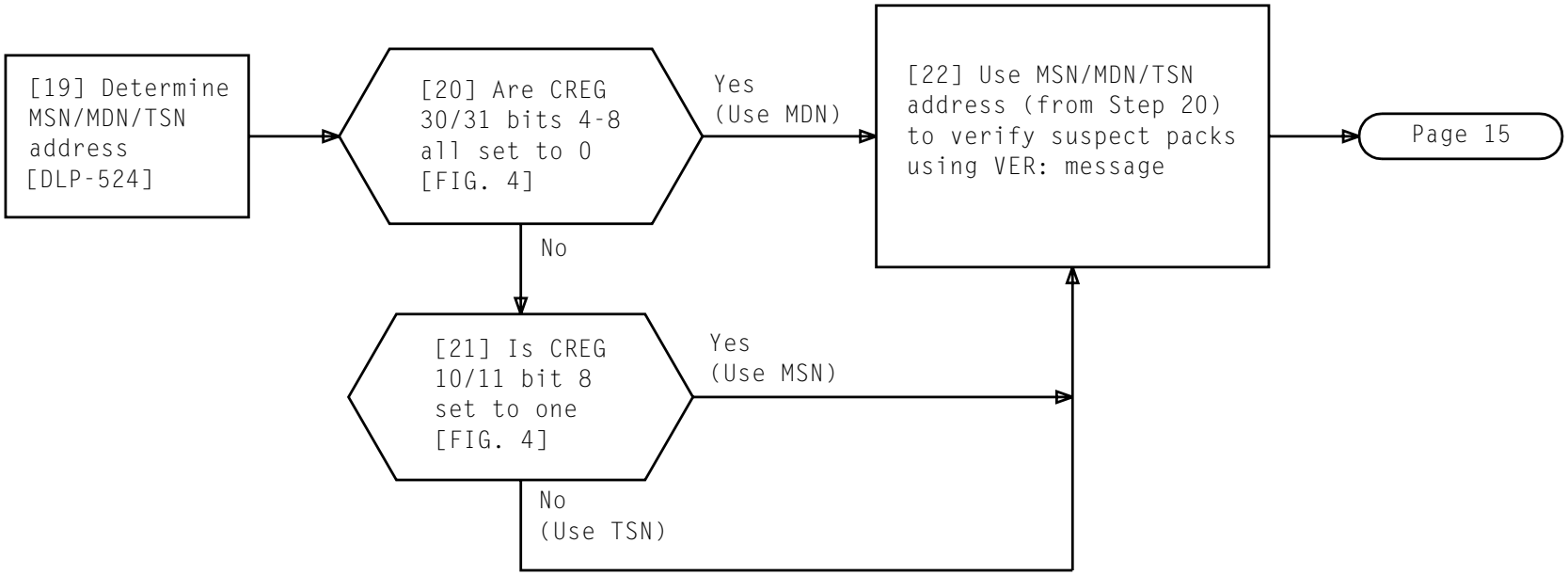


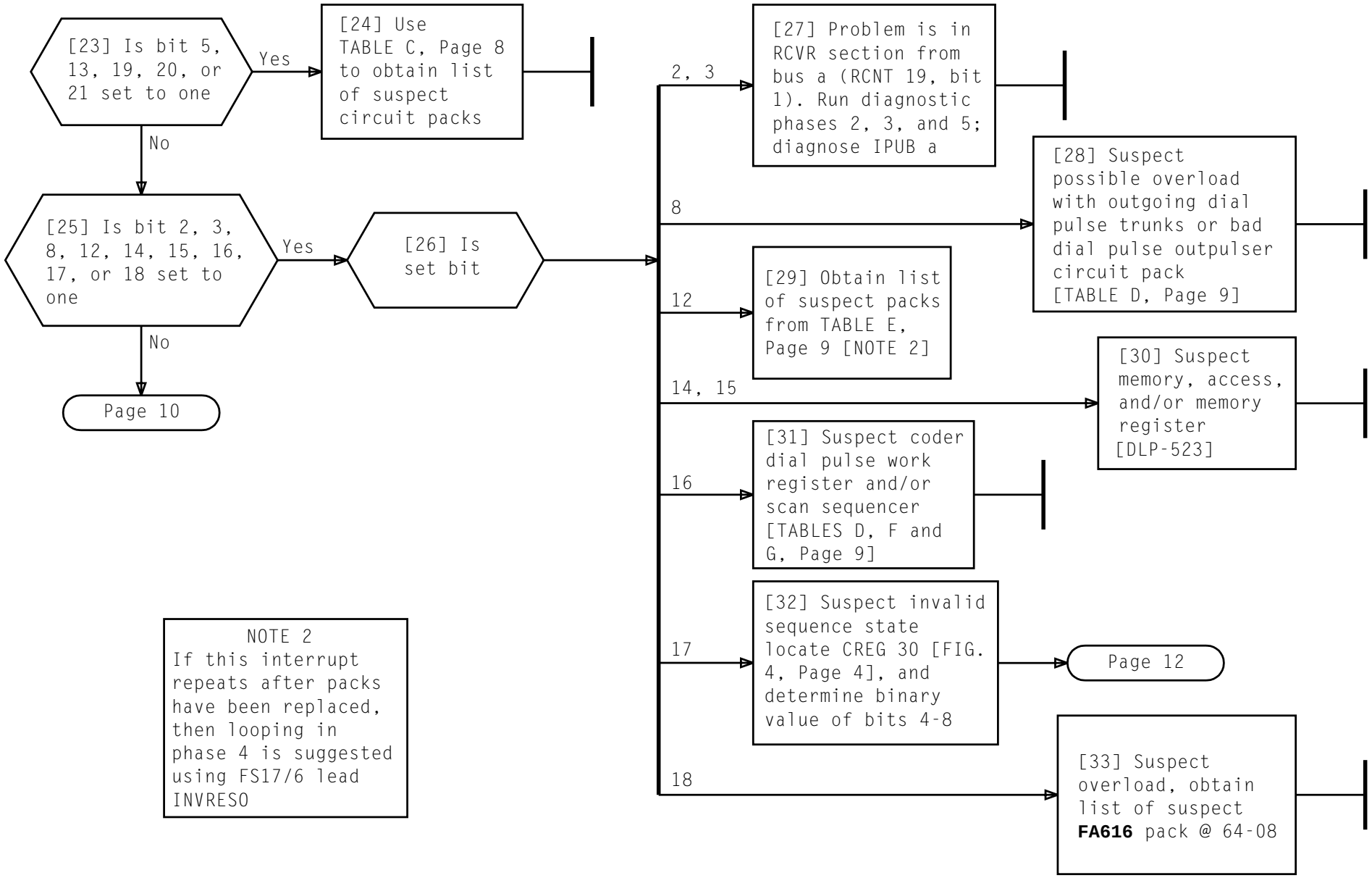
FIG. 4 - SP Internal Register Printout

ANALYZE SP F-LEVEL INTERRUPT



ANALYZE SP F-LEVEL INTERRUPT

TABLE B ESR 1 (RCNT 15 AND 16)			
PACKS IMPLICATED BY ESR BITS CAN BE FOUND IN SD-4A013			
ESR1 BIT	**NET NAME**	**SOURCE FS/SYMBOL**	**COMMENTS**
0	SASWF0	19/10	Directed order failure
1	SATNT0	19/10	Autonomous failure
2	PARE1	1/9	PU bus input parity fail
3	PARO1	1/11	PU bus input parity fail
4	INTJOA	19/24	Interject
5	TROUT0	20/3	Analog timer time-out
6	MXTADRM0	10/14	Matrix address register mismatch
7	RBRMM0	2/9	Reply bus register mismatch
8	DPOLF0	16/3	DP out worklist overflow
9	—	—	—
10	SEQMM0	10/1	Autonomous sequencer mismatch
11	MRMM0	8/11	Memory register mismatch
12	INVRES0	17/6	Invalid OPCODE
13	DETOUT1 CCERR0	20/3 20/6	Level detector error Clock error
14	MRP1ER0	8/3	Memory parity 1
15	MRP2ER0	8/4	Memory parity 2
16	GTH0	14/5	Coder greater than DPWR
17	SQINVS0	10/1	Sequencer invalid state
18	SANTTO0	18/2	Executive sequencer sanity error
19	XMCLER0	20/12	Extended MS clock error
20	CLKMM0	20/9	Ring counters mismatch
21	DPRWER0	12/10	Missing DP in end-of-list flag
22	—	—	—
23	—	—	—



ANALYZE SP F-LEVEL INTERRUPT

TABLE C
ESR1 SUSPECT PACKS/ACTION

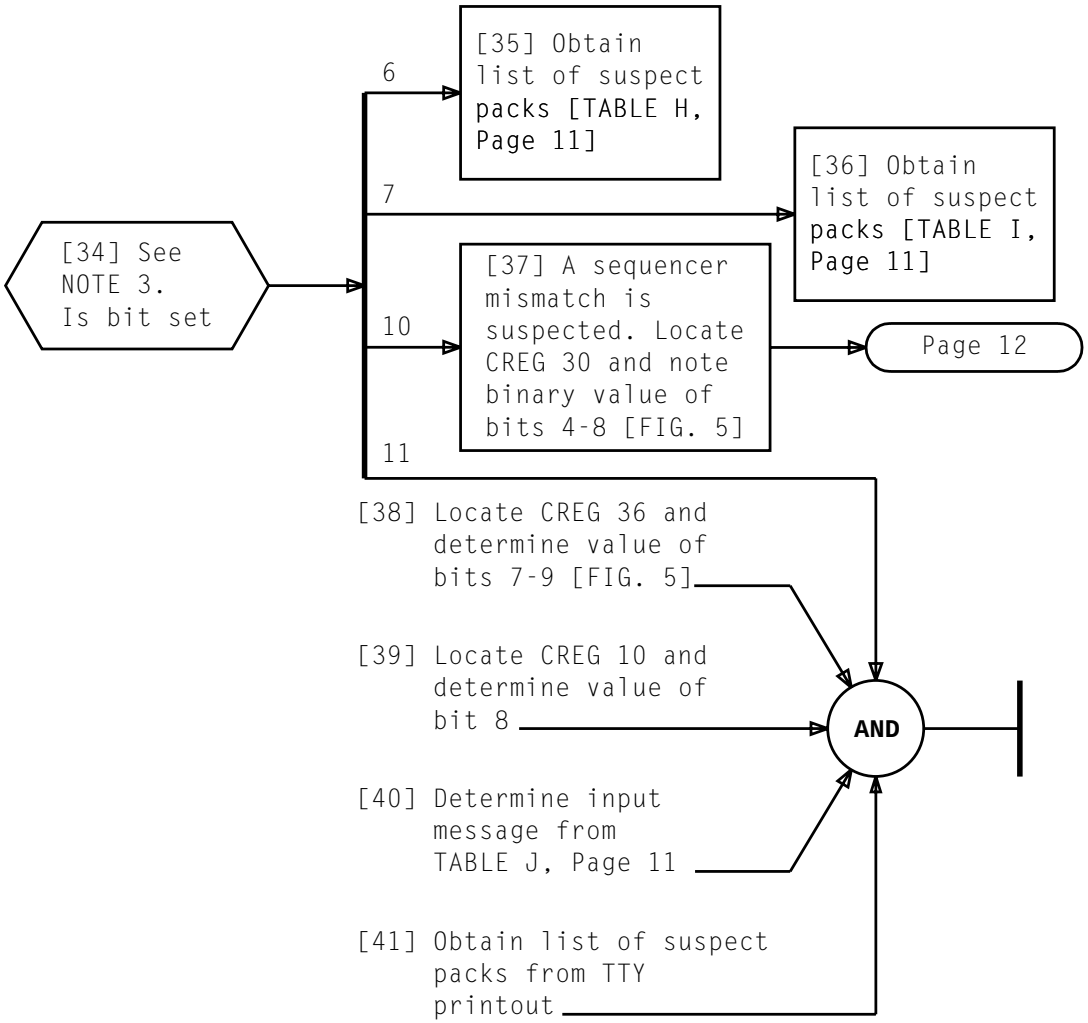
ESR BIT	SP-1 COMBINED MATRIX		COMMENTS/RECOMMENDED PROCEDURE
	PACK TYPE	LOCATION	
2,3	—	—	Problem in RCVR section from BUS a (RCNT 19, bit 1); run DGN phases 2, 3, and 5/**DGN:IPUB** a
5	**FB002** **FB001** **FA668**	60-04 56-04 60-06	
8	—	—	Possible overloaded outgoing dial pulse trunks or bad **FS14** circuit pack
12	—	—	Check lead INVRESO (**FS17**/6) if pack replacement does not solve problem
13, *20	**FB001** **FA663** **FB002** **FB003** **FA664**	56-04 56-06 60-04 56-05 56-07	
14,15	—	—	Perform memory pack procedure [DLP-523]
16	—	—	Suspect coder (**FS13**) dial pulse work reg (**FS14**) and/or scan sequencer (**FS12**)
17	—	—	Check for invalid sequencer state
18	—	—	Possible SP overload (not serving offered load) suspect executive sequencer circuit packs (**FS18**)
19	**FA575**	68-06	
21	**FA577** **FA588**	64-20,21,22 64-25	Also, suspect scan sequencer circuit packs (**FS12**)
* Bad pack could be in either controller			

TABLE D FS14 CIRCUIT PACKS	
SP-1 COMBINED MATRIX	
PACK TYPE	LOCATION
FA577	60-16
FA576	60-14, 13, 12
FA621	60-11
FA620	60-10
FA588	64-23

TABLE E FS17 CIRCUIT PACKS			
SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA618	72-23	**FA1243**	72-23
FA619	72-24	**FA1242**	72-24
FA604	72-20	**FA525**	72-20
FA583	72-21	**FA583**	72-21
FA525	72-22	**FA603**	72-22
FA603	72-25	**FA619**	72-25
FA599	56-26	**FA599**	56-26

TABLE F FS12 CIRCUIT PACKS	
SP-1 COMBINED MATRIX	
PACK TYPE	LOCATION
FA592	64-16
FA593	64-17
FA589	64-18
FA591	64-19
FA600	64-11
FA598	64-10
FA602	64-14
FA613	64-12
FA621	60-11
FA601	64-13

TABLE G FS13 CIRCUIT PACKS	
PACK TYPE	SP-1/COMBINED MATRIX LOCATION
FA576	60-12, 13, 14



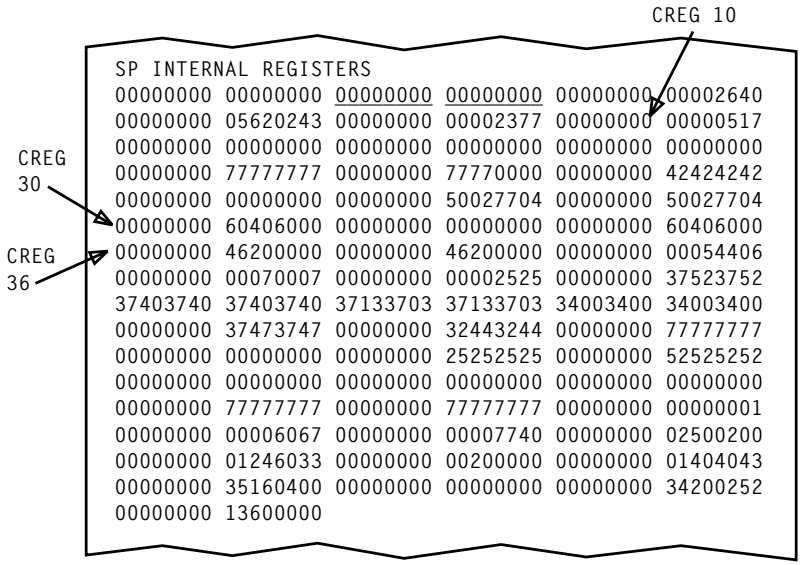


FIG. 5 - SP Critical Register (CREG) Printout

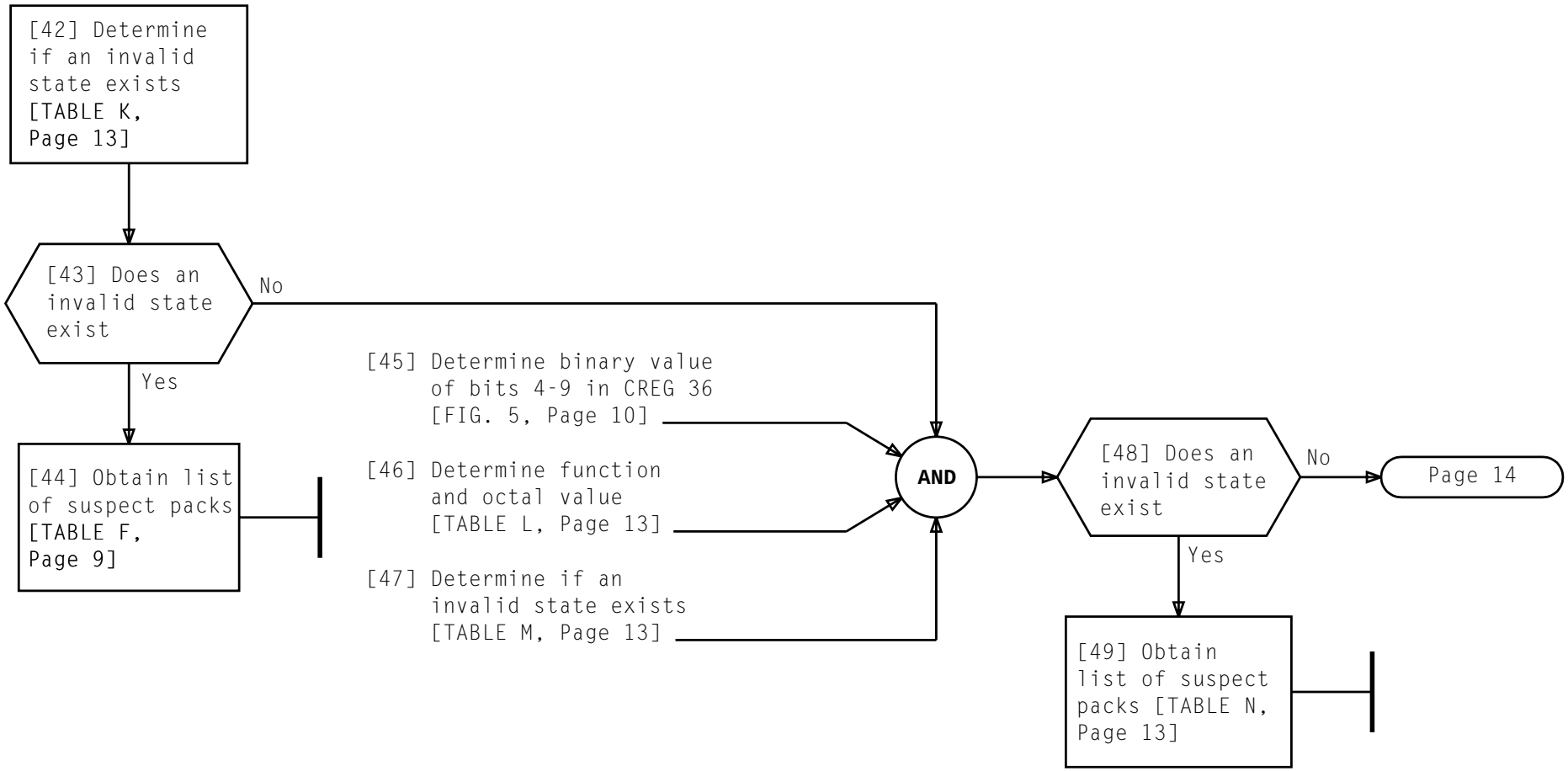
NOTE 3
Bad pack could be in either controller

ANALYZE SP F-LEVEL INTERRUPT

TABLE H FS10 CIRCUIT PACKS			
SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA590	56-19,20,21,22	**FA1239**	56-19,20,21,22
FA587	56-11	**FA1238**	56-11
FA597	56-13	**FA1241**	56-13
FA596	56-12	**FA1240**	56-12
FA584	56-18,17,16,14	**FA584**	56-18,17,16,14
FA599	56-26,25,24	**FA599**	56-26,25,24

TABLE I FS 2 CIRCUIT PACKS	
PACK TYPE	SP-1/COMBINED MATRIX LOCATION
FA531	72-09,10
FA534	72-08
FA528	72-04,05,06,07 72-11,12,13,14

TABLE J VERIFY MESSAGES		
CREG 36 BITS 7-9 VALUE	CREG 10 BIT 8 VALUE	USE VERIFY MESSAGE
0	0	VER:SPMTXPK:SCP,TSN o'a!
0	1	VER:SPMTXPK:SCP,MSN o'a!
≠ 0	0	VER:SPMTXPK:SDM,TDN o'a!
≠ 0	1	VER:SPMTXPK:SDM,MDN o'a!
a = TSN, MSN, TDN, or MDN octal number		



ANALYZE SP F-LEVEL INTERRUPT

TABLE K
INVALID SCAN SEQUENCER STATES

BIT	8	7	6	5	4
VALUE	1	0	1	0	0
		1	0	1	0
			0	1	1
			1	0	0
				0	1
				1	0
					1

TABLE L
FUNCTION AND VALUE OF MATRIX SEQUENCER

BIT			FUNCTION	BIT			OCTAL VALUE	BIT			FUNCTION	BIT			OCTAL VALUE
9	8	7		6	5	4		9	8	7		6	5	4	
0	0	0	A	0	0	0	0	1	0	0	E	1	0	0	4
		1	B			1	1			1	F			1	5
	1	0	C		1	0	2		1	0	G		1	0	6
		1	D			1	3			1	H			1	7

TABLE M
INVALID MATRIX SEQUENCER STATES

FUNCTION	OCTAL VALUE							
	0	1	2	3	4	5	6	7
A				*	*	*		
B				*	*	*		
C					*			
D					*			
E			*	*	*			
F	*	*	*	*	*	*	*	*
G					*			
H			*	*	*			

TABLE N
MATRIX SEQUENCER SUSPECT PACKS

PACK TYPE		LOCATION
SP-1	COMBINED MATRIX	
FA587	FA1238	56-11
FA597	FA1241	56-13
FA596	FA1240	56-12
FA599		56-26,25,24
FA616		64-08

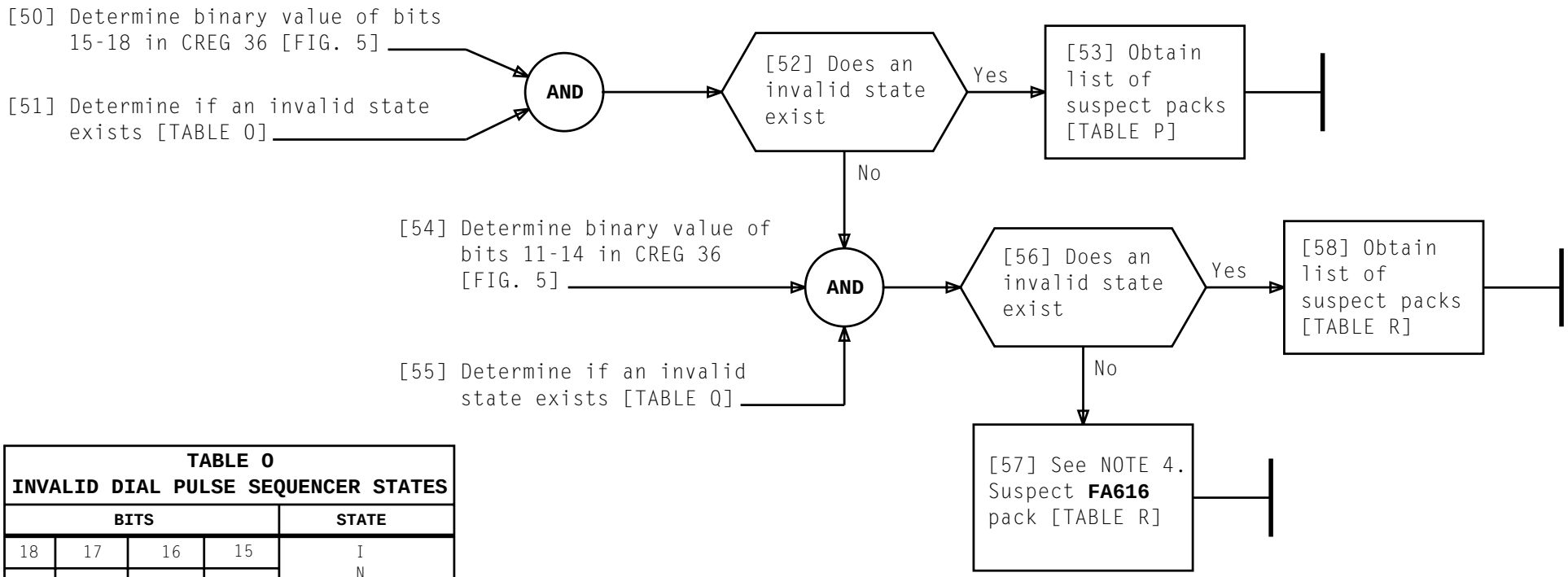


TABLE O
INVALID DIAL PULSE SEQUENCER STATES

BITS				STATE
18	17	16	15	INVALID
1	1	0	0	
			1	
		1	0	
			1	

TABLE P
FS14 CIRCUIT PACKS

PACK TYPE	LOCATION
	SP-1 COMBINED MATRIX
FA577	60-16
FA576	60-14,13,12
FA621	60-11
FA602	60-10
FA588	64-23
FA616	64-08

TABLE Q
INVALID MF OUT SEQUENCER STATES

BIT				STATE
14	13	12	11	INVALID
1	0	1	1	
	1	0	0	
			1	
		1	0	
			1	

TABLE R
MF OUT SEQUENCER

SP-1/COMBINED MATRIX PACKS	
PACK TYPE	LOCATION
FA615	64-04
FA614	64-05
FA588	64-23
FA577	64-06
FA581	64-07
FA616	64-08

NOTE 4
If trouble does not clear, check mate sequencers for invalid state

ANALYZE SP F-LEVEL INTERRUPT

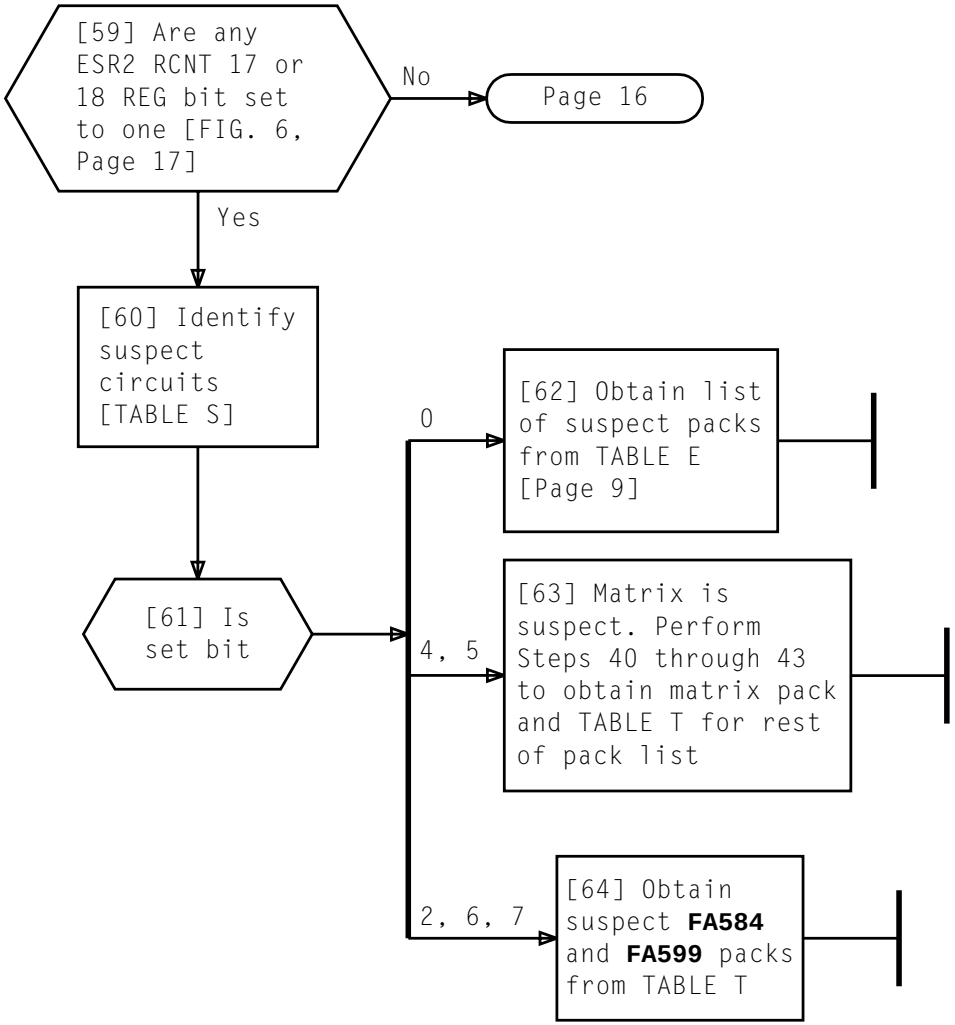


TABLE S

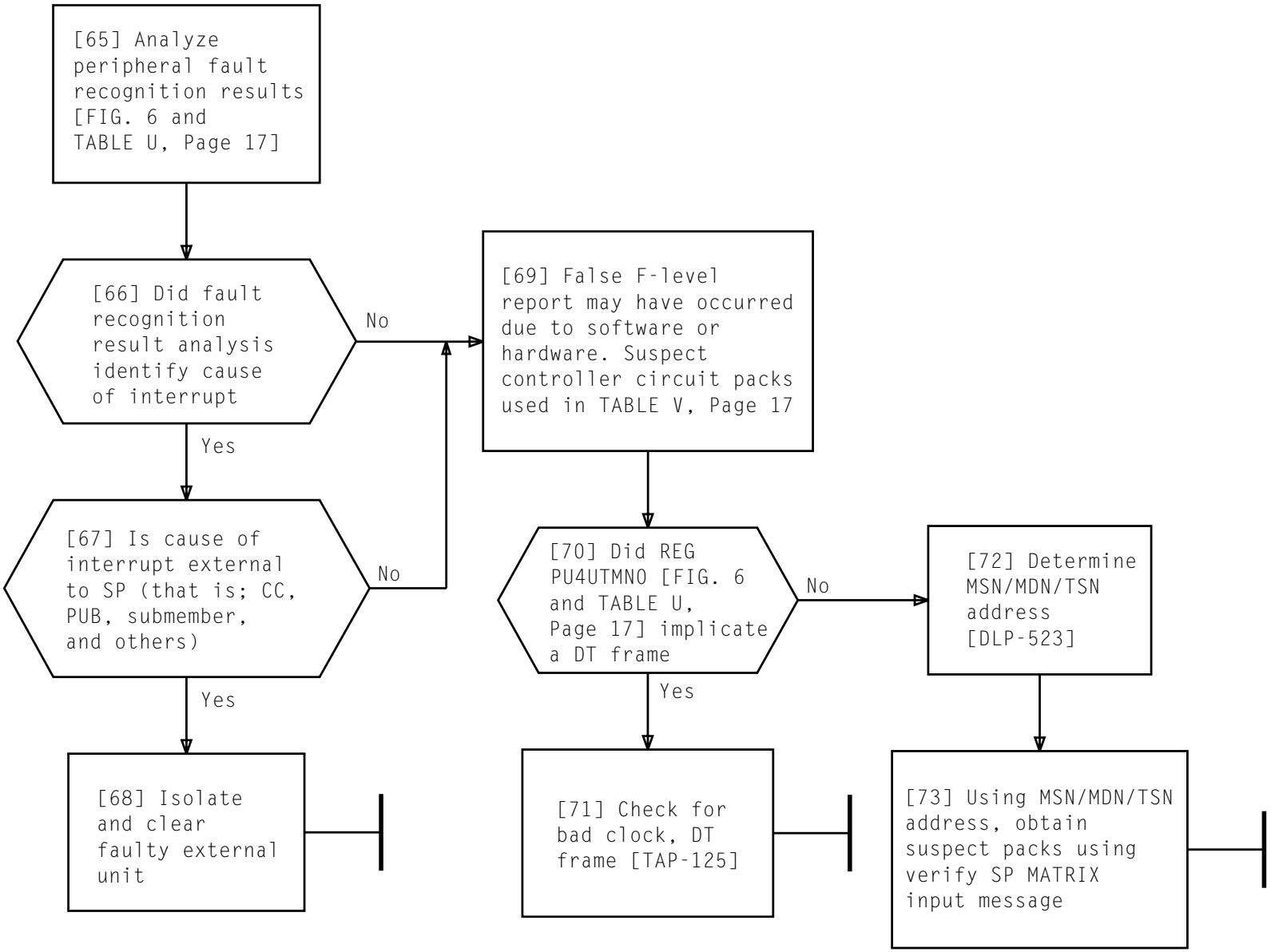
USING INFORMATION FROM TABLE D, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A013 USING CHART BELOW

ESR2 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	PUSOT00	17/8	PU sequencer time-out
1	—	—	—
2	WNEWI0	10/3	Matrix work-work register mismatch
3	—	—	—
4	MXTASWF0	10/26	Matrix ASW failure
5	MXTHOM00	10/27	Matrix homogeneity failure
6	HNEHE0	10/3	Matrix hold-hold register mismatch
7	MXWNCH0	10/10	Matrix work-hold register mismatch
8	—	—	—

TABLE T
BIT 4, 5 SUSPECT PACK LIST

SP-1		COMBINED MATRIX	
PACK TYPE	LOCATION	PACK TYPE	LOCATION
FA584	56-18, 17, 16, 14	**FA584**	56-18, 17, 16, 14
FA599	56-26, 25, 24	**FA599**	56-26, 25, 24
FA590	56-19, 20, 21, 22	**FA1239**	56-19, 20, 21, 22
FA587	56-11	**FA1238**	56-11
FA597	56-13	**FA1241**	56-13
FA596	56-12	**FA1240**	56-12

ANALYZE SP F-LEVEL INTERRUPT



ANALYZE SP F-LEVEL INTERRUPT

TABLE U
PERIPHERAL FAULT RECOGNITION RESULTS

IDENTIFICATION OF REGISTERS IN RESULTS TABLE OF F-LEVEL MESSAGE

PU4RESULT PU4UTMNO PU4FRPMD PU4FRJRG

PU4RESULT ----------NMLKJIHGFEDCBA

Bit	0	A = CC0 found faulty
	1	B = CC1 found faulty
	2	C = Controller 0 found faulty
	3	D = Controller 1 found faulty
	4	E = PU bus 0 found faulty
	5	F = PU bus 1 found faulty
	6	G = PU bus 0 at unit found faulty
	7	H = PU bus 1 at unit found faulty
	8	I = Faulty unit or subunit to be removed and diagnosed
	9	J = Faulty unit or subunit to be removed
	10	K = Fault recognition was unable to find the fault
	11	L = Fault recognition found that a software error caused the F-level
	12	M = Fault recognition found that a transient caused the F-level
	13	N = Signal processor matrix found faulty

PU4UTMNO DDDDDDDCCCCCCCBAAAAAAA--

Bits	2-8	A = Submember found faulty (if any)
	9	B = Set if submember found faulty
	10-16	C = Member number found faulty
	17-23	D = Unit type found faulty

PU4FRPMD --CCCCCCCBBBBBBBAAAAAAAA

Bits	0-7	A = Point of maximum definition MACRO number relative to an FR program
	8-14	B = Fault recognition decision code
	15-21	C = Error analysis action code

PU4FRJRG = FR program address where error was located

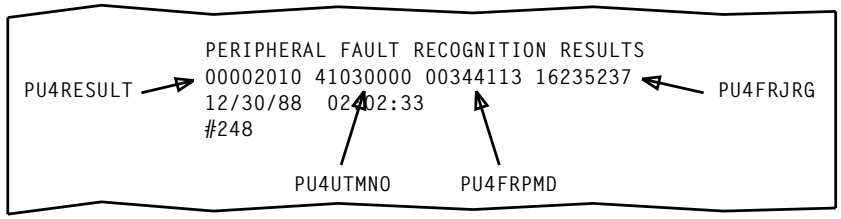


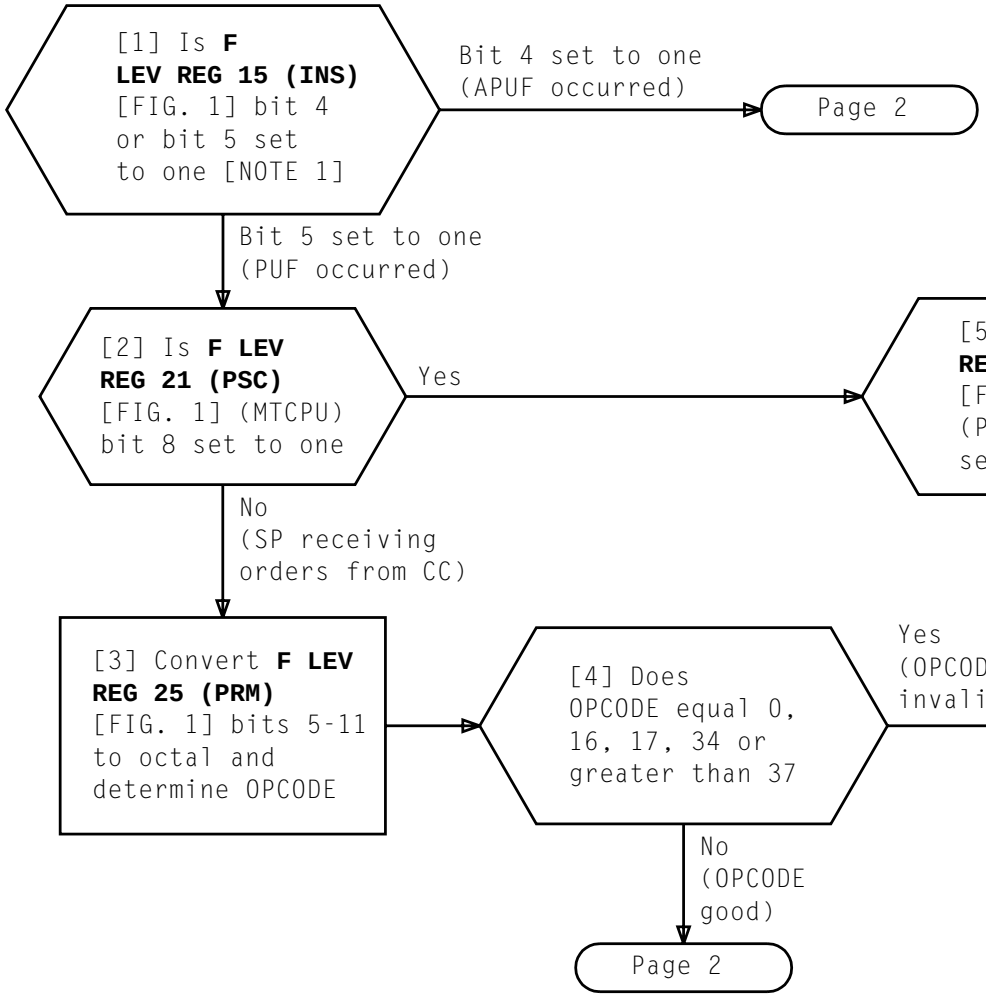
FIG. 6 — Peripheral Fault Recognition Results Printout

TABLE V
SP CONTROLLER PACKS

	PACK	LOCATION
4A013 (FS19)	**FA617**	68-07
	FA529	72-26

ANALYZE SP F-LEVEL INTERRUPT

ANALYZE SP2 F-LEVEL INTERRUPT



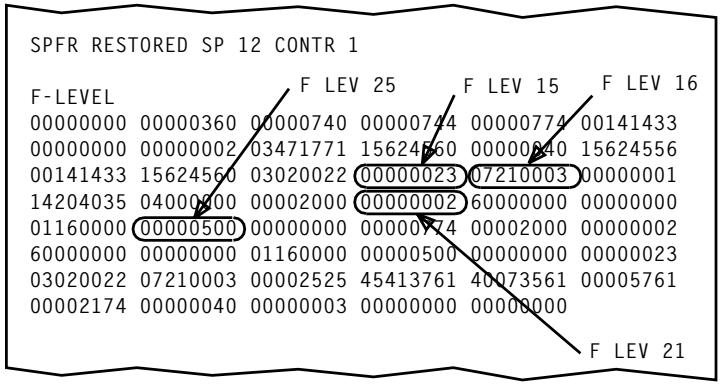
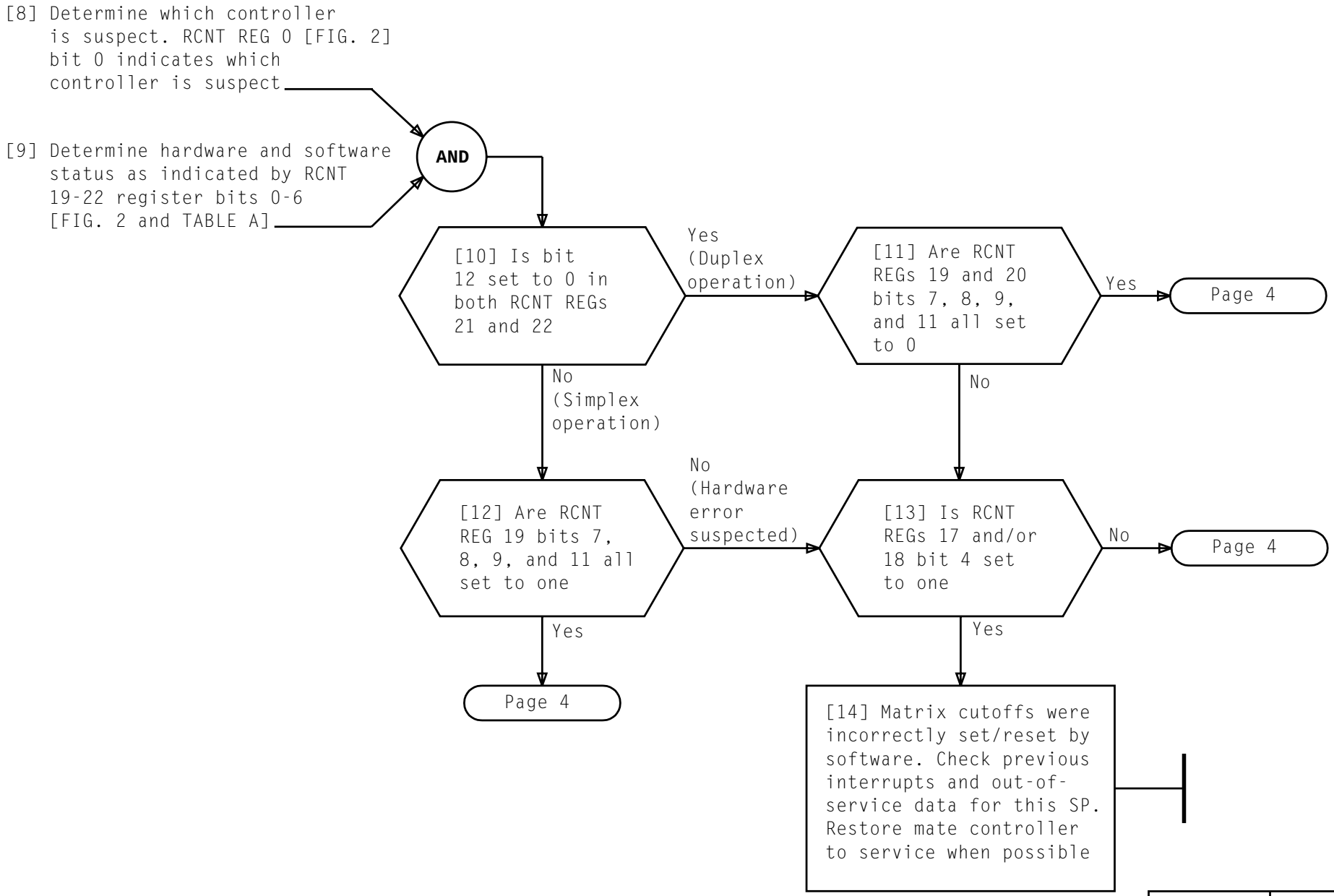


FIG. 1 - F-Level Register Printout

NOTES
1. If both bits are set, then use PUF path
2. If this interrupt repeats, suspect software and notify RWC, N-TAC, etc



ANALYZE SP2 F-LEVEL INTERRUPT

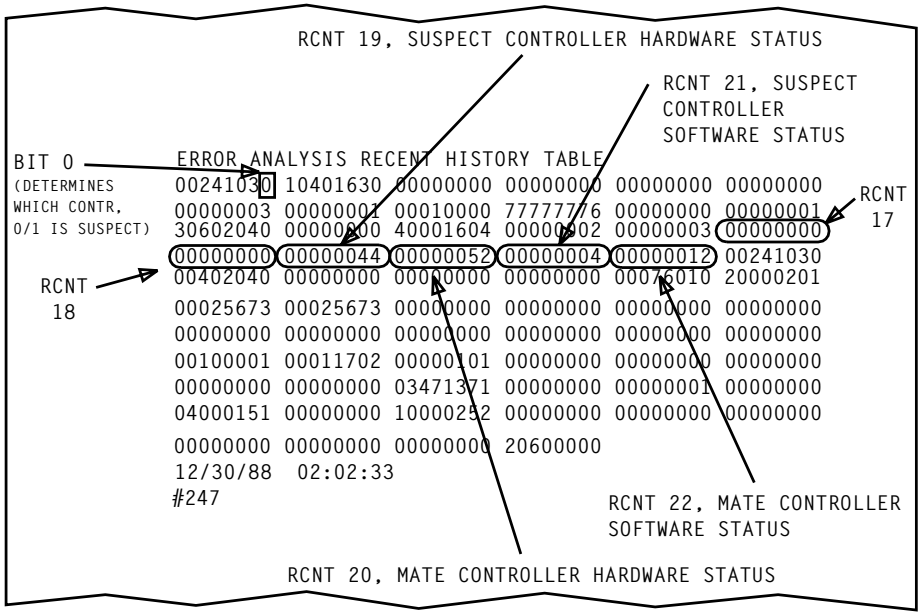
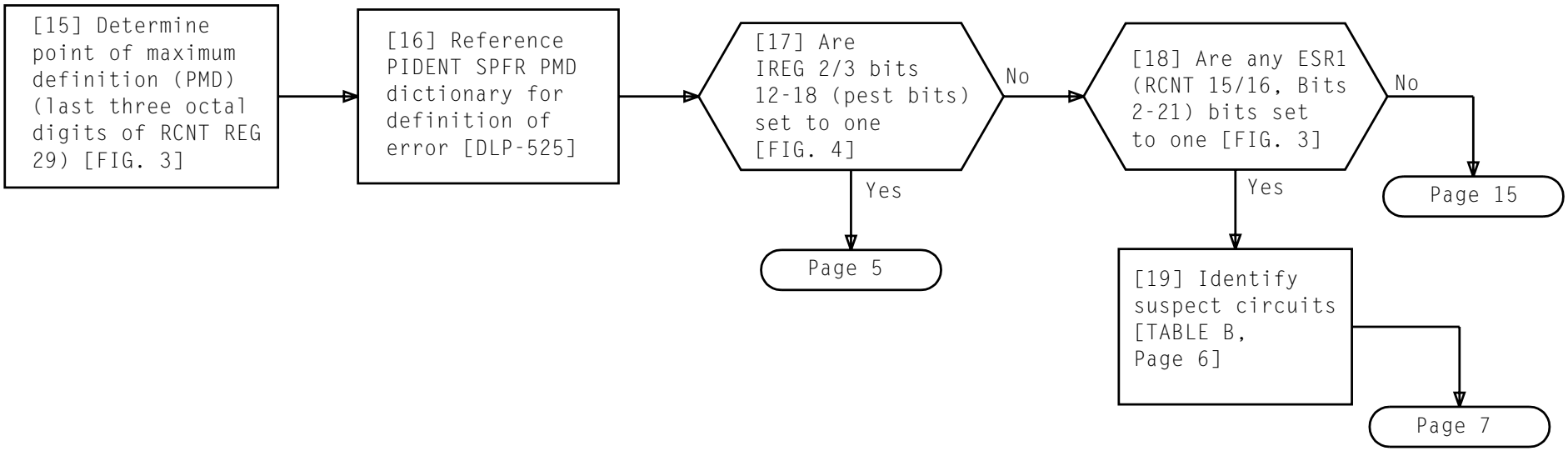


FIG. 2 - RCNT Register Printout

TABLE A
RCNT 19-22, HARDWARE/SOFTWARE STATUS

BIT	NAME	STATE	IMPLICATION
0	MA	0	Operational mode
		1	Maintenance mode
1	RO	0	Receiving on Bus 0
		1	Receiving on Bus 1
2	SO	0	Not sending on Bus 0
		1	Sending on Bus 0
3	S1	0	Not sending on Bus 1
		1	Sending on Bus 1
4	DIV	0	DUPLEX
		1	SIMPLEX — should be set in both controllers
*5	STOP	0	SP not stopped
		1	Stopped for out-of-service or interrupt (only set in out-of-service controller in hardware status)
6	CA	0	Using clock from Controller 0
		1	Using clock from Controller 1 Both controllers should be using the same clock. If the frame is SIMPLEX, it should be the in-service controller

*Bit 5 (RCNT REGs 19 and 20) is always set on an F-level interrupt printout



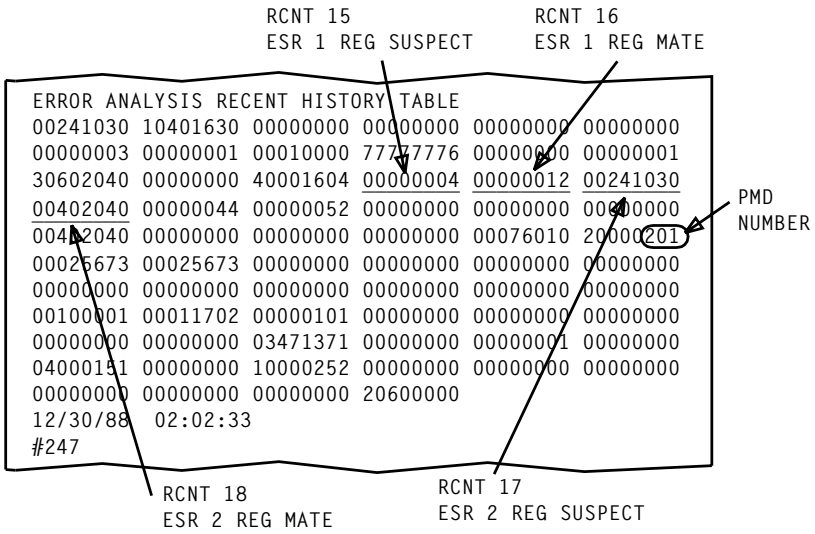


FIG. 3 — RCNT Register Printout

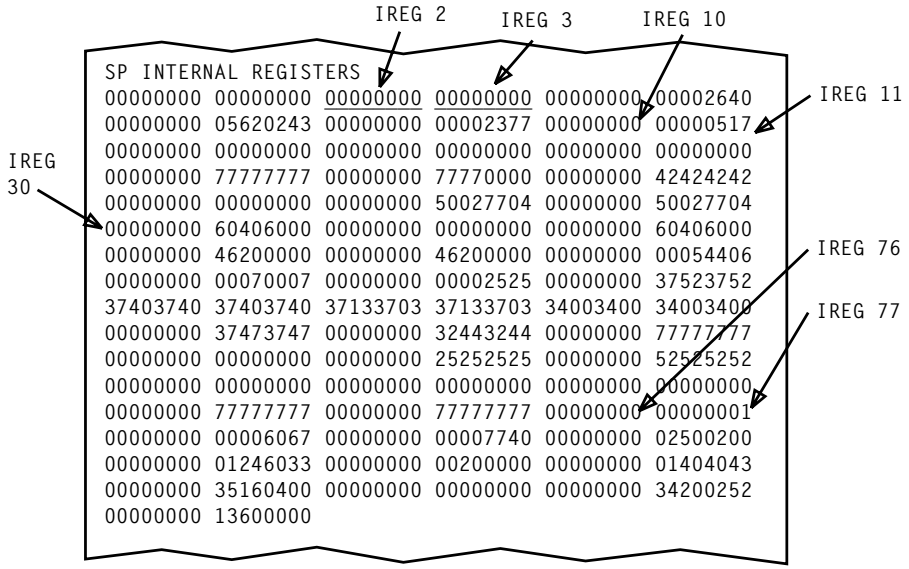
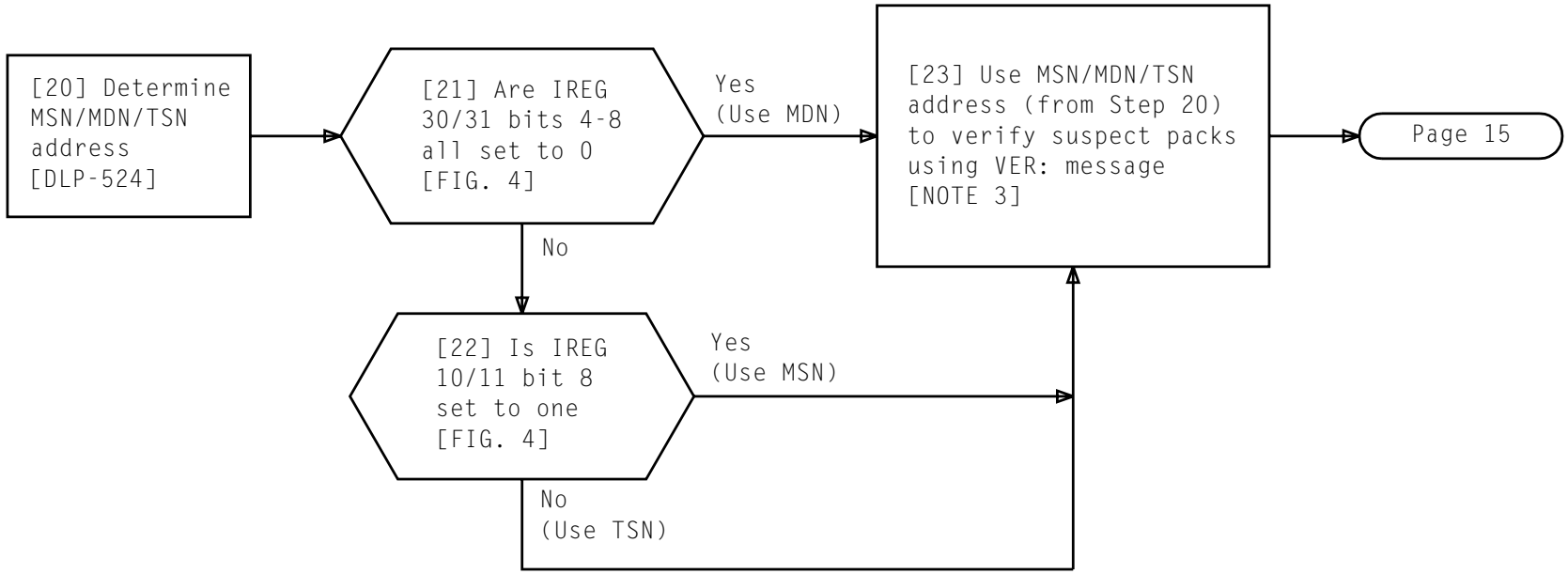


FIG. 4 — SP Internal Register (IREG) Printout

ANALYZE SP2 F-LEVEL INTERRUPT



NOTE 3
An SP-2 may have an associated pack not identified by verify message

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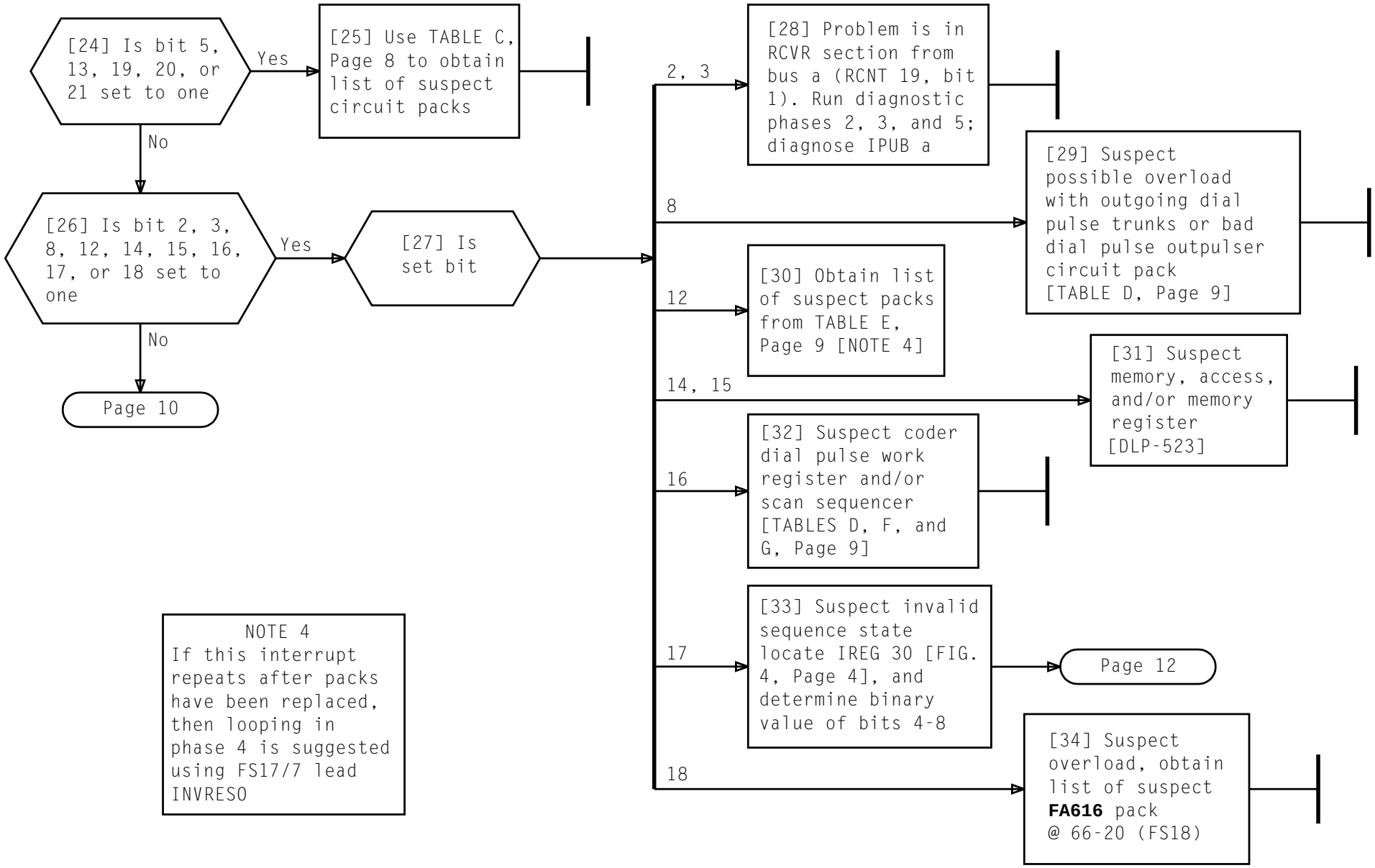
ANALYZE SP2 F-LEVEL INTERRUPT

TABLE B ESR 1 (RCNT 15 AND 16)			
PACKS IMPLICATED BY ESR BITS CAN BE FOUND IN SD-4A067 USING CHART BELOW			
ESR1 BIT	**NET NAME**	**SOURCE FS/SYMBOL**	**COMMENTS**
0	SASWF0	19/10	Directed order failure
1	SATNT0	19/10	Autonomous failure
2	PARE1	1/9	PU bus input parity fail
3	PARO1	1/11	PU bus input parity fail
4	INTJOA	19/24	Interject
5	TROUT0	20/3	Analog timer time-out
6	MXTADRM0	10/14	Matrix address register mismatch
7	RBRMM0	2/9	Reply bus register mismatch
8	DPOLF0	16/3	DP out worklist overflow
9	—	—	—
10	SEQMM0	10/1	Autonomous sequencer mismatch
11	MRMM0	8/11	Memory register mismatch
12	INVRES0	17/6	Invalid OPCODE
13	DETOUT1 CCERR0	20/3 20/6	Level detector error Clock error
14	MRP1ER0	8/3	Memory parity 1
15	MRP2ER0	8/4	Memory parity 2
16	GTH0	14/5	Coder greater than DPWR
17	SQINVS0	10/1	Sequencer invalid state
18	SANTTO0	18/2	Executive sequencer sanity error
19	XMCLER0	20/12	Extended MS clock error
20	CLKMM0	20/9	Ring counters mismatch
21	DPRWER0	12/10	Missing DP in end-of-list flag
22	—	—	—
23	—	—	—



ANALYZE SP2 F-LEVEL INTERRUPT

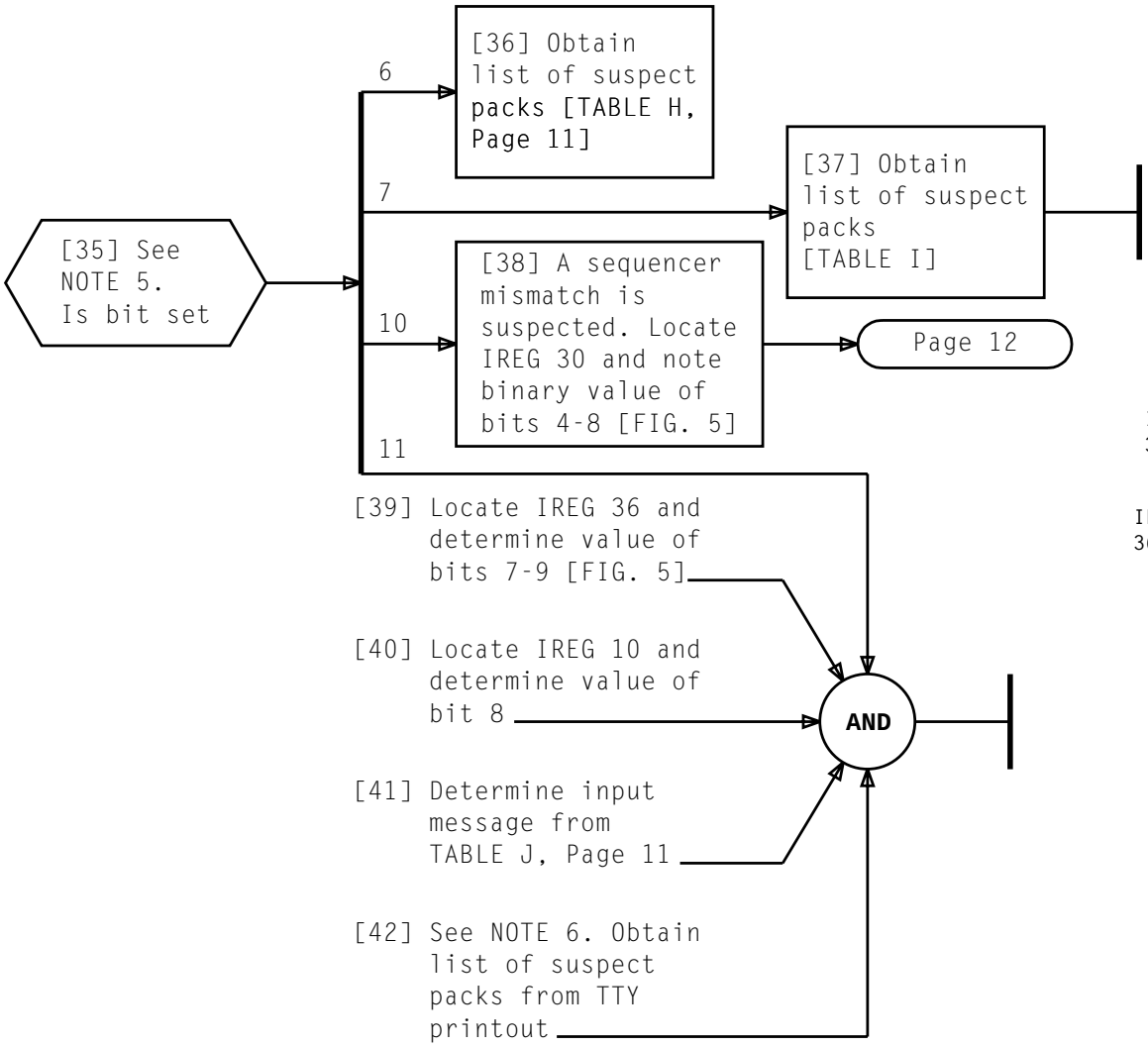
TABLE C ESR1 SUSPECT PACKS/ACTION			
ESR BIT	SP-2		COMMENTS/RECOMMENDED PROCEDURE
	PACK TYPE	LOCATION	
2,3	—	—	Problem in RCVR section from BUS a (RCNT 19, bit 1); run DGN phases 2, 3, and 5/DGN:IPUB a
5	**FB002**	62-12	
	FB002	62-11	
	FA668	62-14	
8	—	—	Possible overloaded outgoing dial pulse trunks or bad **FS14** circuit pack
12	—	—	Check lead INVRESO (FS17/7) if pack replacement does not solve problem
13, *20	**FA663**	66-12	
	FB002	62-12	
	FB003	66-10	
	FA664	66-11	
	FB001	62-11	
14,15	—	—	Perform memory pack procedure [DLP-523]
16	—	—	Suspect coder (FS13) dial pulse work reg (FS14) and/or scan sequencer (FS12)
17	—	—	Check for invalid sequencer state
18	—	—	Possible SP overload (not serving offered load) suspect executive sequencer circuit packs (FS18)
19	**FA575**	58-34	
21	**FA577**	66-32,34,31	Also, suspect scan sequencer circuit packs (FS12)
	FA588	66-41	
* Bad pack could be in either controller			

TABLE D FS14 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA577	62-14
FA576	62-20, 21, 23
FA621	62-22
FA620	62-19
FA588	66-40

TABLE E FS17 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA1195	74-26
FA619	74-29
FA618	74-31
FA604	74-32
FA583	74-38
FA525	74-43
FA603	74-37
FA599	74-13
FA1194	74-25

TABLE F FS12 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA1245	62-16
FA602	62-22
FA591	66-24
FA600	66-18
FA613	66-21
FA589	66-16
FA1246	62-15
FA598	62-17
FA601	66-15
FA621	66-22

TABLE G FS13 CIRCUIT PACKS	
PACK TYPE	LOCATION
FA576	62-20, 21, 23



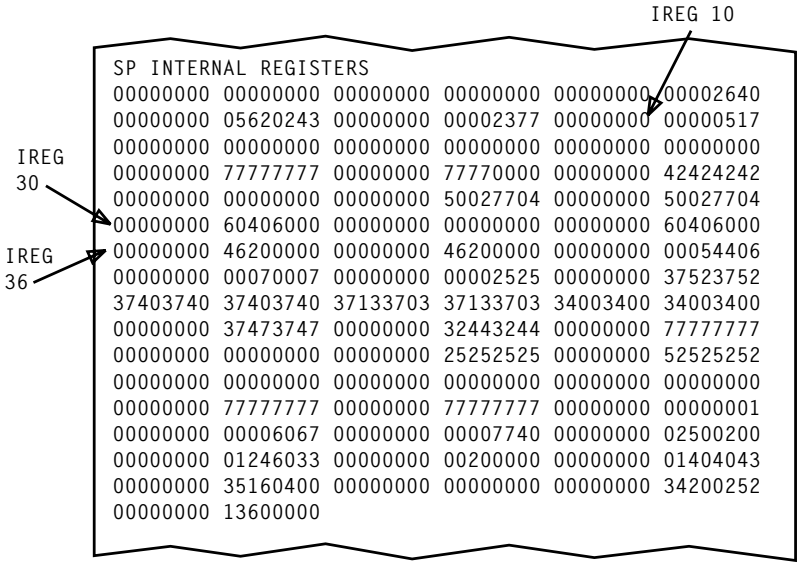


FIG. 5 – SP Internal Register (IREG) Printout

NOTES

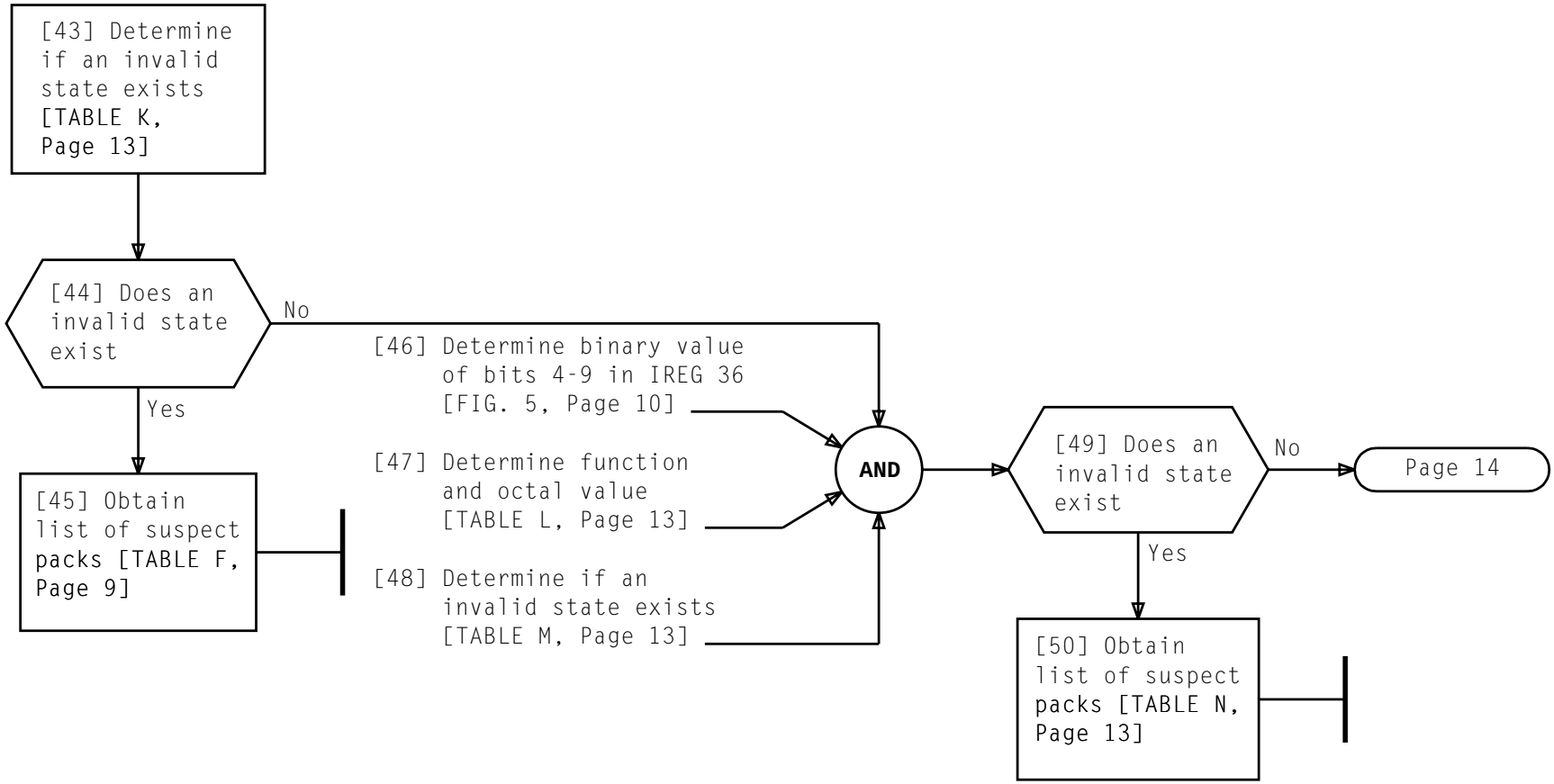
5. Bad pack could be in either controller
6. An SP-2 may have an associated pack not identified by verify message

ANALYZE SP2 F-LEVEL INTERRUPT

TABLE H FS10 CIRCUIT PACKS	
PACK TYPE	**LOCATION**
FA590	66-06,07,08,09
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA584	70-08,09,10,11
FA599	70-06,07,13

TABLE I FS 2 CIRCUIT PACKS	
PACK TYPE	**LOCATION**
FA531	74-14,15
FA534	74-16
FA528	74-27,24,22,23 74-19,21,17,20

TABLE J VERIFY MESSAGES		
CREG 36 BITS 7-9 VALUE	**CREG 10 BIT 8 VALUE**	**USE VERIFY MESSAGE**
0	0	VER:SPMTXPK:SCP,TSN o'a!
0	1	VER:SPMTXPK:SCP,MSN o'a!
≠ 0	0	VER:SPMTXPK:SDM,TDN o'a!
≠ 0	1	VER:SPMTXPK:SDM,MDN o'a!
a = TSN, MSN, TDN, or MDN octal number		



ANALYZE SP2 F-LEVEL INTERRUPT

TABLE K
INVALID SCAN SEQUENCER STATES

BIT	8	7	6	5	4
VALUE	1	0	1	0	0
		1	0	1	0
			0	1	1
			1	0	0
				0	1
				1	0
					1

TABLE L
FUNCTION AND VALUE OF MATRIX SEQUENCER

BIT			FUNCTION	BIT			OCTAL VALUE	BIT			FUNCTION	BIT			OCTAL VALUE
9	8	7		6	5	4		9	8	7		6	5	4	
0	0	0	A	0	0	0	0	1	0	0	E	1	0	0	4
		1	B			1	1			1	F			1	5
	1	0	C		1	0	2		1	0	G		1	0	6
		1	D			1	3			1	H			1	7

TABLE M
INVALID MATRIX SEQUENCER STATES

FUNCTION	OCTAL VALUE							
	0	1	2	3	4	5	6	7
A				†	†	†		
B				†	†	†		
C								
D								
E			†	†				
F	†	†	†	†	†	†	†	†
G								
H			†	†				

TABLE N
MATRIX SEQUENCER SUSPECT PACKS

PACK TYPE	LOCATION
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA599	70-06, 07
FA599	74-13
FA616	66-20

ANALYZE SP2 F-LEVEL INTERRUPT

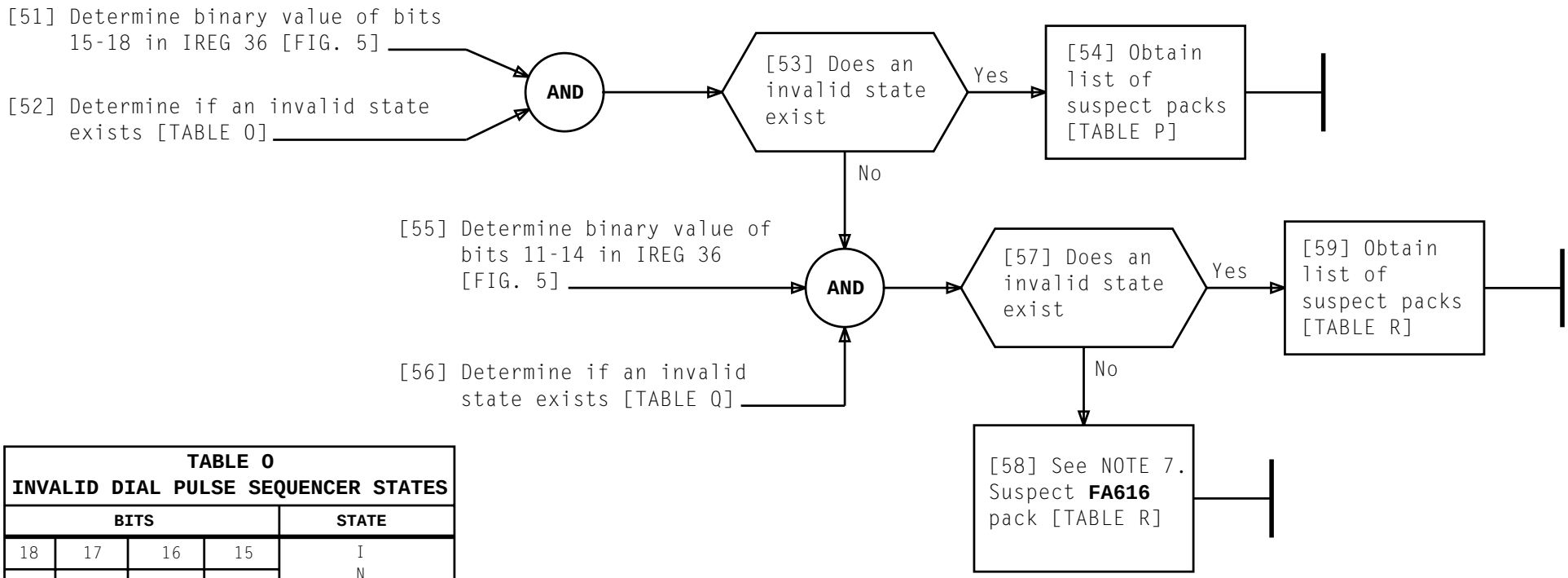


TABLE O
INVALID DIAL PULSE SEQUENCER STATES

BITS				STATE
18	17	16	15	
1	1	0	0	INVALID
			1	
		1	0	
			1	

TABLE P
FS14 CIRCUIT PACKS

PACK TYPE	LOCATION
FA577	62-14
FA576	62-20,21,23
FA621	62-22
FA602	62-19
FA588	66-40
FA616	66-20

TABLE Q
INVALID MF OUT SEQUENCER STATES

BIT				STATE
14	13	12	11	
1	0	1	1	INVALID
	1	0	0	
			1	
		1	0	
			1	

TABLE R
MF OUT SEQUENCER

PACK TYPE	LOCATION
FA666	66-23
FA615	66-19
FA588	66-40
FA577	66-33
FA581	66-30
FA616	66-20

NOTE 7
If trouble does not clear, check mate sequencers for invalid state

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ANALYZE SP2 F-LEVEL INTERRUPT

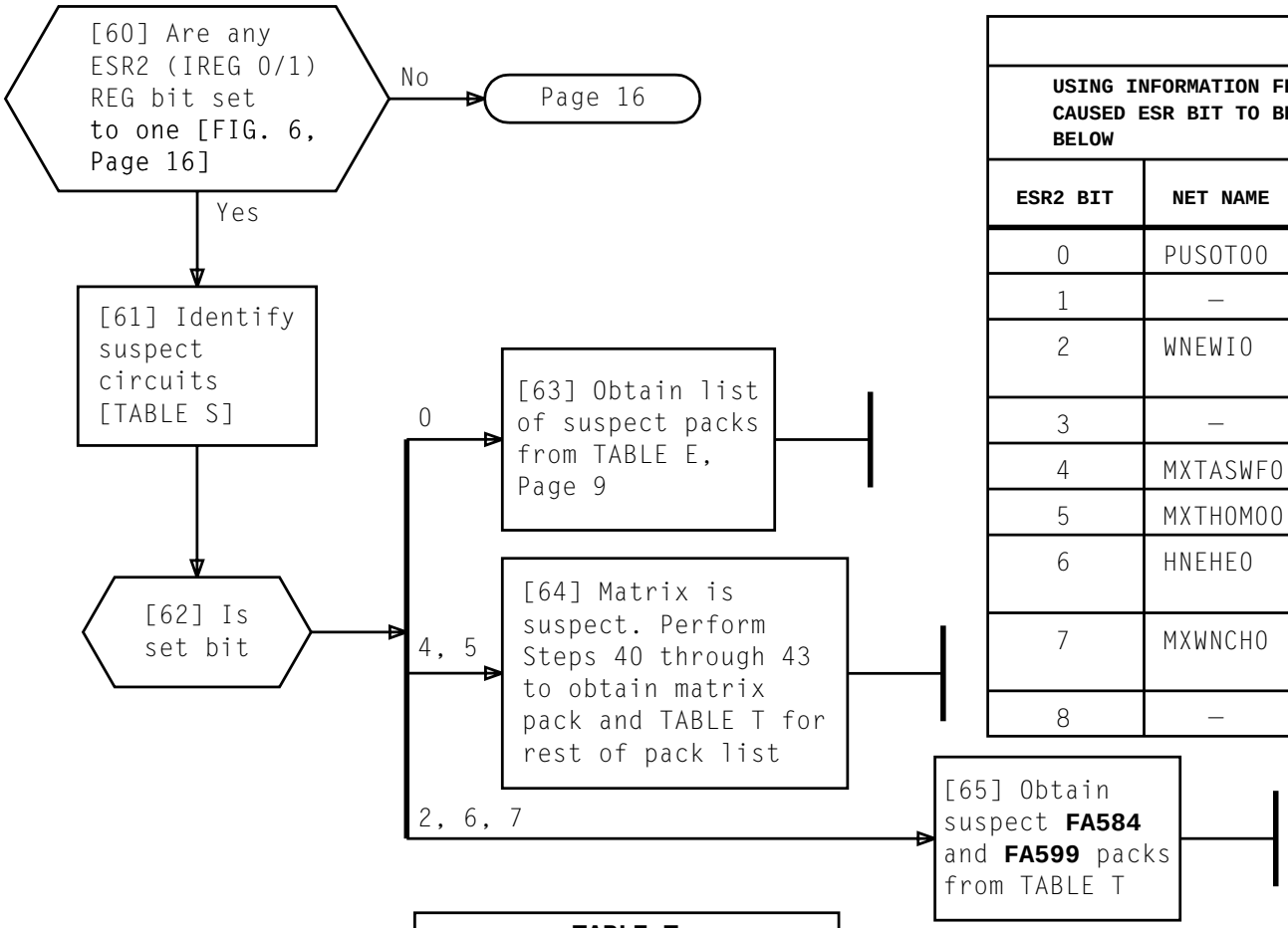


TABLE S

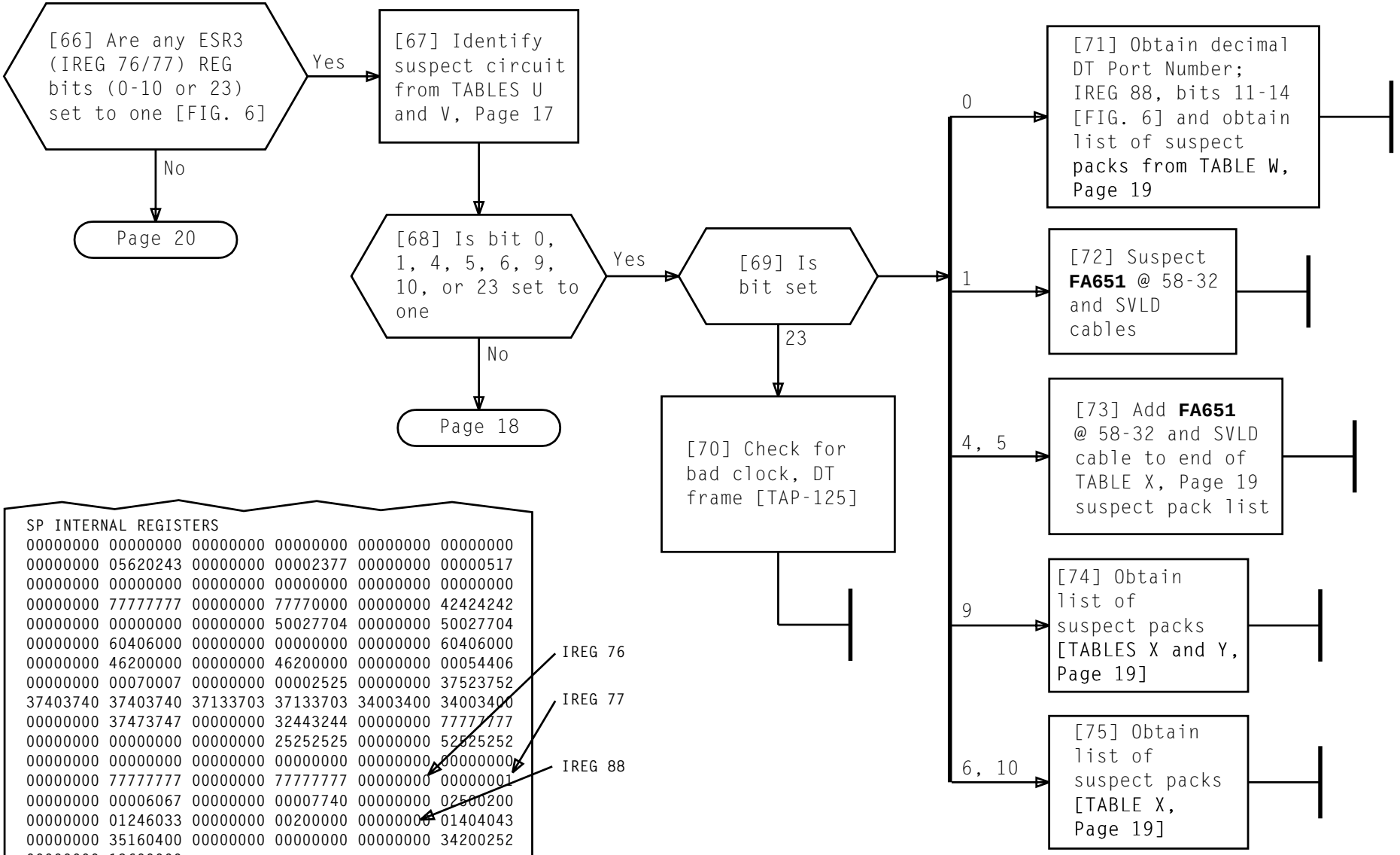
USING INFORMATION FROM TABLE D, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A067 USING CHART BELOW

ESR2 BIT	NET NAME	SOURCE FS/SYMBOL	COMMENTS
0	PUSOT00	17/8	PU sequencer time-out
1	—	—	—
2	WNEWI0	10/3	Matrix work-work register mismatch
3	—	—	—
4	MXTASWF0	10/26	Matrix ASW failure
5	MXTHOM00	10/27	Matrix homogeneity failure
6	HNEHE0	10/3	Matrix hold-hold register mismatch
7	MXWNCH0	10/10	Matrix work-hold register mismatch
8	—	—	—

TABLE T
BIT 4, 5 SUSPECT PACK LIST

PACK TYPE	LOCATION
FA584	70-08, 09, 10, 11
FA599	70-06, 07, 13
FA1191	70-14
FA1192	70-13
FA1193	70-12
FA590	66-06, 07, 08, 09

ANALYZE SP2 F-LEVEL INTERRUPT




```
SP INTERNAL REGISTERS
00000000 00000000 00000000 00000000 00000000 00000000
00000000 05620243 00000000 00002377 00000000 00000517
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77770000 00000000 42424242
00000000 00000000 00000000 50027704 00000000 50027704
00000000 60406000 00000000 00000000 00000000 60406000
00000000 46200000 00000000 46200000 00000000 00054406
00000000 00070007 00000000 00002525 00000000 37523752
37403740 37403740 37133703 37133703 34003400 34003400
00000000 37473747 00000000 32443244 00000000 77777777
00000000 00000000 00000000 25252525 00000000 52525252
00000000 00000000 00000000 00000000 00000000 00000000
00000000 77777777 00000000 77777777 00000000 00000001
00000000 00006067 00000000 00007740 00000000 02500200
00000000 01246033 00000000 00200000 00000000 01404043
00000000 35160400 00000000 00000000 00000000 34200252
00000000 13600000
```

IREG 76

IREG 77

IREG 88

FIG. 6 — SP Internal Register (IREG) Printout

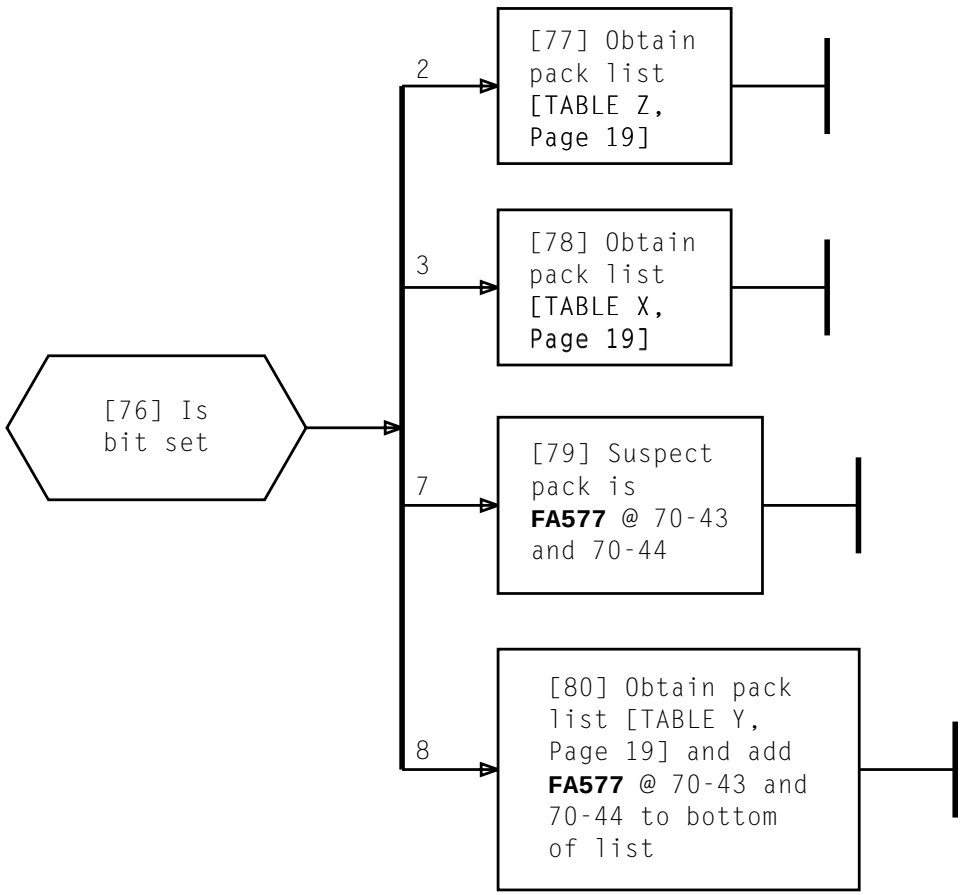
ANALYZE SP2 F-LEVEL INTERRUPT

TABLE U ESR3 — (SP-2 ONLY) IREG 76 AND 77		
BIT	**NAME**	**IMPLICATION**
0	TOK	The DT that this SP-2 was linked to had a transmitter failure
1	DTOCER	The DT that this SP-2 was linked to sent an invalid OPCODE
2	MSGSEQMM	Message sequencers mismatched. Suspect the message sequencer circuit
3	DTPSEQMM	The I/O sequencers mismatched. Suspect I/O sequencer circuit
4	DTBITER	Lost a bit timing from this DT
5	DTFRMER	Lost frame timing from DT
6	DTSAN	SP-2 did not process all DTs in time. Suspect loss of timing from DT
7	DTSERMM	Outgoing (to DT) data reclock registers mismatched. Suspect bad shift register.
8	DTSRMM	The shift registers between controllers mismatched. Suspect shift register or memory path
9	PARER	Parity error on incoming DT data
10	DTPCST	I/O sequencer in an invalid state

TABLE V

USING INFORMATION FROM TABLE F, RELATIONSHIP TO CIRCUIT WHICH CAUSED ESR BIT TO BE SET CAN BE FOUND IN SD-4A067 USING CHART BELOW

ESR3 BIT	NAME	FS/SYMBOL	COMMENTS
2	MSGSEQMM	25/4	Message storage sequencer mismatch
3	DTPSEQMM	23/1-4 22/9 20/8	I/O sequencer mismatch
7	DTSERMM	23/15 23/13	Serial reclock register mismatch
8	DTSRMM	23/15 24/1-16,20-29	Shift register mismatch
10	DTPCST	23/1.2	I/O sequencer in invalid state



ANALYZE SP2 F-LEVEL INTERRUPT

TABLE W
FS22 CIRCUIT PACKS

PORTS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PACK TYPE	LOCATIONS*															
FA524	13	12	11	10	22	21	20	19	49	48	47	46	60	59	58	57
FA533	16 (C1 DRIVER) 15 (CO DRIVER)				25 (C1 DRIVER) 24 (CO DRIVER)				52 (C1 DRIVER) 51 (CO DRIVER)				63 (C1 DRIVER) 62 (CO DRIVER)			
FA649	14 (SWITCH DRIVER)				23 (SWITCH DRIVER)				50 (SWITCH DRIVER)				61 (SWITCH DRIVER)			

* All packs in vertical location 58

TABLE X
FS23 CIRCUIT PACKS

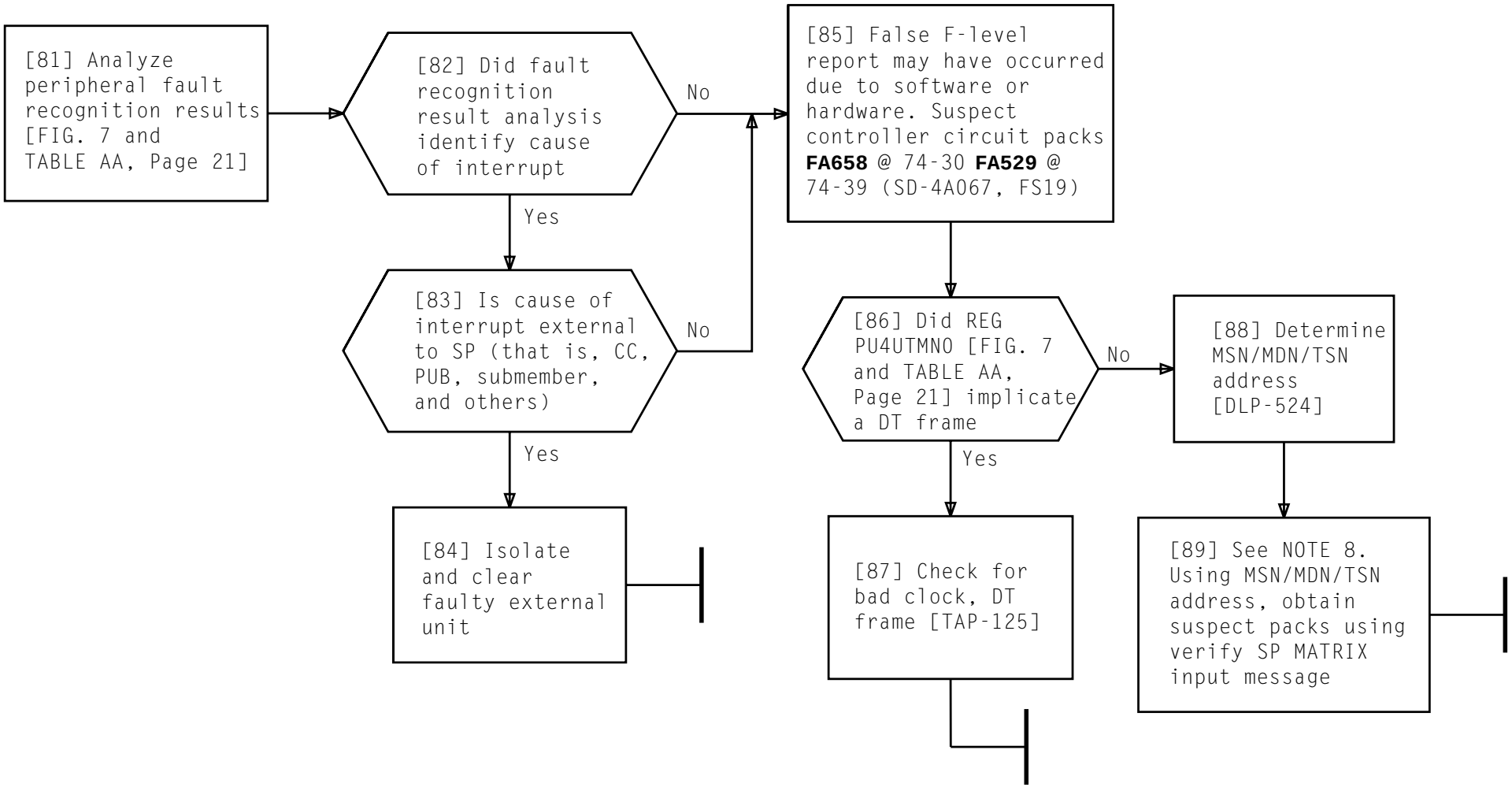
PACK TYPE	LOCATION
FA654	58-28
FA650	62-41
FA656	58-31
FA657	58-27
FA577	70-43,44

TABLE Y
FS24 CIRCUIT PACKS

PACK TYPE	LOCATION
FA1196	66-50,49,43,42
FA650	62-41
FA531	66-51
FA531	62-44

TABLE Z
FS25 CIRCUIT PACKS

PACK TYPE	LOCATION
FA652	58-29
FA655	58-26
FA653	58-30
FA651	58-32



NOTE 8
An SP-2 has associated pack not identified by verify message

ANALYZE SP2 F-LEVEL INTERRUPT

TABLE AA
PERIPHERAL FAULT RECOGNITION RESULTS

IDENTIFICATION OF REGISTERS IN RESULTS TABLE OF F-LEVEL MESSAGE

PU4RESULT PU4UTMNO PU4FRPMD PU4FRJRG

PU4RESULT ----------NMLKJIHGFEDCBA

Bit	0	A = CC0 found faulty
	1	B = CC1 found faulty
	2	C = Controller 0 found faulty
	3	D = Controller 1 found faulty
	4	E = PU bus 0 found faulty
	5	F = PU bus 1 found faulty
	6	G = PU bus 0 at unit found faulty
	7	H = PU bus 1 at unit found faulty
	8	I = Faulty unit or subunit to be removed and diagnosed
	9	J = Faulty unit or subunit to be removed
	10	K = Fault recognition was unable to find the fault
	11	L = Fault recognition found that a software error caused the F-level
	12	M = Fault recognition found that a transient caused the F-level
	13	N = Signal processor matrix found faulty

PU4UTMNO DDDDDDDCCCCCCCBAAAAAAA--

Bits	2-8	A = Submember found faulty (if any)
	9	B = Set if submember found faulty
	10-16	C = Member number found faulty
	17-23	D = Unit type found faulty

PU4FRPMD --CCCCCCCBBBBBBBAAAAAAAA

Bits	0-7	A = Point of maximum definition MACRO number relative to an FR program
	8-14	B = Fault recognition decision code
	15-21	C = Error analysis action code

PU4FRJRG = FR program address where error was located

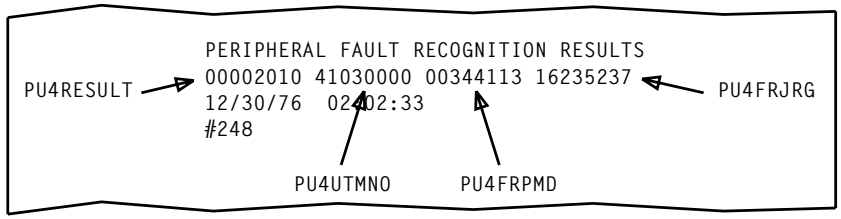


FIG. 7 — Peripheral Fault Recognition Results Printout

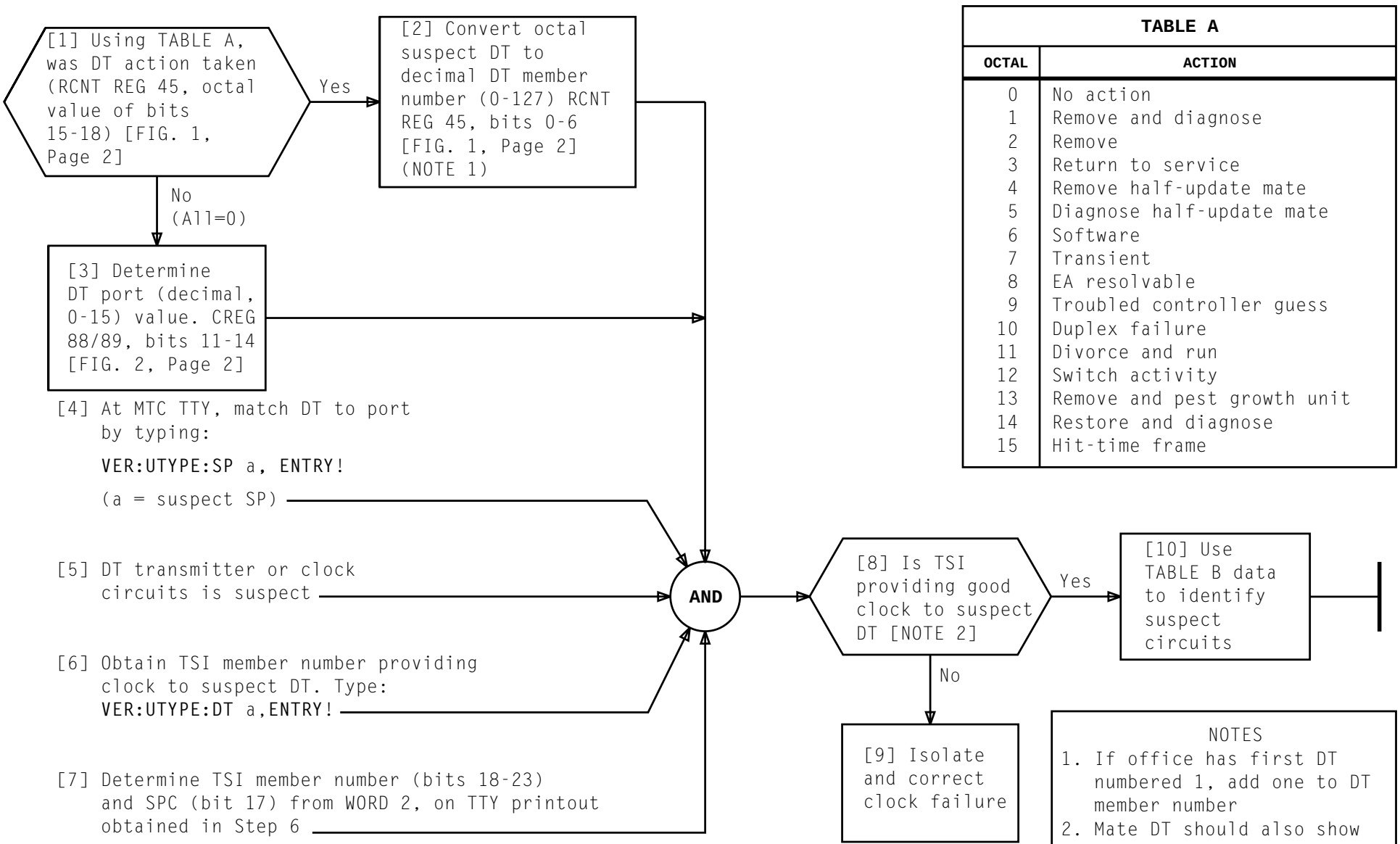


TABLE A

OCTAL	ACTION
0	No action
1	Remove and diagnose
2	Remove
3	Return to service
4	Remove half-update mate
5	Diagnose half-update mate
6	Software
7	Transient
8	EA resolvable
9	Troubled controller guess
10	Duplex failure
11	Divorce and run
12	Switch activity
13	Remove and pest growth unit
14	Restore and diagnose
15	Hit-time frame

NOTES

1. If office has first DT numbered 1, add one to DT member number
2. Mate DT should also show errors if TSI is providing bad clock

ANALYZE SPFR F-LEVEL INTERRUPT, CLOCK CHECK, DIGITAL TERMINAL

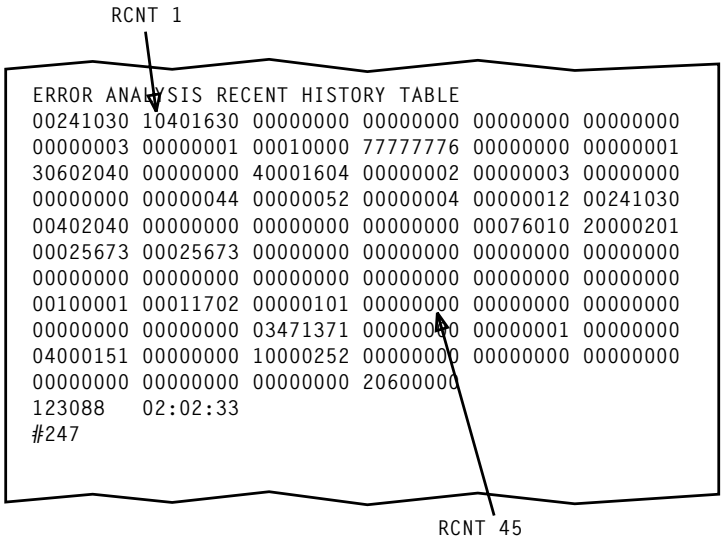


FIG. 1 - RCNT Register Printout

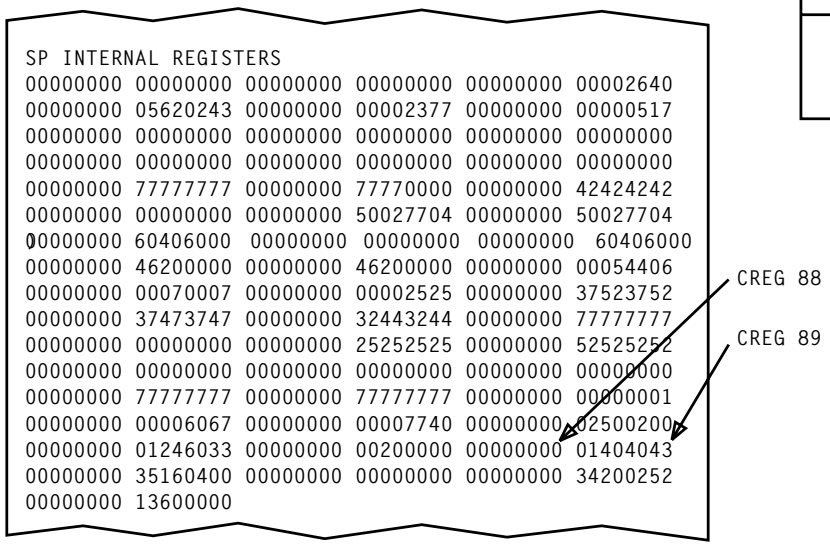


FIG. 2 - SP Critical Register (CREG) Printout

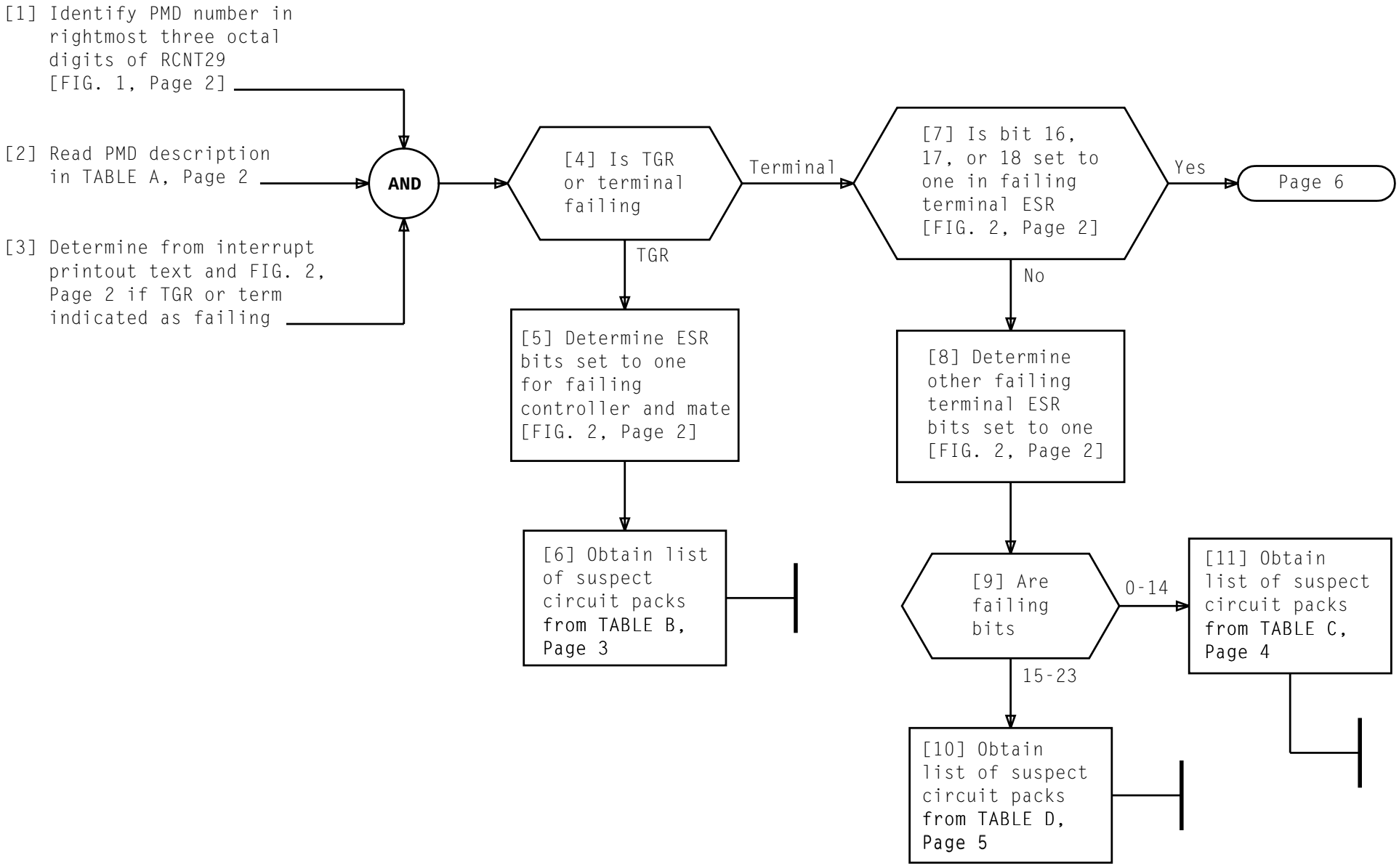
TABLE B
DT SUSPECT CIRCUITS

USING ESR3 INFORMATION IMPLICATING DT, SUSPECT CIRCUIT CAN BE FOUND

ESR3 BIT	LEAD NAME	DT SD-6G114 FS/SYMBOL	SP2 SD-4A067 FS/SYMBOL	COMMENT
0	TOKO	FS 17 FS 18	22/9,18,27,36	Transmitter OK error
*1	DTOCER	FS 17	25/3	Invalid OPCODE
*4	DTBITER	FS 17	23/15 22/9,18,27,36	DT lost bit timing
*5	DTFRMER	FS 17	23/15 22/9,18,27,36	DT lost frame timing
*6	DTSAN	FS 17	23/3,15	SP-2 did not finish processing DTs in time
*7	DTPARER	FS 17	24/19 22/9	Incoming DT parity error

* If TOK is not up, there is only one CKT pack (**FA1188**) on FS 17 which can cause bit 1,4,5,6, or 7 to come up

ANALYZE SPFR F-LEVEL INTERRUPT, CLOCK CHECK, DIGITAL TERMINAL



ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

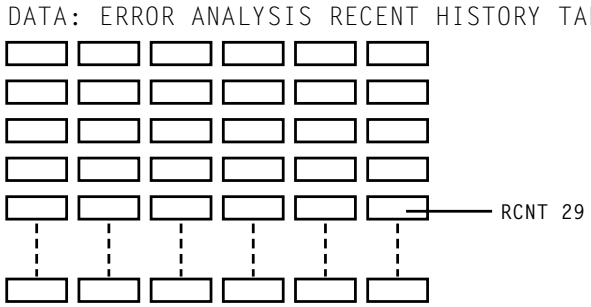


FIG. 1 — Recent History Data

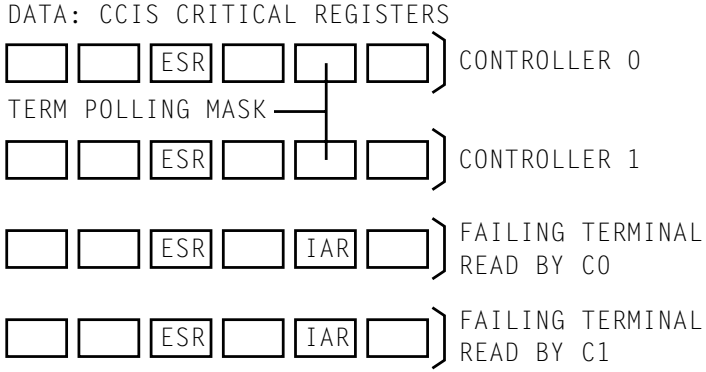


FIG. 2 — CCIS Critical Registers

TABLE A
PMD DESCRIPTIONS

PMD*	DESCRIPTION	PMD*	DESCRIPTION
1, 2	MTCE OPCODE failure (OPCODE ≥ 100)	17, 20	Terminal stopped. Terminal hardware error
3, 4	Invalid TGR OPCODE	21, 22	Terminal retry passed through original controller— transient error
5, 6	Order to unequipped terminal		
7, 10	Retry of TAC order passed — transient error	23, 24	Terminal retry passed through mate. Problem in original controller
11, 12	TAC order retry failed — hard fault in controller	25, 26	Terminal retry failed through both controllers. Terminal hardware suspect
13, 14	Quarantine bit not set in active controller— configuration problem		
15, 16	Terminal accessed was out of service. Check terminal polling mask		

* Odd PMDs — Both controllers in service before interrupt
Even PMDs — Only even controller in service before interrupt

TABLE B
CONTROLLER ESR

BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS*
0	ASWF	All-seems-well failure	**FA824**	02-19	8
1	—	Unassigned			
2	PFE	Parity failure — even	**FA534** **FA534**	06-22 06-23	4
3	PFO	Parity failure — odd	**FA534** **FA534**	06-22 06-23	4
4	TDPF	Terminal data parity failure	**FA824**	02-19	6
5	NTASW	No terminal all-seems-well			6
6	EASW	Erroneous all-seems-well	**FA822**	02-18	6
7	QUAR	Quarantine	—	—	—
8	OPDF	OPCOPE decoder failure	**FA820** **FA821** **FA825**	02-20 02-21 06-20	5
9	DIF	Data transfer failure	**FA534**	06-23	4
10	VOC	Valid OPCODE	**FA822**	02-18	6
11	—	Unassigned	—	—	—

* SD-4A057-01

TABLE C
TERMINAL ESR BITS 0-14

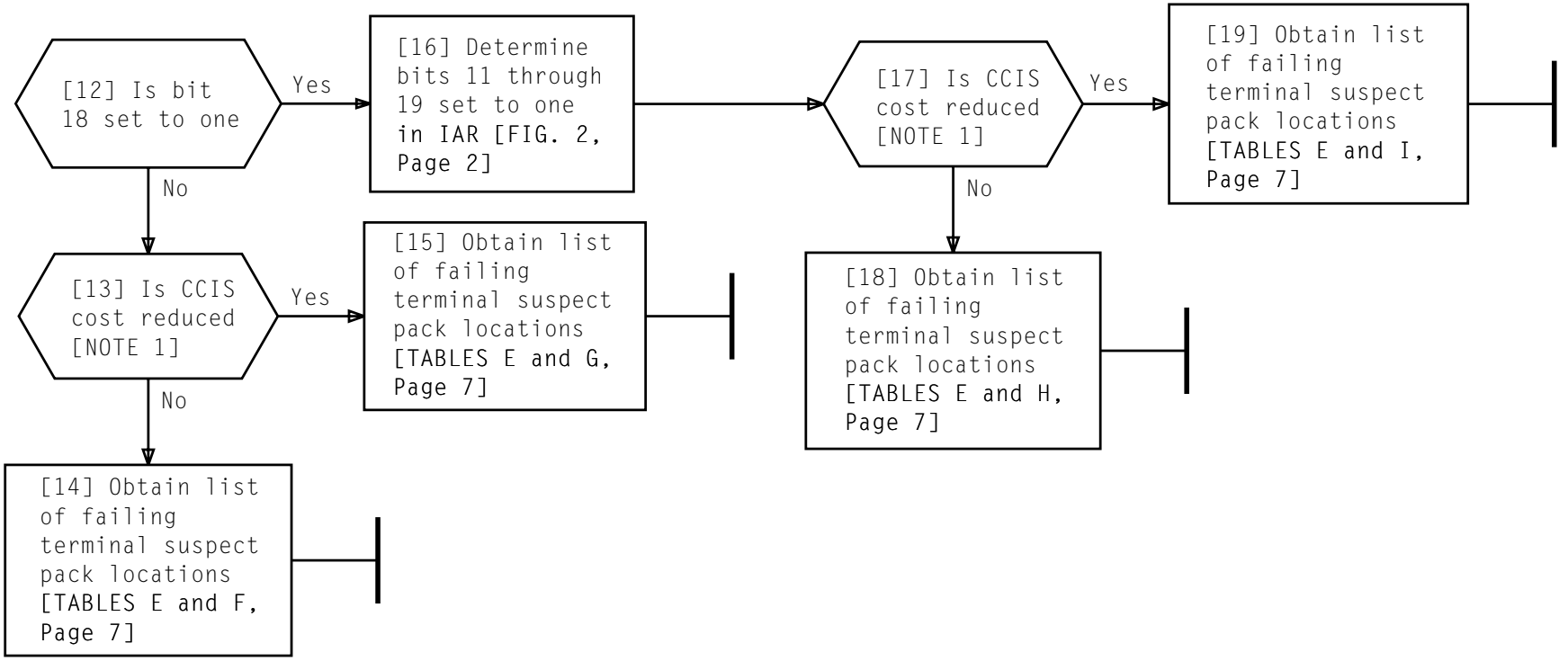
BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS†
0-5	—	Unassigned	—	—	—
6	DSR	Data set ready	*	04-39	1
7	SDATA	Transmitter data	**FA795**	02-12	1
8	RDATA	Receive data	*	04-39	1
9	PESUMB	Partial error summary B (12, 13, 15, 17)	**FA792** **FA790** **FA791** **FA788** **FA789**	02-14 02-13 06-14 02-17 02-16	4 4 4 4 4
10	PESUMA	Partial error summary A (14, 16, 18, 20)	**FA792** **FA790** **FA791** **FA788** **FA789**	02-14 02-13 06-14 02-17 02-16	4 4 4 4 4
11	ESUM	Error summary (A & B)	**FA792** **FA790** **FA791** **FA788** **FA789**	02-14 02-13 06-14 02-17 02-16	4
12	LLA	Link list address error	**FA791**	06-14	4
13	LLD	Link list data failure	—	—	4
14	TBDOF	Transmit bit overflow	**FA795**	02-12	1

* Office-dependent † SD-94833-01

TABLE D
TERMINAL ESR BITS 15-23

BIT	NAME	FUNCTION	PACK TYPE	SUSPECT PACK LOCATION	ASSOCIATED FS*
15	RBOF	Receive bid overflow	**FA795**	02-12	1
16	DCP	Data memory C parity	**FA791**	06-14	4
17	DABP	Data memory AB parity			4
18	PMP	Program memory parity			2
19	LNRP	I/O list number error			4
20	IODEC	I/O decoder error			4
21	IOPBOF	I/O put buffer overflow			1
22	IODP	I/O data parity			1
23	IOOCP	I/O OPCODE parity	**FA794**	02-06	1

* SD-94833-01



NOTE 1
Cost reduced frame does not have packs in terminal locations 02-26, 27 and 06-28, 29

ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

TABLE E

TERM.	BAY	STARTS AT VERTICAL
0	0	33
1		41
2		56
3	1	33
4		41
5		56
6		25
7		33
8	Left supl.	41
9		56
10		66
11	Right supl.	25
12		33
13		41
14		56
15		66

TABLE F

NON-COST REDUCED TERMINAL SUSPECT PACK LOCATIONS

ESR BIT 16	ESR BIT 17
06-12* 06-13	02-09 02-10 02-11* 02-12* 06-09 06-10 06-11* 06-12* 06-13*

*Optional pack

TABLE G

COST REDUCED TERMINAL SUSPECT PACK LOCATIONS

ESR BIT 16	ESR BIT 17
06-12	02-09 02-10 06-09 06-10 06-12

TABLE H

NON-COST REDUCED TERMINAL SUSPECT PACK LOCATIONS

ESR BITS 12-19	ESR BIT 11=0	ESR BIT 11=1
Bit 12 = 1	02-22	06-22
Bit 13 = 1	02-23	06-23
Bit 14 = 1	02-24	06-24
Bit 15 = 1	02-25	06-25
Bit 16 = 1	02-26	06-26
Bit 17 = 1	02-27	06-27
Bit 18 = 1	02-28	06-28
Bit 19 = 1	02-29*	—

*Optional pack

TABLE I

COST REDUCED TERMINAL SUSPECT PACK LOCATIONS

ESR BITS 12-19	ESR BIT 11=0	ESR BIT 11=1
Bit 12 = 1	02-22	06-22
Bit 13 = 1		
Bit 14 = 1	02-23	06-23
Bit 15 = 1		
Bit 16 = 1	02-24	06-24
Bit 17 = 1		
Bit 18 = 1	02-25	06-25
Bit 19 = 1		

ANALYZE CCISFR F-LEVEL INTERRUPT, COMMON CHANNEL INTEROFFICE SIGNALING FRAME

[1] Determine octal PMD number from rightmost three digits of the RCNT+29 register and record [FIG. 1, Page 2]

In TABLE A, Page 5:

[2] Identify row for location of PMD number that was determined in Step 1

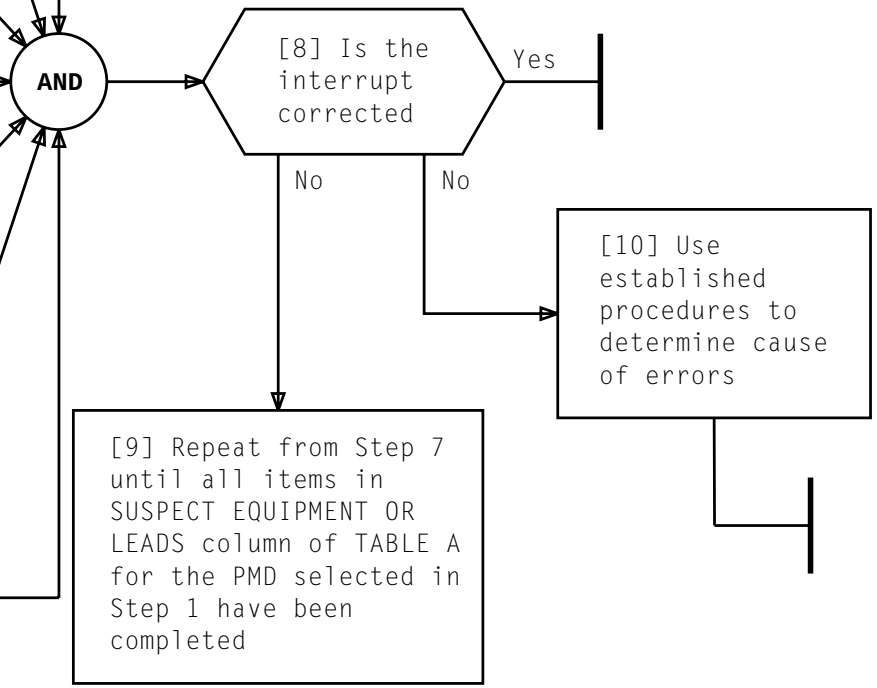
[3] Identify the active or mate controller as required from bit 7 of the STATR register [FIG. 2, Page 3] and record

[4] Identify ESU reporting errors by using position of set bit in the USR (unit error summary) register [FIG. 2, Page 3] and record

[5] Determine the bits or conditions to be inhibited using the position of bits in UPR (unit pest register) [FIG. 2, Page 3] and record

[6] Locate and identify the bits in the last look memory [FIG. 3, Page 4] that are set to one and record

[7] Perform activities listed in the SUSPECT EQUIPMENT/LEADS column by doing one at a time starting with the first item listed in TABLE A, Page 5



ANALYZE ESFR INTERJECT

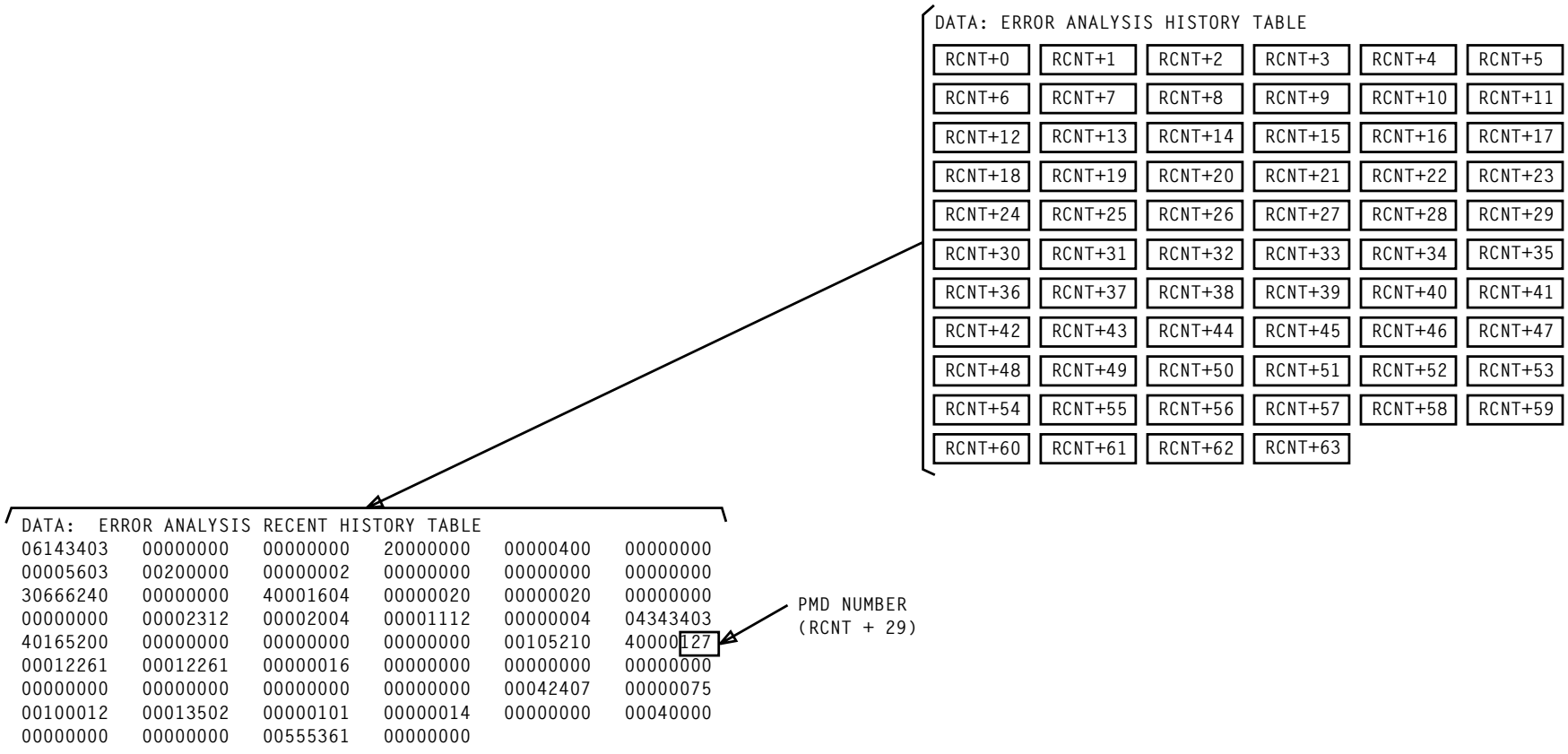


FIG. 1 — Third Part of EST Interject Printout

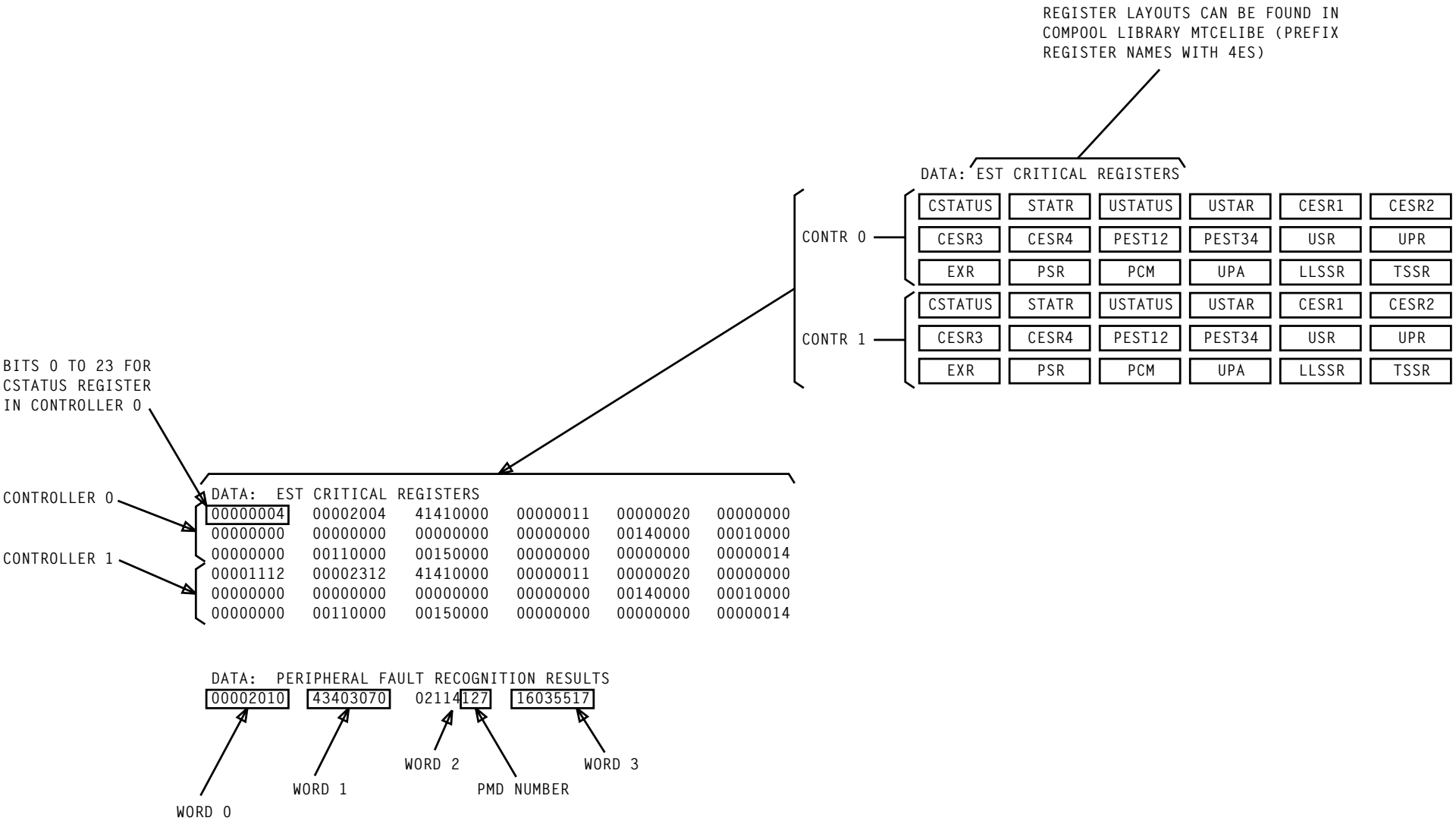


FIG. 2 – Second Part of EST Interject Printout

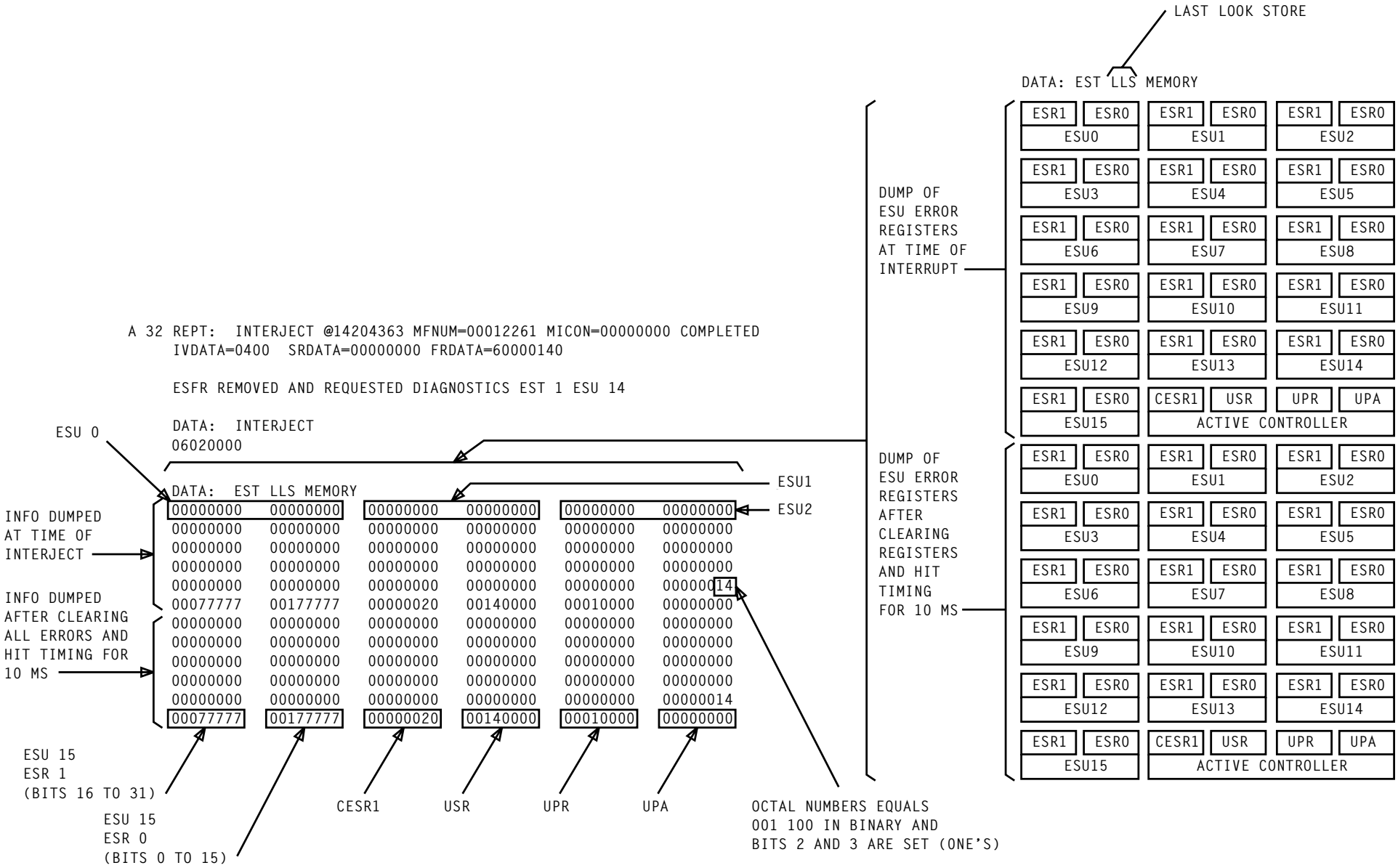


FIG. 3 — First Part of EST Interject Printout

ANALYZE ESFR INTERJECT

TABLE A							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
120	Both controllers in service. APUT set in active and not set in mate	Mate controller	Bit 7 equals zero in mate controller	—	—	—	1. Suspect circuit packs in mate controller that are listed in TABLE B, Page 13 2. Use established office procedures to determine cause of errors in circuitry associated with a INAPUTN LEAD (a = mate controller)
121	Both controllers in service. APUT set in mate and not set in active. Mate USR have bits set	Active controller	Bit 7 equals one in active controller	—	—	—	1. Suspect circuit packs in active controller that are listed in TABLE B, Page 13 2. Use established office procedures to determine cause of errors in circuitry associated with a INAPUTN LEAD (a = active controller)

TABLE A (Contd)							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
122	APUT set in active controller. Same bits set in active USR at interrupt and after 10 ms hit timing delay	ESUs that are alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	—	1. Check cabling between shelf of ESU reporting errors and controller packs of active controller 2. Check backplane wiring from ESU packs reporting to shelf connector 3. Suspect circuit packs in active controller that are listed in TABLE C, Page 13
123	APUT set in active controller. Active USR had bits set. All bits not set at interrupt and after 10 ms hit delay timing	ESUs that are alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	—	1. Check cabling between shelf of ESU reporting errors and controller packs of active controller 2. Check backplane wiring from ESU packs reporting to shelf connector 3. Suspect circuit packs in active controller that are listed in TABLE C, Page 13

TABLE A (Contd)							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
124	APUT set in active controller. Active USR had one bit set. Bit was set at interrupt and not set after 10 ms hit timing delay	ESU that is alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at the time of interrupt for ESU reporting errors and interpret meaning	1. Suspect in ESU that are listed in TABLE D, Page 13, and have error bits set to one 2. Check leads and associated circuitry that are listed in TABLE E, Page 13, and have corresponding bits in the ESR register set to one
125	APUT set in active controller. Active found unpested, unequipped, growth, or special growth ESUs reporting errors	Active controller	Bit 7 equals one in active controller	—	If bits equal one in positions that represent growth or special growth ESUs, do nothing (program pested ESUs). If bits that are equal to one represent other equipped ESUs, replace packs in suspect Equipment/Leads column	—	Suspect NH27 and NH32 circuit packs at locations called out in TABLE C, Page 13

TABLE A (Contd)							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
126	APUT set in active controller. No ESU errors reported through active controller when interrupt occurred	Active controller	Bit 7 equals one in active controller	—	—	—	Suspect NH26 and NH27 circuit packs at locations called out in TABLE C, Page 13
127	APUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing	ESU that is alarming	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also after 10 ms hit delay timing and interpret meaning	1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one

TABLE A (Contd)							
PMD		SIGNIFICANT REGISTER INDICATIONS					SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
130	APUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing. (ESRO bits 4-7)	TSI DS120 line or ESU circuitry on TSI side	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also 10 ms hit delay timing and interpret meaning	1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one 3. Check DS120 line between TSI and ESU reporting errors
131	APUT set in active controller. One ESU reporting errors through active controller. Same errors reported when interrupt occurred and after 10 ms hit delay timing	VIF/DF/DIF DS120 line or ESU circuitry on VIF/DT/ DIF side	Bit 7 equals one in active controller	ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	Identify ESR bits set to one at time of interrupt and also 10 ms hit delay timing and interpret meaning	1. Suspect packs in ESU that are listed in TABLE D, Page 13, and have error bits set to one and ESU reporting errors 2. Check leads and associated circuitry that are listed in TABLE E, Page 14, and have corresponding bits in the ESR register set to one

TABLE A (Contd)							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
132	APUT set in active controller. One ESU reporting errors as indicated by active controller USR bit set. No error bits set in ESR thru active controller	Active controller	Bit 7 equals one in active controller	If both controllers are in service prior to interrupt, ESU reporting errors is identified by bit position that is equal to one in active controller	Ignore ESU reporting errors as indicated by USR bit equal to one if UPR bit in corresponding position also equals one	—	1. If one controller is out of service prior to interrupt, suspect NH32 circuit pack in active controller at location called in TABLE C, Page 13 2. If both controllers are in service perform the following: a. Check cabling between ESU shelf and controller packs or backplane wiring from ESU packs to shelf connector 2. Suspect NH31 and NH32 circuit packs in controller that was active prior to interrupt at locations called out in TABLE C, Page 13

TABLE A (Contd)							
PMD			SIGNIFICANT REGISTER INDICATIONS				SUSPECT EQUIPMENT OR LEADS
PMD NUMBER	DEFINITION	SUSPECT UNIT	STATR FIG. 2	USR FIG. 2	UPR FIG. 2	ESR FIG. 3	
133	APUT set in active and mate controller. No USR bits set in mate controller	Mate controller	—	—	—	—	1. Suspect NH26 and NH27 circuit packs in both controllers at locations called out in TABLE C, Page 13 2. Check for multiple hardware faults in mate controller
134	APUT not set in active or mate controller	Mate controller	—	—	—	—	Request technical assistance per local office practice
135	APUT not set in active and mate is out of service	Active controller					Request technical assistance per local office practice
136	APUT set in mate and not set in active controller. No USR bits set in mate controller	Mate controller	Bit 7 equals one in mate controller	—	—	—	Suspect NH26 and NH27 circuit packs in mate controller at locations called out in TABLE C, Page 13

TABLE B		
PACK	CONTR 0	CONTR 1
NH32	064-09	064-14
NH33	055-11	055-12
NH31	064-08	064-15
NH27	073-09	073-14

TABLE C		
PACK	CONTR 0	CONTR 1
NH33	055-11	055-12
NH32	064-09	064-14
NH31	064-08	064-15
NH27	073-09	073-14
NH26	073-07	073-16

TABLE D
ESU SUSPECT PACK LOCATIONS ASSOCIATED WITH ESR BITS

ESR →	ESR0						ESR1		
BITS →	0-3	4-7	8,9	10-12	13	14,15, 0	1-3	4-8	9-10
PACK / ESU	NH2 LOCATION	NH3 LOCATION	NH1 LOCATION	NH4 LOCATION	NH6 LOCATION	NH5 LOCATION	NH5 LOCATION	NH8 LOCATION	NH7 LOCATION
0	028-07	028-09	028-08	028-06	028-01	028-04	028-02	028-10	028-11
1	028-16	028-14	028-15	028-17	028-22	028-19	028-21	028-13	028-12
2	037-07	037-09	037-08	037-06	037-01	037-04	037-02	037-10	037-11
3	037-16	037-14	037-15	037-17	037-22	037-19	037-21	037-13	037-12
4	046-07	046-09	046-08	046-06	046-01	046-04	046-02	046-10	046-11
5	046-16	046-14	046-15	046-17	046-22	046-19	046-21	046-13	046-12
6	128-07	128-09	128-08	128-06	128-01	128-04	128-02	128-10	128-11
7	128-16	128-14	128-15	128-17	128-22	128-19	128-21	128-13	128-12
8	137-07	137-09	137-08	137-06	137-01	137-04	137-02	137-10	137-11
9	137-16	137-14	137-15	137-17	137-22	137-19	137-21	137-13	137-12
10	146-07	146-09	146-08	146-06	146-01	146-04	146-02	146-10	146-11
11	146-16	146-14	146-15	146-17	146-22	146-19	146-21	146-13	146-12
12	155-07	155-09	155-08	155-06	155-01	155-04	155-02	155-10	155-11
13	155-16	155-14	155-15	155-17	155-22	155-19	155-21	155-13	155-12
14	164-16	164-14	164-15	164-17	164-22	164-19	164-21	164-13	164-12

TABLE E
ESU (LLS MEMORY) ERROR SOURCE REGISTER BITS

ESR	BIT	LEAD	FUNCTION MONITORED	SIGNAL MONITORED
0	0	UESB0	VIF/DT/DIF input framing	GBC3
	1	UESB1		1MHz clock (PHX)
	2	UESB2	VIF/DT/DIF output parity	Serial data parity
	3	UESB3	VIF/DT/DIF output parity	Serial data parity
	4	UESB4	TSI input framing	GBC3
	5	UESB5		1MHz clock (RCK1)
	6	UESB6	TSI output parity	Serial data parity
	7	UESB7	TSI output parity	Serial data parity
	8	UESB8	RCV line driver out	ROUT
	9	UESB9	XMT line driver out	TOUT
	10	UESB10	Each error source bit observes 8 monitor points through an 8-bit parity generator. Odd parity across 8 monitor points is compared with a reference bit from controller	PYUCC at TS 124
	11	UESB11		PYUCB at TS 124
	12	UESB12		PYUCA at TS 124
	13	UESB13		PYTDA at TS 124
	14	UESB14		PFSCA at TS 124
	15	UESB15		PFSCB at TS 124
1	0	UESB16		PFSCC at TS 124
	1	UESB17		PSSCA at TS 124
	2	UESB18		PSSCB at TS 124
	3	UESB19		PSSCC at TS 124
	4	UESB20	TRK status store E/D	TRK status TS 123
	5	UESB21	TRK status store S/F	TRK status TS 123
	6	UESB22	GGC counter SYNC	GGC SYNC
	7	UESB23	EST initialize	INITO
	8	UESB24	Good INTVL CNTR INIT	IGICO
	9	UESB25	GWC counter SYNC	GWCSYNC
	10	UESB26	Controller select	OASP, 1ASP

SUMMARY

Determine active controller and suspect controller. Locate and read PMD description in PR4A348. If no registers are identified which are listed in TABLE A, Page 4 suspect software problem and use established office procedures to determine cause of errors. Otherwise, determine if APUF or PUF source by using AC1INH and AC1INS registers. If APUF source, locate leads in SD5G168-01 for TABLE A PMD register bits set to one using TABLE B and SD lead index. If PUF source, identify OPCODE in AC1PRM register and use TABLE C to determine if read or write order. Locate leads in SD5G168 for TABLE A PMD register bits set to one using SD information, note 312, part B, write or read order information and SD lead index. For APUF or PUF source, suspect packs and leads that could cause lead names located to go active [NOTE 1].

[1] Determine active controller(CACT) and mate controller (CMATE) by noting which controller has bit 7 set to one in STATR register (CACT), and which controller has it set to zero (CMATE) [FIG. 1, Page 2 (EST critical registers)] and record results

[2] Determine suspect controller using bits 2 (CONTR 0) and 3 (CONTR 1) of PU4RESULT word [FIG. 1, Page 2]

[3] Identify and record octal PMD number [FIG. 1, Page 2]

[4] Locate **"PMD**abc**"** in PIDENT ESFRMAIN (PR4A348) cross reference section (abc = is octal PMD number) and record

[5] Note page and line number listed in DEF/REF column for **PMD**abc (abc = octal PMD number) and record

[6] Go to referenced page and line number and read **PMD**abc comments (abc = octal PMD number)

AND

[7] Are any registers listed in TABLE A, Page 4, for PMD number identified

No

[8] Use established office procedures to determine cause of errors

Yes

[9] Is word AC1INS bit 4 set to one (APUF) [FIG. 1, Page 2]

Yes

Page 3, Step 16

No

[10] Is word AC1INS bit 5 set to one (PUF) [FIG. 1, Page 2]

No

Yes

Page 3

NOTE 1

Lead names ending in P go high when active. Lead names ending in N go low when active

ANALYZE ESFR F LEVEL INTERRUPT

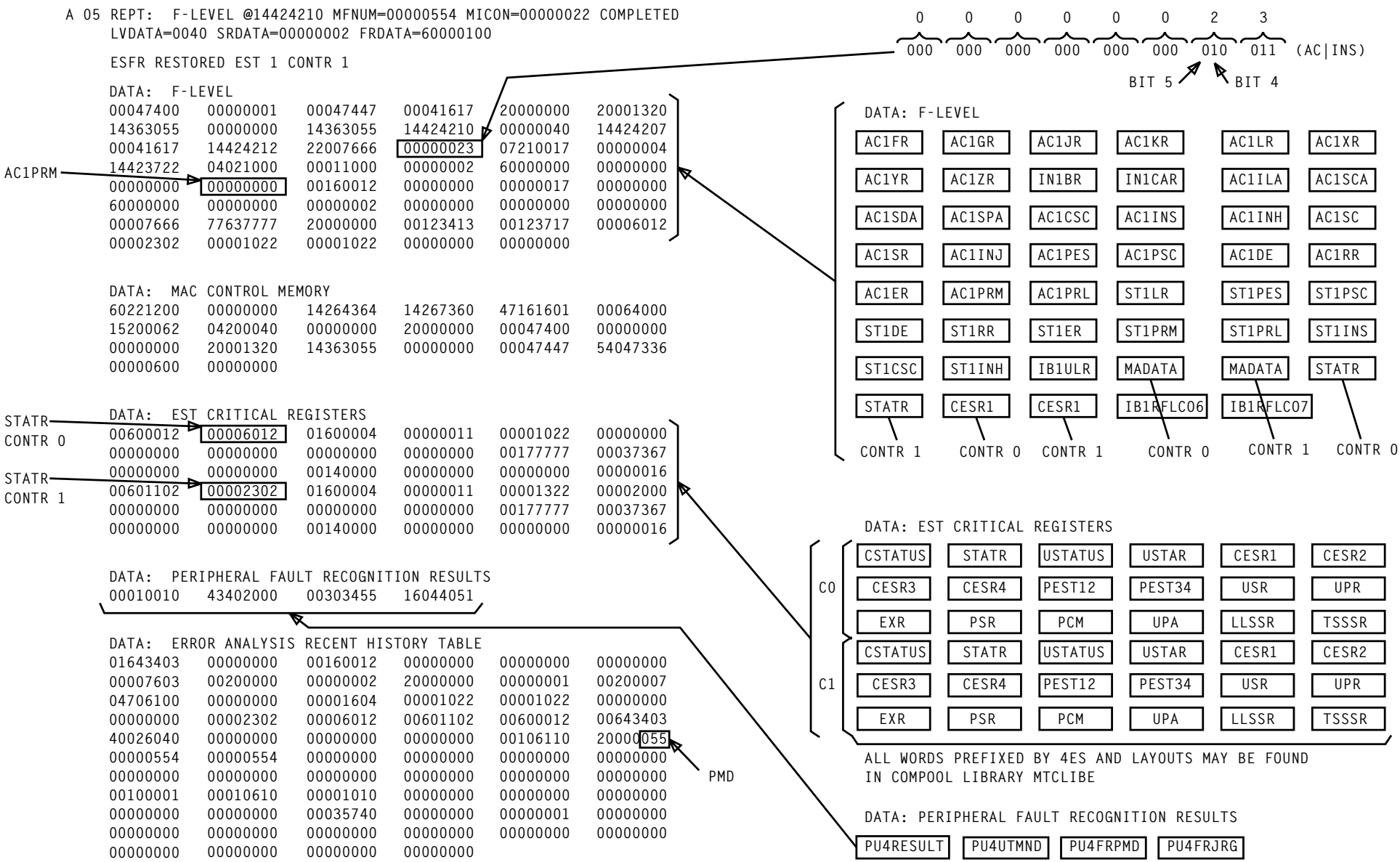


FIG. 1 — Interrupt Printout

ANALYZE ESFR F LEVEL INTERRUPT

[11] Determine OPCODE (octal) in bits 5-11 of word AC1PRM [FIG. 1, Page 2]

[12] See NOTE 2. Use TABLE C, Page 4, to determine if OPCODE was a read or write order

[13] Determine TABLE A, PMD register bits set to one for suspect controller identified in step 2 [FIG. 1, Page 2]

[14] Using information note 312, part B in SD5G168-01 (Sheets D9 and D10), identify write lead name (write order) or read lead name (read order) associated with register bits in TABLE A set to one

[15] See NOTE 3. Use SD lead index to locate each write or read lead name in an FS

AND

[20] See NOTE 1, Page 1. Suspect packs and leads that could cause net name leads located to go active

[21] Is problem corrected

Yes

No

[22] Use established office procedures to determine cause of errors

[16] Determine PMD register bits from TABLE A, Page 4, set to one for suspect controller identified in Step 2 [FIG. 1, Page 2]

[17] Using TABLE B, Page 4, locate SD5G168-01 information notes associated with suspect controller PMD registers having bits set to one

[18] See NOTE 3. For each suspect controller register bit set to one, note its net name and function

[19] See NOTE 3. Use SD lead index located at front of SDs to locate each net name lead in an FS

AND

NOTES

2. OPCODE actions described in SD5G168-01 information notes 325 and 326
3. Prefix lead names with suspect controller (0 or 1)

ANALYZE ESFR F LEVEL INTERRUPT

TABLE A

PMD	REGISTER	BITS
001	*	—
002, 004, 005, 007, 010, 014, 016, 020	MADATA	19,20
	CESR1	11
	CESR4	0
003, 006, 011, 012, 013, 015, 017	MADATA	20,19,6
	CESR1	11
	CESR4	0
021, 022	†	—
023, 024, 025, 026, 027, 030, 031, 032, 033	CESR1	0-15
	CESR2	0-11
	CESR3	0-15
	CESR4	0-11
035, 036, 037, 040, 041, 042, 043, 044, 045, 046, 047, 050, 051, 052, 053, 054, 055, 056, 057, 060, 061, 062, 070, 071, 072	CESR1	0-15
	CESR2	0-11
	CESR3	0-15
	CESR4	0-11
066, 067	††	—
073	†	—

* Duplex failure
† Suspect software
†† No errors found

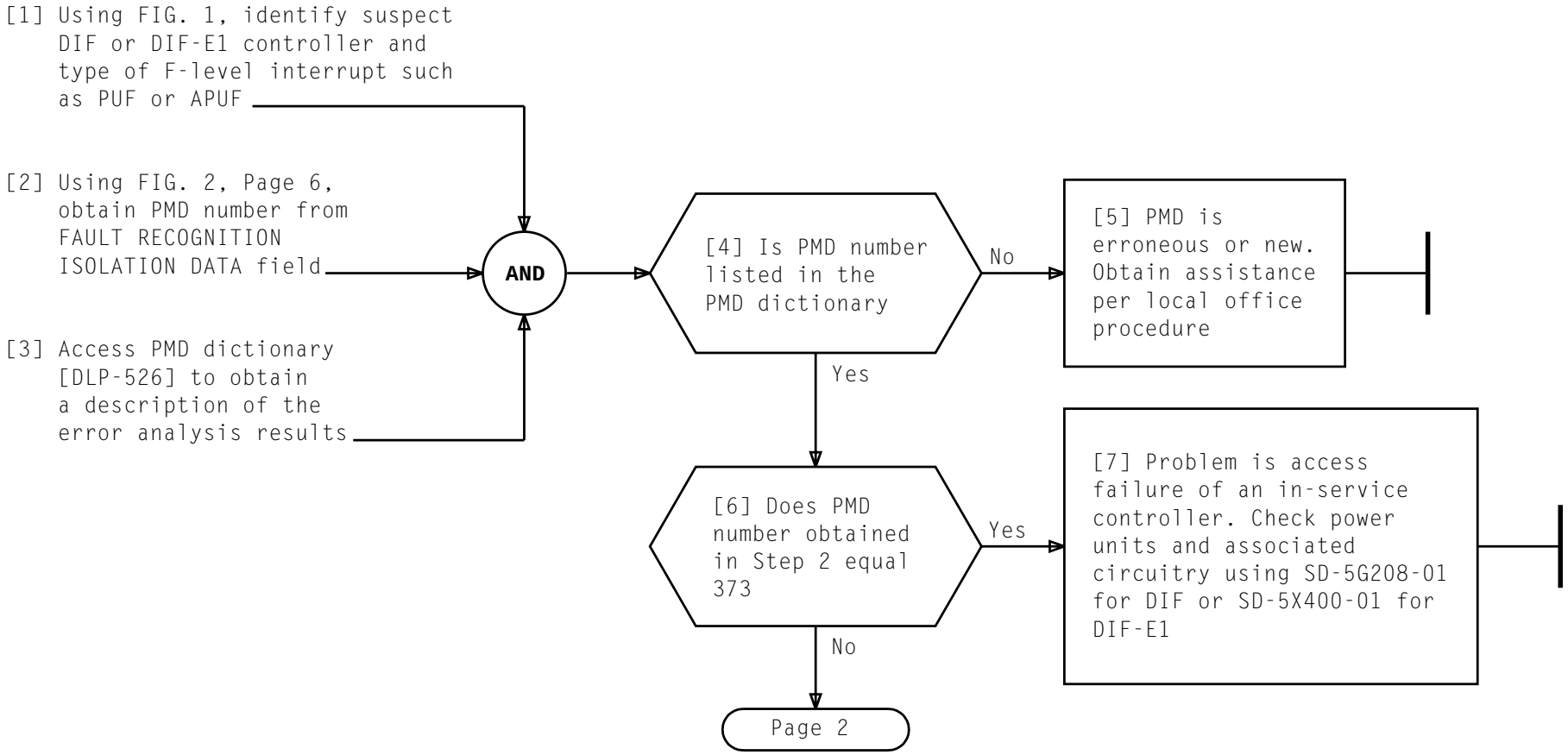
TABLE B

REGISTER	INFO. NOTE	SHEET
MADATA	331	D16
CESR1	346	D17
CESR2	347	D18
CESR3	348	
CESR4	349	

TABLE C

OPCODE	READ	WRITE
003		√
027	√	
044		√
047	√	
105		√
106		√
111		√
112	√	
114		√
117		√
120	√	
141	√	
142		√
160	√	
170	√	
171	√	
172	√	
173	√	
174		√
175		√

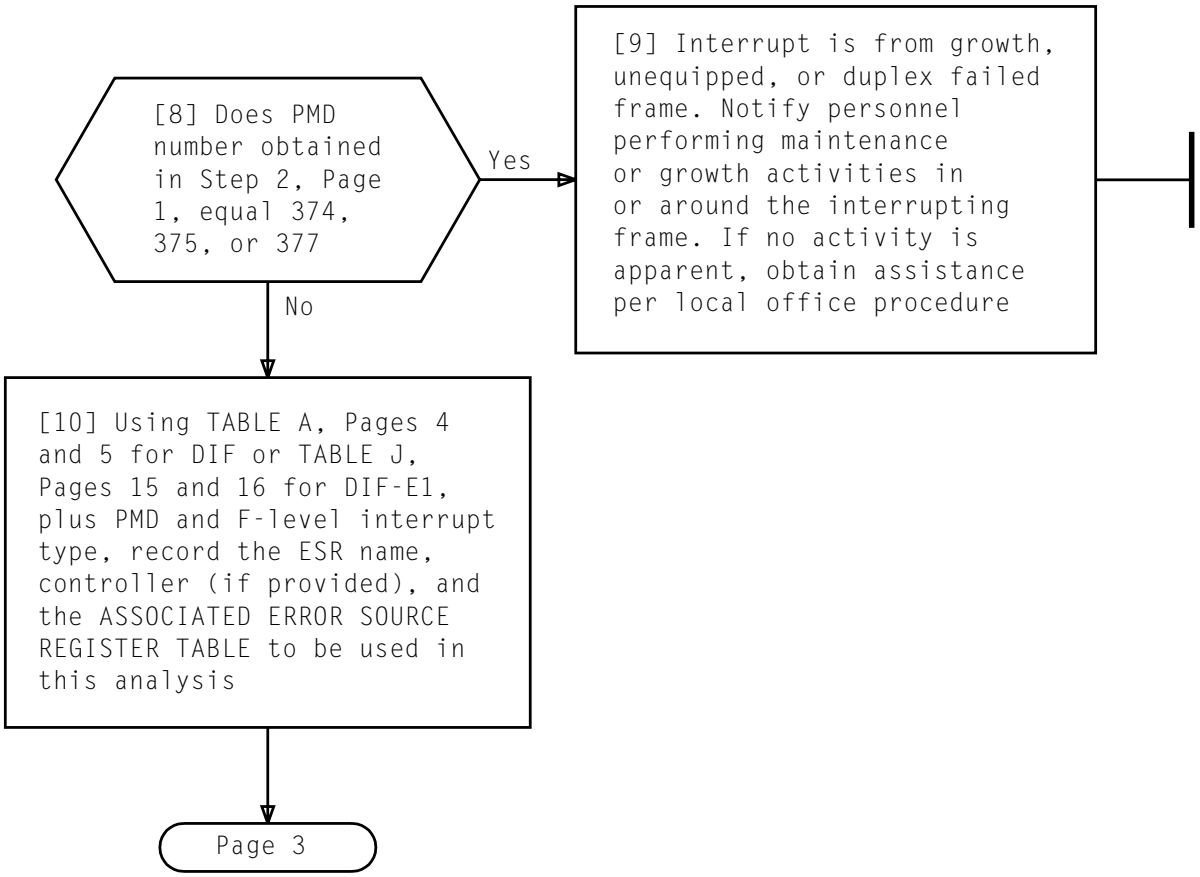
ANALYZE ESFR F LEVEL INTERRUPT



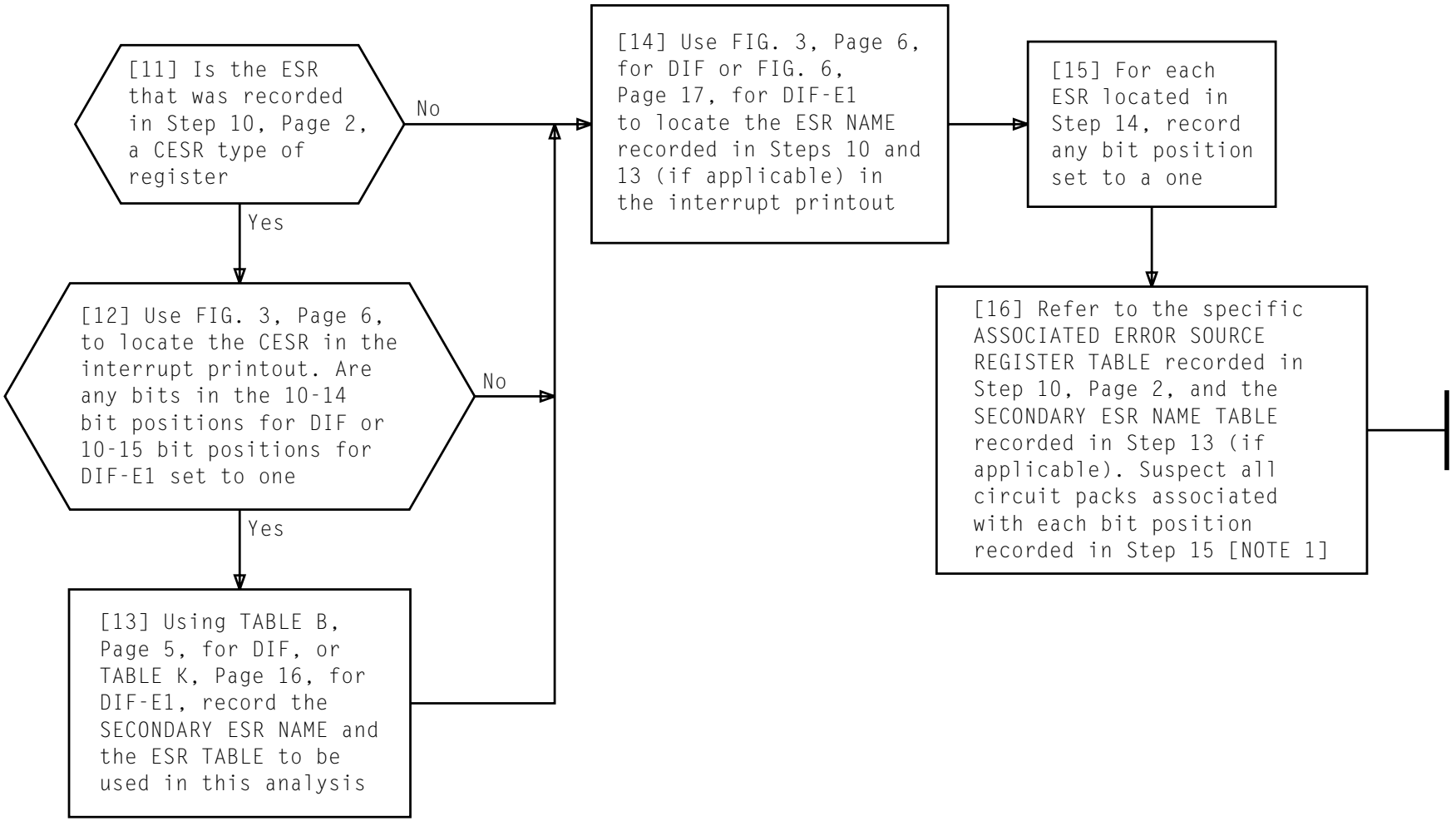

```
A 39 REPT:F-LEVEL 15004417 MFNUM=00000345 MICON=00000022 MSG STARTED
LV=0040 D0=00000000 D1=00000000 D2=00000057 D3=00000000
APUFS INTERRUPT DIF 21
DIFR RESOLVED ERROR DIF 21 CONTR 0
DIFR RECOMMENDED REMOVAL LOM DIF 21 CONTR 0
DIFR RECOMMENDED DIAGNOSTICS DIF 21 CONTR 0
FERA REQUESTED REMOVAL LOM DIF 21 CONTR 0
FERA REQUESTED DIAGNOSTICS DIF 21 CONTR 0
```

FIG. 1 — Text Header Portion of DIFR Printout

ANALYZE DIFR F-LEVEL INTERRUPT



ANALYZE DIFR F-LEVEL INTERRUPT



NOTE 1
The same CP may be contained in the CP list more than once. Duplicate entries should be ignored.

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE A DIF REFERENCE			
PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
11,12,14,15,17,21, 25,26,141,142	CLKESR (Clock error)	C, Page 7	C, Page 7
30-37,40-43,47,50, 51,117,125,150, 151,153,176	CESR for controller with bit 0 (ASWF) and/or bit 1 (AINT) set	D, Page 8	D, Page 8
154,156,160,161, 162,164,165,166	MPESRH for active controller only†	F, Page 10	F, Page 10; H*, Page 12
54,56,60,61, 62,64,65,66	MPESRH and/or MPESRF for both controllers	F, Page 10; G, Page 11	F, Page 10; G, Page 11 H*, Page 12
44,45,46,152	CESR (Mismatch error)	D, Page 8	
70,71,72,75,76,77, 100,101,102,120, 170,171,172,177	CESR		D, Page 8 H*, Page 12
73,74,121	CESR for standby controller†		D, Page 8; H*, Page 12
173,174,175	CESR for active controller		D, Page 8; H*, Page 12
103-107 110-116, 122,123,124	CESR for active controller†		D, Page 8; H*, Page 12
130, 131, 132, 1, 2, 3, 4, 5	CESR	D, Page 8	D, Page 8

* Use TABLE H to expand "E" and "P" registers for PUFS only
† Controller is active when CSTATUS bit 7 = 1 (bit 7 = 0 for standby)

TABLE B

DIF REFERENCE

CESR BIT	SECONDARY ESR NAME	ESR TABLE [NOTE]
10, 11	IBIR	E, Page 9
12	MPESRH	F, Page 10
13	SPESR	I, Page 14
14	CLKESR	C, Page 7

NOTE: Packs associated with circuitry recommended in ESR TABLE should be checked per SD-5G208-01 for other possible problems

```
A 39 REPT:F-LEVEL 01476430/1 MFNUM=0 0004303 MICON=00000020 MSG COMPL
     LV=0040 D0=00000000 D1=04000 000 D2=00000017 D3=00000000
     DATA:PERIPHERAL SYSTEM DATA
     03020102 00000000 00000001 0000000 0 00000000 00000100
     00000112 00000004 00000012 03600001 03600001 03600000
     03600000
     DATA:INTERRUPT SOURCE DATA
     00002400 14130667 03552127 00 000020 00002000
     DATA:FAULT RECOGNITION ISOLATION DATA
     00 000020 00002000 00000PMD 00000000 00000003 00000000
     DATA:ERROR ANALYSIS STRATEGY DATA
     01664210 00000001 00000001 00000001 00000001 00000000
     00000000
     04/29/79 11:38:37
     *825
```

FIG. 2 — Part of DIFR Printout

CSTATUS	HWSTATUS	MADATA	FSTATUS	DIUODO	DIUOS1
CESR	PEST	(1) MPESRH	(2) MPESRF	DIUSUMO	DIUSUM1
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH
PSVL	PSVH	(3) 0...0	(4) 0...0	(5) 0...0	TRKCNTR
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS
SPSTATR	(6) LUSPD0	(7) LUSPD1	(8) LUSPP0	(9) LUSPP1	MPBSTAT
URD1	URD2	URD3	URD4	URD5	URD6
URD7	URD8	URD9	URD10	URD11	URD12
CCPSTO	CCPST1	MPIES	MPRTIS	(10) MPMBSF	0....0
DACPSTO	DACPST1	DRFPSTO	DRFPST1	PSSSL	PSSSH
CALOW	CAHIGH	INTJ	0....0	0....0	0...0
MEMN	XLATE	FIRMVERS	5....5	5....5	5...5

CONTR 0

CSTATUS	HWSTATUS	MADATA	FSTATUS	DIUODO	DIUOS1
CESR	PEST	MPESR	MPRETE	DIUSUMO	DIUSUM1
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH
PSVL	PSVH	MAPESR	EXCESR	EXCMASK	TRKCNTR
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT
URD1	URD2	URD3	URD4	URD5	URD6
URD7	URD8	URD9	URD10	URD11	URD12
CCPSTO	CCPST1	MPIES	MPRTIS	MPMBSF	0....0
DACPSTO	DACPST1	DRFPSTO	DRFPST1	PSSSL	PSSSH
CALOW	CAHIGH	INTJ	0....0	0....0	0...0

CONTR 1

(1) MPESR-DIFE1
(2) MPRETE-DIFE1
(3) MAPESR-DIFE1
(4) EXCFESR-DIFE1
(5) EXCMASK-DIFE1
(6) MAPCNTRS-DIFE1
ESCNCNTL-DIFE1 MF/DTMF 4ST
(7) MAPREGS-DIFE1
(8) MPSTKPTR-DIFE1
(9) MPPMCNT-DIFE1
(10) EXECSMW-DIFE1

FIG. 3 — DIF CREG Layout

TABLE C
CLOCK ERROR SOURCE REGISTER (CLKESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	ERACK16O	1B/D8	CK16 energy detector for controller to unit (link A)	TM21(162-067,219) TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
1	ERAFSYO	1C/C8	Frame SYNC energy de-tector for controller to unit (link A)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
2	ERBCK16O	1B/D8	CK16 energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
3	ERBFSYO	1B/E8	Frame SYNC energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
4	ERAGGCPO	1B/D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link A)	TM22(162-103,183) TM21(162-067,219) TM24(162-085,201)
5	ERBGGCPO	1B/D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link B)	TM22(162-103,183) TM21(152-055,231) TM24(162-085,201)
6	ERGCBO	1B/C8	Controller GBC distribution ESR bit	TM22(162-103,183) TM21(152-055,231) TM24(162-085,201)
7	ERMMFO	1B/C8	Framing signal minor misframe ESR bit	TM22(162-103,183) TM24(162-085,201)
8	ERACCSYO	1C/B4	(A) clock SYNC pulse ESR bit	TM21(162-067,219) TM24(162-085,201)
9	ERBCCSYO	1C/B8	(B) clock SYNC pulse ESR bit	TM21(152-055,231) TM24(162-085,201)
10	ERLFMMO	1D/E7	Combined GGCSY and 10-msec waveform ESR bit	TM24(162-085,201)
11	XSFPCSYO	1D/E7	Super frame pattern (SFP) SYNC ESR bit	TM24(162-085,201)
12	ASAMMO	6/G7	Active standby ESR for link A	TM47(162-073,213)
13	ASBMMO	6/G7	Active standby ESR for link B	TM47(162-073,213)
14	AERSFPSO	B1D/C5	Combined super frame pattern (SFP) SYNC and waveform ESR bit for link A	TM2O(144-115,171) TM24(162-085,201)
15	BERSFPSO	1D/E7	Combined super frame pattern (SFP) SYNC and waveform ESR bit for link B	TM2O(144-115,171) TM24(162-085,201)
16	ERGCCWO	1B/E7	Controller GGC and GWC distribution ESR bit	TM22(162-103,183) TM2O(144-115,171) TM24(162-085,201)
17	ERCK6GWO	1B/F7	T1 smooth sequence signal and T1 frame SYNC signal ESR bit	TM2O(144-115,171) TM24(162-085,201)
18	ER15FSAO	18/F7	T1 clock and T1 frame SYNC ESR bit from link A	TM2O(144-115,171) TM24(162-085,201)
19	ER15FSBO	18/F7	T1 clock and T1 frame SYNC ESR bit from link B	TM2O(144-115,171) TM24(162-085,201)

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE D
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1
0	ASWFPS0	7/C5	All seems well failure	TM46(162-079,207)
1	AINTPS0	7/L5	Autonomous interrupt	TM46(162-079,207)
2	ERPUBEPY0	2A/G8	Peripheral unit bus even parity failure	TM32(170-025,261) TM46(162-079,207)
3	ERPUBOPY0	2A/G8	Peripheral unit bus odd parity failure	TM32(170-025,261) TM46(162-079,207)
4	INAPUT	8G/F9	Internal APUT	TM40(152-085,201) TM46(162-079,207)
5			APUB (not used)	TM46(162-079,207)
6			Unassigned OPCODE firmware writable	TM46(162-079,207)
7	ERPUBMOD0	2A/G8	Mode failure	TM32(170-025,261) TM46(162-079,207)
8	ERMFERM0	1B/B8	Out-of-frame	TM22(162-103,183) TM46(162-079,207)
9	ERCK160	1A/C4	Absence of Intracontroller 16.384 MHz clock alarm	TM23(162-097,195)
10	ERECSUM0	4B/G7	EXEC local ESR summary	TM56(170-085,201) TM46(162-079,207)
11	ERIBSUM0	4B/G7	Internal bus local ESR summary	TM56(170-085,201) TM46(162-079,207)
12	MMESRUM0	8F/F7	MP local ESR summary	TM41(152-091,195) TM46(162-079,207)
13	ERLUSSP0	17G/G7	SP local ESR summary	TM30(144-067,219) TM46(162-079,207)
14	ERCKSUM0	1D/B7	Summary of clock ESR alarms	TM24(162-085,201) TM46(162-079,207)
15	EXSUM3	4G/E4	Extended IBUS summary (future)	TM58(162-109,177) TM46(162-079,207)
16	T1LMM0	1D/E7	Cross-controller M/M SFP ESR alarm	TM24(162-085,201) TM46(162-079,207)
17	ERIBMM0	4B/A7	Internal bus M/M	TM56(170-085,201) TM46(162-079,207)
18	RRPYMM0	2B/E5	PUB reply register M/M	TM34(170-007,279) TM46(162-079,207)
19	PUSEQMM0	2B/E5	PUB sequencer M/M (cross-controller)	TM34(170-007,279) TM46(162-079,207)
20	BPSEQMM0	2B/D5	PUB buffer poll sequencer M/M (cross-controller)	TM34(170-007,279) TM46(162-079,207)
21			Unassigned	
22	ERLFMM0	1D/E7	Low frequency clock (10 msec) M/M (cross-controller)	TM24(162-085,201) TM46(162-079,207)
23			Unassigned	

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE E INTERNAL BUS I REGISTER (IBIR)				
BITS (0-9)				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	IBMIXAMM0	4C/H5	Internal bus return M/M (bits 0-4)	TM48(170-091,195)
1	IBMIXBMM0	4D/E3	Internal bus return M/M (bits 5-9)	TM48(170-097,189)
2	IBMIXCMM0	4D/E7	Internal bus return M/M (bits 10-4)	TM48(170-103,183)
3	IBMIXDMM0	4E/E7	Internal bus return M/M (bits 15-19)	TM48(170-109,177)
4	IBMIXEMM0	4E/E3	Internal bus return M/M (bits 20-23) and parity	TM48(170-115,171)
5	ERIBMXPY0	4A/F7	Receive IB parity error	TM55(170-079,207) TM56(170-085,201)
6	ERIBAKDES0	4A/H7	IB destination and acknowledgment	TM55(170-079,207) TM56(170-085,201)
7	ERIBSOLP0	4A/A7	IB source, destination and OP CODE loop error	TM55(170-079,207) TM56(170-085,201)
8	ERIBAKSOR0	4A/H7	Source acknowledg-ment error	TM55(170-079,207) TM56(170-085,201)
9	Unassigned			

TABLE E (Contd) INTERNAL BUS I REGISTER (IBIR)				
BITS (10-15)				
EXECUTIVE ESR				
BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
10	ERECIALU0	3D/C3	ALU mismatch	TM54(1 70-073,213) TM56(170-085,201)
11	SPORDYERR	4B/G4	PUC firmware detected error (firmware writable)	TM56(170-085,201)
12	UNMPOP	4B/G4	Unassigned MP OPCODE (firmware writable)	TM56(170-085,201)
13	MPDRDYERR	4B/G4	MP data ready error (firmware writable)	TM56(170-085,201)
14	ERECMSEQ0	3B/C3	EXEC sequencer mismatch	TM53(170-043,243) TM56(170-085,201)
15	ERECPT0	3E/D5	EXEC ROM parity error	TM61(170-055,231) TM62(170-049,237) TM56(170-085,201)
16	ERIBSUM0	4B/G7	IB ESR summary	TM56(170-085,201)
17	ERECSUM0	4B/G7	IB EXEC summary	TM56(170-085,201)
18	PEST1A	4B/F3	Pest for ESR Bits (0-15)	TM56(170-085,201)
19	ERCHK1	4B/F3	ROM check ENABLE	TM56(170-085,201)
20	RCHKST1	4B/F3	ROM check STOP	TM56(170-085,201)
Data bits 21-23 are not used at this time				

TABLE F
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRH)
FOR HARDWARE ERRORS

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	HCPYERR0	8C/D8	Hardcore parity M/M	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
1	TRAPERR0	8C/B8	CPU trap	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
2	HLDERR0	8C/D8	DMA request hardware time-out	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
3	RDPYERR0	8C/G8	External bus read parity error	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
4	PTFLERR0	8C/C8	IB reply function failure	TM42(152-103,183) TM52(152-115,171) TM41(152-091,195)
5	CCPYERR1	8F/C6	Incoming CC port parity error	TM41(152-091,195) TM52(152-115,171) TM40(152-085,201) TM42(152-103,183)
6	CNPYERR1	8F/D6	Incoming CN port parity error	TM41(152-091,195) TM52(152-115,171) TM40(152-085,201) TM42(152-103,183)
7	PSTRERR0	8E/D7	Program store parity error	TM37(152-079,207 TM64(152-067,213) TM41(152-091,195)
8	ERLUMB0	20/D8	Unit maintenance bus error	TM41(152-091,195) TM38(144-097,189) TM64(152-067,213) TM37(152-079,207)

TABLE F (Contd)
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRH)
FOR HARDWARE ERRORS

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
9	ERPST0	20/F9	Unit scanner pest error	TM38(144-097,189) TM41(152-091,195)
10			Unassigned	
11	ERUSCN10	19/F8	Unit scan error 1	TM43(144-109,177) TM64(152-067,213)
12	ERUSCN20	19/F8	Unit scan error 2	TM37(152-079,207) TM41(152-091,195)
13	PSTSERR0	8E/C7	Secondary program store parity error	TM64(152-067,213) TM37(152-079,207) TM41(152-091,195)

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE G (DIF)
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESRF)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING			SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
			VALUE OF BITS 0-7 (OCTAL)	ERROR NAME	MEANING	
0-7	ESR0-ESR7	8G/D6	0	NO ERRORS	No errors	
			1	MEMOVFL	OS8 memory overload	
			2	INVOP	Invalid MACRO OPCODE	
			3	EXECTO	EXEC MP service T/O	
			4	REPLYF	Compelled response NA	
			5	OUTPUTF	Invalid output request	TM40 (152-085, 201)
			6	SANITYTO	Sanity Time-out (T/O)	TM42 (152-103, 182)
			7	MBUFOVEL	Maintenance buffer overflow T/O	TM52 (152-115, 171)
			10	UNUSEDINT	Unassigned interrupt error	TM41 (152-091, 195)
			12	UNITF	Excessive number of units alarming	
			14	UMBF	UMB failure pattern for ESR	TM38
			15	SCANF	ESR pattern for scanner failure	TM43
			16	ICOUNTFAIL	MP ESR CODE for wrong ICOUNT	
			Undefined	OTHER	Unknown error type	

TABLE H E & P REGISTER EXPANSION*		
(E REGISTER, F-LEVEL REGISTER 24)		
E REGISTER BITS 21-17 (DECIMAL)		BITS 16-12 (DECIMAL)
VALUE	UNIT TYPE	MEMN
0	Undefined	—
1	MCC/PPI	0
2	SP/DIF	Bits 16-12
3	SCLK	0
4	TMS	Bits 11, 10
5	TSI	Bits 16-11
6	TGR	Bits 16-10
7	IOUS	Bits 16-14
8	Undefined	—
9	EST	Bits 16-12
10	Undefined	—
11	SCS	Bits 16-14
12-31	Undefined	—

* See FIG. 4, Page 13. For all PUF type F-Level interrupts from the DIF, a log should be maintained of the contents of the E, P(upper), and P(lower) registers from the interrupt printout. These registers contain the KCODE and instruction sent by the 1A Processor CC over the PU Bus. This table can then be used to break down the contents of these registers and log the results.

Obtain assistance per local office procedures if bits 21-17 of the E register indicate some other frame than the SP/DIF or if there is a repeating pattern of OPCODE and Extended OPCODE in recurring interrupts

```
      03 REPT: F-LEVEL @115540 45 MFNUM= 00004323 MICON= 00000020  MSG STARTED
         LV=0040 D0=00000000 D1=00000000 D2=00000057 D3=00000000
          APUFS INTERRUPT DIF 8
         DIFR RESOLVED ERROR DIF 8 CONTR 0
         DIFR RECOMMENDED REMOVAL LOM DIF 8 CONTR 0
         DIFR RECOMMENDED DIAGNOSTICS DIF 8 CONTR 0
         FERA REQUESTED RESTORE NO UPDATE DIF 8 CONTR 0
         DATA: F-LEVEL
         00000014 00000005 00177777 00000005 00000007 00000004
         00000002 00002000 15072574 11554045 00000040 11554044
F-LEVEL  00000004 11554046 22001511 00000023 07210003 00000005
REG 24   15075742 04000000 00002017 00400006 40100000 00000000
   └──►  02004000 00001400 00124364 00000000 00000017 00000000
         60000000 00000000 00000000 00000000 00000000 00000000
         00001511 77637777 00000007 20051375 20031175 00002374
         00002563 00010002 00000000 00000000 00000000
```

FIG. 4 – Part of F-Level Interrupt Printout

TABLE I (DIF)
SIGNAL PROCESSOR ERROR SOURCE REGISTER (SPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	LRDEYPO	17D/A9	Parity error on read of ST ROM bits 2-7	TM26(144-085,201) TM30(144-067,219) TM28(144-073,213)
1	URDPYEO	17D/B9	Parity error on read of ST ROM bits 10-15	TM26(144-085,201) TM25(144-067,219) TM28(144-073,213)
2	LARPYEO	17D/B9	ST ROM address parity error on read of bits 2-7	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)
3	URAPYEO	17D/B9	ST ROM address parity error on read of bits 8-15	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)
4	CCESPYEO		Parity error on cross-controller trunk state loopback	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)
5	TSSOPYEO	17D/G9	Parity error on trunk status store output	TM26(144-085,201) TM25(144-079,207) TM28(144-073,213)
6	LABMERRO	17F/B3	M/M on loopback of M signal blocking control-A distribution	TM31(144-049,237) TM30(144-067,219) TM28(144-073,213)
7	LBBMERRO	17F/B8	M/M on loopback of M signal blocking control-B distribution	TM31(144-049,237) TM30(144-067,219) TM28(144-073,213)
8	LAMERRO	17F/A8	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(1 44-067,219) TM27(144-055,231)
9	LBMERRO	17F/A8	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)
10	LAISERRO	17F/B3	M/M on loopback of M data-A distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)
11	LBISERRO	17F/B8	M/M on loopback of IS data-B distribution	TM31(144-049,237) TM30(144-067,219) TM27(144-055,231)
12	ESCNERRO	17E/G7	M/M at output of duplicated E scanners	TM29(144-081,195) TM30(144-067,219) TM28(144-073,213)
13	EAERRORO	17B/F9	E store/trunk status store address parity error	TM27(144-0 55,231) TM25(144-079,207) TM30(144-067,219)
14	MAERRORO	17B/F9	M store trunk status store address parity error	TM27(144-055,231) TM25(144-079,207) TM30(144-067,219)
15	SPARE00		Unused	
16	MDERRORO	17B/F9	M/M on output of duplicated M store	TM27(144-0/55,231) TM28(144-073,213) TM30(144-067,219)
17	ISERRORO	17B/F9	M/M on output of duplicated IS store	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
18	XCMDLEO	17B/G9	M/M of duplicated cross-controller loopback of M data	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
19	XCISLEO	17B/F9	M/M of duplicated cross-controller loopback of IS data	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
20	IBPYEO		Parity error on data loaded from internal bus	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
21	EDERRORO	17B/F9	M/M at output of duplicated E store	TM27(144-055,231) TM28(144-073,213) TM30(144-067,219)
22	SPARE10		Unused	
23	SPARE20		Unused	

TABLE J

DIF-E1 REFERENCE

PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
11,12,14,15,17,21, 25,26,141,142	CLKESR (Clock error)	L, Page 18	L, Page 18
30-37,40-43,47,50, 51,117,125,150, 151,153,176	CESR for controller with bit 0(ASWF) and/or bit 1(AINT) set	M, Page 19	M, Page 19
154,156,160,161, 162,164,165,166	MPESR for active controller only†	O, Page 21; P, Page 22	O, Page 21; Q, Page 23
54,56,60,61, 62,64,65,66	MPESR for both controllers	O, Page 21; P, Page 22	O, Page 21; P, Page 22 Q*, Page 23
44,45,46,152	CESR(Mismatch error)	M, Page 19	M, Page 19
70,71,72 75,76,77 100,101,102,120 170,171,172,177	CESR		M, Page 19; Q*, Page 23
73,74,121	CESR for standby controller†		M, Page 19; Q*, Page 23
173,174,175	CESR for active controller		M, Page 19; Q*, Page 23
103-107 110-116, 122,123,124	CESR for active controller†		M, Page 19; Q*, Page 23

Table J continued on next page.

TABLE J (Contd)

DIF-E1 REFERENCE

PMD	ESR NAME	ASSOCIATED ERROR SOURCE REGISTER TABLE	
		FOR APUF	FOR PUF
130, 131, 132, 1, 2, 3, 4, 5	No action required		
330, 331 340, 341	CESR	M, Page 19	M, Page 19 Q*, Page 23
350, 360	CESR (activet controller)		M, Page 19 Q*, Page 23

* Use TABLE Q to expand "E" and "P" registers for PUFS only

† Controller is active when CSTATUS bit 7 = 1 (bit 7 = 0 for standby)

TABLE K

DIF-E1 REFERENCE (NOTE)

CESR BIT	SECONDARY ESR NAME	ESR TABLE
10, 11	IBIR	N, Page 20
12	MPESR	O, Page 21
13	SPESR	R, Page 25
14	CLKESR	L, Page 18
15	MAPESR	S, Page 26

NOTE: Packs associated with circuitry recommended in ESR TABLE should be checked per SD-5X400-01 for other possible problems

```
A 39 REPT:F-LEVEL 01476430/1 MFNUM=0 0004303 MICON=00000020 MSG COMPL
     LV=0040 D0=00000000 D1=04000 000 D2=00000017 D3=00000000
     DATA:PERIPHERAL SYSTEM DATA
     03020102 00000000 00000001 0000000 0 00000000 00000100
     00000112 00000004 00000012 03600001 03600001 03600000
     03600000
     DATA:INTERRUPT SOURCE DATA
     00002400 14130667 03552127 00 000020 00002000
     DATA:FAULT RECOGNITION ISOLATION DATA
     00 000020 00002000 00000PMD 00000000 00000003 00000000
     DATA:ERROR ANALYSIS STRATEGY DATA
     01664210 00000001 00000001 00000001 00000001 00000000
     00000000
     04/29/79 11:38:37
     *825
```

FIG. 5 — Part of DIFR Printout

CSTATUS	HWSTATUS	MADATA	FSTATUS	DIUODO	DIUOS1	CONTR 0
CESR	PEST	MPESR	MPRETE	DIUSUMO	DIUSUM1	
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH	
PSVL	PSVH	MAPESR	EXCFESR	EXCMASK	TRKCNTR	
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS	
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT	
URD1	URD2	URD3	URD4	URD5	URD6	
URD7	URD8	URD9	URD10	URD11	URD12	
CCPSTO	CCPST1	MPIES	MPRTIS	EXECSMW	0....0	
DACPSTO	DACPST1	DRFPSTO	DRFPST1	PSSSL	PSSSH	
CALOW	CAHIGH	INTJ	0....0	0....0	0...0	
MEMN	XLATE	FIRMVERS	5....5	5....5	5...5	
CSTATUS	HWSTATUS	MADATA	FSTATUS	DIUODO	DIUOS1	CONTR 1
CESR	PEST	MPESR	MPRETE	DIUSUMO	DIUSUM1	
CLKESR	SPESR	IBIR	EXR	PSRL	PSRH	
PSVL	PSVH	MAPESR	EXCFESR	EXCMASK	TRKCNTR	
BSTATR	HPPTRS	LPPTRS	DBPTRS	SZPTRS	MBPTRS	
SPSTATR	MAPCNTRS	MAPREGS	MPSTKPTR	MPPMCNT	MPBSTAT	
URD1	URD2	URD3	URD4	URD5	URD6	
URD7	URD8	URD9	URD10	URD11	URD12	
CCPSTO	CCPST1	MPIES	MPRTIS	EXECSMW	0....0	
DACPSTO	DACPST1	DRFPSTO	DRFPST1	PSSSL	PSSSH	
CALOW	CAHIGH	INTJ	0....0	0....0	0...0	

FIG. 6 — DIF-E1 CREG Layout

TABLE L
CLOCK ERROR SOURCE REGISTER (CLKESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	ERACK160	7B23 / D8	CK16 energy detector for controller to unit (link A)	TM1(162-067,219) TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
1	ERAFSY0	7B23 / D8	Frame SYNC energy de-tector for controller to unit (link A)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
2	ERBCK160	7B23 / E8	CK16 energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
3	ERBFSY0	7B23 / E8	Frame SYNC energy detector for controller to unit (link B)	TM22(162-103,183) TM23(162-097,195) TM24(162-085,201)
4	ERAGGCP0	7B23 / D8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link A)	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)
5	ERBGGCP0	7B23 / E8	Combined GGC 32PY and 32SY ESR bit for controller to unit (link B)	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)
6	ERGCB0	7B23 / B8	GBC Parity error	TM22(162-103,183) TM1(162-067,219) TM24(162-085,201)
7	ERMMF0	7B23 / C9	Minor framing error	TM22(162-103,183) TM24(162-085,201)
8	ERACCSY0	7B25 / G0	Clock chain link A Sync pulse error	TM1(162-067,219) TM24(162-085,201)
9	ERBCCSY0	7B25 / G0	Clock chain link B Sync pulse error	TM1(162-067,219) TM24(162-085,201)
10	ERLFMM0	7B25 / E7	GGCSY and 10 MSEC clock error	TM24(162-085,201)
11	XSFPCSY0	7B25 / E8	Super frame Sync error	TM24(162-085,201)
12	ASAMM0	9B27 / G7	Active/standby link A error	TM364(162-073,213)
13	ASBMM0	9B27 / G7	Active/standby link B error	TM364(162-073,213)
14	AERSFPS0	7B25 / C5	Super frame pattern and SFSY link A error	TM20(144-115,171) TM24(162-085,201)
15	BERSFPS0	7B25 / C5	Super frame pattern and SFSY link B error	TM20(144-115,171) TM24(162-085,201)
16	ERGCCW0	7B25 / D5	Clock chain A GGCPY and GWCPY error	TM22(162-103,183) TM20(144-115,171) TM24(162-085,201)
17	ERCK6GW0	18B58 / D7	Clock chain and SFSY ESR	TM20(144-115,171) TM24(162-085,201)
18	ER15FSA0	18B58 / F7	1.5 MHZ and T1FSY link A error	TM20(144-115,171) TM24(162-085,201)
19	ER15FSB0	18B58 / F7	1.5 MHZ and T1FSY link B error	TM20(144-115,171) TM24(162-085,201)
20-23	UNASSIGNED			

TABLE M
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT PACK - CONTR 0, CONTR 1
0	ASWFPS0	8B26 / B5	All seems well failure — F LEVEL	TM363(162-079,207)
1	AINTPS0	8B26 / C5	Autonomous interrupt — F LEVEL	TM363(162-079,207)
2	ERPUBEPY0	3B7 / G8	Peripheral unit bus even parity failure	TM6(170-115,171) TM363(162-079,207)
3	ERPUBOPY0	3B7 / G8	Peripheral unit bus odd parity failure	TM6(170-115,171) TM363(162-079,207)
4	INAPUT	12B37 / F9	Internal APUT INTERJECT	TM40(152-85,201) TM363(162-079,207)
5		8B26	APUB	TM363(162-079,207)
6		8B26	Unassigned OPCODE received	TM363(162-079,207)
7	ERPUBMOD0	3B7 / G8	Mode failure	TM6(170-115,171) TM363(162-079,207)
8	ERMFERM0	7B23 / C8	Out-of-frame error	TM22(162-103,183) TM363(162-079,207)
9	ERCK160	7B24 / C4	16 MBIT clock error	TM23(162-097,195)
10	ERECSUM0	4B15 / G6	EXEC ESR summary	TM11(170-043,243) TM363(162-079,207)
11	ERIBSUM0	4B15 / G6	Internal bus ESR summary	TM11(170-043,243) TM363(162-079,207)
12	MMESRSUM0	12B36 / F8	MP ESR summary	TM68(152-091,195) TM363(162-079,207)
13	ERLUSP0	15B49 / B8	SP ESR summary	TM18(144-055,231) TM363(162-079,207)
14	ERCKSUM0	7B25 / B7	Clock ESR Summary	TM24(162-085,201) TM363(162-079,207)
15	EXSUM3	8B26	MAP ESR Summary or Frogger error (MF only)	TM363(162-079,207)
16	T1LMM0	7B25 / E7	T1 line mismatch	TM24(162-085-201) TM363(162-079,207)
17	ERIBMM0	4B15 / B6	Internal bus mismatch	TM363(162-079,207)
18	RRPYMM0	3B9 / E5	PUB reply register mismatch	TM7*(170-097,189) TM363(162-079,207)
19	PUSEQMM0	3B9 / E5	PUB sequencer mismatch	TM7*(170-097,189) TM363(162-079,207)
20	SEQMM0	3B9 / D4	SP M-Bit mismatch	TM7*(170-097,189) TM363(162-079,207)
21			Unassigned	
22	ERLFMM0	7B25 / E8	Low frequency clock mismatch	TM24(162-085,201) TM363(162-079,207)
23			Unassigned	

* May be TM371

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE N
INTERNAL BUS I REGISTER (IBIR)

BITS (0-9)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	IBMXAMM0	4B10/H5	IB Multiplexer A — Return mismatch	TM365(170-091,195)
1	IBMXBMM0	4B11/E3	IB Multiplexer B — Return mismatch	TM365(170-085,201)
2	IBMXCMM0	4B11/E7	IB Multiplexer C — Return mismatch	TM365(170-079,207)
3	IBMXDMM0	4B12/F3	IB Multiplexer D — Return mismatch	TM365(170-073,213)
4	IBMXEMM0	4B12/C7	IB Multiplexer E — Return mismatch	TM365(170-067,219)
5	ERIBMXPY0	4B13/F7	Receive IB parity error	TM10*(170-055,231) TM11(170-043,243)
6	ERIBAKDES0	4B13/H7	Destination Ack error	TM10*(170-055,231) TM11(170-043,243)
7	ERIBSDLP0	4B13/A7	Source/Dest/ opcode loop mismatch	TM10*(170-055,231) TM11(170-043,243)
8	ERIBAKSOR0	4B15/G0	Source Ack error	TM10*(170-055,231) TM11(170-043,243)
9	N.A	4B15	Firmware error maintenance buffer	TM11(170-043,243)
10	ERECALU0	5B17/C3	ALU mismatch	TM9(1 70-031,255) TM11(170-043,243)

* May be TM10B

TABLE N (Contd)
INTERNAL BUS I REGISTER (IBIR)

BITS (10-15)

EXECUTIVE ESR

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
11	N. A.	4B15	Firmware error — SP	TM11(170-043,243) TM17(144-067,219)
12	N. A.	4B15	Firmware error — Exec	TM11(170-043,243) TM8(170-019, 267) TM6(170-115, 171)
13	N. A.	4B15	Firmware error — MP	TM11(170-043,243) TM368(152-097,189)
14	ERECMSEQ0	4B15/H0	Exec Sequencer Mismatch	TM8(170-019,267) TM11(170-043,243)
15	ERECPY0	5B18	Exec PROM parity error	TM370(170-025,261) TM11(170-043,243)
16	ERIBSUM0	4B15/G5	IB ESR Summary	TM11(170-043,243)
17	ERECSUM0	4B15/G5	Exec ESR Summary	TM11(170-043,243)
18	PEST1A	4B15/F3	Pest for ESR Bits (0-17, 22)	TM11(170-043,243)
19	ERCHK1	4B15/F3	ROM check enable	TM11(170-043,243)
20	RCHKST1	4B15/F3	ROM check stop	TM11(170-043,243)
21	UNASSIGNED			
22	ECERZZ0	4B15/H0	Buffer RAM address parity check error	TM11(170-043,243)
23	UNASSIGNED			

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE O
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0-7	ESR0-ESR7	12B37 / D5	Firmware writable [TABLE P, Page 22]	TM40(152-085,201) TM366*(152-103,183)
8	HCPYERR0	12B34 / D8	Hardcore parity M/M	TM366*(152-103,183) TM68(152-091,195)
9	TRAPERR0	12B34 / B8	CPU trap error	TM366*(152-103,183) TM68(152-091,195) TM368(152-097,189) TM368(152-109,177) TM366*(152-115,171)
10	HLDERR0	12B34 / D8	DMA request hardware time-out	TM366*(152-103,183) TM68(152-091,195)
11	RDPYERR0	12B34 / G8	External bus read parity error	TM366*(152-103,183) TM68(152-091,195)
12	PTFLERR0	12B34 / C3	Firmware ESR Bit failure	TM366*(152-103,183) TM68(152-091,195)
13	CCPYERR1	12B36 / C6	Incoming CC port parity error	TM68(152-091,195) TM40(152-085,201) TM366*(152-103,183)
14	CNPYERR1	12B36 / D6	Incoming CN port parity error	TM68(152-091,195) TM40(152-085,201) TM366*(152-103,183)
15	PSTRERR0	12B38 / D8	Main program store parity error	TM366*(152-103,183) TM67(152-067,219) TM67(152-073,213) TM57(152-079,207) TM37

* May be TM375

TABLE O (Contd)
MAINTENANCE PROCESSOR ERROR SOURCE REGISTER (MPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
16	ERLUMB0	16B56 / E8	Unit maintenance bus error	TM38(144-103,183) TM68(152-091,195)
17	ERPST0	16B56 / F8	Unit scanner pest error	TM38(144-103,183) TM68(152-091,195)
18			Unit maintenance bus shift register alarm	
19	ERUSCN10	17B57 / F8	Unit Scan error 1	TM19(144-109,177) TM67(152-067,219) (152-073,213 079,207) TM68(152-091,195)
20	ERUSCN20	17B57 / F8	Unit Scan error 2	
21			Unassigned	
22	HALTER0	12B36 / F5	MP halt error	TM68(152-091,195) TM366*(152-103,183)
23	HLTPST1	12B36 / F4	Pest bit for MP halt error	TM68(152-091,195)

* May be TM375

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE P
FIRMWARE ERROR SOURCE REGISTER

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING			SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
			VALUE OF BITS 0-7 (OCTAL)	ERROR NAME	BIT MEANING	
0-7	ESR0-ESR7	12B37 / D5	0	NOERRORS	No errors	
			1	MEMOVFL	OS8 memory overload	
			2	INVOP	Invalid MACRO OPCODE	
			3	EXECTO	EXEC MP service T/O	
			4	REPLYF	Compelled response NA	
			5	OUTPUTF	Invalid output request	TM40(152-085,201)
			6	SANITYTO	Sanity time-out (T/O)	TM366*(152-103,183)
			7	MBUFOVEL	Maintenance buffer overflow T/O	TM365(170-067,219)
			10		Unassigned (interrupt error)	
			11		Unassigned	
			12	UNITF	Unit failure code ESR	
			13	DGF	DG failure code ESR	
			14	UMBF	UMB failure pattern for ESR	
			15	SCANF	ESR pattern for scanner failure	
			16	ICOUNTFAIL	MP ESR CODE for wrong ICOUNT	
			17	FIRMF	Micro DCON Firmware Failure	
			20	MPAUDITERROR	MP PROG. Store Audit Failure	
			21	SPAUDITERROR	SP PROG. Store Audit Failure	

* May be TM375

TABLE Q
E & P REGISTER EXPANSION*

(E REGISTER, F-LEVEL REGISTER 24)		
E REGISTER BITS 21-17 (DECIMAL)		BITS 16-12 (DECIMAL)
VALUE	UNIT TYPE	MEMN
0	Undefined	—
1	MCC/PPI	0
2	SP/DIF	Bits 16-12
3	SCLK	0
4	TMS	Bits 11, 10
5	TSI	Bits 16-11
6	TGR	Bits 16-10
7	IOUS	Bits 16-14
8	Undefined	—
9	EST	Bits 16-12
10	Undefined	—
11-31	Undefined	—

* See FIG. 7, Page 24. For all PUF type F-Level interrupts from the DIF-E1, a log should be maintained of the contents of the E, P(upper), and P(lower) registers from the interrupt printout. These registers contain the KCODE and instruction sent by the 1A Processor CC over the PU Bus. This table can then be used to break down the contents of these registers and log the results.

Obtain assistance per local office procedures if bits 21-17 of the E register indicate some other frame than the SP/DIF-E1 or if there is a repeating pattern of OPCODE and Extended OPCODE in recurring interrupts

```
      03 REPT: F-LEVEL @115540 45 MFNUM= 00004323 MICON= 00000020  MSG STARTED
         LV=0040 D0=00000000 D1=00000000 D2=00000057 D3=00000000
          APUFS INTERRUPT DIF 8
         DIFR RESOLVED ERROR DIF 8 CONTR 0
         DIFR RECOMMENDED REMOVAL LOM DIF 8 CONTR 0
         DIFR RECOMMENDED DIAGNOSTICS DIF 8 CONTR 0
         FERA REQUESTED RESTORE NO UPDATE DIF 8 CONTR 0
         DATA: F-LEVEL
         00000014 00000005 00177777 00000005 00000007 00000004
         00000002 00002000 15072574 11554045 00000040 11554044
F-LEVEL  00000004 11554046 22001511 00000023 07210003 00000005
REG 24   15075742 04000000 00002017 00400006 40100000 00000000
         02004000 00001400 00124364 00000000 00000017 00000000
         60000000 00000000 00000000 00000000 00000000 00000000
         00001511 77637777 00000007 20051375 20031175 00002374
         00002563 00010002 00000000 00000000 00000000
```

FIG. 7 – Part of F-Level Interrupt Printout

TABLE R
SIGNAL PROCESSOR ERROR SOURCE REGISTER (SPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
0	NTSPYERO	15B53 / B9	State translator parity error	TM682(144-085,201) TM17(144-067,219)
1	CTSPYERO	15B53 / F8	Current trunk state parity error	TM682(144-085,201) TM4(144-079,207)
2	LTJMPMMO	15B53 / E8	Looped jump control mismatch	TM682(144-085,201) TM17(144-067,219)
3	LRFMMO	15B53 / E8	Looped RPTFLG control mismatch	TM682(144-085,201) TM17(144-067,219)
4	LAESERO	15B47 / B8	Block of M Bit distribution update mismatch (0-15, 32)	TM5(144-043,243)
5	LBESERO	15B47 / B8	Block of M Bit distribution update mismatch (16-31, 33)	TM5(144-043,243)
6	LAMERO	15B47 / A8	M BIT distribution loop mismatch (0-15, 32)	TM5(144-043,243) TM16*(144-049,237)
7	LBMERO	15B47 / A8	M BIT distribution loop mismatch (16-31, 33)	TM5(144-043,243) TM16*(144-049,237)
8	LAISERO	15B47 / B8	Loop PCIS distribution mismatch (0-15, 32)	TM5(144-043,243) TM16*(144-049,237)
9	LBISERO	15B47 / B8	Loop PCIS distribution mismatch (16-31, 33)	TM5(144-043,243) TM16*(144-049,237)
10	CCTSPYEO	15B52 / C9	Cross controller trunk state mismatch	TM4(144-079,207)
* May be TM372 or TM684				

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	SUSPECT CIRCUIT PACKS CONTR 0, CONTR 1
11			Unassigned	
12	ESCNERRO	15B55 / G7	E Bit Scanner mismatch	TM362 (144-097,189) TM5 (144-043,243) TM17 (144-067,219)
13	EADERO	15B48 / F9	E Bit store — address error	TM16* (144-049,237) TM17 (144-067,219)
14	MADERO	15B48 / F9	M Bit store — address parity error	TM16* (144-049,237) TM17 (144-067,219)
15	EDERO	15B48 / F9	Duplicated E Bit store mismatch	TM16* (144-049,237) TM17 (144-067,219)
16	MDERO	15B48 / F9	Duplicated M Bit store mismatch	TM16* (144-049,237) TM17 (144-067,219)
17	ISERO	15B48 / G9	Duplicated PCIS store mismatch	TM16* (144-049,237) TM17 (144-067,219)
18	XCMDLEO	15B48 / F9	Looped cross controller M Bit data mismatch	TM16* (144-049,237) TM17 (144-067,219)
19	XCISLEO	15B48 / G9	Looped cross controller PCIS data mismatch	TM16* (144-049,237) TM17 (144-067,219)
20	IBPYERO	15B48 / A9	Internal bus data error	TM16* (144-049,237) TM17 (144-067,219)
21	TSSADPYE1	15B51 / E8	TSS address parity error	TM15 (144-073,213) TM365 (170-091,195)
22	CTSEBERO	15B53 / E9	Current trunk state E bit mismatch	TM682 (144-085,201) TM16* (144-049,237)
23			Unassigned	

ANALYZE DIFR F-LEVEL INTERRUPT

TABLE S
MESSAGE ACCOUNTING PROCESSOR ESR BITS 0-9 AND STATUS REGISTER BITS 21-23 (MAPESR)

BIT NUMBER	LEAD DESIGNATION	FS	BIT MEANING	EXR BITS	SUSPECT CIRCUIT PACKS CONT 0, CONTR 1
0	EIBDO	14B41/FO	Parity error over Rcvd IB Data	1,2	TM303* (152-037,249) TM302† (152-043,243)
1	EPTSSO	14B41/FO	Parity error when PTSS is read	1,2	TM303* (152-037,249) TM304 (152-031,255)
2	EPTSRPSO	14B41/FO	Parity error when PTSRPS is read	1,2	TM303* (152-037,249) TM305 (152-019,267)
3	ETRKCTRO	14B41/FO	Read and write trunk counters are out of step	1,2	TM303* (152-037,249) TM304 (152-031,255)
4	EXCLO	14B41/FO	X-CONT UPDATE data link faulty	1,2	TM303* (152-037,249) TM307 (152-025,261)
5	EPPMO	14B41/FO	P-bit link to SP faulty	1,2	TM303* (152-037,249) TM304 (152-031,255)
6	EMUXO	14B41/FO	PTSS Multiplex data fails parity	1,2	TM303* (152-037,249) TM305 (152-019,267)
7	EBPIO	14B41/FO	Data link between PROC and PTSS fails parity	1,2	TM303* (152-037,249) TM307 (152-025,261)
8	EPSADO	14B41/FO	Parity error over P store address	1,2	TM303* (152-037,249) TM304 (152-031,255)
9	EGB3CLKO	14B41/FO	Pipeline CLK to PROC and PTSS memory pack failed loop check	1,2,3	TM303* (152-037,249) TM304 (152-031,255)
21	STOP1A	14B41/AO	Reclocked STOP status bit	—	TM303* (152-037,249) TM1 (152-067,219)
22	UPDAT1	14B41/AO	Reclocked UPDATE status bit	—	TM303* (152-037,249) TM1 (152-067,219)
23	WPESTO	14B41/E1	Pest for all ESR bits (0-9)	—	TM303* (152-037,249) TM304 (152-031,255)

* May be TM374
† May be TM373

Using NCLK F-level printout:

1. See FIG. 1. Identify PMD number in rightmost two octal digits of PU4FRPMD word

2. Note what NCFR found using PMD number and TABLE A

3. See FIG. 1. Convert octal network clock READ 1 and READ 0 data words into binary

4. Check all READ 1 and 0 words at time of interrupt for set bits in order of priority [as listed in TABLE B, Page 2] and follow reference provided; for example, all READ 1 words bit 4, then all READ 1 words bit 6, and others.

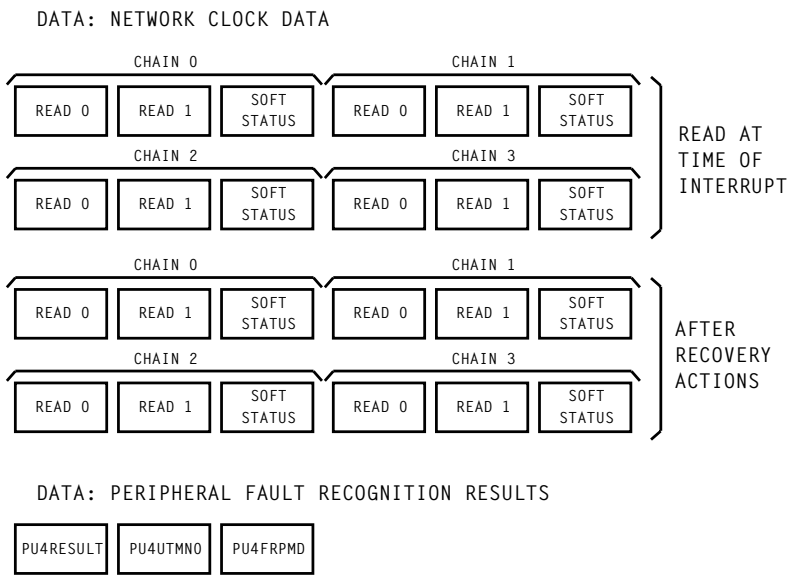


FIG. 1 – Check Register Layout

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE A
PMD DESCRIPTION

PMD*	NCFR FOUND	PMD*	NCFR FOUND	PMD*	NCFR FOUND
1	Fanout level detector	12	No errors found	26	Chain 10 counter failed
2	Master oscillator level detector	13	Phase lock oven control is out of range	27	Chain 11 counter failed
3	Oscillator level detector fault	14	Error summary circuits failed	30	Chain 00 matcher failed
4	Chain is being removed at random because two matchers were indicated, which is invalid combination except for double faults	15	Phase Fault-transient	31	Chain 01 matcher failed
		16	Unassigned	32	Chain 10 matcher failed
		17	Output disconnect fault	33	Chain 11 matcher failed
5	Matcher 00	20	Single MSL (Master Select Level) error	34	Chain failed access test
6	Matcher 01	21	Master oscillator fault	35	Master select failure
7	Matcher 10	22	Phase fault — hard	36	Frame pulse detector
10	Matcher 11	23	Fanout level detector	37	Output Disconnect fault
11	Two chains OOS and matchers up	24	Chain 00 counter failed		
		25	Chain 01 counter failed		

* PMDs 1-17 are transient errors; PMDs 20-37 are hard faults

TABLE B
READ 0 AND 1 WORDS — BIT PRIORITIES* AND RELATED FAULT CONDITIONS

WORD*	BITS*	BIT DESCRIPTION	CONDITIONS	REFERENCE
1	4	Oscillator level detector	Suspect packs and leads in chain with bit 4 set	TABLE C — Page 5
1	6	Master select level detector	Suspect packs and leads in chain with bit 6 set	TABLE D — Page 5
1	12	Phase lock oven monitor	Suspect packs and leads in chain with bit 12 set	TABLE E — Page 6
1	5	Oscillator phase detector	A. Bit 5 set in more than one chain; clear phase error	234-151-013
			B. Bit 5 set in one chain; check phase meter in chain with bit 5 set a. If **PHASE** meter reads greater than plus or minus 3 degrees from zero, clear phase error	234-151-013
			b. If **PHASE** meter reads plus or minus 3 degrees or less from zero, suspect packs and leads in this chain	TABLE F — Page 6
1	7	Phase unlock detector	A. Bit 7 set in one chain; suspect packs and leads in that chain	TABLE G — Page 6
			B. Bit 7 set in more than one chain; clear phase error	234-151-013
0	2 thru 11	Fanout level detector — BRANCH A through Fanout level detector — BRANCH J	A. More than one bit (2-11) set; suspect packs and leads for chain with bit set	TABLE H — Page 7
			B. Single bit (2-11) set; suspect packs and leads for chain with bit set	TABLE I — Page 8
1	10	Error summary	A. Bit 10 set in one chain; bit 0 set in all four chains; no Read 0 bits set; and no other Read 1 bits set; suspect packs and leads in chain with bit 10 set	TABLE J — Page 9
			B. Bit 10 set in one chain and bit 1, 2, or 3 set in same chain; suspect packs and leads in this chain	TABLE K — Page 9

* Words and bits are listed in order of priority

TABLE B (Contd)
READ 0 AND 1 WORDS — BIT PRIORITIES* AND RELATED FAULT CONDITIONS

WORD*	BITS*	BIT DESCRIPTION	CONDITIONS	REFERENCE
0	0	Frame matcher	A. Bit 0 set in one chain and bit 1 not set in any chain, suspect packs and leads in chain having bit 0 set	TABLE L — Page 9
			B. Bit 0 set in three chains and bit 1 not set in any chain, determine common chain [TABLE M] and suspect packs and leads in common chain [TABLE N]	TABLE M — Page 10 TABLE N — Page 10
			C. Bit 0 and bit 1 set in same chain, suspect pack in that chain	TABLE O — Page 10
			D. Bit 0 and bit 1 set in three chains, determine common chain [TABLE M] and suspect packs and leads in common chain (TABLE P)	TABLE M — Page 10 TABLE P — Page 10
			E. Bit 0 set in two chains and bit 1 set in three chains, determine common chain [TABLE M] and suspect packs and leads in common chain [TABLE Q]	TABLE M — Page 10 TABLE Q — Page 11
0	1	Counter matcher	Bit 1 set in one chain, suspect packs and leads for that chain	TABLE R — Page 11
All other READ 0 and 1 word bits are DON'T CARE				
* Words and bits are listed in order of priority				

TABLE C
OSCILLATOR/MASTER SELECT LEVEL ERROR

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-34	0OSCA	1	24
	070-31	0OSCLE1	1	5
	070-29	0OSCLEPO	1	1
	070-23	0SOSCLEO	12	4
		0SOSCLDO		
	044-35	*OSCILLATOR		
1	070-37	1OSCA	2	24
	070-40	1OSCLE1	2	5
	070-42	1OSCLEPO	2	1
	070-48	1SOSCLEO	13	4
		1SOSCLDO		
	033-35	*OSCILLATOR		
2	170-34	0OSCA	1	24
	170-31	0OSCLE1	1	5
	170-29	0OSCLEPO	1	1
	170-23	0SOSCLEO	12	4
		0SOSCLDO		
	144-35	*OSCILLATOR		
3	170-37	1OSCA	2	24
	170-40	1OSCLE1	2	5
	170-42	1OSCLEPO	2	1
	170-48	1SOSCLEO	13	4
		1SOSCLDO		
	133-35	*OSCILLATOR		

*If pack replacement does not clear trouble, check oscillator (level) before replacing oscillator

TABLE D
MASTER SELECT LEVEL ERROR WITH OR WITHOUT PHASE ERROR

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM			LEAD	FS	SYM
0	070-32	0MOSCS	1	2	2	170-32	0MOSCS	1	2
	070-31	0MSLE1	1	4		170-31	0MSLE1	1	4
	070-29	0MSLEPO	1	1		170-29	0MSLEPO	1	1
	070-23	0SMSLDO	12	4		170-23	0SMSLDO	12	4
	070-34	OUTPUT*	1	24		070-34	OUTPUT*	1	24
1	070-39	1MOSCS	2	2	3	170-39	1MOSCS	2	2
	070-40	1MSLE1	2	4		170-40	1MSLE1	2	4
	070-42	1MSLEPO	2	1		170-42	1MSLEPO	2	1
	070-48	1SMSLDO	13	4		170-48	1SMSLDO	13	4
	070-34	OUTPUT*	1	24		070-34	OUTPUT*	1	24

*Clock distribution driver output leads to master oscillator selector

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE E
PHASE LOCK OVEN ERROR

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	078-20	0PLOMPO	1	11
	070-23	0SPLOM1	12	4
	066-33	0TCBCTL	1	9
	066-31	0TEMCTLP	1	12
	066-34	0TEMCTLP	1	13
	Check **PHASE LOCK OVEN TEMP meter [DLP-529]**			
1	078-52	1PLOMPO	2	11
	170-48	1SPLOM1	13	4
	066-39	1TCBCTL	2	9
	066-40	1TEMCTLP	2	12
	066-37	1TEMCTLP	2	13
	Check **PHASE LOCK OVEN TEMP meter [DLP-529]**			
2	178-20	0PLOMPO	1	11
	070-23	0SPLOM1	12	4
	166-33	0TCBCTL	1	9
	166-31	0TEMCTLP	1	12
	166-34	0TEMCTLP	1	13
	Check **PHASE LOCK OVEN TEMP meter [DLP-529]**			
3	178-52	1PLOMPO	2	11
	170-48	1SPLOM1	13	4
	166-39	1TCBCTL	2	9
	166-40	1TEMCTLP	2	12
	166-37	1TEMCTLP	2	13
	Check **PHASE LOCK OVEN TEMP meter [DLP-529]**			

TABLE F
PHASE LOCK ERROR AND PHASE METER EQUAL TO OR LESS THAN 3 DEGREES

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-29	0PLEPO	1	1
	070-23	0SPLLEO	12	4
1	070-42	1PLEPO	2	1
	070-48	1SPLLEO	13	4
2	170-29	0PLEPO	1	1
	170-23	0SPLLEO	12	4
3	170-42	1PLEPO	2	1
	170-48	1SPLLEO	13	4

TABLE G
PHASE UNLOCK ERROR IN ONE CHAIN

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-29	0PULEPO	1	1
	070-23	0SPUEDLO 0SPUEDMO	12	4
	Clear phase error [234-151-013]			
1	070-42	1PULEPO	2	1
	070-48	1SPUEDLO 1SPUEDMO	13	4
	Clear phase error [234-151-013]			
2	170-29	0PULEPO	1	1
	170-23	0SPUEDLO 0SPUEDMO	12	4
	Clear phase error [234-151-013]			
3	170-42	1PULEPO	2	1
	170-48	1SPUEDLO 1SPUEDMO	13	4
	Clear phase error [234-151-013]			

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE H
MULTIPLE FANOUT LEVEL ERRORS

READ 0 BITS 2 THRU 11 SET					READ 0 BITS 2 THRU 6 SET				READ 0 BITS 7 THRU 11 SET			
CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM		LEAD	FS	SYM		LEAD	FS	SYM
0	070-26	0CLFODR	5	1	074-27	0CLFODR	5	2	074-26	0CLFODR	5	3
1	070-45	1CLFODR	6	1	074-44	1CLFODR	6	2	074-45	1CLFODR	6	3
2	170-26	0CLFODR	5	1	174-27	0CLODR	5	2	174-26	0CLFODR	5	3
3	170-45	1CLFODR	6	1	174-44	1CLFODR	6	2	174-45	1CLFODR	6	3

TABLE I
SINGLE FANOUT LEVEL ERROR

BIT	CHAIN 0				CHAIN 1				CHAIN 2				CHAIN 3			
	SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01			SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM		LEAD	FS	SYM		LEAD	FS	SYM		LEAD	FS	SYM
2	070-25	0FOMPOA	10	1	070-46	1FOMPOA	11	1	170-25	0FOMPOA	10	1	170-46	1FOMPOA	11	1
	074-27	0CLFOD1A	5	2	074-44	1CLFOD1A	6	2	174-27	0CLFOD1A	5	2	174-44	1CLFOD1A	6	2
3	070-25	0FOMPOB	10	1	070-46	1FOMPOB	11	1	170-25	0FOMPOB	10	1	170-46	1FOMPOB	11	1
	074-27	0CLFOD1B	5	2	074-44	1CLFOD1B	6	2	174-27	0CLFOD1B	5	2	174-44	1CLFOD1B	6	2
4	070-25	0FOMPOC	10	1	070-46	1FOMPOC	11	1	170-25	0FOMPOC	10	1	170-46	1FOMPOC	11	1
	074-27	0CLFOD1C	5	2	074-44	1CLFOD1C	6	2	174-27	0CLFOD1C	5	2	174-44	1CLFOD1C	6	2
5	070-25	0FOMPOD	10	1	070-46	1FOMPOD	11	1	170-25	0FOMPOD	10	1	170-46	1FOMPOD	11	1
	074-27	0CLFOD1D	5	2	074-44	1CLFOD1D	6	2	174-27	0CLFOD1D	5	2	174-44	1CLFOD1D	6	2
6	070-25	0FOMPOE	10	1	070-46	1FOMPOE	11	1	170-25	0FOMPOE	10	1	170-46	1FOMPOE	11	1
	074-27	0CLFOD1E	5	2	074-44	1CLFOD1E	6	2	174-27	0CLFOD1E	5	2	174-44	1CLFOD1E	6	2
7	070-25	0FOMPOF	10	1	070-46	1FOMPOF	11	1	170-25	0FOMPOF	10	1	170-46	1FOMPOF	11	1
	074-26	0CLFOD1F	5	3	074-45	1CLFOD1F	6	3	174-26	0CLFOD1F	5	3	174-45	1CLFOD1F	6	3
8	070-25	0FOMPOG	10	1	070-46	1FOMPOG	11	1	170-25	0FOMPOG	10	1	170-46	1FOMPOG	11	1
	074-26	0CLFOD1G	5	3	074-45	1CLFOD1G	6	3	174-26	0CLFOD1G	5	3	174-45	1CLFOD1G	6	3
9	070-25	0FOMPOH	10	1	070-46	1FOMPOH	11	1	170-25	0FOMPOH	10	1	170-46	1FOMPOH	11	1
	074-26	0CLFOD1H	5	3	074-45	1CLFOD1H	6	3	174-26	0CLFOD1H	5	3	174-45	1CLFOD1H	6	3
10	070-25	0FOMPOI	10	1	070-46	1FOMPOI	11	1	170-25	0FOMPOI	10	1	170-46	1FOMPOI	11	1
	074-26	0CLFOD1I	5	3	074-45	1CLFOD1I	6	3	174-26	0CLFOD1I	5	3	174-45	1CLFOD1I	6	3
11	070-25	0FOMPOJ	10	1	070-46	1FOMPOJ	11	1	170-25	0FOMPOJ	10	1	170-46	1FOMPOJ	11	1
	074-26	0CLFOD1J	5	3	074-45	1CLFOD1J	6	3	174-26	0CLFOD1J	5	3	174-45	1CLFOD1J	6	3

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE J
MASTER SELECT 0 IN ALL CHAINS AND ERROR SUMMARY IN ONE CHAIN

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-21	0ESPO	14	4
	070-29	0OSCES	1	1
	070-23	0IOOMSE1	12	4
	074-28	0MES1	8	1
	070-25	0FOMES1	10	1
	078-20	0PLOES1	1	11
1	070-50	1ESPO	15	4
	070-42	1OSCES	2	1
	070-48	1IOOMSE1	13	4
	074-43	1MES1	9	1
	070-46	1FOMES1	11	1
	078-52	1PLOES1	2	11
2	170-21	0ESPO	14	4
	170-29	0OSCES	1	1
	170-23	0IOOMSE1	12	4
	174-28	0MES1	8	1
	170-25	0FOMES1	10	1
	178-20	0PLOES1	1	11
3	170-50	1ESPO	15	4
	170-42	1OSCES	2	1
	170-48	1IOOMSE1	13	4
	174-43	1MES1	9	1
	170-46	1FOMES1	11	1
	178-52	1PLOES1	2	11

TABLE K
MASTER SELECT 1, 2, OR 3 WITH ERROR SUMMARY IN ONE CHAIN

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEADS	FS	SYM
0	070-29	Master select control input-output leads	1	1
1	070-42		2	1
2	170-29		1	1
3	170-42		2	1

TABLE L
FRAME MATCH ERROR IN ONE CHAIN

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	074-28	0FMPO	8	1
	070-27	0FRSO	3	2
	074-27	0CLFOMA	5	2
	074-44	1CLFOMB	6	2
	174-45	1CLFOMOC	6	3
1	074-43	1FMPO	9	1
	070-44	1FRSO	4	2
	074-44	1CLFOMA	6	2
	074-27	0CLFOMB	5	2
	174-26	0CLFOMOC	5	3
2	174-28	0FMPO	8	1
	170-27	0FRSO	3	2
	174-27	0CLFOMA	5	2
	174-44	1CLFOMB	6	2
	074-26	0CLFOMOC	5	3
3	174-43	1FMPO	9	1
	170-44	1FRSO	4	2
	174-44	1CLFOMA	6	2
	174-27	0CLFOMB	5	2
	074-45	1CLFOMOC	6	3

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE M
DETERMINE COMMON CHAIN

THREE CHAINS WITH READ 0 BIT 0 OR 1 SET	COMMON CHAIN
0, 1, 2	0
0, 1, 3	1
1, 2, 3	2
0, 2, 3	3

TABLE O
FRAME MATCH AND COUNTER MATCH ERROR IN ONE CHAIN

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01	
		FS	SYM
0	074-28	8	1
1	074-43	9	1
2	174-28	8	1
3	174-43	9	1

TABLE P
FRAME MATCH ERROR AND COUNTER MATCH ERROR IN THREE CHAINS

COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-27	0FRM1A 0FRM1B 0FRM1C 0FRCSO	3	2
	070-28	0CLCM	3	1
1	070-44	1FRM1A 1FRM1B 1FRM1C 1FRCSO	4	2
	070-43	1CLCM	4	1
2	170-27	0FRM1A 0FRM1B 0FRM1C 0FRCSO	3	2
	170-28	0CLCM	3	1
3	170-44	1FRM1A 1FRM1B 1FRM1C 1FRCSO	4	2
	170-43	1CLCM	4	1

TABLE N
FRAME MATCHER ERROR IN THREE CHAINS AND NO COUNTER MATCH ERROR

COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-26	0CLFODR	5	1
	070-27	0FRCSO	3	2
1	070-45	1CLFODR	6	1
	070-44	1FRCSO	4	2
2	170-26	0CLFODR	5	1
	170-27	0FRCSO	3	2
3	170-45	1CLFODR	6	1
	170-44	1FRCSO	4	2

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

TABLE Q
FRAME MATCHER ERROR
IN TWO CHAINS AND COUNTER MATCH ERROR IN THREE CHAINS

COMMON CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM
0	070-27	0FRCS0	3	2
	070-23	0STCPST1	12	4
1	070-44	1FRCS0	4	2
	070-48	1STCPST1	13	4
2	170-27	0FRCS0	3	2
	170-23	0STCPST1	12	4
3	170-44	1FRCS0	4	2
	170-48	1STCPST1	13	4

TABLE R
COUNTER MATCH ERROR ONLY (ONE CHAIN)

CHAIN	SUSPECT PACK LOCATION	SD-4A036-01			CHAIN	SUSPECT PACK LOCATION	SD-4A036-01		
		LEAD	FS	SYM			LEAD	FS	SYM
0	074-28	0CMPO 0FRM1A 1FRM1B 0FRMI1C	8	1	2	174-28	0CMPO 0FRM1A 1FRM1B 0FRMI1C	8	1
	070-27	0FRM1A	3	2		170-27	0FRM1A	3	2
	070-44	1FRM1B	4	2		170-44	1FRM1B	4	2
	170-44	1FRM01C	4	2		070-27	0FRM01C	3	2
1	074-43	1CMPO 1FRM1A 0FRM1B 1FRMI1C	9	1	3	174-43	1CMPO 1FRM1A 0FRM1B 1FRMI1C	9	1
	070-44	1FRM1A	4	2		170-44	1FRM1A	4	2
	070-27	0FRM1B	3	2		170-27	0FRM1B	3	2
	170-27	0FRM01C	3	2		070-44	1FRM01C	4	2

ANALYZE NCFR F-LEVEL INTERRUPT ALL CHAINS IN SERVICE PRIOR TO INTERRUPT

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

[1] Using SCLK F-level printout, identify PMD number rightmost two octal digits of PU4FRPMD word [FIG. 1]

[2] Is PMD number 11, 12, or 16 through 21

Yes → [3] Analyze NCFR F-level interrupt [TAP-130]

No

[4] Is PMD any number 70 through 74

Yes → [5] Read PMD description in TABLE A → TAP-132

No

[6] Note PMD description in TABLE A, Page 2

[7] Identify suspect controller from F-level printout header text

AND

[8] Is any bit 0 through 6 set to one in RCNT+15 or RCNT+16 word [FIG. 2]

Yes → Page 4

No

[9] Is bit 7 set to one in RGNT+15 or RGNT+16

Yes → TAP-132

No

[10] Is AC1LR register all zeros [FIG. 3]

Yes → [11] Use TABLE B, Page 3, to identify suspect packs and leads in suspect CONTR

No → [12] Use TABLE C, Page 3, to identify suspect packs and leads in suspect CONTR

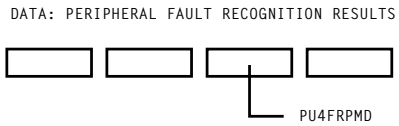


FIG. 1

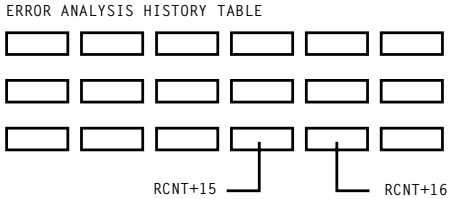


FIG. 2

FIG. 3

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TABLE A
PMD DESCRIPTIONS

PMD	SCFR FOUND
1	Neither controller had errors
2	Both controllers found to be OS
3	Both controllers are in service and controller 1 had ASWF
4	Both controllers are in service and controller 0 had ASWF
5	Controller 0 had ASWF by itself
6	Controller 1 had ASWF by itself
7	Both controllers are in service and controller 0 had counter mismatch
10	Both controllers are in service and controller 1 had counter mismatch
11	Network clock bay 0 is faulty
12	Network clock bay 1 is faulty
13	Duplex CONFIG; counter mismatch not resolved
14	System clock has counter fault and controller 0 is in service
15	System clock has counter fault and controller 1 is in service
16	Network clock bay 1 is in trouble and system clock controller 0 is in service
17	Network clock bay 1 is in trouble and system clock controller 1 is in service
20	Network clock bay 0 is in trouble and system clock controller 0 is in service
21	Network clock bay 0 is in trouble and system clock controller 1 is in service
22	Error not resolved
23	Error not resolved
24	Duplex CONFIG; controller 0 had error
25	Duplex CONFIG; controller 1 had error
26	Reply register mismatch; only controller 0 had error
27	Reply register mismatch; only controller 1 had error
30	Reply register mismatch; error not resolved
31	Duplex, failing OPCODE
32	Simplex, failing OPCODE, controller 0 in service
33	Simplex, failing OPCODE, controller 1 in service
34	Duplex, enable not set
35	Simplex, enable not set, controller 0 in service
36	Simplex, enable not set; controller 1 in service
37	Both controllers recorded invalid OPCODE erroneously
40	Only controller 0 on line recorded invalid OPCODE erroneously
41	Only controller 1 on line recorded invalid OPCODE erroneously
42	Controllers are duplexed and only controller 0 recorded invalid OPCODE incorrectly
43	Controllers are duplexed and only controller 1 recorded invalid OPCODE incorrectly
44	Duplex, M bit not set
45	Simplex, M bit not set, controller 0 in service
46	Simplex, M bit not set, controller 1 in service
47	Both controllers in service but only controller 0 recorded mode failure incorrectly
50	Both controllers in service but only controller 1 recorded mode failure incorrectly
51	Both controllers recorded mode failure incorrectly
52	Only controller 0 in service and it recorded mode failure erroneously
53	Only controller 1 in service and it recorded mode failure erroneously
54	Could not find any parity errors

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

TABLE A (Contd) PMD DESCRIPTIONS	
PMD	**SCFR FOUND**
55	Even parity in simplex controller 0 controller 0
56	Odd parity in simplex
57	Even parity in simplex controller 1
60	Odd parity in simplex controller 1
61	Even, odd, or mixed parities in duplex controllers
62	Even parity in duplex controller 0
63	Even parity in duplex controller 1
64	Odd parity in duplex controller 0
65	Odd parity in duplex controller 1
66	Even parity in duplex controllers 0 and 1
67	Odd parity in duplex controllers 0 and 1
70	SYSCLK duplexed with NCSU ASWF in only one controller's ESR
71	SCLK duplex with NCSU ASWF error bit set in controller 1
72	SCLK simplex with NCSU ASWF error bit set in in-service SCLK controller
73	SCLK duplex with NCSU ASWF error bit set in both SCLK controllers
74	SYNC Unit caused reply register mismatch in duplex SCLK controllers

TABLE B
AC1LR REGISTER ALL ZEROS

UNIT	SUSPECT PACK TYPE	SUSPECT PACK LOCATION	LEAD*	FS*	SYM*	COMMENT
SCLU IPUB	**FA1237**	060-32	0BCLMP1†	2	31	
		160-32	1BCLMP1†	3	31	
	OPSC2 RELAY	055-59	0BSEL	12	30	Contact 2M (SCLK CONTR 0)
	1PSC2 RELAY	155-59	1BSEL	13	30	Contact 2M (SCLK CONTR 1)
SCLK	FC12	56-44‡	§MABB	8	1	

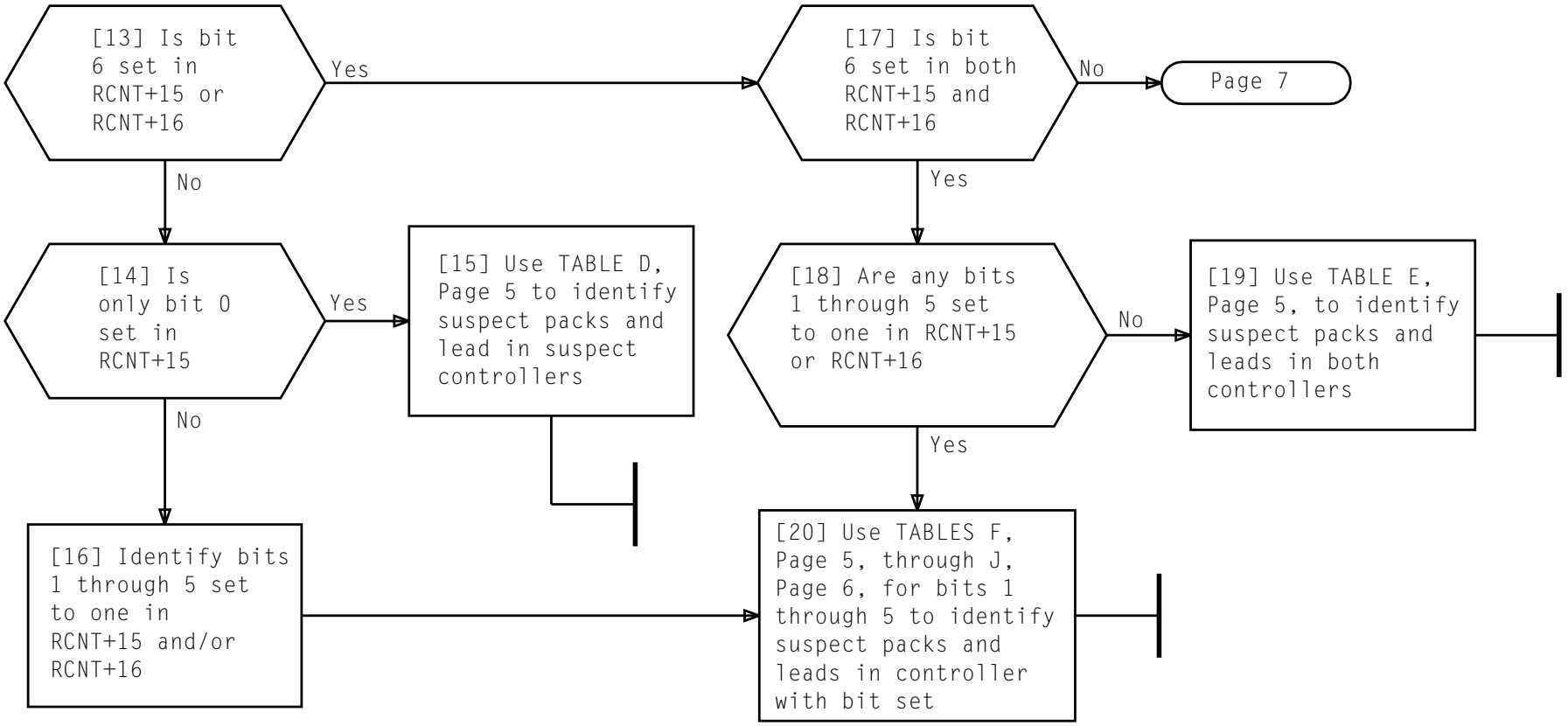
* SCLK — SD-4A037-02, NCLK — SD-4A014-02
† SCLK CONTR
‡ SCLK Suspect pack bay location — SCLK controller number
§ BUS

TABLE C
AC1LR REGISTER NOT ZEROED

UNIT	SUSPECT PACK TYPE	SUSPECT PACK LOCATION†	LEAD*	FS*	SYM*	COMMENT
SCLK	**FA1807**	†56-41	RPASW0	9	2	
	FA641	†56-42	ASW0‡	9	1	
SCLU IPUB	**FA1237**	060-31	0ASW	2	32	BUS 0
		160-31	1ASW	3	32	BUS 1
	FC13	060-27	0PUASWP/NI	2	12	BUS 0
		160-27	1PUASWP/NI	3	12	BUS 1

* SCLK — SD-4A037-02, NCLK — SD-4A014-02
† SCLK Suspect bay location — SCLK controller number
‡ BUS

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK



ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

TABLE D
BIT 0 (ONLY)

SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION*	LEAD	FS	SYM
FA529	56-39	ESASW	5	2
FA529	56-40	ERRSUM	5	7
FA1807	56-41	ESRG	9	2

* Suspect pack bay location - SCLK controller number

TABLE E
BIT 6 (BOTH CONTROLLERS)

SUSPECT PACK*		SD-4A037-02		
TYPE	LOCATION†	LEAD	FS	SYM
FA531	56-34	RPBMAT1	4	4,5
	56-33	RPBMA01	4	1,2,3
	56-23	MORB0,1,2	1	2
	56-20	MORB3,4,5	1	5
	56-24	MORB6,7,8	1	8
	56-25	MORB9,10,11	1	11
FA528	56-22	MORB12,13,14	1	14
	56-21	MORB15,16,17	1	17
	56-31	MORB18,19,20	1	20
	56-32	MORB21,22,23	1	23
FA1807	56-41	STRMF	9	2
FB232	56-06	16CLAP	12	1

* Suspect pack list applies to both SCLK controllers
† Suspect pack bay location — SCLK controller number

TABLE F
BIT 1

UNIT	SUSPECT PACK LOCATION	LEAD*	FS*	SYM*	COMMENT
SCLK	56-39†	CNTRMM	5	2	**FA529**
	56-13†	MATO	11	1	**FA640**
	56-41†	ESRG	9	2	**FA1807**
	56-07†	MATCH	13	5-7	**FA531**
	56-08†	MATCH (0,1)	13	1-4	**FA636**
	56-10†	ST0A-ST6A	14	1,2	**FA636**
	56-12†	ST0B-ST6B	14	3,4	**FA637**
	56-11†	ST7A-ST28A	15	1	**FA637**
	56-09†	ST7B-ST28B	15	2	**FA637**
	56-06†	8KCAP, 8KCBP, WINAP	12	1	**FB232**
NCLK	078-21‡	0CLK00	1	1	If SCLK CONTR 0 suspect
	078-22‡	0CLK01	1	1	If SCLK CONTR 1 suspect
	178-21‡	1CLK00	1	2	If SCLK CONTR 1 suspect
	178-22‡	1CLK01	1	2	If SCLK CONTR 0 suspect
	Cables carrying 16 mHz signal from NCLK (**FB211**) to SCLK (**FB232**) are also suspect				

* SCLK — SD-4A037-02;NCLK — SD-4A014-02
† SCLK suspect pack bay location — SCLK controller number
‡ These **FB211** packs require special replacement procedures. See [234-151-013]

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

TABLE G
BIT 2

SUSPECT PACK		SD-4A037-02			SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM	TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-39	ESPFE	5	2	**FA528**	56-23	WRPEV0	1	1
FA534	56-27	PEVCHK	2	1,3		56-20	WRPEV1	1	4
FA551	56-38	STRPTF	7	1		56-24	WRPEV2	1	7
FA1807	56-41	STERRA0	9	2		56-25	WRPEV3	1	10
FA641	56-42	TANIO	9	1		56-22	WRPEV4	1	13
						56-21	PRTEV	1	16
						56-31	WRPEV6	1	19
						56-32	EA00	1	22

* Suspect pack bay location — SCLK controller number

TABLE H
BIT 3

SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-39	ESPF0	5	2
FA534	56-27	PODCHK	2	2,4
FA551	56-38	STRPTF	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1
FA528	56-23	WRPOD0	1	1
	56-20	WRPOD1	1	4
	56-24	WRPOD2	1	7
	56-25	WRPOD3	1	10
	56-22	PRTOD	1	13
	56-21	WRPOD5	1	16
	56-31	EA01	1	19
	56-32	WRPOD7	1	22

* Suspect pack bay location — SCLK controller number

TABLE I
BIT 4

SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-40	ESIVOP	5	7
FA639	56-43	IVOPC	10	1
FA528	56-23	WB29	1	1
	56-24	WB31 WB33 WB35	1	7
	56-25	WB30 WB32 WB34	1	10
	56-32	EA00	1	22
	56-31	EA01	1	19
FA551	56-38	STIVOP	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1

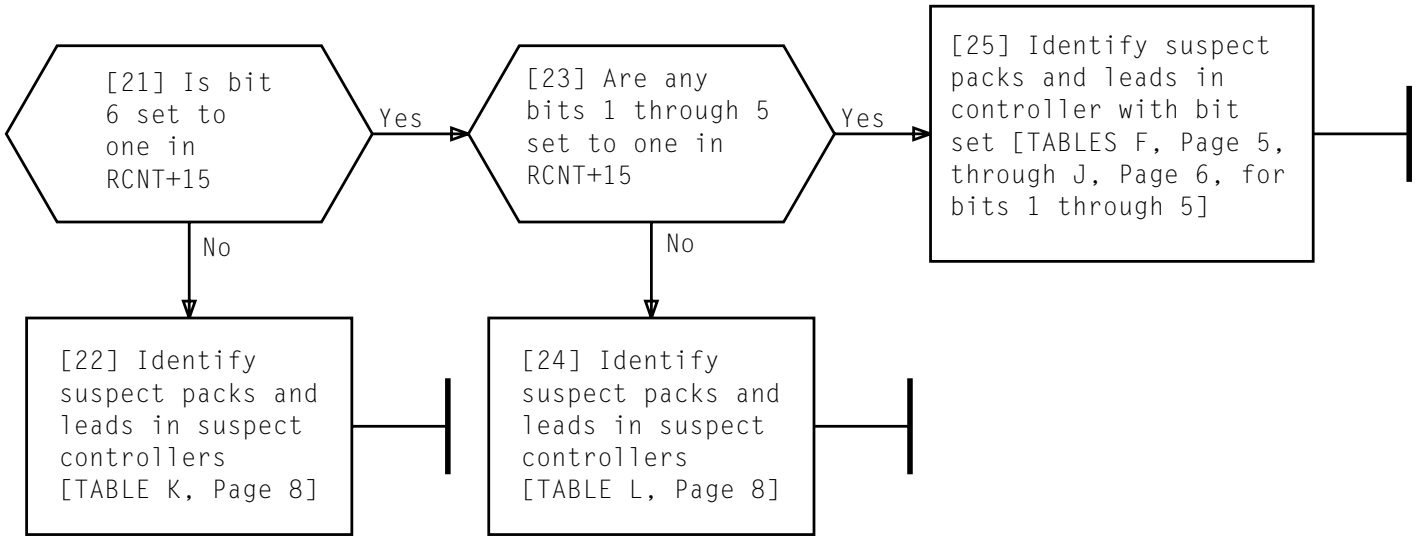
* Suspect pack bay location — SCLK controller number

TABLE J
BIT 5

SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION *	LEAD	FS	SYM
FA529	56-40	ESMODF	5	7
FA639	56-43	MODF	10	1
FA528	56-24	WB35	1	7
	56-32	MBIT	1	22
FA529	56-39	SRMAS	5	2
FA551	56-38	STIVOP	7	1
FA1807	56-41	STERRA0	9	2
FA641	56-42	TANIO	9	1

* Suspect pack bay location — SCLK controller number

ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK



ANALYZE SCFR F-LEVEL INTERRUPT, SYSTEM CLOCK

TABLE K
RCNT+16 REGISTER BIT 6 SET

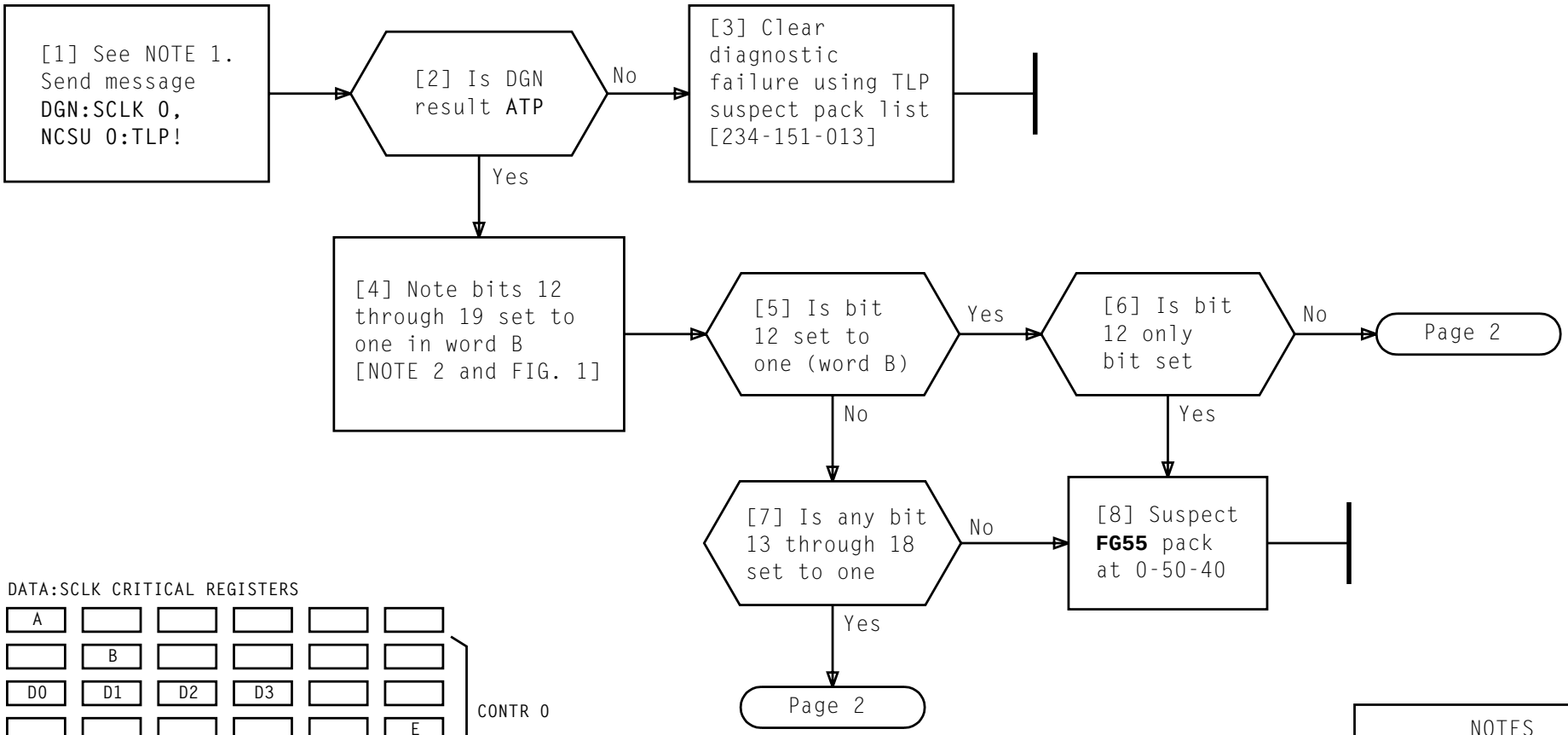
UNIT	SUSPECT PACK		LEAD*	FS†	SYM†
	TYPE	LOCATION*			
SCLK	**FA1807**	56-41	RPASWO	9	2
	FA641	56-42	CLOUT	9	1
	FB232	56-06	16CLAP	12	1
	FA639	56-43	ACOPC	10	1
	FA531	56-26	KMATCH1	3	2
	FA528	56-22	EA3, EA5	1	13
		56-21	EA2, EA4, EA6	1	16
		56-31	EA7, EA9, EA11	1	19
		56-32	EA8, EA10	1	22
SCLK IPUB	**FC12**	060-34	OSYCO	2	7
		160-34	ISYCO	3	7

*SCLK suspect pack bay location — SCLK controller number
†SCLK — SD-4A037-02, NCLK — SD-4A014-02

TABLE L
RCNT+15 REGISTER BIT 6 SET

SUSPECT PACK		SD-4A037-02		
TYPE	LOCATION*	LEAD	FS	SYM
FA529	56-40	ESRMF	5	7
FA531	56-34	RPBMAT1	4	4,5
	56-33	RPBMA01	4	1,2,3
FA1807	56-41	STRMF	9	2
FB232	56-06	16CLAP	12	1

*Suspect pack bay location — SCLK controller number



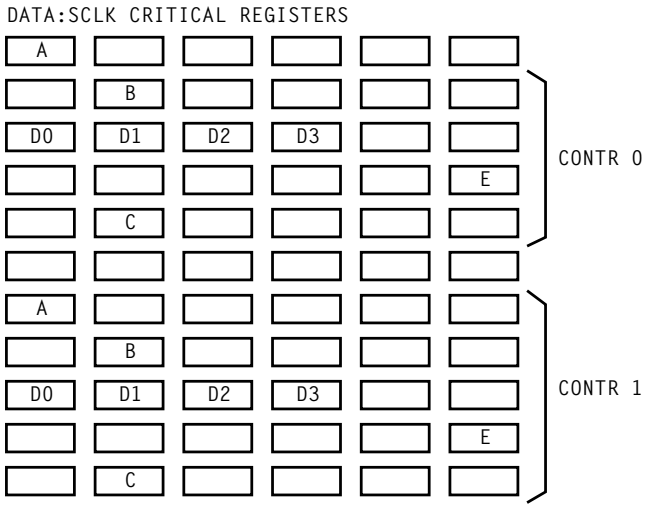
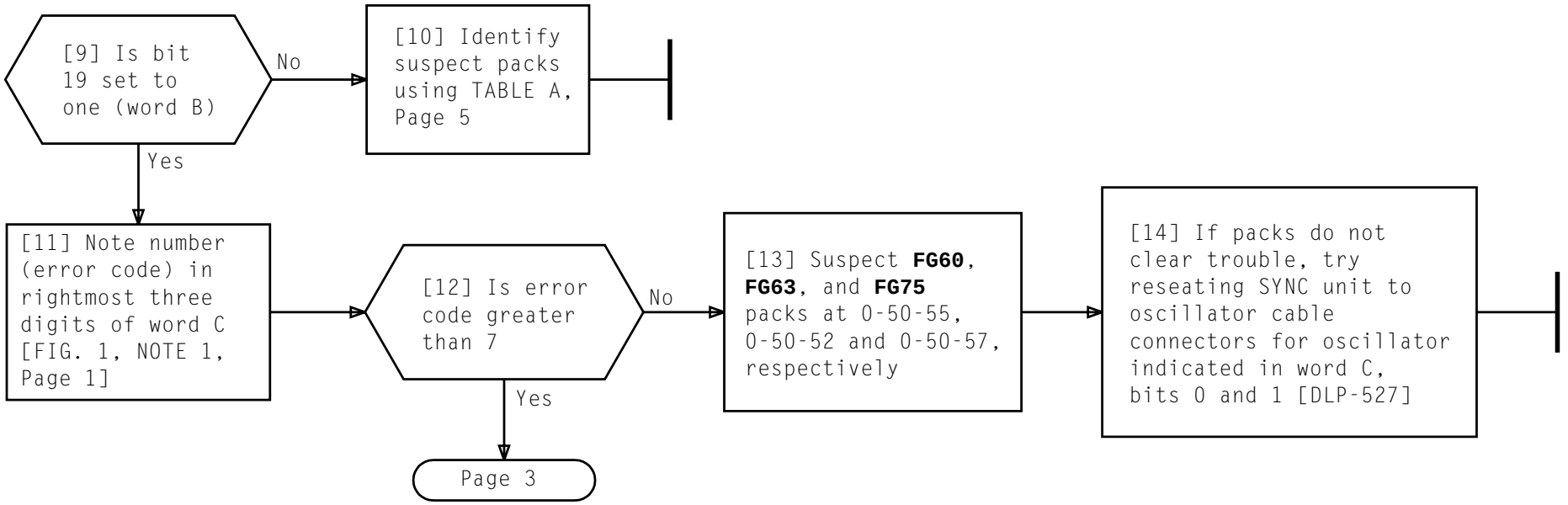


FIG. 1 – SCLK Critical Registers

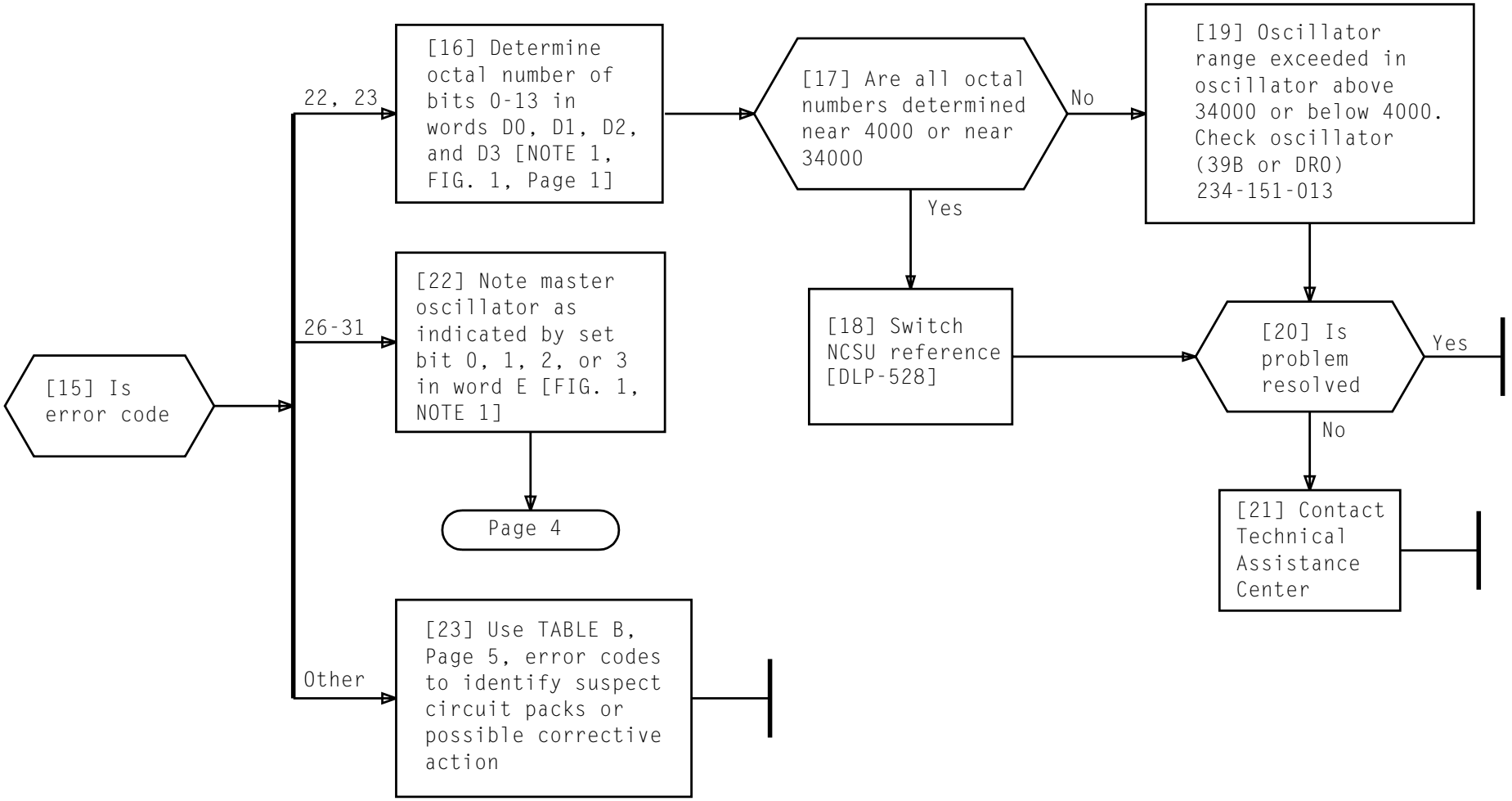
NOTES

1. If NCSU uses BSRF, be sure its signal level is within specifications.
2. If bit 12 of word A equals 0, use CONTR 0 words in FIG. 1. If it equals 1, use CONTR 1 words

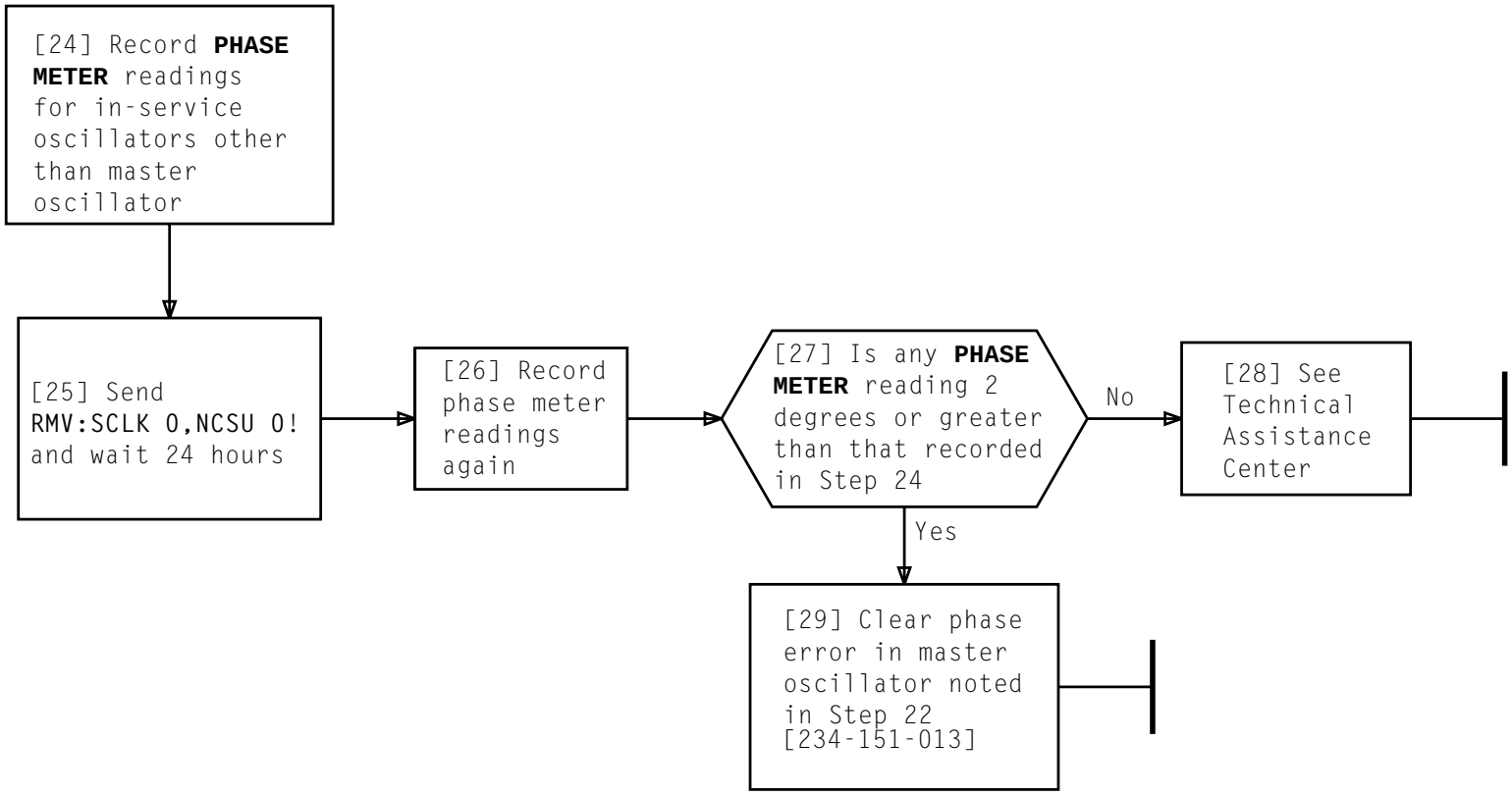
ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) F-LEVEL INTERRUPT



ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) F-LEVEL INTERRUPT



ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) F-LEVEL INTERRUPT



ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) F-LEVEL INTERRUPT

TABLE A
ALL SEEMS WELL ERROR SOURCE REGISTER (ASWESR)

BIT	BIT DESCRIPTION	PACK	LOCATION	COMMENTS
13	Clock parity error	**FG56**	0-50-36	SD-4A105, FS2, SYM 1, leads B1-B40
14	Clock error	**FG55** **FG63** **FG56**	0-50-40 0-50-52 0-50-36	
15	Microprocessor match failure	**FG57** **FG63** **FG58**	0-50-42 0-50-52 0-50-44	FG92 for DRO OSC.
16	Microprocessor sanity	**FG63** **FG62**	0-50-52 0-50-59	
17	Invalid OPCODE	**FG56** **FG53**	0-50-36	
		FA1806	*-56-43	System clock
18	Microprocessor trap	**FG63** **FG58** **FG59**	0-50-52 0-50-44 0-50-46	FG92 for DRO OSC.

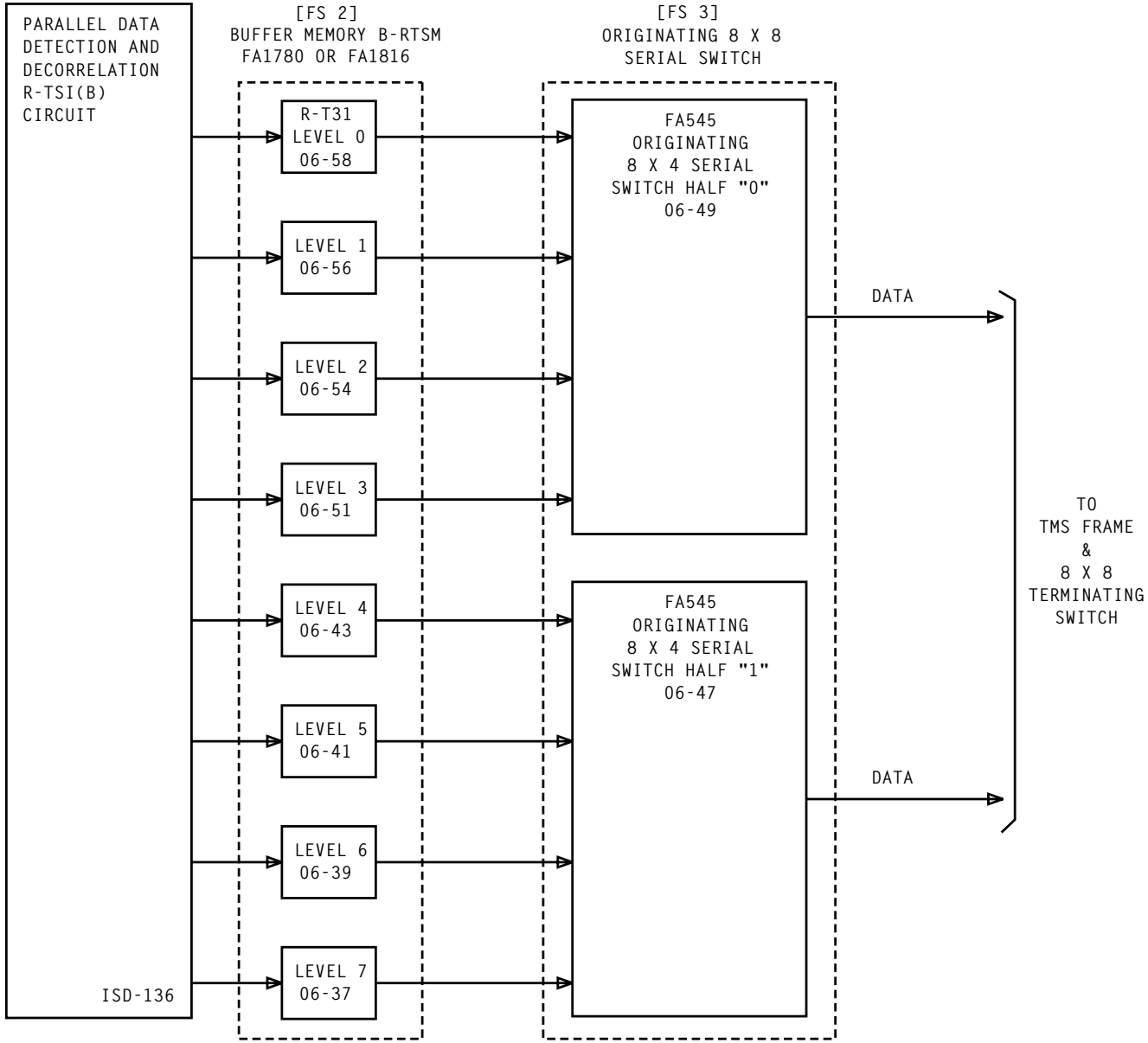
* If FIG. 1, word A, bit 1 set, * = 1; if not set, * = 0

TABLE B
ERROR CODES (WORD C)*

CODE	PACK	LOCATION	COMMENTS
10	**FG61** **FG62**	0-50-63 0-50-59	
	Clear phase error — 234-151-013		
11	Same as code 40		
13	**FG63** **FG64** **FG59**	0-50-52 0-50-65 0-50-46	
	Clear phase error — 234-151-013		
14	Same as code 10		
15	Same as code 40		
17	**FG64** **FG63** **FG59**	0-50-65 0-50-52 0-50-46	
20	**FG64** **FG61**	0-50-65 0-50-63	
21	Switch NCSU reference [DLP-528]		
	FG65 **FG64**	0-50-67 0-50-65	
24	Switch NCSU reference [DLP-528]		
32	Same as code 21		
33	Same as code 40		
34	**FG61** **FA628** **FA628** **FA628** **FA628**	0-50-63 0-70-29 0-70-42 1-70-29 1-70-42	 Chain 0 Chain 1 Chain 2 Chain 3
35	**FG63** **FG61**	0-50-52 0-50-63	
36	Same as code 10 (for 39B OSC.)		
	Check for major alarm on a DRO OSC.		
37	**FG64** **FB232** **FG61**	0-50-65 -56-96† 0-50-63	 SCLK
40	See RWC, 4ESAC, or PECC		
42	Check for DRO OSC. power failure		

* Partial list — other error codes within this TAP
† If FIG. 1, word A, bit 1 set, * = 1; if not set, * = 0

ANALYZE NETWORK CLOCK SYNC UNIT (NCSU) F-LEVEL INTERRUPT



BUFFER MEMORY B AND ORIGINATING R-TSI(B) CIRCUIT

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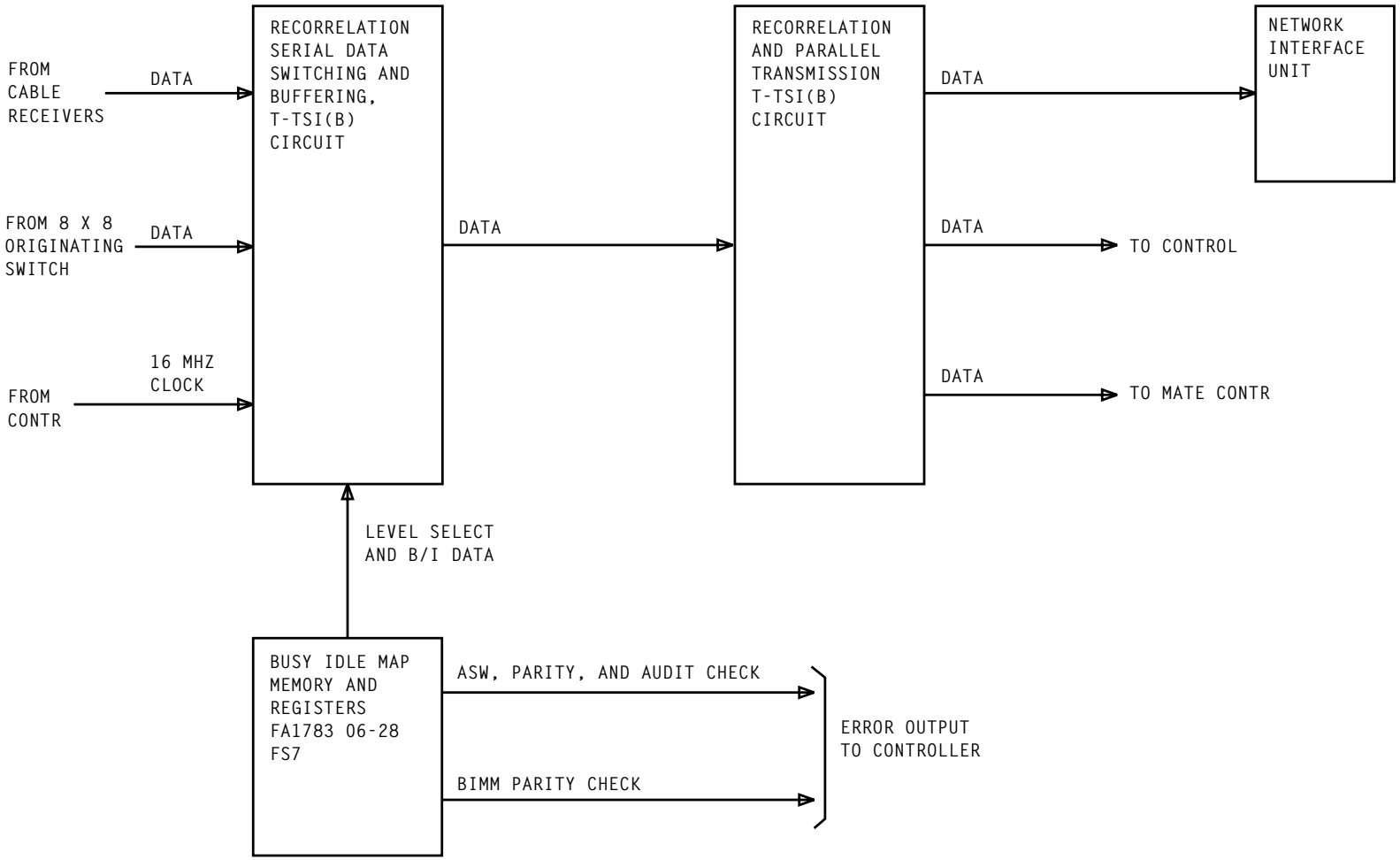
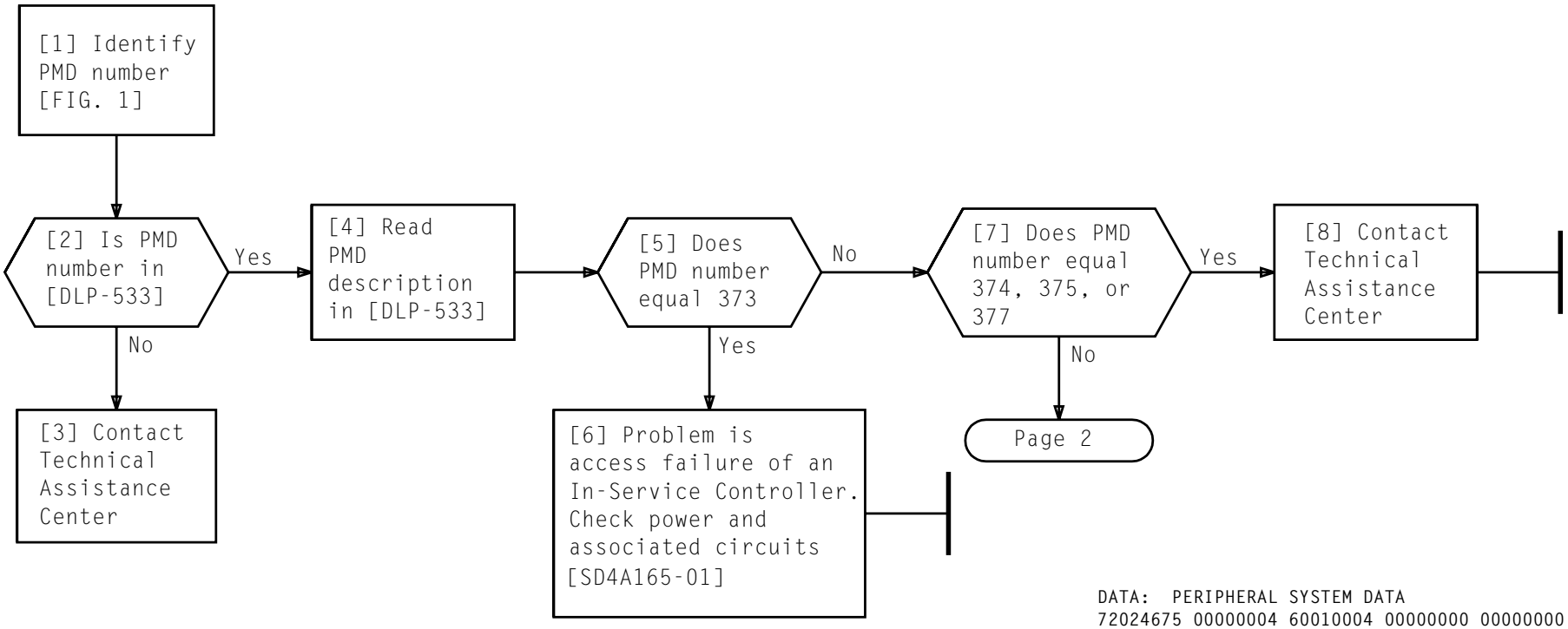


TRANSMIT TSI, TSI-B SWITCHING AND PERMUTING CIRCUIT

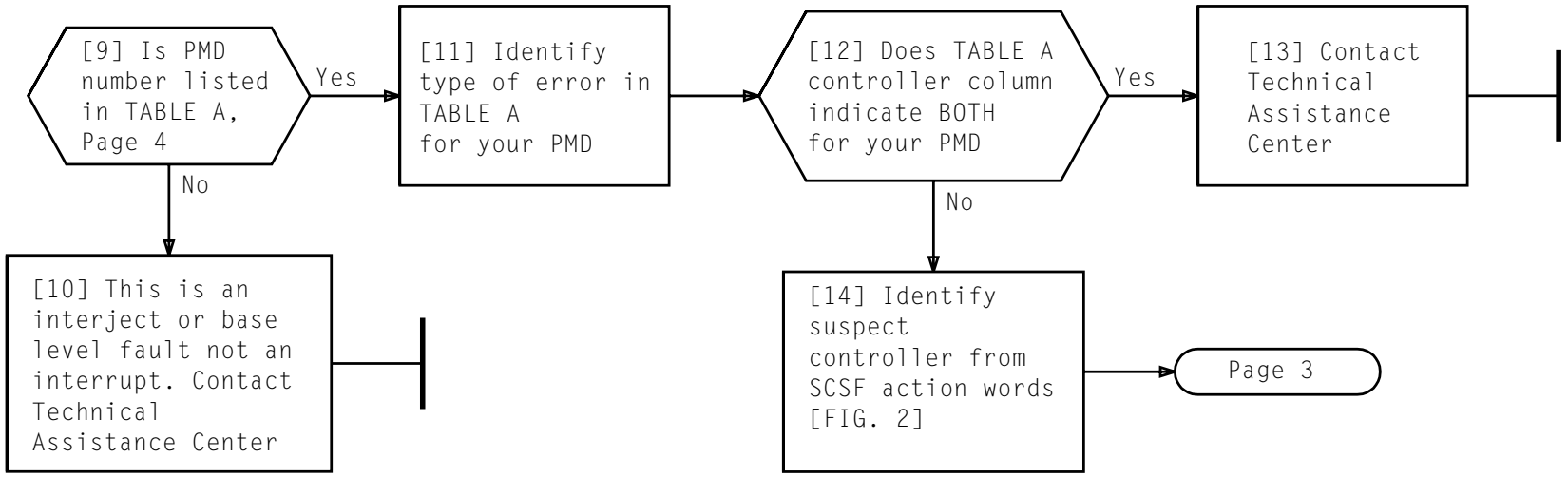



```
DATA:  PERIPHERAL SYSTEM DATA
72024675 00000004 60010004 00000000 00000000 00000004
00000000 00000004 00000000 01600001 01600041 60070041
01600041
DATA:  INTERRUPT SOURCE DATA
00004401 77777766 00754000 02000000 00000001
DATA:  FAULT RECOGNITION ISOLATION DATA
00000001 00000000 00000051 00000000 00000003 00000000
DATA:  ERROR ANALYSIS STRATEGY DATA
00112000 00037200 00200100 00000022 00012000 01000101
00000000 00040000 00003051 01000000 62000000 01000000
00000000 00000000 00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000 00000000 12330204
12326240 14401152 00433106 00000034 00000000 00000001
00000000 00001604
04/21/92  10:00:52
#469
```

POINT OF MAXIMUM DEFINITION (PMD)

FIG. 1 — Part of SCSF F-Level Printout

ANALYZE SCSF, F-LEVEL INTERRUPT



CSTATUS	HWSTATR	MADATA	FSTATUS	SCUOS	CESR
PEST	CONTROL	EBLKSTATL	EBLKSTATH	EBLKADR	GRESR
GRCNTR	GADRMO	GADRM1	EXESR	EXCSTATML	EXCSTATMH
EXFPTR	EXPC	EXSANTIM	EXSTKBL	EXSTKBH	EXSTRPTR
EXINTR	RLPBPTR	WLPBPTR	RDBPTR	WDBPTR	MBPTRS
SDOWMBPTR	MBSTAT	SCU0ESR	SCU1ESR	SCU2ESR	SCU3ESR
SCU4ESR	SCU5ESR	SCU6ESR	SCU7ESR	SCU8ESR	SCU9ESR
SCU10ESR	SCU11ESR	SCU12ESR	SCU13ESR	SCU14ESR	SCU15ESR
FWERRBUF0	FWERRBUF1	FWERRBUF2	FWERRBUF3	FWERRBUF4	FWERRBUF5
FWERRBUF6	FWERRBUF7	FWERRBUF8	FWERRBUF9	EBERRORM	EBLKADRM
EBLKSTATML	EBLKSTATMH	0.....0	0.....0	0.....0	0.....0
MEMN	XLATE	5.....5	5.....5	5.....5	5.....5
CSTATUS	HWSTATR	MADATA	FSTATUS	SCUOS	CESR
PEST	CONTROL	EBLKSTATL	EBLKSTATH	EBLKADR	GRESR
GRCNTR	GADRMO	GADRM1	EXESR	EXCSTATML	EXCSTATMH
EXFPTR	EXPC	EXSANTIM	EXSTKBL	EXTKBH	EXSTRPTR
EXINTR	RLPBPTR	WLPBPTR	RDBPTR	WDBPTR	MAPTAS
SDOWMBPTR	MBSTAT	SCU0ESR	SCU1ESR	SCU2ESR	SCU3ESR
SCU4ESR	SCU5ESR	SCU6ESR	SCU7ESR	SCU8ESR	SCU9ESR
SCU10ESR	SCU11ESR	SCU12ESR	SCU13ESR	SCU14ESR	SCU15ESR
FWERRBUF0	FWERRBUF1	FWERRBUF2	FWERRBUF3	FWERRBUR4	FWERRBUF5
FWERRBUF6	FWERRBUF7	FWERRBUR8	FWERRBUF9	EBERRORM	EBLKADRM
EBLKSTATML	EBLKSTATMH	0.....0	0.....0	0.....0	0.....0

CONTR 0

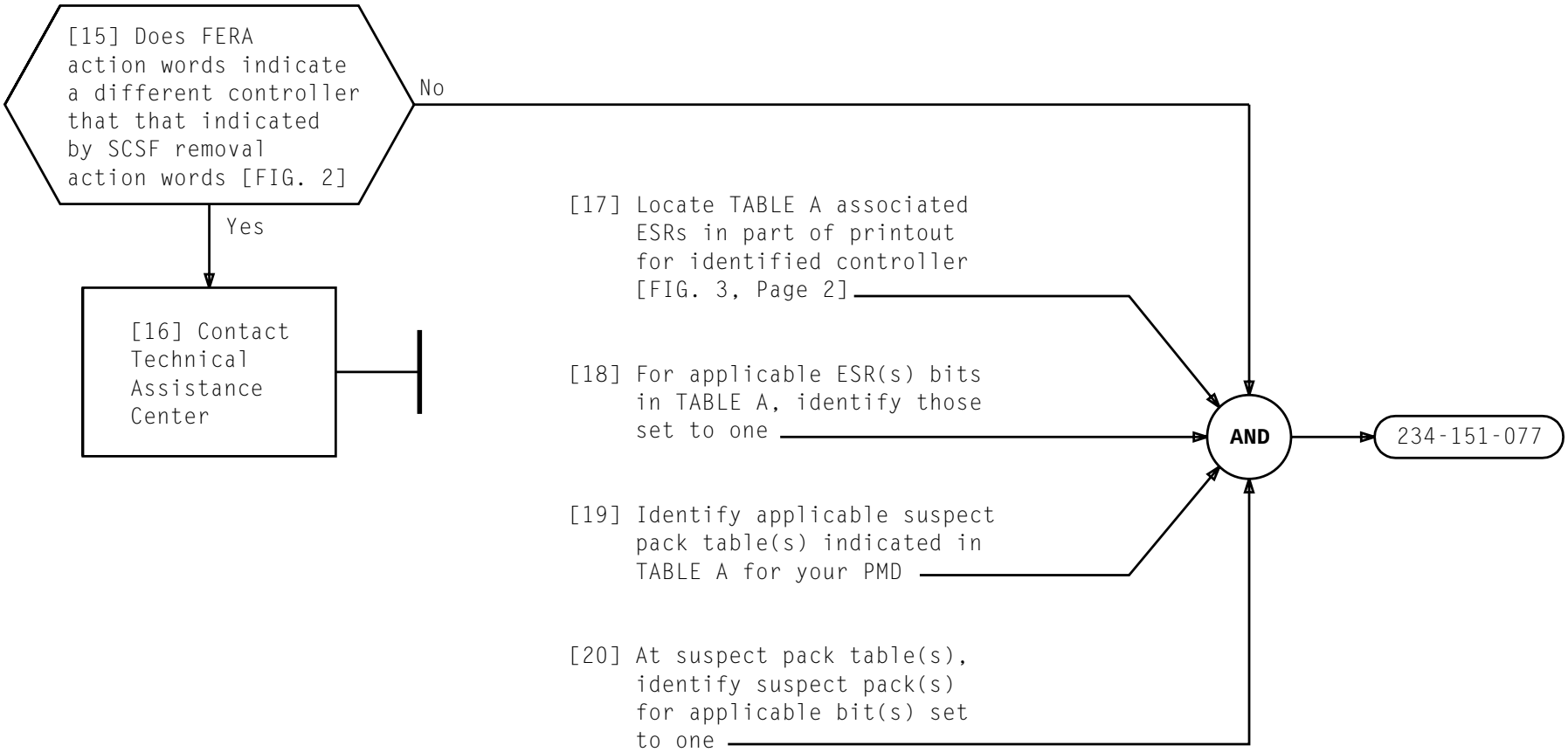
CONTR 1

FIG. 3 — SCS Critical Register (CREG) Layout [Part of REPT Message]

```
A 00 REPT: F-LEVEL @15742476 MFNUM=00000034 MICON=00000020   MSG STARTED
     LV=0040 D0=00000000 D1=00000000 D2=00000217 D3=00000000
      APUFS INTERRUPT SCS 0
     SCSF RESOLVED ERROR SCS 0 CONTR 0
     SCSF RECOMMENDED NORMAL REMOVAL SCS 0 CONTR 0
     SCSF RECOMMENDED DIAGNOSTICS SCS 0 CONTR 0
     FERA REMOVED SCS 0 CONTR 0
     FERA SCHED DGN SCS 0 CONTR 0
     DATA:  F-LEVEL
```

FIG. 2 — Part of F-Level Interrupt Printout

ANALYZE SCSF, F-LEVEL INTERRUPT



ANALYZE SCSF, F-LEVEL INTERRUPT

TABLE A					
PMD NUMBER	CONTROLLER	TYPE OF ERROR	ASSOCIATED ERROR SOURCE REGISTER	APPLICABLE ESR BIT(S)	ESR SUSPECT PACK TABLE
331,340,350,360	ACTIVE	RAM ERROR	GRESR	0,1,2,3,4,5,6,7	E
330,341	STANDBY		EXESR	3,5,6,7,8,9,10,11,12	F
57	BOTH	SANITY/STACK BOUNDARY	EXESR	0,1	F
56,75,155,173	ACTIVE				
55,76	STANDBY				
332	BOTH	FATAL FIRMWARE	CESR	8	B
333,343,353,363	ACTIVE				
334,344	STANDBY				
47	BOTH	FIRMWARE (NO PPE)	CESR	7,9,10,11	B
50,117,153,176	ACTIVE				
51,125	STANDBY				
52	BOTH	FIRMWARE (WITH PPE)	CESR	7,9,10,11,13	B
53,126,154,174	ACTIVE				
54,127	STANDBY				
46,62,113,114,115,116,124	BOTH	MISMATCH	CESR	22,23	B
44,60,103,104,105,106,122,152,175	ACTIVE				
45,61,107,110,111,112,123	STANDBY				
262,272	BOTH	IAS	EBLKSTATL	0,1,2,4,7	C
261,271	ACTIVE				
260,270	STANDBY		EBLKSTATH	0,1,4	D
40,41,42,43	BOTH	HARDWARE	CESR	6,12,13,14,15,16,17,18,19,20,21	B
30,31,32,33,71,72,120,150,151,171,172,177	ACTIVE				
34,35,36,37,73,74,121	STANDBY				
1,4,5,70	BOTH	NO ERROR SOURCE	CESR	0,1	B
2,130,131,132,170	ACTIVE				
3	STANDBY				

TABLE B
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ASWF	0DPUR260	B11/G7	1DPUR260	B24/H7	All-Seems-Well Failure (An ASWF asserts the Peripheral Unit Failure (PUF) flag)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
1	AINT	0DPUR260	B11/G7	1DPUR260	B24/H7	Autonomous Interrupt (An AINT asserts the Autonomous Peripheral Unit Failure (APUF) flag)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
2	PUPFE	0DPUW390	B11/B8	1DPUW390	B24/B8	Peripheral unit bus even parity failure (This error asserts an ASWF)	UN350 UN349 UN349 UN349	045-112 045-152 045-160 045-168	053-112 053-152 053-160 053-168
3	PUPFO	0DPUW380	B11/B8	1DPUW380	B24/B8	Peripheral unit bus odd parity failure (This error asserts an ASWF)	UN350 UN349 UN349 UN349	045-112 045-152 045-160 045-168	053-112 053-152 053-160 053-168
4	APUT	0DPUR270	B11/G7	1DPUR270	B24/H7	Autonomous Peripheral Unit Trouble (interject level) — (Indicates a Service Circuit Unit (SCU) detected error or a digit buffer overflow)	SCU x UN350 KCN3 KCN3	* 045-112 045-048 045-056	* 053-112 053-048 053-056
5	APUB	0DPUR280	B11/G7	1DPUR280	B24/H7	Autonomous Peripheral Unit Base level (NOT CURRENTLY USED BY THE SCS)	UN350 UN351	045-112 045-072	053-112 053-072
6	UNASOP	None		None		Invalid/unassigned op-code (This error asserts an ASWF)	UN350 UN349 UN349 UN351	045-112 045-152 045-160 045-072	053-112 053-152 053-160 053-072

TABLE B (Contd)
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
7	SWERR0	None		None		Firmware error bit 0 (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
8	SWERR1	None		None		Firmware error bit 1 (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
9	SWERR2	None		None		Firmware error bit 2 (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
10	SWERR3	None		None		Firmware error bit 3 (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
11	SWERR4	None		None		Firmware error bit 4 (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
12	MODFL	None		None		PUBI [UN350] Mode Failure (This error asserts an ASWF)	UN350 UN349 UN349	045-112 045-144 045-152	053-112 053-144 053-152

TABLE B (Contd)
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
13	PPE	None		None		PUBI [UN350] Parity Error (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056
14	SPARE14	None		None		Spare bit (NOT ASSIGNED) (This bit asserts an AINT/ASWF†)	UN350 UN351	045-112 045-072	053-112 053-072
15	LCLKF	None		None		PUBI [UN350] local clock failure (This error asserts an AINT/ASWF†)	UN350 UN351	045-112 045-072	053-112 053-072
16	HWSPARE0	None		None		Hardware spare 0 (NOT ASSIGNED) (This bit asserts an AINT/ASWF†)	UN350 UN351	045-112 045-072	053-112 053-072
17	HWSPARE1	None		None		Hardware spare 1 (NOT ASSIGNED) (This bit asserts an AINT/ASWF†)	UN350 UN351	045-112 045-072	053-112 053-072
18	EBSUM	0EEBSUM0	B11/B3	1EEBSUM0	B24/B3	Extended Bus interface [KCN3] error summary (This error asserts an AINT/ASWF†)	KCN3 UN350	045-048 045-112	053-048 053-112
19	GRAMSUM	0EGRSUM0	B10/F8	1EGRSUM0	B23/F8	Global RAM [UN352] memory data parity error summary (This error asserts an AINT/ASWF†)	UN352 UN350	045-088 045-112	053-088 053-112
20	EXECSUM	0EEXSUM0	B10/C5	1EEXSUM0	B23/C5	EXEC [UN351] error source summary for bits 0-15 in the EXEC error source register (This error asserts an AINT/ASWF†)	UN351 UN350	045-072 045-112	053-072 053-112
21	BPSUM	0EBPSUM0	B10/F8	1EBPSUM0	B23/F8	Backplane error summary (Detected on the GRAM [UN352] circuit pack) (This error asserts an AINT/ASWF†)	UN350 UN351 UN352 KCN3 KCN3 UN357 UN357	045-112 045-072 045-088 045-048 045-056 045-024 045-120	053-112 053-072 053-088 053-048 053-056 053-024 053-120
22	CPMM	0ECPMM0	B10/C5	1ECPMM0	B23/C5	EXEC [UN351] clock phase error (This error asserts an AINT/ASWF†)	UN351 UN350	045-072 045-112	053-072 053-112

ANALYZE SCSF, F-LEVEL INTERRUPT

TABLE B (Contd)
CONTROLLER ERROR SOURCE REGISTER (CESR)

BIT NUMBER	REGISTER BITNAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING†	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
23	CCMM	0ECCMM0	B10/F8	1ECCMM0	B23/F8	Cross-controller mismatch (Detected on the GRAM [UN352] circuit pack) (This error asserts an AINT/ASWF†; a fault on the mate controller can also trigger this error)	UN350 UN351 UN352 KCN3 KCN3	045-112 045-072 045-088 045-048 045-056	053-112 053-072 053-088 053-048 053-056

* SCU x is the Service Circuit Unit in which the fault was detected, where x is the value of the contents of the Extended Bus Address Register. A TSI fault can also trigger this error. The KCN3 in position 48 interfaces with SCUs 0—7; whereas, the KCN3 in position 56 interfaces with SCUs 8—15.

† AINT/ASWF — AINT (Autonomous Interrupt) is generated by the error if no peripheral unit order is being processed; whereas, all-seems-well failure (ASWF) occurs if the error is triggered during order processing.

TABLE C
EXTENDED BUS LINK STATUS REGISTER LOW (EBLKSTATL)
(32 bit register – upper 8 bits are listed in EBLKSTATH)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION*	CONTR 1 LOCATION*
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ICRSCU	None		None		Illegal command received by the SCU	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
1	RPESCU	None		None		SCU receive link parity error	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
2	RFESCU	None		None		SCU receive link frame error	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
3	SPARE3	None		None		Spare bit (NOT USED)			
4	RFFSCU	None		None		SCU receive fifo full (NO ERROR)			
5	RFHFSCU	None		None		SCU receive fifo half full (NO ERROR)			
6	TFNESCU	None		None		SCU transmit fifo not empty (NO ERROR)			
7	ERRSUM	None		None		SCU error summary bit	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
8	TSA	None		None		Transmit sequencer active (NO ERROR)			
9-14	TSEQS	None		None		Transmit sequencer state (NO ERROR)			
15	STATLSSRB	None		None		This bit reflects the state of the Set Status Register Bit (bit 17) of the EBI control register (NO ERROR)			
16	RSA	None		None		Receive sequencer active (NO ERROR)			
17-21	RSEQS	None		None		Receive sequencer state (NO ERROR)			
22	NOC	None		None		Near operation complete (NO ERROR)			
23	EBIOC	None		None		Operation complete sync (NO ERROR)			

* SCU n is the Service Circuit Unit in which the KCN4 is located, where n is the value of the contents of the Extended Bus Address Register. The KCN3 in position 48 interfaces with SCUs 0–7; whereas, the KCN3 in position 56 interfaces with SCUs 8–15.

ANALYZE SCSF, F-LEVEL INTERRUPT

TABLE D
EXTENDED BUS LINK STATUS REGISTER HIGH (EBLKSTATH)
(32 bit register – lower 24 bits are listed in EBLKSTATL)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION*	CONTR 1 LOCATION*
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	ICRSCC	None		None		Illegal command received by the controller	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
1	RLVSCC	None		None		Receive link violation by the controller	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
2	STATHSSRB	None		None		This bit reflects the state of the Set Status Register Bit (bit 17) of the EBI control register (NO ERROR)			
3	DDATPE	None		None		Controller destination data parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088
4	RPE	None		None		Receiver parity error from an EB link	KCN4 KCN3 KCN3	SCU n-024 045-048 045-056	SCU n-024 053-048 053-056
5	SPE	None		None		Controller source address parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088
6	DPE	None		None		Controller destination address parity error (This error asserts the EBSUM flag in the UN350 CESR register)	KCN4 KCN3 UN350 UN351 UN352	045-048 045-056 045-112 045-072 045-088	053-048 053-056 053-112 053-072 053-088

TABLE D (Contd)
EXTENDED BUS LINK STATUS REGISTER HIGH (EBLKSTATH)
(32 bit register – lower 24 bits are listed in EBLKSTATL)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
7	TPE	None		None		Transmit parity error to an EB link (This error asserts the EBSUM flag in the UN350 CESR register)	KCN3 KCN3	045-048 045-056	053-048 053-056

* SCU n is the Service Circuit Unit in which the KCN4 is located, where n is the value of the contents of the Extended Bus Address Register. The KCN3 in position 48 interfaces with SCUs 0–7; whereas, the KCN3 in position 56 interfaces with SCUs 8–15.

TABLE E
GLOBAL RAM ERROR SOURCE REGISTER (GRESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0-3	ERAP	None		None		Ram bank A data parity error bits (These errors assert the GRAMSUM flag in the UN350 CESR register)	UN352	045-088	053-088
4-7	ERBP	None		None		Ram bank B data parity error bits (These errors assert the GRAMSUM flag in the UN350 CESR register)	UN352	045-088	053-088
8-11	EDDP	None		None		Destination bus data parity error bits (These errors assert the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
12	EDAP	None		None		Destination bus address parity error (These errors assert the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
13	ESAAP	None		None		Source bus A address parity error (This error asserts the BPSUM flag in the UN350 CESR register)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
14	ESBAP	None		None		Source bus B address parity error (This error asserts the BPSUM flag in the UN350 CESR register)	UN352 UN351	045-088 045-072	053-088 053-072
15	EXUMM	None		None		Cross-connect update bus mismatch (This error asserts the CCMM flag in the UN350 CESR register; it may be generated due to a mate controller fault)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056

TABLE E (Contd)
GLOBAL RAM ERROR SOURCE REGISTER (GRESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
16	EXSMM	None		None		Cross-connect syndrome bus mismatch (This error asserts a CCMM flag in the UN350 CESR register; it may be generated due to a mate controller fault)	UN352 UN351 UN350 KCN3 KCN3	045-088 045-072 045-112 045-048 045-056	053-088 053-072 053-112 053-048 053-056
17	SPARE17	None		None		(NOT USED)			
18	SPARE18	None		None		(NOT USED)			
19	SPARE19	None		None		(NOT USED)			
20	SPARE20	None		None		(NOT USED)			
21	SPARE21	None		None		(NOT USED)			
22	SPARE22	None		None		(NOT USED)			
23	SPARE23	None		None		(NOT USED)			

TABLE F
EXEC ERROR SOURCE REGISTER (EXESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
0	STKBNDERR	None		None		EXEC stack bounds error (This error asserts the EXECSUM flag in the UN352 CESR register. A firmware bug may cause this error)	UN351	045-072	053-072
1	SANITYTMR	None		None		Sanity timer elapsed (This error asserts the EXECSUM flag in the UN352 CESR register. A firmware bug may cause this error)	UN351	045-072	053-072
2	ALUMM	None		None		ALU mismatch*	UN351	045-072	053-072
3	MALUPERR	None		None		Source A or B data parity error*	UN351 UN352 UN350 KCN3 KCN3	045-072 045-088 045-112 045-048 045-056	053-072 053-088 053-112 053-048 053-056
4	SPARE4	None		None		(NOT USED)			
5	MPERR0	None		None		Microword parity error (byte 0)*	UN351	045-072	053-072
6	MPERR1	None		None		Microword parity error (byte 1)*	UN351	045-072	053-072
7	MPERR2	None		None		Microword parity error (byte 2)*	UN351	045-072	053-072
8	MPERR3	None		None		Microword parity error (byte 3)*	UN351	045-072	053-072
9	MPERR4	None		None		Microword parity error (byte 4)*	UN351	045-072	053-072
10	MPERR5	None		None		Microword parity error (byte 5)*	UN351	045-072	053-072
11	MPERR6	None		None		Microword parity error (byte 6)*	UN351	045-072	053-072
12	MPERR7	None		None		Microword parity error (byte 7)*	UN351	045-072	053-072
13	SPARE13	None		None		(NOT USED)			
14	SPARE14	None		None		(NOT USED)			
15	SOFTERR	None		None		Software defined error (This error is normally set by software and asserts the EXECSUM flag in the UN352 CESR register)	UN351	045-072	053-072

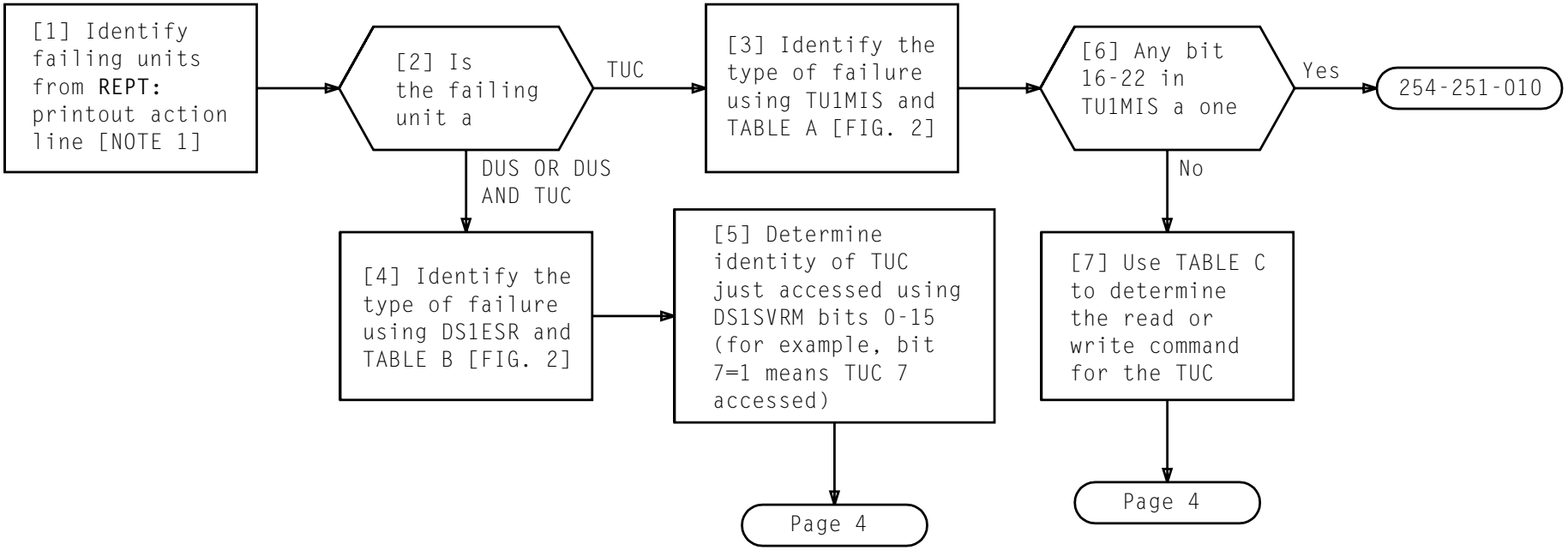
TABLE F (Contd)
EXEC ERROR SOURCE REGISTER (EXESR)

BIT NUMBER	REGISTER BIT NAME	CONTROLLER 0		CONTROLLER 1		BIT MEANING	SUSPECT PACK	CONTR 0 LOCATION	CONTR 1 LOCATION
		FS LEAD	SHT/LOC	FS LEAD	SHT/LOC				
16	CFPEMW0	None		None		Force microword parity error - byte 0 (NO ERROR)			
17	CFPEMW1	None		None		Force microword parity error - byte 1 (NO ERROR)			
18	CFPEMW2	None		None		Force microword parity error - byte 2 (NO ERROR)			
19	CFPEMW3	None		None		Force microword parity error - byte 3 (NO ERROR)			
20	CFPEMW4	None		None		Force microword parity error - byte 4 (NO ERROR)			
21	CFPEMW5	None		None		Force microword parity error - byte 5 (NO ERROR)			
22	CFPEMW6	None		None		Force microword parity error - byte 6 (NO ERROR)			
23	CFPEMW7	None		None		Force microword parity error - byte 7 (NO ERROR)			

* These errors assert the EXECSUM flag in the UN352 CESR register.

SUMMARY

This type of failure is due to either a CC read or write of an internal DUS location or a write of an internal TUC register location. When CC writes into an internal TUC location, the write data is looped back to the DUSOBR. When CC reads an internal TUC location, the TUC read data (for that read operation) is gated into the DUSOBR. In order to verify data written into a TUC or to obtain data read from a TUC, CC must perform a read of the DUSOBR. Most often, the DUS-TUC communication portion of the CC-TUC read/write operation fails, causing the DUS to freeze. When this happens, the CC read of the DUSOBR to obtain TUC read or write data also fails because the DUS is frozen. This produces the D-Level interrupt.



DATA: D-LEVEL

```
IN1FR  IN1GR  IN1JR  IN1KR  IN1LR  IN1XR
IN1YR  IN1ZR  IN1BR  IN1CAR IN1ILA IN1SCA
IN1SDA IN1SPA IN1CSC IN1INS IN1INH IN1SC
IN1SR  IN1INJ IN1CES ST1CES
```

FIG. 1 — Part of D-Level Printout

NOTE 1

ADDRESS where interrupt occurred is in IN1CAR. DUS/TUC address being read or written that caused the interrupt is in IN1SDA [FIG. 1]

ANALYZE D-LEVEL DUS/TUC INTERRUPT

DATA: INTERNAL DUS REGISTERS AND TEST RESULTS

DS1OBR	DS1IBR	DS1OAR	DS1IRA	DS1SELREG	DS1SVRM
DS1OIRA	DS1MCR	DS1PCR	DS1ESR	GCPA	GCPR
DS1R_TFWRD	DS1R_TADDR	DS1R_TVCTR	DS1R_TRSLT	DS1R_XFRWD0	DS1R_SVR1
DS1R_TFWRDB	DS1R_TADDRB	DS1R_TVCTRB	DS1R_TRSLTB	DS1R_XFRWD1	DS1R_SVR2
DS1ROVSTAT+0	DS1RSTAT0+0	DS1RSTAT0+1	DS1RSTAT1+0	DS1RSTAT1+1	DS1R_SVR3
DC1RSTAT0+0	DC1RSTAT0+1	DC1RSTAT0+2	DC1RSTAT0+3	DC1RSTAT0+4	DC1RSTAT0+5
DC1RSTAT0+6	DC1RSTAT0+7	DC1RSTAT0+8	DC1RSTAT0+9	DC1RSTAT0+10	DC1RSTAT0+11
DC1RSTAT0+12	DC1RSTAT0+13	DC1RSTAT0+14	DC1RSTAT0+15	AU1RSTAT+12	AU1RSTAT+13
DC1RSTAT0+0*	DC1RSTAT0+1*	DC1RSTAT0+2*	DC1RSTAT0+3*	AU1STAT0+4*	AU1STAT0+5*
DC1RSTAT0+6*	DC1RSTAT0+7*	DC1RSTAT0+8*	DC1RSTAT0+9*	DC1RSTAT0+10*	DC1RSTAT0+11*
DC1RSTAT0+12*	DC1RSTAT0+13*	DC1RSTAT0+14*	DC1RSTAT0+15*	AU1RSTAT+12*	AU1RSTAT+13*
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee	ffffffff
gggggggg	hhhhhhhh	iiiiiiii	jjjjjjjj	kkkkkkkk	mmmmmmmm
nnnnnnnn	pppppppp	qqqqqqqq	rrrrrrrr	XR	XR
TU1AREG	TU1DR	TU1CCREG	TU1DBR	TU1COM	TU1PCREG
TU1MR	TU1CBREG	ssssssss	tttttttt	TU1MIS	TU1OIS
TU1TTS	uuuuuuuu	TU1CIBG	TU1HLSB		

WORD	BITS 23-12	BITS 11-0
aaaaaaaa	DC1RSTAT2+0	DC1RSTAT1+0
bbbbbbbb	+1	+1
cccccccc	+2	+2
dddddddd	+3	+3
eeeeeeee	+4	+4
ffffffff	+5	+5
gggggggg	+6	+6
hhhhhhhh	+7	+7
iiiiiiii	+8	+8

WORD	BITS 23-12	BITS 11-0
jjjjjjjj	DC1RSTAT2+9	DC1RSTAT1+9
kkkkkkkk	+10	+10
mmmmmmmm	+11	+11
nnnnnnnn	+12	+12
pppppppp	+13	+13
qqqqqqqq	+14	+14
rrrrrrrr	+15	+15
ssssssss	TU1ECREG	TU1WDREG
tttttttt	TU1RCRCREG	TU1WCRCREG

WORD	BITS 23-18	BITS 17-0
uuuuuuuu	TU1SRR	TU1LTCR

* NOT ALWAYS AVAILABLE FOR PRINT

FIG. 2 – Part of D-Level Printout

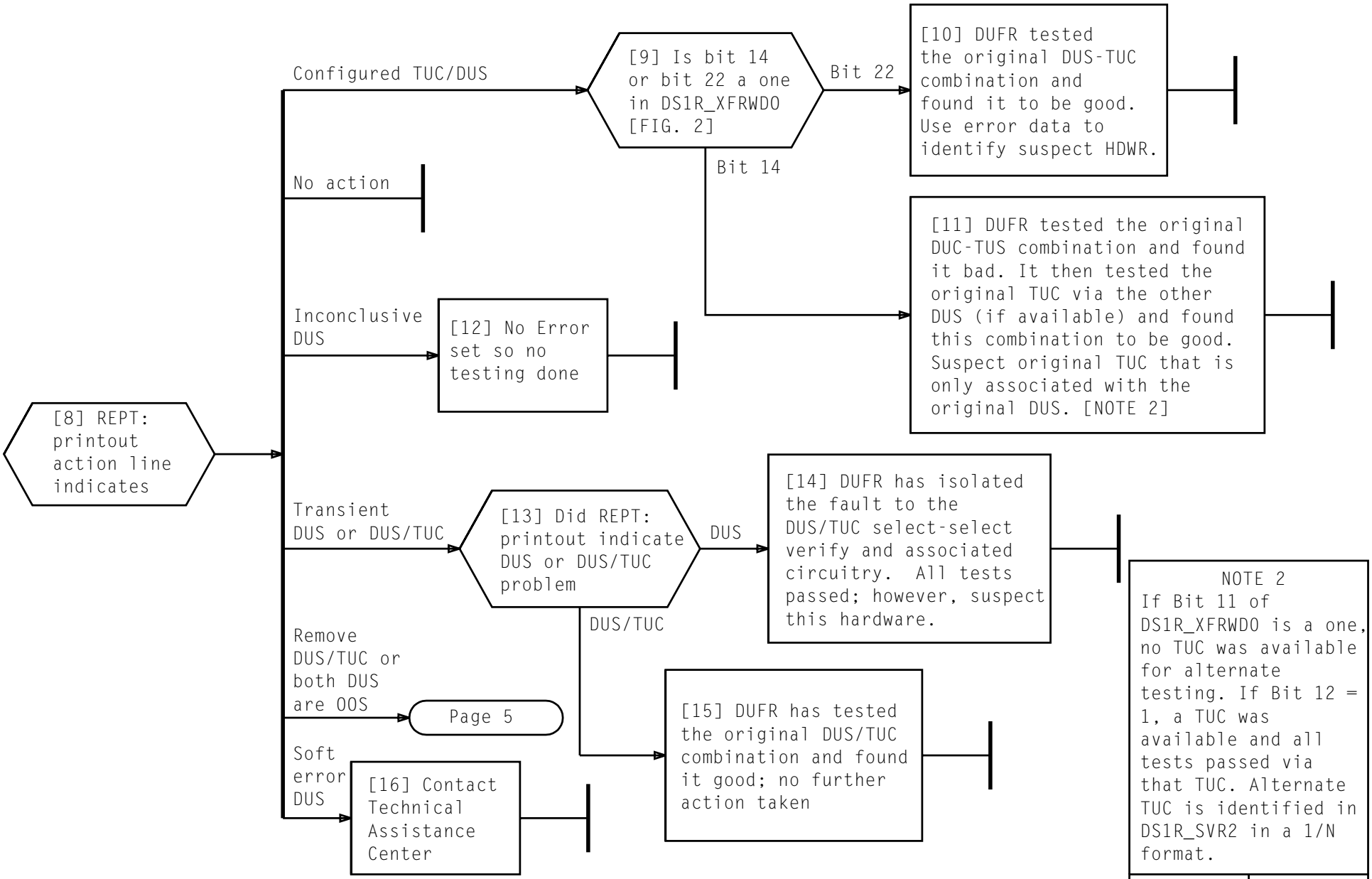
TABLE A — TU1MIS	
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY TUC
0	CLOCK SYNC FAILURE
1	ADDRESS PARITY FAILURE
2	R/W REGISTER SELECT FAILURE
3	DATA PARITY FAILURE
8	INCREMENT PARITY FAILURE
9	SELF-CHECK FAILURE
10	DATA XFER PARITY FAILURE
11	BUFFER PARITY FAILURE ON WRITE
12	AUTONOMOUS REGISTER SELECT FAILURE
13	TIME OUT
14	LATE DATA
15	DATA OVERWRITE
16	ERASE-WRITE HEAD CURRENT FAILURE
17	CAPSTAN MOTION ABNORMAL
18	DC POWER FAILURE
19	AC POWER FAILURE
20	TAPE ARMS ABNORMAL
21	SERVO LAMP FAILURE
22	TEMPERATURE ABNORMAL

TABLE B — DS1ESR*			
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY DUS	LEAD NAME	FS
0	DUC SEQUENCER ERROR	DUCSER	3/1
1	CS/PS SEQUENCER ERROR	SSQER	3/1
6	MODE ERROR READ ONLY	MEO	2/3
9	IBR PARITY FAIL CS/PS	PEO	2/3
10	CS/PS ASW ERROR	SASWE	3/1
12	DUC REPLY BUS PARITY FAILURE	AUCRPER	3/1
13	DUC REPLY BUS ASW FAILURE	AUCBASWO	3/1
14	DUC CONTROL BUS PARITY FAILURE	AUCCPER	3/1
18	DUC SELECT VERIFY FAILURE	AUCSVER	3/1
19	DUC MI REPLY	AUCBMI	3/1

* DS1ESR = 00070000 indicates a complete loss of communication to the TUC. Check TU1HLSB [FIG. 1] bits 1 and 2 for possible cause (TBL FF SET or improper bus routing).

TABLE C		
TU1COM	FUNCTION	REGISTER RESULT
BIT 10 = 1	READ	DUS OUTPUT ADDRESS REGISTER (DS1OAR) SHOULD EQUAL THE TUC ADDRESS REGISTER (TU1AREG) AFTER READING THE TUC ADDRESS REGISTER. ALSO, THE DUS OUTPUT BUFFER REGISTER (DS1OBA) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER READING THE TUC DATA REGISTER.
BIT 2 = 1	WRITE	DUS INPUT BUFFER REGISTER (DS1IBR) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER WRITING THE TUC DATA REGISTER.

ANALYZE D-LEVEL DUS/TUC INTERRUPT



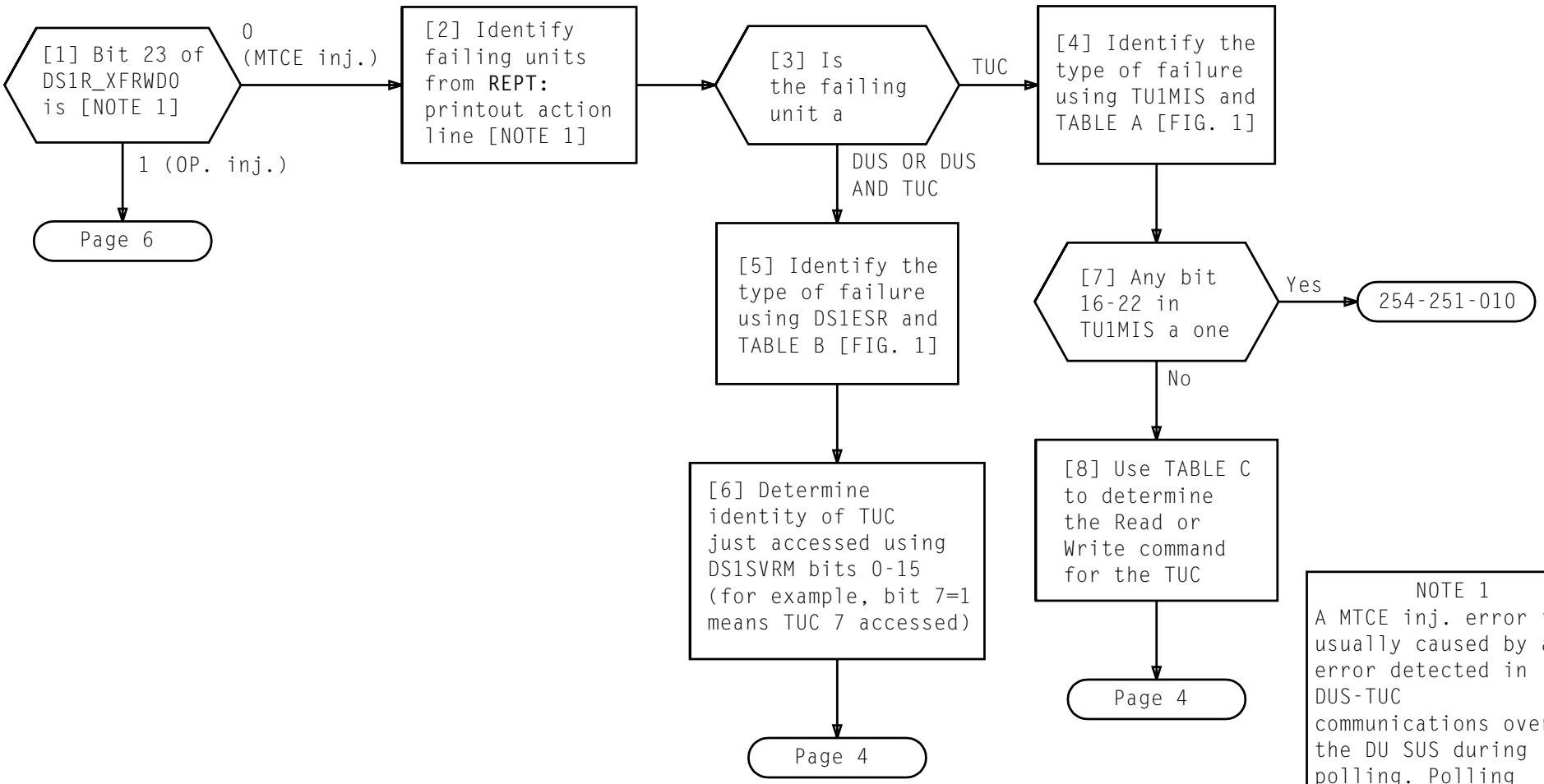
NOTE 2

If Bit 11 of DS1R_XFRWDO is a one, no TUC was available for alternate testing. If Bit 12 = 1, a TUC was available and all tests passed via that TUC. Alternate TUC is identified in DS1R_SVR2 in a 1/N format.

ANALYZE D-LEVEL DUS/TUC INTERRUPT

[17] Identify suspect unit using DS1R_XFRWDO [FIG. 2] and TABLE D

TABLE D — DS1R_XFRWDO	
BIT SET TO ONE	**SUSPECT UNIT/CONDITION**
0	SUSPECT DUS
1	SUSPECT TUC FOR DUS REMOVAL
2	BOTH DUS' SUSPECTED FOR TUC REMOVAL
4	ONE DUS THEN THE OTHER DUS FAILED SAME DUFR TEST
5	ONE DUS THEN THE OTHER DUS FAILED A DIFFERENT DUFR TEST
6	TUC CANNOT COMMUNICATE VIA THE OTHER DUS
9	SUSPECT TUC. OTHER DUS IS AVAILABLE BUT TUC FAILS DUFR
10	SUSPECT DUS. FAILED DUFR TEST VIA A TUC
13	SUSPECT DUS. FAILED VIA TWO DIFFERENT DUCs
15	SUSPECT TUC. FAILS DUFR TEST VIA DUS TO TUC
17	SUSPECT DUS. TEST PASS VIA EACH TUC
19	SUSPECT TUC. TEST PASS VIA EACH DUS
20	SUSPECT TUC. CANNOT SWITCH TO OTHER DUS BECAUSE OF PREVIOUS TROUBLE — RECORD
21	SUSPECT TUC. OTHER DUS NOT AVAILABLE



NOTE 1

A MTCE inj. error is usually caused by an error detected in DUS-TUC communications over the DU SUS during polling. Polling involves reading the TUC address register and/or writing the TUC data register. An operational interject indicates the failure is internal to the TUC.

ANALYZE DUS/TUC INTERJECT

DATA: INTERNAL DUS REGISTERS AND TEST RESULTS

DS1OBR	DS1IBR	DS1OAR	DS1IRA	DS1SELREG	DS1SVRM
DS1OIRA	DS1MCR	DS1PCR	DS1ESR	GCPA	GCPR
DS1R_TFWRD	DS1R_TADDR	DS1R_TVCTR	DS1R_TRSLT	DS1R_XFRWD0	DS1R_SVR1
DS1R_TFWRDB	DS1R_TADDRB	DS1R_TVCTRB	DS1R_TRSLTB	DS1R_XFRWD1	DS1R_SVR2
DS1ROVSTAT+0	DS1RSTAT0+0	DS1RSTAT0+1	DS1RSTAT1+0	DS1RSTAT1+1	DS1R_SVR3
DC1RSTAT0+0	DC1RSTAT0+1	DC1RSTAT0+2	DC1RSTAT0+3	DC1RSTAT0+4	DC1RSTAT0+5
DC1RSTAT0+6	DC1RSTAT0+7	DC1RSTAT0+8	DC1RSTAT0+9	DC1RSTAT0+10	DC1RSTAT0+11
DC1RSTAT0+12	DC1RSTAT0+13	DC1RSTAT0+14	DC1RSTAT0+15	AU1RSTAT+12	AU1RSTAT+13
DC1RSTAT0+0*	DC1RSTAT0+1*	DC1RSTAT0+2*	DC1RSTAT0+3*	AU1STAT0+4*	AU1STAT0+5*
DC1RSTAT0+6*	DC1RSTAT0+7*	DC1RSTAT0+8*	DC1RSTAT0+9*	DC1RSTAT0+10*	DC1RSTAT0+11*
DC1RSTAT0+12*	DC1RSTAT0+13*	DC1RSTAT0+14*	DC1RSTAT0+15*	AU1RSTAT+12*	AU1RSTAT+13*
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee	ffffffff
gggggggg	hhhhhhhh	iiiiiiii	jjjjjjjj	kkkkkkkk	mmmmmmmm
nnnnnnnn	pppppppp	qqqqqqqq	rrrrrrrr	XR	XR
TU1AREG	TU1DR	TU1CCREG	TU1DBR	TU1COM	TU1PCREG
TU1MR	TU1CBREG	ssssssss	tttttttt	TU1MIS	TU1OIS
TU1TTS	uuuuuuuu	TU1CIBG	TU1HLSB		

WORD	BITS 23-12	BITS 11-0
aaaaaaaa	DC1RSTAT2+0	DC1RSTAT1+0
bbbbbbbb	+1	+1
cccccccc	+2	+2
dddddddd	+3	+3
eeeeeeee	+4	+4
ffffffff	+5	+5
gggggggg	+6	+6
hhhhhhhh	+7	+7
iiiiiiii	+8	+8

WORD	BITS 23-12	BITS 11-0
jjjjjjjj	DC1RSTAT2+9	DC1RSTAT1+9
kkkkkkkk	+10	+10
mmmmmmmm	+11	+11
nnnnnnnn	+12	+12
pppppppp	+13	+13
qqqqqqqq	+14	+14
rrrrrrrr	+15	+15
ssssssss	TU1ECREG	TU1WDREG
tttttttt	TU1RCRCREG	TU1WCRCREG

WORD	BITS 23-18	BITS 17-0
uuuuuuuu	TU1SRR	TU1LTCR

* NOT ALWAYS AVAILABLE FOR PRINT

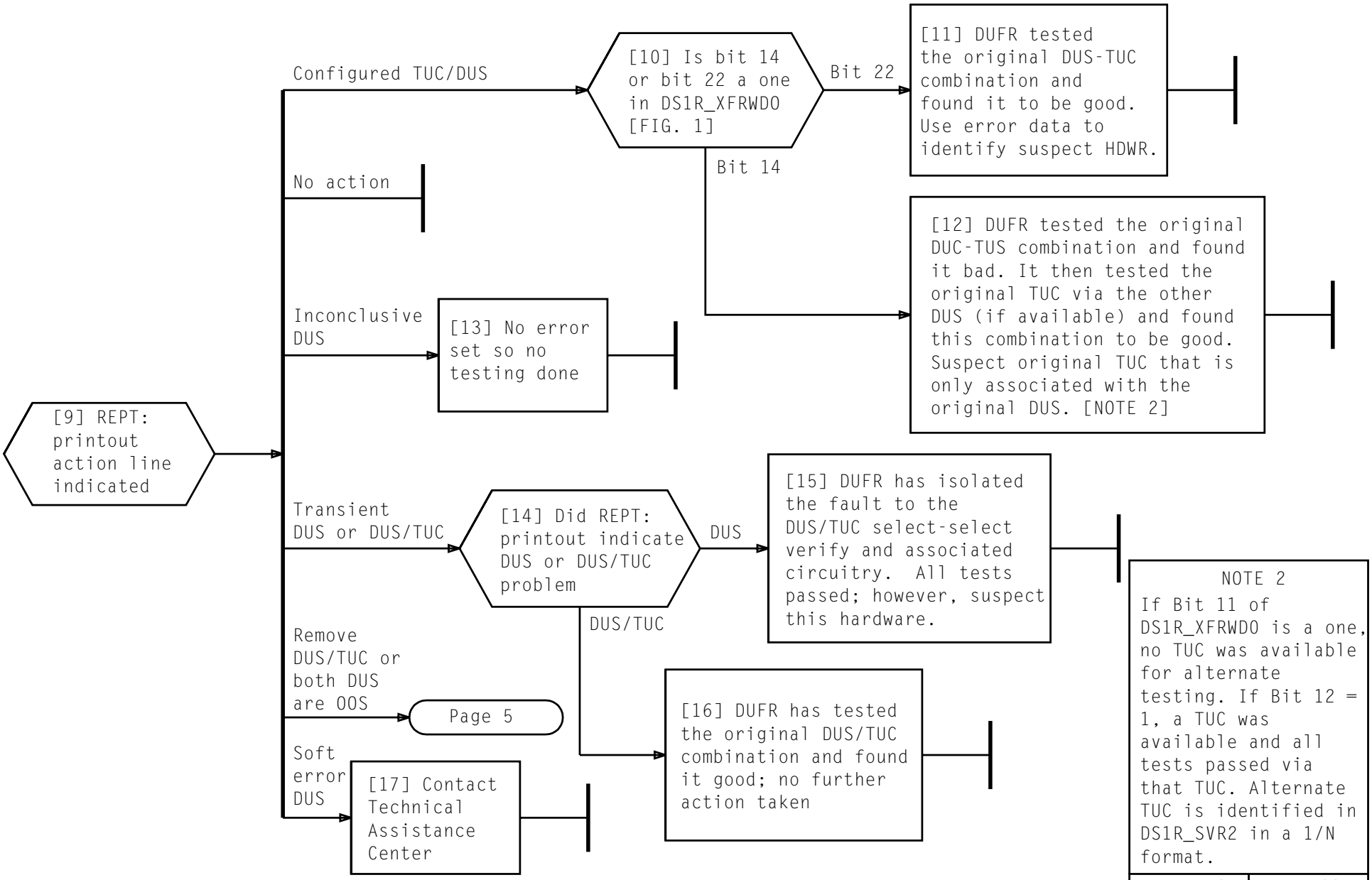
FIG. 1 — Part of Interject Printout

TABLE A — TU1MIS	
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY TUC
0	CLOCK SYNC FAILURE
1	ADDRESS PARITY FAILURE
2	R/W REGISTER SELECT FAILURE
3	DATA PARITY FAILURE
8	INCREMENT PARITY FAILURE
9	SELF-CHECK FAILURE
10	DATA XFER PARITY FAILURE
11	BUFFER PARITY FAILURE ON WRITE
12	AUTONOMOUS REGISTER SELECT FAILURE
13	TIME OUT
14	LATE DATA
15	DATA OVERWRITE
16	ERASE-WRITE HEAD CURRENT FAILURE
17	CAPSTAN MOTION ABNORMAL
18	DC POWER FAILURE
19	AC POWER FAILURE
20	TAPE ARMS ABNORMAL
21	SERVO LAMP FAILURE
22	TEMPERATURE ABNORMAL

TABLE B — DS1ESR*			
BIT SET TO ONE	TYPE OF FAILURE AS SEEN BY DUS	LEAD NAME	FS†
0	DUC SEQUENCER ERROR	DUCSER	3/1
1	CS/PS SEQUENCER ERROR	SSQER	3/1
6	MODE ERROR READ ONLY	MEO	2/3
9	IBR PARITY FAIL CS/PS	PEO	2/3
10	CS/PS ASW ERROR	SASWE	3/1
12	DUC REPLY BUS PARITY FAILURE	AUCRPER	3/1
13	DUC REPLY BUS ASW FAILURE	AUCBASWO	3/1
14	DUC CONTROL BUS PARITY FAILURE	AUCCPER	3/1
18	DUC SELECT VERIFY FAILURE	AUCSVER	3/1
19	DUC MI REPLY	AUCBMI	3/1

* DS1ESR = 00070000 indicates a complete loss of communication to the TUC. Check TU1HLSB [FIG. 1] bits 1 and 2 for possible cause (TBL FF SET or improper bus routing).
† SD5A024

TABLE C		
TU1COM	FUNCTION	REGISTER RESULT
BIT 10 = 1	READ	DUS OUTPUT ADDRESS REGISTER (DS1OAR) SHOULD EQUAL THE TUC ADDRESS REGISTER (TU1AREG) AFTER READING THE TUC ADDRESS REGISTER. ALSO, THE DUS OUTPUT BUFFER REGISTER (DS1OBA) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER READING THE TUC DATA REGISTER.
BIT 2 = 1	WRITE	DUS INPUT BUFFER REGISTER (DS1IBR) SHOULD EQUAL THE TUC DATA REGISTER (TU1DR) AFTER WRITING THE TUC DATA REGISTER.



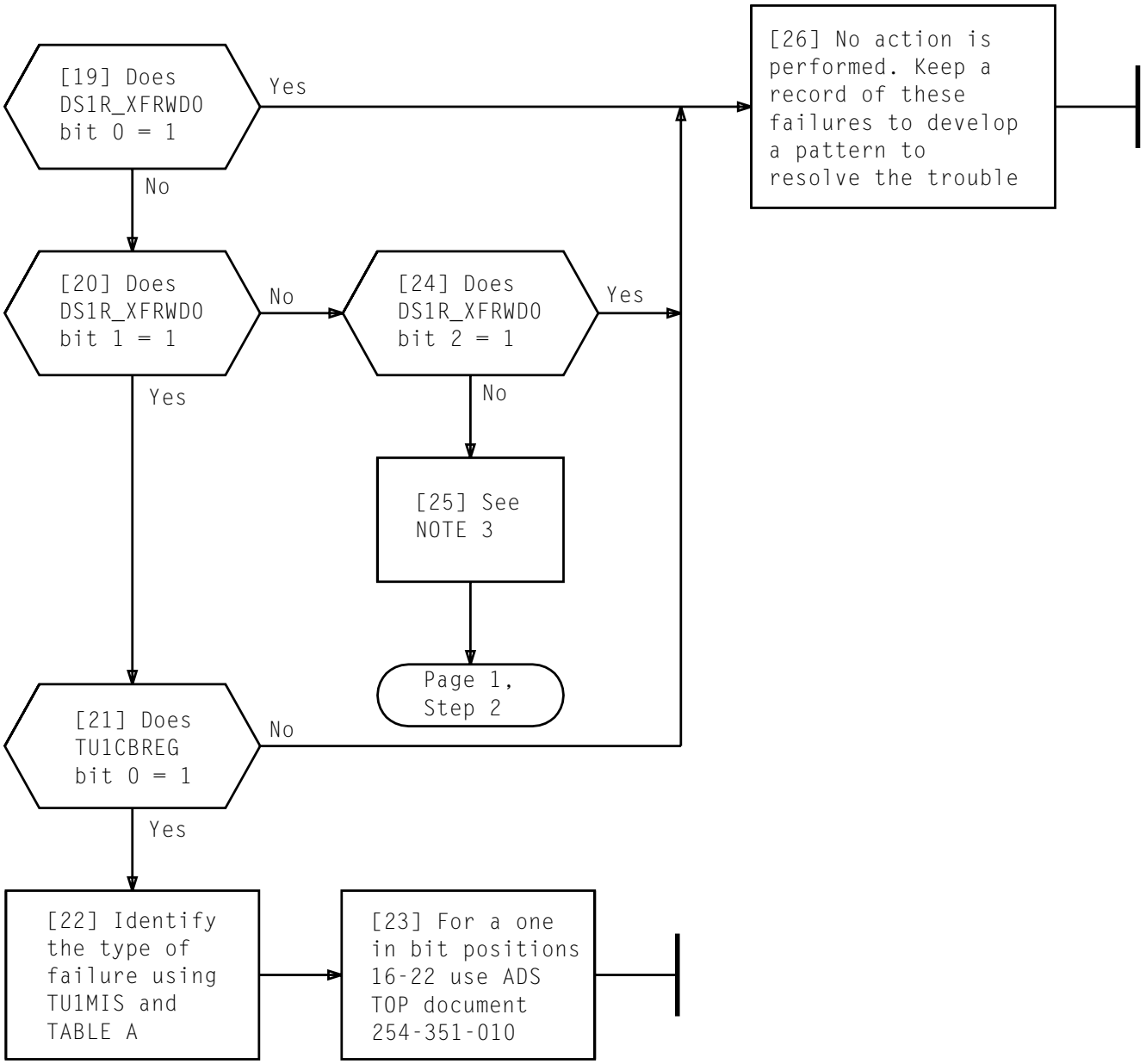
NOTE 2

If Bit 11 of DS1R_XFRWDO is a one, no TUC was available for alternate testing. If Bit 12 = 1, a TUC was available and all tests passed via that TUC. Alternate TUC is identified in DS1R_SVR2 in a 1/N format.

ANALYZE DUS/TUC INTERJECT

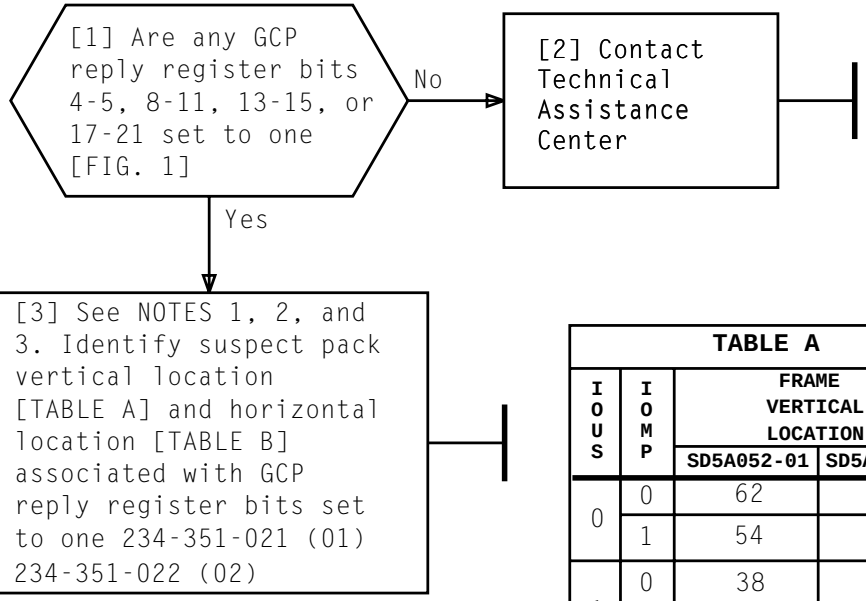
[18] Identify suspect unit using DS1R_XFRWDO [FIG. 1] and and TABLE D

TABLE D — DS1R_XFRWDO	
BIT SET TO ONE	**SUSPECT UNIT/CONDITION**
0	SUSPECT DUS
1	SUSPECT TUC FOR DUS REMOVAL
2	BOTH DUS' SUSPECTED FOR TUC REMOVAL
4	ONE DUS THEN THE OTHER DUS FAILED SAME DUFR TEST
5	ONE DUS THEN THE OTHER DUS FAILED A DIFFERENT DUFR TEST
6	TUC CANNOT COMMUNICATE VIA THE OTHER DUS
9	SUSPECT TUC. OTHER DUS IS AVAILABLE BUT TUC FAILS DUFR
10	SUSPECT DUS. FAILED DUFR TEST VIA A TUC
13	SUSPECT DUS. FAILED VIA TWO DIFFERENT DUCs
15	SUSPECT TUC. FAILS DUFR TEST VIA DUS TO TUC
17	SUSPECT DUS. TEST PASS VIA EACH TUC
19	SUSPECT TUC. TEST PASS VIA EACH DUS
20	SUSPECT TUC. CANNOT SWITCH TO OTHER DUS BECAUSE OF PREVIOUS TROUBLE — RECORD
21	SUSPECT TUC. OTHER DUS NOT AVAILABLE



NOTE 3
The Data Unit Administration Program has detected:
- a) an unsuccessful job completion
- b) some other non-interruptable operational malfunction
- c) a hardware consistency check failure
- d) a hardware/ software consistency check failure

ANALYZE DUS/TUC INTERJECT



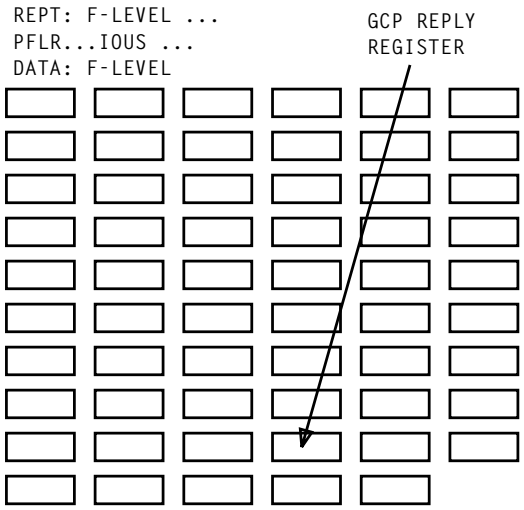


FIG. 1 — Part of Interrupt Printout

TABLE A

IOUS	IOMP	FRAME VERTICAL LOCATION	
		SD5A052-01	SD5A052-02
0	0	62	62
	1	54	54
1	0	38	32
	1	30	24
2	0	62	62
	1	54	54
3	0	38	32
	1	30	24
4	0	62	62
	1	54	54
5	0	38	32
	1	30	24
6	0	62	62
	1	54	54
7	0	38	32
	1	30	24

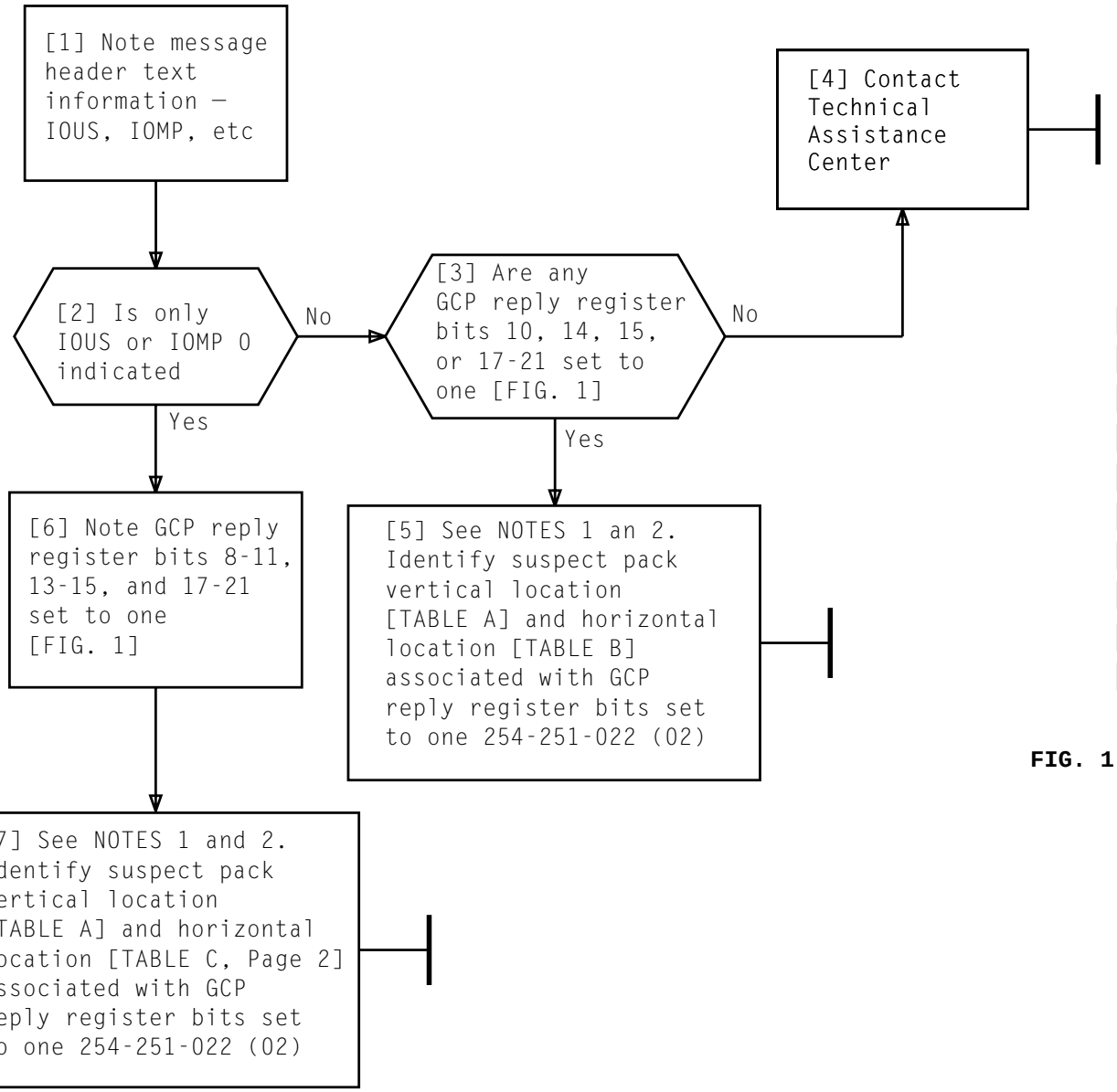
TABLE B
GCP REPLY REGISTER

GCP BIT	SUSPECT EQUIPMENT		
	TYPE	HORIZONTAL LOCATION	COMMENTS
4,5	**FG23**	35	—
	FG41	24	—
	FG25	39	—
	136H	08	Power unit*
	235A	02	Power unit
8,9	**FG41**	24	—
	FG44	28	May be **FG87**
10,11	**FG20**	22	—
	FG43	31	May be **FG86**
13,14	**FG44**	28	May be **FG87**
	FG22	26	—
15	**FG20**	22	—
	FG22	26	—
17	**FG44**	28	May be **FG87**
	FG22	26	—
18,19	**FG43**	31	May be **FG86**
	FG44	28	May be **FG87**
	FG42	33	May be **FG85**
20	**FG22**	26	—
21	**FG22**	26	—
	FG42	33	May be **FG85**

* Even IOUS — Vert 68
Odd IOUS — Vert 44

NOTES
1. If IOUS only is indicated, assume IOMP 0 for TABLE A use
2. IOUS number on printout is same as IOP number on power switch
3. Notify users that channels are to be removed from service

ANALYZE PFLR F-LEVEL INTERRUPT, IOP FRAME (SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)



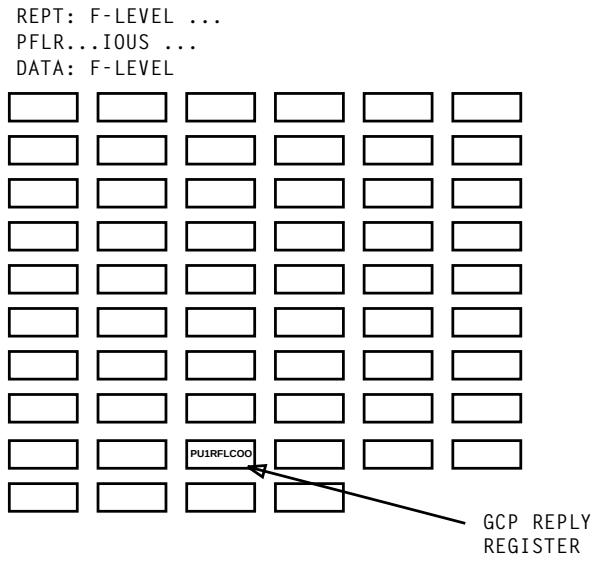


FIG. 1 — Example of Partial Interrupt Printout

NOTES

1. IOUS number on printout is same as IOP number on power switch
2. Notify users that channels are to be removed from service

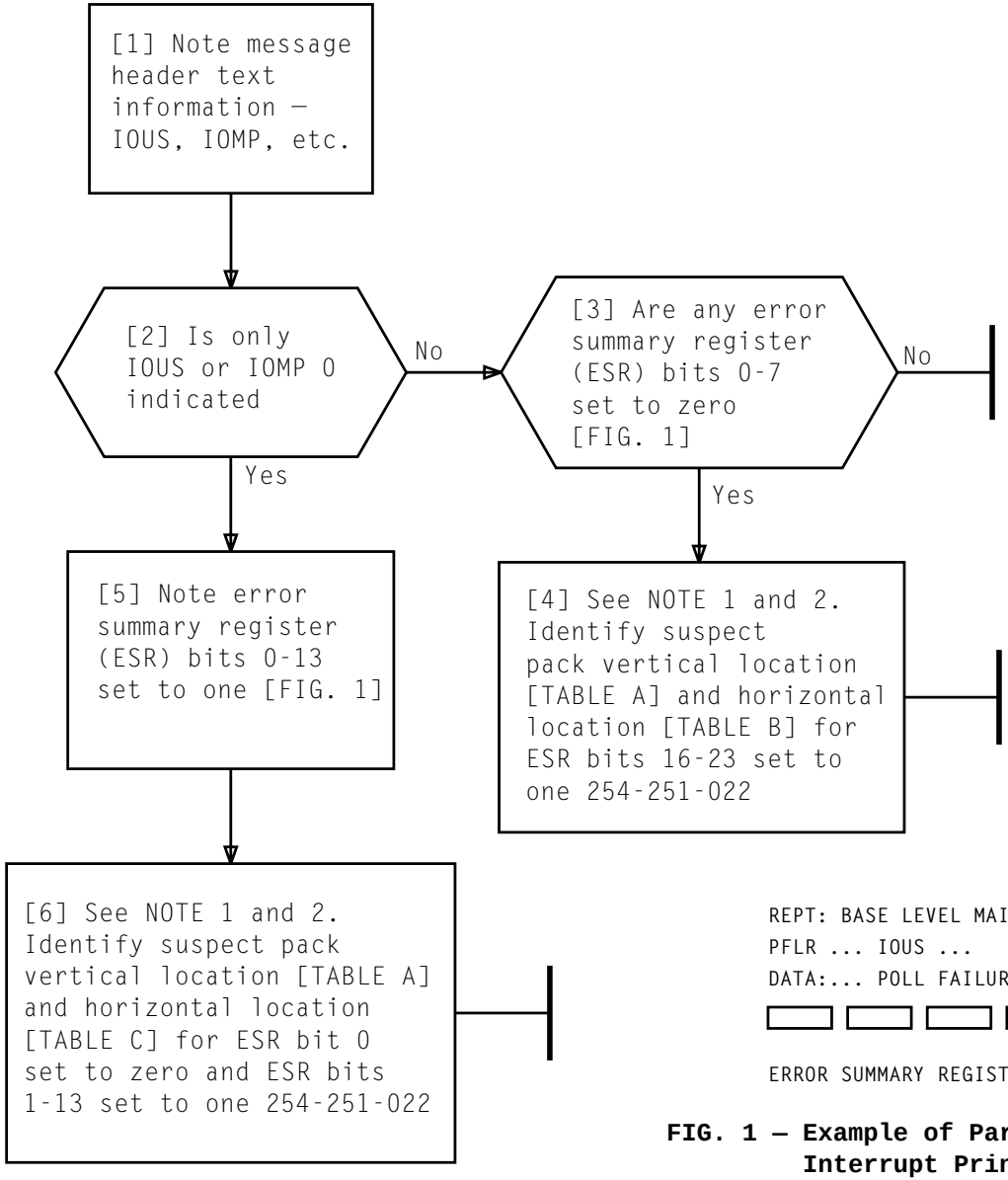
ANALYZE F-LEVEL PFLR INTERRUPT, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

TABLE A		
IOUS	IOMP	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	54
3	0	32
	1	24
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B			
IOMP 1			
GCP BIT	SUSPECT PACK		
	TYPE	HORIZONTAL LOCATION	COMMENTS
10	**UN60**	056	—
	(PC20)*	108	These RC packs are not listed in order of fault probability
	(PC21)*	100	
	(PC22)*	092	
	(PC23)*	084	
	(PC30)*	048	
	(PC31)*	040	
	(PC32)*	032	
	(PC33)*	024	
14	**FG87**	28	At IOMP 0 vertical location
	FG22	26	
15	**FG20**	22	
	FG22	26	
17	**FG87**	28	
	FG22	26	
18,19	**FG86**	31	
	FG87	28	
	FG85	33	
20	**FG22**	26	
21	**FG22**	26	
	FG85	33	
* **TN75, TN75B, TN75C,** or **TN82B** (office dependent)			

TABLE C		
IOMP 0		
GCP BIT	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
8,9	**FG41**	24
	FG87	28
10,11	**FG20**	22
	FG86	31
13,14	**FG87**	28
	FG22	26
15	**FG20**	22
	FG22	26
17	**FG87**	28
	FG22	26
18,19	**FG86**	31
	FG87	28
	FG85	33
20	**FG22**	26
21	**FG22**	26
	FG85	33

ANALYZE F-LEVEL PFLR INTERRUPT, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)



REPT: BASE LEVEL MAINTENANCE
PFLR ... IOUS ...
DATA:... POLL FAILURE

FIG. 1 — Example of Partial Base Level Interrupt Printout

TABLE A

IOUS	IOMP	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B
IOMP 1

ESR BIT	SUSPECT PACK TYPE	SUSPECT PACK HORIZONTAL LOCATION
16	**(PC20)***	108
	UN60	056
17	**(PC21)***	100
	UN60	056
18	**(PC22)***	092
	UN60	056
19	**(PC23)***	084
	UN60	056
20	**(PC30)***	048
	UN60	056
21	**(PC31)***	040
	UN60	056
22	**(PC32)***	032
	UN60	056
23	**(PC33)***	024
	UN60	056

*** TN75, TN75B, TN75C** or **TN82B** (office dependent)

NOTES
1. IOUS number on printout is same as IOP number on power switch
2. Notify users that channels are to be removed from service

ANALYZE BASE LEVEL PFLR POLL FAILURE, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

TABLE C				
IOMP 0				
ESR BIT		SUSPECT PACK		
POSITION	SET	TYPE	HORIZONTAL LOCATION	COMMENTS
0	No	**FG41**	24	—
1	Yes	**FG41**	24	Pin 5,6 bottom 400-ns square wave
2	Yes	**FG41**	24	—
3	Yes	**FG21**	18	
		FG41	24	
4	Yes	**FG20**	22	
		FG41	24	
		FG22	26	
5,6	Yes	**FG41**	24	
7	Yes	*	14	Line unit packs not listed in order of fault probability
		*	12P	
		*	11	
		*	09P	
		*	08	
		*	06P	
		*	05	
		*	03P	
8-13	Yes	**FG86**	31	—
		FG87	28	
		FG22	26	
		FG23	35	
		FG85	33	
* **FG19, FG26,** or **FG27**				

ANALYZE BASE LEVEL PFLR POLL FAILURE, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

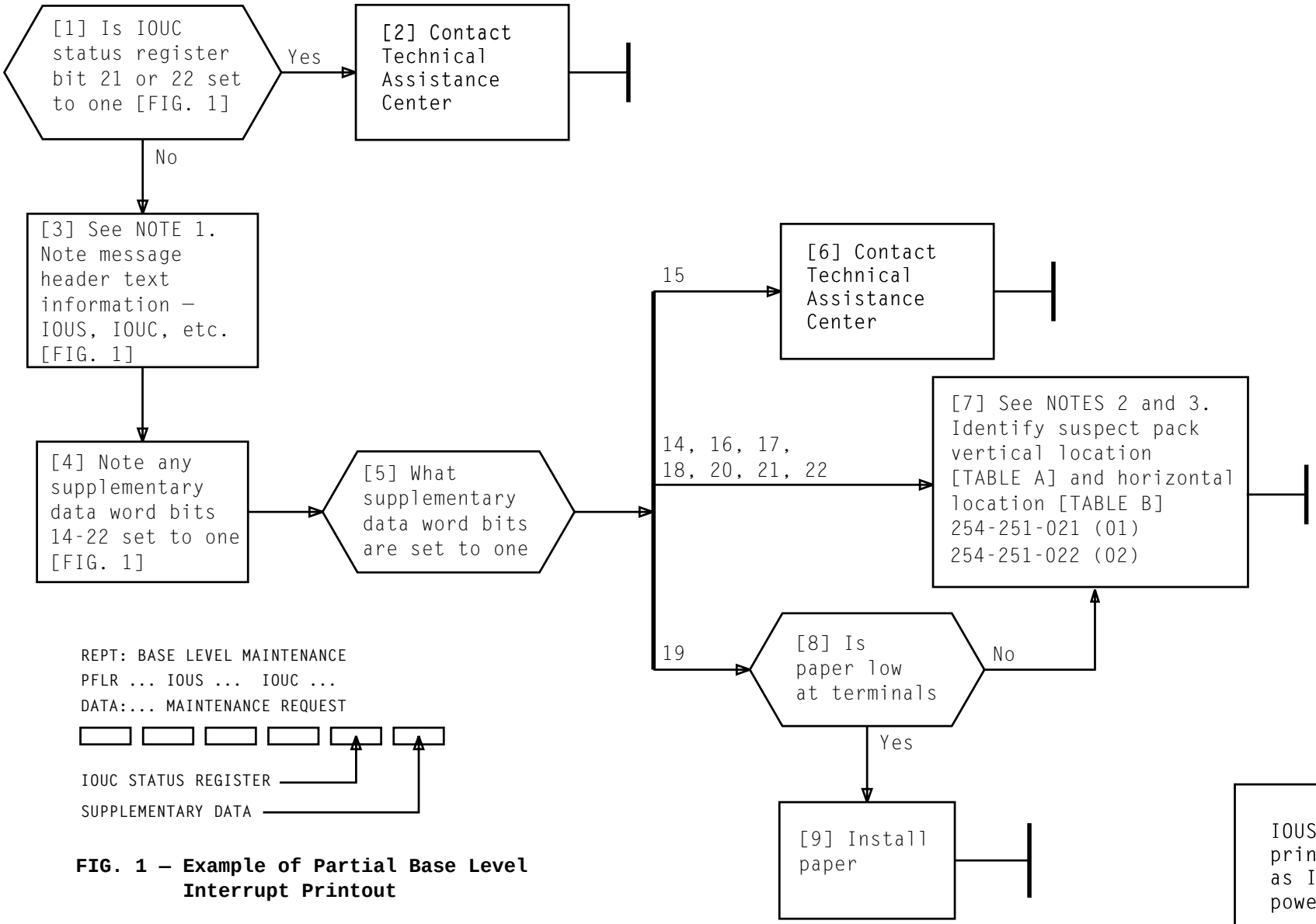


FIG. 1 — Example of Partial Base Level Interrupt Printout

NOTE 1
IOUS number on printout is same as IOP number on power switch

ANALYZE BASE LEVEL PFLR MTCE REQUEST, IOP FRAME (SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)

TABLE A			
IOUS	IOUC	FRAME VERTICAL LOCATION	
		SD5A052-01	SD5A052-02
0	0-7	62	62
	8-15	50	50
1	0-7	38	32
	8-15	30	20
2	0-7	62	62
	8-15	54	54
3	0-7	38	32
	8-15	30	24
4	0-7	62	62
	8-15	54	54
5	0-7	38	32
	8-15	30	24
6	0-7	62	62
	8-15	54	54
7	0-7	38	32
	8-15	30	24

TABLE B		
IOUC	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
0, 8	*	14
1, 9	*	12P
2, 10	*	11
3, 11	*	09P
4, 12	*	08
5, 13	*	06P
6, 14	*	05
7, 15	*	03P
* **FG19**, **FG26**, or **FG27**		

TABLE C	
SUSPECT PACKS	
TYPE	HORIZONTAL LOCATION
FG20	22
FG41	24

NOTE

3. If interrupt recurs after replacing most suspect pack and the supplementary data word bit 17 and 18 are zero, suspect IOUC terminal equipment or terminal cabling. If 17 or 18 set to one suspect packs using TABLE A and C.

ANALYZE BASE LEVEL PFLR MTCE REQUEST, IOP FRAME (SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)

[1] Identify error summary register (ESR) bits 0-13 set to one [FIG. 1]

[2] See NOTES 1 and 2. Identify suspect pack vertical location [TABLE A] and horizontal location [TABLE B] for ESR bit 0 set to zero and ESR bits 1-13 set to one
254-251-021 (01)
254-251-022 (02)

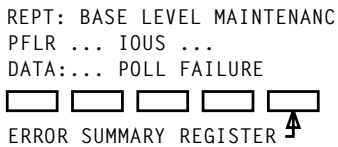


FIG. 1 — Example of Partial Base Level Interrupt Printout

NOTES
1. If IOUS only is indicated on printout, IOMP 0 should be assumed for TABLE A use. IOUS number on printout is same as IOP number on power switch
2. Users should be notified that channels are to be removed from service

ANALYZE BASE LEVEL PFLR POLL FAILURE IOP FRAME (SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)

TABLE A

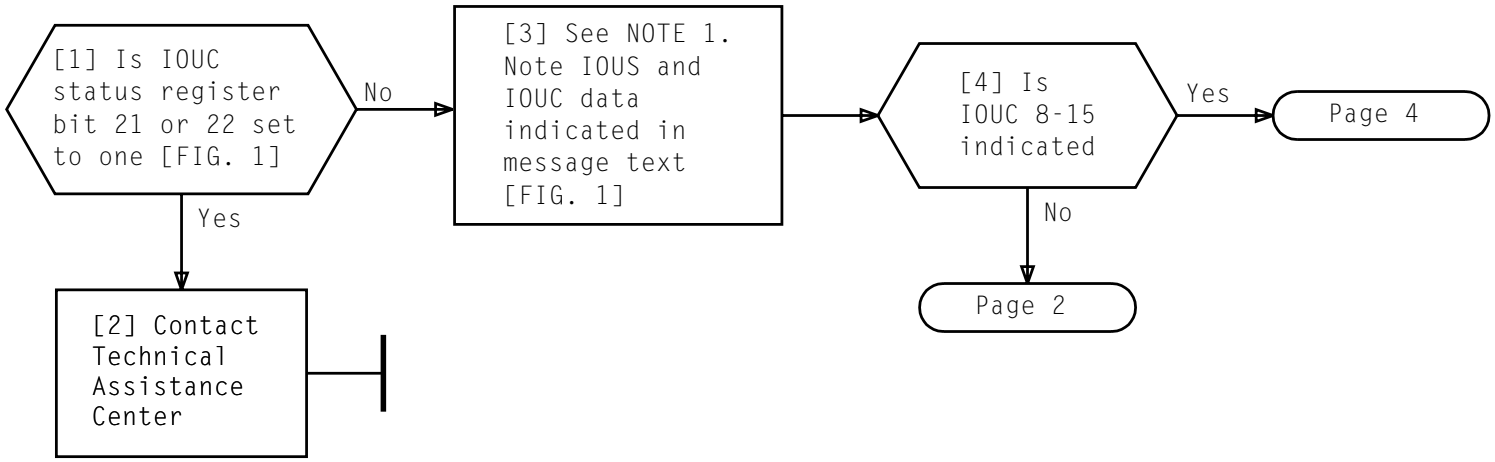
IOUS	IOMP	FRAME VERTICAL LOCATION	
		SD5A052-01	SD5A052-02
0	0	62	62
	1	54	54
1	0	38	32
	1	30	24
2	0	62	62
	1	54	54
3	0	38	32
	1	30	24
4	0	62	62
	1	54	54
5	0	38	32
	1	30	24
6	0	62	62
	1	54	54
7	0	38	32
	1	30	24

TABLE B

ESR BIT		SUSPECT PACK		
POSITION	SET	TYPE	HORIZONTAL LOCATION	COMMENTS
0	No	**FG41**	24	—
1	Yes	**FG41**	24	Pin 5, 6 bottom 400NS square wave
2	Yes	**FG41**	24	—
3	Yes	**FG21**	18	
		FG41	24	
4	Yes	**FG20**	22	
		FG41	24	
		FG22	26	
5,6	Yes	**FG41**	24	
7	Yes	*	14	Line unit packs not listed in order of fault probability
		*	12P	
		*	11	
		*	09P	
		*	08	
		*	06P	
		*	05	
		*	03P	
8-13	Yes	**FG43**	31	May be **FG86**
		FG44	28	May be **FG87**
		FG22	26	—
		FG23	35	
		FG42	33	May be **FG85**

* **FG19**, **FG26**, or **FG27**

ANALYZE BASE LEVEL PFLR POLL FAILURE, IOP FRAME (SD-5A052-01/02) EQUIPPED WITH 1A GROWTH UNIT (SD-4C049-01)



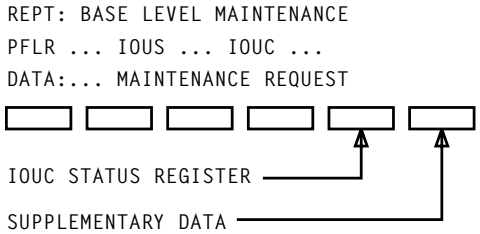
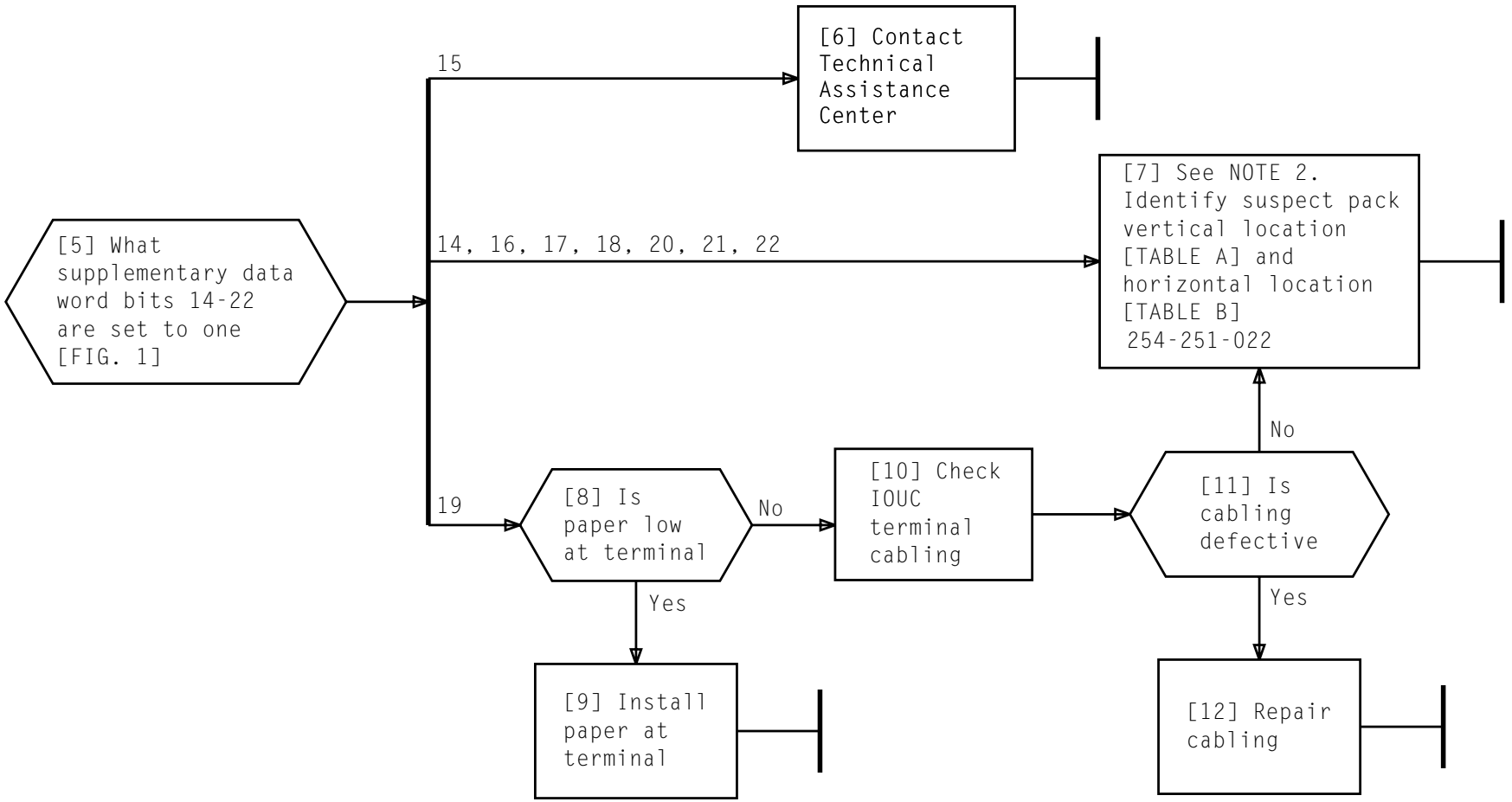


FIG. 1 — Example of Partial Base Level Interrupt Printout

NOTE 1
IOUS number on printout is same as IOP number on power switch

ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)



NOTE 2
Notify users that channels are to be removed from service

ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

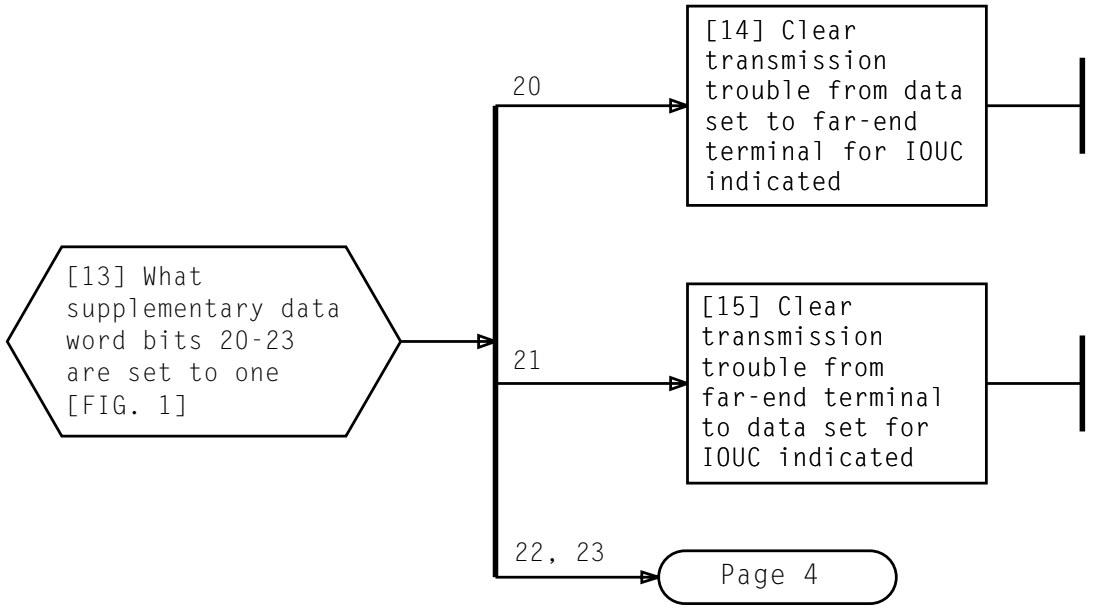


TABLE A

IOUS	IOMP	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE B

IOUC	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
0	*	14
1	*	12P
2	*	11
3	*	09P
4	*	08
5	*	06P
6	*	05
7	*	03P

* **FG19, FG26,** or **FG27**

ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

[16] See NOTES 2 and 3. Identify suspect pack vertical location [TABLE C] and horizontal location [TABLE D] 254-251-022

TABLE C

IOUS	IOMP	VERTICAL LOCATION
0	0	62
	1	50
1	0	32
	1	20
2	0	62
	1	50
3	0	32
	1	20
4	0	62
	1	50
5	0	32
	1	20
6	0	62
	1	50
7	0	32
	1	20

TABLE D

IOUC	SUSPECT PACK	
	TYPE	HORIZONTAL LOCATION
8	**PC20**	108
9	**PC21**	100
10	**PC22**	092
11	**PC23**	084
12	**PC24**	048
13	**PC25**	040
14	**PC26**	032
15	**PC27**	024

NOTE 3
If interrupt recurs after replacing most suspect pack and the supplementary, data word bit 2 is set to one, clear automatic calling unit (ACU) trouble in data set frame of IOUC indicated. If bit 2 is not set to one, check data set associated with indicated IOUC. If data set is OK clear transmission trouble between data set and frame far end.

ANALYZE BASE LEVEL PFLR INTERRUPT MTCE REQUEST, IOP FRAME (SD-5A052-02) EQUIPPED WITH 3B GROWTH UNIT (SD-4C049-02)

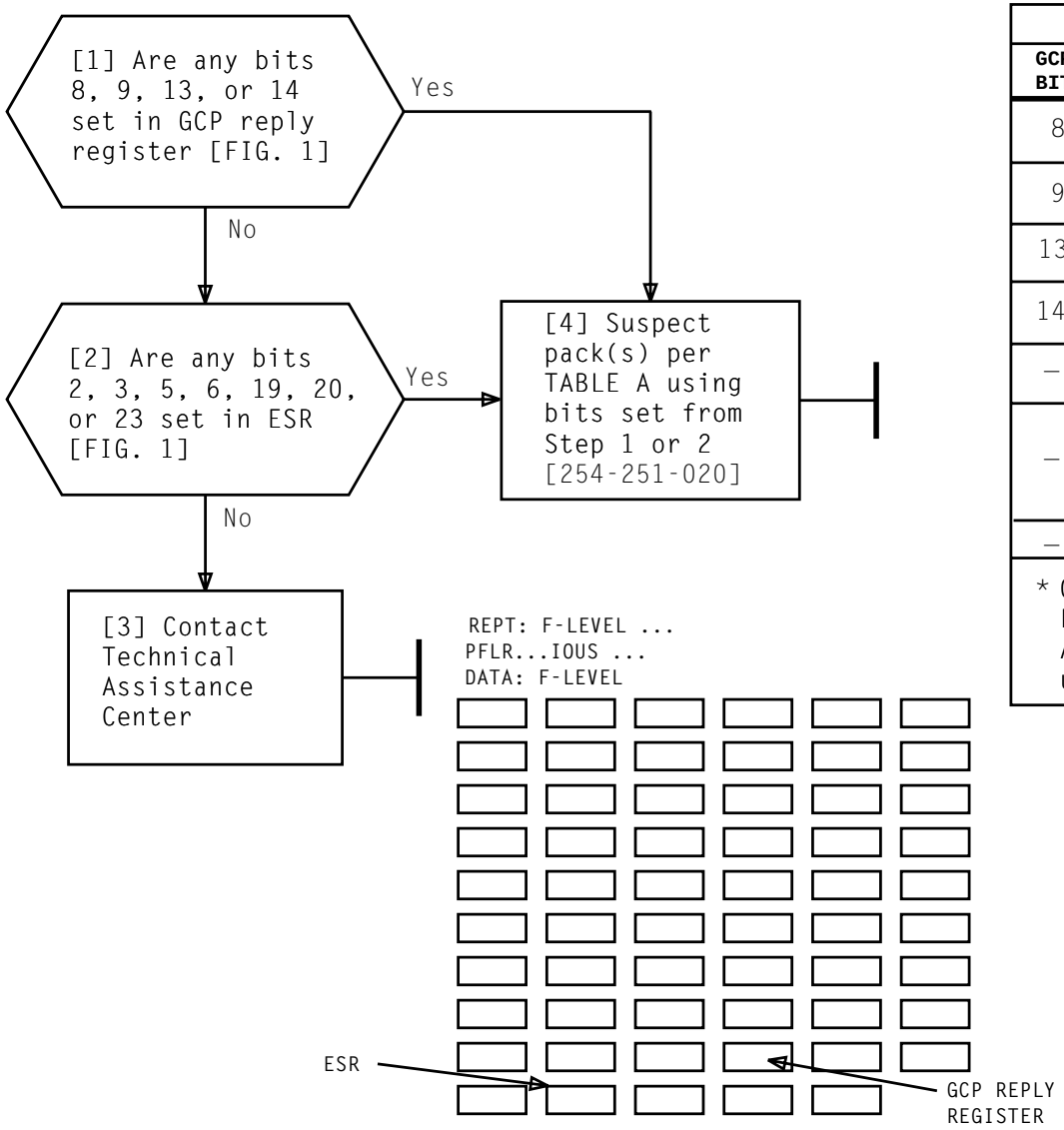


FIG. 1 — Part of Interrupt Printout

TABLE A

GCP BIT	ESR BIT	SUSPECT PACK	UNIT LOC. *	COMMENT
8	2	FA440	06-29	PARITY FAIL EVEN BITS
		FA444	06-22	
9	3	FA440	06-29	PARITY FAIL ODD BITS
		FA444	06-22	
13	5	FA440	06-29	MULTI K-CODE MATCH
		FA444	06-22	
14	6	FA441	06-19	INVALID INSTRUCTION
		FA444	06-22	
—	19	See TABLE B	See TABLE B	CHANNEL RESPONSE FAIL
—	20	FA448	06-27	CHANNEL BUFFER PARITY FAIL
		FA447	06-31	
		FA447	06-14	
		FA447	06-25	
—	23	FA444	06-22	CLOCK FAILURE

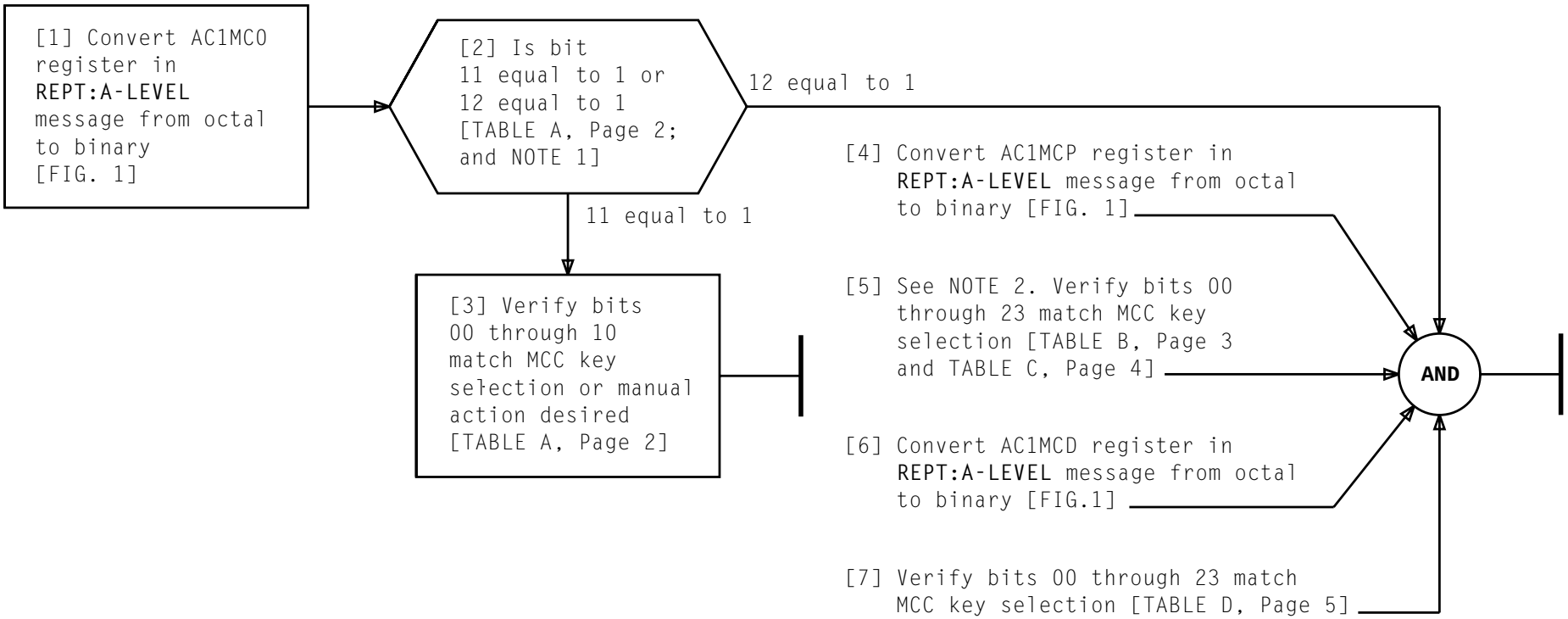
* ODD unit location starts at vertical 18.
Even unit locations starts at vertical 46.
Add unit vertical location given to suspect unit starting location to get frame vertical.

TABLE B

CHANNEL MEMN*	SUSPECT PACK	UNIT LOC.
0	FA453	10-10
1	FA453	06-07
2	FA453	02-10
3	FA453	10-21
4	FA453	02-21
5	FA456	10-35
6	FA453	06-38
7	FA456	02-35

* See REPT: text phrase

ANALYZE PFLR F-LEVEL INTERRUPT OR BASE LEVEL POLL FAILURE, IO FRAME (SD-5A021)




```
A 40 REPT:A-LEVEL @04425643 MFNUM=00002373 MICON=00000021 COMPLETED
     LVDATA=0001 SRDATA=00000000 FRDATA=00000000

      A-LEVEL       ACIMCO    ACIMCP    ACIMCD

     00000011 04173452  00000001 04173453 00000017 00000021
     00075562 00000022  04424650 04425643 00000001 04425642
     00000001 00010000  06000400 00000100
     03/08/77   12:40:24
```

FIG. 1 — Sample A-Level Interrupt Message

NOTES

1. It is possible to have both bits 11 and 12 set to one. This would occur if manual override was in effect when A-level program request was activated
2. When bit 08 equals 1 in the MCP register, MCD register specifies **DIRECT DATA INSERT** key used and corresponding bit in INH register will be set to one

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE A
MCO LAYOUT

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	READ ACCESS INDICATOR	WRITE ACCESS INDICATOR	FS LOCATION	DESCRIPTION	MODIFIED LINES COMPOOL MNEMONIC
MCO		MCO133		D			MCC OVERRIDE REGISTER	MCO
MCCPS0	00	MCO133		R		112	MCC SELECT PROG STORE 0	MCCPS0
MCCRS0	01			R			SELECT ROVER PROG STORE 0	MCCRS0
MCCRS1	02			R			SELECT ROVER PROG STORE 1	MCCRS1
MCCPC	03			R			INHIBIT NORMAL PC TRIGGERS	MCCPC
MCCCC0	04			R			FORCE CC0 ACTIVE	MCCCC0
MCCCC1	05			R			FORCE CC1 ACTIVE	MCCCC1
MCCAUB0	06			R			FORCE AU BUS 0 ACTIVE	MCCAUB0
MCCAUB1	07			R			FORCE AU BUS 1 ACTIVE	MCCAUB1
MCCPSB0	08			R			FORCE PS BUS 0 ACTIVE	MCCPSB0
MCCPSB1	09			R			FORCE PS BUS 1 ACTIVE	MCCPSB1
MCCSR	10			R			FORCE SYSTEM REINITIALIZATION	MCCSR
OVREN	11			R			OVERRIDE ACTIVITY FF	OVREN
PREQ	12			R		112	MCC PROGRAM REQUEST A-LEVEL INTERRUPT	PREQ
	13							
	14							
	15							
	16							
	17							
	18							
	19							
	20							
	21							
	22							
	23	MCO133						

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE B
MCP LAYOUT

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	READ ACCESS INDICATOR	WRITE ACCESS INDICATOR	FS LOCATION	DESCRIPTION	MODIFIED LINES COMPOOL MNEMONIC
MCP		MCP132		C			MCC A-LEVEL PROGRAM REQUEST REG	MCP
MCPR1	00	MCP132		R		112	MCC PROGRAM REQUEST PHASE 1	MCPR1
MCPR2	01			R			2	MCPR2
MCPR3	02			R			3	MCPR3
MCPR4	03			R			4	MCPR4
MCPR5	04			R			3	MCPR5
MCPR6	05			R		112	MCC PROGRAM REQUEST PHASE 3	MCPR6
	06							
	07							
MCINB	08			R		112	MCC INHIBIT INTERRUPT SOURCES SPECIFIED	MCINB
MCUTL	09			R			MCC CLEAR UTILITY MATCH CONDITION	MCUTL
MCPA1	10			R			MIN CFG EMER MODE	MCPA1
MCPA2	11			R			FULL CFG EMER MODE	MCPA2
MCPA3	12			R			MODIFY RECOVERY ACTIONS	MCPA3
MCPA4	13			R			RESTORE MTCE I/O	MCPA4
MCPA5	14			R		112	MCC PROGRAM REQUEST AUX FF 5	MCPA5
	15							
	16							
	17							
	18							
MCCPOFF	19			R		112	POWER OFF IN MCC	MCCPOFF
MCCROS	20			R		112	MCC REQUEST OUT-OF-SERVICE FOR MCC	MCCROS
	21							
MCHAUB0	22			R		112	MCC INHIBIT PC SWITCHING TO AU BUS 0	MCHAUB0
MCHAUB1	23	MCP132		R		112	MCC INHIBIT PC SWITCHING TO AU BUS 1	MCHAUB1
MCHAUB0	22			R		112	NORMAL/UPDATE – APS	MCHAUB0
MCHAUB1	23	MCP132		R		112	FILE SELECTED – APS	MCHAUB1

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE C
INH LAYOUT

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	READ ACCESS INDICATOR	WRITE ACCESS INDICATOR	FS LOCATION	DESCRIPTION		MODIFIED LINES COMPOOL MNEMONIC
INH		INH143	AW				INTERRUPT INHIBIT REG		INH
IJS	00	INH143	RW	095			INHIBIT J-LEVEL INTERRUPT SOURCE		IJS
IHS	01						H		IHS
IIVTGS	02						G	(INTVL TIMER)	IIVTGS
IMGS	03						G	(MATCHER)	IMGS
IAPUFS	04						F	(APU)	IAPUFS
IPUFS	05						F	(PU)	IPUFS
IES	06						E	(PROGRAM STORE)	IES
ISCDS	07						D	(STACK CNTR)	ISCDS
IPADS	08						D	(PROTECT AREA)	IPADS
IAUDS	09						D	(AUX UNIT)	IAUDS
ICSDS	10						D	(CALL STORE)	ICSDS
IPSBS	11						INHIBIT B-LEVEL INTERRUPT SOURCE	(PULSE SOURCE)	IPSBS
ISCUFS	12						INHIBIT SCANNER CONTROL UNIT F LEVEL INT SOURCE		ISCUFS
IORDS	13			RW	095		INHIBIT OUT-OF-RANGE D-LEVEL INT SOURCE		IORDS
	14								
	15								
IWEIPU	16			RW	106		INHIBIT ASW & ENABLE VERIFY FOR CPD ENABLING		IWEIPU
IKLOS	17			RW	095		INHIBIT K-LEVEL INTERRUPT SOURCE		IKLOS
*IKL1S	18						1		IKL1S
*IKL2S	19						2		IKL2S
*IKL3S	20						INHIBIT K-LEVEL 3 INTERRUPT SOURCE		IKL3S
FREZ	21			RW	095		INTERRUPT FREEZE FF		FREZ
IASWEPU	22			RW	106		INHIBIT SET OF ASWEPU FF		IASWEPU
IAPEPU	23	INH143		RW	106		INHIBIT SET OF APEPU FF		IAPEPU

* Always set in 4ESS switch

VERIFY A-LEVEL INTERRUPT REQUEST

TABLE D
MCD LAYOUT (MRA and DDI keys should be verified during a "Hand A")

BIT OR REGISTER MNEMONIC	ACCESS BIT NUMBER	MNEMONIC FOR CC REGISTER OR GROUP	OCTAL ADDRESS (7 LEAST SIGNIFICANT BITS)	READ ACCESS INDICATOR	WRITE ACCESS INDICATOR	FS LOCATION	DESCRIPTION	
MCD		MCD134	C				MCC INPUT DATA REGISTER	APPLICATION
KEY00	00	MCD134	R	112			LEAVE ALL PESTS SET DURING AND AFTER THE PHASE	PH 1,2,3,4
KEY01	01						ROLLBACK TO TAPE 1	PH 3,4
KEY02	02						ROLLBACK TO TAPE 2	PH 3,4
KEY03	03						ROLLBACK NUMBER OF ORDERS INDICATED BY DATA INSERT KEYS	PH 2,3,4
KEY04	04						ROLLBACK TO ORDER NUMBER INDICATED BY DATA INSERT KEYS	PH 2,3,4
KEY05	05						CLEAR DISK AREAS SPECIFIED BY SYSTEM INTEGRITY PROGRAM	PH 3,4
KEY06	06						CLEAR NETWORK MANAGEMENT CONTROLS	PH 2,3,4
KEY07	07						INITIALIZE TOSL	PH 3,4
KEY08	08						REMOVE MAS AUDIO	PH 4
KEY11	11						RESTORE DUPLEX FAILED UNITS (WITH MRA SET)	PH 3
KEY11	11						RESTORE ALL UNITS TO DUPLEX	PH 4
KEY14	14						DUPLEX FAIL PUBB	PH 4
KEY15	15						MULTIPLE TAPE SR (GEN AND ODA ON SEPARATE TAPES)	SR
KEY16	16						ZERO ALL CALL OR PROGRAM STORE MEMORY NOT BACKED UP ON DISK	AO,PC (PUMP)
KEY17	17						SKIP HASH SUM CALCULATIONS. SKIP ID2FS MAP CHECKS	SR,AO,PC
KEY18	18						BYPASS CC SANITY TESTS (ALLOW DUPLEX FAILED PUBS)	PH 3,4,SR,PC
KEY19	19						INHIBIT TAPE ERROR CORRECTION PROCEDURE DURING SR	SR
KEY20	20						INHIBIT MAP AUDIT FAILURES DURING AN SR	SR
KEY21	21						INHIBIT STORE MAINTENANCE TESTS	SR,AO,PC (PUMP)
KEY22	22						DISK DATA READBACK AND VERIFY	SR
KEY23	23	MCD134	R	112			ALLOW DUPLEX API FAILURES DURING SR	SR(MIN CFG EMER MODE)

SR = System Reinitialization, PC = Processor Configuration, AO = Activate Override, PH = Phase(s)

WRITE ODA DATA ON TAPE (800 BPI)

[1] See CAUTION 1. Notify MAC personnel that ODA tape is to be written

[2] Mount blank or erasable tape with permit ring on tape transport [DLP-512]

[3] At MCC, depress **RESTRICT RECENT CHANGE** pushbutton

RESTRICT RECENT CHANGE lamp lights

[4] Type:

SET:TUC a;FUNCTION CPY!

(a = member number of TUC)

Output message
SET:TUCa; [FIG. 1]

AND

[5] Read SET:TUC message and verify proper tape was mounted

[6] Type:

ALW;TUC a:RW!

a = member number of TUC)

Output messages
COPY:ODA;TAPE COMPL
COPY:VFY;TAPE COMPL
REPT:DEMOUNT TAPE

[7] Type:

COPY:ODA;TAPE:VFY!

[8] Demount tape from tape transport [DLP-513]

AND

[9] Depress **RESTRICT RECENT CHANGE** pushbutton

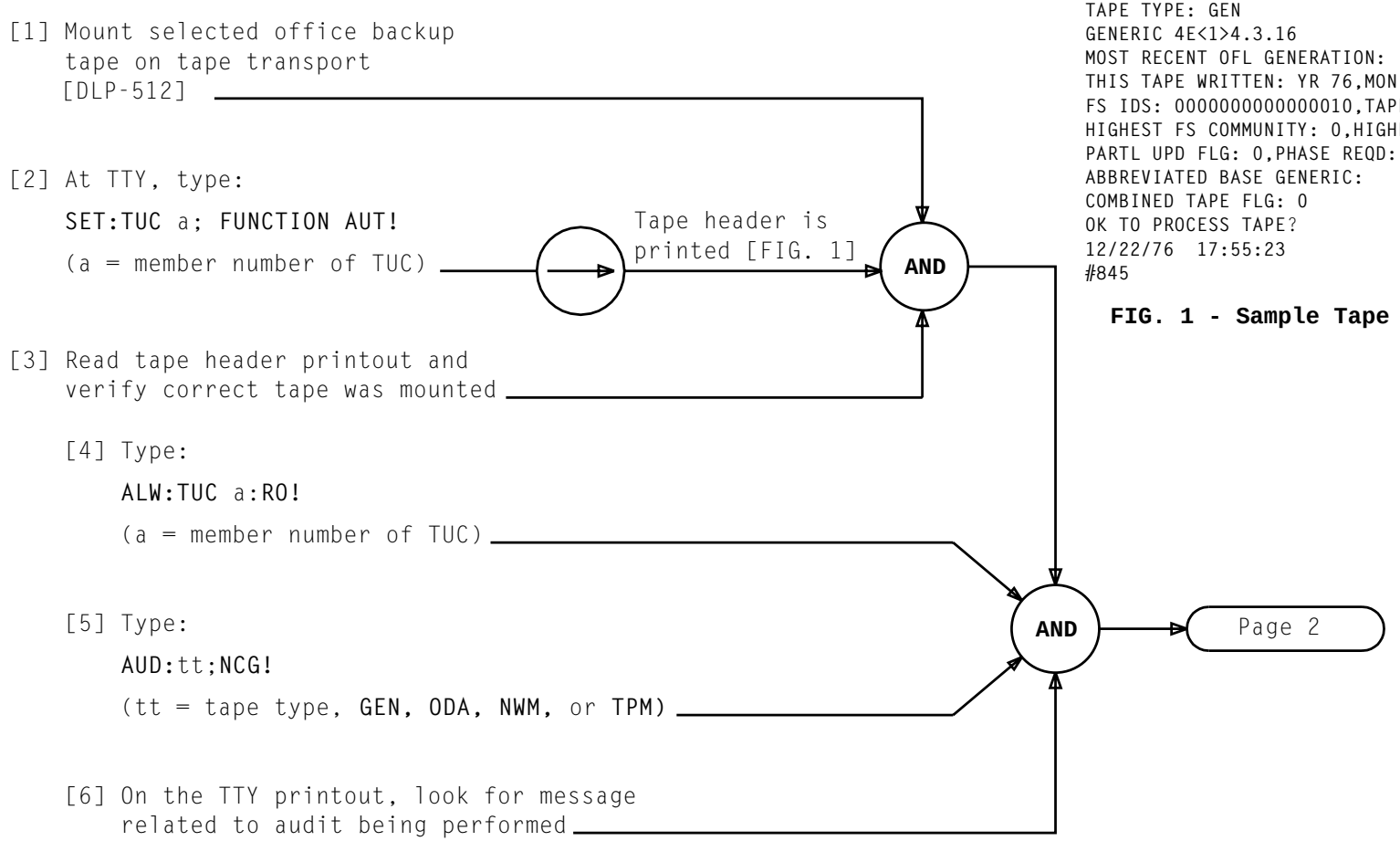
RESTRICT RECENT CHANGE lamp goes off

```
M 42 SET:TUC   1;
     TAPE MOUNTED ON TUC
     TAPE TYPE: BLANK
     OK TO PROCESS TAPE?
     07/11/77  12:42:18
     #989
```

FIG. 1 — Sample for Blank Tape

CAUTION 1
Writing new ODA tape will affect rollback ability

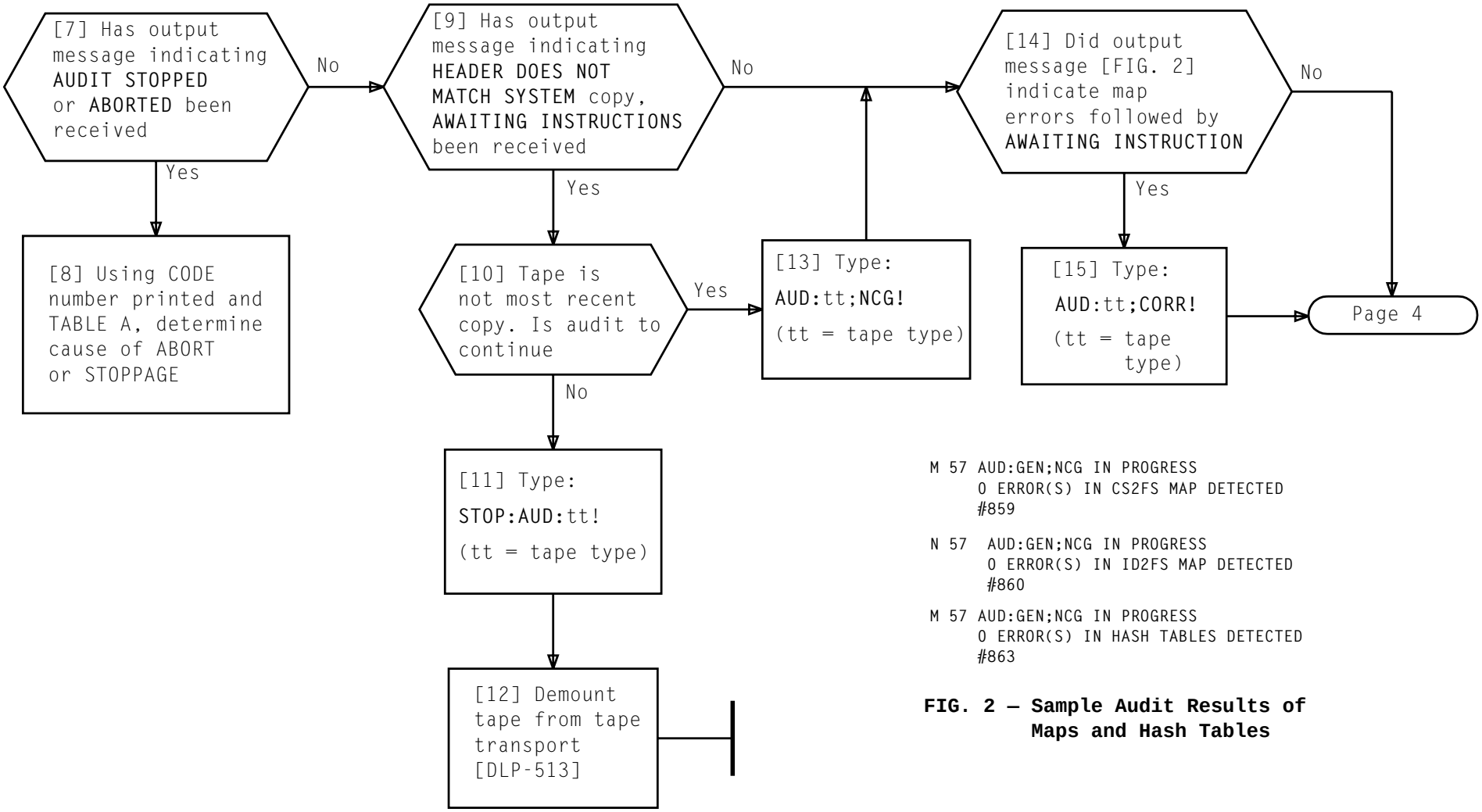
SUMMARY	
On idle tape transport, select and mount tape containing data to be audited. Input appropriate message to allow tape audit (SAST) to run in noncorrecting mode. Observe TTY for output messages.	When output message indicates **AWAIT INSTRUCTION**, system wait 30 minutes for response before timing out. Analyze output message and when appropriate, run audit in correction mode, correct errors, or type **STOP:AUD** message to clear tape audit program




```
M 55 SET:TUC  3;
     TAPE MOUNTED ON TUC
     TAPE TYPE: GEN
     GENERIC 4E<1>4.3.16
     MOST RECENT OFL GENERATION:  YR 76,MON 09,DAY 01 AT 19:23
     THIS TAPE WRITTEN: YR 76,MON 09,DAY 01 AT 19:23
     FS IDS: 0000000000000010,TAPE IDS 0000000011111111
     HIGHEST FS COMMUNITY: 0,HIGHEST FS: 2
     PARTL UPD FLG: 0,PHASE REQD: 0000100
     ABBREVIATED BASE GENERIC:
     COMBINED TAPE FLG: 0
     OK TO PROCESS TAPE?
     12/22/76  17:55:23
     #845
```

FIG. 1 - Sample Tape Audit Header Printout

PERFORM TAPE AUDIT OF WRITABLE STORES (SAST)




```
M 57 AUD:GEN;NCG IN PROGRESS
     0 ERROR(S) IN CS2FS MAP DETECTED
     #859

N 57  AUD:GEN;NCG IN PROGRESS
      0 ERROR(S) IN ID2FS MAP DETECTED
      #860

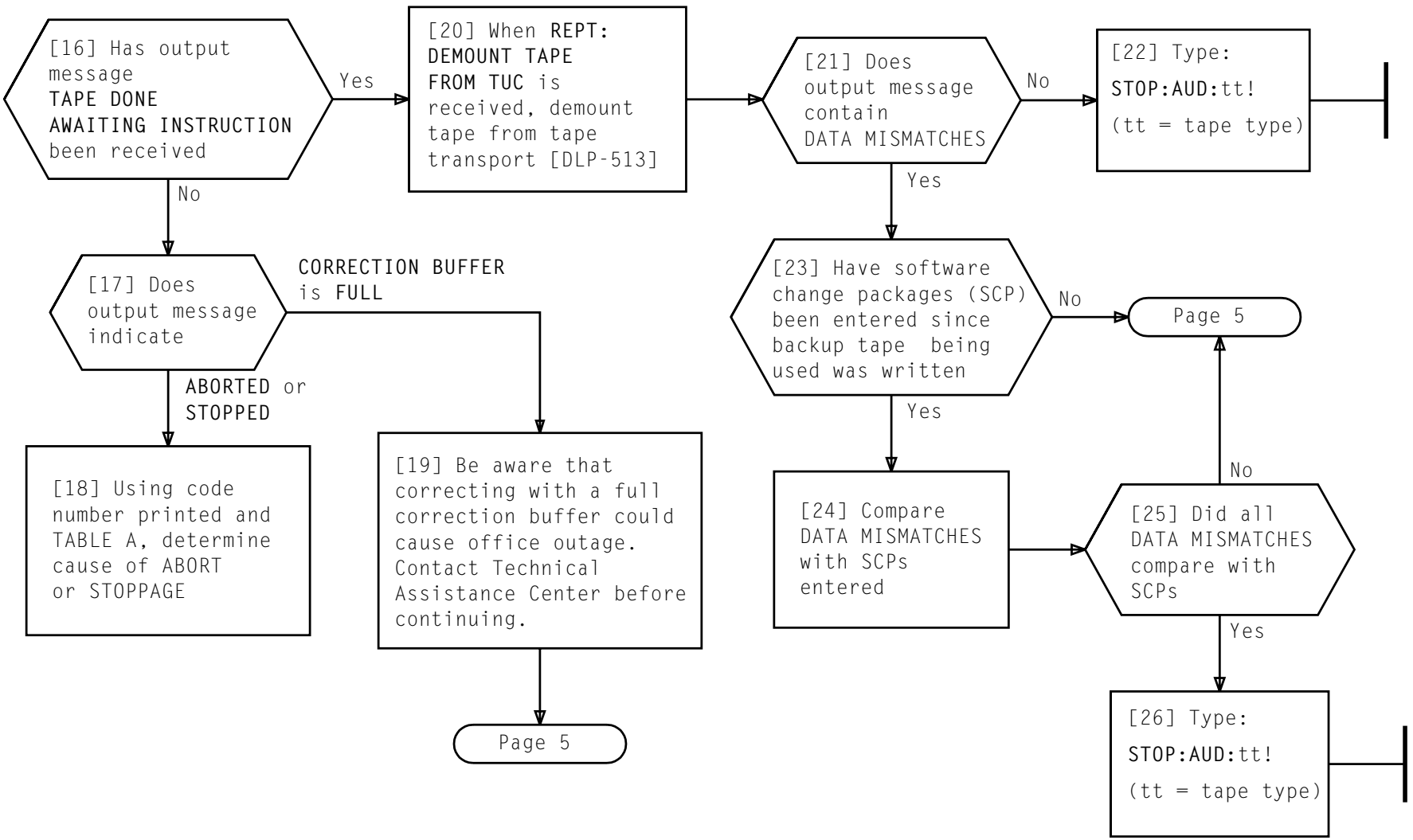
M 57 AUD:GEN;NCG IN PROGRESS
     0 ERROR(S) IN HASH TABLES DETECTED
     #863
```

FIG. 2 — Sample Audit Results of Maps and Hash Tables

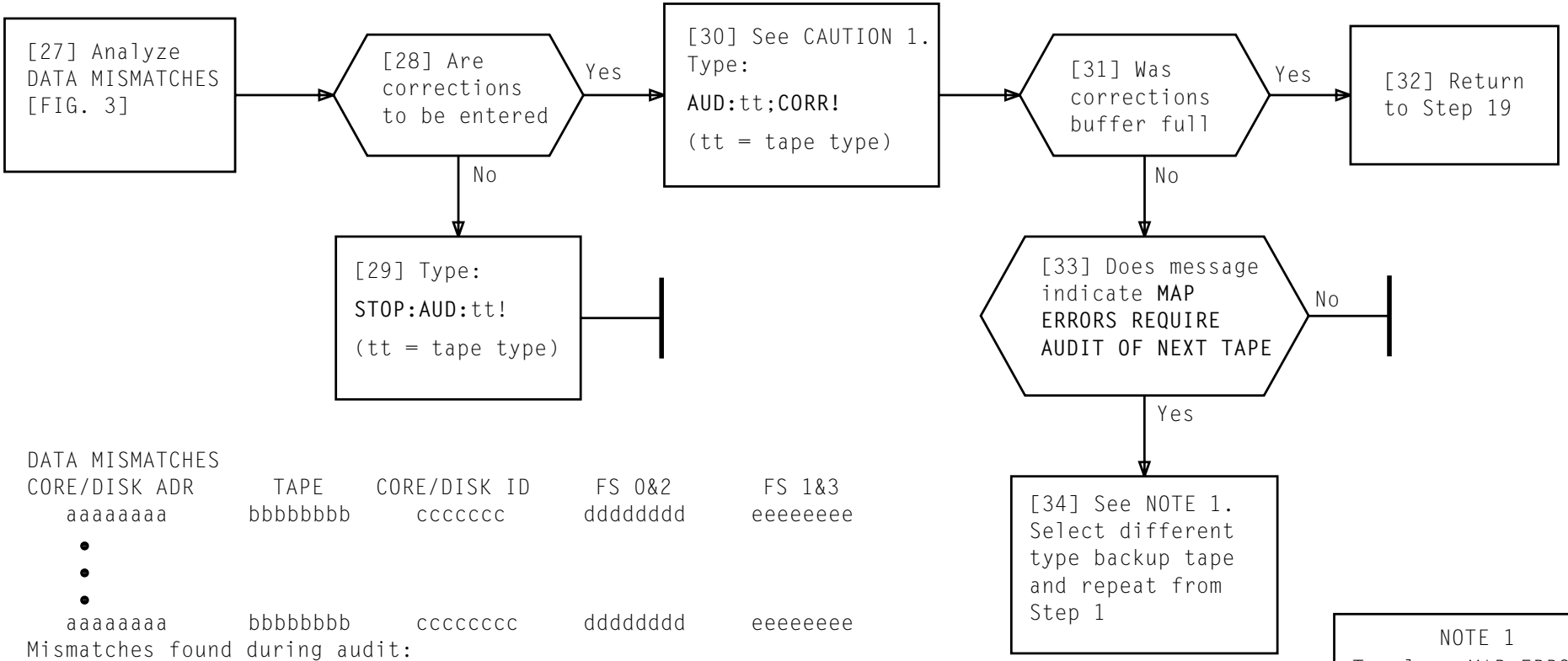
PERFORM TAPE AUDIT OF WRITABLE STORES (SAST)

TABLE A
STOPPED AND ABORTED CODE DEFINITIONS

CODE	DEFINITION	CODE	DEFINITION
1.	Tape header expected, EOF read	62.	Mismatches found between system maps and maps on nonmemory allocating tape
3.	Merge data file header expected, EOF read	63.	Invalid load mode for given tape type
4.	Merge data file header expected, ID mismatch	64.	Invalid hash sum head table index encountered while processing hash sums in load mode
5.	CS2FS map expected, EOF read	70.	Tape secure failed
6.	CS2FS map expected, ID mismatch	71	Tape unit not in proper mode
7.	ID2FS map expected EOF read	72.	Read tape header request rejected
10.	ID2FS map expected, ID mismatch	73.	Read data record request rejected
11.	Hash sum head table expected, EOF read	74.	Tape operation failed
12.	Hash sum head table expected, ID mismatch	75.	Unexpected EOT detected
14.	File header expected, ID mismatch	76.	Open file request rejected
15.	SAST unable to determine hash head cell contents	78.	Advance to end-of-file request rejected
40.	Print request rejected	79.	Advance to end of file failed
50.	Disk read request rejected	80.	RC check failed. Personnel must decide if rollback is required
51.	Disk write request rejected	91.	Disk operation failed
52.	Disk queue full	93.	MACP holding time exceeded
53.	Both file stores out of service	94.	Paging supervisor aborted
54.	Core address to file store address conversion failed. No backup	96.	Interrupt occurred while SAST was in progress
60.	SAWS lockout. Other core changing client in progress	97.	Termination manually requested
61.	Unable to determine disk address of hash sum	Other	Unassigned



PERFORM TAPE AUDIT OF WRITABLE STORES (SAST)



DATA MISMATCHES

CORE/DISK ADR	TAPE	CORE/DISK ID	FS 0&2	FS 1&3
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee
•				
•				
•				
aaaaaaaa	bbbbbbbb	cccccccc	dddddddd	eeeeeeee

Mismatches found during audit:

a = Octal number indicating core (or disk) address. If address is FS, only bit 23 is set

b = Octal number indicating data found on tape

c = Octal number indicating data found in core (or disk ID tag is FS only)

d = Octal number indicating data found in FS 0

e = Octal number indicating data found in FS 1

FIG. 3 — Mismatch Data Layout

NOTE 1

To clear MAP ERRORS may require this procedure to be used with each type of backup tape

CAUTION 1

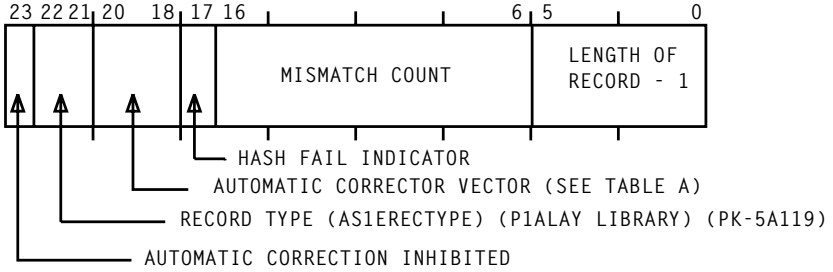
SCPs entered since last backup tape was written is lost at this point and must be reentered

PERFORM TAPE AUDIT OF WRITABLE STORES (SAST)

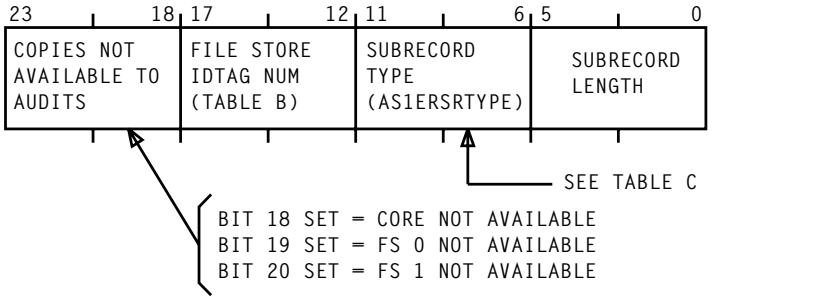
1. Use FIG. 1 and TABLES A, B, and C to analyze data

```
aaaaaaaa bbbbbbbb cccccccc cccccccc cccccccc cccccccc cccccccc cccccccc
cccccccc cccccccc dddddddd dddddddd dddddddd eeeeeeee ffffffff gggggggg
gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg
gggggggg gggggggg gggggggg gggggggg gggggggg gggggggg
```

WORD a = SAWS Record Header



WORD b = Error Subrecord Header



WORDS c = CC Registers
WORDS d = Stack Entries
WORD e = SAWs Subtask Activity Word
WORD f = SAWs Inhibit, Update Program Activity Word
WORDS g = SAWs Update Client Subroutine Control Block

FIG. 1

ANALYZE LOCKOUT INTERFACE FAILURE AND DATA MISMATCH DURING UPDATE WORDS FOR SAWS AUDIT

TABLE A AUTO CORRECTION VECTOR STATES	
STATE	**DESCRIPTION**
0	Core corrected from either file store
1	Write to file store 0
2	Write to file store 1
3	Core corrected from file store 1
4	Core corrected from file store 0
5	Write to file store 0 and file store 1
6	File store 0 copied to file store 1
7	File store 1 copied to file store 0

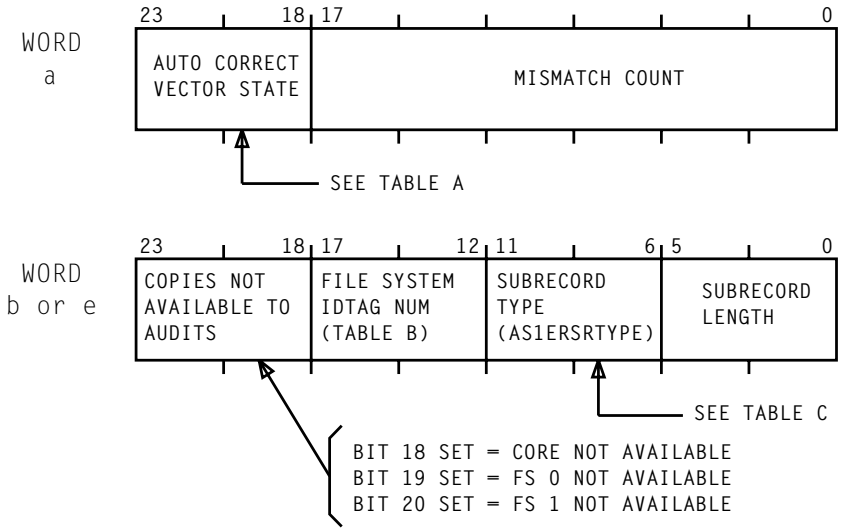
TABLE B			
FS ID TAG NUM	**FS AREA NAME**	**FS ID TAG NUM**	**FS AREA NAME**
01	Generic program	12	Merge
02	Library area	13	RC rollback
03	Office data	14	TR/PLT measurement
07	NTWK management	Other	Invalid for SAWS

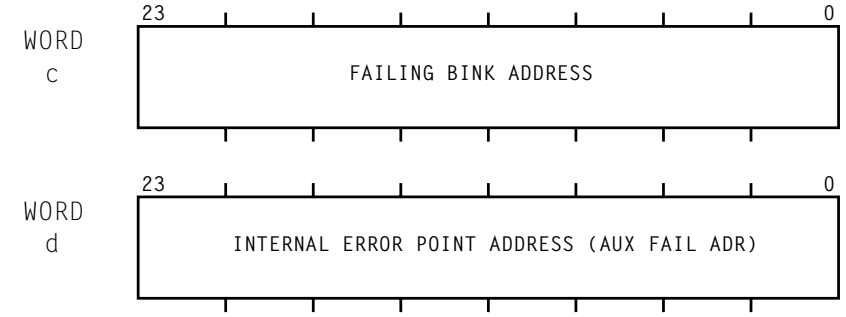
TABLE C ERROR SUBRECORD TYPE	
STATE	**DESCRIPTION**
1	Mismatch subrecord
2	Bink hash failure subrecord
3	Merge structure hash failure
4	Failing range corrected
5	Automatic correction inhibited
6	Excessive failing binks within 64-bink range
7	Internal error detected
8	Terminal error detected
9	Immediate fail return from DKAD of read into buffer
10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWs update subroutine
Other	Unassigned

ANALYZE LOCKOUT INTERFACE FAILURE AND DATA MISMATCH DURING UPDATE WORDS FOR SAWS AUDIT

1. Use FIG. 1 and TABLES A, B, and C to analyze data

```
Text phrase or phrases
DATA: aaaaaaaa
DATA:
bbbbbbbb cccccccc dddddddd
HASH CODE FAILURE
DATA:
eeeeeeee ffffffff gggggggg hhhhhhhh iiiiiiii jjjjjjjj
DATA MISMATCH
DATA:
eeeeeeee ffffffff gggggggg hhhhhhhh iiiiiiii jjjjjjjj
```





WORD	FOR HASH CODE FAILURE	FOR DATA MISMATCH
f	FAILING BINK ADDRESS	MISMATCH ADDRESS
g	CORE-RESIDENT STORE HASH SUM	FILE SYSTEM ADDRESS
h	COMPUTED FS 1 HASH SUM	FS 1 DATA
i	COMPUTED FS 0 HASH SUM	FS 0 DATA
j	COMPUTED CORE HASH SUM	CORE DATA

FIG. 1

ANALYZE HASH CODE FAILURE AND DATA MISMATCH WORDS FOR SAWS AUDIT

TABLE A AUTO CORRECTION VECTOR STATES	
STATE	**DESCRIPTION**
0	Core corrected from either file system
1	Write to file system 0
2	Write to file system 1
3	Core corrected from file system 1
4	Core corrected from file system 0
5	Write to file system 0 and file system 1
6	File system 0 copied to file system 1
7	File system 1 copied to file system 0

TABLE B			
FS ID TAG NUM	**FS AREA NAME**	**FS ID TAG NUM**	**FS AREA NAME**
01	Generic program	12	Merge
02	Library area	13	RC rollback
03	Office data	14	TR/PLT measurement
07	NTWK management	Other	Invalid for SAWS

TABLE C ERROR SUBRECORD TYPE	
STATE	**DESCRIPTION**
1	Mismatch subrecord
2	Bink hash failure subrecord
3	Merge structure hash failure
4	Failing range corrected
5	Automatic correction inhibited
6	Excessive failing binks within 64-bink range
7	Internal error detected
8	Terminal error detected
9	Immediate fail return from DKAD of read into buffer
10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWs update subroutine
Other	Unassigned

ANALYZE HASH CODE FAILURE AND DATA MISMATCH WORDS FOR SAWS AUDIT

1. Use FIG. 1 and TABLES A and B to analyze data

EXCESSIVE HASH FAILURE DATA:

aaaaaaaa bbbbbbbb cccccccc dddddddd eeeeeeee

WORD a = ERROR SUBRECORD HEADER

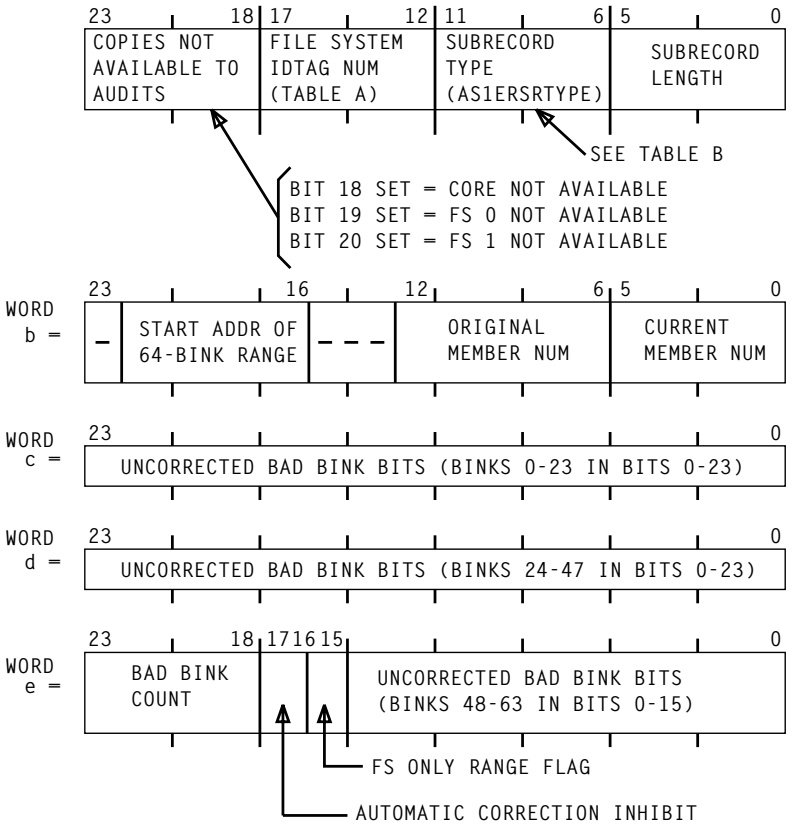


FIG. 1

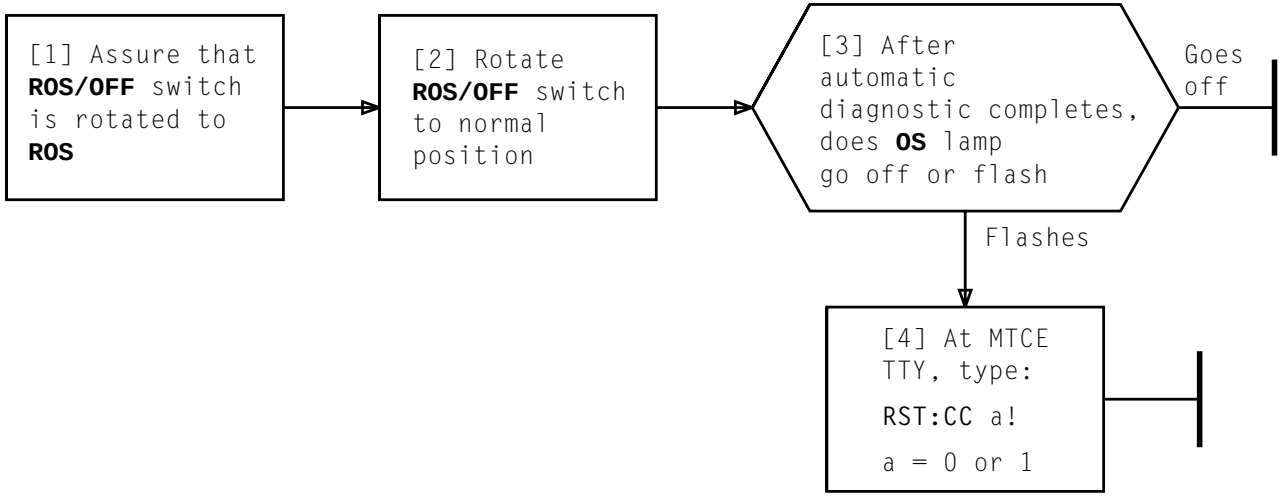
TABLE A

FS ID TAG NUM	FS AREA NAME	FS ID TAG NUM	FS AREA NAME
01	Generic program	12	Merge
02	Library area	13	RC rollback
03	Office data	14	TR/PLT measurement
07	NTWK management	Other	Invalid for saws

TABLE B
ERROR SUBRECORD TYPE

STATE	DESCRIPTION
1	Mismatch subrecord
2	Bink hash failure subrecord
3	Merge structure hash failure
4	Failing range corrected
5	Automatic correction inhibited
6	Excessive failing binks within 64-bink range
7	Internal error detected
8	Terminal error detected
9	Immediate fail return from DKAD of read into buffer
10	Special hash sums mismatch
11	No good copy of failing range available
12	Good copy of failing range not identifiable
13	Immediate fail return from DKAD during correction
14	Audit-update program interface problem detected
15	Hash structure problem detected
16	DKAD failure return in a SAWs update subroutine
Other	Unassigned

ANALYZE EXCESSIVE HASH CODE FAILURE AND DATA MISMATCH WORDS FOR SAWS AUDIT



RESTORE CENTRAL CONTROL TO SERVICE

1. Use most significant bits to
   determine order number and type: [TABLE A]

TABLE A

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS	FOOTNOTES
000 000 00	X	S20	FILL	
000 000 01	S	S10A	SX	
000 000 1	S	S09A	S (INX)	*
000 001 0	W	S08A	CW	
000 001 1	L	S07A	C	
000 010 0	W	S08A	AW	
000 010 1	L	S07A	A	
000 011 0	W	S08A	LW	
000 011 1	L	S07A	L	
000 100 01	S	S10B	SZ (INX)	*
000 100 1	S	S09B	S (INX)	*
000 101 0	W	S08B	CW (INX)	*
000 101 1	L	S07B	C (INX)	*
000 110 0	W	S08B	AW (INX)	*
000 110 1	L	S07B	A (INX)	*
000 111 0	W	S08B	LW (INX)	*
000 111 1	L	S07B	L (INX)	*
001 000 01	S	S10C	SX (INX)	*
001 000 1	S	S09C	S (INX)	*
001 001 0	W	S08C	CW (INX)	*
001 001 1	L	S07C	C (INX)	*
001 010 0	W	S08C	AW (INX)	*
001 010 1	L	S07C	A (INX)	*
001 011 0	W	S08C	LW (INX)	*
001 011 1	L	S07C	L (INX)	*
001 1	W	S13	LWA (INX)	*
010 0	L	S11	LA (INX)	*
010 1	A	S12	SA (INX)	*

* Index register specified

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 00	L	L01A	IF(T):<LACPUX>	(INX)	*
011 00	L	L01B	IF(T):<LACPUX>	REL	†
011 00	L	L01C	IF(T):<LACPUX>	REL INX	* †
011 00	L	L01D	IF(T):<LACPUX>	INX	*
011 00	L	L01E	IF(T):<LACPUX>	REL	†
011 00	L	L01F	IF(T):<LACPUX>	REL INX	* †
011 00	S	L01G	IF(T):<S/SS>	(INX)	*
011 00	S	L01H	IF(T):<S/SS>	REL	†
011 00	S	L01I	IF(T):<S/SS>	REL INX	* †
011 00	S	L01J	IF(T):<S/SS>	(INX)	*
011 00	S	L01K	IF(T):<S/SS>	REL	†
011 00	S	L01L	IF(T):<S/SS>	REL INX	* †
011 00	W	L01M	IF(T):<LACPUX>W	(INX)	* †
011 00	W	L01N	IF(T):<LACPUX>W	REL	†
011 00	W	L01O	IF(T):<LACPUX>W	REL INX	* †
011 00	W	L01P	IF(T):<LACPUX>W	(INX)	* †
011 00	W	L01Q	IF(T):<LACPUX>W	REL	†
011 00	W	L01R	IF(T):<LACPUX>W	REL INX	* †
011 00	X	L01S	IFT:<LACPUX/S/SS>	(INX)	*
011 00	X	L01S	IFT:<LACPUX/S/SS>	REL	†
011 00	X	L01S	IFT:<LACPUX/S/SS>	REL INX	* †
011 00	X	L01S	IFT:<LACPUX/S/SS>	(INX)	* †
011 00	X	L01S	IFT:<LACPUX/S/SS>	REL	†
011 00	X	L01S	IFT:<LACPUX/S/SS>	REL INX	* †
011 010	L	L02A	<LACPUX>	(INX)	*
011 010	L	L02B	<LACPUX>	REL	†
011 010	L	L02C	<LACPUX>	REL INX	* †
011 010	L	L02D	<LACPUX>	(INX)	*
011 010	L	L02E	<LACPUX>	REL	†
011 010	L	L02F	<LACPUX>	REL INX	* †
011 010	S	L02G	<S/SS>	(INX)	*
011 010	S	L02H	<S/SS>	REL	†

* Index register specified
† Relative addressing

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS	FOOTNOTES
011 010	S	L02I	<S/SS> REL INX	* †
011 010	S	L02J	<S/SS> (INX)	*
011 010	S	L02K	<S/SS> REL	†
011 010	S	L02L	<S/SS> REL INX	* †
011 010	W	L02M	<LACPUX>W (INX)	*
011 010	W	L02N	<LACPUX>W (REL)	†
011 010	W	L02O	<LACPUX>W REL INX	* †
011 010	W	L02P	<LACPUX>W (INX)	*
011 010	W	L02Q	<LACPUX>W REL	†
011 010	W	L02R	<LACPUX>W REL INX	* †
011 011 00	L	L14A	<H/Q>:<LACPUX> (INX)	*
011 011 00	L	L14B	<H/Q>:<LACPUX> REL	†
011 011 00	L	L14C	<H/Q>:<LACPUX> REL INX	* †
011 011 00	S	L14D	<H/Q>:<S/SS> (INX)	*
011 011 00	S	L14E	<H/Q>:<S/SS> REL	†
011 011 00	S	L14F	<H/Q>:<S/SS> REL INX	* †
011 011 010 0	T	L04A	IF:T(A)	
011 011 010 0	T	L04B	IF:T(A)	
011 011 010 0	T	L04C	IF:T(A) INX	*
011 011 010 0	T	L04D	IF:TI(A) INX	*
011 011 010 0	T	L04E	IF:T(A) REL	†
011 011 010 0	T	L04F	IF:TI(A) REL	†
011 011 010 0	T	L04G	IF:T(A) REL INX	* †
011 011 010 0	T	L04H	IF:TI(A) REL INX	* †
011 011 010 1	T	L06A	IF:T DT (INX)	* †
011 011 010 1	T	L06B	IF:T DT VT INX)	* ‡ §
011 011 010 1	T	L06C	IF:TI DT INX)	* ‡
011 011 010 1	T	L06D	IF:T DT REL INX	* † ‡
011 011 010 1	T	L06E	IF:TI DT REL INX	* † ‡

* Index register specified
† Relative addressing
‡ Delayed transfer (condition cannot be used until late in first cycle)
§ Vector table addressing

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 011 011 00	T	L03A	T	(INX)	*
011 011 011 00	T	L03B	TI	(INX)	*
011 011 011 00	T	L03C	T	REL	†
011 011 011 00	T	L03D	TI	REL	†
011 011 011 00	T	L03E	T	REL INX	* †
011 011 011 00	T	L03F	TI	REL INX	* †
011 011 011 01	T	L03A	IF:TI	(INX)	*
011 011 011 01	T	L05B	IF:TI	(INX)	*
011 011 011 01	T	L05C	IF:T	REL	†
011 011 011 01	T	L05D	IF:TI	REL	†
011 011 011 01	T	L05E	IF:T	REL INX	* †
011 011 011 01	T	L05F	IF:TI	REL INX	* †
011 011 011 01	T	L07A	<F/Z>:T(I)	(REL) (INX)	* †
011 011 011 01	T	L07B	<F/Z>:T DT	(INX)	* ‡
011 011 011 01	T	L07C	<F/Z>:TI DT	(INX)	* ‡
011 011 011 01	T	L07D	<F/Z>:T DT	REL (INX)	* † ‡
011 011 011 01	T	L07E	<F/Z>:TI DT	REL (INX)	* † ‡
011 011 100	L	L08A	LA	(INX)	*
011 011 100	L	L08B	LA	REL	†
011 011 100	L	L08C	LA	REL INX	* †
011 011 101	S	L09A	SA	(INX)	*
011 011 101	S	L09B	SA	REL	†
011 011 101	S	L09C	SA	REL INX	* †
011 011 110	W	L10A	LWA	(INX)	*
011 011 110	W	L10B	LWA	REL	†
011 011 110	W	L10C	LWA	REL INX	* †
011 011 111 000 0	L	L11	L (24 Bit)	(INX)	*
011 011 111 000 1	W	L13	LW (24 Bit)	(INX)	*
011 011 111 001 0	S	L12	S (24 Bit)	(INX)	*
011 011 111 001 1	Y	L18A	PUSH	(INX)	*

* Index register specified
† Relative addressing
‡ Delayed transfer (condition cannot be used until late in first cycle)

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 011 111 001 1	Y	L18B	PUSH	REL	†
011 011 111 001 1	W	L18C	PUSH	REL INX	* †
011 011 111 010	S	L15	<SD/SSD>	(INX)	*
011 011 111 011 ππ1	W	L19	SCINS		π
011 011 111 10	T	L16A	EXC	(INX)	*
011 011 111 10	T	L16B	EXC	REL	†
011 011 111 10	T	L16C	EXC	REL INX	* †
011 011 111 11	L	L17	SEARCH		
011 100 000 000 0ππ 00	W	IO1A	OW	(INX)	* π
011 100 000 000 0ππ 00	W	IO1B	OW	REL	† π
011 100 000 000 0ππ 00	W	IO1C	OW	REL INX	* † π
011 100 000 000 0ππ 00	W	IO1D	OW	(INX)	* π
011 100 000 000 0ππ 00	W	IO1E	OW	REL	† π
011 100 000 000 0ππ 00	W	IO1F	OW	REL INX	* † π
011 100 000 000 1ππ 00	L	IO2A	O	(INX)	* π
011 100 000 000 1ππ 00	L	IO2B	O	REL	† π
011 100 000 000 1ππ 00	L	IO2C	O	REL INX	* † π
011 100 000 000 1ππ 00	L	IO2D	O	(INX)	* π
011 100 000 000 1ππ 00	L	IO2E	O	REL	† π
011 100 000 000 1ππ 00	L	IO2F	O	REL INX	* † π
011 100 000 000 1ππ 00	L	IO2G	O	(INX)	* π
011 100 000 000 1ππ 00	L	IO2H	O	REL	† π
011 100 000 000 1ππ 00	L	IO2I	O	REL INX	* † π
011 100 000 000 1ππ 00	L	IO2J	O	(INX)	* π
011 100 000 000 1ππ 00	L	IO2K	O	REL	† π
011 100 000 000 1ππ 00	L	IO2L	O	REL INX	* † π
011 100 000 001 0ππ 00	W	IO3A	IW	(INX)	* π
011 100 000 001 0ππ 00	W	IO3B	IW	REL	† π
011 100 000 001 0ππ 00	W	IO3C	IW	REL INX	* † π
011 100 000 001 0ππ 00	W	IO3D	IW	(INX)	* π
011 100 000 001 0ππ 00	W	IO3E	IW	REL	† π

* Index register specified
† Relative addressing
π Don't care bit (can be 0 or 1)

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 100 000 001 0ππ 00	W	I03F	IW	REL INX	* †π
011 100 000 000 0ππ 00	L	I04A	I	(INX)	* π
011 100 000 000 0ππ 00	L	I04B	I	REL	† π
011 100 000 000 0ππ 00	L	I04C	I	REL INX	* †π
011 100 000 000 0ππ 00	L	I04D	I	(INX)	* π
011 100 000 000 0ππ 00	L	I04E	I	REL	† π
011 100 000 000 0ππ 00	L	I04F	I	(INX)	* † π
011 100 000 001 1ππ 00	L	I04G	I	REL INX	* π
011 100 000 001 1ππ 00	L	I04H	I	REL	†π
011 100 000 001 1ππ 00	L	I04I	I	REL INX	* †π
011 100 000 001 1ππ 00	L	I04J	I	(INX)	* π
011 100 000 001 1ππ 00	L	I04K	I	REL	†π
011 100 000 001 1ππ 00	L	I04L	I	REL INX	* †π
011 100 000 010 0ππ 00	W	I05A	DW	(INX)	* π
011 100 000 010 0ππ 00	W	I05B	DW	REL	†π
011 100 000 010 0ππ 00	W	I05C	DW	REL INX	* †π
011 100 000 010 0ππ 00	W	I05D	DW	(INX)	* π
011 100 000 010 0ππ 00	W	I05E	DW	REL	†π
011 100 000 010 0ππ 00	W	I05F	DW	REL INX	* †π
011 100 000 010 1ππ 00	L	I06A	D	(INX)	* π
011 100 000 010 1ππ 00	L	I06B	D	REL	†π
011 100 000 010 1ππ 00	L	I06C	D	REL INX	* †π
011 100 000 010 1ππ 00	L	I06D	D	(INX)	* π
011 100 000 010 1ππ 00	L	I06E	D	REL	†π
011 100 000 010 1ππ 00	L	I06F	D	REL INX	* †π
011 100 000 011 0ππ 00	W	I07A	IWE	(INX)	* π
011 100 000 011 0ππ 00	W	I07B	IWE	REL	†π
011 100 000 011 0ππ 00	W	I07C	IWE	REL INX	* †π
011 100 000 011 0ππ 00	W	I07D	IWE	(INX)	* π
011 100 000 011 0ππ 00	W	I07E	IWE	REL	†π
011 100 000 011 0ππ 00	W	I07F	IWE	REL INX	* †π

* Index register specified * π
† Relative addressing
π Don't care bit (can be 0 or 1)

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 100 000 011 1ππ 00	L	I08A	IE	(INX)	* π
011 100 000 011 1ππ 00	L	I08B	IE	REL	† π
011 100 000 011 1ππ 00	L	I08C	IE	REL INX	* † π
011 100 000 011 1ππ 00	L	I08D	IE	(INX)	* π
011 100 000 011 1ππ 00	L	I08E	IE	REL	† π
011 100 000 011 1ππ 00	L	I08F	IE	REL INX	* † π
011 100 000 10	L	I21	SPKT	(INX)	‡
011 100 000 110 0	L	I19	LXXI/LKUI	(INX)	*
011 100 000 110 1	L	I20A	TUPK	(INX)	*
011 100 000 110 1	L	I20B	TUPX	(INX)	*
011 100 000 111 0	L	I22A	LE	(INX)	*
011 100 000 111 0	L	I22B	LE	REL	†
011 100 000 111 0	L	I22C	LE	REL INX	* †
011 100 000 111 0	L	I22D	LE	(INX)	*
011 100 000 111 0	L	I22E	LE	REL	†
011 100 000 111 0	L	I22F	LE	REL INX	* †
011 100 000 111 1	L	I23A	LP	(INX)	*
011 100 000 111 1	L	I23B	LP	REL	†
011 100 000 111 1	L	I23C	LP	REL INX	* †
011 100 000 111 1	L	I23D	LP	(INX)	*
011 100 000 111 1	L	I23E	LP	REL	†
011 100 000 111 1	L	I23F	LP	REL INX	* †
011 100 010 000 0ππ 00	W	I01A	OW	(INX)	* π
011 100 010 000 0ππ 00	W	I01B	OW	REL	† π
011 100 010 000 0ππ 00	W	I01C	OW	REL INX	* † π
011 100 010 000 0ππ 00	W	I01D	OW	(INX)	* π
011 100 010 000 0ππ 00	W	I01E	OW	REL	† π
011 100 010 000 0ππ 00	W	I01F	OW	REL INX	* † π
011 100 010 000 1ππ 00	L	I02A	O	(INX)	* π
011 100 010 000 1ππ 00	L	I02B	O	REL	† π
011 100 010 000 1ππ 00	L	I02C	O	REL INX	* † π

* Index register specified
† Relative addressing
π Don't care bit (can be 0 or 1)

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 100 010 000 1ππ 00	L	I02D	O	(INX)	*π
011 100 010 000 1ππ 00	L	I02E	O	REL	†π
011 100 010 000 1ππ 00	L	I02F	O	REL INX	*π
011 100 010 000 1ππ 00	L	I02G	O	(INX)	* † π
011 100 010 000 1ππ 00	L	I02H	O	REL	*π
011 100 010 000 1ππ 00	L	I02I	O	REL INX	†π
011 100 010 000 1ππ 00	L	I02J	O	(INX)	* †π
011 100 010 000 1ππ 00	L	I02I	O	REL	*π
011 100 010 000 1ππ 00	L	I02J	O	REL INX	* †π
011 100 010 001 0ππ 00	W	I03A	IW	(INX)	* π
011 100 010 001 0ππ 00	W	I03B	IW	REL	†π
011 100 010 001 0ππ 00	W	I03C	IW	REL INX	* †π
011 100 010 001 0ππ 00	W	I03D	IW	(INX)	* π
011 100 010 001 0ππ 00	W	I03E	IW	REL	†π
011 100 010 001 0ππ 00	W	I03F	IW	REL INX	* †π
011 100 010 001 1ππ 00	L	I04A	I	(INX)	* π
011 100 010 001 1ππ 00	L	I04B	I	REL	†π
011 100 010 001 1ππ 00	L	I04C	I	REL INX	* †π
011 100 010 001 1ππ 00	L	I04D	I	(INX)	* π
011 100 010 001 1ππ 00	L	I04E	I	REL	†π
011 100 010 001 1ππ 00	L	I04F	I	REL INX	* †π
011 100 010 001 1ππ 00	L	I04G	I	(INX)	* π
011 100 010 001 1ππ 00	L	I04H	I	REL	†π
011 100 010 001 1ππ 00	L	I04I	I	REL INX	* †π
011 100 010 001 1ππ 00	L	I04J	I	(INX)	* π
011 100 010 001 1ππ 00	L	I04K	I	REL	†π
011 100 010 001 1ππ 00	L	I04L	I	REL INX	* †π
011 100 010 010 0ππ 00	W	I05A	DW	(INX)	* π
011 100 010 010 0ππ 00	W	I05B	DW	REL	†π
011 100 010 010 0ππ 00	W	I05C	DW	REL INX	* †π
011 100 010 010 0ππ 00	W	I05D	DW	(INX)	* π

* Index register specified
† Relative addressing
π Don't care bit (can be 0 or 1)

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 100 010 010 0ππ 00	W	I05E	DW	REL	† π
011 100 010 010 0ππ 00	W	I05F	DW	REL INX	* † π
011 100 010 010 1ππ 00	L	I06A	D	(INX)	* π
011 100 010 010 1ππ 00	L	I06B	D	REL	† π
011 100 010 010 1ππ 00	L	I06C	D	REL INX	* † π
011 100 010 010 1ππ 00	L	I06D	D	(INX)	* π
011 100 010 010 1ππ 00	L	I06E	D	REL	† π
011 100 010 010 1ππ 00	L	I06F	D	REL INX	* † π
011 100 010 011 0ππ 00	W	I07A	IWE	(INX)	* π
011 100 010 011 0ππ 00	W	I07B	IWE	REL	† π
011 100 010 011 0ππ 00	W	I07C	IWE	REL INX	* † π
011 100 010 011 0ππ 00	W	I07D	IWE	(INX)	* π
011 100 010 011 0ππ 00	W	I07E	IWE	REL	† π
011 100 010 011 0ππ 00	W	I07F	IWE	REL INX	* † π
011 100 010 011 1ππ 00	L	I08A	IE	(INX)	* π
011 100 010 011 1ππ 00	L	I08B	IE	REL	† π
011 100 010 011 1ππ 00	L	I08C	IE	REL INX	* † π
011 100 010 011 1ππ 00	L	I08D	IE	(INX)	* π
011 100 010 011 1ππ 00	L	I08E	IE	REL	† π
011 100 010 011 1ππ 00	L	I08F	IE	REL INX	* † π
011 100 010 110 0	L	119	LXXI/LKUI	(INX)	*
011 100 1π0	L	124A	IRM	(INX)	* π
011 100 1π1	W	124B	IRW	(INX)	* π
011 101 000	L	125A	IMR	(INX)	*
011 101 001	W	125B	IWR	(INX)	*
011 101 010	L	125A	IMR	(INX)	*
011 101 101	W	125B	IWR	(INX)	*
011 101 100	L	126A	ORM	(INX)	*
011 101 101	W	126B	ORW	(INX)	*
011 101 110	L	127A	OMR	(INX)	*

* Index register specified
† Relative addressing
π Don't care bit (can be 0 or 1)

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
011 101 111	W	127B	OWR	(INX)	*
011 11π πππ 00	L	M01	ML	(INX)	* π
011 11π πππ 01	S	M02	MS	(INX)	* π
011 11π πππ 11	W	M04	GCP	(INX)	* π
100	T	S01A	IF:T	REL	†
101 0	T	S01B	IF:T	VT	§
101 1	T	S01C	IF:T	INX	*
101 1	T	S01D	IF:T	INX	*
101 1	T	S01E	IF:T		
110 00	T	S02A	IF:T	DT REL	† ‡
110 010	T	S02A	IF:T	DT REL	† ‡
110 011 0ππ π 0	W	S05A	LR	REL	† π
110 011 0ππ π 1	W	S14	H	(INX)	* π
110 011 100	T	S03A	T	REL	†
110 011 101 0	T	S04A	EXC	REL	†
110 011 101 1	X	S15A	SAVR		
110 011 101 1	X	S15B	NOP		
110 011 110	T	S06A	PUSH	REL	†
110 011 111 0	T	S17	POP		**
110 011 111 10	X	S18	GBN		
110 011 111 11	X	S19	GBNHJ		
110 10	T	S02A	IF:T	DT REL	† ‡
110 110	T	S02A	IF:T	DT REL	† ‡
110 111 0ππ π 0	W	S05A	LR	REL	† ‡
110 111 100	T	S03A	T	REL	†
110 111 101 0	T	S04A	EXC	REL	†
110 111 101 1	X	S16	RESR		
110 111 110	T	S06A	PUSH	REL	†

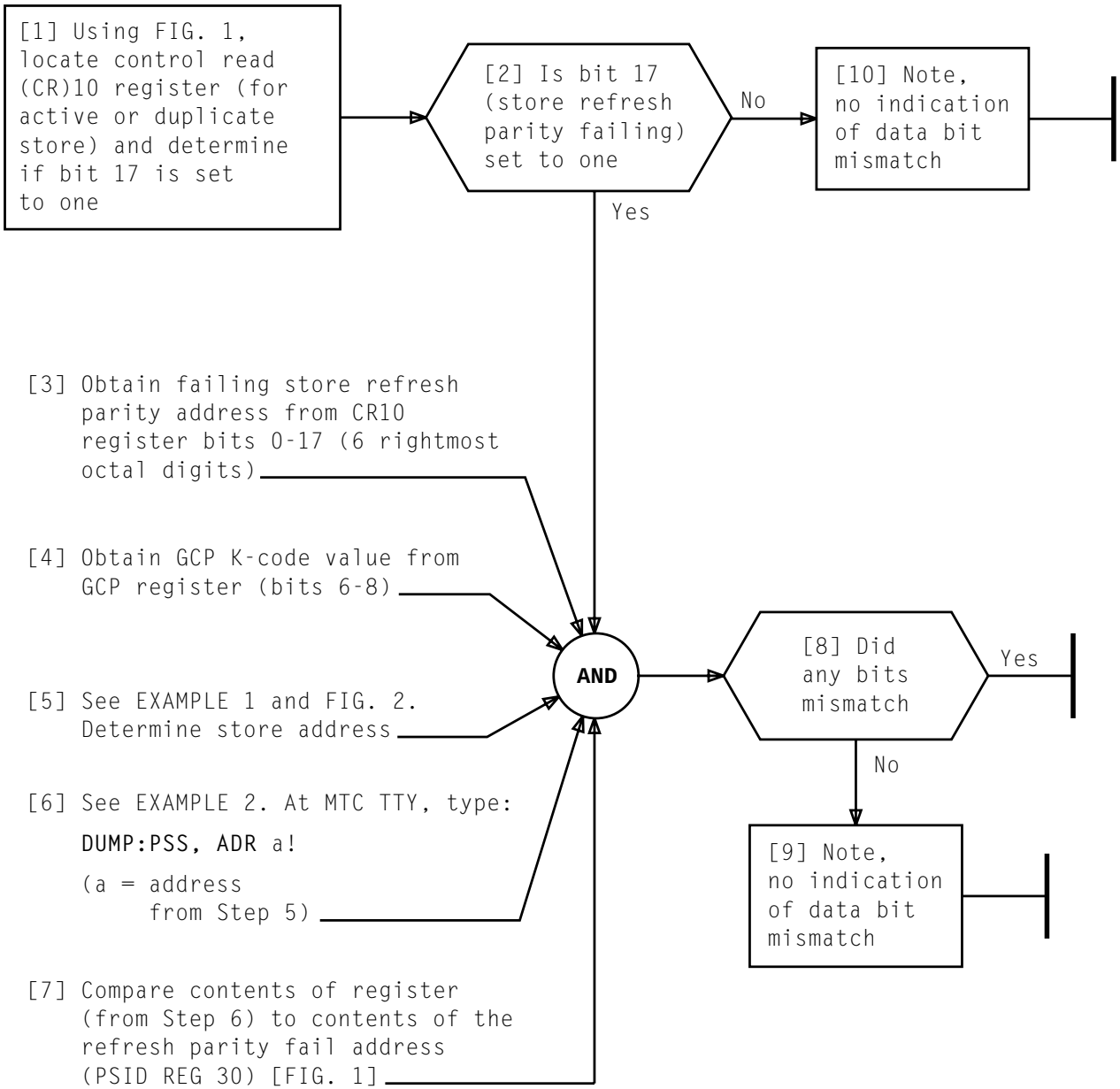
* Index register specified
† Relative addressing
‡ Delayed transfer (condition cannot be used until late in first cycle)
§ Vector table addressing
π Don't care bit (can be 0 or 1)
** POP option for transfer on stack

DETERMINE INSTRUCTION ORDER TYPES AND NUMBERS

TABLE A (Contd)

PROGRAM INSTRUCTION MOST SIGNIFICANT BITS	ORDER TYPE	ORDER NUMBER	ORDER SYNTAX/CHARACTERISTICS		FOOTNOTES
110 111 111	X	S21	STALL		
111 00	T	S02B	IF:T	DT VT	‡ §
111 010	T	S02B	IF:T	DT VT	‡ §
111 010 0ππ π 0	L	S05B	LV		π
111 011 0ππ π 1	W	S14	Q	(INX)	* π
111 011 101 0	T	S04B	EXC	VT	§
111 011 111	T	S22	TI	REL	†
111 011 100		S22	TI	VT	†
111 10	T	S02C	IF:T	DTINX	* ‡
111 10	T	S02D	IF:T	DT	‡
111 110	T	S02C	IF:T	DT INX	* ‡
111 110	T	S02D	IF:T	DT	‡
111 111 0ππ π 1	W	S14	QS	(INX)	* π
111 111 100	T	S03C	T	INX	*
111 111 100	T	S03D	T		
111 111 101 0	T	S04C	EXC	INX	*
111 111 110	T	S06C	PUSH	INX	*
111 111 111	T	S22	TI	REL	†
111 111 111		S22	TI	REL	†
		S03B			

* Index register specified
† Relative addressing
‡ Delayed transfer (condition cannot be used until late in first cycle)
§ Vector table addressing
π Don't care bit (can be 0 or 1)
** POP option for transfer on stack



VERIFY CONTENTS OF FAILING ADDRESS FOR MISMATCHED DATA BITS

```
REPT: E-LEVEL @14335133 MFNUM=00000171 MICON=00000020 COMPLETED
LV=0020 D0=00004000 D1=00000000 D2=00000000 D3=00000000
PSFR REMOVED PS 0
DATA: E-LEVEL

25735661   00000000   00000400   00000004   00000017   00000125
00224525   00320700   00000000   34335133   24040020   14335132
00320700   14335134   33031533   00000103   17210003   00000002
54704236   04000000   02012660   00064100

DATA: PROGRAM STORE IDENTIFICATION DATA

14335134   00000000   40000000   00000000   02012660   41400030
07414005   00000000   33236410   77777777   00000000   41400030
07414005   04000004   00000000   00000000   47760716   00000033
04000003   00000000   00020102   00020500   00000000   00000000
00000000   00000000   54402406   30006406   30344135   00000005
32004400   41400030   12345670   54512411   30406406   31750673
00000005   72205511   41400030   12345670
```

CONTROL READ (CR)10 RESPONSE OF ACTIVE MEMBER

GCP RESPONSE OF ACTIVE MEMBER NUMBER

K-CODE GCP VALUE

GCP RESPONSE OF DUPLICATE MEMBER NUMBER

CONTROL READ 10 RESPONSE OF DUPLICATE MEMBER

FIG. 1 — PSID Register

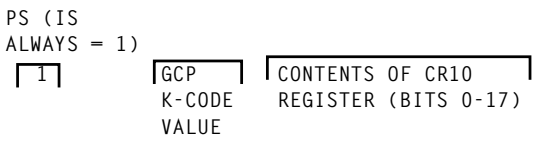
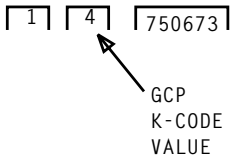


FIG. 2 — PSS Register Format

TO OBTAIN PSS ADDRESS FROM FIG. 1:
BIT 18 IS SET TO ONE IN DUPLICATE CR10 (STEP 2, PAGE 1) REGISTER SO CONTENTS OF THIS REGISTER IS USED AND THIS STORE IS SUSPECT:

CONTENTS OF CR10 (DUPLICATE REGISTER)



THEREFORE, PSS ADDRESS IN THIS EXAMPLE IS:
14750673

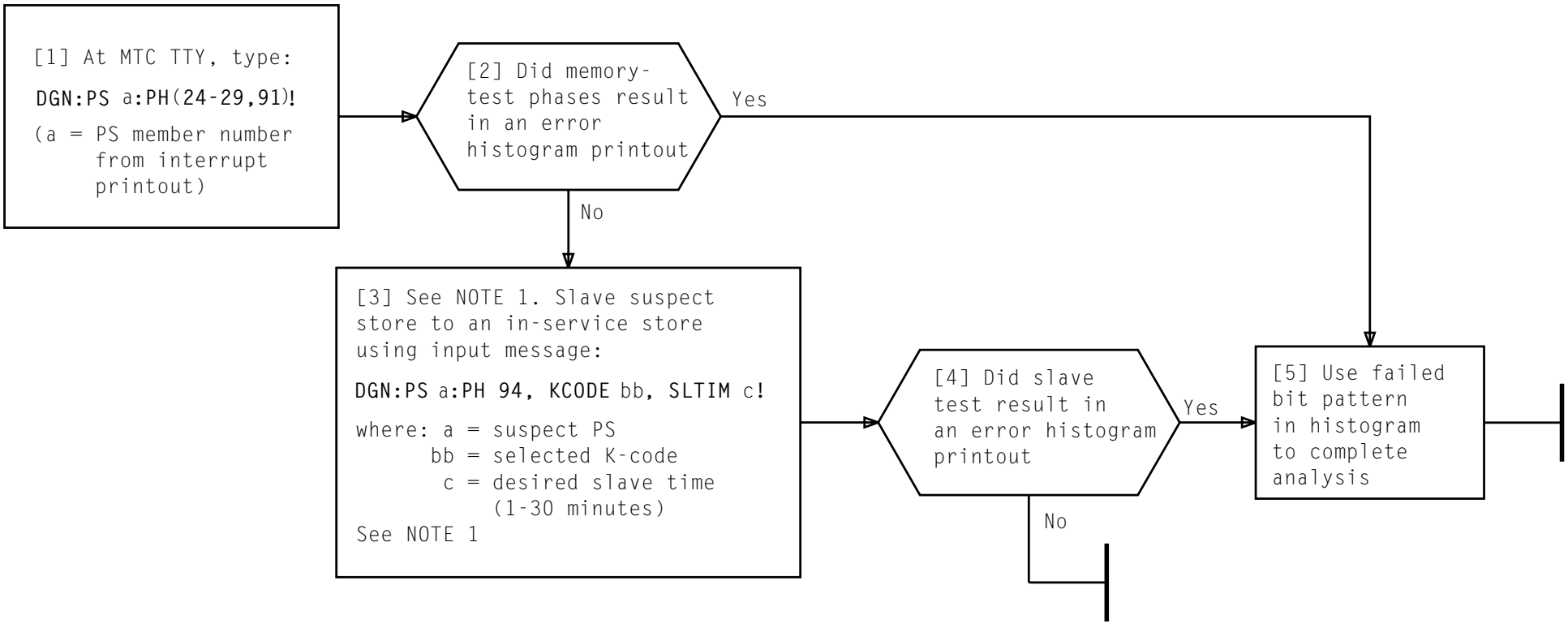
EXAMPLE 1 — Deriving PSS Address

```
DUMP:PSS,ADR 14750673! PF, CODE 091
M 18 DUMP:PSS,INDIR 0,ARD 14750673,INC +0 COMPLETED
     14750673  31600673
     #696
```

CONTENTS OF CR10 ADDRESS BEFORE INTERRUPT (BITS 12-15 MISMATCH)

EXAMPLE 2 — CR10 Dump

COMPARE CONTENTS OF FAILING PROGRAM STORE ADDRESS USING VERIFY MESSAGE FOR DATA BIT MISMATCH



NOTE 1
Selected K-code should be normal office K-code that is assigned to only one in-service store and is other than base store or K-code 34

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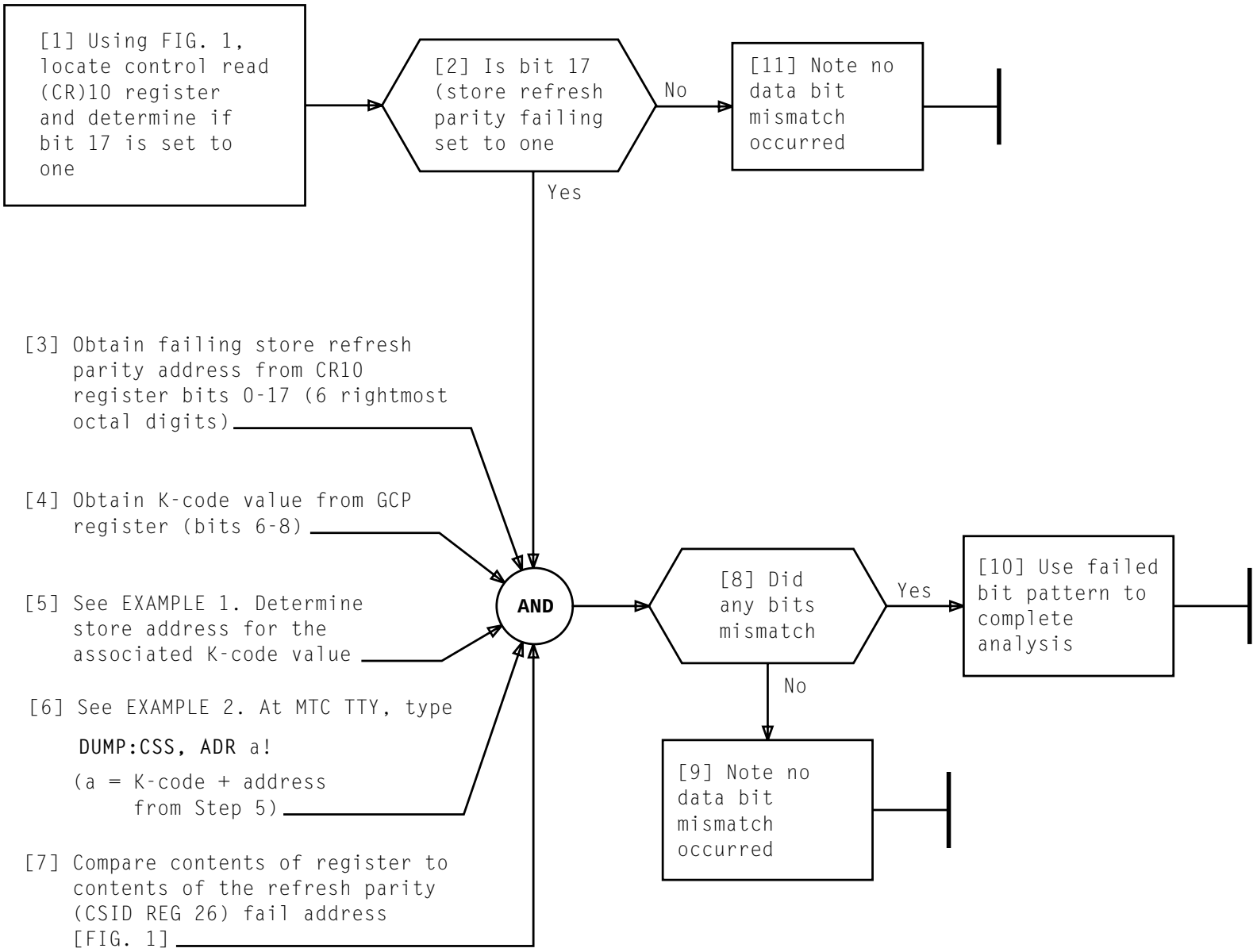
OBTAIN HISTOGRAM USING PROGRAM STORE MEMORY TEST/SLAVE TEST



COMPARE CONTENTS OF FAILING CALL STORE ADDRESS USING VERIFY MESSAGES FOR DATA BIT MISMATCH

```
REPT: D-LEVEL @14442304 MFNUM=00000071 MICON=00000020 COMPLETED
LV=0010 D0=00000010 D1=00000000 D2=00000000 D3=00000000
CSFR REMOVED-CS 3
DATA: D-LEVEL

00047400   07210003   00140000   00041573   00000000   00000001
14362113   00041573   07210003   14442304   00600010   14442302
77777743   14442304   23033711   00002003   17210003   00000005
14342412   04000000   01300400   00104020

DATA: CALL STORE IDENTIFICATION DATA

00004404   00000000   40000003   00000000   01300400   00000100
00000000   00000000   14341722   00000000   00000000   00000000
00000000   74030176   00000011   04000440   00000000   00020503
00000000   00000000   00000000   00000000   55512011   70406011
31600252   00000000   00000000   14341722   00000000   55502010
70006011   30356236   00000000   00000000   14341722   00000000
00004140   00000000   00000000   00000000   00000000   00000000
23401010   10200000   23000000   32000000   43000000
```

CONTROL READ 10 RESPONSE OF ACTIVE MEMBER

CONTROL READ 01 RESPONSE OF ACTIVE MEMBER

GCP RESPONSE OF DUPLICATE MEMBER

CONTROL READ 01 RESPONSE OF DUPLICATE MEMBER

CONTROL READ 10 RESPONSE OF DUPLICATE MEMBER

GCP RESPONSE OF ACTIVE MEMBER

FIG. 1 — D-Level Interrupt Printout

1. FROM STEP 3:
   6 RIGHTMOST OCTAL DIGITS
   ARE XX406011

2. FROM STEP 4:
   GCP K-CODE VALUE (BITS 6-8)
   IS OCTAL 2 (THIS BECOMES 7TH
   OCTAL DIGIT OF ADDRESS)

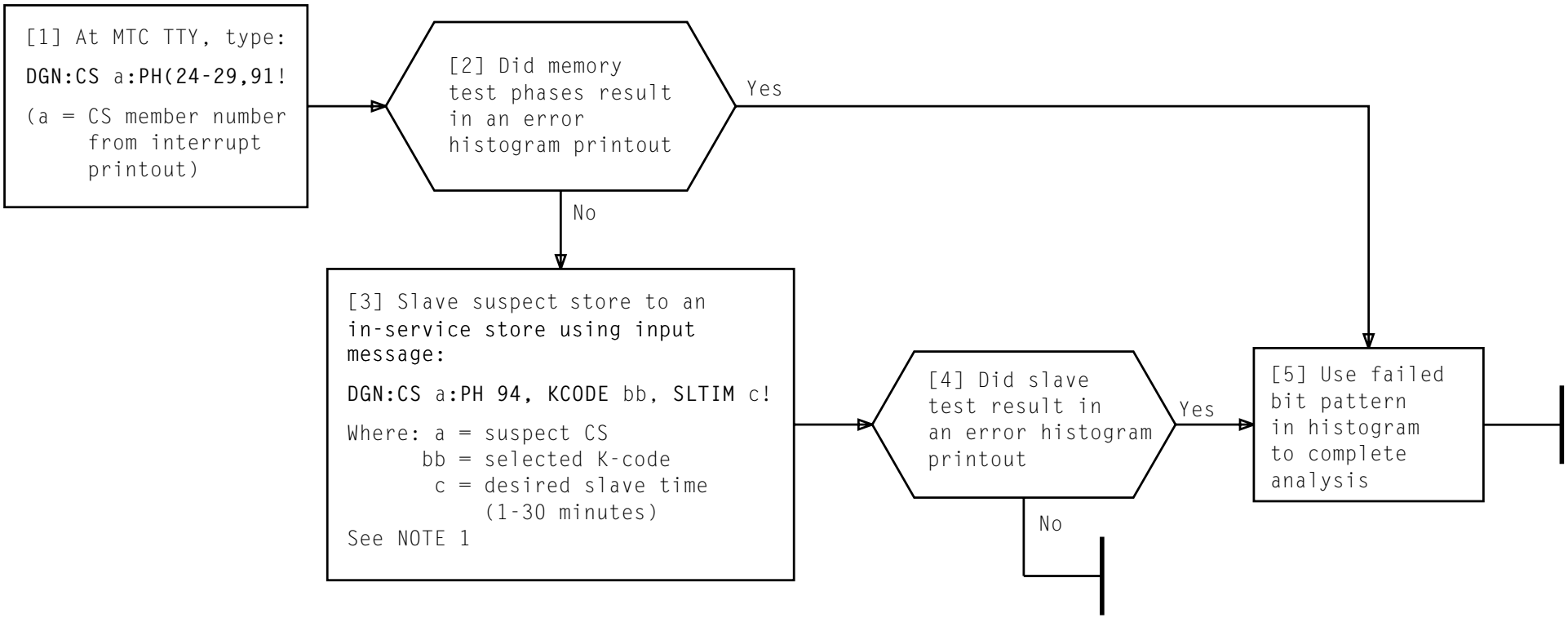
3. THE 8TH OCTAL DIGIT IS 0 BECAUSE UNIT IS A CALL STORE; THEREFORE, THE ADDRESS TO BE DUMPED IS: 02406011

EXAMPLE 1 — Determining Address To Be Dumped

```
DUMP:CS,ADR 02406011! PF, CODE 091
M 18 DUMP:CS,INDIR 0,ADR 02406011,INC +0 COMPLETED
    02406011 00600673        CONTENTS OF CR10
    #696                     BEFORE INTERRUPT
                             (BITS 12-15 MISMATCH)
```

EXAMPLE 2 — CR10 Dump

COMPARE CONTENTS OF FAILING CALL STORE ADDRESS USING VERIFY MESSAGE FOR DATA BIT MISMATCH



NOTE 1
Selected K-code should be normal office K-code that is assigned to only one in-service store and is other than base store or K-code 34

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OBTAIN HISTOGRAM USING CALL STORE MEMORY TEST/SLAVE TEST

At tape transport:

[1] Open interlocked cover door; at upper right of tape transport, pull interlock plunger out

[2] Depress **LOCAL/REMOTE** pushbutton to obtain **LOCAL** lighted condition

LOCAL lamp lights

[3] Verify empty lower (take-up) tape reel is same size or larger than tape reel to be mounted

[4] With hub (knob) of upper reel in counterclockwise position, mount reel with tape on reel holder

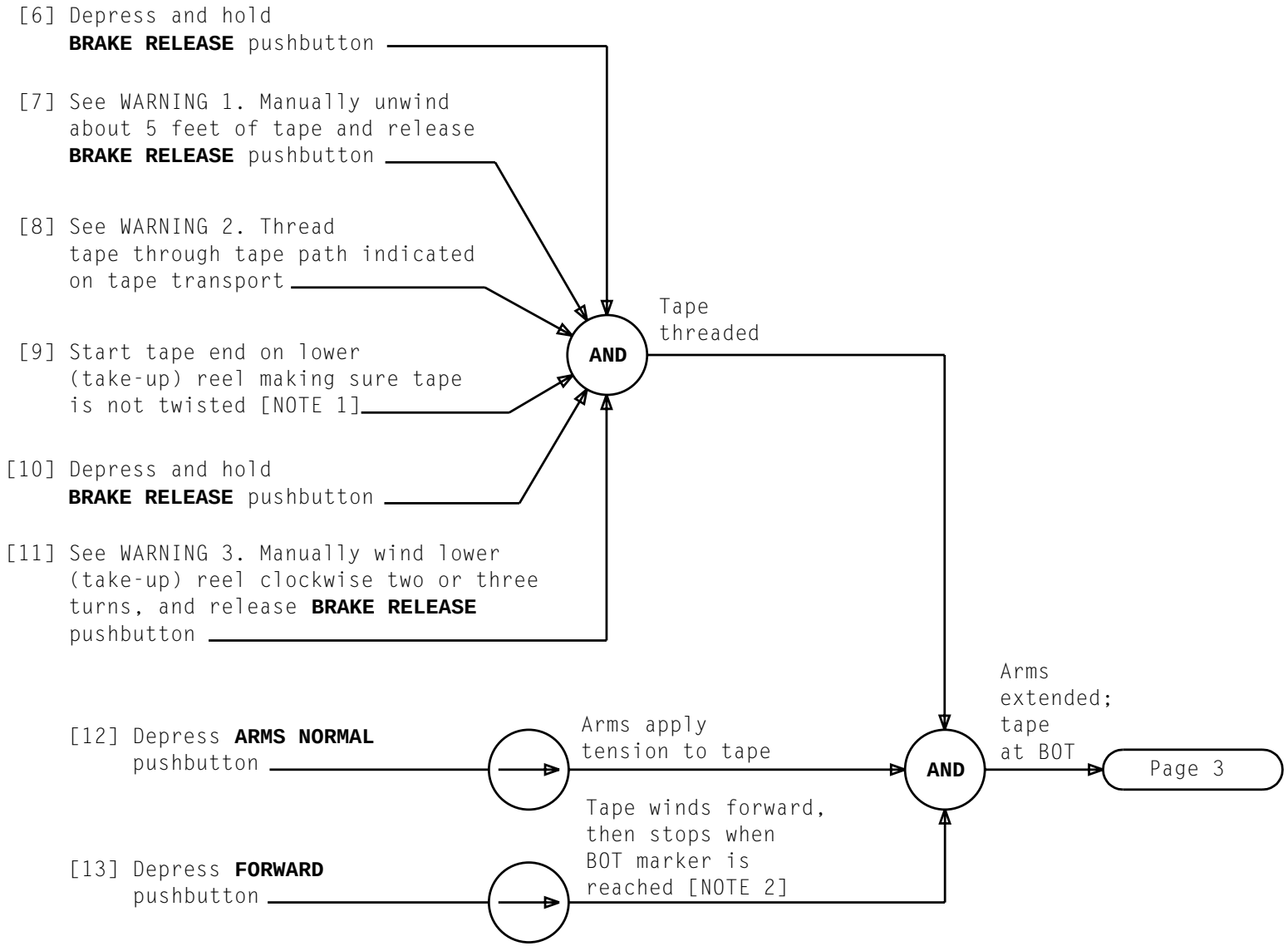
[5] Rotate hub (knob) of upper reel clockwise to detent to lock tape reel securely

AND

Tape reel and take-up reel mounted

Page 2

MOUNT TAPE ON TAPE TRANSPORT, 4ESS TAPE UNIT



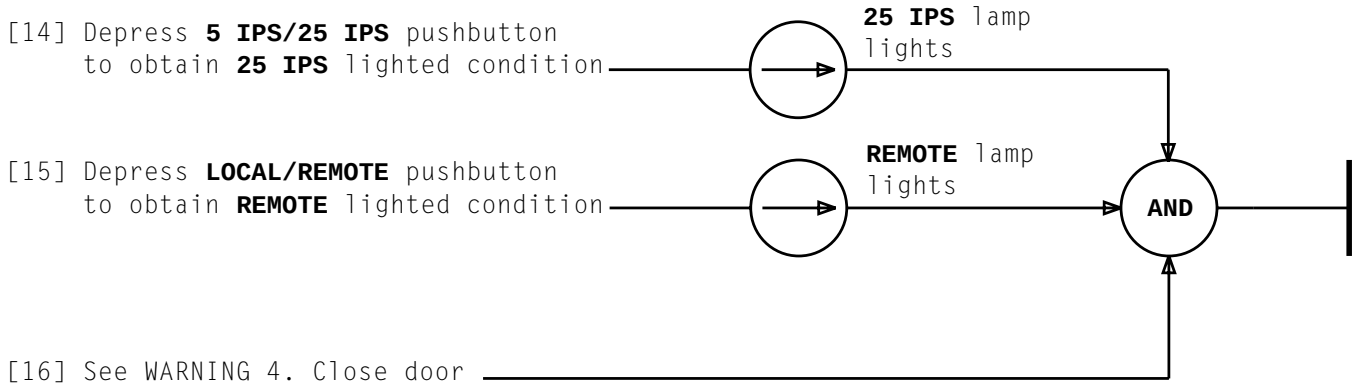
NOTES

1. To start tape on take-up reel, it may help to moisten the tape end (moistened fingers) and stick it to reel axle
2. Tape may not stop at BOT marker if **FAST FORWARD** is depressed

WARNINGS

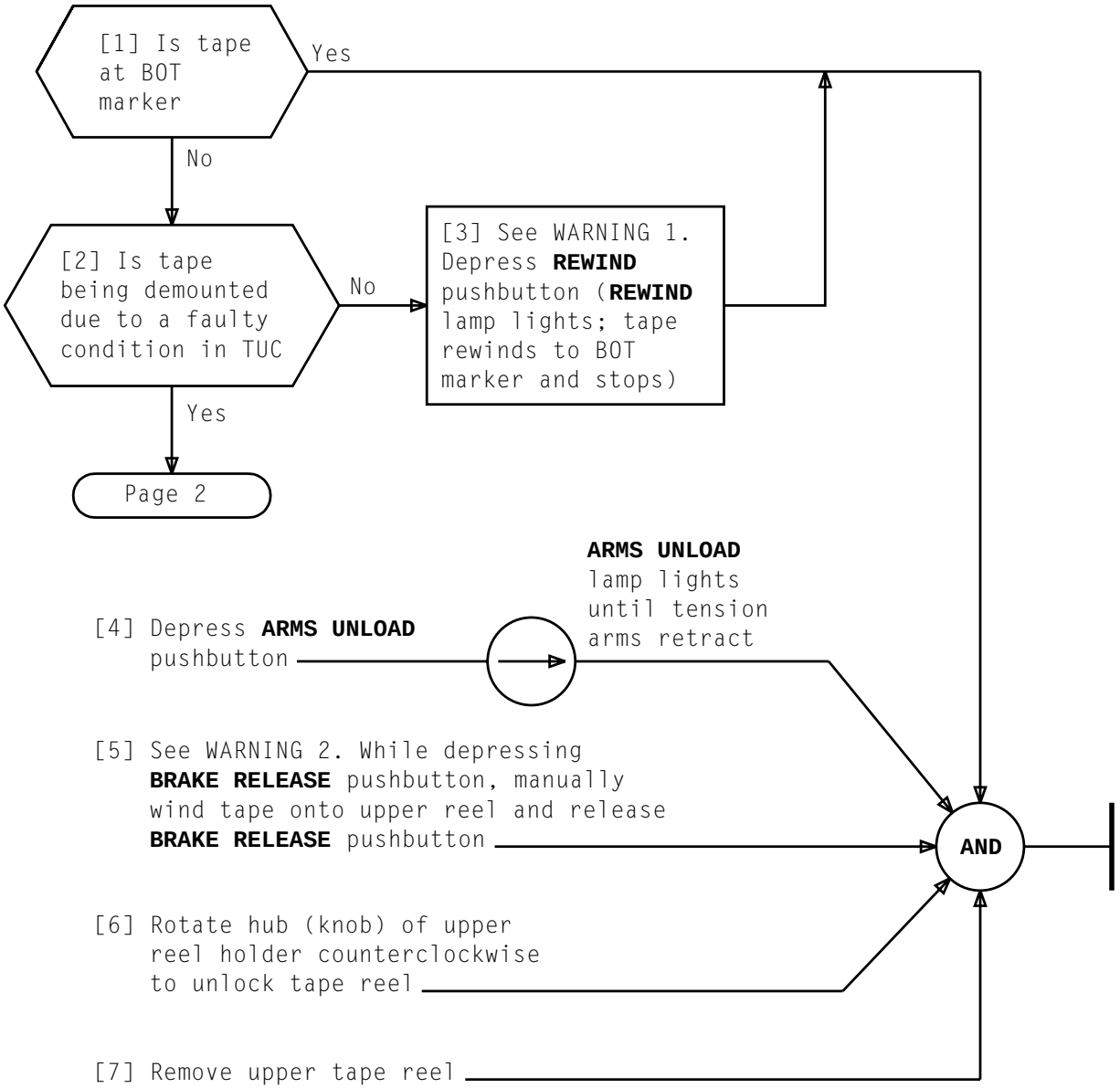
1. *Contamination of tape by contact with floor will damage tape heads*
2. *Do not touch tape head surfaces; body oils will contaminate tape*
3. *If tape is not properly aligned along rollers and guides or is too loose, it may be damaged*

MOUNT TAPE ON TAPE TRANSPORT, 4ESS TAPE UNIT



WARNING 4
Closing tape transport door in harsh manner may upset alignment

MOUNT TAPE ON TAPE TRANSPORT, 4ESS TAPE UNIT



WARNINGS

1. *If alignment tape is mounted, use* **REVERSE** *pushbutton to rewind tape*
2. *Pulling or dragging last 5 feet of tape across heads may contaminate heads*

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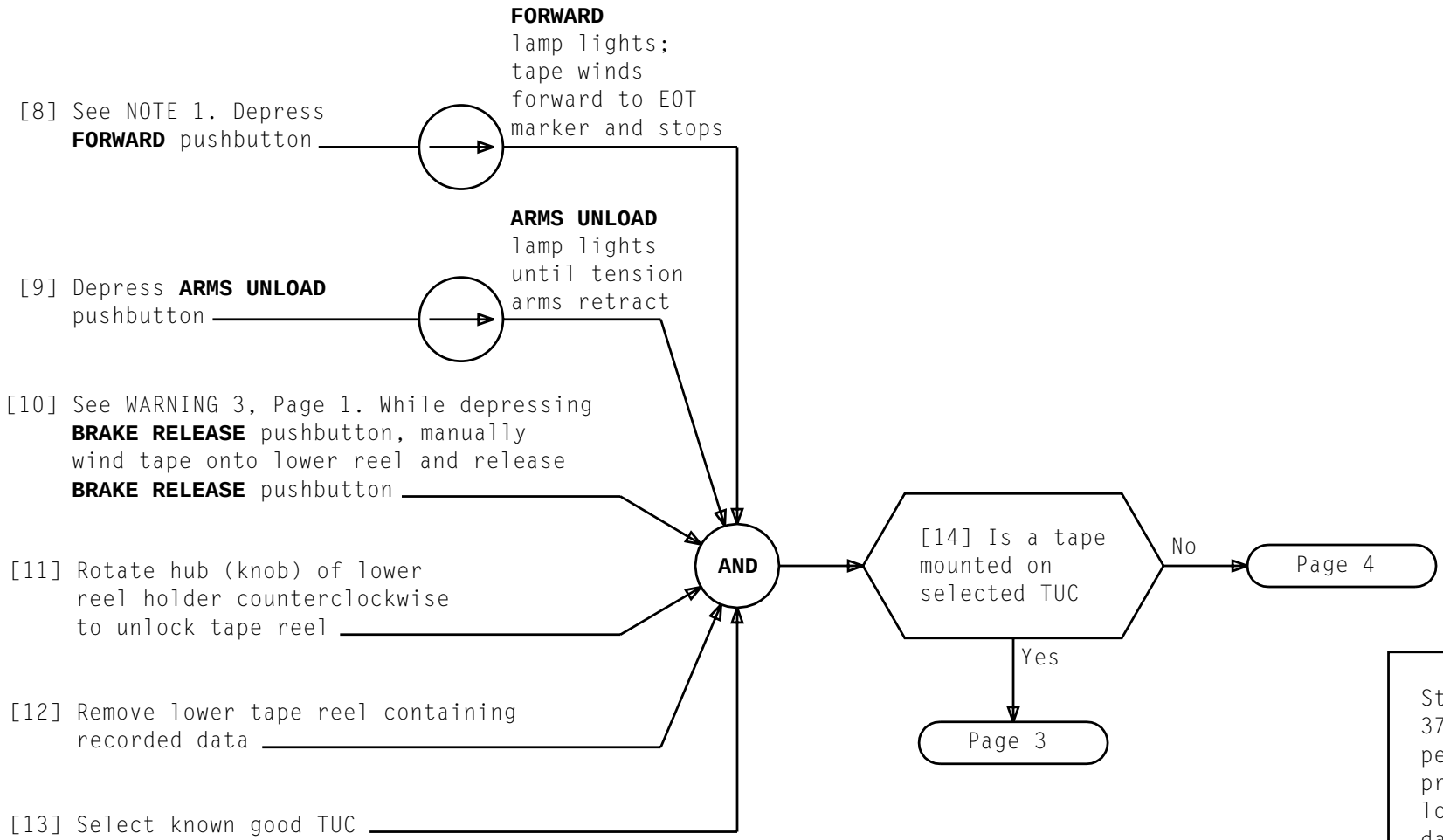
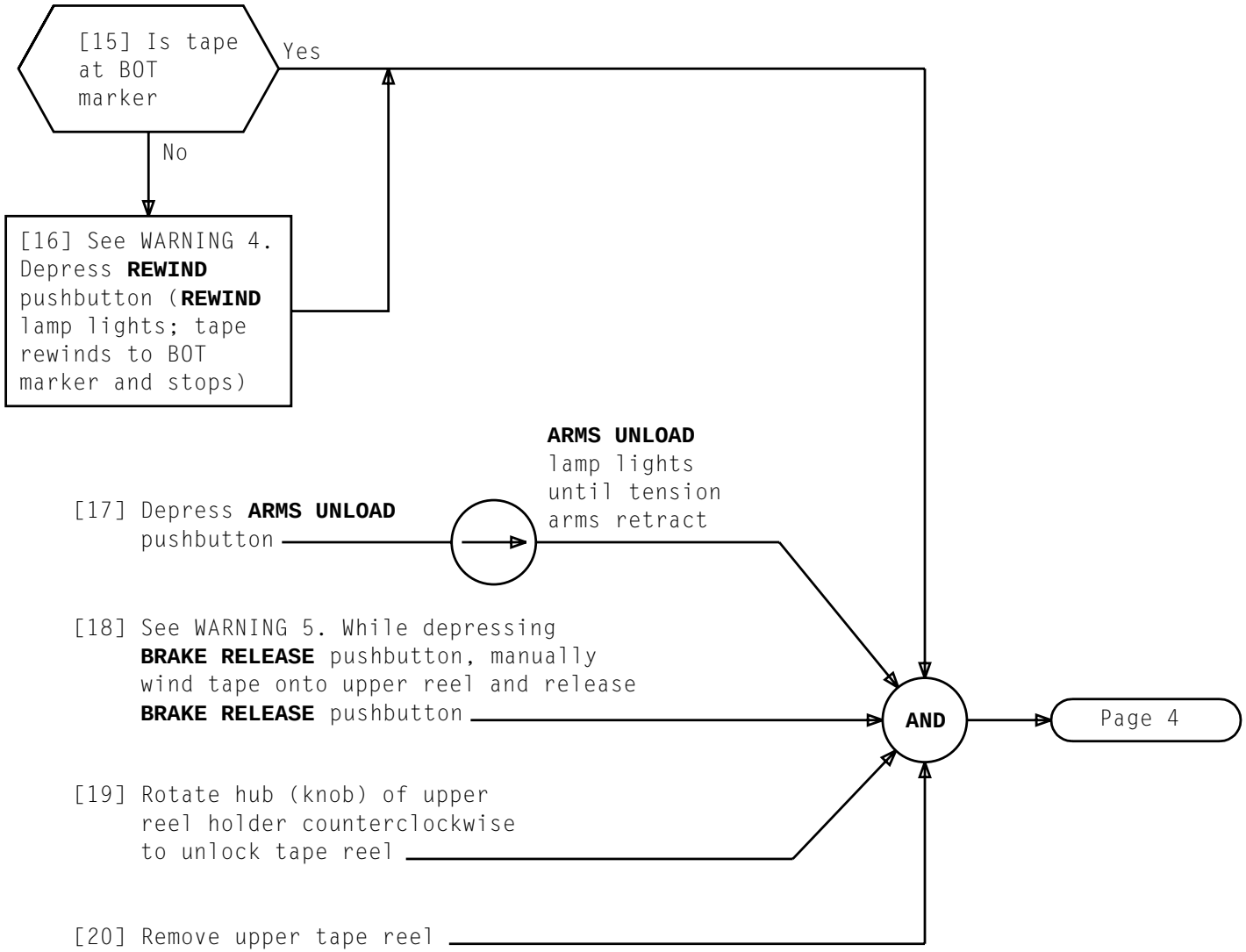
DEMOUNT TAPE ON 4ESS TAPE TRANSPORT



NOTE 1
Steps 8 through 37 are being performed to prevent possible loss of recorded data

WARNING 3
Pulling or dragging last 5 feet of tape across heads may contaminate heads

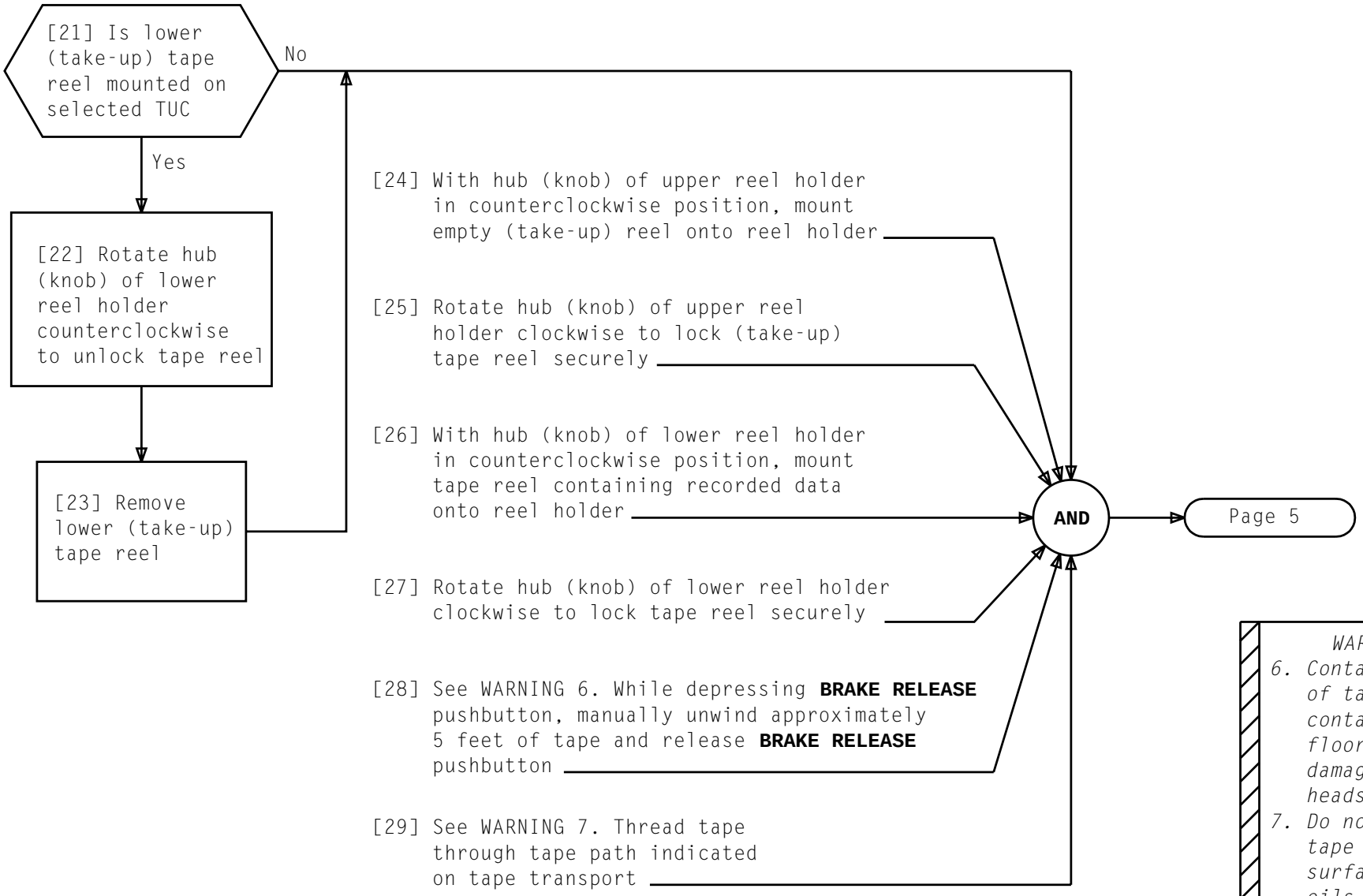
DEMOUNT TAPE ON 4ESS TAPE TRANSPORT



WARNINGS

4. *If alignment tape is mounted, use* **REVERSE** *pushbutton to rewind tape*
5. *Pulling or dragging last 5 feet of tape across heads may contaminate heads*

DEMOUNT TAPE ON 4ESS TAPE TRANSPORT



WARNINGS

6. Contamination of tape by contact with floor damages tape heads

7. Do not touch tape head surfaces; body oils contaminate tape

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DEMOUNT TAPE ON 4ESS TAPE TRANSPORT

[30] See NOTE 2. Start tape on upper (take-up) reel making sure tape is not twisted

[31] See WARNING 8. While depressing **BRAKE RELEASE** pushbutton, manually wind upper (take-up) reel three or four turns and release **BRAKE RELEASE** pushbutton

[32] Depress **ARMS NORMAL** pushbutton

ARMS NORMAL lamp lights until arms apply tension to tape

[33] Depress **REWIND** pushbutton

REWIND lamp lights; tape rewinds to BOT marker and stops

AND

[34] Depress **ARMS UNLOAD** pushbutton

ARMS UNLOAD lamp lights until tension arms retract

[35] See WARNING 9. While depressing **BRAKE RELEASE** pushbutton, manually wind tape onto upper reel and release **BRAKE RELEASE** pushbutton

[36] Rotate hub (knob) of upper reel holder counterclockwise to unlock tape reel

[37] Remove upper tape reel

AND

NOTE 2

To start tape on take-up reel, it may help to moisten tape end (moistened fingers) and stick tape to reel axle

WARNINGS

8. If tape is not properly aligned along rollers and guides or is too loose, it may be damaged

9. Pulling or dragging last 5 feet of tape across heads may contaminate heads

DEMOUNT TAPE ON 4ESS TAPE TRANSPORT

1. Note absolute address to be converted

2. Use address space map for applicable generic (PK4A002) and absolute address to identify pident and strip containing this address (for example: if address was 11261737, the pident would be FERACONT and the strip would be AD per Fig. 1)

3. Using octal arithmetic, subtract pident and strip starting address from absolute address to be converted [FIG. 2]

End of procedure

000C11254470	12	10	FERACOMM	DF	FERACOMM_AA
000C11254502	105	69	FERACOMM	DG	FERACOMM_AA
000C11254610	316	206	FERACOMM	DH	FERACOMM_AA
000C11255126	1042	546	FERACOMM	EA	FERACOMM_AA
000C11256170	267	183	FERACOMM	GE	FERACOMM_AA
000C11256460	2441	1313	FERACONT	AA	FERACONT_AA
000C11261122	254	172	FERACONT	AB	FERACONT_AA
000C11261376	156	110	FERACONT	AC	FERACONT_AA
000C11261554	401	257	FERACONT	AD	FERACONT_AA
000C11262156	136	94	FERACONT	AE	FERACONT_AA
000C11262314	76	62	FERACONT	AF	FERACONT_AA
000C11262412	66	54	FERACONT	AG	FERACONT_AA

FIG. 1 — Excerpt from Address Space Map

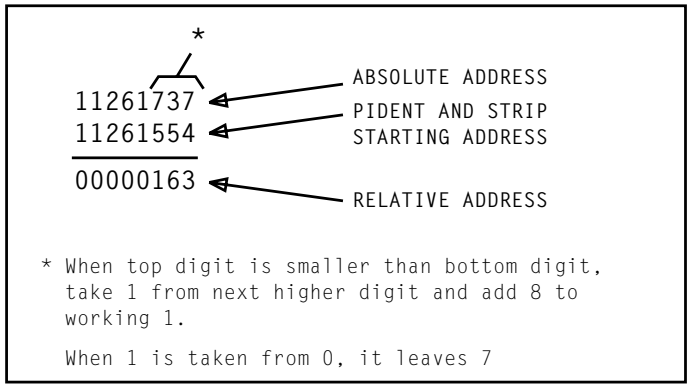


FIG. 2 — Sample of Absolute to Relative Address Conversion

CONVERT ABSOLUTE ADDRESS TO RELATIVE ADDRESS

1. Define error using PMDs [TABLE A]

TABLE A

PMD-006 Fault isolated by TNFRISAD. PMD indicates that one controller of suspect member failed access test. Controller which failed is suspect controller

PMD-007 Fault isolated by TNFRISAD. PMD indicates that both controllers failed access test. Each controller is assigned half weight indicating nonunique failure

PMD-010 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in only one controller; therefore, it is transient unique (AINT)

PMD-011 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in only one controller; therefore, it is hard unique (AINT)

PMD-012 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in one controller only; therefore, it is transient unique (AINT)

PMD-013 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in one controller only; therefore, it is hard unique (AINT)

PMD-020 Fault isolated by TNFRTMMN. This is a matched or nonunique type error which occurred in both controllers. Retry was performed and passed; therefore, it is transient nonunique (AINT)

PMD-021 Fault isolated by TNFRTMMN. This is a matched or nonunique type error which occurred in both controllers. Retry was performed and failed; therefore, it is hard nonunique (AINT)

PMD-050 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique fault which is up in only one controller; therefore, it is transient unique (ASWF)

PMD-051 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique fault which is up in only one controller; therefore, it is hard unique (ASWF)

PMD-052 Fault isolated by TNFRTMMN. This is a software type fault. This PMD indicates that software has caused a problem. Hardware is not suspected (ASWF)

PMD-053 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a unique type fault which occurred in both controllers; therefore, it is transient nonunique (ASWF)

PMD-054 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a unique type fault which occurred in both controllers

PMD-055 Fault isolated by TNFRTMMN. Retry was performed and passed. This is a match type fault which occurred in one controller only; therefore, it is transient unique (ASWF)

PMD-056 Fault isolated by TNFRTMMN. Retry was performed and failed. This is a match type fault which occurred in one controller only; therefore, it is is hard unique (ASWF)

DEFINE PMD DICTIONARY TNFR NODES, TIME MULTIPLEXED SWITCHING, TIME SLOT INTERCHANGE

TABLE A (Contd)

PMD-100 Fault isolated by TNFRTSMN. Fault type is unique class-1 transient (retry passed). Error is PFE,PFO,MODEF,RTSMPF,TTSMPF,BIMPF, or ASWF in only one controller when unit is simplex or duplex; or an RTSMA,TTSMA, or BIMA in only one controller when unit is duplex (ASWF)

PMD-101 Fault isolated by TNFRTSMN. Fault type is a unique class-1 hard (retry failed). Error is PFE,PFO, MODEF,RTSMPF,TTSMPF, BIMPF, or ASWF in only one controller when unit is simplex or duplex; or RTSMA, TTSMA,or BIMA in only one controller when unit is duplex (ASWF)

PMD-102 Fault isolated by TNFRTSMN. Fault type is unique soft. Error is MODEF in both controllers or RTSMA,TTSMA, or BIMA in both controllers if unit is duplex; or up in the in-service controller if unit is simplex (ASWF)

PMD-103 Fault isolated by TNFRTSMN. Fault type is unique transient (retry passed). Error is AMM,DWMM, or BIMWM in only one controller if unit is duplex; or up in the in-service controller if unit is simplex. BIMWM is not checked for CRTSI (ASWF)

PMD-104 Fault isolated by TNFRTSMN. Fault type is unique class-3 hard (retry failed). Error is AMM,DWMM, or BIMWM in only one controller if unit is duplex; or up in the in-service controller if unit is simplex. BIMWM is not checked for CRTS1 (ASWF)

PMD-105 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is PFE,PFO,RTSMPF,TTSMPF,BIMPF, or ASWF in both controllers (ASWF)

PMD-106 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is PFE, PFO,RTSMPF,TTSMPF,BIMPF, or ASWF in both controllers (ASWF)

PMD-150 Fault isolated by TNFRTSMN. Fault type is unique class-1 transient (retry passed). Error up in AINT error source register may be AINT only or SSWF or any error which has secondary registers (RTMP,TTMP,BIMP, RSW, or BMAPF) where no errors are up in secondaries

PMD-151 Fault isolated by TNFRTSMN. Fault type is unique class-1 hard (retry failed). Error up in AINT error source register may be AINT only or SSWF or any error which has secondary registers (RTMP,TTMP,BIMP,RSW, or BMAPF) where no errors are up in secondaries

PMD-152 Fault isolated by TNFRSTMN. Fault type is unique class-2 transient (retry passed). Error in AINT error source register may be CE or TSSC in only one controller with errors up in secondary registers

PMD-153 Fault isolated by TNFRTSMN. Fault type is unique class-2 hard (retry failed). Error in AINT error source register may be CE or TSSC in only one controller or RTMP,TTMP,BIMP,RSW,BMAPF, or TSW in only one controller with errors in secondary register

PMD-160 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed — both controllers). Error in AINT error source register or sense and and lock register may be AINT only, CE,SSWF, or TSSC in both controllers or RIMP,TIMP,BIMP, or BMBPF in both controllers with errors up in secondaries

TABLE A (Contd)

PMD-161 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed — either controller). Error in AINT error source register or sense and lock register may be AINT only, CE, SSWF, or TSSC in both controllers or RTMP,TTMP,BIMP, or BMBPF in both controllers with errors up in secondaries

PMD-170 Fault isolated by TNFRTSMN. Either a receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in only one controller. The error is partitionable and a retry of the failing controller has failed. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-2 hard fault

PMD-171 Fault isolated by TNFRTSMN. Either a receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in only one controller. The error is partitionable and a retry of the failing controller has passed. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-2 transient fault

PMD-172 Fault isolated by TNFRTSMN. A receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in both controllers. One or both of the controllers have failed the retry. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-4 hard failure

PMD-173 Fault isolated by TNFRTSMN. A receive or transmit time slot memory parity failure has been detected in the AINT and/or SAL error source registers in both controllers. Both of the controllers have passed the retry. The AUX data block provides the K-code of the suspect unit and the failing level. This is a class-4 transient failure

PMD-207 Fault isolated by TNFRTSMN. Fault is either TRPF, TMM, or TSW. The channel is busy to a time slot. In attempting to trace the call through the network, a mismatch in the TSM data was found in the RTSI. An RTMP error was then found in the RTSI AINT ESR. Suspect frame is changed to RTSI and fault isolation reentered

PMD-210 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. A path was found back to RTSI. RTSI has some error source bits set. Suspect frame is changed to RTSI and fault isolation reentered

PMD-211 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, the network routine (NTRO) for one controller is incorrect. Fault is treated as unique error. AUX data block has more information

PMD-212 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, TTSM memory did not have appropriate data. AUX data block has more information. Fault is treated as unique error

TABLE A (Contd)

PMD-213 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, TTSM information from two controllers did not agree. Fault is treated as nonunique error. AUX data block has more information

PMD-214 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one TMS controller failed to pass access test. AUX data block has information. This TMS controller is treated as unique fault

PMD-215 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, both TMS controllers failed to pass access test. Fault is treated as nonunique TMS fault. AUX data block has more information

PMD-216 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call though network, mismatch in data stored in TSM memory was found. AUX data block has more information. Fault is treated as TMS nonunique error

PMD-217 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, cutoff or multiple path has been found in TMS. AUX data block has more information. Fault is treated as software fault

PMD-220 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, it was found RTSI duplex failed. AUX data block has more information. Fault is treated by letting ERAT attempt to take out RTSI

PMD-221 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one RTSI controller failed access test. AUX data block has more information. Fault is treated as unique RTSI fault

PMD-222 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, both RTSI controllers failed access tests. More information in AUX data block. Fault is treated as nonunique RTSI fault

PMD-223 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, broken or multiple path found in or multiple path found in RTSI. AUX data block has more information. Fault is treated as RTSI software fault

PMD-224 Fault isolated by TNFRXMIT. Fault type is either TRPF,TMM, or TSW. Channel is busy to time slot. In attempting to trace call through network, mismatch in TMS routing F/F was found. AUX data has more information. Fault is treated as RTSI nonunique fault

TABLE A (Contd)

PMD-225 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, one TRSI controller has incorrect network routing.
C AUX data has more information. Fault is treated as TRSI unique fault

PMD-226 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Channel is busy to a time slot. In attempting to trace call through network, mismatch in TSM data in RTSI was found. AUX data has more information. Fault is treated as RTSI nonunique fault

PMD-227 Fault isolated by TNFRMIT. Fault is either TRPF, TMM, or TSW. The channel is busy to a time slot. In attempting to trace the call through the network, a broken or multiple path was found in the RTSI. An RTMP error was then found in the RTSI AINT ESR. Suspect frame is changed to the RTSI and fault isolation reentered

PMD-230 Fault isolated by TNFRXMIT. Fault type is TRPF, TMM, or TSW with no corresponding secondary ESR bits set. Fault is probably in indicated controller ESRS

PMD-231 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error in both controllers but channel on which error occurred is not involved in network path. Therefore, fault is in this unit but is transient because retry passed. Fault may be in recorrelator or involve BUFC memory but cannot be isolated to controller

PMD-232 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error in both controllers but channel on which error occurred is not involved in network path. Therefore, fault is in this unit and is hard because retry failed. Fault may be in recorrelator or involve BUFC memory but cannot be isolated to unique controller

PMD-233 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy idle memory map bits against TS memory was run. Check found that suspect contoller has mismatch between time-slot memory information and BIMM information. Information not found in other controller. Therefore, BIMM or TTSM in suspect controller may be at fault

PMD-234 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy-idle memory map bits against TS memory was run. Check found mismatch in data between two controllers which is attributable to controller fault but cannot be further isolated to unique controller. BIMM or TTSM in one of two controllers is suspect

PMD-235 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of busy-idle memory map bits against TS memory was run. Check has found data between controllers to match but BIMM data and TS data does not correlate. Therefore, error is probably result of software error

TABLE A (Contd)

PMD-236 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of BIMM and TTSM information passed. Recorrelator tested and both controllers failed. Problem may be in cross controller matchers and is treated as nonunique

PMD-237 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Error of BIMM and TTSM information passed. Recorrelator tested and one controller failed. Fault is in recorrelator or associated circuits and is treated as unique fault

PMD-240 Fault isolated by TNFRXMIT. Fault type is TMM or TSW error occurring in both controllers. Check of BIMM and TTSM information passed. Recorrelator tested and both controllers passed. Since failing channel is not involved in network path, no more testing can be done and fault must be in failing frame. Fault is treated as nonunique

PMD-241 Fault isolated by TNFRXMIT. Fault type is either TRPF, TMM, or TSW. Path was found on failing time slot. Attempts made to isolate fault to one of six possible controllers by reconfiguring network routing. AUX data block has more information. Error was not isolated and must be considered nonunique. Final suspect list which is passed on to error analysis is found in AUX data block

PMD-242 Fault isolated by TNFRXMIT. Error is unresolvable TRPF. Request controller restore.

PMD-243 Fault isolated by TNFRXMIT. Error is a hard unique TRPF. Request controller removed to listen only and request a diagnostic on the controller.

PMD-250 Fault isolated by TNFRXMIT. Fault type is hard RSW (retry failed). Fault is probably not in TSI recording error but in transmission subunit connected to interrupting port. AUX data block has details of interrupting ports

PMD-251 Fault isolated by TNFRXMIT. Fault type is transient RSW (retry passed). Fault is probably not in TSI recording error, but in transmisson subunit connected to interrupting ports. AUX data block has details of interrupting ports

PMD-300 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to change state of BMA port pest has failed

PMD-301 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to change state of HFIS bit in hardware status register has failed

PMD-302 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Attempt to reset FS and FE bits of hardware status register has failed

PMD-303 Fault isolated by TNFRMMRT. Fault type is unique software error. Mismatch between controllers of data in critical register dump at time of interrupt. Either HFIS bit of hardware status word (for non-CRTSI only) or port pests do not match or software state and CREG value of port pests do not match

PMD-304 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. RMM,BMAPF, or BMBPF BMBPF error not detected in SAL registers for either controller after both registers were cleared and unit was allowed to autonomously cycle

TABLE A (Contd)

PMD-305 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. Network connection from failing channel in BMA to maintenance channel in BMD made. Data received in BMD does not match data sent from BMA for both controllers

PMD-306 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Network connection from failing channel in BMA to maintenance channel in BMD made. Data received in BMD does not match data sent from BMA for one controller

PMD-307 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. Attempt to make connection across the network failed.

PMD-310 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. Loop-around connection of network made. Data received in maintenance channel of BMD matches data sent through failing channel of BMA or both controllers

PMD-311 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 transient. Loop-around connection of network made. Data received in maintenance channel of BMD does not match data sent through failing channel of BMA for both controllers

PMD-312 Fault isolated by TNFRMMRT. Fault type is unique class-3 hard. Loop-around connection of network has been made. Data received in maintenance channel of BMD does not match data sent through failing channel of BMA for one controller

PMD-313 Fault isolated by TNFRMMRT. Fault type is nonunique class-3 hard. No test made. Attempt to make loop-around connection of network failed

PMD-360 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is BIMWM up in both controllers

PMD-361 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard transient (retry passed). Error is AMM in both controllers

PMD-362 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is AMM in both controllers

PMD-363 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is AMM in both controllers

PMD-364 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 transient (retry passed). Error is DWMM in both controllers

PMD-365 Fault isolated by TNFRTSMN. Fault type is nonunique class-4 hard (retry failed). Error is DWMM in both controllers

PMD-366 Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (MWM) Retry performed and passed; therefore, it is transient nonunique (ASWF)

PMD-367 Fault isolated by TNFRTMMN. Match type error which occurred in both controllers; (MWM) therefore, it is hard unique (ASWF)

PMD-370 Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (AMM) Retry performed and passed; therefore, it is transient nonunique (ASWF)

PMD-371 Fault isolated by TNFRTMMN. Match type error which occurred in both controllers. (AMM) Retry performed and failed; therefore, it is hard nonunique (ASWF)

1. See FIG. 1 and EXAMPLE 1. Check contents of CREG 3

2. Convert octal data to binary

3. Regroup bits 7-13 starting at bit 7 and grouping from right to left

4. Convert binary bits back to octal. This is the memory number

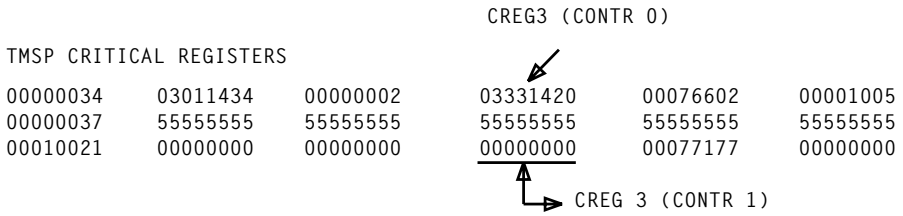


FIG. 1 – TMS ESR+1 Register

ESR+1 DATA	0			3			3			3			1			4			2			0		
BINARY	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0
REGROUPED											1	1	0	0	1	1	0							
RECONVERTED OCTAL VALUE											* 1		4			6								

* INDICATES BAY (0 OR 1)

EXAMPLE 1 – Determine Memory Number

IDENTIFY SUSPECT MEMORY AND MEMORY REGISTER CIRCUIT PACKS, TIME MULTIPLEXED SWITCHING

[1] Using bit set in CREG 20/21 (if TSI-B), determine SPC and level from TABLE A

[2] Extract octal time slot from bits 17-19 in CREG 3 [TABLE B]

[3] Use time slot to determine SLIP [TABLE C and Step 2]

[4] Use SLIP and TSWF TMM level [Step 1] to determine BMC level from TABLE D

[5] Use BMC level and SPC [Step 1] to obtain list of primary suspect circuit packs listed in TABLE E, Page 2

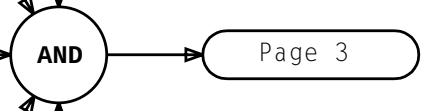


TABLE B
TIME SLOT EXTRACTION

CREG 3 OCTAL DATA	7			3			0		
BIT POSITION	23	22	21	20	19	18	17	16	15
BINARY EQUIVALENT	1	1	1	0	1	1	0	0	0
OCTAL TIME SLOT					1	1	0	=	6

TABLE C

OCTAL TIME SLOT (MOD 8)	0	1	2	3	4	5	6	7
SLIP	4	5	6	7	0	1	2	3

TABLE D

SLIP		0	1	2	3	4	5	6	7	
TSWF LEVEL	0	0	1	2	3	4	5	6	7	BMC
	1	1	2	3	4	5	6	7	0	
	2	2	3	4	5	6	7	0	1	
	3	3	4	5	6	7	0	1	2	
	4	4	5	6	7	0	1	2	3	
	5	5	6	7	0	1	2	3	4	
	6	6	7	0	1	2	3	4	5	
	7	7	0	1	2	3	4	5	6	

TABLE A
BMB, SPC, AND LEVEL

CREG	SPC								SPC							
20 21	1 3								0 2							
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

DETERMINE F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING TABLES

TABLE E
SUSPECT BMC CIRCUIT PACK LOCATIONS

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
		FA1190	50-57	50-56	50-55	50-54	50-53	50-52	50-51	50-50
	1	FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
		FA1190	72-57	72-56	72-55	72-54	72-53	72-52	72-51	72-50
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
		FA1784	28-26	28-26	28-21	28-21	28-12	28-12	28-07	28-07
		FA1785	28-15	28-15	28-15	28-15	28-14	28-14	28-14	28-14
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
		FA1784	40-26	40-26	40-21	40-21	40-12	40-12	40-07	40-07
		FA1785	40-15	40-15	40-15	40-15	40-14	40-14	40-14	40-14
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
		FA1784	52-26	52-26	52-21	52-21	52-12	52-12	52-07	52-07
		FA1785	52-15	52-15	52-15	52-15	52-14	52-14	52-14	52-14
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
		FA1784	64-26	64-26	64-21	64-21	64-12	64-12	64-07	64-07
		FA1785	64-15	64-15	64-15	64-15	64-14	64-14	64-14	64-14

*FA1781 could be FA1817

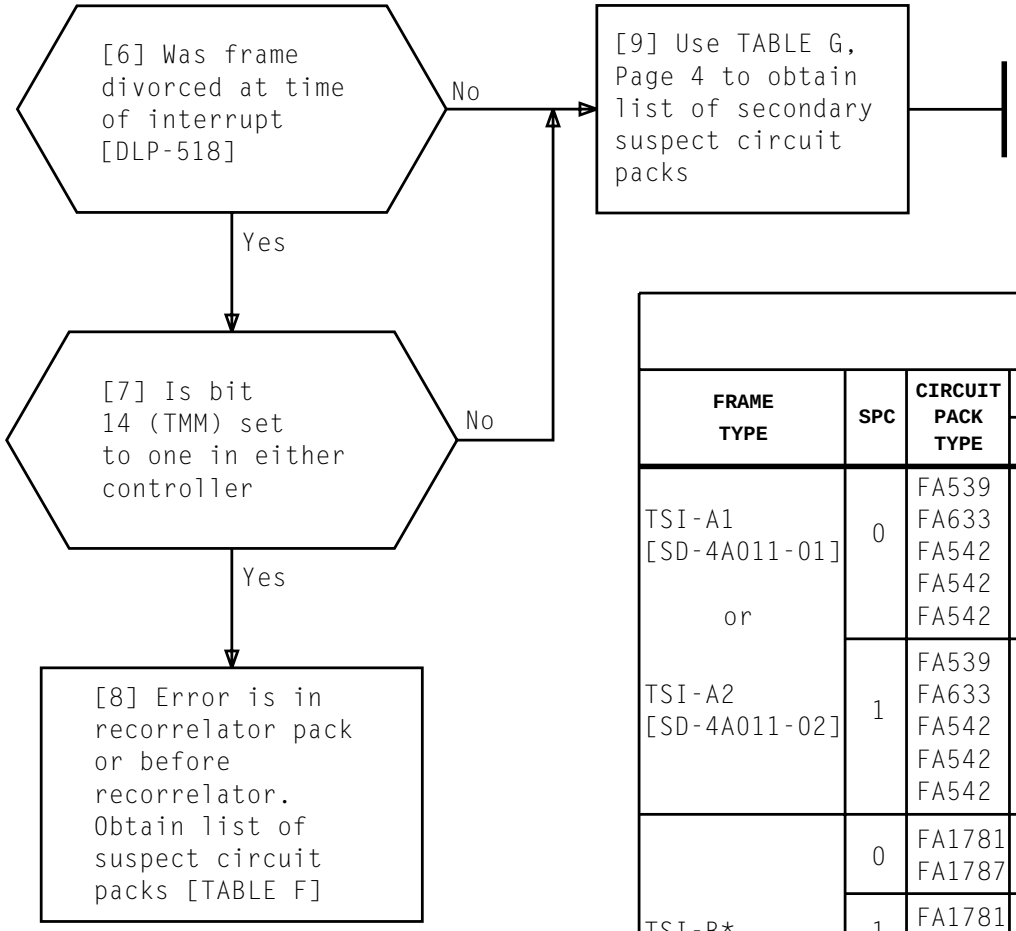


TABLE F
SUSPECT BMC CIRCUIT PACKS (BIT 14)

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA539	38-56	38-55	38-54	38-53	38-52			
		FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
	1	FA539	60-56	60-55	60-54	60-53	60-52			
		FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1787	28-29	28-29	28-29	28-29	28-29	28-29	28-29	28-29
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1787	40-29	40-29	40-29	40-29	40-29	40-29	40-29	40-29
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1787	52-29	52-29	52-29	52-29	52-29	52-29	52-29	52-29
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1787	64-29	64-29	64-29	64-29	64-29	64-29	64-29	64-29

*FA1781 could be FA1817

DETERMINE F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING TABLES

TABLE G
SUSPECT CIRCUIT PACK LOCATIONS FOR ESR BIT 11

FRAME TYPE	SPC	CIRCUIT PACK TYPE	LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA571 FB220	38-50 38-45	38-50 38-45	38-49 38-44	38-49 38-44	38-48 38-43	38-48 38-43	38-46 38-42	NA
	1	FA571 FB220	60-50 60-45	60-50 60-45	60-49 60-44	60-49 60-44	60-48 60-43	60-48 60-43	60-46 60-42	NA
TSI-B [SD-4A083-01]	0	FA1790 FA1789 FA1787	24-32 28-34 28-29	24-31 28-34 28-29	24-29 28-34 28-29	24-28 28-34 28-29	24-26 28-34 28-29	24-24 28-34 28-29	24-23 28-33 28-29	24-22 28-33 28-29
	1	FA1790 FA1789 FA1787	36-32 40-34 40-29	36-31 40-34 40-29	36-29 40-34 40-29	36-28 40-34 40-29	36-26 40-34 40-29	36-24 40-34 40-29	36-23 40-33 40-29	36-22 40-33 40-29
	2	FA1790 FA1789 FA1787	48-32 52-34 52-29	52-31 52-34 52-29	48-29 52-34 52-29	48-28 52-34 52-29	48-26 52-34 52-29	48-24 52-34 52-29	48-23 52-33 52-29	48-22 52-33 52-29
	3	FA1790 FA1789 FA1787	60-32 64-34 64-29	60-31 64-34 64-29	60-29 64-34 64-29	60-28 64-34 64-29	60-26 64-34 64-29	60-24 64-34 64-29	60-23 64-33 64-29	NA

Using TTY printout and TABLE A, examine registers [FIG. 1] for both controllers to determine the following:

NOTE: If frame is divorced, ignore error bits in OOS controller. Use Error Source Registers for in-service controller only

1. Determine if frame is operating in DUPLEX (not divorced) or SIMPLEX (divorced) mode

2. Determine OOS controller (if any)

NOTE: A TRPF may occur where the TRPF traces back to receive TSI; in this case, CREG 2 could contain all zeros

3. Determine type of error (APUF or PUF)

4. If APUF, check for TRPF (AUX. DATA Reg 0 contains 0' 174 or 175 value), or if bit 10 is set to one in either CREG 3 (AINT REG) or CREG 4 (Sense and lock REG)

TABLE A

STEP NUMBER	REGISTER AND BIT POSITION	BIT VALUE	INDICATION
* [1]	CREG 0, BIT 4	0	Frame is not divorced (in DUPLEX operating mode)
		1	Frame is divorced (in SIMPLEX operating mode)
[2]	CREG 0, BIT 0	0	Controller is in service
		1	Controller is OOS
† [3]	CREG 2, BIT 0	1	Error type is PUF
†	GREG 2, BIT 1	1	Error type is APUF
[4]	AUX. DATA REG. 0	0'174	Transmit parity failure (TRPF)
	CREG 3, BIT 10	1	
	CREG 4, BIT 10	1	

* If bit 4 is not set to same value in both controllers, suspect a software error and notify PECC

† If bits 0 and 1 are set to one, treat as PUF

DETERMINE TYPE OF ERROR AND MODE OF FRAME OPERATION, F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE

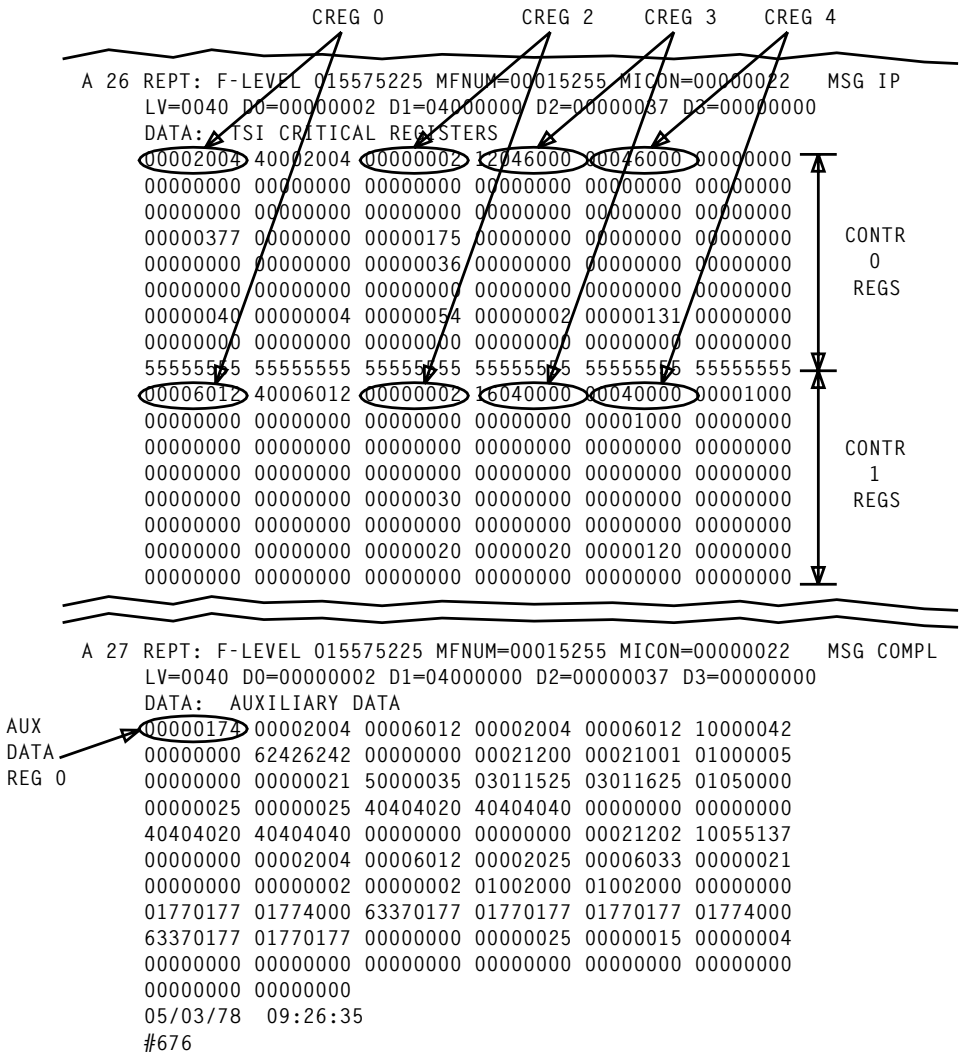


FIG. 1 - Part of F-Level Register Dump

DETERMINE TYPE OF ERROR AND MODE OF FRAME OPERATION, F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE

[1] Using bit set in CREG 20/21 (if TSI-B), determine SPC and level from TABLE A

[2] Extract octal time slot from bits 17-19 in CREG 3 [TABLE B]

[3] Add 4 to octal time slot

[4] Add result to level obtained in Step 1

[5] Use rightmost digit as BMC level and SPC obtained in Step 1 to obtain primary list of suspect circuit packs listed in TABLE C, Page 2

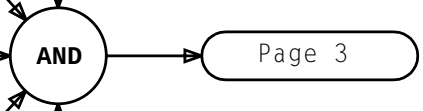


TABLE A
SPC AND LEVEL

CREG	SPC								SPC							
20 21	1 3								0 2							
BIT	15	14	13	12	11	10	09	08	07	06	0 5	04	03	02	01	00
LEVEL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

TABLE B
TIME SLOT EXTRACTION

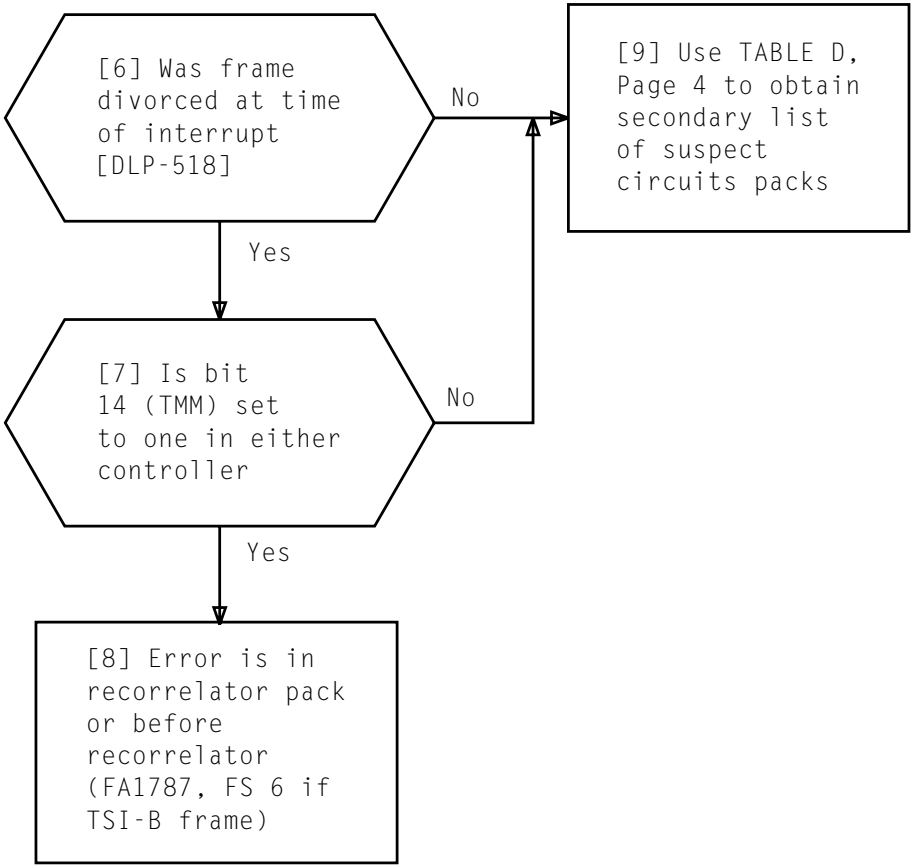
CREG 3 OCTAL DATA	7			3			0		
BIT POSITION	23	22	21	20	19	18	17	16	15
BINARY EQUIVALENT	1	1	1	0	1	1	0	0	0
OCTAL TIME SLOT				1	1	0	=	6	

DETERMINE F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING FORMULA

TABLE C
SUSPECT BMC CIRCUIT PACK LOCATIONS

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01] or TSI-A2 [SD-4A011-02]	0	FA633	46-57	46-56	46-55	46-54	46-53	46-52	46-51	46-50
		FA542	42-59	42-59	42-59	42-59	42-56	42-56	42-56	42-56
		FA542	42-58	42-58	42-58	42-58	42-55	42-55	42-55	42-55
		FA542	42-57	42-57	42-57	42-57	42-54	42-54	42-54	42-54
		FA1190	50-57	50-56	50-55	50-54	50-53	50-52	50-51	50-50
	1	FA633	68-57	68-56	68-55	68-54	68-53	68-52	68-51	68-50
		FA542	64-59	64-59	64-59	64-59	64-56	64-56	64-56	64-56
		FA542	64-58	64-58	64-58	64-58	64-55	64-55	64-55	64-55
		FA542	64-57	64-57	64-57	64-57	64-54	64-54	64-54	64-54
		FA1190	72-57	72-56	72-55	72-54	72-53	72-52	72-51	72-50
TSI-B* [SD-4A083-01]	0	FA1781	28-24	28-23	28-19	28-17	28-10	28-09	28-05	28-04
		FA1783	28-28	28-28	28-28	28-28	28-28	28-28	28-28	28-28
		FA1784	28-26	28-26	28-21	28-21	28-12	28-12	28-07	28-07
		FA1785	28-15	28-15	28-15	28-15	28-14	28-14	28-14	28-14
	1	FA1781	40-24	40-23	40-19	40-17	40-10	40-09	40-05	40-04
		FA1783	40-28	40-28	40-28	40-28	40-28	40-28	40-28	40-28
		FA1784	40-26	40-26	40-21	40-21	40-12	40-12	40-07	40-07
		FA1785	40-15	40-15	40-15	40-15	40-14	40-14	40-14	40-14
	2	FA1781	52-24	52-23	52-19	52-17	52-10	52-09	52-05	52-04
		FA1783	52-28	52-28	52-28	52-28	52-28	52-28	52-28	52-28
		FA1784	52-26	52-26	52-21	52-21	52-12	52-12	52-07	52-07
		FA1785	52-15	52-15	52-15	52-15	52-14	52-14	52-14	52-14
	3	FA1781	64-24	64-23	64-19	64-17	64-10	64-09	64-05	64-04
		FA1783	64-28	64-28	64-28	64-28	64-28	64-28	64-28	64-28
		FA1784	64-26	64-26	64-21	64-21	64-12	64-12	64-07	64-07
		FA1785	64-15	64-15	64-15	64-15	64-14	64-14	64-14	64-14

*FA1781 could be FA1817



DETERMINE F-LEVEL INTERRUPT, TIME SLOT INTERCHANGE BUFFER MEMORY C (BMC) USING FORMULA

TABLE D
SUSPECT CIRCUIT PACK LOCATIONS FOR ESR BITS 11

FRAME TYPE	SPC	CIRCUIT PACK TYPE	BMC LEVEL							
			0	1	2	3	4	5	6	7
TSI-A1 [SD-4A011-01]	0	FA571 FB220	38-50 38-45	38-50 38-45	38-49 38-44	38-49 38-44	38-48 38-43	38-48 38-43	38-46 38-42	NA
TSI-A2 [SD-4A011-02]	1	FA571 FB220 FB639	60-50 60-45	60-50 60-45	60-49 60-44	60-49 60-44	60-48 60-43	60-48 60-43	60-46 60-42	NA
TSI-B [SD-4A083-01]	0	FA1790 FA1789 FA1787	24-32 28-34 28-29	24-31 28-34 28-29	24-29 28-34 28-29	24-28 28-34 28-29	24-26 28-34 28-29	24-24 28-34 28-29	24-23 28-33 28-29	24-22 28-33 28-29
	1	FA1790 FA1789 FA1787	36-32 40-34 40-29	36-31 40-34 40-29	36-29 40-34 40-29	36-28 40-34 40-29	36-26 40-34 40-29	36-24 40-34 40-29	36-23 40-33 40-29	36-22 40-33 40-29
	2	FA1790 FA1789 FA1787	48-32 52-34 52-29	48-31 52-34 52-29	48-29 52-34 52-29	48-28 52-34 52-29	48-26 52-34 52-29	48-24 52-34 52-29	48-23 52-33 52-29	48-22 52-33 52-29
	3	FA1790 FA1789 FA1787	60-32 64-34 64-29	60-31 64-34 64-29	60-29 64-34 64-29	60-28 64-34 64-29	60-26 64-34 64-29	60-24 64-34 64-29	60-23 64-33 64-29	NA

1. Define error using PMDs [TABLE A]

TABLE A

PMD-1	Growth unit
PMD-2	Soft error configuration was duplex controllers
PMD-3	Soft error configuration was simplex controller 0
PMD-4	Soft error configuration was simplex controller 1
PMD-5	Transient error configuration was duplex controllers
PMD-6	Transient error configuration was simplex controller 0
PMD-7	Transient error configuration was simplex controller 1
PMD-10	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-11	Bus at unit fault configuration was duplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-12	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-13	Bus at unit fault configuration was duplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect
PMD-14	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-15	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-16	Bus at unit fault configuration was duplex controllers; simplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-17	Bus at unit fault configuration was duplex controllers; simplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-20	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 0 suspect
PMD-21	Bus at unit fault configuration was simplex controllers; duplex bus controller 0 and minor bus (IPUB) 1 suspect
PMD-22	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 0 suspect
PMD-23	Bus at unit fault configuration was simplex controllers; duplex bus controller 1 and minor bus (IPUB) 1 suspect
PMD-24	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 0 suspect
PMD-25	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 0 and minor bus (IPUB) 1 suspect
PMD-26	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 0 suspect
PMD-27	Bus at unit fault configuration was simplex controllers; duplex PUB, simplex bus at unit CONTR 1 and minor bus (IPUB) 1 suspect
PMD-30	PUB fault configuration was duplex; bus major bus 0 suspect
PMD-31	PUB fault configuration was duplex; bus major bus 1 suspect
PMD-32	PUB fault configuration was simplex; bus major bus 0 suspect

TABLE A (Contd)

PMD-33	PUB fault configuration was simplex; bus major bus 1 suspect
PMD-34	Controller fault configuration was duplex controllers; controller 0 suspect
PMD-35	Controller fault configuration was duplex controllers; controller 1 suspect
PMD-36	Controller fault configuration was simplex controllers; controller 0 suspect
PMD-37	Controller fault configuration was simplex controllers; controller 1 suspect
PMD-40	Controller fault configuration was simplex controller; bus suspect undetermined
PMD-41	Controller fault configuration was simplex controller; bus suspect undetermined
PMD-42	Controller fault configuration was duplex controllers; controller 0 suspect, but not conclusively. Sequence table tries to remove and diagnose mate controller on subsequent interrupts if they occur
PMD-43	Controller fault configuration was duplex controllers; controller 1 suspect, but not conclusively. Sequence table tries to remove and diagnose mate controller on subsequent interrupts if they occur
PMD-44	CC fault suspect active CC 0
PMD-45	CC fault suspect active CC 1
PMD-46	CC fault suspect stand-by CC 0
PMD-47	CC fault suspect stand-by CC 1
PMD-50	Interrupt from duplex failed unit
PMD-51	No unit found; PBFR could not identify a unit that was responsible for the interrupt or interject
PMD-52	System clock controller fault configuration was simplex system clock controllers; controller 0 suspect
PMD-53	System clock controller fault configuration was simplex system clock controllers; controller 1 suspect
PMD-54	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-55	System clock controller fault configuration was simplex system clock controller; and bus suspect undetermined
PMD-56	System clock soft error configuration was simplex system clock controllers; controller 0 suspect
PMD-57	System clock soft error configuration was simplex system clock controllers; controller 1 suspect
PMD-60	System clock transient error configuration was simplex system clock controllers; controller 0 suspect
PMD-61	System clock transient error configuration was simplex system clock controllers; controller 1 suspect

[1] See NOTE 1. Identify failing test type and failing test number (in octal) [FIG. 1 and 2]

[2] Identify failing data bit positions (binary)

[3] Identify PBFR relative address that initiated test

[4] Using TABLE A, Page 2 identify failing test function

AND

[5] Is failing test number greater than 71

No

Yes

[6] On TABLE B, Page 5 identify bit pattern for identified test number

[7] Has each group of trace tests that were run been analyzed

No

Yes

[8] Repeat from Step 1 for next group of trace tests

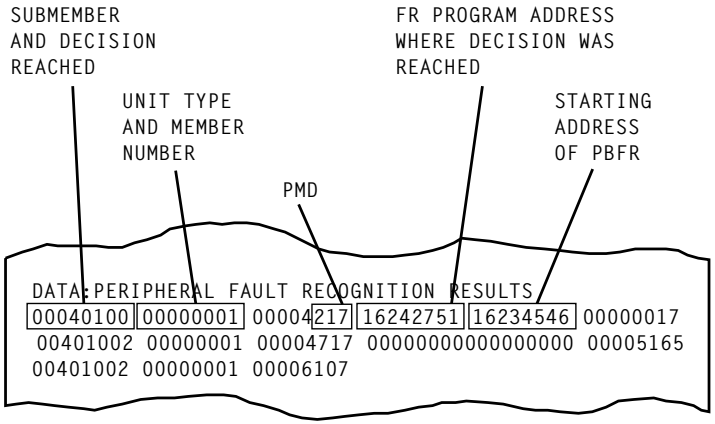


FIG. 1 - Part of PBFR Printout With Trace Data Words 6 Through 14

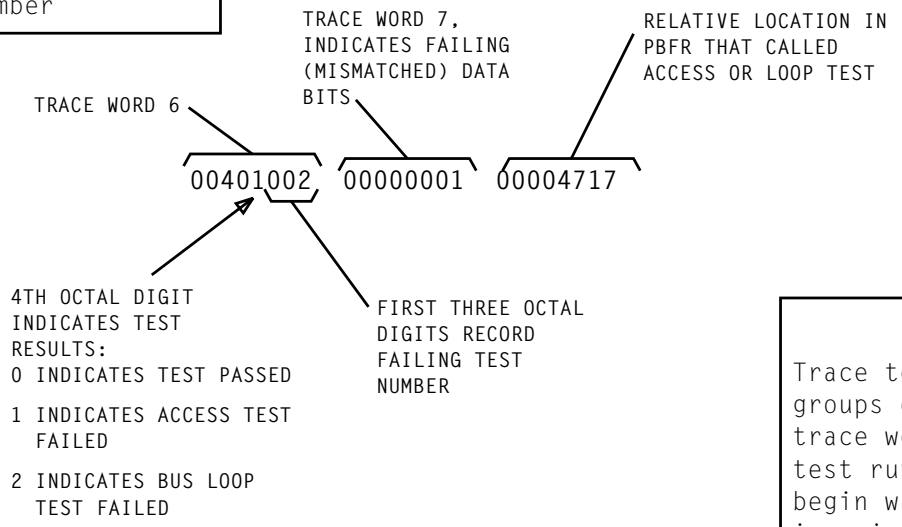


FIG. 2 - Trace Word Layout

NOTE 1
Trace tests are in groups of three trace words for each test run and always begin with word 6 in printout

ANALYZE F-LEVEL INTERRUPT, PBFR TRACE FEATURE

TABLE A			
ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
1	Reset MA, read SR to verify MA=0	30	Looparound pattern 20202020
2	Set MA, read SR to verify MA=1	31	Read reply register, verify 20202020
3	Verify ASWEPU=0 due to above orders	32	Looparound 57575757
4	Looparound pattern 00000000	33	Read reply register, verify 57575757
5	Read reply register, verify 00000000	34	Looparound pattern 40404040
6	Looparound pattern 77777777	35	Read reply register, verify 40404040
7	Read reply register, verify 77777777	36	Looparound 37373737
10	Looparound pattern 01010101	37	Read reply register, verify 37373737
11	Read reply register, verify 01010101	40	Looparound 07007007
12	Looparound 76767676	41	Read reply register, verify 07007007
13	Read reply register, verify 76767676	42	Looparound 70770770
14	Looparound pattern 02020202	43	Read reply register, verify 70770770
15	Read reply register, verify 02020202	44	Looparound 700700700
16	Looparound 75757575	45	Read reply register, verify 700700700
17	Read reply register, verify 75757575	46	Looparound 077077077
20	Looparound pattern 04040404	47	Read reply register, verify 077077077
21	Read reply register, verify 04040404	50	Looparound 00700707
22	Looparound 73737373	51	Read reply register, verify 00700707
23	Read reply register, verify 73737373	52	Looparound 77077070
24	Looparound pattern 10101010	53	Read reply register, verify 77077070
25	Read reply register, verify 10101010	54	Verify APEPU = 0 & non-TMS, TSI ASWEPU=0
26	Looparound 67676767	55	Clear ESR, read ESR, verify PFE=0 & PFO=0
27	Read reply register, verify 67676767		

TABLE A (Contd)			
ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
56	Looparound with EDATA (bit 10) inverted, verify PFE,PFO=0	75	Set IP1,IP2=1, send bit pattern D, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
57	Looparound with EDATA (bit 11) inverted, verify PFE,PFO=0	76	Set IP1,IP2=1, send bit pattern E, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
60	Looparound with EDATA (bit 12) inverted, verify PFE,PFO=0	77	Set IP1,IP2=1, send bit pattern F, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
61	Looparound with EDATA (bit 13) inverted, verify PFE,PFO=0	100	Set IP1,IP2=1, send bit pattern G, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
62	Looparound with EDATA (bit 14) inverted, verify PFE,PFO=0	101	Set IP1,IP2=1, send bit pattern H, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
63	Looparound with EDATA (bit 15) inverted, verify PFE,PFO=0	102	Set IP1,IP2=1, send bit pattern I, verify PFE,PFO=1 MTCPU=1 BIT 35 =0
64	Looparound with EDATA (bit 16) inverted, verify PFE,PFO=0	103	Set IP1,IP2=1, send bit pattern J, verify PFE,PFO=1 MTCPU=0 BIT 35 =0
65	Looparound with EDATA (bit 17) inverted, verify PFE,PFO=0	104	Set IP1,IP2=1, send bit pattern K, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
66	Looparound with EDATA (bit 18) inverted, verify PFE,PFO=0	105	Set IP1,IP2=1, send bit pattern U, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
67	Looparound with EDATA (bit 19) inverted, verify PFE,PFO=0	106	Set IP1,IP2=1, send bit pattern L, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
70	Looparound with EDATA (bit 20) inverted, verify PFE,PFO=0	107	Set IP1,IP2=1, send bit pattern V, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
71	Looparound with EDATA (bit 21) inverted, verify PFE,PFO=0 MTCPU=1 BIT 35 =0		
72	Set IP1,IP2=1, send bit pattern A, verify PFE,PFO=1 MTCPU=1 BIT 35 =0		
73	Set IP1,IP2=1, send bit pattern B, verify PFE,PFO=1 MTCPU=1 BIT 35 =0		
74	Set IP1,IP2=1, send bit pattern C, verify PFE,PFO=1 MTCPU=1 BIT 35 =0		

TABLE A (Contd)			
ACCESS TEST	PBFR TABLE OF ACCESS TESTS	ACCESS TEST	PBFR TABLE OF ACCESS TESTS
110	Set IP1,IP2=1, send bit pattern M, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	120	Set IP1,IP2=1, send bit pattern Q, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
111	Set IP1,IP2=1, send bit pattern W, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	121	Set IP1,IP2=1, send bit pattern 1, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
112	Set IP1,IP2=1, send bit pattern N, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	122	Set IP1,IP2=1, send bit pattern R, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
113	Set IP1,IP2=1, send bit pattern X, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	123	Set IP1,IP2=1, send bit pattern 2, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
114	Set IP1,IP2=1, send bit pattern O, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	124	Set IP1,IP2=1, send bit pattern S, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
115	Set IP1,IP2=1, send bit pattern Y, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	125	Set IP1,IP2=1, send bit pattern 3, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
116	Set IP1,IP2=1, send bit pattern P, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	126	Set IP1,IP2=1, send bit pattern T, verify PFE,PFO=1 MTCPU=0 BIT 35 =1
117	Set IP1,IP2=1, send bit pattern Z, verify PFE,PFO=1 MTCPU=0 BIT 35 =1	127	Set IP1,IP2=1, send bit pattern 4, verify PFE,PFO=1

TABLE B
PBFR TABLE OF ACCESS TESTS

BIT PATTERN	PRM	PRL	BIT PATTERN	PRM	PRL
A	0000	00000000	O	7410	10101010
B	0001	01010101	P	7420	20202020
C	0002	02020202	Q	7440	40404040
D	0004	04040404	R	7507	07007007
E	0010	10101010	S	7570	70070070
F	0020	20202020	T	7577	00700707
G	0011	40404040	U	7577	77777777
H	0022	07007007	V	7576	76767676
I	0037	70070070	W	7575	75757575
J	0007	00700707	X	7573	73737373
TESTS 72-103	Skip for EST, TMS, and TSI		Y	7567	67676767
72-127	Skip for DIF and SCS		Z	7557	57575757
104-127	Skip for TAC, SYSCLK		1	7537	37373737
			2	7470	70770770
K	7400	00000000	3	7407	07707707
L	7401	01010101	4	7400	77077070
M	7402	02020202			
N	7404	04040404			

1. Define error using PMDs [TABLE A]

TABLE A

PMD-001	VCFR00 allowed error analysis to resolve the error. VIC 1 failed the access test. The VIF was simplexed	PMD-011	VCFR00 allowed error analysis to resolve the error. This is the VIF DUPLEX failure for controller 0. VCFR main flow leg
PMD-002	VCFR00 allowed error analysis to resolve the error. VIC 0 failed the access test. The VIF was simplexed	PMD-012	VCFR00 allowed error analysis to resolve the error. This is the VIF DUPLEX failure for controller 1. VCFR main flow leg
PMD-003	VCFR00 decided to remove and diagnose controller 1. VIC 1 failed the access test. The VIF was duplexed	PMD-013	VCFR00 took no action because of transient error. Select mode circuitry appears functional. ESM mismatch leg
PMD-004	VCFR00 decided to remove and diagnose controller 1. VIC 0 failed the access test. The VIF was duplexed	PMD-014	VCFR00 decided to remove and diagnose controller 1. The ESM flip-flop in controller 0 is stuck at 0. ESM mismatch leg
PMD-005	VCFR00 decided to remove and diagnose controller 1. A unique failure in controller 1 has been detected. VCFR main flow leg	PMD-015	VCFR00 decided to remove and diagnose controller 0. The ESM flip-flop in controller 0 is stuck at 0. ESM mismatch leg
PMD-006	VCFR00 decided to remove and diagnose controller 0. A unique failer in controller 0 has been detected. VCFR main flow leg	PMD-016	VCFR00 decoded tp remove and diagnose controller 1. The ESM flip-flop in controller 1 is stuck at 1. ESM mismatch leg
PMD-007	VCFR00 allowed error analysis to resolve the error. A nonunique failure in controller 1 has been detected. VCFR main flow leg	PMD-017	VCFR00 decided to remove and diagnose controller 0. The ESM flip-flop in controller 0 is stuck at 1. ESM mismatch leg
PMD-010	VCFR00 allowed error analysis to resolve the error. A nonunique failure in controller 0 has been detected. VCFR main flow leg		

DEFINE PMD DICTIONARY NODES, VCFR

TABLE A (Contd)

PMD-020	VCFR00 took no action because of a transient error. Register test gives ATP results. Reply register mismatch routine
PMD-021	VCFR00 decided to remove and diagnose controller 0. A fault in a register in controller 0 was detected. Reply register mismatch — general purpose register test
PMD-023	VCFR00 allowed error analysis to resolve the error. A single VIU 1 failed in a frame which had a protection switch up. VIC 1 was active. This VIU is restored on the first interrupt. Multiple VIU failure leg
PMD-024	VCFR00 allowed error analysis to resolve the error. A single VIU failed in a frame which had a protection switch up. VIC 0 was active. This VIU is restored on the first interrupt. Multiple VIU failure leg
PMD-025	VCFR00 allowed error analysis to resolve the error. VIC 1 recorded failing VIUs. Multiple VIU failure leg
PMD-026	VCFR00 allowed error analysis to resolve the error. VIC 0 recorded failing VIUs. Multiple VIU failure leg
PMD-027	VCFR00 allowed error analysis to resolve the error. Allow error analysis to resolve possible TSI-VIU data stream problem. Controller 0 was in service. VCFR00 passed control to error analysis
PMD-030	VCFR00 allowed error analysis to resolve the error. Allow error analysis to resolve possible TSI-VIU data stream problem. Controller 1 was in service. VCFR00 pased control to error analysis
PMD-031	VCFR00 allowed error analysis to resolve the error. CS0 recorded in multiple VIUs; possible controller problem. Multiple VIU failure leg
PMD-032	VCFR00 allowed error analysis to resolve the error. VIUs 0—3 errors implicate VIC 0. Multiple VIU failure leg
PMD-033	VCFR00 allowed error analysis to resolve the error. VIUs 4—7 errors implicate VIC 1. Multiple VIU failure leg
PMD-034	VCFR00 decided to remove and diagnose controller 0. Controller 0 failed register state proof test. Multiple VIU leg — special register test
PMD-035	VCFR00 decided to remove and diagnose controller 1. Controller 1 failed register state proof test. Multiple VIU leg — special register test
PMD-036	VCFR00 decided to remove and diagnose controller 0. Error resolved to controller 0. Input parity failure leg
PMD-037	VCFR00 decided to remove and diagnose controller 1. Error resolved to controller 1. Input parity failure leg

TABLE A (Contd)			
PMD-040	VCFR00 decided to remove and diagnose controller 0. Error resolved to controller 0. Clock error subroutine	PMD-042	VCFR00 allowed error analysis to resolve the error. Restore VIU on first interject
PMD-041	VCFR00 decided to remove and diagnose controller 1. Error resolved to controller 1. Clock error subroutine	PMD-043	VCFR00 decided to remove and diagnose controller 0. A controller problem has been found. VIU interject leg

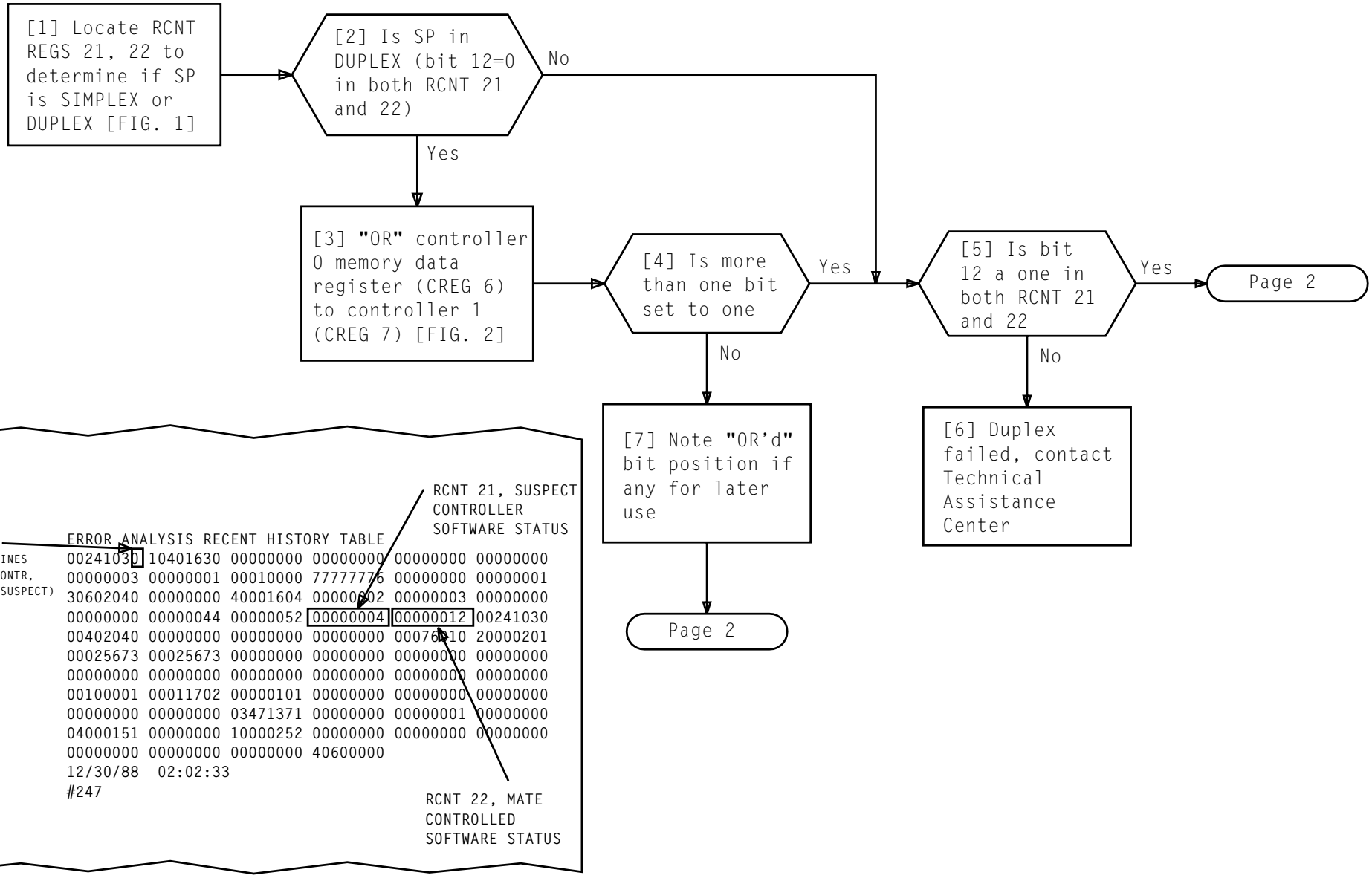
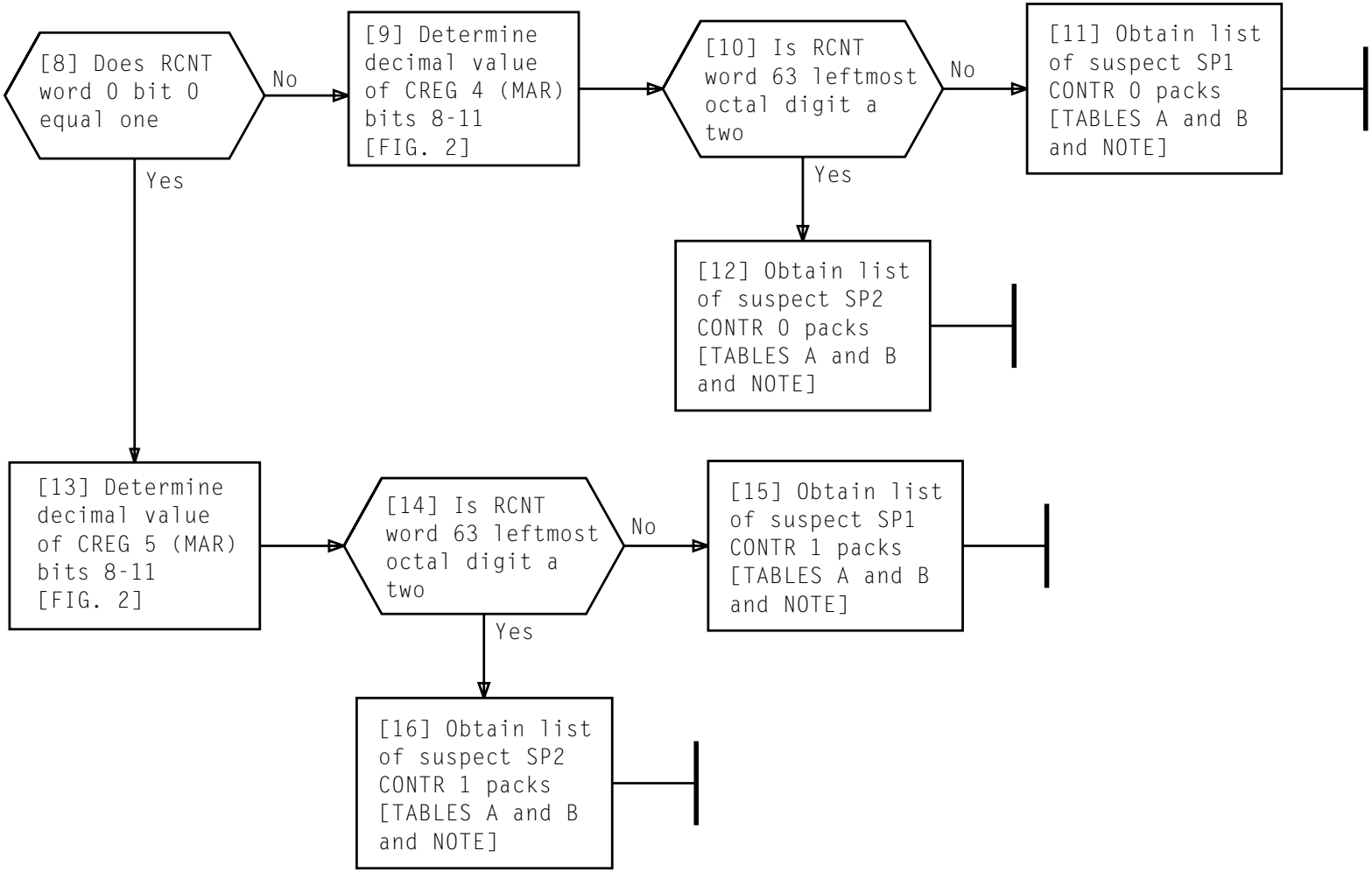


FIG. 1 – RCNT Register Printout

PERFORM MEMORY ROUTINE, SIGNAL PROCESSOR



NOTE
If this step was reached use "OR'D" bit position to select a suspect memory (column)

PERFORM MEMORY ROUTINE, SIGNAL PROCESSOR

TABLE A
FA634 AND FA580 PACKS

CREG 4 BITS 8-11 DECIMAL VALUE	FA634/FA634B PACK LOCATIONS					
	SP-2/COMBINED MATRIX			SP-1/COMBINED MATRIX		
	BITS 0-8	BITS 9-17	18-23/ No bits set	BITS 0-8	BITS 9-17	18-23/ No bits set
0	62-51	62-56	62-64	60-31	60-35	60-39
1	62-52	62-57	62-65	60-32	60-36	60-40
2	62-54	62-58	62-66	60-33	60-37	60-41
3	62-55	62-59	62-67	60-34	60-38	60-42
4	70-51	70-56	70-64	68-31	68-35	68-39
5	70-52	70-57	70-65	68-32	68-36	68-40
6	70-54	70-58	70-66	68-33	68-37	68-41
7	70-55	70-59	70-67	68-34	68-38	68-42
	BITS 0-7	BITS 8-16	17-23/ No bits set			
8		62-60	70-60			
9		62-61	70-61			
10		62-62	70-62			
11		62-63	70-63			
FA580 Pack Locations	66-54, 66-55, 66-58, 66-59, 66-63, 66-64			64-35, 64-36, 64-37, 64-39, 64-41, 64-42		

TABLE B
MEMORY REGISTER PACKS

PACK TYPE	SP-1/COMBINED MATRIX	SP-2/COMBINED MATRIX
FA582	64-38	66-57
FA580	64-40	66-58
FA578	64-26, 27, 28	66-43, 44, 45
FA578	64-31, 32, 33	66-46, 47, 48

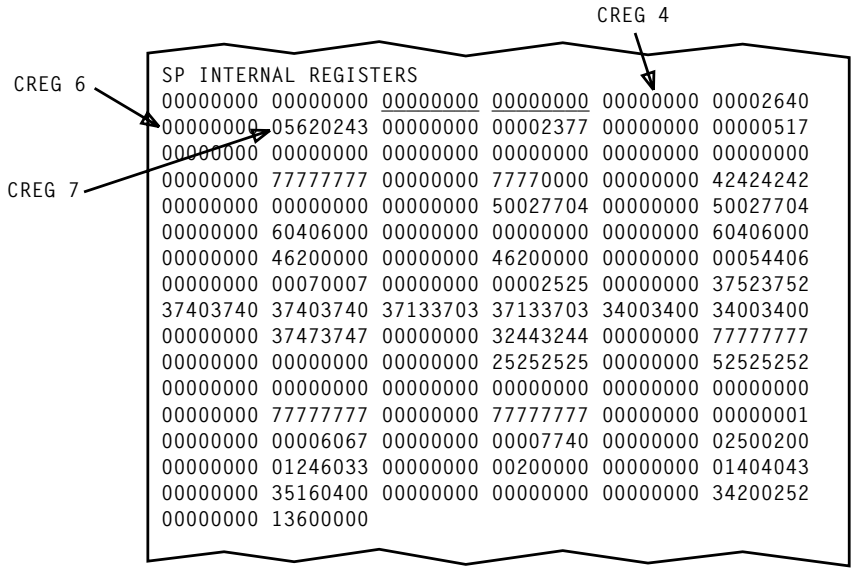


FIG. 2 — SP Critical Register (CREG) Printout

PERFORM MEMORY ROUTINE, SIGNAL PROCESSOR

[1] Is interrupt APUF (bit 4 set) or PUF (bit 5 set) from F-LEVEL REG 15

APUF (4 = 1) → Page 2

PUF (5 = 1)

	K-BLOCK				CREG BITS (ROW DATA)								F-LEVEL BITS			
BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STEP 3							1	1	0	1	1	1	0	0	0	0
STEP 4					0	0	1	1	0	1	1	1	0	0	0	0
STEP 6	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0
STEP 7 Octal MSN	0				1		5				6		0			

STEP 5 SP = 0

STEP 2 K = 4
STEP 4 − 4
(FROM NOTE) K = 0

EXAMPLE 1

[2] See EXAMPLE 1. Obtain SP column (from F-LEVEL REG 26, bits 0-3), SP row (from CREG 10, 11; bits 0-5) and SP K-block (CREG 10, 11; bits 6-8)

[3] Combine data from both registers with SP column being bits 0-3; SP row becomes bits 4-9

[4] See NOTE 1. Insert K-block in bit positions 10 and 11

[5] Obtain SP member number from text header [FIG. 1, Page 2]

[6] Convert SP member number to binary and place result in bit positions 12-15

[7] Convert bit positions 0-16 to octal. This is MSN, MDN, TSN

AND

NOTE 1
Only two data bits (10 and 11) are reserved for K-Block data; therefore, if K is 4 or 5, then subtract 4 from the K

DETERMINE MSN, MDN, OR TSN NUMBER

[8] Obtain SP member number from text of interrupt printout [FIG. 1]

[9] Locate CREG 8/9 and obtain octal value of bits 0-11 [FIG. 2]

AND

[10] Obtain MSN, MDN, TSN by placing SP member number (octal) in front of value contained in CREG 8/9 [EXAMPLE 2]

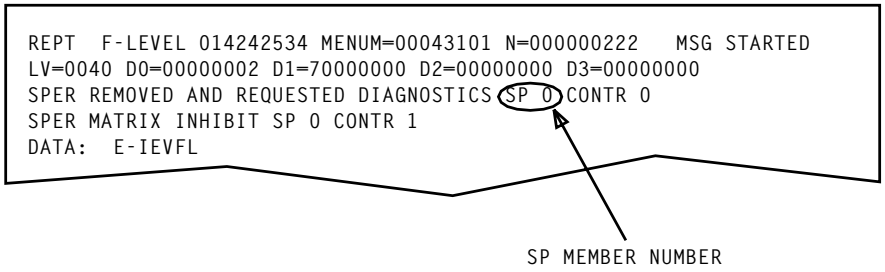


FIG. 1 - Text Header

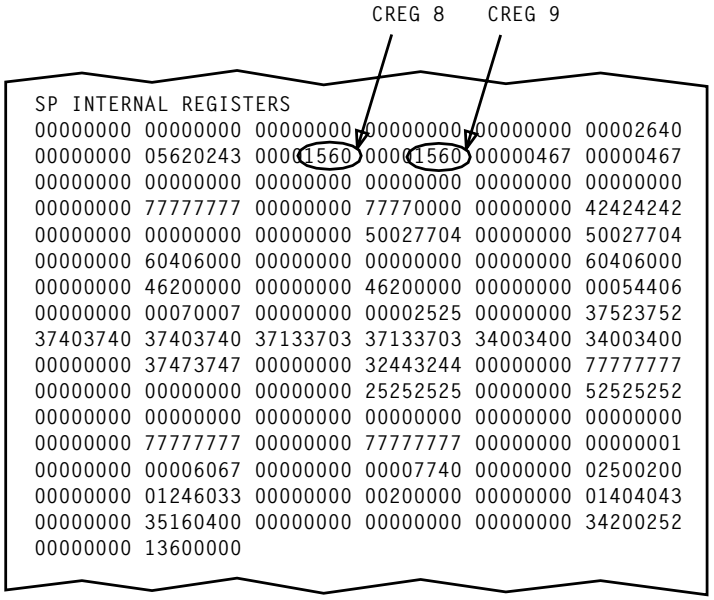


FIG. 2 - P/O F-Level Printout

SP MEMBER NUMBER = 0
CREG 8/9 = 1560

MSN, MDN, TSN = 01560

EXAMPLE 2

DETERMINE MSN, MDN, OR TSN NUMBER

1. Define error using PMDs [TABLE A]

End of procedure

TABLE A

PMD-001	Millisecond clock values stored at time of interrupt were unequal. Testing proved to show clock in CONTR 0 was at fault
PMD-002	Millisecond clock values stored at time of interrupt were unequal. Testing proved to show clock in CONTR 1 was at fault
PMD-003	Millisecond clock values stored at time of interrupt were unequal. Further testing was unable to find problem. Error exits to error analysis preparation when one controller is out of service
PMD-004	CONTR 0 was only controller in service at time of interrupt. Its clock activity does not set to 0
PMD-005	CONTR 1 is only controller in service at time of interrupt. Its clock activity does not set to 1
PMD-006	CONTR 0 is only controller in service at time of interrupt. R0 does not set to active bus
PMD-007	CONTR 1 is only controller in service at time of interrupt. R0 does not set to active bus
PMD-010	Only CONTR 0 was in service at time of interrupt. Its memory parameters indicate internal bus failure
PMD-011	Only CONTR 1 was in service at time of interrupt. Its memory parameters indicate internal bus failure
PMD-012	Only CONTR 0 was in service at time of interrupt. It has unique error
PMD-013	Only CONTR 1 was in service at time of interrupt. It has unique error
PMD-014	CONTR 0 is in service at time of interrupt and analog timer has timed out; that is, on-line controller is assumed to have stopped longer than 100 ms but stop flop of controller is assumed at fault
PMD-015	CONTR 1 is in service at time of interrupt and analog timer has timed out; that is, on-line controller is assumed to have stopped longer than 100 ms but stop flop of controller is assumed to be at fault
PMD-016	Memory mismatch caused AINT interrupt. Memory access REG MAR and MDR were found equal. CONTR 0 matcher detector is in error
PMD-017	Memory mismatch caused AINT interrupt. Memory access REG MAR and MDR were found equal. CONTR 1 matcher detector is in error
PMD-020	CONTR 0 has bad clock circuit
PMD-021	CONTR 1 has bad clock circuit
PMD-022	CONTR 1 has bad error source register
PMD-023	CONTR 0 has bad error source register
PMD-024	CONTR 0 has failed memory parameter check of fixed memory words. Suspect internal busing system or memory access circuit
PMD-025	CONTR 1 failed memory parameter check of fixed memory words. Suspect internal busing system or memory access circuit

TABLE A (Contd)

PMD-026	Both controllers AINT and ASWF are reset. Suspect transient or ESR
PMD-027	Unique error in CONTR 0 has AINT unique error involving an SR
PMD-030	Unique error in CONTR 1 has AINT unique error involving SR
PMD-031	No controller is on-line according to status. Force CONTR 0 on-line by assuming CONTR 0 simplex failure
PMD-032	CONT 0 failed. Suspect analog timer circuitry
PMD-033	CONTR 1 failed. Suspect analog timer circuitry
PMD-034	One or both controllers had analog timer timed out. Call store status said it was not stopped. Thus, it was left stopped by unknown program for excessive amount of time
PMD-035	CONTR 1 has unique error. Found after ASWF interrupt involving SP
PMD-036	CONTR 0 has unique error. Found after ASWF interrupt involving SP
PMD-037	CONTR 0 has peripheral sequencer time-out failure
PMD-040	CONTR 1 has peripheral sequencer time-out failure
PMD-041	SP was duplexed. Only CONTR 0 recorded software error such as invalid OPCODE. Both would have recorded error if it existed; CONTR 0 recorded it incorrectly
PMD-042	SP was duplexed. Only CONTR 1 recorded software error such as invalid OPCODE. Both would have recorded error if it existed; CONTR 1 recorded it incorrectly
PMD-043	CONTR 1 received on F/F, RO, failed
PMD-044	CONTR 0 received on F/F, RO, failed
PMD-045	CONTR 0 has error in matrix interface or matrix sequencing logic
PMD-046	CONTR 1 has error in matrix interface or matrix sequencing logic
PMD-047	Duplexed SP interrupt. Fault isolated to SP simplex matrix
PMD-050	Matrix interrupt occurred; testing failed to find cause
PMD-051	Matrix error in CONTR 0 of simplexed SP detected, retired, and failed again
PMD-052	Matrix error in CONTR 1 of simplexed SP detected, retired, and failed again
PMD-053	Simplex SP had matrix error which could not be found
PMD-054	Simplex SP had matrix error which could not be found
PMD-055	Universal row accessed by duplexed controller but row was out of range. Multilation detection number already loaded in recent history table for error analysis
PMD-056	Unequipped portion of matrix accessed in simplex SP with CONTR 0 active
PMD-057	Unequipped portion of matrix accessed in simplex SP with CONTR 1 active
PMD-060	Miscellaneous row accessed by duplexed controller but row was out of range. Multilation detection number already loaded in recent history table for error analysis

TABLE A (Contd)

PMD-061	Unequipped portion of matrix accessed in simplex SP with CONTR 0 active
PMD-062	Unequipped portion of matrix accessed in simplex SP with CONTR 1 active
PMD-063	Matrix error found in duplex SP
PMD-064	Matrix error found in simplex SP with CONTR 1 on line
PMD-065	Transient matrix failure found in duplexed SP
PMD-066	CONTR 0 has memory access mismatch. Controllers were duplexed. Error occurred during a peripheral order access
PMD-067	CONTR 1 has memory access mismatch. Controllers were duplexed. Error occurred during peripheral order access
PMD-070	Memory access mismatch detected while controllers were duplexed. Further testing unable to find error. Error occurred during CC order access
PMD-071	CONTR 0 failed PU reply bus register test
PMD-072	CONTR 1 failed PU reply bus register test
PMD-073	CONTR 0 failed and caused PU reply bus register mismatch
PMD-074	CONTR 1 failed and caused PU reply bus register mismatch
PMD-075	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table
PMD-076	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table
PMD-077	SP detected invalid OPCODE. Audit MDN number loaded in RCNT history table
PMD-100	DPOWL full, bit set in both controllers. MDNs loaded in RCNT history table. SP was duplexed.
PMD-101	DPOWL full, in CONTR 0 while simplexed. Audit MDN loaded into RCNT history table
PMD-102	DPOWL full, in CONTR 1 while simplexed. Audit MDN loaded into RCNT history table
PMD-103	CONTR 0 has invalid INVOP ESR bit stuck or failing pest bit
PMD-104	CONTR 1 has invalid INVOP ESR bit stuck or failing pest bit
PMD-105	CONTR 0 simplexed. Invalid ESR bit set
PMD-106	CONTR 1 simplexed. Invalid ESR bit set
PMD-107	CONTR 0 has analog timer timed out. SP stopped
PMD-110	CONTR 1 has analop timer timed out. SP stopped
PMD-111	ASWF recorded in ESR of duplexed SP. PUF not recorded in CC
PMD-112	ASWF recorded in ESR of simplexed SP. PUF not recorded in CC
PMD-113	ASWF recorded in ESR of simplexed SP. PUF not recorded in CC
PMD-114	Ring counters mismatched between controllers
PMD-115	Ring counters mismatched between controllers
PMD-116	CONTR 0 has matrix error in simplex SP
PMD-117	SP recorded ASWF interrupt; CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN a controller. Pest the matrix so DGN can complete

TABLE A (Contd)

PMD-120	SP recorded ASWF interrupt, CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN controller 0 and pest the matrix so DGN could complete.
PMD-121	SP recorded ASWF interrupt, CC recorded APUF in (INS) register and matrix errors were set. No error processing could be done. Remove and DGN controller 1 and pest the matrix so DGN could complete.
PMD-122	SP recorded ASWF. CC did not remove and diagnose controller 0 because it has errors set
PMD-123	SP recorded ASWF. CC did not remove and diagnose controller 1 because it has errors set
PMD-124	Simplexed controller 0 digit buffer not full but ESR had INTJ set
PMD-125	Simplexed controller 1 digit buffer not full but ESR had INTJ set
PMD-126	SP duplexed. Digit buffer not full. ESR INTJ bit set in CONTR 0 only
PMD-127	SP duplexed. Digit buffer not full. ESR INTJ bit set in CONTR 1 only
PMD-130	CONT 0 simplexed. Digit buffer full. Suspect software error and unload buffer
PMD-131	CONTR 1 simplexed. Digit buffer full. Suspect software error and unload buffer
PMD-132	SP duplexed. Digit buffer full. Suspect software error and unload buffer
PMD-201	Error in DT interface found. CONTR 0 implicated by fault recognition
PMD-202	Error in DT interface found. CONTR 1 implicated by fault recognition
PMD-203	Mismatch in DT interface found. Fault recognition determined SP CONTR 0 faulty
PMD-204	Mismatch in DT interface found. Fault recognition determined SP CONTR 1 faulty
PMD-205	Unique error found in simplexed SP, CONTR 0
PMD-206	Unique error found in DT interface. SP CONTR 1 simplexed
PMD-207	Transient DT interface error detected by CONTR 0. All link tests passed
PMD-210	Transient DT interface error detected by CONTR 1. All link tests passed
PMD-310	AINT memory mismatch occurred. CONT 0 accessed out-of-range address. Incompatible with state of active sequencer
PMD-311	AINT memory mismatch occurred. CONT 1 accessed out-of-range address. Incompatible with state of active sequencer
PMD-312	AINT memory mismatch occurred. Tests run on memory address and data registers were ATP
PMD-313	ASW interrupt caused by sequencer mismatch when CONTR 0 failed to stop in valid stopping state for peripheral access of SP
PMD-314	ASW interrupt caused by sequencer mismatch when CONTR 1 failed to stop in valid stopping state for peripheral access of SP

TABLE A (Contd)	
PMD-315 Client sequencer found active in CONTR 0. Incorrect client	PMD-326 SPRF suspected MF out. Sequencer in error. Retry ATP
PMD-316 Client sequencer found active in CONTR 1. Incorrect client	PMD-327 DPO sequencer in CONTR 0 mismatched and is not faulty
PMD-317 CONTR 0 incorrectly sensed a sequencer mismatch	PMD-330 DPO sequencer in CONTR 1 mismatched and is faulty
PMD-320 CONTR 1 incorrectly sensed a sequencer mismatch	PMD-331 SDR sequencer in CONTR 0 mismatched and is faulty
PMD-321 Executive sequencer mismatched. No apparent reason for mismatch found.	PMD-332 SDR sequencer in CONTR 1 mismatched and is faulty
PMD-322 Executive sequencer mismatched. CONTR 0 faulty	PMD-333 CONTR 0 failed a general register check. SPFR ran a memory mismatch test but did not find a suspect controller. Address of register checked is in the J register
PMD-323 Executive sequencer mismatched. CONTR 1 faulty	PMD-334 CONTR 1 failed a general register check. SPFR ran a memory mismatch test but did not find a suspect controller. Address of register checked is in the J register
PMD-324 MF out; sequencer active. Mismatch occurred. CONTR 0 faulty	
PMD-325 MF out; sequencer active. Mismatch occurred. CONTR 1 faulty	

1. Define error using PMDs [TABLE A]

End of procedure

TABLE A

PMD-001	APUF (Duplex) no error found
PMD-002	PUF (Duplex) no error found; ASWF set in active only
PMD-003	PUF (Duplex) no error found; ASWF set in mate only
PMD-004	PUF (Duplex) no error found
PMD-005	(Duplex) no CC PUF or APUF error source found
PMD-011	Clock error in active only; hit-timed and clock error still present
PMD-012	Clock error in active only; hit-timed and clock error is gone
PMD-014	Clock error in mate only; hit-timed and clock error is still present
PMD-015	Clock error in mate only; hit-timed and clock error is gone
PMD-017	Clock error in both controllers; hit-timed and clock error in active only
PMD-021	Clock error in both controllers; hit-timed and clock error in mate only
PMD-025	Clock error in both controllers; hit-timed and clock error in both controllers
PMD-026	Clock error in both controllers; hit-timed and error is gone in both
PMD-030	Unique error in active only; pested mismatch and hit-timed; then error in active only
PMD-031	Unique error in active only; pested mismatch and hit-timed; then error in mate only
PMD-032	Unique error in active only; pested mismatch and hit-timed; then error in both controllers
PMD-033	Unique error in active only; pested mismatch and hit-timed; then error is gone
PMD-034	Unique error in mate only; pested mismatch and hit-timed; then error in active only
PMD-035	Unique error in mate only; pested mismatch and hit-timed; then error in mate only
PMD-036	Unique error in mate only; pested mismatch and hit-timed; then error in both controllers
PMD-037	Unique error in mate only; pested mismatch and hit-timed; then error was gone
PMD-040	Unique error in both controllers; pested mismatch and hit-timed; then error was inactive only
PMD-041	Unique error in both controllers; pested mismatch and hit-timed; then error in standby only
PMD-042	Unique error in both controllers; pested mismatch and hit-timed; then error in both controllers
PMD-043	Unique error in both controllers; pested mismatch and hit-timed; then error is gone
PMD-044	Mismatch found in active only
PMD-045	Mismatch found in mate only
PMD-046	Mismatch found in both controllers
PMD-047	Firmware detected errors found in both controllers
PMD-050	Firmware detected errors in active controller
PMD-051	Firmware detected errors in standby controller
PMD-054	Microprocessor in both controllers has detected a normal buffer overflow

TABLE A (Contd)	
PMD-056	Microprocessor in both controllers has detected a normal maintenance buffer overflow
PMD-060	Microprocessor in both controllers has detected an invalid macro
PMD-061	Microprocessor in both controllers has detected a task table overflow
PMD-062	Microprocessor in both controllers has detected an error condition
PMD-064	Microprocessor in both controllers has detected an invalid macro
PMD-065	Microprocessor in both controllers has detected a task table overflow
PMD-066	Microprocessor in both controllers has detected an error condition
PMD-070	The peripheral order was no good
PMD-071	Unique error in active controller; retry the order and active still has unique error
PMD-072	Unique error in active controller; retry the order and active has no error
PMD-073	Unique error in mate controller; retry the order and mate still has unique error
PMD-074	Unique error in mate controller; retry the order and mate has no error
PMD-075	T1 line mismatch in active only
PMD-076	T1 line mismatch in standby only
PMD-077	T1 line mismatch in both controllers
PMD-100	Low frequency clock mismatch in active only
PMD-101	Low frequency clock mismatch in standby only
PMD-102	Low frequency clock mismatch in both controllers
PMD-103	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in active only
PMD-104	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in mate only
PMD-105	Highest priority mismatch found in active only; reset divorce in mate and retry order; order fails in both controllers
PMD-106	Highest priority mismatch found in active only; reset divorce in mate and retry order; order passes in both controllers
PMD-107	Highest priority mismatch found in standby only; reset divorce in active and retry order; order fails in active only
PMD-110	Highest priority mismatch found in mate only; reset divorce in active and retry order; order fails in mate only
PMD-111	Highest priority mismatch found in standby only; reset divorce in active and retry order; order fails in both controllers
PMD-112	Highest priority mismatch found in standby only; reset divorce in active and retry order; order passes in both controllers
PMD-113	Highest priority mismatch found in both controllers; retry order; order fails in active only
PMD-114	Highest priority mismatch found in both controllers; retry order; order fails in mate only
PMD-115	Highest priority mismatch found in both controllers; retry order; order fails in both controllers

TABLE A (Contd)

PMD-116	Highest priority mismatch found in both controllers; retry order; order passes in both controllers
PMD-117	Firmware detected errors in active controller
PMD-120	Unique error in active controller during a "buffer read" order
PMD-121	Unique error in mate controller during a "buffer read" order
PMD-122	Highest priority mismatch found only in active controller during a "buffer read" order
PMD-123	Highest priority mismatch found only in mate controller during a "buffer read" order
PMD-124	Highest priority mismatch found in both controllers during a "buffer read" order
PMD-125	Firmware detected errors in standby controller
PMD-130	APUF (simplex); no error found
PMD-131	PUF (simplex); no error found
PMD-132	(Simplex); no CC PUF or APUF error source found
PMD-141	Clock error found; hit-timed and clock error was still present
PMD-142	Clock error found; hit-timed and clock error was gone
PMD-150	Unique error found; pested mismatch and hit-timed; error was still present
PMD-151	Unique error found; pested mismatch and hit-timed; error was gone
PMD-152	Mismatch found in T1 line, low frequency clock, internal reply register or LUSP M-bit (DIF-E1 only)
PMD-153	Firmware detected errors
PMD-154	Microprocessor has detected a normal maintenance buffer overflow
PMD-156	Microprocessor has detected a normal maintenance buffer overflow
PMD-160	Microprocessor has detected an invalid macro
PMD-161	Microprocessor has detected a task table overflow
PMD-162	Microprocessor has detected an error condition
PMD-164	Microprocessor has detected an invalid macro
PMD-165	Microprocessor has detected a task table overflow
PMD-166	Microprocessor has detected an error condition
PMD-170	Peripheral order was no good
PMD-171	Unique error found; retry the order; unique error was still present
PMD-172	Unique error found; retry the order; unique error was gone
PMD-173	T1 line mismatch found
PMD-174	Low frequency clock mismatch found
PMD-175	"Sequencer", "internal bus", "reply register", or "LUSP M-bit" (DIF-E1) mismatch found
PMD-176	Firmware detected errors
PMD-177	Unique error found during a "buffer read" order
PMD-200	CONSISTENCY CHECK — HARD LOM STB — DGN INAPUT set in ACT and STB, IAS zero in STB
PMD-201	CONSISTENCY CHECK — HARD LOM ACT — DGN INAPUT set in ACT, reset in STB, IAS zero in STB
PMD-202	CONSISTENCY CHECK — HARD LOM STB — DGN INAPUT set in ACT, reset in STB, IAS nonzero in STB

TABLE A (Contd)	
PMD-203 CONSISTENCY CHECK — TRANSIENT LOM STB — DGN INAPUT reset in ACT and STB	PMD-240 INTERJECT FILTER — DIU Restore DIU — Cleanup Consistency check passes, common alarm, DS120 line error
PMD-204 CONSISTENCY CHECK — HARD LOM STB — DGN INAPUT reset in ACT, set in STB, IAS zero in STB	PMD-241 INTERJECT FILTER — DIU Force DIU — DGN — Cleanup Consistency check passes, common alarm
PMD-205 CONSISTENCY CHECK — HARD LOM ACT — DGN INAPUT reset in ACT, set in STB, IAS nonzero in STB	PMD-242 INTERJECT FILTER — HARD LOM ACT — DGN Multiple DIU's alarming
PMD-206 CONSISTENCY CHECK — TRPF TRANSIENT Force STB INAPUT reset in ACT, simplex frame, INTJ from O/S contr	PMD-301 BASE FILTER — DIU Force Digroup — DGN DIU BLM, Digroup failure
PMD-207 INTERJECT FILTER — SOFTWARE No Action Consistency check passes, normal DB overflow	PMD-302 BASE FILTER — DIU Force DIU — DGN BLM, routine diagnostic failure, implicates DIU
PMD-210 INTERJECT FILTER — HARD LOM ACT — DGN Consistency check passes, duplex frame, DB overflow, but pointers are inconsistent	PMD-303 INVALID
PMD-211 INTERJECT FILTER — HARD Restore ACT Consistency check passes, simplex frame, DB overflow, but pointers are inconsistent	PMD-304 BASE FILTER — DIU Force Digroup — DGN DIU BLM, routine diagnostic failure, implicates digroup
PMD-215 INTERJECT FILTER — HARD LOM ACT — DGN Force DIU if I/S else Restore SUBJ Consistency check passes, duplex frame, PSW audit failure	PMD-305 BASE FILTER — HARD Hit Time BLM, illegitimate report, duplex frame
PMD-216 INTERJECT FILTER — HARD Restore ACT Force DIU if I/S else Restore SUBJ Consistency check passes, simplex frame, PSW audit failure	PMD-306 BASE FILTER — HARD Hit Time BLM, illegitimate report, simplex frame
PMD-217 INTERJECT FILTER — TRANSIENT LOM ACT — DGN Consistency check passes, duplex frame, but no sources found	PMD-307 BASE FILTER — DIU Force DIU — DGN BLM, illegitimate report from spare DIU — not PSW
PMD-220 INTERJECT FILTER — TRANSIENT Restore ACT — Force STB Consistency check passes, simplex frame, but no sources found	PMD-330 RAM errors found in standby only or in both controllers (DIF-E1 only)
PMD-221 INTERJECT FILTER — TRANSIENT Restore ACT — Audit 27 DB overflow from DIF out of polling range	PMD-331 RAM errors found in active controller only and standby may have F/W errors (DIF-E1 only)
	PMD-340 Firmware detected errors in active controller with RAM errors (DIF-E1 only)
	PMD-341 Firmware detected errors in standby controller with RAM errors (DIF-E1 only)

TABLE A (Contd)	
PMD-350	Firmware detected errors found and RAM errors (DIF-E1 only — APUF)
PMD-360	Firmware detected errors found and RAM errors (DIF-E1 only — PUF)
PMD-373	Hardware access test failure
PMD-374	Interrupt from a growth frame
PMD-375	Interrupt from an unequipped frame
PMD-377	Interrupt from a duplex failed frame

1. Enter: **RMV:SCLK 0,NCSU 0!**

   NOTE: Bit 12 of word A indicates controller status. If 0, use word C in CONTR 0. If 1, use word C in CONTR 1

2. Identify oscillator using bits 0, 1, and 2 of word C and TABLE A [FIG. 1]

3. At oscillator, disable oscillator using **ENABLE/DISABLE** switch

4. Locate cable connectors at NCSU [TABLE A]

5. Remove cable connectors and inspect for broken connectors, broken leads, etc.

6. Reseat cable connectors

7. At oscillator identified in Step 2, remove and reseat cable connector (labeled **D/A INPUT /OUTPUT**)

8. Enable oscillator using **ENABLE/DISABLE** switch on oscillator

9. Enter: **RST:SCLK 0,NCSU 0!**

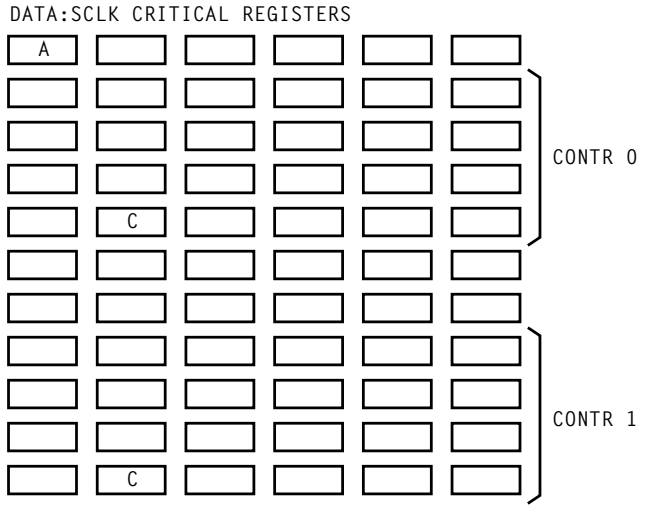
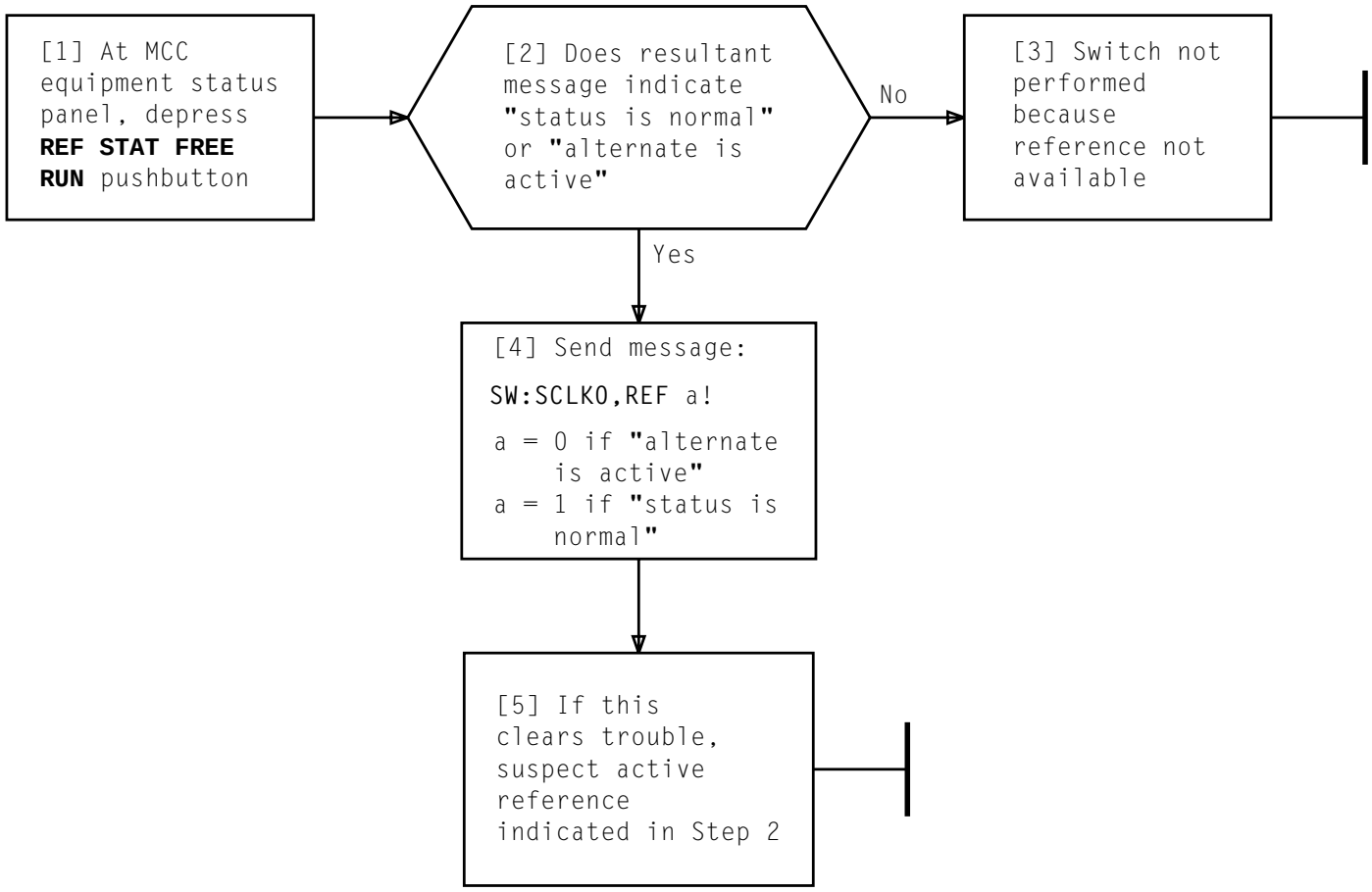


FIG. 1 – SCLK Critical Registers

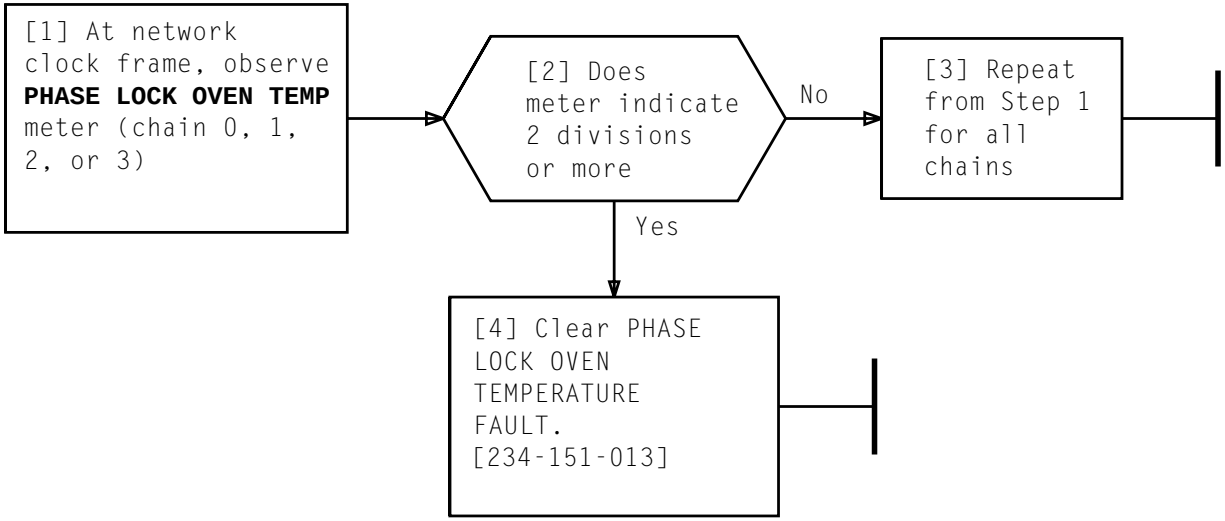
TABLE A

BIT			OSC	NCSU CONNECTORS
2	1	0		
0	0	0	0	0-48-56
0	0	1	1	0-52-56
0	1	0	2	0-52-58
0	1	1	3	0-48-58
1	0	0	0	0-48-56
1	0	1	1	0-52-56
1	1	0	2	0-52-58
1	1	1	3	0-48-58

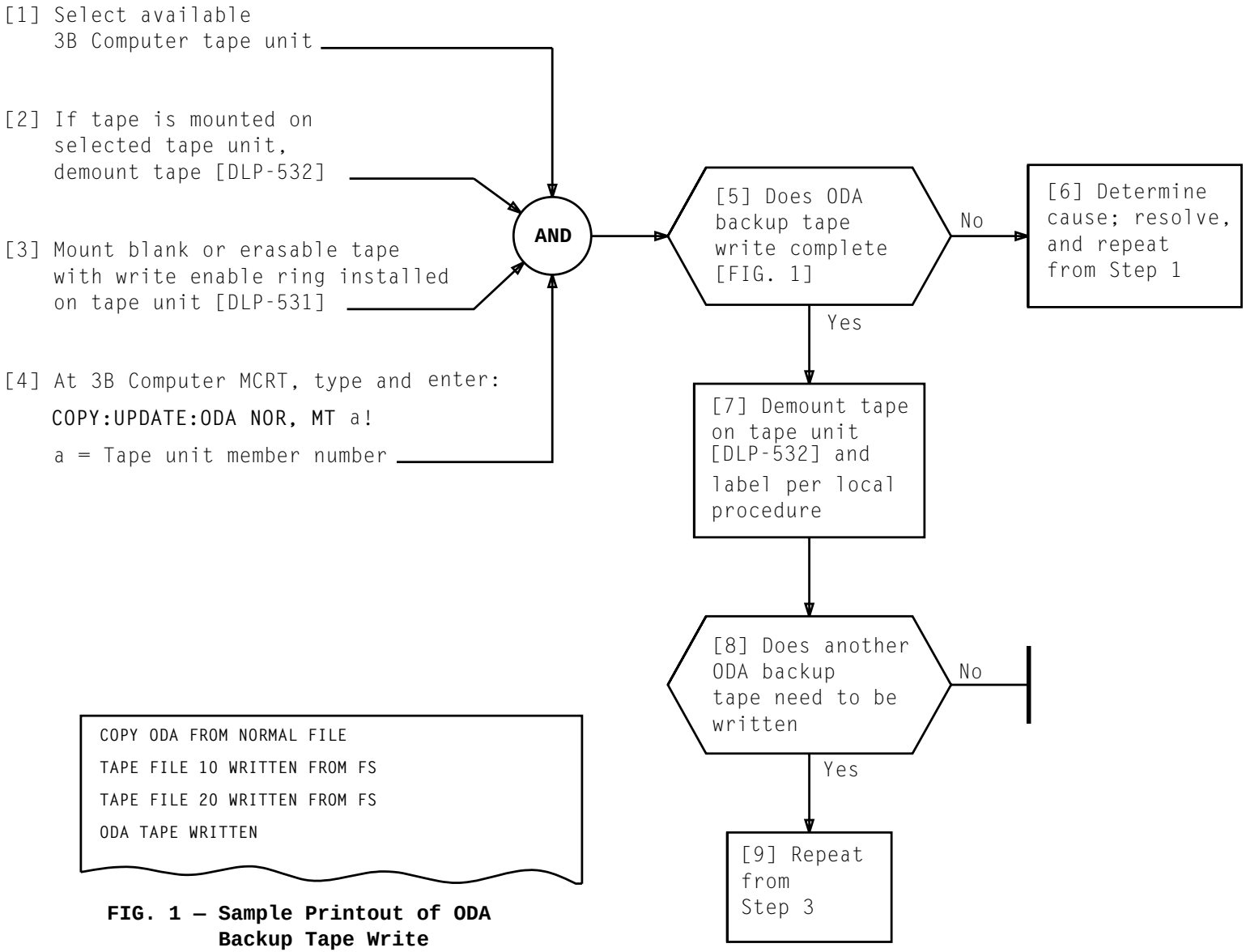
RESEAT NCSU, OSCILLATOR CABLE CONNECTORS



SWITCH NCSU REFERENCE



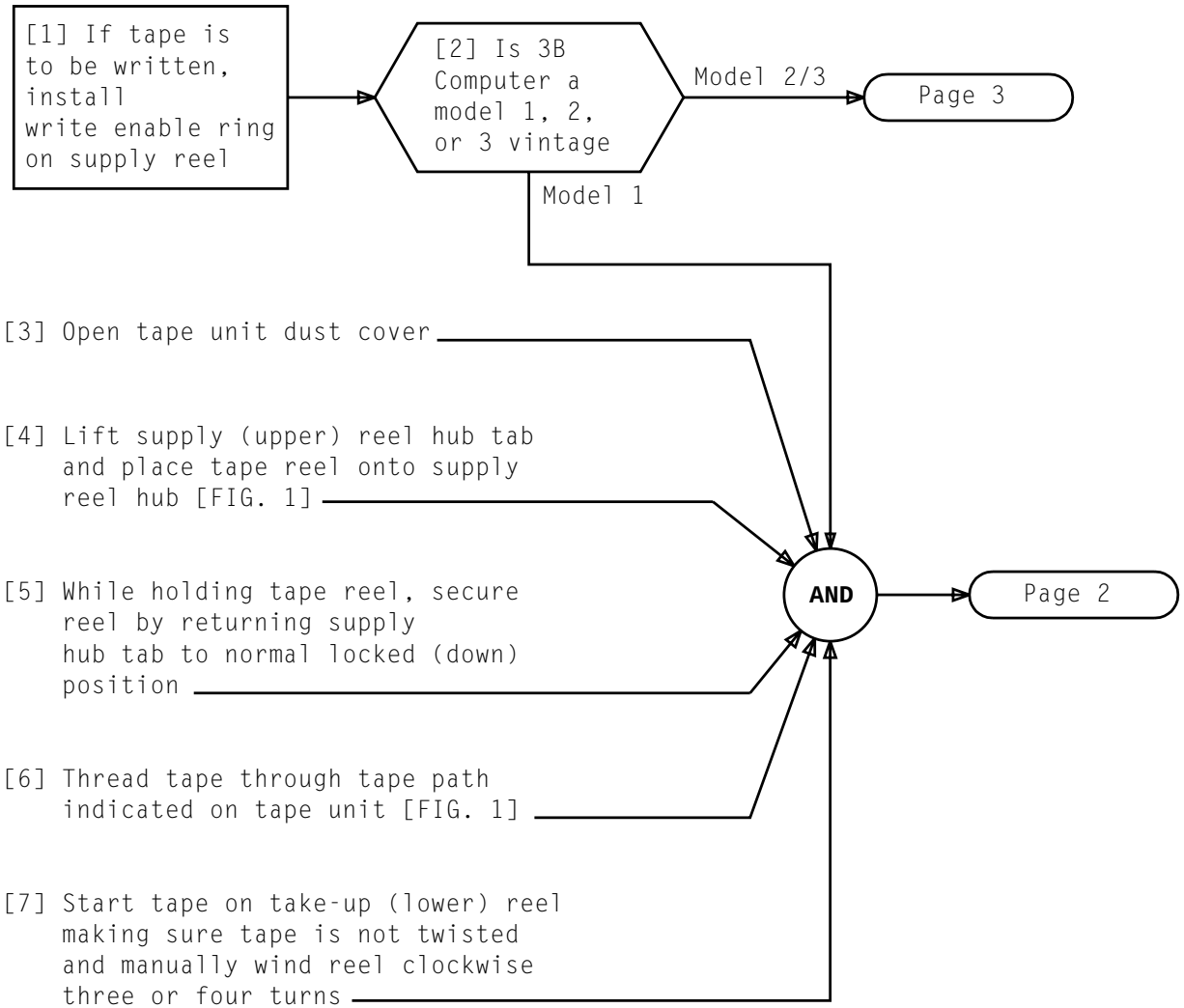
CHECK PHASE LOCK OVEN TEMP METER




```
COPY ODA FROM NORMAL FILE
TAPE FILE 10 WRITTEN FROM FS
TAPE FILE 20 WRITTEN FROM FS
ODA TAPE WRITTEN
```

FIG. 1 — Sample Printout of ODA Backup Tape Write

WRITE 1600 BPI OFFICE DATA ASSEMBLY (ODA) TAPE



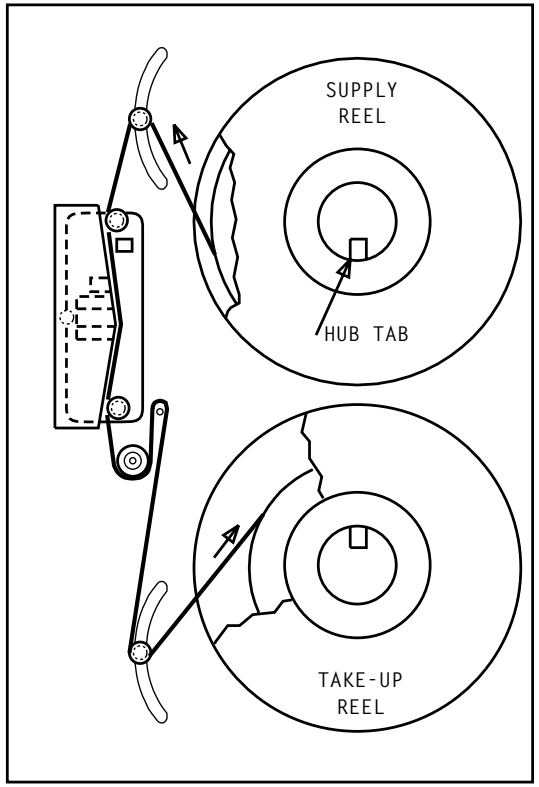
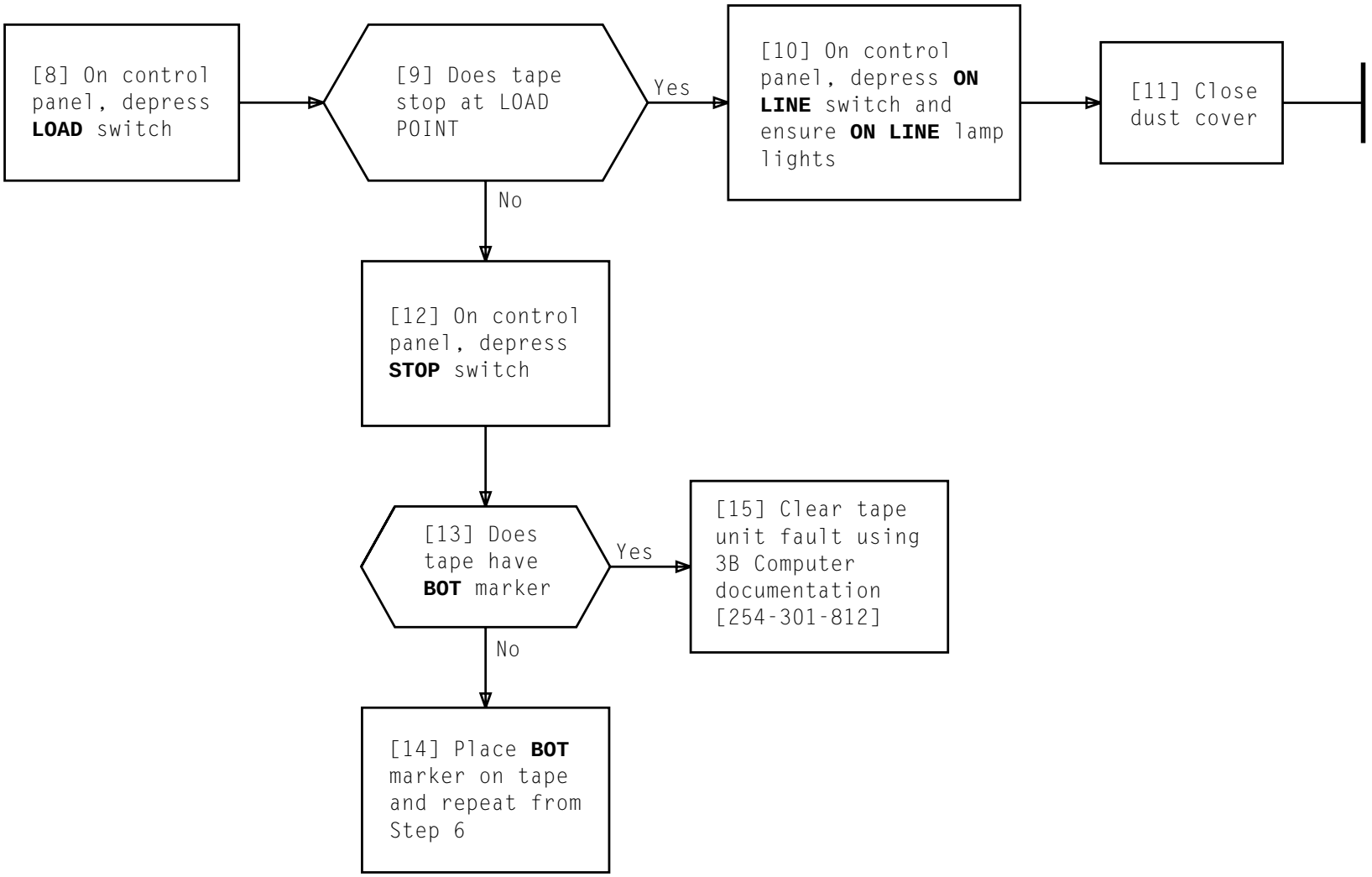


FIG. 1 — 3B Computer Tape Unit

MOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT



MOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT

[16] On control panel, is **LOGIC OFF** LED lighted

Yes

[17] Depress **LOGIC ON** switch

No

[18] Open dust cover

[19] Place supply (upper) reel on hub and depress hub latch [FIG. 2]

[20] Thread tape through tape path indicated on tape drive [FIG. 2]

[21] Start tape on take-up (lower) reel making sure tape is not twisted and manually wind reel clockwise three or four turns

[22] Close dust cover

[23] On control panel, depress **LOAD/REWIND** switch

AND

[24] Does tape load and **BOT** LED light

Yes

[25] Depress **ON LINE** switch

No

[26] Depress **RESET** switch, place BOT marker on tape and repeat from Step 20

No

[27] Request technical assistance from applicable support organization

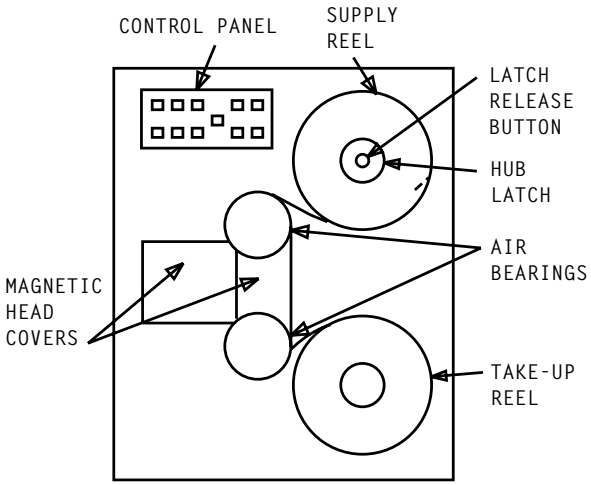
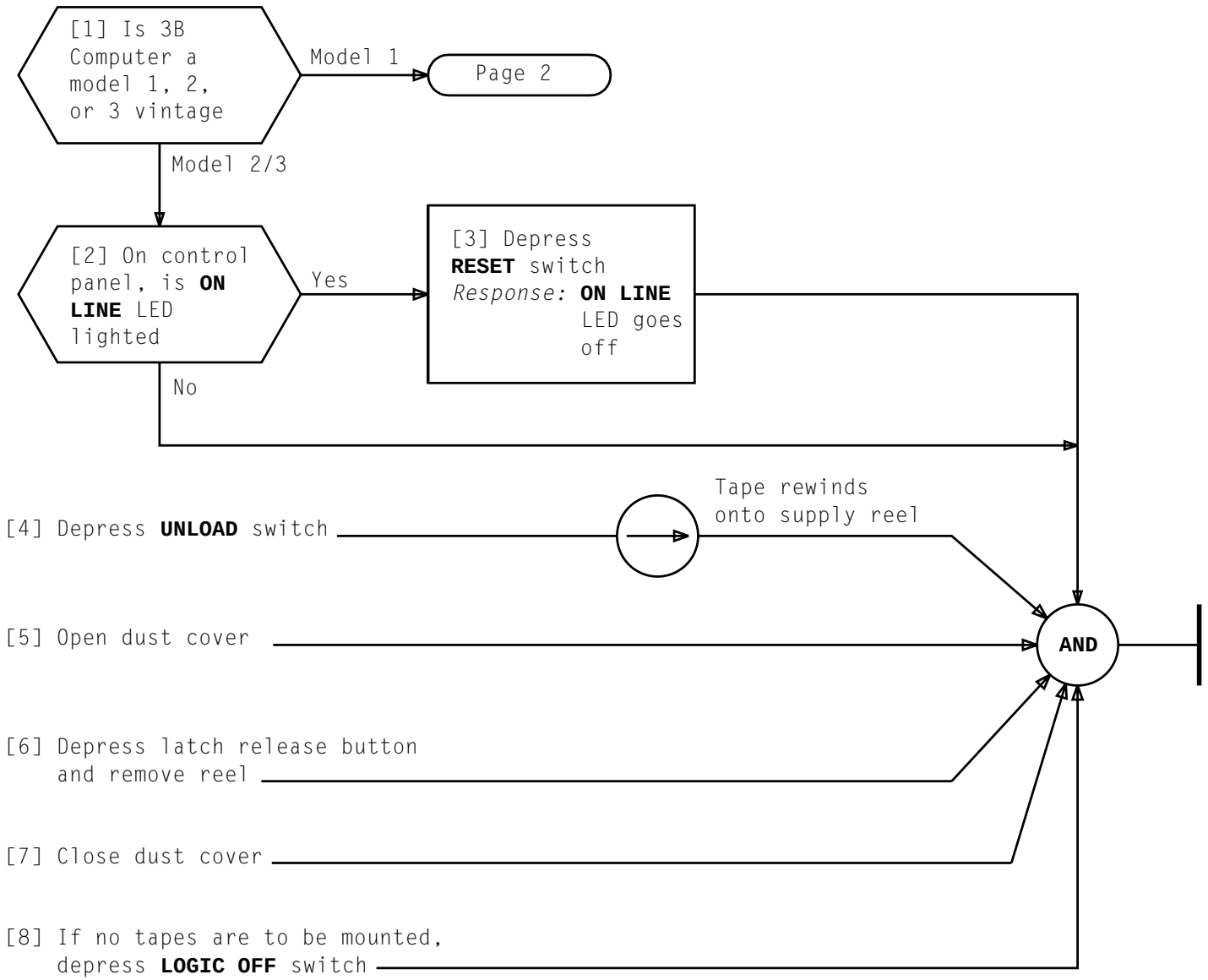


FIG. 2 — 3B Computer Tape Unit

MOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT



DEMOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT

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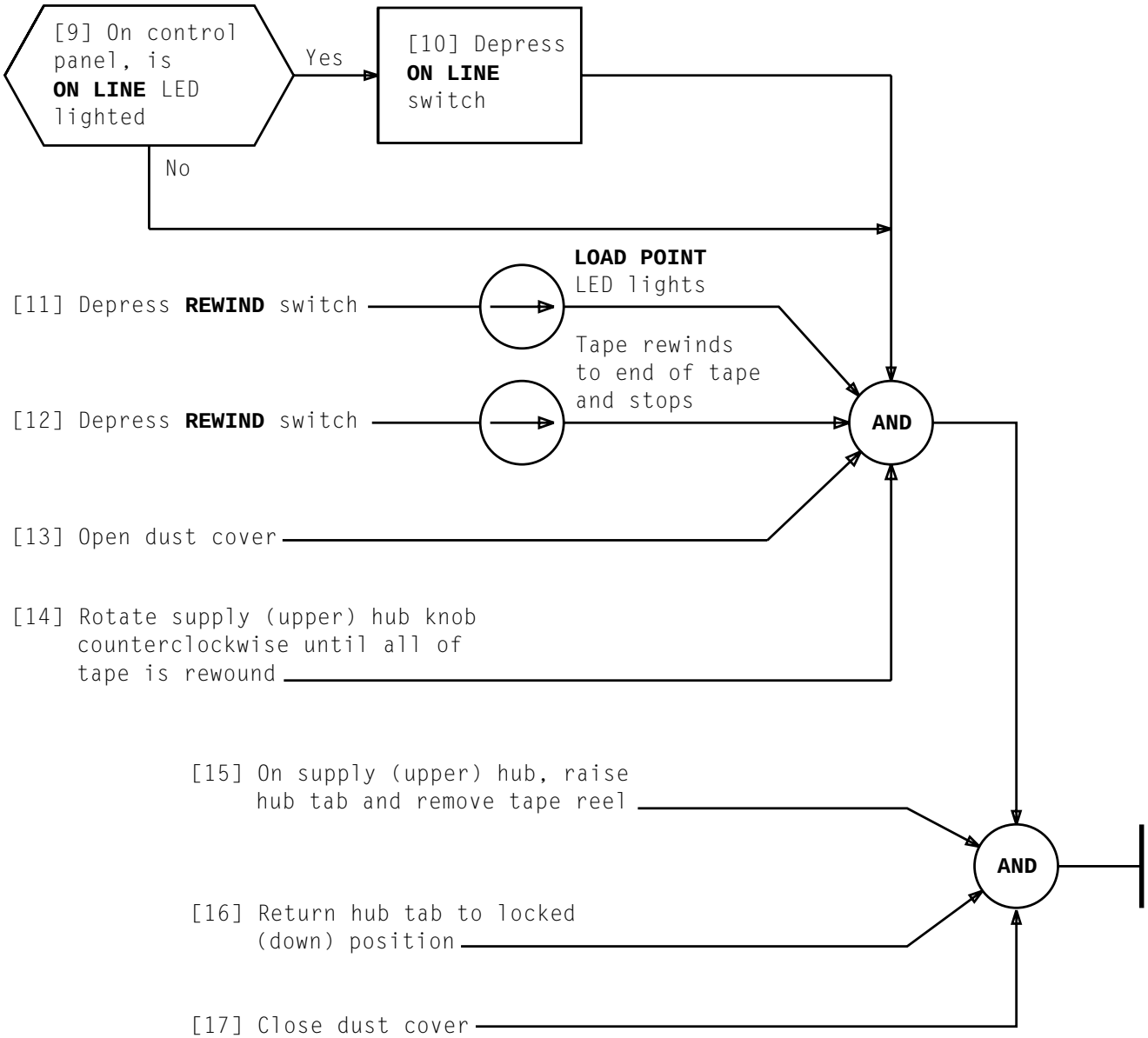

DEMOUNT 1600 BPI TAPE ON 3B COMPUTER TAPE UNIT

1. Define error using PMDs [TABLE A]

TABLE A

PMD-001 apuf (duplex) — no error found

PMD-002 puf (duplex) — no error found — aswf set in act only

PMD-003 puf (duplex) — no error found — aswf set in stby only

PMD-004 puf (duplex) — no error found

PMD-005 Duplex — no cc puf or apuf error source found

PMD-030 Unique error in act only, after hit-timing, then error in act only

PMD-031 Unique error in act only, after hit-timing, then error in stby only

PMD-032 Unique error in act only, after hit-timing, then error in both contrs

PMD-033 Unique error in act only, after hit-timing, then error is gone

PMD-034 Unique error in stby only, after hit-timing, then error in act only

PMD-035 Unique error in stby only, after hit-timing, then error in stby only

PMD-036 Unique error in stby only, after hit-timing, then error in both contrs

PMD-037 Unique error in stby only, after hit-timing, then error is gone

PMD-040 Unique error in both contrs, after hit-timing, then error in act only

PMD-041 Unique error in both contrs, after hit-timing, then error in stby only

PMD-042 Unique error in both contrs, after hit-timing, then error in both contrs

PMD-043 Unique error in both contrs, after hit-timing, then error is gone

PMD-044 Clock phase mismatch found in act only

PMD-045 Clock phase mismatch found in stby only

PMD-046 Clock phase mismatch found in both contrs

PMD-047 Firmware detected errors found in both controllers, no PPE (no ram errors)

PMD-050 Firmware detected errors found in active contr only, no PPE (no ram errors)

PMD-051 Firmware detected errors found in stby contr only, no PPE (no ram errors)

PMD-052 Firmware detected errors found in both controllers with PPE (no ram errors)

PMD-053 Firmware detected errors found in active contr only with PPE (no ram errors)

PMD-054 Firmware detected errors found in stby contr only with PPE (no ram errors)

PMD-055 Stack boundary or sanity timer error found in both or stby contr EXEC pack

PMD-056 Stack boundary or sanity timer error found in active contr EXEC pack only

PMD-057 Stack boundary or sanity timer error found in both contr EXEC pack

PMD-060 Cross controller mismatch in act contr only, no EB intj source found

DEFINE PMD DICTIONARY NODES — SCS

TABLE A (Contd)

PMD-061 Cross controller mismatch in stby contr only, no EB intj source found	PMD-111 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in both contrs
PMD-062 Cross controller mismatch in both contr only, no EB intj source found	PMD-112 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, passes in both contrs
PMD-070 The peripheral order is no good	PMD-113 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in act only
PMD-071 Unique error in act contr, retry the order and act still has unique error	PMD-114 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in stby only
PMD-072 Unique error in act contr, retry the order and act has no error	PMD-115 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order fails in both contrs
PMD-073 Unique error in stby contr, retry the order and stby still has unique error	PMD-116 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs, retry order, order passes in both contrs
PMD-074 Unique error in stby contr, retry the order and stby has no error	PMD-117 Firmware detected errors in active contr, no PPE (no ram errors)
PMD-075 puf — stack boundary or sanity timer error found in act contr EXEC pack	PMD-120 Unique errors in act contr during a "no retry allowed" order
PMD-076 puf — stack boundary or sanity timer error found in stby contr EXEC pack	PMD-121 Unique errors in stby contr during a "no retry allowed" order
PMD-103 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in act only	PMD-122 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act contr during a "no retry allowed" order
PMD-104 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in stby only	PMD-123 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby during a "no retry allowed" order
PMD-105 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, fails in both contrs	PMD-124 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in both contrs during a "no retry allowed" order
PMD-106 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in act only, retry order, passes in both contrs	PMD-125 Firmware detected errors in stby contr, no PPE (no ram errors)
PMD-107 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in act only	PMD-126 Firmware detected errors in act contr with PPE (no ram errors)
PMD-110 cpmm or ccmm (IAS_ACT = 0, IAS_STB = 0) found in stby only, retry order, fails in stby only	PMD-127 Firmware detected errors in stby contr with PPE (no ram errors)

TABLE A (Contd)	
PMD-130 apuf (simplex) — no error found	PMD-201 CONSISTENCY CHECK — inaput set in act, reset in stby, ias zero in stby (duplex)
PMD-131 puf (simplex) — no error found	PMD-202 CONSISTENCY CHECK — inaput set in act, reset in stby, ias nonzero in stby (duplex)
PMD-132 simplex — no cc puf or apuf error source found	PMD-203 CONSISTENCY CHECK — inaput reset in act and stby (duplex)
PMD-150 Unique error found, after hit-timing, error still present	PMD-204 CONSISTENCY CHECK — inaput reset in act, set in stby, ias zero in stby (duplex)
PMD-151 Unique error found, after hit-timing, error is gone	PMD-205 CONSISTENCY CHECK — inaput reset in act, set in stby, ias nonzero in stby (duplex)
PMD-152 Mismatch found (cpmm, ccmm)	PMD-206 CONSISTENCY CHECK — inaput reset in act, frame simplex interject from o/s contr (simplex)
PMD-153 Firmware detected errors found, no PPE (no ram errors)	PMD-207 INTERJECT FILTER — consistency check pases, normal digit buffer overflow (entry_configuration)
PMD-154 Firmware detected errors found with PPE (no ram errors)	PMD-217 INTERJECT FILTER — consistency check passes, but no sources found, frame duplex
PMD-155 Stack boundary or sanity timer error found in contr EXEC pack	PMD-220 INTERJECT FILTER — consistency check passes, but no sources found, frame simplex
PMD-170 Peripheral order is no good	PMD-221 INTERJECT CONT — aput set in both contr, but no error source found in neither, frame duplex
PMD-171 Unique error found, retry the order, unique error is still present	PMD-240 INTERJECT FILTER — single ds120 error
PMD-172 Unique error found, retry the order, error is gone	PMD-241 INTERJECT FILTER — single LAN error
PMD-173 Stack boundary or sanity timer error found in contr EXEC pack	PMD-242 INTERJECT FILTER — single invalid state error (active-active or standby-standby)
PMD-174 Firmware detected errors found with PPE (no ram errors)	PMD-243 INTERJECT FILTER — illegal command or data received by scu
PMD-175 cpmm or ccmm found	PMD-244 INTERJECT FILTER — illegal command or data received by controller
PMD-176 Firmware detected errors found, no PPE (no ram errors)	PMD-245 INTERJECT FILTER — receive FIFO full
PMD-177 Unique error found during a "no retry allowed" order	
PMD-200 CONSISTENCY CHECK — inaput set in act and stby, ias zero in stby (duplex)	

TABLE A (Contd)

PMD-246	INTERJECT FILTER — scu hard error, bad scu
PMD-247	INTERJECT FILTER — multiple ds120 errors on the same TSI
PMD-250	INTERJECT FILTER — multiple ds120 errors on different TSIs
PMD-251	INTERJECT FILTER — multiple LAN errors
PMD-252	INTERJECT FILTER — multiple invalid link state, hardware status indicates software act contr is active
PMD-253	INTERJECT FILTER — multiple invalid link state, hardware status indicates software act contr is not active
PMD-260	ccmm found during apuf, IAS_ACT = 0, IAS_STB = 1
PMD-261	ccmm found during apuf, IAS_ACT = 1, IAS_STB = 0
PMD-262	ccmm found during apuf, IAS_ACT = 1, IAS_STB = 1
PMD-270	ccmm found during puf, IAS_ACT = 0, IAS_STB = 1
PMD-271	ccmm found during puf, IAS_ACT = 1, IAS_STB = 0
PMD-272	ccmm found during puf, IAS_ACT = 1, IAS_STB = 1
PMD-301	BASE FILTER — autonomous report
PMD-311	BASE FILTER — illegitimate report
PMD-330	ram errors found in stby only or both controllers
PMD-331	ram errors found in act contr (stby may have f/w detected error)
PMD-332	fatal firmware detected errors found in both controllers (no ram errors)
PMD-333	fatal firmware detected errors found in active controller (no ram errors)
PMD-334	fatal firmware detected errors found in stby controller (no ram errors)
PMD-340	ram errors in active controller
PMD-341	ram error in stby controller
PMD-343	fatal firmware detected errors found in active controller (no ram errors)
PMD-344	fatal firmware detected errors found in stby controller (no ram errors)
PMD-350	ram errors
PMD-353	fatal firmware detected errors found (no ram errors)
PMD-360	ram errors
PMD-363	fatal firmware detected errors found (no ram errors)
PMD-373	hardware access test failure
PMD-374	interrupt from a growth frame
PMD-375	interrupt from an unequipped frame
PMD-377	interrupt from a duplex failed frame

ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE	ITEM	ISSUE
• IXL-001		ISD-133		• DLP-522							
NTP-002		ISD-134		• DLP-523							
• TAD-100		TAP-135		• DLP-524							
TAP-101		TAP-136		• DLP-525							
TAP-102		TAP-137		• DLP-526							
• TAP-103		TAP-138		• DLP-527							
TAP-104		TAP-139		• DLP-528							
TAD-105		• TAP-140		• DLP-529							
TAP-106		• TAP-141		• DLP-530							
TAP-107		• TAP-142		• DLP-531							
TAP-108		• TAP-143		• DLP-532							
TAP-109		• TAP-144		• DLP-533							
TAP-110		• TAP-145		• CKL-891							
TAD-111		DLP-500		TNG-893							
TAP-112		DLP-501									
• TAP-113		DLP-502									
TAP-114		DLP-503									
TAP-115		DLP-504									
TAD-116		DLP-505									
TAD-117		DLP-506									
TAP-118		DLP-507									
TAP-119		• DLP-508									
TAP-120		DLP-509									
• TAP-121		DLP-510									
TAP-122		DLP-511									
TAP-123		DLP-512									
• TAP-124		DLP-513									
TAP-125		DLP-514									
TAP-126		DLP-515									
TAP-127		DLP-516									
TAP-128		DLP-517									
• TAP-129		• DLP-518									
TAP-130		• DLP-519									
TAP-131		• DLP-520									
TAP-132		• DLP-521									

• REVISED OR ADDED ITEM □ CANCELED ITEM

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