4ESS™ Switch
1B Processor
General Description

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1. Overview

1.01 This practice describes the 1B Processor which is a replacement for the 1A Processor and explains how the 1B Processor functions. Detailed information concerning the operation of the 1B Processor is provided to a wide range of users. This information is a broad, high-level description of the 1B Processor.

1.02 This practice is being reissued to include the following:

- Corrections necessary for the 4E24 generic.
- Various corrections in formatting text.

1.03 This practice does not contain safety labels.

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1.06 Every effort was made to ensure that the information in this practice was complete and accurate at the time of printing. However, information is subject to change.

1.07 This document was developed by Lucent Technologies Customer Training and Information Products.
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1.08 Information contained in this practice is organized as follows:

(1) Part 2 describes the purpose and characteristics of the 1B Processor.

(2) Part 3 contains a high-level description of the 1B Processor. This description identifies the functional areas of the 1B Processor community and describes the operations performed by each area.

(3) Part 4 provides a physical description of the 1B Processor complex and other frames in the 1B Processor community.

(4) Part 5 contains a detailed description of the 1B Processor signal and control circuits.

(5) Part 6 describes the 1B Processor power distribution system, grounding system, and power-related alarm circuits.

(6) Part 7 describes the design of 1B Processor complex (*Fastech** Packaging System technology).

(7) Part 8 describes the 1A Technology used in the input/output (I/O), input/output processor (IOP), data unit selectors (DUS), tape unit controller (TUC), and power conversion and distribution (PCD) frames.

(8) Part 9 contains a reference to 1B Processor maintenance documents.

(9) Part 10 contains a reference to 1B Processor growth documents.

(10) Part 11 contains a reference to other 1B Processor documents.

(11) Part 12 provides a list of abbreviations and acronyms used in this practice.

* Registered trademark of Berg Technology, Inc.

2. General

Purpose of the 1B Processor

2.01 The 1B Processor is a replacement for the 1A Processor and controls *4ESS*™ switch. The 1B Processor solves the 1A Processor problem of memory and real-time exhaustion. The 1B Processor has twice the memory space and a processing speed of 2.4 times faster. Figure 1 shows the replacement of the processor hardware.

2.02 The 1A Processor will be replaced by the 1B Processor in the 4E18 generic time frame. The 4E18 and 4E19 generics will have the same feature content. The 4E18 generic will be 1A based, while the 4E19 generic will be 1B based.

Comparison of 1A and 1B Processors

2.03 The major differences between the 1A and 1B Processors are summarized in Table A.

A. 1B Processor Hardware

2.04 The following features are in the 1B Processor but not in the 1A Processor:

- Interface bus (IFB) that supports direct memory access (DMA) and memory mapped input/output (MMIO) access
- Twelve IFB client unit pairs (or 24 individual units). Eight pairs are dedicated for auxiliary unit interface (AUI), maintenance control center (MCC)/Utility Processor (MUP), and scanner and signal distributor (SSD). Eight individual units are available for future use (two slots are used for each MUP.)
- 28-K word boot read-only memory (ROM) which supports booting the system, processor reconfiguration, interrupt handling, and low-level (dead start) system tests
- Forced air cooling fans.

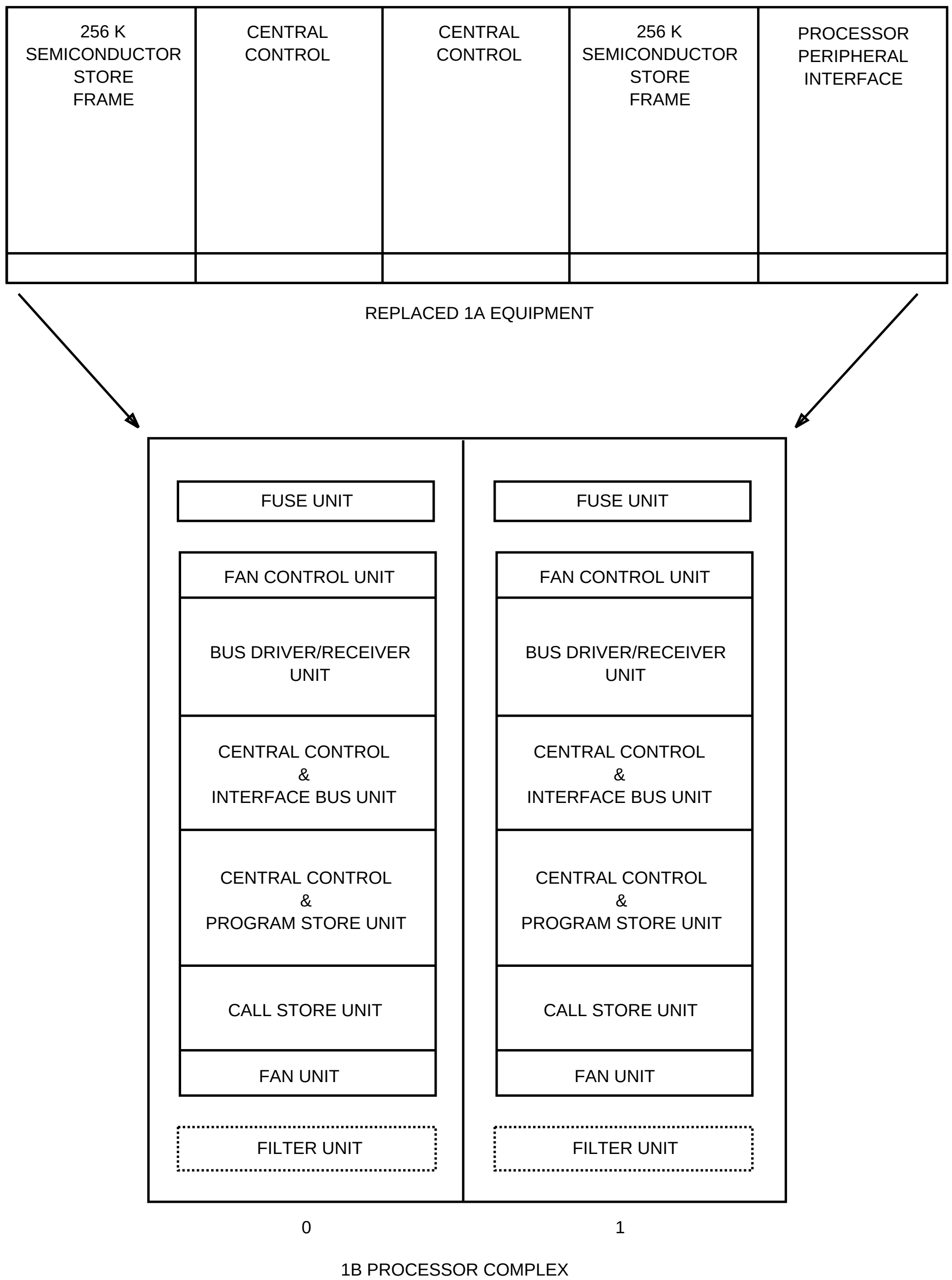


Figure 1. Replacement of Processor Hardware

B. 1B Integrated Utility System

2.05 A 1B Utility System is fully integrated into the 1B Processor. The hardware that provides an interface to the Utility System is the 1B Processor MUP, Ethernet, and a *SUN** computer workstation. The Utility System can be used for the following:

- Laboratory development
- Factory system test
- Field installation
- 1A to 1B generic retrofit
- Field debugging.

The *SUN* computer workstation is removed after the installation of the 1B Processor.

Processor Characteristics

2.06 The 1B Processor is a stored program-controlled data processing machine which operates in a real-time environment. The hardware and software of the 1B Processor are configured so the processor can control its peripheral switching network.

2.07 The MCC video display terminal is provided to monitor the overall operation of the processor and to exercise manual control over processor operations. There are terminals connected to input/output processor that can be used to control the *4ESS* switch. These input/output terminals interface with the 1B Processor via software-defined input/output channels.

2.08 To provide continuous trouble-free operation, the 1B Processor equipment units are duplicated. Failure in one unit will not reduce processor capability. Internal and external interfaces are also duplicated so that any problem encountered in transferring data either within the 1B Processor or external to the peripheral switching network will not result in a system failure. The 1B Processor units are automatically diagnosed by maintenance software on a regular basis. A malfunctioning unit detected during this diagnosis is removed from service and the standby unit is switched on line.

* Registered trademark of SUN Microsystems, Inc.

Table A. 1A/1B Processor Comparison

Attribute	1A Processor	1B Processor
Software Addressing	22-bits*	23-bits and 30-bits¶
Maximum Accessible Memory	4 MW*	8 MW
Program Store (PS) Memory Spectrum	2 MW - 32 KW	2 MW
Call Store (CS) Memory Spectrum	2 MW*	5 MW
Extended Call Store (XS) 4E21	N/A	14MW**
Extended Program Store (PSE) 4E22	N/A	1MW-64KW††
Extended MMIO (XM) 4E21	N/A	256MW
Memory Mapping Input/Output (MMIO) Memory Spectrum	N/A	32 KW
PS/CS Address Buses	21-bits	29-bits
CS/PS Word Size	26-bits (24 data, 2 parity)	36-bits (32 data, 4 parity)
Clock Speed	1.43 MHz	6 MHz
Cycle Time	700 nsec	166.67 nsec
Memory Access	1 cycle	1 cycle
1A/1B Cycle Ratio	N/A	1.6
PS/CS Unit Size	256 K words	1M words
Maximum PS/CS Equipage	10/14 units	6/40 units
On-line PS/CS Units	8/8 units*	3/20 units
Spare PS/CS Units	2/8 units*	3/20 units
Floor Space	9'9" x 2	5'5" x 2†
Number of Circuit Packs	1168 x 2	50 x 2
Capacity in busy hour call attempts (BHCAs)	520 K	1.4 M‡
Maximum Terminations	60 K	107 K
Processor Downtime	3.4 min/yr§	< 3.4 min/yr
Central Control (CC) Failure in Time (FIT)	478 K	458 K
Master Control Console (MCC)	Hard-wired Panel	Color CRT
Field Utility System	Generic Utility Program (GULP)	Optional SUN4 + GULP
Lab Utility System	Laboratory Support System (LSS)	SUN4 Network
Auxiliary Unit Bus (AUB) Ports	4 of 16 used	4 of 4 used
Interface Bus (IFB) Clients	N/A	16 of 24 clients used
Availability	prior to 4E19	4E20

Table A. 1A/1B Processor Comparison (Contd)

* 1A with extended call store (ECS) actually has 23-bit addressing (via the M-bit) and an increase in the maximum number of CSs from the 16 shown above to 22 (the largest offices currently use only 13 CSs. The existing memory frame can house 3 additional CSs, while a new external frame can house an additional 6 CSs). This allows an additional 1.75 MW of ECS memory spectrum (for a total of 3.75 MW of CS memory spectrum).

† Each of the two simplex cabinets is 7’ high, 2.2’ wide, and 22" deep (4" deeper than the 1A frames). The plan includes 2 future growth cabinets (needed for some IFB clients) that will need an additional 5’ 5" of aisle space. One growth cabinet will be located on each side of the initial cabinet complex.

‡ 1.4-M BHCAs is 2.4 times the 1A capacity of 520-K BHCAs. This is the effective speed up measured in real work.

§ The current 1A Processor downtime is 3.4 minutes/year. The *4ESS*™ switch downtime requirement is 3 min/yr and is composed of the following components: 1A Processor, PUB & PUs, AUB & AUs, Attached Processor Interface (API). The following components are not included: Attached Processor System, Common Network Interface (CNI) Ring.

¶ 1B Processor uses 30-bit addressing using window circuitry to gain access to 256 MW extended address spectrum.

** This is above and beyond the 5 MW of standard call store.

†† This is above and beyond the 2 MW of standard program store.

2.09 Both frames which make up the 1B Processor complex are designed and constructed using *Fastech* Packaging System technology. This internally developed technology provides a dense, high-performance, standardized interconnection technology. Circuit packs are either 7.67 by 13.375 inches or 15.67 by 13.375 inches.

2.10 The attached processor interface (API) frame is also designed and constructed according to the *Fastech* System of packaging electronic hardware.

Special Notation

2.11 Throughout this document, some numbers are represented in octal form. These numbers are preceded with the symbol ϕ (for example, ϕ 14).

3. System Overview

3.01 Figures 2 and 3 show block diagrams of the 1B Processor complex divided into the following major areas:

a. Central control (CC)

b. Program store (PS)

c. Program store bus (PSB)

d. Call store (CS)

e. Call store bus (CSB)

f. Auxiliary unit interface (AUI)

g. Scan and signal distributor (SSD)

h. Interface bus (IFB)

i. MCC and utility processor (MUP)

j. MCC terminal.

Figure 2 shows the 1B Processor with the DUS and TUC attached for 4E21 and earlier generics. Figure 3 shows the DUS and TUC functionally removed for 4E22 and later generics.

3.02 The following equipment is also associated with the 1B Processor:

(a) Attached processor interface (API)

(b) Attached processor system (APS)

(c) Auxiliary data system (ADS)

(d) Input/output (I/0) interface.

Central Control (CC)

3.03 The CC controls the 1B Processor community. The CC interfaces with the peripheral units through the peripheral unit bus (PUB) and peripheral unit bus branching frame (PUBB). The CC performs the processing functions in the 1B Processor. Under program control, the CC controls all areas of the 1B Processor community to carry out the function assigned to the 1B Processor. This function is to control the peripheral units in the *4ESS* switch so that telephone calls are switched in a reliable manner. The CC also executes program-controlled maintenance routines which check operations of the 1B Processor and the *4ESS* switch.

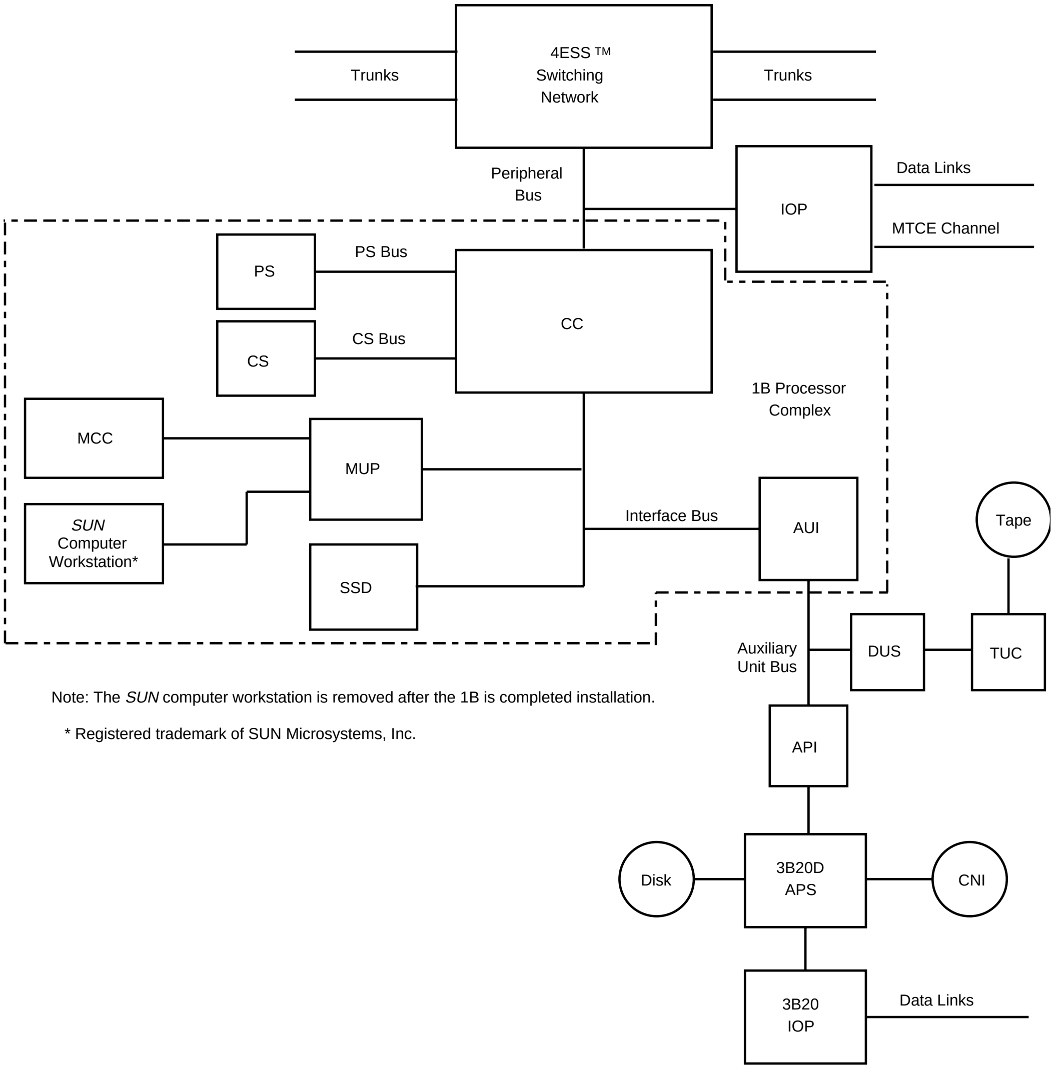
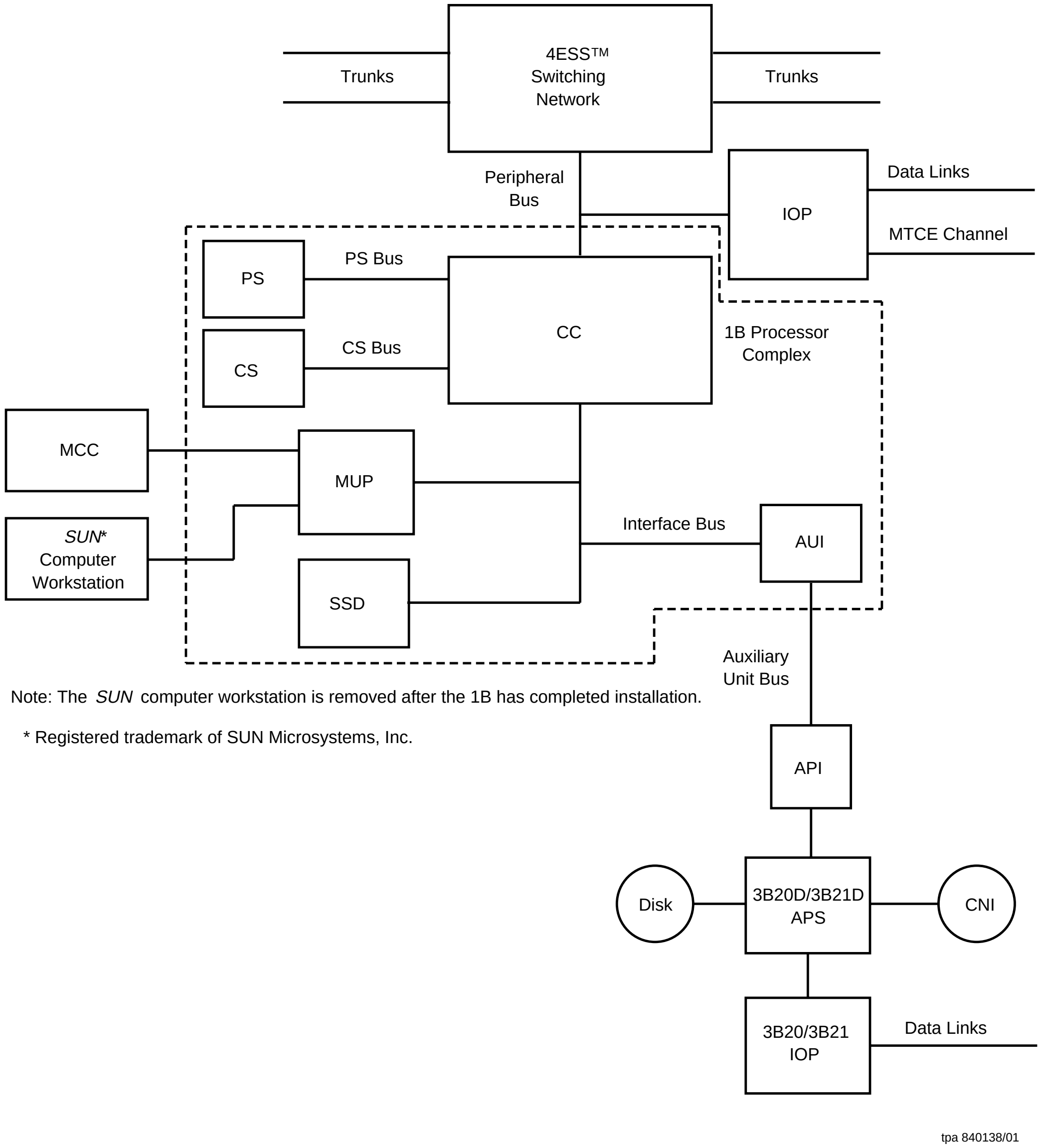


Figure 2. 1B Processor Functional Block Diagram for 4E21 and Earlier Generics



Note: The *SUN* computer workstation is removed after the 1B has completed installation.

* Registered trademark of SUN Microsystems, Inc.

Figure 3. 1B Processor Functional Block Diagram for 4E22 and Later Generics

Program Store (PS)

3.04 Program store is a high-speed semiconductor memory used primarily for the storage of program instructions. Program store contains 1B Processor and *4ESS* switch configuration data that is rarely changed. This type of data is also stored in call store. Unlike the 1A Processor that had separate cabinets for program store and call store, program store and call store are located in the 1B Processor cabinet.

Program Store Bus (PSB)

3.05 The PSB is used to connect the PSs with the CCs. The PSB is a fully duplicated bus. The PSB consists of 29 bits of address, 32 bits of write, 64 bits of data on its reply, and control signals.

Call Store (CS)

3.06 Call store is a high-speed semiconductor memory (similar to program store) used for the storage of translation data and frequently changed call-processing data. The frequently changed data includes, but is not limited to the following:

- Status of trunks and switching network
- Records of network terminations used for each call in progress
- Transient call data (such as digits received and digits to be outpulsed)
- Maintenance data related to programmed diagnostic tests.

Call Store Bus (CSB)

3.07 The CSB is used to connect the CSs with the CCs. The CSB is a fully duplicated bus. The CSB contains 29 bits of address, 32 bits of write, 32 bits of data on its reply, and control signals.

Interface Bus (IFB)

3.08 The IFB is an I/O bus that supports word block and device to device transfers. The IFB permits new application circuit packs (called IFB clients) to be connected to the CC in the 1B Processor. The IFB clients may include I/O and network controllers, adjunct processors, and data bases. The IFB provides the connection for the SSD, MUP, and the AUI to the 1B processor.

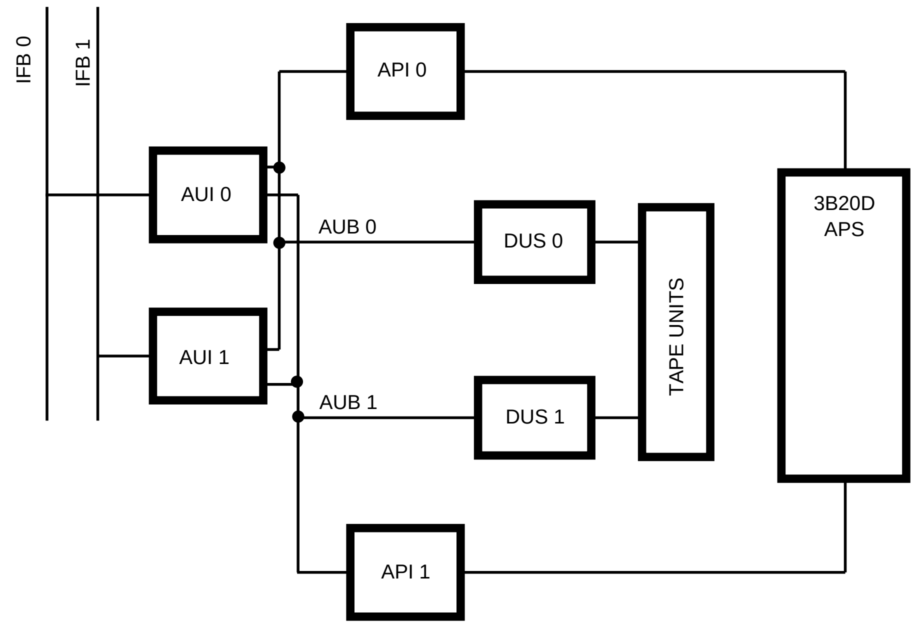


Figure 4. Auxiliary Unit Community for 4E21 and Earlier Generics

Auxiliary Unit Interface (AUI)

3.09 The AUI provides the connection between the CC and the existing APS (Figures 4 and 5). The AUI will support the following clients currently on the 1A auxiliary unit bus (AUB):

- Two attached processor interfaces (APIs) [API 0 and API 1]
- Two data unit selectors (DUSs) [DUS 0 and DUS 1].

NOTE:
The DUSs apply to 4E21 and earlier generics (See Figure 4). The DUSs will be effectively removed with 4E22 and later generics (See Figure 5).

The AUI will interface to both AUBs (0 and 1), and an AUI will be provided on each IFB. This interface is not designed to be a growth path for adding capabilities to the 1B Processor. Additional capabilities will be added directly on the IFB.

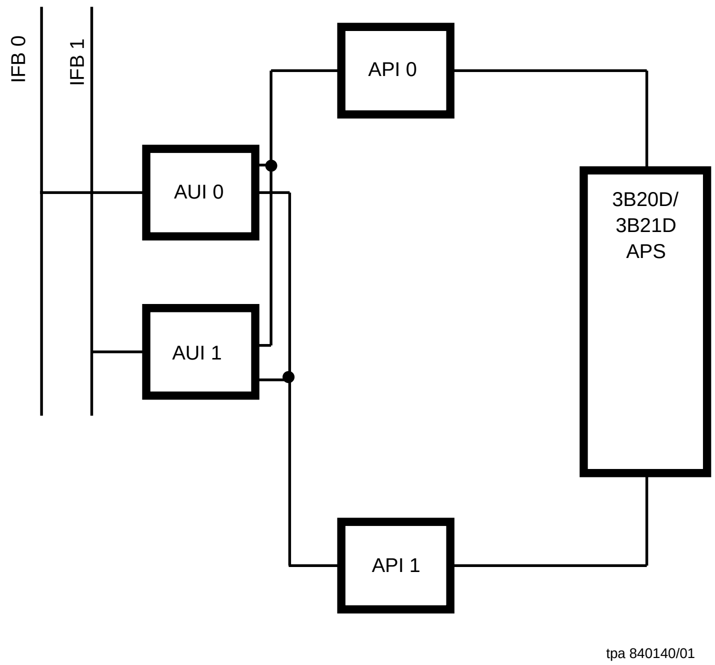


Figure 5. Auxiliary Unit Community for 4E22 and Later Generics

Scan and Signal Distributor (SSD)

3.10 Two SSD circuit packs replace the SSD function of the processor peripheral interface (PPI) frame in the 1A Processor. The SSD provides the required SSD points for all processor units; API, DUS, TUC, IOP, and PUBB.

NOTE:
The DUS and tape unit controller (TUC) apply to 4E21 and earlier generics. The DUS and TUC will be effectively removed with 4E22 and later generics.

MCC and Utility Processor (MUP)

3.11 The MUP is a microprocessor system that provides the control for the MCC video display terminal (VDT) and the Utility System. The MUP memory stores the MUP operating system, on-board diagnostics, the MCC driver code, and the Utility System MUP-resident code. The MUP connects to the interface bus and contains four RS-232C ports for connection to MCC VDTs. An Ethernet port is provided for connection to the *SUN* computer workstation.

MCC Video Display Terminal (VDT)

3.12 The MCC VDT is a computer terminal that provides control and display functions either at the switch or at a remote site such as the Technical Control Center (TCC). The MCC terminal is a replacement for the electromechanical master control console used in the 1A Processor. The MCC terminal is similar to the maintenance terminal on the 3B20D/3B21D computer. Furthermore, the MCC terminal provides control over the 1B Processor and the switch, and displays various processor and switch attributes. Control refers to the ability to change the state of the 1B Processor or *4ESS* switch components, ranging from causing an indicator to be turned on or off, to forcing a processor reconfiguration. Display refers to the functions involved in providing status indications of the various components of the 1B Processor and *4ESS* switch peripheral equipment.

Attached Processor Interface (API)

3.13 The API frame is a common hardware and software package used to effectively interconnect the 1B Processor to a duplex 3B20D/3B21D computer in the Attached Processor System (APS). The direct memory access (DMA) facilities are interconnected so that data and interprocessor messages can be effectively transferred between the two processors. The common software consists of 1B Processor and 3B20D/3B21D computer resident programs. The programs administer and maintain a high-speed, fully duplicated interprocessor communication link.

Attached Processor System (APS)

3.14 An APS consists of a 3B20D/3B21D computer which is used as an additional stand-alone processor by the 1B Processor. The primary use of a 3B20D/3B21D computer is to provide backup storage for program store and portions of call store memory. The same APS (3B20D/3B21D computer) also supports other features such as CCS7 signaling.

Auxiliary Data System (ADS)

3.15 The ADS provides the 1B Processor with a magnetic tape facility that stores and retrieves data. The magnetic tape facility is used for system reinitialization, memory dumps, automatic message accounting, program updating, and general data handling. The ADS interfaces with CC control via DUSs and AUIs.

NOTE:
The magnetic tape facility to the 1B Processor applies to 4E21 and earlier generics. The DUS and TUC will be effectively removed with 4E22 and later generics.

Input/Output (I/O) Interface

3.16 The I/O interface serves as an interface between the 1B Processor and I/O terminals located in the *4ESS* switch. These terminals are used to input control messages to software and to receive output responses and status messages from software. These terminals may also have general purpose usages as data sets for remote use, cathode ray tube applications, etc. The I/O interface may be provided via either an I/O frame or I/O processor frame.

4. Equipment Description

1B Processor

4.01 Two standard floor plan arrangements (A and B) are shown in Figure 6 for *4ESS* switches converting to the 1B Processor. The 1B Processor will be equipped either to the right (Figure 6-A) or to the left (Figure 6-B) of the PPI and IO/IOP 0 frame. When equipped to the left of the PPI, the IO/IOP 0 frame will be relocated to the right of the PPI. A minimum of one frame location on each side will be left vacant for future growth. There will be a 3-foot space at the front and rear of each frame lineup.

1B Processor Complex Frame (J4A023A)

4.02 Duplex 1B Processors are contained within a two-cabinet complex (Figure 7). Each cabinet contains the following units beginning at the top of the frame:

- Fuse Unit J4A023AG
- Fan Control Unit J4A023AA
- CC and Interface Bus Unit (J4A023AB)
- CC and Program Store Unit (J4A023AC)
- Call Store Unit (J4A023AD)
- Fan Unit (J4A023AF)
- Filter Unit (J4A023AH).

4.03 The two cabinet complex is approximately 7 feet high, 5 feet 4 inches wide, and 1 foot 10 inches deep. The bezel contains alarm LEDs that indicate the condition of the cooling system and fuse unit.

4.04 The Cooling System consists of the fan and fan control/alarm units. The Cooling System for the 1B Processor complex consists of two physical units. The lower unit contains six variable speed fans, inlet air temperature sensors, and an air filter. These are located in the base of the frame. The upper control unit contains duplicated fan controllers and duplicated temperature sensors for each outlet air channel. The output of the fan control unit adjusts the speed to keep temperatures inside the cabinet within the control limits. An output for lighting cooling status LEDs on the bezel is provided as well as an interface to the SCAN/SD matrix for sending cooling error messages and for reporting status of the unit.

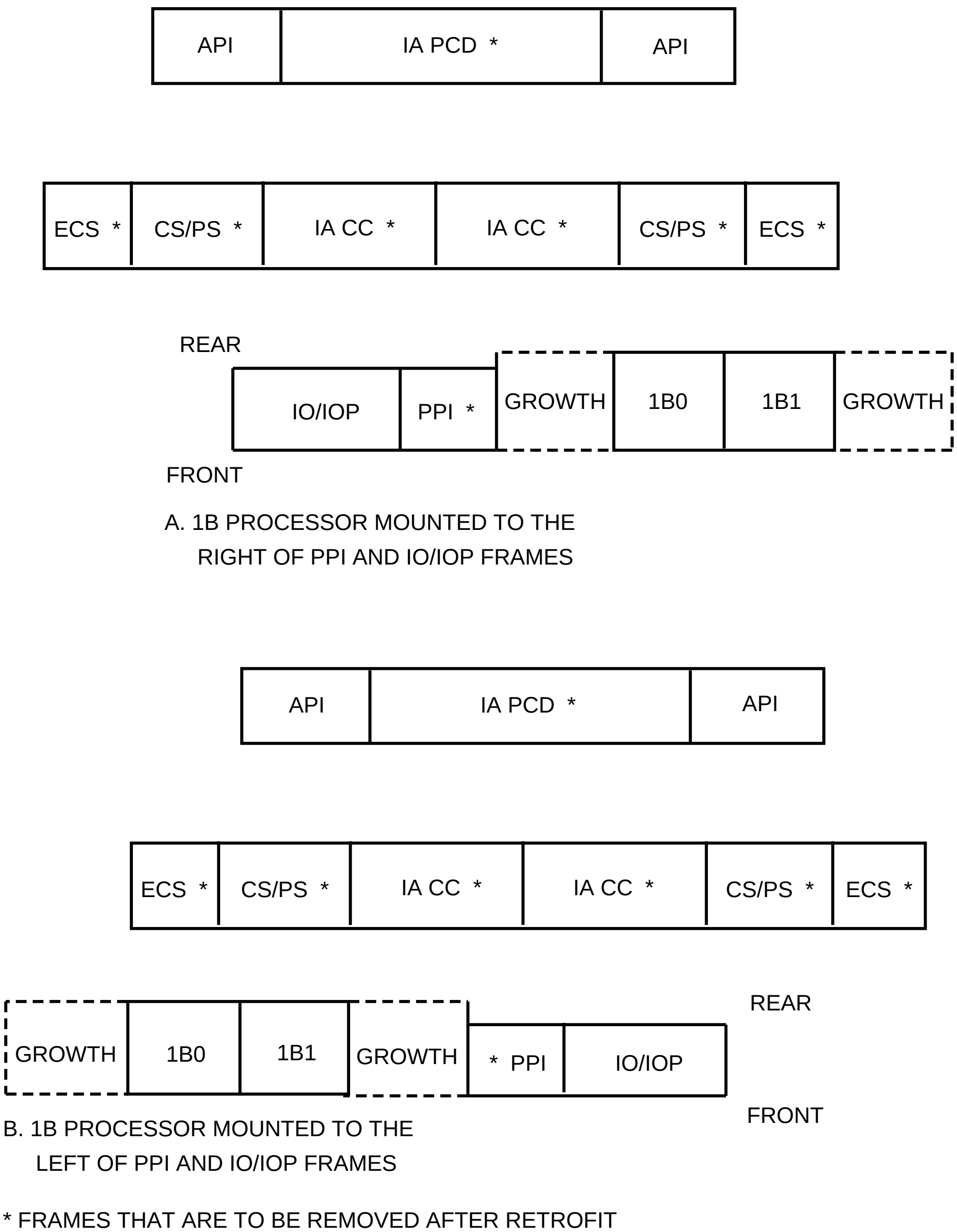


Figure 6. 1B Processor Standard Floor Plan Arrangements

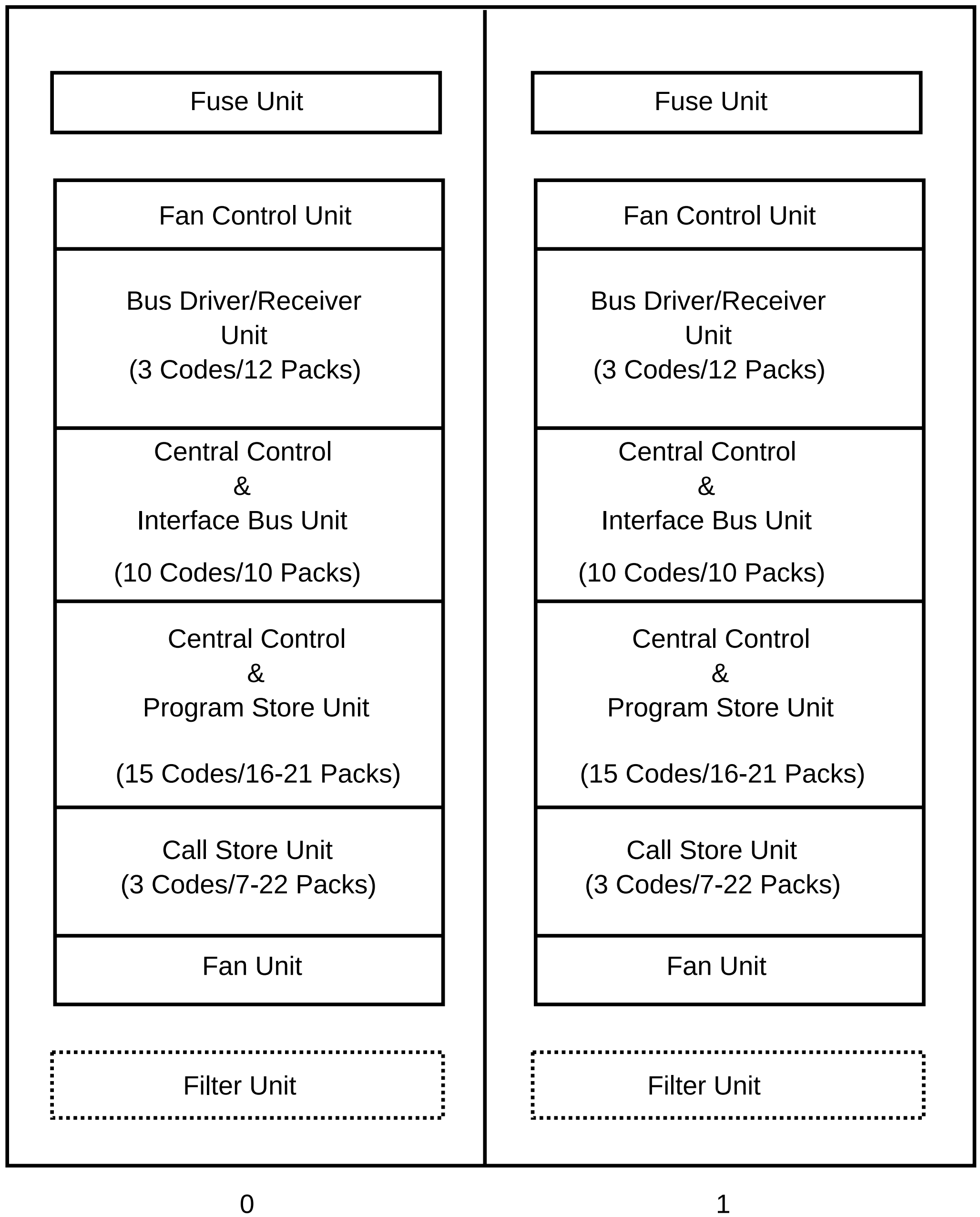


Figure 7. 1B Processor Complex

Attached Processor Interface Frame (J5A012A)

4.05 The Attached Processor Interface (API) system is a fully duplexed system made up of two identical API frames 0 and 1. The APIs interface the 1B Processor with the APS over the auxiliary unit bus, auxiliary unit interface and interface bus. The APS is one 3B20D/3B21D computer which is a fully duplexed computer system.

4.06 The API frame is a single-bay frame, 7 feet high and 3 feet 3 inches wide, and 1 foot 6 inches deep. Each API frame contains one DUS J5A004AZ-1 and one API unit J5A012AA-1.

Auxiliary Data System (ADS)

4.07 The ADS is a versatile, medium-speed, data handling system using magnetic tape storage. The ADS is used for relatively slow-speed data storage and retrieval functions. The ADS community contains the following subassemblies:

- DUSs
- TUCs (also called tape control and logic units)
- Tape units (TUs).

4.08 The ADS community contains two DUSs. The DUSs are assigned as a pair (DUS 0 and DUS 1). DUS 0 is located in API cabinet 0, and DUS 1 is located in API cabinet 1. DUS 0 interfaces with auxiliary unit bus 0, and DUS 1 interfaces with auxiliary unit bus 1. The TUCs and tape units are mounted in tape frame J5A002A. A tape frame contains one TUC, one tape unit, and a power converter. The pair of DUSs can support a maximum of 16 tape frames. The distance between a DUS and a tape frame cannot exceed 250 feet.

NOTE:
The DUSs, TUCs, and tape units connected to the 1B Processor apply to 4E21 and earlier generics. The DUSs, TUCs, and tape units connected to the 1B Processor will be effectively removed with 4E22 and later generics.

Input/Output Frame (J5A006A)

NOTE:
The I/O frame is not in every *4ESS* switching office.

4.09 The I/O frame, J5A006A, contains the circuits required to interface the 1B Processor with various input/output terminals in the *4ESS* switch.

4.10 The input/output frame is a single-bay frame, 7 feet high, 2 feet 2 inches wide, and 1 foot 6 inches deep. The I/O frame is equipped according to the number of input/output terminals used. An I/O frame in a fixed floor plan arrangement must be equipped with two input/output units and two power control units. Each input/output unit has a selector and from one to eight controllers. Thus, a fully equipped I/O frame provides 16 input/output channels.

Input/Output Processor Frame (J5A006C)

4.11 The IOP frame, J5A006C, contains the circuits required to provide a programmable interface between the 1B Processor and the various input/output terminals in the *4ESS* switch.

4.12 The IOP frame is a single-bay frame, 7 feet high, 2 feet 2 inches wide, and 1 foot 6 inches deep. This frame is equipped according to the number of input/output terminals used. An IOP frame in a 1B Processor fixed floor plan arrangement must be equipped with two IOP logic units and two IOP power units. Each IOP logic unit can be equipped with two microprocessor communities. Each microprocessor community can be equipped to communicate with up to eight line unit peripherals as required. Thus, a fully equipped IOP frame provides 32 input/output channels, double the capacity of the input/output frame.

Input/Output Processor Frame (J5A006D)

4.13 The IOP frame, J5A006D, contains the circuits required to interface the 1B Processor with the various input/output terminals in the *4ESS* switch. This includes input/output interfaces between the *4ESS* switch and other systems which are via data sets.

4.14 The IOP frame is a single-bay frame, 7 feet high, 2 feet 2 inches wide, and 1 foot 6 inches deep. The frame is equipped according to the number and characteristics of the input/output channels required by the *4ESS* switch. An IOP frame in a 1B Processor fixed floor plan arrangement must be equipped with two input/output bus units, two input/output processor logic units, and one filter unit. Each IOP logic unit consists of a direct memory access controller and one microprocessor community. A second microprocessor community or a peripheral unit controller may be added to each input/output processor. Each microprocessor community and each peripheral controller community can accommodate up to eight input/output channels. Thus, a fully equipped IOP frame provides 32 input/output channels.

MCC Video Display Terminal

4.15 The MCC video display terminal is a computer terminal that provides control and display functions either at the switch or at a remote site such as the Technical Control Center (TCC). The MCC terminal is a replacement for the electromechanical MCC used in the 1A Processor. The MCC terminal is similar to the maintenance terminal on the 3B20D/3B21D computer.

4.16 The MCC terminal interfaces the 1B Processor through MUP circuit pack. There are two MUPs with only one MUP active at a time. The other MUP operates in a warm spare, nonmatching mode. Each MUP has four MCC ports with each port paralleled to a companion port on the other MUP. Each port is operational as long as one MUP is active. All four ports operate independently in a full duplex 9600 baud mode. The active MUP is able to receive a different message from all four ports and to transmit four different messages to all four ports, simultaneously.

4.17 MCC control and display information is presented via pages on the MCC color monitor. Each page consists of indicators and poke commands. There are various MCC pages that are selected by entering a poke command corresponding to the page number of each page. The exception is the Emergency Action Interface page that is selected by depressing the **EA DISP** key (see paragraph 5.41 for a description of each page). Indicators on the MCC pages convey information about entities in the 1B Processor and *4ESS* switch peripheral. Each indicator is given a name and unique item number. Many indicators change color or text to indicate the occurrence of different events in the switch. These various color and text combinations indicate the unique state of the indicator. The background color of each indicator is intended to convey the status of the indicator. The foreground colors are generally constrainted by the need to make indicators readable.

4.18 Following the **CMD:** prompt, the poke commands are entered by entering the unique numeric value for each command (the term poke comes from the description of depressing a key on the electromechanical MCC used in the 1A Processor).

Utility System

4.19 The Utility System is an interactive video display system that interfaces with the 1B Processor through the MUP. It is primarily used by product development for debugging and testing. The Utility System is also used for factory system test (FST), for 1B Processor installation, and for retrofit. The Utility System can be used as a booting device, a diagnostic source, and an IOP substitute for stand-alone testing during installation.

4.20 The Utility System is a *SUN* computer workstation that connects to the MUP via an Ethernet port. The *SUN* computer workstation must be installed within 600 cable feet of the 1B Processor.

4.21 Utility System functions are either interfering or noninterfering. The following functions are considered interfering:

- Writing of memory or registers
- Altering the sequence of instructions
- Stopping and resuming program execution
- Overwrites/dumps to or from memory or 3B20D/3B21D disk
- Generic Utility Program (GULP) non-interfering
- Input and output of *4ESS* switch I/O messages
- Boot capabilities.

The following functions are considered noninterfering to the 1B Processor:

- Reading 1B Processor registers or memory
- Reading IFB client registers
- Matching of address or data
- Tracing
- Access to the Utility Systems data bases.

5. Functional Description

General

5.01 Figures 8 and 9 are block diagrams with connections between units and connections to the *4ESS* switch peripheral. Figure 8 shows connections to the DUS for 4E21 and earlier generics. Figure 9 shows no connection to the DUS due to DUS removal in 4E22 and later generics. These figures do not show 1B Processor power and power-related alarm circuits. The following are the functional contents of the 1B Processor complex:

- Duplicated CCs
- Program store community
- Call store community
- Auxiliary unit interface
- Internal and external bus networks
- Scan and signal distributor
- MCC and utility processor
- MCC video display terminal
- Fan units.

5.02 The following are functional contents of the other equipment in the 1B Processor community:

- Auxiliary unit community consisting of magnetic disk memory (attached processor system) and magnetic tape memory (data unit selector)
- Input/output interface capability.

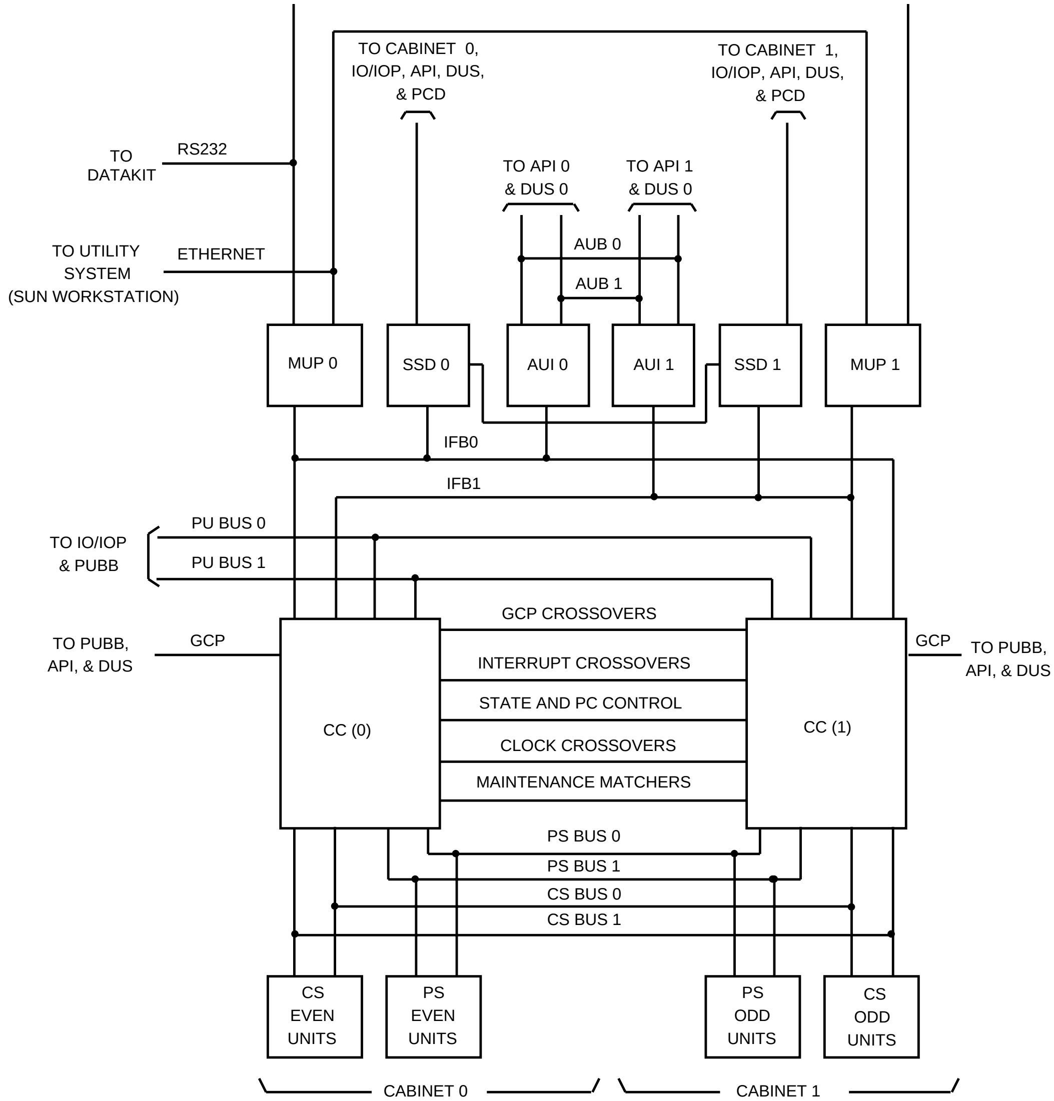


Figure 8. 1B Processor Complex Functional Block Diagram for 4E21 and Earlier Generics

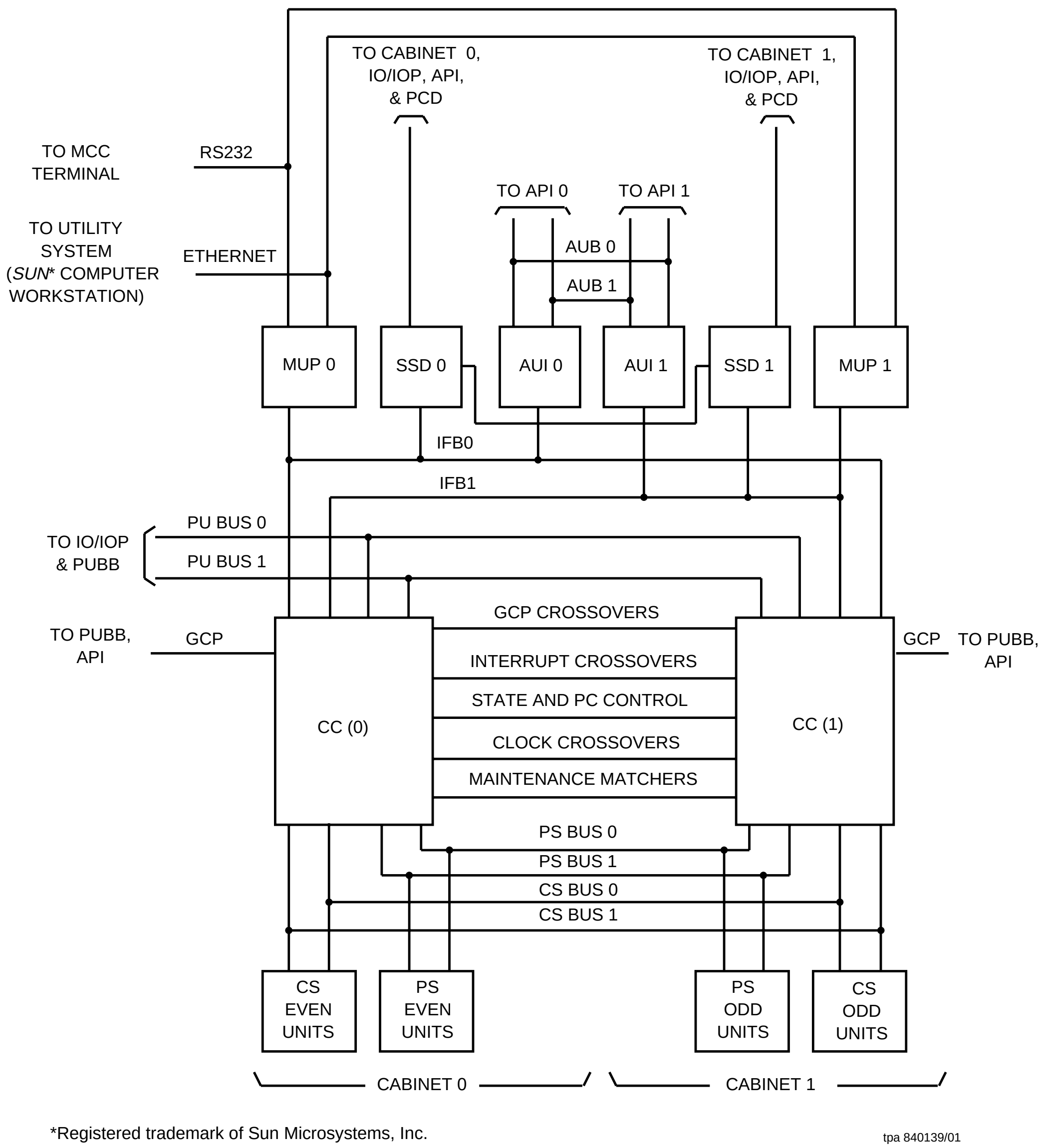


Figure 9. 1B Processor Complex Functional Block Diagram for 4E22 and Later Generics

5.03 Duplicated CC frames form the hub of the 1B Processor. The CC interfaces with the CSB, PSB, PUB, and IFB bus; and performs the processing functions for the 1B Processor. The CC executes a set of instructions written to support the associated switching system. These instructions are stored primarily in the program store community. The 1B Processor memory is arranged by MCODE reflecting the 1-MW density of the memory circuit pack. Program store contains 2 MW of memory and CS contains 5 MW of memory. The 4E22 Generic Extended Program Store feature provides an additional 1 MW -64 KW of memory while the 4E21 Generic Extended Call Store feature provides an additional 14 MW of memory. The PSs and CSs are fully duplicated. The CS community provides the CC with a scratch pad or temporary data storage area. The CSs are used for the storage of relatively short-term data related to call processing. The CSs also contain semipermanent office-dependent data (for example, translations). The boot ROM loads 80K words of PS memory during the initial phase of a pumping recovery. This is commonly referred to as PS block 0. Initialization and reconfiguration codes needed prior to the full memory pump, must reside within PS block 0.

5.04 The CC has access to magnetic disk and tape storage facilities via APS and ADS. Blocks of data can be transferred from disk or tape to CS or program store via the AUI and IFB. Normally, the magnetic disk storage is used as a backup for program stores, CSs, and disk-only programs and data. Magnetic tape is used to initialize the 1B Processor in case of disk failures, and to perform trouble-locating procedures (TLP) and library functions. The magnetic-tape-storage capability is referred to as the ADS .

NOTE:
The ADS applies to 4E21 and earlier generics. The DUSs, TUCs, and tape units connected to the 1B Processor will be effectively removed in 4E22 and later generics. Functions done with the ADS in 4E21 and earlier generics will be performed with the APS tape storage facilities in 4E22 and later generics.

5.05 The 1B Processor communicates with the peripheral switching system via the peripheral unit bus.

5.06 A number of I/O terminals are provided to exercise manual control over the system. The terminals are used for maintenance, troubleshooting, monitoring purposes, and updating office data. These I/O terminals interface with the 1B Processor via the I/O frame or IOP frame. The I/O terminals can be connected directly to the I/O or IOP frame, or indirectly via a pair of data sets. The following conditions exist when terminals are connected directly:

- Interconnection cable distance cannot exceed 200 feet when interfaced with an I/O frame.
- Interconnecting cable distance cannot exceed 500 feet when interfaced with an IOP frame.

However, if these specifications cannot be met, terminals are connected via a pair of data sets. When data sets are used, the interconnecting cable distance between the data set and the IO frame or IOP frame cannot exceed 50 feet. In general, the equipage of data sets is office-engineered.

5.07 The MCC video display terminal is a computer terminal that provides control and display functions to technicians at the switch or at remote sites. The MCC terminal is a replacement for the Master Control console used with the 1A Processor. The displays are arranged as "pages" similar to screens on the terminal used with the 3B20D/3B21D APS. The MCC terminal can display the operating condition of the 1B Processor and also permit manual control of certain system functions. The MUP provides the control for the MCC terminal.

5.08 Figure 8 shows the communication buses between the CCs and other 1B Processor units, and between the CCs and the switching system peripheral units. These buses are duplicated to maintain a high level of processor reliability. Under normal operating conditions, one bus of a duplicate pair is designated as the active bus and the other is designated as the standby. These buses are assigned to the active and standby CCs, respectively. Whenever possible, both buses are used to communicate with duplicate 1B Processor units or *4ESS* switch. In the event of a bus failure, a processor unit failure, or a peripheral unit failure, the CCs—under control of system software—make appropriate CC and bus configuration changes to maintain an operating system.

5.09 Each of the buses shown in Figure 8 consists of control signal leads, a write bus, a reply bus, and an address bus. Write, reply, and address buses, with the exception of the auxiliary unit bus, are each parallel-connected to all units in any one community. The write buses carry data from the CCs to the units in the community. The reply buses carry data from the various units back to the CCs. The address bus forwards address data from the CCs to the units in a community. Part of this address data consists of an enable code field. The enable code (MCODE) identifies the unit being accessed by the CC. When the unit accessed is a memory unit, other address data identifies the memory location to be read or written. Address data also specifies the type of operation to be performed and designates the mode in which the unit will operate. Units connected to the auxiliary unit bus can also transmit address data to the CC. This capability is required when data is transferred between disk or tape, and program store or call store. The address data transmitted identifies the store and memory location where the data is to be read or written.

5.10 A bus offered on the 1B Processor and not available on the 1A Processor is the IFB. The IFB provides an I/O bus with features such as block and device-to-device transfers. The MUP, SSD, and AUI are presently the only clients connected to the IFB. The IFB has spare frame slots to allow the addition of 8 duplex or 16 simplex clients (adjunct processors, memory devices, etc.) in the future.

5.11 The IFB offers the following services to its clients:

- **Word DMA:** A client transfers a single word at a time between itself and PS, or CS.
- **Block DMA:** A client is granted exclusive access to either PS or CS for a series of contiguous cycles. One word can be transferred each cycle.
- **Client to Client:** A client can transfer words between itself and another client on the same IFB.
- **Memory Mapped I/O (MMIO):** The 1B CC can transfer words between itself and any client. Client registers appear in the 1B address spectrum. Regular memory reference instructions are used for MMIO.
- **Interrupt/Interject:** A client can request interrupt service, or two levels of interject service from the 1B CC.

The 1B CC can only initiate MMIO with the IFB clients. It cannot initiate word DMA, block DMA, or client-to-client I/O. The IFB clients can only initiate word DMA, block DMA, or client-to-client I/O; they cannot initiate MMIO.

5.12 The AUI is an IFB client that is used to provide the connection between the 1B Processor and the existing 1A Processor AUB clients. The existing 1A Processor AUB clients are the API and the DUS. The API provides the connection to the APS and the DUS provides the connection to the TUC. The TUC provides an interface to the magnetic tape frames. The DUS, TUC, and tape frames are referred to as the ADS.

5.13 The AUI interconnection is shown in Figure 4. The 1B Processor supports two AUIs; one on each IFB. The AUI0 is located on IFB0 and AUI1 is located on IFB1. Each AUI is connected to both AUBs (0 and 1) through the driver/receiver circuit packs. The AUI supports two APIs and two DUSs. There is an API and DUS attached to each AUB. The API 0 and DUS 0 are accessible only on AUB 0; API 1 and DUS 1 are accessible only on AUB 1. Only one API or DUS is active at any given time; the mate unit functions as a warm spare.

NOTE:
The ADS (DUS,TUC, and tape drives) connected to the 1B Processor apply to 4E21 and earlier generics. The DUS, TUC, and tape drives are effectively removed in 4E22 and later generics.

5.14 The AUI supports the following subset of IFB capabilities:

(a) **MMIO:** The AUI supports MMIO on the IFB. The MMIO can read or write 32 bits of data in the AUI. However, most registers contain 24 bits to ease interfacing to the APS.

(b) **Word DMA**: The AUI supports IFB Word DMA. Each word DMA is initiated by an AUB client. The AUI cannot initiate DMA on its own except under diagnostic control. Although the AUI interface to the IFB consists of a full 32 bits, each word DMA transfers only 24 bits of data with zeros in the upper byte. This occurs because the AU data bus consists of 24 bits. The address and data widths on the AUB will not be modified. The addressing capability for DMA transactions will be 22 bits. The IFB address bits 22-29 will be specified by an 8-bit upper address register, located in the AUI; and must be initialized by the CC before any transfers can take place.

(c) **Interrupt/Interject:** The AUI supports both interrupts and interjects. The IFB errors generate interrupts. Maintenance Interjects are associated with AUB clients and errors. Operational interjects can only be requested by clients.

(d) **Generated Control Pulse (GCP):** As an IFB client, the AUI can receive a GCP signal, which isolates it from both its associated IFB and AUB. The AUI also allows the GCP of AUB clients. In response to the GCP operation, originating from the CC, the AU client sends a response which is latched onto by the AUI. The CC can then read the result via MMIO.

(e) **No Block DMA:** Due to the slow speed of the AUB (compared to the IFB), the AUI does not support IFB Block DMA.

(f) **No Client-to-Client Transfer:** Since there is no provision in the current AUB protocol to specify a client-to-client transfer, the AUI does not support transfers to other IFB clients.

5.15 The scan and signal distributor (SSD) provides the required scan and signal distributor points for all processor units. The SSD circuit pack provides 162 scan points and 158 signal distributor (SD) points. Forty-eight SSD points provide the special interfaces with units external to the 1B cabinet. The SSD is an MMIO client of the IFB. The SSD0 handles all odd 1B units, except itself; and API0, DUS0, TUC0, IOP0, and SSD1. The SSD1 handles all even 1B units, except itself; and API1, DUS1, TUC1, IOP1, and SSD0.

NOTE:
The DUS and TUC apply to 4E21 and earlier generics. They are effectively removed in 4E22 and later generics.

5.16 The MCC is controlled by the MUP. There are two MUPs in the 1B Processor. Only one MUP is active at a time; the other MUP operates in a warm spare mode. The MUP0 and MUP1 are powered independently from the CC and are interface bus clients. Communication between MUPs and MCC is via the RS232 asynchronous link. The IFB allows the CC to monitor and configure the MUP, and provides a communication path for MUP fault recovery and diagnostic control.

5.17 The 1B Processor uses a 23-bit base address configuration along with a 7-bit Transition Access Register (TAR). The base address combined with the TAR register produces a 30-bit address. The memory-bus arbiter (part of the CC) performs address decoding and memory-bus selections for the CC accessing CS, PS, boot ROM, or IFB; and for the IFB accessing CS or PS. The memory-bus arbiter takes the 30-bit address to perform the address decoding and then sends a 29-bit address to the store community. Address bit 29 is used to decode the active store community and is absorbed as part of the decoding. The memory-bus arbiter function resides on KLW22 circuit pack (bus-node address). The PSE feature needs a KLW122 circuit pack for the memory-bus arbiter. The arbiter directs CC addresses to either the CS, PS, boot ROM, or IFB. It directs addresses it receives from the IFB client to either the CS or PS. The PS and CS are allocated by MCODE reflecting the 1-MW density of their respective circuit packs. The 1B Processor complex will contain a fully duplicated 2 MW of PS and 5 MW of CS. Memory expansion features can further increase a duplicated 1MW-64KW of PS and 14MW of CS. The address spectrum for MMIO, BB, and boot ROM will be the upper address of the 1B spectrum. (See Table C.)

Bus Structure

5.18 The major 1B Processor interfaces are referred to as buses. They are identified as the PUB, PSB, CSB, and IFB. The AUB, a carry over from the 1A Processor, connects to the AUI, an IFB client. The following buses contain separate 1-way subordinate buses which are assigned to carry specific data:

(a) Buses contained in the CSBs and PSBs:

- Address bus
- Write bus
- Reply bus.

(b) Buses contained in the IFB:

- Control bus
- Address bus
- Data bus.

(c) Buses contained in the PUB:

- Enable address bus
- Write bus
- Reply bus
- Control bus.

(d) Buses contained in the AUB:

- Address bus
- Write bus
- Reply bus
- Store address bus
- Control bus.

5.19 Each of the five major buses is fully duplicated. The buses are referred to as bus 0 and bus 1. In the case of the peripheral unit bus, call store bus, and program store bus, both buses (bus 0 and bus 1) connect to all units in their community. In the case of the IFB, each IFB connects to both CCs, but only connects to the clients in its CC frame (0 or 1). Therefore, IFB clients may be made fault tolerant by placing one on each IFB. As shown in Figure 4, auxiliary unit buses 0 and 1 do not connect to all the auxiliary units.

5.20 The duplicated peripheral unit, program store, and call store buses are assigned by the CC. The CC designates one of the buses (bus 0 or bus 1) as an active bus and the other as a standby bus. During normal operating conditions, the CC also operates in this active-standby configuration. The active and standby buses are used by the active and standby CC, respectively. Because of duplicated equipment and buses, it is important to control the path that equipment uses to exchange data. Data can only be effectively transferred between two units when they are communicating on the same bus (bus 0 or bus 1). Bus select flip-flops, in each unit of the 1B Processor, independently select the bus over which that unit will communicate with the CC. These flip-flops are controlled by CC. Bus select flip-flops are used to designate which bus (bus 0 or bus 1) is active and which is standby.

5.21 In addition to the five major buses, 1B Processor internal interfaces consist of many dedicated leads. These leads connect between the CC and other units of the 1B Processor. These leads carry control and timing signals.

5.22 There are also leads from the scan and signal distributor circuit packs that connect to all processor units; these leads are within the 1B Processor cabinets and external to the 1B cabinets. These leads connect to the scan and signal distributor points of the scan and signal distributor circuit packs. The scan leads monitor the power monitor points of all processor power control circuits. The SD leads provide a means to control the OS and ACK lamps of all processor power control circuits.

Address Structure

5.23 Within the 1B Processor, more than one unit is connected to each of the five major buses. The method used to access a particular unit on a bus within the 1B Processor is referred to as coded enabling. Peripheral units in the using systems are also accessed using coded enabling.

5.24 In the 1B Processor coded enabling scheme, each unit to be accessed by the CC is assigned a coded name. For PS or CS, this coded name is called an MCODE.

5.25 The CC uses a 23-bit base address along with a 7-bit TAR register configuration when communicating with units on the call store bus and program store bus.

5.26 The 4E21 generic XS feature enables the 1B Processor to be expanded from 5 MW to 19 MW of CS on each unit bay. This feature additionally provides the Extended MMIO access from address 4000000000 to 5777777777 (octal). The XS feature uses a window-mapping address technique. There are eight contiguous 8-KW size windows, which when enabled, perform data address translation. The address for instruction fetches and data words are not translated. Each of the 8-KW windows are associated with a window-pointer register. The 8-KW windows are located within CS MCODE 1776. Translated data addresses are generated if the store access falls within one of the eight possible windows. The contents of the window-pointer register in combination with lower original 13 address bits will formulate a new designated 30-bit address. The window-pointer registers can be configured as either CS or MMIO type of access.

5.27 The PSE feature (4E22) enables the 1B Processor to be expanded from 2 MW to 3 MW -64 KW. This feature reallocated MCODE 1777 from a CS community to a PS community.

5.28 The XS and PSE features are not dependent upon each other. One or the other, or both may be selected for an memory feature upgrade.

5.29 For the Interface bus, the 1B Processor directly addresses IFB clients by using MMIO. The IFB client registers appear in the 1B Processor address spectrum. Regular memory reference instructions are used for MMIO. The IFB with DMA clients can directly address PS or CS, and transfer a single word at a time or transfer a block of words with one word transferred each cycle.

5.30 This addressing scheme also provides a means for the CC to read and write registers within each CC. These registers consist of flip-flops which indicate general status conditions such as error conditions, bus selection and parity generator outputs. Storage locations in the call stores and program stores are all accessed using the same type of instructions. The unique address specified with each particular instruction accesses the appropriate memory community or internal register.

5.31 Tables B and C show the composition of the 1B Processor address spectrum. The address range for the active CC identifies internal-control points in the active CC. The address range for the standby CC identifies the identical internal control points in the standby CC. The address range for both CCs identifies internal-control points which are accessed in both CCs simultaneously if the CCs are running in step.

Memory Write Protection

5.32 In addition to the address spectrum assignments, the 1B Processor address spectrum is divided into four protected and three nonprotected areas. The protected areas are defined by two boundary registers: lower protected area (LPA) and upper protected area (UPA). The registers apply equally to MCODEs 1770-1773 and 1774-1777 by ignoring bit 22 of the address. The extended address spectrum, which is below MCODE 1770, is unprotected. These registers are restricted to 4-KW boundaries. Memory protected by LPA and UPA may be written with the store secure (SS) order. Unprotected memory is written with any memory access operation except "SS" [for example, the store (S) order]. Executing an "SS" into unprotected memory or an "S" into protected memory results in a protected address range violation (D-level) interrupt. Maintenance orders and DMA may write independently of the LPA and UPA boundaries. The 4E21 generic XS feature allows protection area definitions to remain the same within MCODEs 1770-1777; as well as ensuring that access to XS and Extended MMIO memory will never be protected. The XS and Extended MMIO memory transactions are never checked for UPA or LPA boundaries, since these memory regions are not in MCODEs 1770-1777.

5.33 Memory may also be protected in 4-KW bocks by write-protect circuitry contained on the CS and PS circuit packs. Administration of the write-protect circuitry is done by software through special maintenance orders. Once the memory range of the store is marked as protected and the corresponding CC inhibits are allowed, any writes to that area will generate a D-level/E-level (internal store error) interrupt.

1B Processor

5.34 As shown in Figure 8, duplicated CCs are the primary functional elements of the 1B Processor. The CCs interface with all 1B Processor units via the five major bus systems. The CCs provide the 1B Processor with its processing capability which enables the processor to control a *4ESS* switch.

5.35 The CCs directly access program stores and call stores through the program store and call store buses. The CCs process instructions and data stored in these memories. These program instructions and data consist of separate 32-bit words, excluding parity. The program instructions can be one or two such words in length.

5.36 The duration of the CC operating cycle is 166.67 ns. Timing circuits within the CC provide a further division into 8 separate 20.833-ns intervals called phases (phases designated are T0 through T7). These interval designations are used to identify timing control pulses which originate at the CC and are applied to other units in the 1B Processor for synchronization. Timing pulses are identified by a naming convention which begins with a number to indicate the time of the leading signal transition, a "T" to indicate Transition, a second number which indicates the time of the trailing transition, and a 0 or 1 to indicate the polarity of the signal. An example is the main clock which is designated 0T41. This signal goes high at time T0 and goes low at time T4. The polarity indicator can show an inverted signal in the event that the trailing signal transition is needed as the zero to one transition (for example, 2T60).

5.37 The duration of the call store and program store operating cycle is 166.67 ns. Program store replies with two 32-bit words. Call store replies with one 32-bit word. Therefore, long instructions executed out of program store require a single fetch cycle of 166.67 ns. Long instructions fetched from call store require two store accesses (2 x 166.67 ns or 333.34 ns) Fetched instructions are placed in a fetch queue. This fetch queue allows the instruction fetching process to get ahead of the indexing/execution process. The fetch queue is five registers each holding a 32 bit quantity. Data received on the program store read bus (64 bits) is loaded into the fetch queue register in pairs. Instructions coming from call store are received as single words, with two fetch operations being necessary to acquire a long instruction. The CC normally executes instructions obtained from program store; however, special-use programs are stored in call store which can also be accessed and executed by the CC.

Table B. 1B Processor Memory Layout (Note)

Address Range	Attributes	Range	Type	Memory Use Description
0000000000-1777777777	—	—	—	Window CS (4E22)
2000000000-2377777777	—	—	—	Future PS
2400000000-3777777777	—	—	—	Expanded MMIO
4000000000-5777777777	—	—	—	Window MMIO (4E22)
6000000000-7737777777	—	—	—	Expanded MMIO
7740000000-7740027777	P(B&N)A14	LCS	DATA	High Usage - Protected
7740030000-7740037777	UNA14	LCS	BSS	High Usage - Unprotected
7740040000-7740047777	UNA21	LCS	BSS	UNA14 Overflow
7740050000-7742117777	UNA21	LCS	BSS*	Unprotected COMPOOL
7742120000-7747177777	UNA21	LCS	BSS*	ODA Engineered
7747200000-7747377777	PNA21	LCS	TEXT	Library Area (CS KCODE 35)
7747400000-7747777777	PBA21	LCS	DATA	PBAC/PBAL (CS KCODEs 36 & 37)
7750000000-7753777777	PBA22	PS	TEXT	PS Text
7754000000-7754237777 7754000000 7754017740 7754020000	PBA22	PS	TEXT	80K Pump Area Beginning of Vector Table Beginning of Utility Execute Table Bonded Interrupt Handlers
7754400000-7754422677	PNA-Nonzero PNA-Zero	PS	Data	Fault Recovery Data
7754422700-7754507777	Core-Page	PS	Hole	Paging Areas
7754510000-7757777777	PBA22	PS	TEXT	PS Text
7760000000-7760027777	PN23	UCS	DATA	Protected UCS
7760030000-7772357777	UN23	UCS	BSS	Unprotected ODA Unprotected COMPOOL ODA Engineered
	PB23	UCS	DATA	ODA-Translation
7772360000-7773577777	PB23	UCS	TEXT	PSBX (Protected, Backed Executed Text)
7773600000-7773617777	Core XS	UCS	Hole	XS-XA1WA0 Window Pointer #0
7773620000-7773637777	Core XS	UCS	Hole	XS-XA1WA1 Window Pointer #1
7773640000-7773657777	Core XS	UCS	Hole	XS-XA1WA2 Window Pointer #2
7773660000-7773677777	Core XS	UCS	Hole	XS-XA1WA3 Window Pointer #3

See notes and footnotes at end of table.

Table B. 1B Processor Memory Layout (Note) (Contd)

Address Range	Attributes	Range	Type	Memory Use Description
7773700000-7773717777	Core XS	UCS	Hole	XS-XA1WA4 Window Pointer #4
7773720000-7773737777	Core XS	UCS	Hole	XS-XA1WA5 Window Pointer #5
7773740000-7773757000	Core XS	UCS	Hole	XS-XA1WA6 Window Pointer #6
7773760000-7773777777	Core XS	UCS	Hole	XS-XA1WA7 Window Pointer #7
7774000000-7777577777	PB23	PSE	TEXT	Program Store
7777600000-7777657777	—	MMIO	INT	Individual client MMIO O'(37600000)+(O'(1777) IFB slot#)
7777660000-7777667777	—	MMIO	INT	Unused
7777670000-7777670377	—	MMIO	INT	Relocation Region for MMIO
7777670400-7777677777	—	MMIO	INT	Unused
7777700000-7777767777	—	ROM	INT	BOOT ROM
7777770000-7777775777	—	BB	INT	Unused
7777776000-7777776377	—	BB	INT	Active CC Buffer Bus
7777776400-7777776777	—	BB	INT	Standby CC Buffer Bus
7777777000-7777777377	—	BB	INT	Invalid Buffer Bus
7777777400-7777777777	—	BB	INT	Internal Buffer Bus

Note:

P = Protected
U† = Unprotected (via LPA/UPA)
B = Disk Backed
A = AUB/API Addressable
N = Non-disk backed
14 = 14-bit Addressable
21 = 21-bit Addressable
22 = 22-bit Addressable
23 = 23-bit Addressable
INT = CC Internal Reserved Addresses
PSE= Program Store Expansion

LCS = Lower Call Store
UCS = Upper Call Store
ODA = Office Data Assembler
MMIO = Memory Mapped I/O (IFB Access)
PBAC = Common ODA translators
PBAL = Programs and tables, loader populated
BSS = Uninitialized data
DATA = Initialized data
TEXT = Executable code

* These BSS areas are more valuable than the BSS area in UCS, which should be allocated first.

† This area may or may not be protected via the store-write protection.

Table C. 1B Processor MCODE Designations

MCODE (4E21 and Later)	**MCODE (4E19)**	**O'(Address Range)**	**Communities**
0-377	—	0000000000-1777777777	Window CS (4E21 and Later)
400-477	—	2000000000-2377777777	Future PS
500	—	2400000000-3777777777	Expanded MMIO
1000-1377	—	4000000000-5777777777	Window MMIO(4E21 and Later)
1400	—	6000000000-7737777777	Expanded MMIO
1770	0	7740000000-7743777777	CS
1771	1	7744000000-7747777777	CS
1772	2	7750000000-7753777777	PS
1773	3	7754000000-7757777777	Base PS PS Power Up
1774	4	7760000000-7763777777	CS
1775	5	7764000000-7767777777	CS
1776	6	7770000000-7773777777	CS
1777	7	7774000000-7777577777 7777600000-7777677777 7777700000-7777767777 7777770000-7777775777 7777776000-7777776377 7777776400-7777776777 7777777000-7777777377 7777777400-7777777777	Unconfigured CS (4E21 and earlier) or (4E22 and Later) PSE MMIO BOOT ROM Unused Active CC Standby CC Invalid Buffer Bus Internal Buffer Bus

5.38 The CCs also have access to auxiliary storage devices on the auxiliary unit bus system. The auxiliary unit bus (AUB) is connected to the AUI which is an IFB client. All AU transactions are conducted via the IFB by appropriately controlling the AUI. These storage devices consist of magnetic disk and magnetic tape memories. Magnetic disk memory is provided by the Attached Processor System. Magnetic disk memory is used primarily as a backup for program stores and some call stores. The Auxiliary Data System is used to record billing information and test results. The CC cannot directly access these auxiliary storage devices. Instead, the CC issues commands to the attached processor interface units or data unit selectors (magnetic tape). These control circuits then control the transfer of data blocks through the CC to and from program stores and call stores. The CC reads or writes to or from these data blocks in call stores or program stores.

NOTE:
The DUSs apply to 4E21 and earlier generics. The DUSs are effectively removed in 4E22 and later generics. Magnetic Tape functions are done via the APS in 4E22 and later generics.

5.39 The CC communicates with the *4ESS* switch peripheral units via the peripheral unit bus system. The 1B Processor supports coded enable instructions for communicating with peripheral units. In addition to the peripheral unit bus system, some peripheral units require additional interfaces with the CC. This interface is called GCP points. These pulse points are applied to selected peripheral units.

5.40 The CC also interfaces with various devices which permit operating and maintenance personnel to access the system and exercise manual control. This interface is commonly referred to as the craft-machine interface. The interface is normally accomplished in either of the following two methods; however, a third method is available for 1B Processor recovery.

(a) The **first** method of accomplishing a craft-machine interface is via input/output terminals which are located in the *4ESS* switch. These input/output terminals interface with the CC via the peripheral unit bus system and the input/output frame or input/output processor frame. The input/output frame contains the input/output unit selectors and input/output unit controllers required to buffer data between the input/output terminals and the CC. The input/output processor frame uses microprocessor-controlled data memories to buffer the data between the input/output terminals and the CC.

(b) The **second** of these methods is an MCC video display terminal. All control and display capabilities are provided by the 1B Processor MCC video display terminal. This terminal is a craft I/O device similar to the 3B20D/3B21D computer video display terminal. The KLW16 generates all pages except Pages 109 and 110. The KLW116 generates Pages 109 and 110 in addition to all other pages (KLW116 is used for 4E21 generic XS feature and 4E22 generic PSE feature). The KLW216 replaces the KLW116 in 4E22R2 generic. The KLW216 generates Page 111 in addition to all other pages. The pages used to provide control and display functions follow:

- Emergency Action Interface (EAI) page (the default page)
- Page 100—Page Index
- Page 106—MUP Status and Control
- Page 108—System Status
- Page 109—Program Store Status and Control Page
- Page 110—Call Store Status and Control Page
- Page 111—IFB Clients Status and Control Page
- Page 118—1B Processor Status
- Page 119—DDI Key Options
- Page 120—Data Display
- Page 1990—Dead Start.

(c) A **third** method of monitoring and controlling the 1B Processor is the Utility System. The Utility System is a control and display system that is fully integrated into the 1B Processor. The Utility System contains the following hardware: the 1B Processor MUP which contains an Ethernet port and a *SUN* computer workstation which connects to the Ethernet port. The Utility System can be used for the following:

- Laboratory development
- Factory system test
- Field installation
- 1A to 1B generic retrofit
- Field debugging.

5.41 The Utility System can perform the following functions:

- Reading and writing of 1B Processor memory or registers
- Altering the sequence of instructions
- Stopping and resuming program execution
- Hardware matchers of address or data
- Program Tracing
- Access to Utility Systems data bases
- Overwrites/dumps to or from memory or 3B20D/3B21D disk
- Software breakpoints
- Input and output of ESS I/O messages
- Boot capabilities.

The Utility System replaces the 1A Processor Laboratory Support System (LSS) and the Portable Recovery Test Set (PORTS).

5.42 Control signal and pulse point interfaces also exist between the CC and other 1B Processor community units. These interfaces are provided to control 1B Processor activities and coordinate data transfers between units.

Central Control

A. General

5.43 The duplicated CC frames are the primary functional element of the 1B Processor. The CC interfaces with all 1B Processor units and *4ESS* switch peripheral units. The CC processes instructions and data stored in program store and call store. The CC controls the *4ESS* switch by issuing commands to and receiving replies from the *4ESS* switch peripheral units.

B. Operating Configuration

5.44 Two identical CCs are provided in the 1B Processor for increased reliability. The normal system configuration has the two CCs operating in step. One CC functions as the active CC, and the other CC is assigned a standby role. In this configuration, both CCs perform matching checks on significant data and address for every instruction executed by the two CCs.

5.45 Should any of these duplex CC operations result in a mismatch, appropriate diagnostic and maintenance software routines are activated. These routines exercise the CCs to determine the cause of the mismatch. The mismatch may be caused by a CC, a 1B Processor unit, or the using system. Appropriate indications acknowledging a problem condition and, as near as possible, identifying the problem are provided via the craft-machine interface. If the active CC is determined to be the cause of the problem, the standby CC is designated active, and the defective CC is placed in an out-of-service condition. The system continues to function with one operating CC.

C. Internal 1B Processor Interfaces and Communication

Memory Community Interfaces

5.46 The duplicated CCs communicate with the program stores, call stores, and auxiliary unit communities over the following four bus systems:

- Program store bus (PSB)
- Call store bus (CSB)
- Interface bus (IFB)
- Auxiliary unit bus (AUB).

NOTE:
The AUB does not connect directly to the 1B Processor but connects to the AUI which is an IFB client.

Details of these four bus systems are discussed along with descriptions of the memory communities in the following paragraphs.

Call Store and Program Store Interfaces

5.47 Two-way data transfers occur between the CC processing registers and the call store and program store memory communities. The CC transmits address data and write data to the call stores and program stores. The CC receives reply data from these stores. Address data sent on the bus identifies the memory unit to be accessed, the mode in which the memory unit is to operate (normal, control, or maintenance), the type of operation to be performed (read or write), and the memory location to be accessed. When the memory access is a write operation, the data to be written is transmitted on the write bus. When the memory access is a read operation, the data read from memory is returned on the reply bus.

Auxiliary Unit Interfaces

5.48 The manner which CC obtains data from the auxiliary unit communities is not as straightforward as the CC-call store or CC-program store interface. The CC **cannot** directly access information stored on magnetic tape or magnetic disk. Instead, blocks of data are transferred through CC to call store or program store. When the transfer is complete, the CC accesses the data. The different accessing method is due to the large difference in operating speeds of the CC and the auxiliary units. By using this indirect method of access, the operation of the CC, with a 166.67-ns operating cycle, is not restricted by the slower mechanical speed of magnetic tapes or disks. These data transfers take place through the CC but under control of an auxiliary unit sequencer. The CC continues with other Processing operations while the data transfers take place. In addition to address, write, and reply data, the auxiliary unit bus also transfers store address data. During data transfers, store address data identifies the call store or program store location where data is to be either read or written.

Operating Modes

5.49 The memory units can be accessed in a normal mode or control mode. In normal mode memory accesses, data is read from or written into specific memory array locations. In control mode memory accesses, data is read from or written into control locations within the store. Control write operations enable the CC to change the configuration of the store or auxiliary units. Control read operations enable the CC to read the status of various store flip-flops and registers to obtain memory status information. The 1B Processor units also have a maintenance mode in addition to the normal mode and control mode.

Control Signals and Pulse Points

5.50 In addition to the four bus systems previously described, the CC also communicates with the various memory communities using various control signal interfaces. These control signals are required for bus management and for controlling data transfers to and from the auxiliary unit communities. The control signals applied to call store and program store consist entirely of pulse points and timing signals. The control signals applied to auxiliary units consist of a mixture of pulse points, bus management, and data transfer control signals.

5.51 The CC also communicates with 1B Processor units using GCP points. These pulse points consist of specific control pulses generated under software control within the CC. These control pulses or pulse points are applied to the 1B Processor units to initiate or control specific operations.

5.52 Each CC can generate up to 360 separate pulse points. The pulse points currently assigned are as follows:

57	CC
8	auxiliary units
14	program store
40	call store
105	peripheral units
32	interface bus clients.

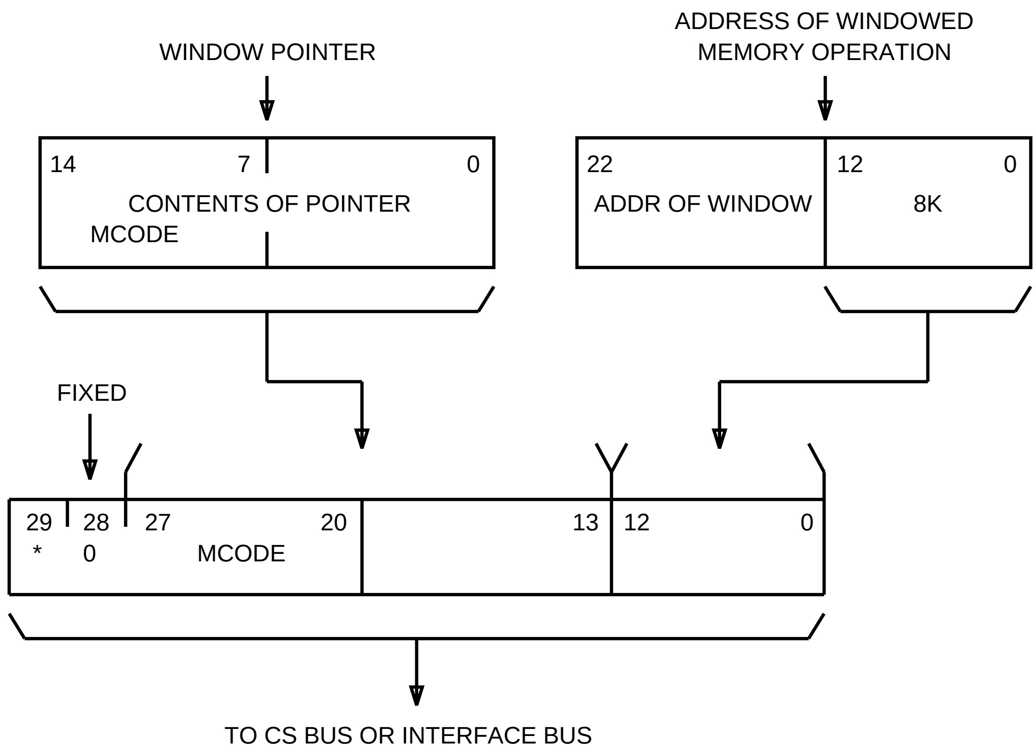
Under normal operating conditions, only the active CC generates pulse points. However, provisions are made for the standby CC to generate pulse points for diagnostic purposes.

Extended Memory Access

5.53 Figure 10 shows how access to the extended address range is accomplished using a windowed addressing scheme. There are eight fixed window address areas; each being 8 KW and 8 associated read/write window pointers that "point" to the memory in the extended range. The Extended Access Window-type register can assign the window and associated pointer to access the XS or the Extended MMIO (XM) address range. Each window can be enabled or disabled via the Extended Access Control register.

Timing

5.54 Figure 11 illustrates the general timing relationship of a data transfer between the CC and call store or program store during a read operation. Figure 12 illustrates the general timing relationship of a data transfer between the CC and call store or program store during a write operation. The timing reference shown is based on the 166.67-ns CC operating cycle. A 1B Processor cycle is defined as the time between two consecutive T0 transitions.



NOTE: The least 13 bits (8K) of the window address being accessed is concatenated with the contents of the associated window pointer and the result is sent to the selected address bus (bit 28 is forced to zero to limit each extended address spectrum to 256 megawords).

* If the window type is XS, then bit 29 is set to zero and the result is sent to the CSB. If the window type is XM, then bit 29 is set to one and the result is sent to the IFB.

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Figure 10. Address Translation of Extended Access Through 8-K Window

5.55 Circuits called bus nodes provide an interface between the CCs and the CS/PS buses. Their principle function is to control the transmission of data between the CCs and the stores. Each CC contains a set of three bus node circuit packs which are bus node address, bus node data high, and bus node data low-circuit packs.

5.56 Call store and program store are accessed from the bus nodes over duplicated buses (Bus 0 and Bus 1), which are shared by both CCs. Either bus operates at the 1B Processor cycle time (that is, a read or write operation requires one 166.67-ns cycle.).

5.57 The following signals are transmitted from the bus nodes to the call store or program store:

- Address
- Address parity
- Read
- Write
- Control
- Maintenance
- Write data
- Write data parity
- Control parity
- Clock.

5.58 The following signals are transmitted from the call stores or program stores to the bus nodes:

- Reply data
- Reply data parity
- All-seems-well (ASW)
- All-seems-well failure (ASWF)
- Data parity failure (DPF).

5.59 The timing for a CC to stores read or write operation is shown in Figure 11 and 12, respectively. Both of these transactions require one CC cycle.

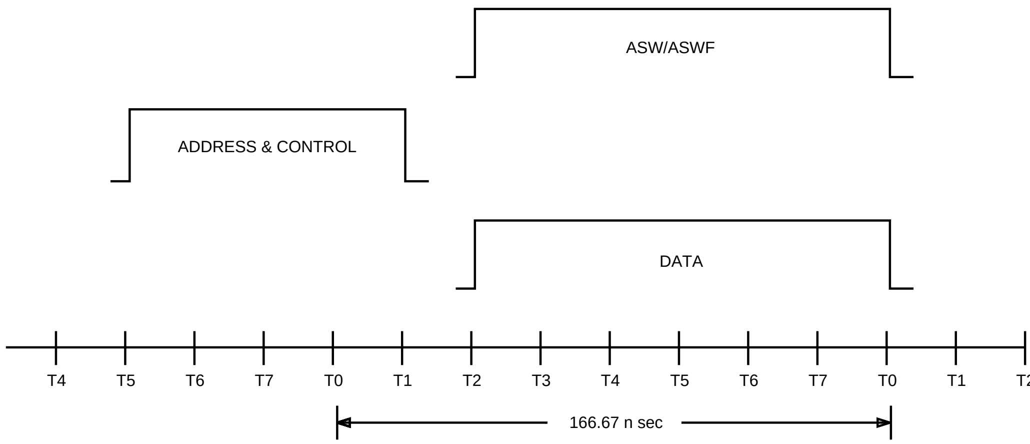


Figure 11. Central Control — Call Store/Program Store Read Data Timing

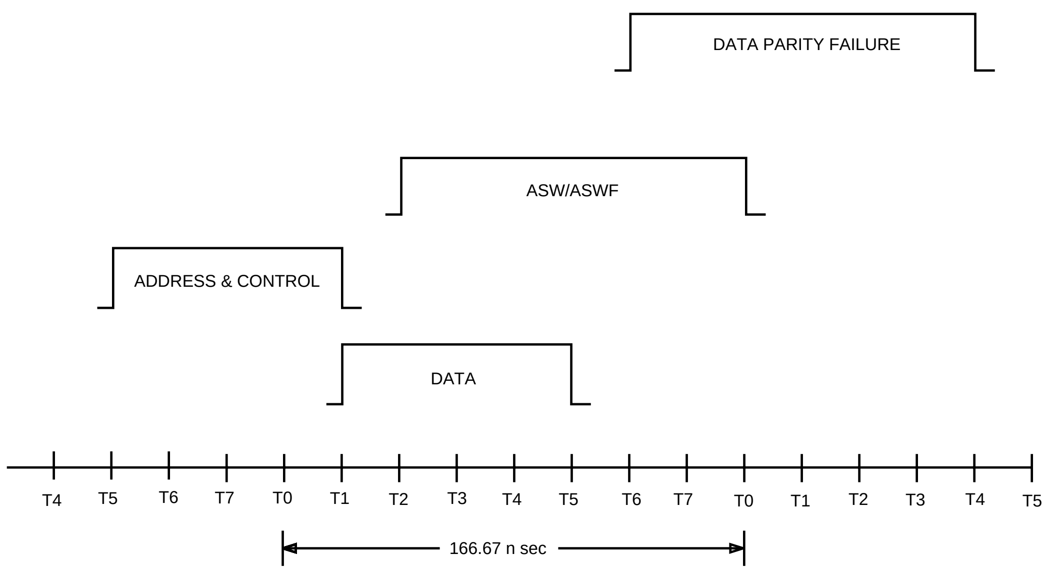


Figure 12. Central Control — Call Store/Program Store Write Data Timing

5.60 The write data includes byte parity. Parity bits are generated on the circuit pack providing the data. Faults in the backplane drivers and cabling to the bus node data circuit packs are found with parity checking. The data parity is checked by the program store and call store circuit packs. Store writes occur regardless of the outcome of the data parity check. A data parity check that fails will result with the memory circuit packs generating a data parity fail (DPF) signal for the transaction. A failed parity check of the address or control bit fields will suppress a store write, but a write data parity failure will not suppress a write. Data parity failure returns one-half clock cycle later than ASW/ASWF.

5.61 Figure 4 illustrates the relationship of the AUB and the 1B Processor. The AUI provides the connection between the AUB and the 1B CC. The 1B Processor supports two AUIs (one on each IFB).

5.62 In the 1A Processor, the AUB timing was synchronized to the 700 ns CC timing. In the 1B Processor, the CC timing and the AUB timing are asynchronous. The timing reference for the AUB is based on 700 ns which was the cycle time for the 1A Processor. Since the 1B Processor has a cycle time based on 166.67 ns, the AUI must retime the 700 ns transactions to conform to the 166.67 ns cycle time of the 1B Processor IFB.

5.63 The CCs communicate with the AUIs using memory-mapped I/O (MMIO). The AUIs have several registers, including address and data, that appear in the 1B Processor address spectrum. Regular memory instructions are used for MMIO which permits the 1B CC to read or write 32 bits of data in the AUIs.

5.64 The AUIs transfer a single word at a time between itself, and PS and CS through a process called Word DMA. Each word DMA is initiated by the AUI in response to a DMA request by an AUB client (the API or DUS). Although the AUI interface to the IFB is a full 32 bits, each DMA transfers only 24 bits of data with zeros in the upper byte. This is because the AUB is 24 bits. The addressing capability for DMA transactions will be 22 bits. The IFB address bits 22 through 29 will be specified by an eight bit upper address register located in the AUI which must be initialized by the CC before any transfers can take place.

5.65 The AUI interfaces the low performance AUB to the much faster IFB. Therefore, the maximum throughput is determined generally by the speed of the AUB. Table D describes the performance of several AUI functions assuming no contention on the IFB or memory buses.

D. Peripheral Unit Interfaces and Communication

5.66 The CC communicates with the *4ESS* switch over the PUB system (Figure 13). The CC monitors and controls the *4ESS* switch by transmitting instructions to the *4ESS* switch peripheral units. These peripheral units, in turn, perform the function of scanning, signal distribution, and network control.

Table D. AUI Operation Performance

Maximum Throughput with No Contention				
Operation	**1B cycles**	**AU cycles**	**Time nsec**	**Description**
IFB Read	3	X	500	IFB MMIO Read of an AUI Register
IFB Write	4	X	667	IFB MMIO Write of an AUI Register
AU Read	X	3	2100	AU MMIO Read to an AU Client Register
AU Write	X	3	2100	AU MMIO Write to an AU Client Register
DMA Read	X	5	3500	DMA Read from Memory
DMA Write	X	5	3500	DMA Write to Memory

Input/Output terminals located throughout the *4ESS* switch also use this bus and the Input/Output frame or Input/Output Processor frame to access the CC.

Peripheral Unit Bus (PUB)

5.67 The peripheral unit bus (PUB) links the CC to the *4ESS* switch peripheral units. The PUB is activated by the 1B Processor's peripheral unit instruction set and the GCP instruction set. The Peripheral Unit Bus in the 1B Processor *4ESS* switch is identical to the Peripheral Unit Bus in the 1A Processor *4ESS* switch. The PUB has the following characteristics:

- Is fully duplicated and referred to as PUB 0 and PUB 1.
- Peripherals which are connected to the PUB can be configured to respond to CC orders
- Bus selection circuits in each peripheral unit are under CC control.

5.68 The Peripheral Unit Bus consists of the following (see Figure 14):

(a) **Peripheral Unit Enable Address (PUEA) Bus:** The PUEA bus consists of 16 bits that are generated in the CC and are applied to the *4ESS* switch peripheral units. The main purpose of the PUEA is to transmit address information that will identify the peripheral unit that is selected for CC access. The PUEA contains 13 bits and a synchronization lead. The PUEA carries the peripheral unit name (K code) for the peripheral order. The K code consists of 12 bits with bits 7 through 11 identifying a unit type and bits 0 through 6 designating which member of that type. The 12 bits come from bits 10 through 21 of the E register on the KLW24 circuit pack. Bit 12 is the maintenance mode bit and is zero for normal peripheral orders where the MTCPU bit of the Peripheral Sequencer Control (PSC) register is not set and is one for a maintenance order where the MTCPU bit is set. The PUSYS signal is a sync pulse, sent .5 microsecond ahead of every peripheral order to all frames to clear their input register. The input/output clock start peripheral sequencer and high/low pulses (IOCH/IOCL) are generated by the 1B Processor CC (bits 15 and 16).

(b) **Peripheral Unit Write (PUW) Bus:** The PUW consists of 40 signals that are generated in the CC and are applied to the *4ESS* switch peripheral frames. In general, information on this portion of the PUB represents various instructions and/or data to be applied to the addressed *4ESS* peripheral equipment. Bits 0 through 28 of the PUW are the data or address field for the peripheral order. Bits 29 through 35 are the opcode used to specify the action to be taken on the data. Bits 0 through 35 come from the P register that resides on the KLW24 circuit pack. Bit 36 is an oscilloscope sync pulse, used for diagnostic purposes, and generated by a GCP. Bit 37 is not presently used. Bit 38 is a parity bit over odd bits of E and P registers (odd parity). Bit 39 is a parity bit over even bits of E and P register (odd parity).

(c) **Peripheral Unit Reply (PUR) Bus:** The PUR consists of 29 signals that are generated by the addressed *4ESS* switch peripheral frame and are transmitted to the CC. Information carried on this bus consists of reply data sent to the CC as a result of some control pulse (GCP) or equipment instruction. Bits 0 through 23 of the PUR contain data returned by the peripheral unit and bit 25 is the odd parity calculated over the data. Bit 24 is the ASW indicator that is returned by the peripheral unit regardless of whether any data was returned. Bits 26, 27, and 28 contain autonomous peripheral unit (APU) reply signals. The APU signals notify the CC of F-level interrupts (bit 26), interjects (bit 27), and base-level (bit 28, not presently used).

(d) **Peripheral Unit Control (PUC) Bus:** The PUC consists of eight control bits that are generated in the CC from GCP instructions and applied to the *4ESS* switch peripheral frames. These control bits initiate or control specific operations in frames according to design functions. The control signals are as follows:

- Four polling pulses applicable for digital interface frame (DIF), signal processor (SP), and Service Circuit System (SCS):
  - — Poll high priority (PHP)
  - — Poll low priority (PLP)
  - — Poll digit (PDG)
  - — Poll seizure (PSZ).
- One I/O polling pulse
- One member interrogate (MI) polling pulse
- One group interrogate (GI) polling pulse
- Clock Interrogate (CLKI)—timing signal.

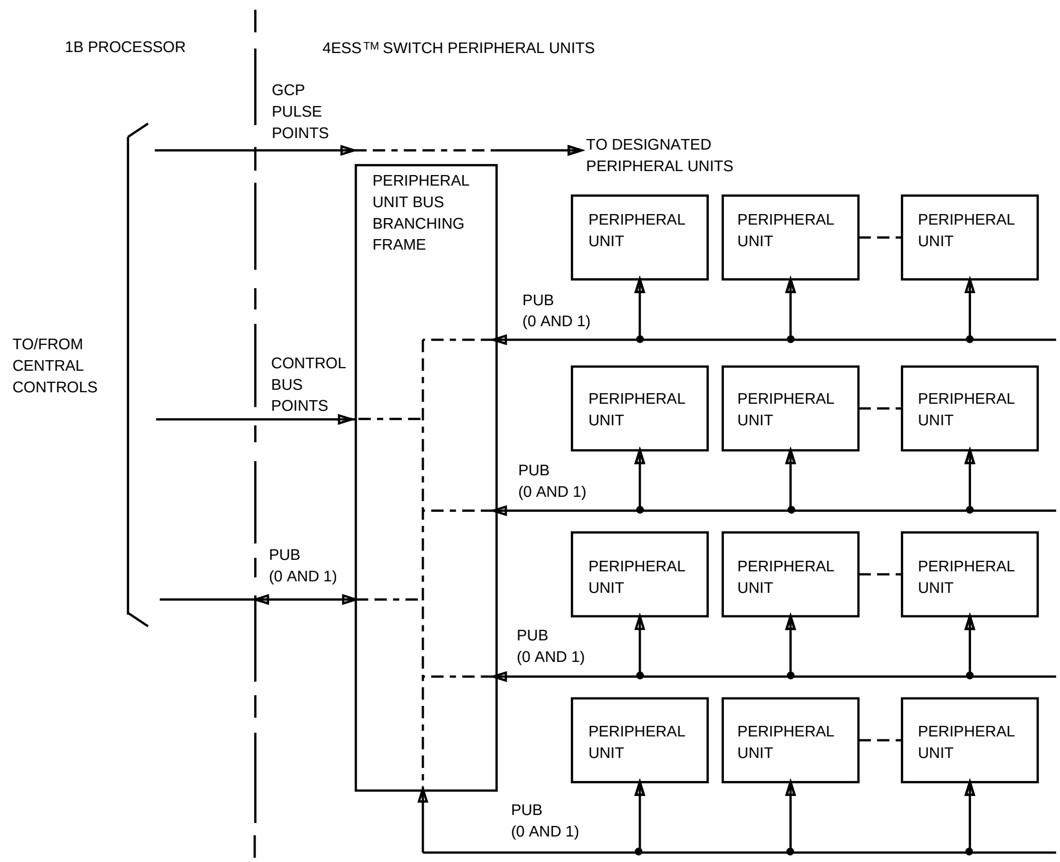


Figure 13. Peripheral Unit Bus — Simplified Block Diagram

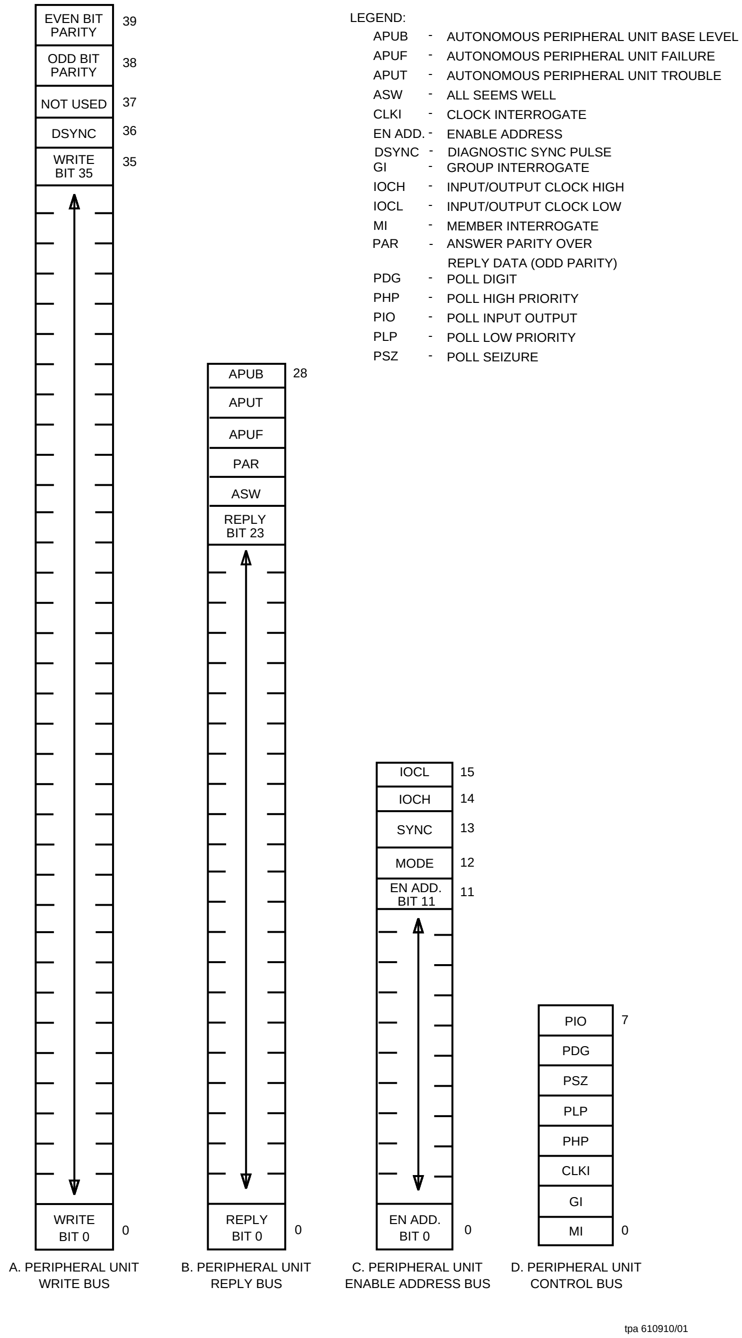


Figure 14. Peripheral Unit Bus

Peripheral Unit Enabling

5.69 The 1B Processor is designed to support coded enable instructions for communicating with *4ESS* switch peripheral units. Coded enabling requires a unique set of peripheral unit instructions and data that are applied to the addressed *4ESS* switch peripheral equipment. The 1B Processor uses a different method of accessing peripheral units to obtain status data. This 1B Processor accessing method is referred to as peripheral unit polling utilizing GCP instructions that activate peripheral unit pulse points. Coded enabling and peripheral unit polling are discussed in the following paragraphs.

Coded Enabling

5.70 The 1B Processor supports coded enable instructions (also called peripheral unit instructions) for communicating with *4ESS* switch peripheral units. These instructions are designed to send/receive data over the peripheral unit bus. The CC fetches the instruction from call store or program store. The CC places the address (K code) of the selected peripheral unit on the PUEA bus. Only the peripheral unit whose K code matches the K code on the PUEA will respond. Other peripheral units will ignore this instruction. The instruction or data that is to be applied to the addressed peripheral unit is placed on the peripheral unit write (PUW) bus by the CC. The addressed peripheral unit places its reply on the peripheral unit reply (PUR) bus which will be received by the CC.

Peripheral Unit Polling

5.71 Peripheral unit polling is used to simultaneously obtain status data from up to 24 peripheral units. This status data may represent a request for service condition, a full buffer, or any of a number of conditions to be transmitted to the CC. Peripheral unit polling occurs when the CC executes a peripheral unit GCP instruction. The address contained in the GCP instruction causes the CC to generate control pulses to the selected peripheral unit(s) either over dedicated lead(s) or over the peripheral unit control bus. The polled peripheral units respond by transmitting a single bit on an assigned bit position of the peripheral unit reply bus.

Timing

5.72 System timing requirements and transmission characteristics of the peripheral unit bus system dictate the maximum bus length between the CC and the peripheral units. In addition to the delay associated with round-trip transmission time between the peripheral units and the CC, some time is spent by the enabled peripheral unit in performing the requested operation. To make more efficient use of CC resources, provisions are made for overlapping execution of peripheral unit operations and other instructions. When a peripheral unit instruction is initiated, instruction control of the peripheral operation is passed from the CC execution sequencer to a peripheral sequencer. The peripheral sequencer monitors the progress of the instruction and notifies the CC execution sequencer when the peripheral instruction is complete. In the interim, the CC execution sequencer continues with the execution of any instructions which do not conflict with the peripheral unit instructions. However, the CC execution sequencer will not continue execution if the next instruction is dependent upon the response to the peripheral unit instruction.

5.73 Figure 15 illustrates the timing sequence for a CC coded enable access of a *4ESS* switch peripheral unit. The time reference is based on 166.67-ns CC operating cycles. A coded enable access can take from a minimum of 11 to a maximum of 136 CC operating cycles. The first two cycles of this operation are used to set up the peripheral unit address and data registers in the CC. This setup may involve an access of call store or program store. Address and control data to be written into the peripheral unit are transmitted on the peripheral unit enable address and write buses during cycles 4 through 6 of the operation. As the CC waits for a response, the execution sequencer can execute nonconflicting instructions as previously described. The peripheral unit operation is considered complete upon receipt of peripheral unit reply data and/or an all-seems-well signal at the CC. This can occur at any time in the reply data interval shown in Figure 15. Reply data and the all-seems-well signal are returned to the CC on the peripheral unit reply bus.

E. Program Execution Facilities

General Processing Registers

5.74 The CC processing registers are designated as the F-, G-, J-, K-, L-, X-, Y-, and Z- registers. Each of these registers may contain one 32-bit data word. The F-, G-, K-, X-, Y-, and Z-registers are general purpose index registers and can be specified in any instruction requiring a working register. The T-register holds the top of the return address stack. Its uses are limited to indexing instructions and to special functions in storing and retrieving information from the stack.

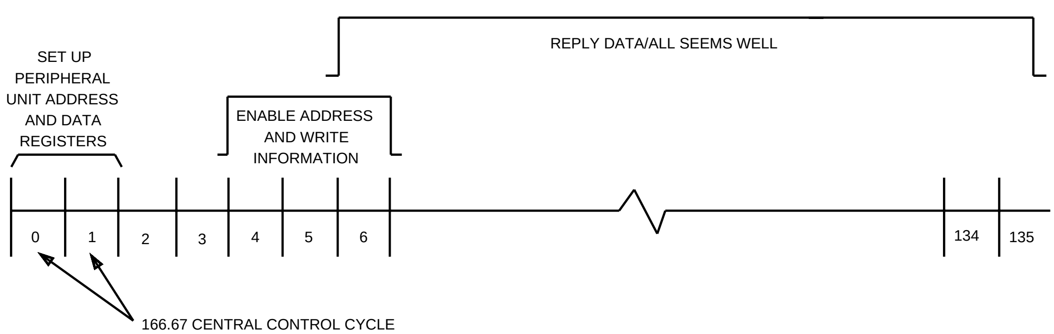


Figure 15. Peripheral Unit Access Timing

5.75 The L- and J-registers serve some unique functions. Therefore, their use is subject to certain restrictions. Use of the L-register is predefined during masking operations. Therefore, during masking operations the L-register cannot be used for any other operation. In addition, the L-register receives data from the peripheral unit reply bus. This restricts use of the L-register during operations involving the peripheral unit bus. Use of the J-register is normally reserved for single-level subroutine linkage. When a program being executed by the CC is involved in a transfer to a subroutine, the J-register is set to the address of the next sequential program address following the transfer instruction. When the subroutine execution is complete, the contents of the J-register are used to locate the next program instruction to be executed.

5.76 Each of the processing registers has a duplicate register called a shadow. A shadow register is used to store a duplicate copy of the data in the processing register. This duplication is exercised under program command only. This feature enables the previous contents of the registers to be restored at any time after a series of calculations has altered the contents.

5.77 The last item associated with general registers is a condition detector. It does the comparison needed in a conditional transfer based on the content of a general register. Its output is a sign bit (bit 23 of the selected register) and a homogeneity bit (if the register is entirely 1 or entirely 0; zero otherwise). These outputs are used by the index logic in determining whether the transfer will occur. The detector output is recorded in the sign/homogeneity condition flipflops.

Execution Unit

5.78 The execution unit contains circuits that perform a variety of arithmetic and logic functions. It permits several instructions to be processed simultaneously which increases throughput. The actual operations performed are specified by the program instruction being executed. Program instructions may specify various combinations of logic and arithmetic operations to be performed. In addition, program instructions may be executed conditionally, based on the status of internal CC control flip-flops. Program instructions may also involve conditional or unconditional transfers to other programs.

Pushdown Stack Interface

5.79 The stack is sixty-four 32-bit words located in call store. Stack accesses can be explicitly requested, using the PUSH or POP instructions. Stack accesses are also used for address storing and restoring during subroutine linkage. In this case, the transfer references the T-register for destination index or return address purposes. The stack address is provided by a 6-bit Stack Counter (SC) register which is expanded to 30 bits by a hardwired constant. Word usage in the stack advances from low addresses to high addresses. Thus the stack counter is automatically incremented after each use in a PUSH function. A combinational decrementer is attached to the stack counter to improve time efficiency in POP functions. The decrementer output is used for addressing in POP, making the appropriate address available immediately. After the POP access, the stack counter is automatically loaded from the decrementer.

Processing Interject

5.80 An interject is a service that the CC runs during a base-level program. Interjects are caused by hardware or software requests or requested at fixed intervals. Interjects are important but are not as urgent as an interrupt. Interjects do not cause interruption of the currently executing program. The following interject sources are provided in the 1B Processor:

- Autonomous peripheral unit (APU) interject source
- Software interject source
- Interval timer interject source
- IFB operational interject source
- IFB maintenance interject source.

5.81 The interject (INJ) source register provides separate bits for setting and clearing each source to allow the software to clear a bit risk free, without requiring a read-modified-write sequence. INJ also provides the ability to individually inhibit each interject source, as well as a bit which logically ORs all five interject sources. Interjects have relatively low priority, and will normally be handled when the software currently running has reached a logical point to start a new task. This could be hundreds of instructions after the interject is requested. A delay of more than 10 milliseconds after an interject request will result in a K-level interrupt.

F. Instruction Processing

Classes of Instructions

5.82 The 1B Processor program instructions are divided into the following main categories:

(a) General processing instructions

(b) Peripheral instructions

(c) Maintenance instructions.

Instructions may be either short instructions (one 24-bit word) or long instructions (two 24-bit words). Peripheral and maintenance instructions are always two words. Only a limited set of general processing instructions use one word.

General Processing Instructions

5.83 Most general processing instructions (including transfer instructions) use the program execution facilities. The execution time for these instructions varies depending upon the type of instruction issued, and the instruction options exercised. For example, a search instruction can take several CC operating cycles. This is a special use general processing instruction. However, most general processing instructions require one to five 166.67-ns CC operating cycles.

Peripheral Instructions

5.84 Peripheral instructions are used by the CC to control *4ESS* switch peripheral units. These instructions are also used to access input/output channels. A peripheral unit instruction can require from 11 to 136 166.67-ns CC operating cycles. The CC can execute general processing or maintenance instructions while waiting for completion of a peripheral unit instruction.

Maintenance Instructions

5.85 Maintenance instructions provide software control for testing various system functions. These instructions are also used to implement control read and control write operations on the various 1B Processor memory communities.

Instruction Fetching

5.86 The CC instruction-fetching mechanism presents program instructions to the CC execution facilities in an orderly manner.

5.87 Instruction addresses are generated in a CC program address register. Instruction addresses are not translated through the window mechanism offered by the 4E21 generic XS feature. Instructions cannot be fetched through the window pointers. Instruction addressses are redirected to the PSE memory as offered by the 4E22 generic PSE feature.

5.88 Instructions from call store are fetched one word at a time, while instructions from program store are fetched two words at a time. Therefore, the instruction address register must have the capability of being incremented in steps of one or two addresses. Instructions are stored in program store in a mixed format to efficiently use all available storage locations. This means that the contents of two adjacent program store data locations, which are fetched by CC, may contain two short instructions, one long instruction, one short instruction and the first half of a long instruction, two halves of a long instruction, or the second half of a long instruction and a short instruction. An example follows:

PS address n and n+1 (short — short)

PS address n+2 and n+3 (long 1 — long 2)

PS address n+4 and n+5 (short — long 1)

PS address n+6 and n+7 (long 2 — long 1)

PS address n+8 and n+9 (long 2 — short).

The CC instruction fetching queue consists of the fetch logic and five data registers. The instruction fetch queue allows the instruction fetching process to get ahead of the indexing/execution process. This queue detects the various formats and appropriately assembles the instructions for presentation to the instruction execution facility.

Instruction Decoding and Execution

5.89 The instruction decoding and execution sequence is illustrated in Figure 16. This illustration shows the sequence of events for an instruction which accomplishes the following:

- Fetches data from a 1B Processor memory community (data in call stores configured in the extended memory area cannot be fetched)
- Adds this data to the existing contents of a general processing register (register one)
- Writes the result in a second general processing register (register two).

Decoding of the instruction begins at the start of the first CC cycle shown in Figure 16. The add instruction with a memory reference is decoded, and the memory data address is generated. After the instruction is decoded, the data currently in register one is moved to the Arithmetic Logic Unit (ALU). As this transfer takes place, the address, generated as a result of instruction decoding, is further decoded to determine whether the address is for call store, program store, or an auxiliary unit (MMIO). When this address is decoded, the appropriate memory community is accessed. The data is received from memory and applied to the ALU late in the second CC cycle. The ALU performs the required addition and inserts the result into the second register during the early portion of the third CC cycle. Also during the third CC cycle, the CC begins processing the next instruction to be executed.

5.90 This execution sequence will vary greatly if the data is to be obtained from an auxiliary unit; that is, magnetic tape or disk. In this case, an MMIO request is made via the appropriate software mechanism to transfer the required data from the auxiliary unit to call store. The CC continues operation by executing other instructions until the requested data has been transferred to call store. In the previous example, the completion of this particular instruction would be delayed by an indeterminate interval.

G. Maintenance Facilities

5.91 The 1B Processor and its *4ESS* switch must remain operational on a continuous basis regardless of failures within the 1B Processor or within the *4ESS* switch. In order to satisfy this requirement, the units in the 1B Processor and the *4ESS* switch must be able to detect errors and provide some error indication which can be recognized by control software. The 1B Processor must be able to isolate the faulty unit(s) and reconfigure itself or its *4ESS* switch in order to remain operational. In addition, the 1B Processor must be able to diagnose the faulty unit and notify maintenance personnel via the craft-machine interface so that appropriate repairs can be rapidly made in order to maintain a high degree of reliability.

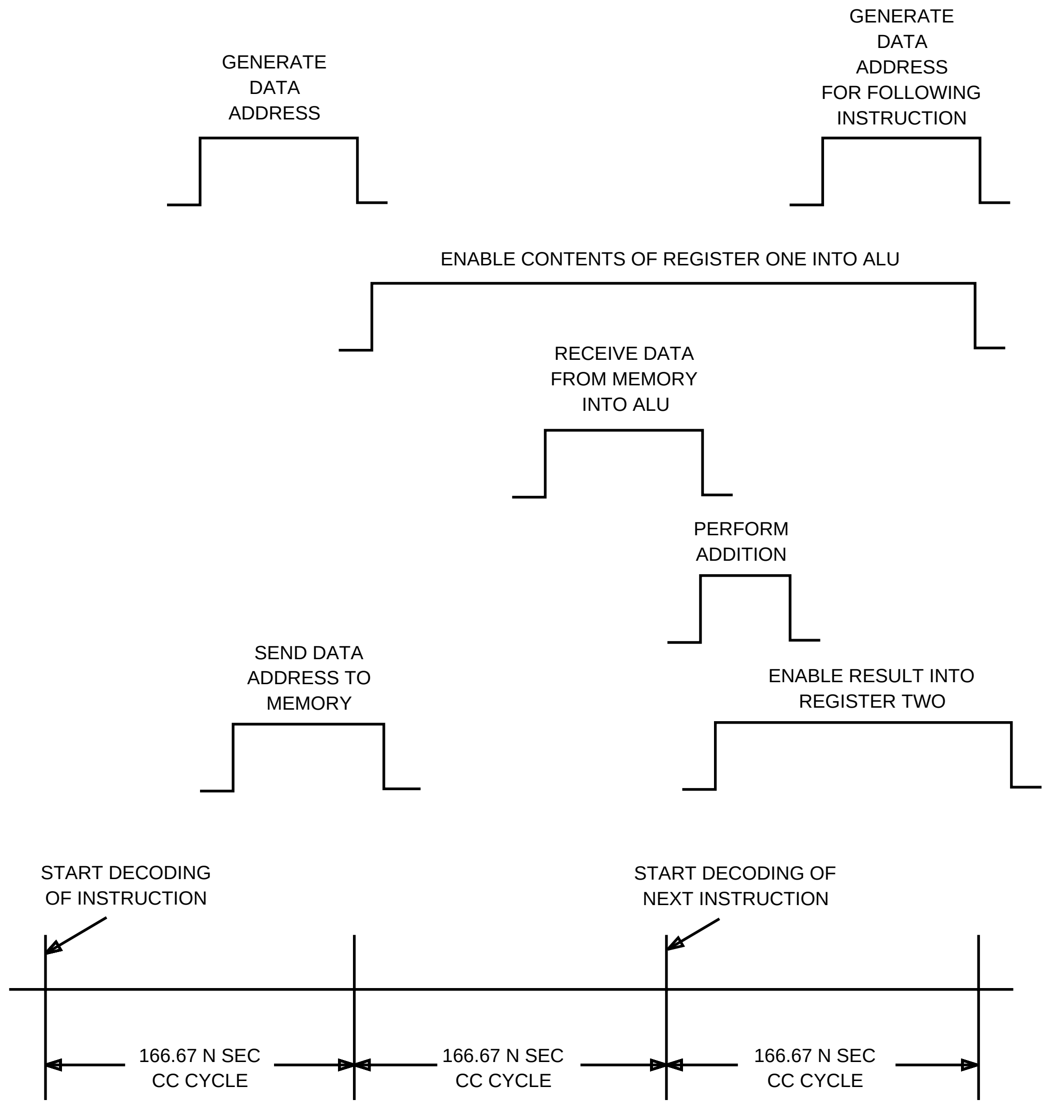


Figure 16. Example Instruction Decoding and Execution Sequence

5.92 Maintenance features have been incorporated into the CC, other 1B Processor hardware, and *4ESS* switch hardware. These features are used in conjunction with the *4ESS* switch maintenance software to closely monitor system operation. These hardware and software maintenance features include self-checking circuits, communication checks between 1B Processor units and the *4ESS* switch peripheral units, communication checks between CCs, and an interrupt capability. In addition, the CCs contain Processor Configuration which is located in Boot ROM and is used to establish a working 1B Processor if software cannot. Processor Configuration is a processor recovery concept that will automatically try possible combinations of the duplex units to bring itself up into a working configuration. This Processor Configuration reconfigures the processor should a critical equipment failure occur. An interval timer provides software with a mechanism to test hardware and perform system functions which require relatively long timing intervals. All maintenance features may be inhibited by software or manual control.

Communication Checks

5.93 Parity checks are made on all data that travels between units in the 1B Processor frame. The 1B Processor uses odd parity which is defined as the number of ones including the parity bit in an error-free transmission is always odd. The 1B Processor has the following parity encoding scheme:

- Byte parity (one parity bit per 8 bits of information)
- Parity over address and data individually.

The stores will check address parity (and data parity on writes) and report failures when detected. If address or control bit mutilation is suspected, a write operation is inhibited and the trap bit associated with the detected failure is set. If parity failures are detected on write data bits, the write will not be inhibited. This allows test access to the error detection logic in both stores and in the CCs. The data parity failure (DPF) error indicator causes immediate action to be taken in the case of unexpected data parity errors, so no system level reliability is sacrificed and diagnosability is enhanced with this arrangement.

5.94 The following checks are used to verify and maintain the integrity of the data stored in memory:

(a) **Trap Mode Error (TME):** The TME bit is set when the store has an MCODE match and invalid orders as follows are sent to the store:

- Control parity failure over the control bits (A00, A01, R, W, C, M).
- Invalid orders with the Control Instruction bit not set (C = 0) and both the read and write bits set (R/W = 1).

(b) **Trap Address Parity Fail (TAPF):** The TAPF bit is used to latch the occurrence of a store bus cycle that has bad address parity. Address bits (A28-A00) are protected by byte parity bits (P3-P0) and a failure in any address byte will cause the TAPF bit to be set. Unique address byte parity failure bits (APF3-APF0) are stored in CR11 and can be used to further define the failed bits, reducing the failure group to a single cable if there is a cabling problem.

(c) **Trap Data Parity Fail (TDPF):** The TDPF bit is used to latch the occurrence of a store bus cycle that has bad write data parity. Write data bits (D31-D00) are protected by byte parity bits (WP3-WP0), and a failure in any data byte will cause the TDPF bit to be set. Unique data byte parity failure bits (DPF3-DPF0) are stored in CR11 and can be used to further define the failed bits; thus, reducing the failure group to a single cable if there is a cabling problem.

(d) **Trap All Seems Well Failure (TASWF):** In error-free operation, every store order is answered with an ASW signal over the reply bus. If no store replies when expected, the processor can detect a failure since no ASW was received. If a store detects an error, the ASW reply is suppressed and the ASWF reply is sent instead. When a MCODE match is detected, ASWF is sent in the following cases:

- Bad address parity detected
- Bad control parity detected
- Write-protection violation occurred.

The ASWF reply is continuously sent when the store is accessed until all errors are cleared.

5.95 The peripheral unit sequencer and the auxiliary unit sequencer operate autonomously with respect to program execution. Communication checks are made between the sequencers and the units they control. These checks verify the identity of the unit being controlled. Failure of a peripheral unit check results in a maintenance interrupt. Failure of an auxiliary unit check causes the auxiliary unit sequencer to stop and causes a maintenance interject flip-flop to be set in the CC.

5.96 Auxiliary units read and write program stores and call stores through the CCs. Communication checks are performed by the stores and auxiliary units. Detection of a failure at the stores or auxiliary units results in a maintenance interject flip-flop being set in the CCs.

Communication Between Central Controls

5.97 As previously described, the normal system configuration has two CCs (CC0 and CC1) operating in step performing identical functions. Communication paths between the CCs are used for matching operations, and exchanging error and test data. The active and standby CCs exchange address, and write or reply data. Each CC matches this information against the other. Detection of a mismatch results in the generation of an interrupt. The CC which detects the error and initiates an interrupt passes a signal to the other CC to keep it in step.

5.98 The active CC can monitor, test, or exercise the other CC under program control. This is accomplished by reading and writing internal CC control registers. This communication takes place through dedicated address, data, and control leads between the two CCs. The 1B Processor address ranges used to access these registers are illustrated in Tables B and C. Through the use of these addresses, the program can read or write control registers in the active CC, the standby CC, or both CCs. Each CC contains approximately 130 of these accessible control registers.

Interrupt System

5.99 The CC has an interrupt hierarchy consisting of eight levels (A through G, and K). The H and J interrupts were used in the 1A Processor. An interrupt causes program control to transfer from the current instruction being executed to interrupt recovery and fault recovery programs. These programs determine the source of interrupt, initiate corrective or other appropriate action, and return program control to normal processing programs. The interrupt levels are assigned priorities, with "A" having the highest priority and "K" the lowest priority. A and B level interrupt programs can interrupt each other and lower priority interrupt programs. The remaining interrupt level programs can only interrupt lower level programs.

5.100 Table E identifies the sources that can initiate various interrupts. The interrupt types are divided into the following four categories:

- System configuration
- Fault detection
- Testing
- Processing.

Each interrupt type is categorized into levels. System configuration interrupts have two levels (A and B). These interrupts are initiated when 1B Processor program control malfunctions or a manual request is made. Fault detection interrupts have five levels (B, C, D, E, and F). These interrupts are initiated by memory failures, CC mismatches, protected store area violations, peripheral unit failures, and others. Testing interrupt, level G, is initiated by interval timer or CC utility matches. Processing interrupt, level K, is initiated by interject timer timeout.

Processor Configuration

5.101 Processor configuration is the high-level strategy to pull together a working 1B Processor. It will not be used if lower-level fault recovery strategies work. Processor configuration, which is located in boot ROM, is a processor recovery concept that will automatically try possible combinations of the duplex units available so that the system will always try to bring itself up into a working configuration. These configurations are shown in Table F.

5.102 For a low-level fault, the appropriate fault recognition program is selected (for C- through F-level interrupts) to isolate and correct the fault. The system restarts (unwinds) so the application software is at a safe point. If software is unable to function properly, a sanity timer will trip a B-level interrupt to start the processor configuration (PC) cycle. Processor configuration recovery (PCRV) starts with minimal changes (no change, then switch CCs); then specifies PS and PSB. After state 7, PCRV will pump memory, and completely specify the configurable units (except CS, and PUB). After state ϕ 77, the PCRV state cycles back to ϕ 40, so the upper states are continually trying to select a working processor configuration. After a working processor configuration is found, software will reset the PCRV state counter to zero within a minute of proper functioning. Repeated PC after ϕ 60 and system tries to recover with reduced sanity checks.

5.103 If Processor configuration does not pull together a working 1B Processor, the manual forces may be used to bring up the system via the MCC terminal.

Interval Timer

5.104 An interval timer in each CC provides a mechanism for conducting tests on the *4ESS* switch. The interval timer permits critical timing of system functions during relatively long intervals. The timer is initialized to a maximum value of 256 milliseconds. If expected results are not achieved within the specified interval, a G-level interrupt is initiated; the request timer interval must be reset. Normal system activities continue throughout the interval.

Table E. 1B Processor Interrupts

Request Type	Service	Level	Maskable	Unwound	Source of Interrupt
Configuration	Immediate	Hard A	No	No	Manual PC and/or Pump Request
Program Request	Deferred	Soft A	No	No Yes Yes Yes	Manual Phase Inhibit Interrupts Modify Recovery/DDI Restore I/O
Utility System	Deferred	Soft A	INH Reg	Yes	High Priority US Interrupt
Configuration	Immediate Immediate	Hard B Hard B	No MCC INH	No No	Manual PC Request† Automatic PC Request (from Timers or Program)
Fault Detection	Immediate	Hard B	INH Reg	No	GCP Failure
Fault Detection	Immediate	Hard B	INH Reg*	No	Boot ROM Parity, ASWF or BN Control Parity
Fault Detection	Immediate	Hard C	MMR Reg	No	CC Mismatch
Fault Detection	Immediate	Hard D	INH Reg INH Reg INH Reg INH Reg INH Reg	No No No No No	CS Access Failure (Bus/Parity) Stack Counter Overflow/Underflow Protected Area Write Attempt Invalid Instruction/BB Address Interface Bus Error
Fault Detection	Immediate	Hard E	INH Reg	No	PS Access Failure (Bus/Parity)
Fault Detection	Deferred	Soft F	INH Reg INH Reg	Yes Yes	Peripheral Unit Failure Autonomous PU Failure
Utility System	Deferred	Soft G	INH Reg	Yes	Low Priority US Interrupt
Diagnostic SW	Deferred	Soft G	INH Reg	Yes	Interval Timer Timeout
Diagnostic SW	None	Soft H	INH Reg‡	Yes	Spare (after 1A-to-1B conversion)
Diagnostic SW	None	Soft J	INH Reg‡	Yes	Spare (after 1A-to-1B conversion)
Fault Detection	Deferred	Soft K	INH Reg	No	Interject Timeout

* Automatically inhibits itself after first error.
† Requires MCC inhibit (poke 71).
‡ Always inhibited by Fault Recovery.

Table F. 1B Processor Configuration State Table

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
0	-	-	-	-	-	0	No	Normal
1	-	-	-	-	-	0	Yes	
2	-	-	-	-	-	0	No	No Change
3	Toggle	-	-	-	-	0	No	Switch Base PS
4	0	0	-	-	-	0	Yes	PS0/PSB0
5	1	1	-	-	-	0	No	PS1/PSB1
6	0	1	-	-	-	0	No	PS0/PSB1
7	1	0	-	-	-	0	No	PS1/PSB0
10	0	0	0	1	0	0	Yes	Pumping States
11	1	1	1	0	1	0	No	
12	0	1	0	1	0	0	No	
13	1	0	1	0	1	0	No	
14	0	0	1	1	0	0	No	
15	1	1	0	0	1	0	No	
16	0	1	1	1	0	0	No	
17	1	0	0	0	1	0	No	
20	0	0	0	0	1	0	Yes	
21	1	1	1	1	0	0	No	
22	0	1	0	0	1	0	No	
23	1	0	1	1	0	0	No	
24	0	0	1	0	1	0	No	
25	1	1	0	1	0	0	No	
26	0	1	1	0	1	0	No	
27	1	0	0	1	0	0	No	
30	0	0	0	1	1	0	No	
31	1	1	1	0	0	0	No	
32	0	1	0	1	1	0	No	
33	1	0	1	0	0	0	No	
34	0	0	1	1	1	0	No	
35	1	1	0	0	0	0	No	
36	0	1	1	1	1	0	No	
37	1	0	0	0	0	0	No	

See footnotes at end of table.

Table F. 1B Processor Configuration State Table (Contd)

State (Octal)	PS	PSB	CSB	IFB	AUB	Repeat PC	Switch CC	Comments
40	0	0	0	0	0	0	Yes*	Repeated PC†
41	1	1	1	1	1	0	No	
42	0	1	0	0	0	0	No	
43	1	0	1	1	1	0	No	
44	0	0	1	0	0	0	No	
45	1	1	0	1	1	0	No	
46	0	1	1	0	0	0	No	
47	1	0	0	1	1	0	No	
50	0	0	0	1	0	1	No	Repeated PC
51	1	1	1	0	1	1	No	
52	0	1	0	1	0	1	No	
53	1	0	1	0	1	1	No	
54	0	0	1	1	0	1	No	
55	1	1	0	0	1	1	No	
56	0	1	1	1	0	1	No	
57	1	0	0	0	1	1	No	
60	0	0	0	0	1	1	Yes	Repeated PC
61	1	1	1	1	0	1	No	
62	0	1	0	0	1	1	No	
63	1	0	1	1	0	1	No	
64	0	0	1	0	1	1	No	
65	1	1	0	1	0	1	No	
66	0	1	1	0	1	1	No	
67	1	0	0	1	0	1	No	
70	0	0	0	1	1	1	No	Repeated PC
71	1	1	1	0	0	1	No	
72	0	1	0	1	1	1	No	
73	1	0	1	0	0	1	No	
74	0	0	1	1	1	1	No	
75	1	1	0	0	0	1	No	
76	0	1	1	1	1	1	No	
77	1	0	0	0	0	1	No	Loop to O’(40) for repeated PC

* Switch CCs if not Repeated PC

† Repeated PC starts with O’(40) when cycle returns from state O’(77).

Program Store Community

A. General

5.105 A complex series of program instructions are required to control the 1B Processor and its associated *4ESS* switch. The program stores (PSs) are provided to store these program instructions and make them available to the CC. In addition to these instructions, PSs are also used to store some semipermanent office-related data.

B. Functional Capability

5.106 The storage capacity of PS is 2 MW of static RAM. The 4E22 generic PSE program storage capacity allows an additional 1 MW -64 KW of static RAM. The PS is comprised of 4-KLW2 circuit packs (or 6-KLW2 circuit packs if 4E22 generic PSE feature is added) each containing one megaword (1,048,576 bytes) of memory. This provides 2 MWs of fully duplicated memory or 3 MW -64 KW if 4E22 generic PSE feature is present. One megaword of memory is referred to as an MCODE. Each word contains 32 bits. Any PS circuit pack can be configured to any MCODE. Only PS0 and PS1 can be specified as base (MCODE 1773) by the boot code.

5.107 The 4E22 generic PSE feature actually converts MCODE 1777 from a call store allocation to a program store allocation. The 64 KWs are lost because of the existing MMIO, boot ROM, and buffer bus allocation in MCODE 1777. Hence, the Extended Program Store is 1 MW -64 MW in size. This will alter the store community from 2 MW of program store and 6 MW -64 MW of call store to a new configuration of 3 MW -64 MW of program store and 5 MW of call store.

5.108 A 1B Processor program instruction can be one or two words in length. During PS read accesses, two words are simultaneously returned to the CC. This is done to reduce instruction waiting time. During PS write accesses, only one word is sent to the store.

C. Redundancy

5.109 The program stores are fully duplicated. All data stored in PS is a duplicate of information stored in the APS. The CC regularly performs software-controlled checks which verify the proper operation of each PS. If a malfunctioning PS is detected, it is removed from service and its duplicate mate is configured in service. Program-controlled indicators on the 1B Processor MCC terminal and printed messages on using-system input/output terminals notify operating personnel of the failure and the change in system configuration.

Program Store Bus

5.110 Figure 17 illustrates in detail the information carried on the PS address, write, and reply buses.

Address Bus

5.111 The duplicated address bus (Figure 17-A) contains 39 bits and consists of the following bit grouping:

- 29 Address Bits
  - — 20 bits (A19-A00): The KLW circuit pack internal addresses of one megaword
  - — 9 bits (A28-A20): The MCODE for a KLW circuit pack.
- 2 Mode Bits
  - — C = Control
  - — M = Maintenance.
- 2 Operation Bits
  - — R = Read
  - — W = Write.
- 5 Parity Bits
  - — 4 bits (AP3-AP0): Address byte parity
  - — 1 control parity bit over A00, A01, R, W, C, M.
- 1 Timing Signal.

Write Bus

5.112 When data is written into a PS, the data is transmitted from the CC on the PS write bus (Figure 17-B). The write bus consists of 32 data bits and four data byte parity bits. The four data byte parity bits are also transmitted with the write data. Parity is checked at the store as the data is received. If parity failures are detected, the write will not be inhibited and PS will generate a data parity failure (DPF).

Reply Bus

5.113 The PS reply bus (Figure 17-C) carries read data from the PSs back to the CC. The PS reply bus is configured to simultaneously carry two 32-bit words plus 8 data byte parity bits (4 data byte parity bits for each word). In addition to this reply data, the reply bus is capable of returning all-seems-well, all-seems-well failure, and data parity failure. These bits indicate the combined results of parity and several other internal PS checks performed during the access. The two halves are called left word (A0 equal 0) and right word (A0 equal 1).

D. Read and Write Access

5.114 Read or write access is selected by the read or write operation bits on the address bus. Program store read and write accesses differ in the following manner. During PS write operations, one data word is entered into memory. During read operations, two words are simultaneously read from memory; bit 0 is ignored.

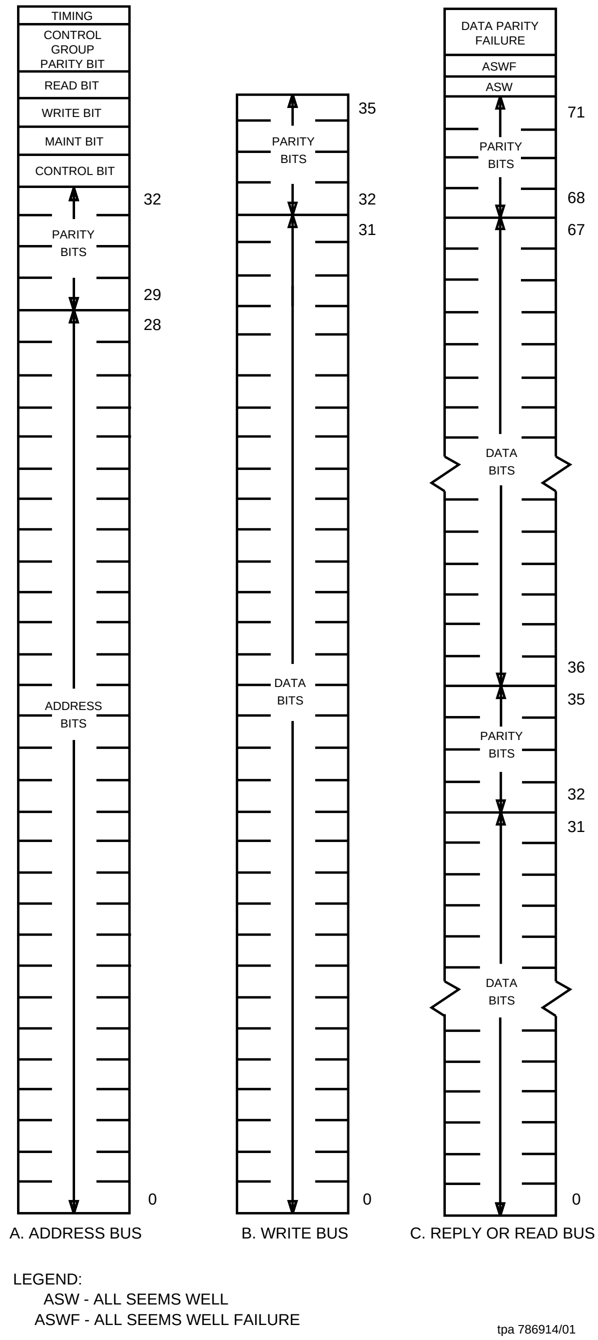


Figure 17. Program Store Bus Data Format

E. Operating Modes

5.115 The following three modes of operation are provided for communication between the 1B Processor and the stores:

- **Normal Mode:** Normal mode operation allows the 1B Processor to read or write memory in all stores within a selected community (PS or CS) whose MCODE matches address bits 20 through 28 and whose MTCE bit is reset.
- **Maintenance Mode:** Maintenance orders will be recognized by all stores within a selected community whose MCODE matches address bits 20 through 28 and whose MTCE bit is set. This allows operation of stores in all possible MCODEs assignments without impact on the operation of the duplicated normal mode memory. Maintenance mode orders can be used to read and write memory, status, or control.
- **Control Mode:** Control mode allows the 1B Processor to interrogate and alter control and maintenance registers within a store without disturbing the contents of the store's memory array.

F. Operation

5.116 In order for a PS to be accessed by the CC, each PS must be assigned an MCODE and 2-way communication must be established between the PS and CC. This is accomplished by conditioning the store MCODE register and bus select flip-flops. The store MCODE register is set to the MCODE assigned to the store. The bus select flip-flops are designated RO, S0, and S1. The RO flip-flop determines whether the PS will receive data on address and write bus 0 (RO reset) or on address and write bus 1 (RO set). The status of the S0 and S1 flip-flops determines which bus, if any, that the store will reply over. If S0 (S1) is set, the store will reply over the reply bus 0 (1). This allows sending over either bus, both buses, or neither bus.

5.117 Whenever a PS is powered-up, the following occurs:

- Initialize MCODE to ϕ 773
- Clear RO, S0, and S1 (receive on bus 0, send on neither bus)
- Clear Update bit (UPD)
- Set CRI and MTCE (inhibit all store replies, isolate store from normal access)
- Clear TME, TAPF, TDPF, and TWPVLT (clear store errors sources)
- Set WPINH (disable write protection).

Call Store Community

A. General

5.118 The 1B Processor call stores (CSs) are provided to store the frequently changed data related to call processing and ODA and programs associated with PS fault recovery.

B. Functional Capability

5.119 Functionally, call stores are similar to the program stores. The major difference is that call stores return one data word instead of two to the CC each time data is read from the store.

C. Redundancy

5.120 All call stores are fully duplicated. They are selected in the same manner as the program stores. If the operation of a CS becomes suspect, it is removed from service and the CS duplicate is used instead. Program-controlled indicators on the 1B Processor MCC terminal and printed messages on *4ESS* switch input/output terminals notify personnel of the failure.

5.121 Call stores also contain some data (semipermanent) which, like program store, is stored in the APS. This data consists of the following:

- COMPOOL or library programs
- ODA
- PS fault recovery
- PIDENTS (data and executable).

Call stores configured in the extended address spectrum can contain ODA and transient data. They cannot contain program text.

D. Call Store Interfaces

5.122 The primary CS interface is with the CC over the CS bus.

Call Store Bus

5.123 Figure 18 illustrates the information carried on the CS address, write, and reply buses.

Address Bus

5.124 The CS address bus (Figure 18-A) is identical to the program store address bus.

Write Bus

5.125 The CS write bus (Figure 18-B) is identical to the program store write bus.

Reply Bus

5.126 The CS reply bus (Figure 18-C) carries store reply data to the CCs. Data carried on this bus is similar to data carried on the program store reply bus. The only difference is the reply data bit capacity of these buses. Since CS returns only one data word at a time, the CS reply bus carries only 39 bits as specified in the following list:

- Thirty-two data bits
- Four data byte parity bits
- All-seems-well bit
- All-seems-well-failure bit
- Data parity failure bit.

E. Read and Write Access

5.127 Read or write access is selected by the read or write operation bits on the address bus. Call store read and write accesses are similar in that only one word of data is affected during both the read and the write operation. As with program store, the data location address illustrated in Figure 18-A is used to identify the actual data location to be accessed in call store.

F. Operating Modes

5.128 The call store operating modes are the same as program store operating modes.

G. Operation

5.129 The call store operation is the same as program store operation except the MCODE is initialized to ϕ 777 when a CS is powered-up.

Auxiliary Unit Communities

A. General

5.130 The auxiliary unit (AU) communities provide the 1B Processor with bulk magnetic disk and magnetic tape data storage. The magnetic disk memory is provided by an APS. The magnetic tape memory is used in the auxiliary data system. These auxiliary memories are used by the 1B Processor for the following:

- Primary storage for programs and data (for example, diagnostic programs, trunk measurement test results) infrequently used and, therefore, not stored in call store and program store (disk storage)
- Storage of system reinitialization data (tape storage)
- Storage of large amounts of data such as accounting information generated during system operation (tape and disk storage)
- Storage of library programs for special testing and growth (tape storage).

5.131 In the 1A Processor, the auxiliary unit communities connected to the AUB which connected to the CCs. In the 1B Processor, the AUB does not connect directly to the CCs, but connects to the AUI. The AUI connects to the 1B Processor's IFB. See Figure 4 for the connection of the auxiliary unit communities to the 1B Processor.

5.132 Data is transferred between the AUs and call store or program store through the AUI. There is no direct access by the auxiliary unit to the upper call store. In order to transfer data to or from a call store or program store, an AU must have the following information:

- The type of operation, read, or write access of call store or program store
- The call store or program store starting address for the read or write access
- The auxiliary unit starting address
- The size of the block of data to be transferred.

This information may be conveyed to the AUs in several ways. The CC may pass the information to the AU via the AUI. The AU may obtain the information by read-accessing call store or program store.

B. Auxiliary Unit Bus

5.133 Auxiliary unit (AU) data and address exchanges with the CC occur on the AUB, the AUI, and the IFB. Additional control and timing signals are required to administer the transfer of information to and from the AUs.

5.134 The AUB is a fully duplicated bus. However, it differs from other major bus systems in that both sections of the bus (AUB 0 and AUB 1) do not connect to all units in the community. Instead, AUB 0 connects to API and DUS 0; while AUB 1 connects to the API and DUS 1 as illustrated in Figure 4. The AUB 0 and 1 are comprised of separate addresses, write, replies, and store address buses. Figure 19 shows the data carried on each of these buses.

Address Bus

5.135 Data applied to AUs on the AU address bus serves several functions. The five data bits designated K-code (Figure 19-A) identify the AU to be addressed. The 11 data bits designated AU control-register address identify a unique register in the AU. This register is written with the appropriate information to control any data transfers between an AU and call store or program store. In Figure 19-A, the 16 bits designated K-code and control register address are the same as binary address bits 15 through 00 shown in Tables B and C. The read and write bits specify whether data is to be read from or written into the auxiliary community. The control bit designates the operating mode of the AU.

5.136 The parity bit is transmitted to maintain odd parity over the address and K-code bits. The SYNC bit is transmitted with the address information to enable the AU to receive and process the address data.

Write Bus

5.137 All data transferred to an AU, whether destined for a control register or memory, is carried on the write bus (Figure 19-B). The data to be written consists of write bits 23 through 00. Two parity bits are also transmitted with the write data.

Reply Bus

5.138 The reply bus (Figure 19-C) carries read data from the AUs to the CCs for application to call stores, program stores, or MMIO response. During MMIO read operations, reply data is read by the CC from the AUI. Reply data consists of 24 data bits and 2 parity bits. The reply bus also carries an all-seems-well bit from the AU to the CC. This bit is sent at the end of each access when internal checks indicate the AU operated correctly.

Store Address Bus

5.139 The store address bus (Figure 19-D) carries address information from the AU to the CC for application to call stores or program stores. This address information identifies the store community and data location to be accessed by the AU. Store address data consists of 22 bits. The 22 address bits shown in Figure 19-D correspond to the 22 binary address bits shown in Tables B and C. The store address bus also carries a read bit, write bit, and parity bit. The read and write bits indicate the type of access to be performed on call store or program store. Parity is computed over the 22-bit address. The parity bit is transmitted to maintain odd parity for call store addresses and even parity for program store addresses. Parity that is transmitted or received by the AU is not compatible with the 1B Processor parity schemes. The AUI must make the conversions and checks.

C. Attached Processor System (APS)

5.140 The 1B Processor uses an APS for the disk storage of programs and data. An equipment functional block diagram of a 1B Processor equipped with the APS is provided in Figure 2.

Functional Capability

5.141 The use of the high-capacity, duplexed 3B20D/3B21D Computer System gives the 1B Processor community a disk storage capacity of up to 32-M data words.

5.142 The 3B20D/3B21D Computer Disk System also uses expandable file structures that are accessible to the 1B Processor via the 3B20D/3B21D Computer Disk File Management System. Addressing within the 3B20D/3B21D computer file structures is on a file pathname, word offset basis. The 1B Processor access is limited to 20 separate 3B20D/3B21D computer files. This area of the 3B20D/3B21D computer disk storage is referred to as the 3B__File.

Redundancy

5.143 The interconnection of the 1B Processor and the 3B20D/3B21D computer is via the attached processor interface (API) unit pair (API 0 and API 1). The API units interface the 24-bit word, parallel AUB structure of the 1B Processor with the 32-bit word, serial bus structure of the 3B20D/3B21D computer. The API does not directly interface the CC through the AUB as in the 1A Processor. In the 1B Processor, the AUB connects to an AUI which is an IFB client. Refer to Figure 4 for the connection of the APIs to the 1B Processor. The duplexed 3B20D/3B21D computer direct memory access controller connects to each API unit via a dual serial bus. Under software control, one of these API units is defined as the active unit while the other is defined as the standby unit. In the event that the active unit fails, the 1B Processor reconfigures the API units. Also, the 3B20D/3B21D computer can request a reconfiguration of API units. However, the actual reconfiguration is controlled by the 1B Processor via AUB selection and API unit interprocessor commands. In the event of a duplex failure, either both API units or 3B20D/3B21D Computer System failure, the 1B Processor can continue operation until a failure which requires a memory-pump request occurs.

5.144 The APS uses a duplexed 3B20D/3B21D Computer Disk System. The 1B Processor programs and data stored by the 3B20D/3B21D computer are stored on both halves of the duplicated 3B20D/3B21D Computer Disk System. The storage of data on the disk system is transparent to the 1B Processor.

Operation

5.145 The API units connect the direct memory access (DMA) facilities of the 3B20D/3B21D computer and 1B Processor to efficiently transfer messages and data between the two processors. Direct memory access means that an API unit can transfer data messages between memories in the 1B Processor and 3B20D/3B21D computer without requiring direct 1B Processor or 3B20D/3B21D computer control (central processing unit controls) of the actual transfer.

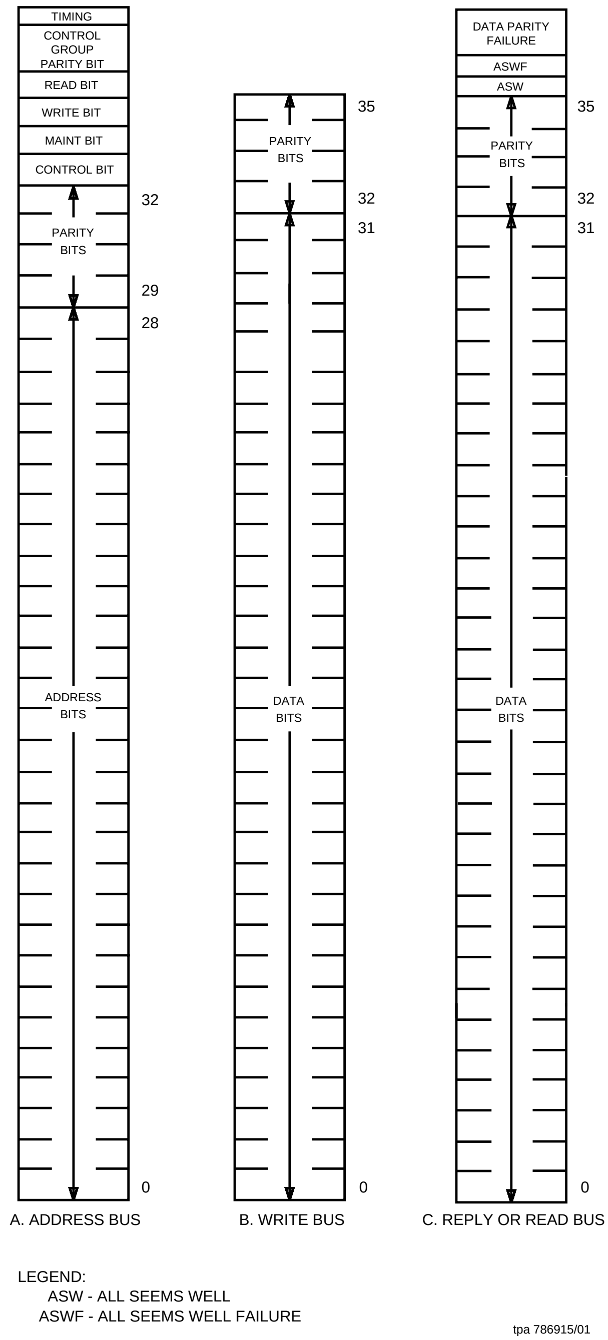


Figure 18. Call Store Bus Data Format

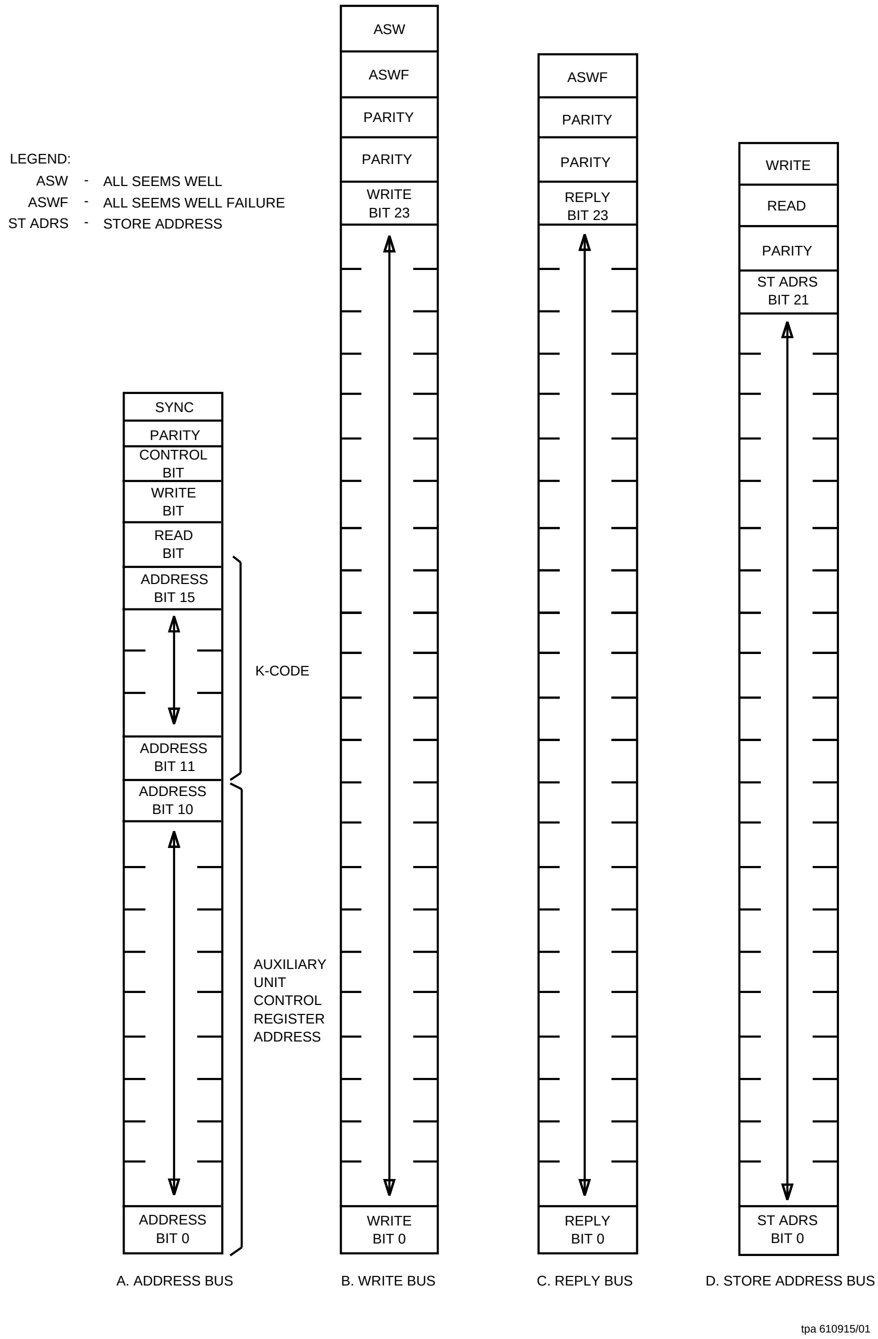


Figure 19. Auxiliary Unit Bus Data Format

Thus, direct memory access operations are more efficient in terms of processor real-time than operations requiring continuous processor control. This allows the processors to execute other programs at the same time that a direct memory access job is in process. The transfer of data over the 1B Processor AUB is under the control of the AUI. The transfer of data over the 3B20D/3B21D computer dual serial buses is under the control of the 3B20D/3B21D computer direct memory access controller.

5.146 Normal 1B Processor disk requests, read or write, are stored in a disk request area of 1B Processor main memory (call store). The active API unit autonomously polls (reads) this information via the AUB. The API unit copies the disk request information to the 3B20D/3B21D computer main memory. The 3B20D/3B21D computer control unit polls the originated disk request information looking for direct memory access work.

5.147 For 1B Processor read requests, the 3B20D/3B21D computer first performs a direct memory access transfer of the requested data from the 3B20D/3B21D Disk System to the 3B20D/3B21D computer main memory. When this operation is complete, the API is informed that the job is available. A transfer request is issued by the API to the 3B20D/3B21D direct memory access controller and the data is sent to the 1B Processor main memory via the AU reply bus. This is a two stage operation: (1) 3B20D/3B21D computer to API, and (2) API to 1B Processor.

5.148 For normal 1B Processor write requests, this process is reversed. The API initiates a read of 1B Processor memory. Data is transferred from the 1B Processor main memory to the API unit via the AUI. The API puts it into 3B20D/3B21D computer memory which is written to disk. This requires two DMA operations: (1) API to 3B20D/3B21D computer memory, and (2) 3B20D/3B21D computer memory to disk. Completed disk requests are acknowledged in a disk-request-completed area of memory in both the 1B Processor and 3B20D/3B21D computer. The originating 1B Processor client programs are notified that the disk request is completed through disk administration polling of the disk-request-completed area of memory. The 3B20D/3B21D computer releases the area of main store memory used for the disk request data based on the polling of the disk-request-completed data. Normal disk requests are processed by the active API on a first-in/first-out basis.

5.149 A CCS7 traffic stream is provided by the API using a circular buffer protocol. The high-volume signaling data stream is managed by the APS (3B20D/3B21D computer) software to provide minimal real-time overhead to the APS. The API provides the means to transport signaling messages to/from the 1B Processor call store memory directly to/from the APS (3B20D/3B21D computer) main memory where it is retrieved by signaling processors.

5.150 Two circular buffers are provided in call store with load and unload pointers indicating segments in use. One buffer provides memory for messages bound for the APS (3B20D/3B21D computer), and the other buffer provides memory for messages bound for the 1B Processor. The buffer protocol is embedded into the firmware present in the API. High-priority 1B Processor disk requests (read or write) are sent to the active API unit via the AUB. The 1B Processor auxiliary unit K-codes (AU address bits 15 through 11) used to address API units 0 and 1 are ϕ 00 and ϕ 01, respectively.

5.151 The aspect of disk file administration is handled internally to the 3B20D/3B21D computer. High-priority disk requests will temporarily suspend normal operations. Normal disk request processing is resumed when the high-priority requests have been completed.

5.152 High-priority disk request processing is the same as previously described for normal requests with the exception of how the disk request information is sent to the API unit.

Operating Modes

5.153 The API units can be operated in a control mode or a normal mode. A control bit, sent on the AU address bus, specifies the mode in which the API unit will operate for each access. In the control mode, internal API unit control registers are accessed (read or written as applicable). Control read operations enable the 1B Processor CCs to obtain API unit status information. Control write operations enable the 1B Processor CCs to change the condition of specific control points within the API unit. The normal mode is used when data is to be read from or written to the APS (3B20D/3B21D computer) for direct memory access operations.

Status Interface

5.154 API units 0 and 1 each have an API out-of-service status indicator. When the API unit maintenance flip-flop is set, the applicable API out-of-service indicator on the MCC terminal is displayed.

D. Auxiliary Data System Community

5.155 The 1B Processor can accommodate one ADS community. The ADS community consists of two DUSs, and a maximum of 16 tape unit controllers and associated magnetic tape units. The DUSs are wired logic processors that buffer data input or output from the tape unit controllers. Each tape unit controller serves as an interface between its associated tape unit and two DUSs.

NOTE:
The ADS community applies to 4E21 and earlier generics. The ADS community (DUSs, TUCs, and associated tape units) is effectively removed in 4E22 and later generics. Functions performed by the ADS community in 4E21 and earlier generics are performed via the APS tape drives in 4E22 and later.

Functional Capability

5.156 The two DUSs provided in an ADS community are each connected to one AUB (data unit selector on AUB 0 and data unit selector on AUB 1). When appropriately conditioned, a data unit selector can access call store and program store through the AUI (independent of CC processing operations). An internal ADS bus system provides a hard-wired connection between each DUS and all the tape unit controllers and associated tape units within an ADS community. However, the DUSs are configured by CC to communicate only with software-designated tape unit controllers. This means that, even though a tape unit controller is physically connected to both DUSs, the tape unit controller can only communicate with the DUS that is appropriately configured.

5.157 The DUS functions as an interface between the AUB and the tape unit controllers in the ADS community. Tape unit controllers which are actively transferring data will request both DUSs to provide access to the AUB. Only the assigned DUS will respond. The DUSs provide this access in sequence for each of the tape unit controllers assigned to them. The assigned DUS carries out the required control signal interface with the AUI to complete the data transfer. The DUSs coordinate the transfer of interject requests from the various tape unit controllers to the AUI. The DUSs also process data transfer requests originating at the CCs and coordinate these requests with appropriate tape unit controllers.

5.158 The tape unit controllers are responsible for controlling the operation of their associated tape unit. The tape unit controllers initiate appropriate control signals required to carry out a data transfer. Tape unit controller activity is initiated by commands and information originating at the CC. Once a data transfer is initiated, the tape unit controllers directly control data transfers to and from their associated tape unit. The tape unit controllers generate memory orders and addresses required for a data transfer and direct the transfer to take place through the specified data unit selector. During tape unit read operations, the tape unit controllers reformat the data read from tape to a form compatible with the 1B Processor units. During tape unit write operations, the controllers reformat write data to be compatible with the tape units.

Redundancy

5.159 Design characteristics of the ADS provide several methods of redundant operation. The method used to interface equipment with the AUB system provides redundancy against certain types of equipment failures. If any one DUS or one side of the AU bus fails, the other DUS can be configured to interface with the tape unit controller. If a tape unit controller or tape unit malfunctions, the magnetic tape can be mounted on another tape unit. The system function assigned to the failing unit can be transferred to the new unit. The 1B Processor software and the ADS can be configured to perform critical functions such as recording automatic message accounting data. One tape unit is designated as active and a separate tape unit is designated as standby. In the event of an active tape unit failure, the standby tape unit will be used to continue recording the data.

Operation

5.160 A magnetic tape storage and retrieval system requires a greater degree of manual control and management than semiconductor store or disk storage facilities. This is attributed to several factors. Before being mounted on tape units, magnetic tape reels must be physically configured for read-only or read/write operations. Steps must be taken to mount specific tapes (blank, test, diagnostic, accounting, and others) on appropriate tape units. Also, the tape units in the ADS must be configured to support one of the following three ADS functions:

- **System Reinitialization**—involves the reloading of 1B Processor memory with control programs and office data
- **Automatic Message Accounting**—involves the recording of customer billing information
- **Utility**—involves the use of ADS tape units for various activities such as the following:
  - — Inputting updated programs
  - — Using as source of special maintenance programs
  - — Recording maintenance data or test results
  - — Performing other general data handling functions.

These functions must be manually designated via an input/output terminal.

5.161 Specific DUSs are accessed using the coded enabling scheme. The K-codes assigned to DUSs are wired into each unit during manufacturing. Unlike the API, the K-codes cannot be changed by CC. Whenever CC accesses the ADS, only the DUS whose assigned K-code matches the K-code transmitted on the AU address bus will respond to the access. Auxiliary unit address bus bit 10 specifies whether the access is directed at a DUS or a tape unit controller. Auxiliary unit address bus bits 9 through 0 identify the DUS register or tape unit controller to be accessed.

5.162 As shown in Figure 4, a DUS is only connected to one side of the AUB. Therefore, bus control flip-flops are not required. However, when CC programs are written, steps are taken to ensure that ADS accesses designate the K-code of the tape unit controller connected to the bus used. Furthermore, steps are taken to ensure that tape unit controllers are configured to communicate with the tape unit controller specified in the address.

Read and Write Access

5.163 In the normal operating mode, the CCs have read and write access to two internal registers in the DUS. Normal mode read accesses are rarely implemented. Write accesses are implemented to write tape unit controller commands and address data into these registers. The DUSs forward this data to the appropriate tape unit controller. The controller then prepares to initiate a read or write access to program store or call store. The data applied to the DUS registers generally consist of the following:

- Tape unit controller commands which cause the tape units to locate a specific area on the magnetic tape
- Address data which identifies the starting address of the call store or program store area to be accessed
- Data which identifies the operation as a store read or write access
- Data which defines the size of the data block to be transferred.

While the addressed tape unit controller is processing this data and going through the relatively time-consuming process of positioning the magnetic tape, the DUS is free to service another tape unit controller.

5.164 During normal operation, DUSs scan their assigned tape unit controllers to detect any call store or program store access requests. The DUSs coordinate this scanning function with CC requests to read or write data unit selector registers. When a tape unit controller with an access request is detected, the DUSs enable the tape unit controller. From this point in time, the tape unit controller can autonomously read or write call store or program store. However, this access is coordinated through the assigned DUS and an AUI in the CC This coordination is required to eliminate conflicts in AU bus usage by the API units, DUSs, and the AUI. Data is transferred one word at a time between the tape unit controller and program store or call store. The transfer is controlled by control signals.

Memory Reinitialization

5.165 Several levels of system software reinitialization may be exercised within the 1B Processor. The type of data in program store and call store that is rewritten varies with each level of reinitialization. For most levels of reinitialization, the data to be rewritten is obtained from disk memory. These levels of reinitialization can be automatically or manually initiated. However, the most severe level of memory reinitialization, referred to as system reinitialization, must be manually initiated. During a system reinitialization, all program store, call store, and disk memory data is rewritten. Valid data is obtained from the ADS and is transferred from tape to store and then to disk storage.

5.166 The 1B Processor MCC terminal provides the manual controls required to implement system reinitialization. However, a tape unit controller and associated tape unit must be properly conditioned. This conditioning involves two items. First, a magnetic tape containing system reinitialization data must be mounted on a tape unit. Second, the associated tape unit controller must be assigned the system reinitialization function. When this is accomplished, both DUSs send a ready-for-system-reinitialization signal to the MUP which is displayed on the MCC terminal.

NOTE:
System reinitialization, using the DUS/TUC equipment is not valid for 4E22 and later generics. The DUSs and TUCs are not functional in 4E22 and later generics.

5.167 When system reinitialization is requested, CC program control is interrupted and a reinitialization signal is sent to the DUS. The DUS receiving the signal is the one associated with the AUB which is designated active (0 or 1). The DUS receiving the reinitialization signal applies it to all the tape unit controllers in the community. However, only the controller which has been assigned the system reinitialization function will respond. Once the reinitialization process is started, the DUS forwards a system-reinitialization-activate signal to the MUP. During this reinitialization operation, the ADS is conditioned to complete the data transfer even if errors are detected. If errors are detected, a system reinitialization error signal is forwarded to the MUP. This signal activates an indicator on the MCC terminal to notify operating personnel that an error condition existed.

Operating Modes

5.168 The ADS can be operated in a control mode or a normal mode. A control bit sent on the address bus specifies the mode in which the ADS will operate. In the control mode, memory accesses are not initiated. Instead, the CC is provided read and write access to most registers within the DUSs. The read access enables the CC to obtain status information concerning operation of the DUSs. The write-access capability enables the CC to change the condition of control registers and flip-flops within the DUSs.

Input/Output Frame (J5A006A)

A. General

NOTE:
The I/O frame is not in every *4ESS* switching office.

5.169 The I/O terminals provide the primary facility for interaction between the 1B Processor and operating personnel. The I/O frame provides an interface between the 1B Processor CC and these I/O terminals. The I/O terminals, located throughout the *4ESS* switch, may be various configurations of keyboard/display terminals, printers, or data sets. I/O programs executed by the CC communicate with these terminals using peripheral unit instructions applied to multiple channel I/O units in the I/O frame. These units are required to provide an interface between the relatively slow operating I/O terminals and the high-speed CC. One I/O frame, J5A006A; one IOP frame, J5A006C, or one IOP frame J5A006D, is required by the 1B Processor. Additional IOP frames or I/O frames may be provided outside of the 1B Processor fixed floor plan arrangement as part of the *4ESS* switch. The additional frames are for offices which require a greater I/O capability.

B. Interfaces

5.170 The interface between the I/O frame and the CC is the duplicated peripheral unit bus system. The I/O frame also receives GCP pulse points from the CC. These pulse points are used within the frame to control maintenance functions. External to the 1B Processor, the I/O frame interfaces with I/O terminals and data sets as required by the *4ESS* switch.

C. Functional Capability

5.171 The I/O frame consists of two identical I/O unit selectors. Each of these selectors interfaces with a maximum of eight I/O unit controllers. Each controller is assigned to a software-defined I/O channel. Thus, a totally equipped I/O frame will provide 16 I/O channels. Each channel can accommodate up to three terminals which are used for transferring the same information. Each I/O unit selector (like other 1B Processor and coded enabled using system peripheral units) is assigned its own unique K-code. The CC can access the I/O unit selectors using peripheral unit instructions transmitted on peripheral unit write bus 0 or bus 1. The appropriate K-code must be transmitted on the corresponding peripheral unit enable address bus before the I/O unit selectors will process any peripheral unit orders.

5.172 In addition to identifying the applicable input/output unit selector, the K-code field of the enable address bus also identifies the input/output unit controller to be accessed. The enabled selector decodes the peripheral unit instruction and accesses the specified controller. The controller, in turn, forwards output data to the respective input/output terminal. The output from the controller is compatible with the RS232C Electronic Industries Association (EIA) Interface Standard. The controller is capable of interfacing with input/output terminals that are within 200 cable feet of the controller. Connections to data sets must be made if the distance exceeds 200 cable feet or if the terminal is not compatible with an EIA standard interface. These data sets are provided as part of the using system (office engineered). When data sets are provided, the data sets must be equipped within 50 cable feet of the input/output frame. Input/output terminals which require a current loop interface may be located up to 4000 cable feet from the input/output frame. Data sets are **not** used in a current loop interface circuit.

5.173 At regular intervals, the CC polls the input/output unit controllers to search for service requests. When detected, the CC generates appropriate peripheral unit instructions to read this data via the peripheral unit reply bus. This data can be obtained on either bus 0, bus 1, or both.

D. Redundancy

5.174 The input/output frame consists of two input/output unit selectors and their associated input/output unit controllers. In the event of a failure of any selector or controller, sufficient hardware redundancy is provided through the remaining selector or controllers to permit data to be effectively input or output. The software assigned input/output channels are appropriately configured to provide this flexibility. Power distribution within the frame is configured so that a complete frame failure is unlikely.

Input/Output Processor Frame (J5A006C)

A. General

5.175 Input/output terminals provide the primary facility for the interaction between the 1B Processor and operating personnel. The IOP frame provides an interface between the 1B Processor CC and these I/O terminals. The I/O terminals, located throughout the *4ESS* switch, may be various configurations of keyboard/display terminals, printers, or data sets. The I/O programs executed by the CC communicate with these terminals using peripheral unit instructions applied to the multiple channel microprocessor communities of the IOP frame. These microprocessor communities are required to provide an interface between the relatively slow I/O terminals and the high speed CC. One IOP frame, J5A006C; one IOP frame, J5A006D, or one I/O frame, J5A006A, is required by the 1B Processor. Additional IOP frames (three maximum) may be added as part of the 1B Processor complex.

B. Interfaces

5.176 The IOP frame interfaces the CC via the duplicated peripheral unit bus system. The IOP frame also receives GCP pulse points from the CC. These pulse points are used within the IOP frame to control maintenance functions. External to the 1B Processor, the IOP frame interfaces with I/O terminals and data sets as required by the *4ESS* switch.

C. Functional Capability

5.177 The IOP frame consists of two identical IOPs. These processors consist of a direct memory access controller and either one or two microprocessor communities. Each microprocessor community consists of a microprocessor and from one to eight line units. Functionally, a direct memory access controller and its associated microprocessors are the equivalent of an I/O unit selector. Each of the line units is the equivalent of an I/O unit controller. Each of the two IOP equipped in the frame may support up to 16 I/O channels. Thus, a totally equipped IOP frame will provide 32 I/O channels, double the capacity of the I/O frame. In addition, the data rate of each of these channels is under software control and can be changed as required to any one of the following: 110, 300, 1200, 1800, 2400, 4800 or 9600 bps, full-duplex.

5.178 Communication between the CC and the IOP frame is via the duplicated (K-code enabled) peripheral unit bus system. The CC can access the direct memory access controllers using peripheral unit instructions transmitted on the peripheral unit write bus 0 or bus 1. The appropriate K-code must be transmitted on the peripheral unit enable address bus before a direct memory access controller will process any peripheral unit orders. The K-code also identifies the channel to be accessed.

5.179 Each direct memory access controller is a read-only-memory driven controller which executes the I/O instructions received from CC. Each direct memory access controller provides the interface between the high-speed CC and slower microprocessor communities. The microprocessors buffer and check the I/O data and provide control for each I/O channel. Communication between a direct memory access controller and a microprocessor is via fixed data locations in a random access memory (data memory) of the microprocessor. The data memory is configured by the microprocessor and is used as a channel buffer for the line units. The line units provide for the connection between the I/O terminals or data sets and the microprocessor. The output of the line unit is compatible with the RS232C Electronic Industries Association (EIA) Interface Standard. The line interface units are capable of interfacing with I/O terminals that are within 200 cable feet of the IOP frame. Connections to data sets must be made if the distance exceeds 200 cable feet or if the I/O terminal is not compatible with an EIA standard interface. These data sets are provided as part of the *4ESS* switch (office engineered). When data sets are provided, the data sets must be equipped within 50 cable feet of the input/output processor frame. I/O terminals which require a current loop interface may be located up to 1000 cable feet from the IOP frame. Data sets are **not** used in a current loop interface circuit.

5.180 At regular intervals, the CC polls the IOPs processors to search for service requests. When detected, the CC generates appropriate peripheral unit instructions to read this data via the peripheral unit reply bus. This data can be obtained on either bus 0, bus 1, or both.

D. Redundancy

5.181 The IOP frame consists of two IOPs. In the event of the failure of an IOP, sufficient redundancy is provided via channel and back-up channel assignments. Channel and back-up channels are assigned between both IOPs to permit data to be effectively input or output. Power distribution within the frame is configured so that complete frame failure is unlikely.

Input/Output Processor Frame (J5A006D)

A. General

5.182 The I/O terminals provide the primary facility for the interaction between the 1B Processor and operating personnel. The IOP frame provides an interface between the relatively slow I/O terminals and the high-speed 1B Processor CC. The I/O terminals, located throughout the *4ESS* switch, may be various configurations of keyboard/display terminals, printers, or data sets. I/O programs executed by the CC communicate with these terminals using peripheral unit instructions applied to the multiple channel microprocessor communities of the IOP frame. One IOP frame, J5A006D; one IOP frame, J5A006C, or one I/O frame, J5A006, is required by the 1B Processor. Additional IOP frames or I/O frames may be provided outside of the 1B Processor fixed floor plan arrangement as part of the *4ESS* switch. These frames are for offices which require a greater I/O capability. The J5A006D IOP frame may be equipped with an expanded I/O feature. This allows the 1B Processor to accommodate up to 32 IOP frames.

B. Interfaces

5.183 The IOP frame interfaces with the CC via the duplicated peripheral unit bus system. The IOP frame also receives GCP pulse points from the CC. The pulse points are used within the IOP frame to control maintenance functions. External to the 1B Processor, the IOP frame interfaces with I/O terminals and data sets as required by the *4ESS* switch.

C. Functional Capability

5.184 The IOP frame consists of two identical IOPs. These IOPs consist of an IOP logic unit. Also, each IOP may include either a 1B IOP growth unit or a 3B20D/3B21D IOP growth unit. The IOP logic unit consists of a direct memory access controller and one microprocessor community. The microprocessor community contains one microprocessor and up to eight line units. A line unit may be one of the following:

- A three-port line unit (EIA interface)
- A one-port current loop interface line unit
- An auto-callback line unit.

The 1B IOP growth unit provides a second microprocessor community for an IOP. The 3B20D/3B21D IOP growth unit provides two peripheral controller communities. Each community is capable of supporting up to four peripheral controllers (four single-port I/O channels). Functionally, a direct memory access controller and its associated microprocessors are the equivalent of an I/O selector. Each of the line units and peripheral controllers is the equivalent of an I/O unit controller. These units are used by the 1B Processor software programs to identify I/O channels.

5.185 The maximum capacity of an IOP frame is dependent on the operating characteristics of the IO channels equipped. When a frame is fully equipped using two 1B IOP growth units, the IOP frame can support 32, three-port I/O channels (16 channels in each IOP processor). Each microprocessor has a maximum throughput capability of 19,200 bps. This limitation is based on the maximum operating speed of the microprocessors used in the IOP logic unit and 1B IOP growth unit communities. Therefore, the summation of the operating rates of each of the I/O channels equipped for a given microprocessor community cannot exceed 19,200 bps, half-duplex (or 9,600 bps, full-duplex). If higher operating speeds are required for an I/O channel in this configuration, a corresponding decrease in the number of I/O channels supported by the given community is necessary. The equipage of a 3B20D/3B21D I/O processor growth unit differs in this regard. Each of the eight channels of a 3B20D/3B21D IOP growth unit is driven by a dedicated microprocessor (peripheral unit controller). Therefore, each equipped I/O channel of a peripheral controller community can be operated at a maximum rate of 19,200 bps, half-duplex (or 9,600 bps, full-duplex). In addition, the 3B20D/3B21D IOP growth unit may be optionally equipped to support data rates up to 56,000 bps, full-duplex. The data rate of an I/O channel is determined by translations data and the IOP equipage. An input/output channel may be operated at data rates of 110, 300, 1200, 1800, 2400, 4800, 9600, or 56,000 bps, full-duplex. Thus, within the limitations of frame equipage, the data rates of the various I/O channels are determined by software (translations).

5.186 Communication between the CC and the IOP frame is via the duplicated (K-code enabled) peripheral unit bus system. The CC can access the direct memory access controllers using peripheral unit instructions transmitted on the peripheral unit write bus 0 or bus 1. The appropriate K-code must be transmitted on the peripheral unit enable address bus before a direct memory access controller will process any peripheral order. The K-code also identifies the channel to be accessed.

5.187 Each direct memory access controller is a read-only, memory-driven controller which executes the I/O instructions received from CC. Each direct memory access controller provides the interface between the CC and microprocessor communities or microprocessor and peripheral controller communities. These communities buffer and check the I/O data and provide control for each I/O channel. Communication between a direct memory access controller and either a microprocessor community or peripheral controller community is via fixed data locations in a random access memory (data memory) within each community. The data memory is configured by a microprocessor and is used as a channel buffer. The output of these communities is compatible with the Electronic Industries Association (EIA) Interface Standards. Direct connection with I/O terminals can be made providing that the distance between the IOP frame and the I/O terminals do not exceed 200 feet. Connections to I/O terminals must be via data sets when the distance exceeds 200 cable feet. When data sets are used, the data sets must be equipped within 50 cable feet of the IOP frame. I/O terminals which require a current loop interface may be located up to 1000 cable feet from the IOP frame. Data sets are **not** used in a current loop interface circuit.

5.188 At regular intervals, the CC polls the input/output processors to search for service requests. When detected, the CC generates appropriate peripheral unit instructions to read this data via the peripheral unit reply bus. This data can be obtained on either bus 0, bus 1, or both buses.

D. Redundancy

5.189 The IOP frame consists of two IOPs. In the event of the failure of an IOP, sufficient redundancy is provided via channel and backup channel assignments. Channel and back-up channels are assigned between both IOP to permit data to be effectively input or output. Power distribution within the frame is configured so that complete frame failure is unlikely.

MCC Terminal

5.190 In addition to I/O terminals, the MCC terminal serves as a direct link between operating personnel and the 1B Processor. Displays on the MCC terminal dynamically reflect system status. Controls are provided to permit operating personnel to initiate and control certain system actions. If other elements of the 1B Processor are in a valid configuration and are operating normally, losing the MCC terminal will have no impact on system operation. Most monitoring and control activities can be implemented using I/O terminals.

5.191 The MCC terminal may be remoted to a No. 2 Switching Control Center System or equivalent Centralized Switching Maintenance Facility. This interface is provided via a port on the MUP. Certain I/O channels are also remoted via data links to the same Centralized Maintenance Facility.

6. Power

1B Processor Power Inputs

6.01 The power source for the 1B processor is -48V nominal (-42.75 to -60V dc measured at the 1B Processor power lugs). This power can be derived from one of the following two sources:

- -48V battery plant connected through a J86334B Power Distribution Frame (PDF) to the 1B Processor complex
- Bulk converters operating from a 140-volt battery plant and connecting through a J86334C Power Distribution Frame to the 1B Processor complex.

The power source must be capable of supplying 6000 watts to the 1B Processor complex.

6.02 Refer to Figure 20 for the 1B Processor Power Connections. Ten -48V Power Distribution Frame (PDF) power feeders, each supplied from a 45 amp fuse, enter the 1B cabinet and connect to a fuse and filter unit at the top of each cabinet, 5 for each processor cabinet. These are divided into groups (Branch A and Branch B), which must be completely independent for reliability. The CC 0 and KLW23 (Miscellaneous Power Board— -48V to +5V and +24V converter) in cabinet 0 are fed by Branch A of one feeder. CC 1 and KLW23 in cabinet 1 are fed by Branch B of the same feeder. The other four feeders in each cabinet (two from Branch A and two from Branch B) are used to power the CSs, PSs, Fans, and IFB clients. Each of these packs receive both A and B power and combine them through diode ORing. If either the A or B feeders should fail, the office will lose a CC, but the stores and IFB clients will continue to operate on power from the other feeder.

DC Power Distribution to API, IO/IOP, and Tape Frames

6.03 The J5A007B/C Power Conversion and Distribution Frame (PCDF) will be removed once the 1A Processor is removed. The +24V source from the PCDF to the API, IO(P), and Tape frames will be removed and another +24V source must be found for these frames. The power connections for the API, IO/IOP and Tape frames is illustrated in Figure 21.

Power and Power-Related Alarm Circuits

6.04 Power and power-related alarm circuits are monitored via SD and scan points. The SD and scan points are connected to two Scan and Signal Distributor (SSD) circuit packs in the 1B Processor complex. One SSD circuit pack serves complex cabinet 0 and one-half of the external users. The other circuit pack serves complex cabinet 1 and the other half of the external users. Some power-related alarm circuits can be tested manually by operating personnel and automatically under the control of SD points from the SSD circuit pack. The SSD frame power and power-related alarm circuits are monitored and tested by the CC. Various failures within the power and power-related alarm circuits, such as fuse and converter failures, result in a major alarm. Major alarms are sent to the office alarm system.

Protective Grounding System

6.05 Electronic circuits in both the *4ESS* switch peripheral frames and the 1B Processor frames cannot tolerate transient voltages and noise levels. To eliminate stray currents generated outside the electronic system, the frames are bonded into a ground plane that is isolated except for a single-point connection to building ground. Grounding methods are specified in Lucent Technologies Practice 802-001-195. All 1B Processor frames are incorporated into this ground plane in the same way as the peripheral frames. For this discussion, the 1B Processor will be considered within the peripheral area of the *4ESS* switch (Figure 22).

6.06 All frames are insulated from building steel and other foreign grounds.

6.07 The 1B Processor frames, peripheral frames, and their overhead cable rack sections are connected to a frame ground bus system. The lead connecting the frames is called the frame ground strap (FGS) and is connected to the frame steelwork. The bus is connected to the overhead **ground bus** of each Power Distribution Frame. The cable racks are isolated from transmission area cable racks by an insulated section that is at least 2 inches in length.

6.08 For power grounding, the discharge ground bus, called "discharge bus return equalizer," of each Power Distribution Frame is connected to its overhead ground bus. All overhead ground buses and the **main ground** bus are connected in a series ring-type configuration.

6.09 The main ground bus is a splice plate that is the center of the peripheral area "ground window." All conduits, shields, and conductors connected to foreign grounds coming into the peripheral area and connecting to locally grounded circuits must pass through this window and be connected to the main ground bus. The main ground bus is connected at a single point to the central office ground on the associated floor.

7. 1B Processor Complex—Technology, Physical Design, and Environment

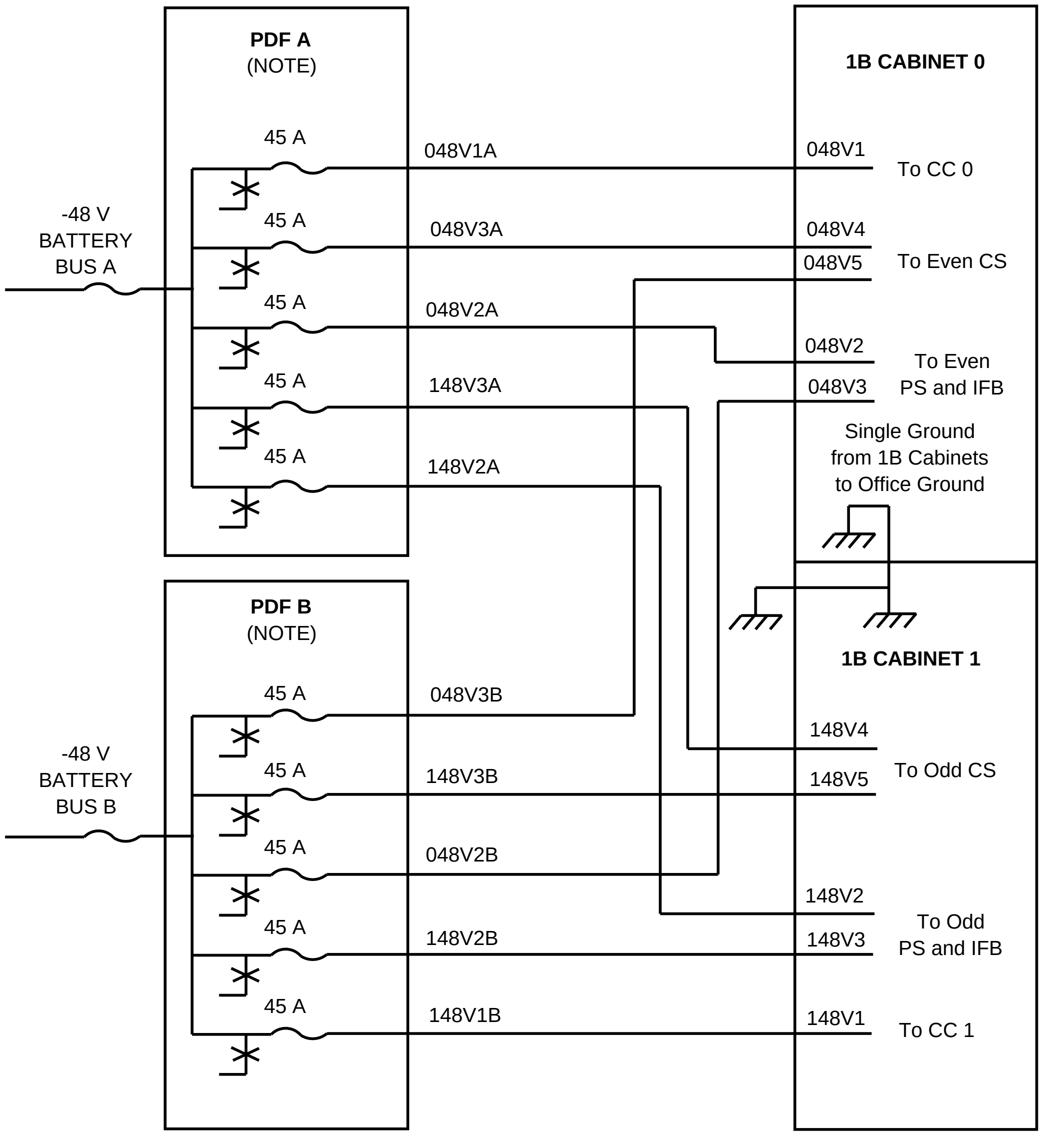
Interconnection Technology

7.01 The packaging technology used in the 1B Processor complex is *Fastech* packaging system. This internally developed technology provides a dense, high-performance, standardized interconnection technology. This approach to system packaging brings with it an immense amount of evaluation and supportive design and manufacturing environments. This allows rapid development, due to the use of existing installed bases of engineering, development, and manufacturing tools and processes.

A. Component Technology

7.02 Several factors governed the selection of devices used in the 1B. These factors include speed, frequency, noise, power, and thermal characteristics. The 1B Processor uses the following technology (the reason each is used is also stated):

- Programmable Logic Devices (PLD)—cost effective means of reducing circuit board real-estate
- Complementary Symmetry Metal Oxide Semiconductors (CMOS)—frequency and transmission-line properties
- Advance CMOS (AC)—best characteristics for minimizing noise [for example, Electromagnetic Interference (EMI) and device-generated noise such as ground-bounce, undershoot, and dynamic threshold shift]
- Emitter Coupled Logic (ECL)—speed
- Large-Scale Integration (LSI)—high-speed and high-density
- Fairchild Advance Schottky (FAST)—ground-bounce and device latch-up characteristics
- Low-Power Schottky (LS) TTL devices—low-power dissipation.



NOTE: When -48 V battery plant power source is used, the Power Distribution Frame (PDF) is J86334B.

When converter power plant power source is used, the PDF is J86334C.

Figure 20. 1B Processor Power Connections

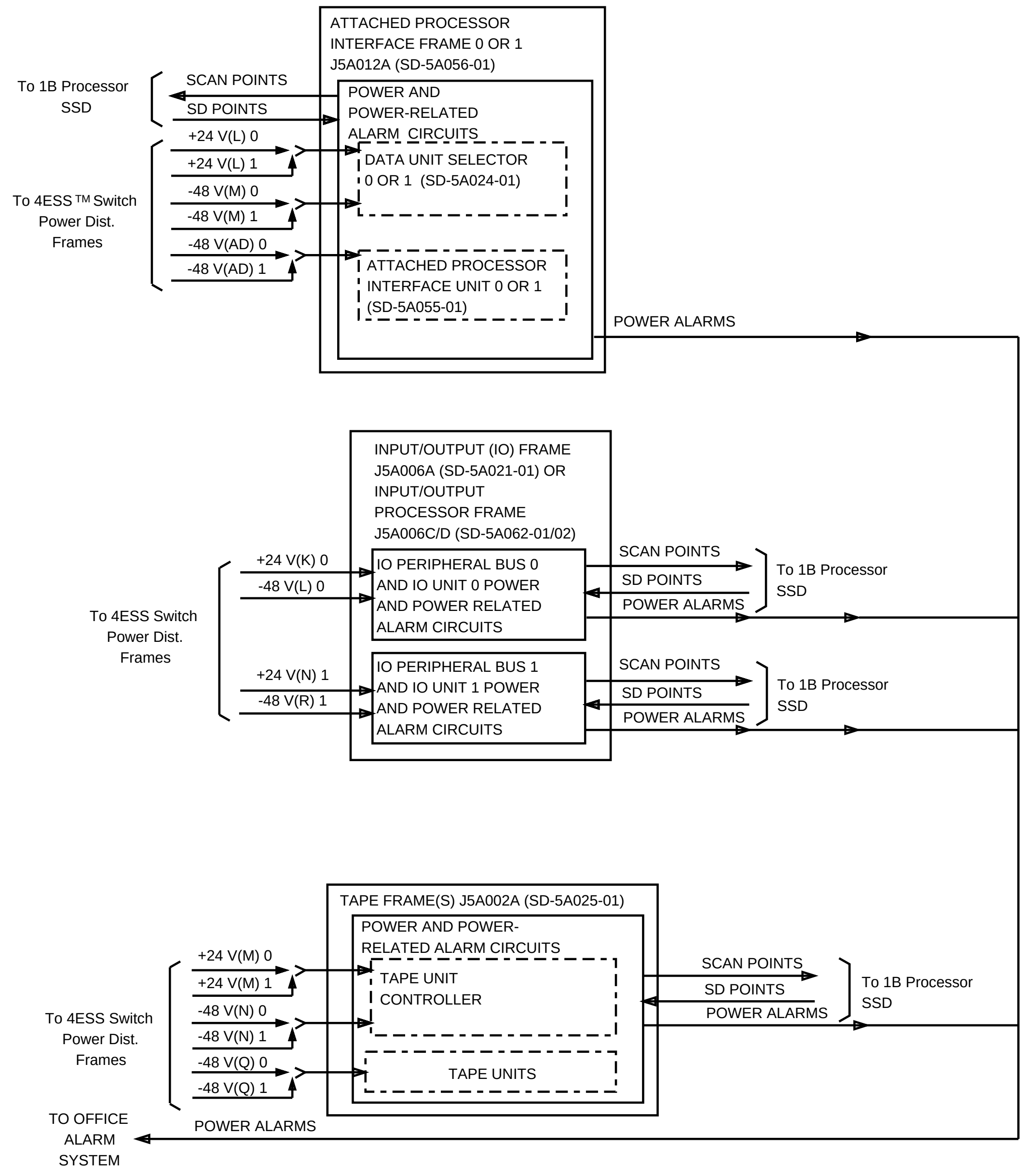
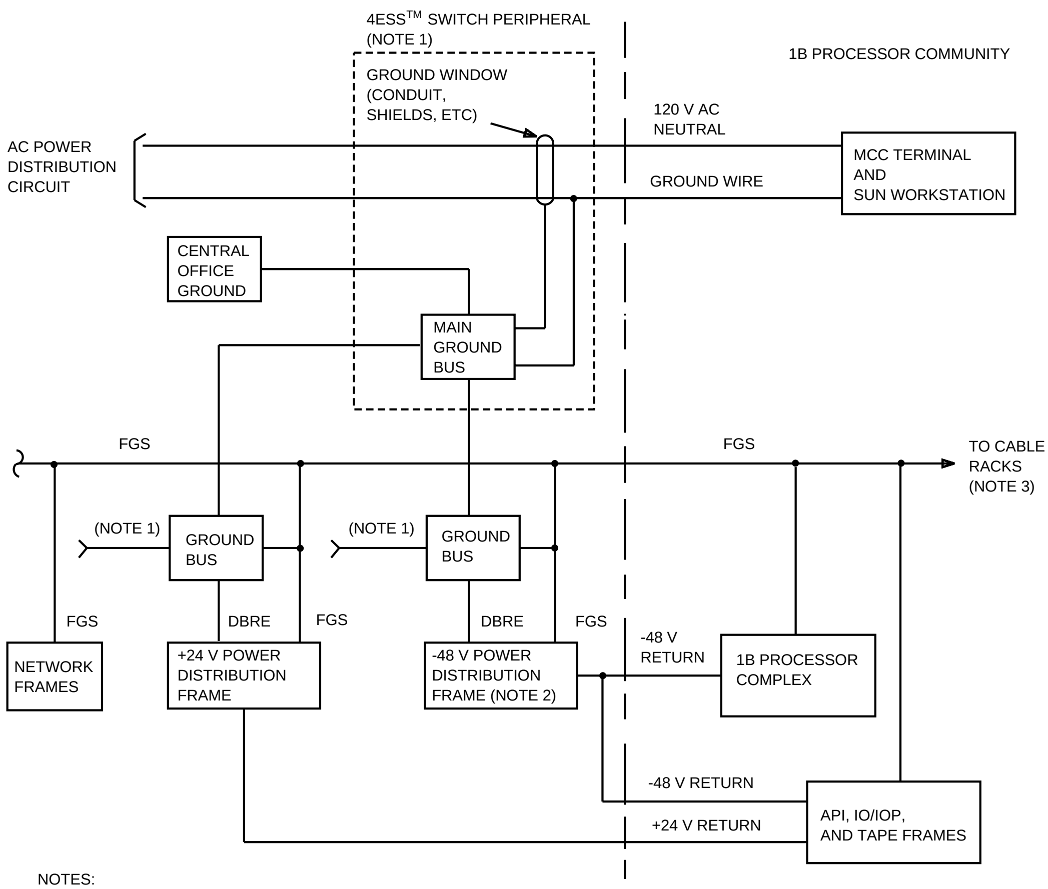


Figure 21. API, IO or IOP, and Tape Frames Power and Power-Related Alarm Circuits



NOTES:

1. ONLY A PORTION OF THE 4ESS SWITCH PERIPHERAL GROUNDING SYSTEM IS SHOWN TO SHOW THE INCORPORATION OF THE 1B PROCESSOR INTO THE SYSTEM.
2. WHEN -48 V BATTERY PLANT POWER SOURCE IS USED, THE POWER DISTRIBUTION FRAME IS J86334B. WHEN CONVERTER POWER PLANT SOURCE IS USED, THE POWER DISTRIBUTION FRAME IS J86334C.
3. 1B PROCESSOR CABLE RACKS ARE BONDED TO 4ESS SWITCH PERIPHERAL CABLE RACKS. BOTH ARE ELECTRICALLY ISOLATED FROM TRANSMISSION CABLE RACKS.

Figure 22. 1B Processor Protective Grounding System

7.03 Discrete devices (for example; resistors, resistor networks, capacitors, diodes, inductors, transistors, power modules, relays, oscillators, relays, oscillators) are required to have a 20-year life cycle and a high reliability rating. The KS devices are generally used. However, in cases where volume is not sufficient to support a KS specification, a WP-specification or commercial devices with the appropriate qualifications are used.

7.04 Components chosen for use in the 1B Processor complex are selected based on the following requirements in rank order:

- Availability
- Manufacturability (packaging & machine insertion)
- Supplier classification/preference
- Thermal characteristics
- Steady state fit rate
- Electrostatic discharge (ESD) rating
- Water soluble flux (WSF) rating
- Through-hole (TH) mountable.

7.05 Although packaging of devices is restricted to through-hole technology, it is recognized that some devices are only available in Surface Mount Technology (SMT). In these cases, the SMT device is mounted onto a chip carrier Circuit Module (CM) assembly.

7.06 Reliability of devices is based on calculations from *Reliability Information Notebook (RIN)*, Fifth Edition, October, 1985. Failure in Time (FIT) rates were obtained by reliability modeling using steady state conditions and are recorded in the PCL.

7.07 Electrostatic Discharged (ESD) is rated by the device's technology family. The 1B Processor PCL has device ratings obtained from the ICRQ data base in Allentown, N. J. The model used to obtain these ratings is the positive human-body model of (150 Ω by 150 pfd).

B. Circuit-Pack-Level Interconnection

7.08 To maximize manufacturability and design uniformity, the following two sizes of circuit packs make up the majority of the circuit pack designs used in the 1B Processor:

- UN (7.67 by 13.375 inches, 300-pin connector)
- KLW (15.67 by 13.375 inches, 600-pin connector).

These circuit packs represent the replacement modules within the system. Primarily consisting of multiple-layer printed wiring boards, these circuit packs typically consist of

4 to 8 signal-layers, a single-power layer and a single-ground layer. All circuit packs used in the 1B Processor also have full-width front faceplates which are both functional and aesthetic.

7.09 The circuit packs use a connector which provides 300 contacts which interconnect to a matrix of pins on the backplane (the KLW circuit pack codes utilize two of these connectors). These contacts are of a highly reliable bifurcated and selectively gold-plated design to ensure design life. These connectors have a force of 130 grams per contact during insertion. This is significant for this project due to the larger number of circuit pack contacts (600) on the KLW packs and therefore corresponding insertion forces. Due to the high insertion forces required to insert a circuit pack, all packs are equipped with a lever/latch which which eases insertion/extraction of the circuit packs from its associated apparatus mounting. KLW circuit packs have two levers, one located at the top and the other located at the bottom of the pack. A latch spring lock is incorporated into the lever, which allows a positive locking of the circuit pack to its mating apparatus mounting upon full insertion.

7.10 The circuit pack connectors form one-half of the *Fastech* packaging system keying scheme. The other half is being provided by the backplane assembly. The keying scheme employed is such that each circuit pack code will have a unique key code. This scheme provides a method whereby the circuit pack insertion lever will not engage the associated apparatus mounting, thus not allowing a circuit pack to be inserted, unless it is in its proper location as defined by the backplane mounted keyholder.

C. Unit-Level Interconnection

7.11 The next level of packaging involves the interconnection of the circuit packs to each other and their interface to other parts of the system. The building block structure which provides this level of interconnection is the unit. The unit hardware in the 1B Processor consists of *Fastech* packaging system designed apparatus mountings and associated hardware. The 1B Processor utilizes primarily two different apparatus mountings: the 132B for the UN-coded circuit packs and the 132L for the KLW-coded circuit packs. Both the 132B and 132L apparatus mountings provide for 22 circuit pack mounting centers, 1.00 inches apart. These mountings are 8 or 16 inches high, 14 inches deep, and 26 inches wide.

7.12 The inter/intraconnection and mechanical alignment of the apparatus mountings and the circuit packs within the unit is made via the backplane assembly. The backplane assembly is the heart of the interconnection system. The backplanes used in the 1B Processor are of two sizes: 8 by 23 inches for the UN-coded circuit packs, and 16 by 23 inches for the KLW-coded circuit packs. These backplanes are equipped with compliant pins which are press-fit into plated-through holes which form the mechanical and electrical connection to the backplane PWB. A field of these pins in the backplane constitutes a male connector, which mates with the 963L2 circuit pack connector on the circuit pack side of the backplane. The wiring side extension of these pins provides the pin field for cable connectors and discrete wiring. The backplanes used in the 1B Processor are multilayer PWBs, which have 10 to 18 layers of interconnection. All backplanes also incorporate design for assembly (DFA) features to allow for ease of overall equipment assembly in the factory. The DFA features were incorporated at the request of manufacturing to simplify the assembly of these parts to the backplane. This will also save assembly time and money as well as increase the quality level.

D. Frame-Level Interconnection

7.13 The final level of interconnection is the frame or cabinet level, involving the interconnection of all associated units and access interconnection from the "outside world" via pluggable cables. Three basic types of cables are used for unit or frame interconnections: switchboard cable, flat ribbon (tape) cable, and twinax cable.

Equipment Design

7.14 Duplex 1B Processors are contained within a two-cabinet complex, which is approximately 7 foot high, 5 foot 4 inches wide, 1 foot 10 inches deep, with each cabinet identical to the other. The 1B complex consists of the following:

- Two mechanically-joined, 7-foot, 4-post frames
- Center-opening doors mounted on the front and rear of the frame assembly
- Bezels on the front and rear
- End guards.

The 7-foot cabinet is required for containing the 1B in two frames. The bezel contains alarm LEDs for the cooling system and the fuse unit. The cabinets are joined using four bolts that screw into weldnuts that have been added to the cabinet frames. This will allow additional growth cabinets to be added without powering down a side of the 1B to remove the fuse unit. The complex consists of the following eight major units within each cabinet (see Table G):

(a) **Fuse Unit**: The fuse unit provides fusing for the other units, fuse alarms, and a TEL/TTY jack. It features pluggable cards that house the fuses. It is located in the top most position of the frame and is covered by the frame bezel.

(b) **Bus Driver/Receiver Unit**: The bus driver/receiver unit contains the necessary hardware to interface the 1B to the outside world (that is; the AU, PU, and GCP interface).

(c) **CC and IFB Unit**: The CC and IFB unit contains one-half of the CC and one IFB. There are a total of 12 client positions available.

(d) **CC and PS Unit**: The CC and PS unit contains one-half of the CC and one-half of the PS memory. This unit provides slots for up to seven PS circuit packs. One-half of PS [two PS circuit packs (three PS circuit packs if 4E22 generic PSE feature is present)] is contained in one cabinet and the other half [two PS circuit packs (three PS circuit packs if 4E22 generic PSE feature is present)] is contained in the other cabinet.

Table G. 1B Unit Names

#	Unit Name	Equipment Number	Subsystem
1	Fuse Unit	J4A023AG-1	PWR
2	Fan Control Unit	J4A023AE-1	COOLING
3	Bus Driver/Receiver Unit	J4A023AA-1	BDR
4	Central Control & Interface Bus Unit	J4A023AB-1	CC / IFB
5	Central Control & Program Store Unit	J4A023AC-1	CC / MEM
6	Call Store Unit	J4A023AD-1	MEM
7	Fan Unit	J4A023AF-1	COOLING
8	Filter Unit	J4A023AH-1	PWR

(e) **CS Unit**: The CS unit provides 20 CS memory positions along with the CS bus buffer circuit packs. One-half of CS (up to 20 CS circuit packs) is contained in one cabinet and the other half is contained in the other cabinet.

(f) **Filter Unit**: The filter unit is located in the base of the frame. It contains a mounting plate that holds filter capacitors for the system power.

(g) **Cooling System (Fan & Fan Control/Alarm Units)**: The cooling system consists of the fan and fan control/alarm units. The cooling system for the 1B consists of two physical units. The lower unit contains six variable-speed fans, inlet air temperature sensors, and an air filter; these are all located in the base of the frame. The upper control unit contains duplicated fan controllers and duplicated temperature sensors for each outlet air channel. The output of the fan control unit adjusts the speed to keep temperatures inside the cabinet within the control limits. An output for lighting cooling status LEDs on the bezel is provided as well as an interface to the SCAN/SD matrix for sending cooling error messages and for reporting status of the unit.

Environmental

7.15 The 1B Processor project has adopted the design philosophy of designing environmental compliance into the product with an emphasis on up-front engineering analysis performed as early as possible in the design stage. In this scenario, up-front design allows experimentation to be a verification rather than a design mechanism. Several tests were performed on the 1B Processor and a description of each follows:

- **Thermal Performance**: An initial study of the 1B System Thermal Capability in its early configuration was performed. In this study, maximum circuit pack wattages for each location of the processor were recommended. Recommendations were also made for possible cooling schemes and potential problem areas were identified. Forced convection cooling is the appropriate cooling method for the 1B power dissipation densities. This deviates from previous *4ESS* switching equipment where natural air convection cooling was used because of high temperature-grade devices and low-power densities. The circuit pack placement is based on 1-inch centers to create a uniform airflow. Blockages and component heights were kept to a minimum in order to maximize volumetric airflow through the cabinet. The cooling system was sized to allow for future client and memory additions.

- **Airborne Contamination**: The 1B processor has been designed with sensitivity to contamination standards. Except for particulate matter, there are no known components that are used in the 1B processor that are suspected to be vulnerable to these levels of listed contaminants. With a forced convection cooling scheme, there is the possibility of quickly building up large amounts of particulate matter on the components inside the system. This reduces heat transfer capability and the ability to move air easily through the system. To reduce this build up, all air is filtered through a polyester filter. This push fan arrangement allows positive pressure inside the cabinet thus preventing unfiltered air from contaminating components. Although this filter is effective for large particles, it is not for small ones. Design against hygroscopic dust contamination has also been considered in the design of the 1B Processor. Since no air filtering material can mechanically filter dust particles of this size, some provisions have been made to run the cooling fans only at speeds required to reliably cool the electronics. This will minimize all levels of contamination and will require less filter maintenance. Voltage levels have also been kept below levels observed to be susceptible to shorting due to hygroscopic dust.
- **Acoustical Noise**: Acoustical noise for a single frame is to be kept below 60 dB. For this reason, a fan with a redesigned blade has been selected for use in the fan unit. The fans have also been tuned to operate at the same speed. Reduction in fan speed at typical office environmental conditions will lower fan noise.
- **Fire Resistance**: All components selected for use in the 1B Processor are fire resistant.
- **Earthquake and Office Vibration**: Earthquake and vibration has been considered in the design of the 1B Processor. Standard *Fastech* packaging system hardware has been used to minimize susceptibility.
- **Electromagnetic Compatibility**: Testing was performed to verify that emissions and susceptibility design objectives are met.
- **Electrostatic Discharge**: Testing was performed to verify ESD requirements. Care should be taken when handling 1B Processor circuit packs. The use of wrist straps is required when removing and installing circuit packs.

8. 1A Technology—I/O, I/OP, DUS, and TUC Frames

General

A. Introduction

8.01 1A technology (1A) is a system consisting of a set of common hardware and circuit devices which are assembled in accordance with specific rules and design tools to form electronic switching equipment frames.

8.02 The smallest building blocks of this system are the integrated circuit device and the discrete component. At this level, physical packaging and circuit interconnection are accomplished by connectorized circuit packs. Circuit packs are connected to other circuit packs and to other small pieces of equipment such as memories and power supplies to form a unit. The main physical support for a unit is a mounting plate on which connectors and apparatus mountings are attached. The apparatus mountings provide support for the circuit packs and also guide them into the connectors, thus ensuring proper mating. The circuit pack connectors are interconnected within a unit by the combined use of printed circuit and wire-wrapped connections. Units are assembled into a standard frame from the front by attaching the unit mounting plate to the frame mounting bars. Interconnection between units within the same frame or between units in different frames are connectorized to allow for rapid installation and repair of the electronic switching equipment.

B. Application of 1A Technology

8.03 1A technology is unique from previous technologies in its extensive use of integrated circuits and modular, connectorized concept of design. This allows for factory testing, rapid field installation, and ease in equipment modification and repair. The 1A technology was initially developed for use with the 1A Processor and the *4ESS* switch.

Frame Description

A. Frame Types

8.04 The following three types of sheet-metal frames are used in 1A technology as the basic equipment support structure. Dimensions of these frame types are provided in Table H.

- Single-bay frames
- Double-bay frames
- Triple-bay frames.

B. Frame Units

8.05 Frames are equipped by installing units via front-accessible mounting plates. The mounting plates span the area between the frame bay uprights and attach to the vertical-frame bay mounting bars. Frames are cooled by free convection air flow. Where necessary, heat baffles are installed between units to direct hot air away from the upper unit while not impeding the air flow through the lower unit. A typical unit is constructed on a mounting plate. The mounting plate contains a number of circuit packs housed in apparatus mountings, circuit pack connectors, multilayer printed wiring board(s) for interconnecting circuit pack connectors, and intra-unit wiring. Also, a wide assortment of electrical hardware and terminal blocks are provided on various frame units.

Table H. Frame Dimensions

Frame Type	Standard			Optional Depth*
	Height	Width	Depth	
Single Bay	7’0"	2’2" 3’3"	1’0"	1’6"
Double Bay	7’0"	4’4" 6’6"	1’0"	1’6"
Triple Bay	7’0"	6’6"	1’0"	1’6"

* All 1A Processor frames are 1’6" deep.

C. Circuit Pack Types

8.06 The **FA ceramic circuit packs** are constructed from a 3.25-inch by 4-inch hybrid integrated circuit (HIC) attached to a 4-inch by 7-inch aluminum plate. Electrical connections to the HIC are implemented via a 946-type plug connector which is mechanically attached to the aluminum plate. Although the aluminum plate is primarily a heat sink for the HIC, it also provides a mechanical link to the connector during removal and installation of the circuit pack. The HIC is encapsulated with a coating of silicon rubber [room temperature vulcanized (RTV)] for protection against humidity and dust. Mechanical protection for the HIC is provided by a cover plate which attaches to the aluminum plate. Two basic types of FA circuit packs constructed for 1A technology are as follows:

(a) The **FA digital circuit pack** HICs consist of bi-level substrate, film integrated circuits to which active logic devices (beam-leaded silicon-integrated circuits) and capacitors are bonded. The HIC has a fixed format that allows a maximum of 52 silicon integrated circuits (SICs) to be bonded to the substrate. The fixed format also allows for the extensive use of machine aids in the design, manufacture, and testing of FA circuit packs.

(b) The **FA augmented circuit pack** HICs consist of bi-level substrate, film-integrated circuits. However, in addition to the standard devices, any approved beam-leaded active or passive devices and thin film resistors can be bonded to the substrate. Insulated gate field effect transistor (IGFET) memories are an example of devices which can be bonded to the substrate.

8.07 Seven types of **discrete component circuit packs** (FB, FC, FE, FF, FG, JK, and JL) are constructed for 1A technology (Table I).

D. Circuit Pack Connectorization

8.08 Plug connectors are designed to be attached to circuit packs. Receptacle connectors are designed to be attached to the unit's mounting plate (Table I). The 971B-type receptacle connector consists of two 947-type receptacle connectors. The 947-type receptacle provides 82 leads. These leads are thermal-compression (TLCN) bonded to the gold lands on the ceramic substrate.

8.09 The 947A-, 947C-, and 947E-type receptacle connectors are attached to the unit's mounting plate. These receptacle connectors provide an 82-pin terminal/connector designed to connect an FA ceramic circuit pack or a double-sided discrete component circuit pack to the backplane. Terminal pin and quadrant designations are shown in Figure 23. The terminals of the 947C-type receptacle connector are hard, gold plated. The hard, gold plate is required when mating with backplane connector.

8.10 The 947B-, 947D-, and 947F-type receptacle connectors provide a 42-pin terminal/connector designed to connect single-sided discrete component circuit packs to the backplane. Terminal pin and quadrant designations are shown in Figure 24. The terminals of the 947D-type receptacle connector are hard gold plated. The hard, gold plate is required when mating with backplane connectors.

Table I. Discrete Component Circuit Packs

Circuit Pack	Circuit Board Type	Size	Type Plug	Connector Terminal	Receptacle
FB	0.062-inch thick, epoxy-glass	4" x 8"	946B	42	947A, B, C, D, E, and F
FC	0.062-inch thick, epoxy-glass	4" x 8"	946C	82	947A, B, C, D, E, and F
FE	0.062-inch thick, epoxy-glass multilayer	8" x 13"	970A*	164	971B†
FF	0.062-inch thick, epoxy-glass multilayer	8" x 9"	970A*	164	971B†
FG	0.062-inch thick, epoxy-glass multilayer	8" x 7"	970A*	164	971B†
JK	0.062-inch thick, epoxy-glass	6" x 8"	946C	82	947F
JL	0.062-inch thick, epoxy-glass	6" x 8"	946B	42	947F

* 970A-types are two 946C-type connector.
† 971B-type receptacles are two 947C-type receptacles.

E. Circuit Pack Apparatus Mountings

8.11 Circuit packs are held in place on a unit by apparatus mountings which attach to the frame's mounting plate. Designation strips are attached to the top-front of the apparatus mountings. These strips identify the circuit pack code, circuit pack position, and the circuit schematic. Circuit pack designation strips are further discussed as part of the coordinate numbering plan. Fourteen types of circuit pack apparatus mountings are used in 1A technology: 79B, 80C, 80D, 81B, 87B, 97B, 97C, 97D, 98B, 98C, 98D, 104B, 104C, and 104D. The 80C- and 81B-type apparatus mountings are for mounting fourteen and sixteen 4-inch high circuit packs on 1/2-inch centers, respectively. The 80D-type apparatus mounting is for mounting nine 4-inch high circuit packs on 3/4-inch centers. The 79B-type apparatus mounting is for mounting eleven 4-inch-high circuit packs on 1/2-inch centers. The 87B-type apparatus mounting is for mounting fourteen 6-inch-high circuit packs on 1/2-inch centers. The 97-, 98-, and 104-type apparatus mountings are designed for the FE, FF, and FG coded discrete component circuit packs. These apparatus mountings use insertable plastic card guides. The card guides provide flexibility in the horizontal spacing and number of circuit packs which may be equipped within each apparatus mounting. Card guides may be placed on 0.25 inch increments. However, when the 97-, 98-, and 104-type apparatus mountings are used to mount FE, FF, and FG coded circuit packs, a 0.50-inch minimum distance must be maintained between the packs. All circuit pack apparatus mounting used for FE, FF, or FG coded discrete component circuit packs have an optional spring(s) for circuit pack retention. This option is only used for circuit packs with miniature relays.

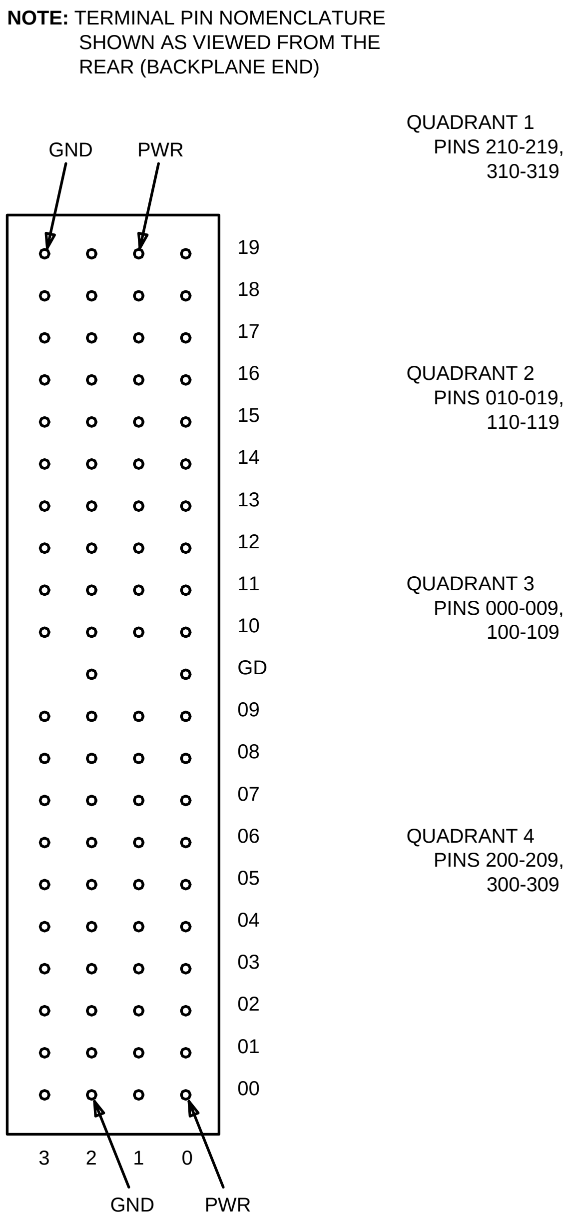


Figure 23. 947A-, 947C-, and 947E-Type Receptacle Connector — Terminal Pin Nomenclature

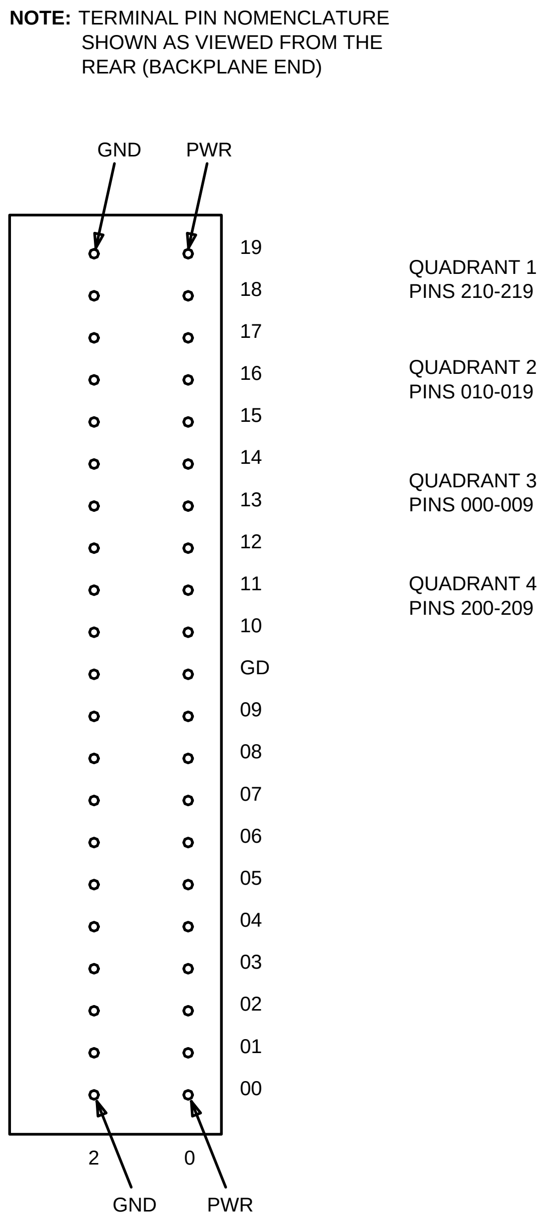


Figure 24. 947B-, 947D-, 947F-Type Receptacle Connectors — Terminal Pin Nomenclature

F. Multilayer Printed Wiring Board Backplanes

8.12 Presently, multilayer printed wiring board (MLPWB) backplanes are used primarily for power, ground, and some signal distribution. The MLPWB backplanes consist of a number of single- or double-sided, epoxy-glass, printed circuit boards laminated into a single structure with embedded copper paths (Figure 25). The various layers are connected to each other and the outside world by means of plated-through holes. The plated-through holes are arranged in a 0.125-inch grid that matches the geometry of the 947-type receptacle connector and coax terminal field pins. Present technology limits the characteristics of the MLPWB backplanes to a maximum of ten circuit layers, and a maximum board size of 16 inches high by 24 inches wide. In addition, the thickness of all MLPWB backplane is fixed at approximately 0.1 inch. This restriction allows the use of standardized hardware when mounting MLPWB backplanes to the back of the frame.

Coax Terminal Fields

8.13 Coax terminal fields (CTFs) supplement the 947-type receptacle connector terminal fields. The CTF provides a maximum of 32 positions on which coax signal and ground leads can be terminated. The signal leads and ground leads from the CTF are connected to corresponding 947-type receptacle connector terminals via the MLPWB backplane. A CTF consists of a plastic strip from which the terminals extend. During unit assembly, the plastic strip is placed between the mounting plate and the MLPWB backplane. The CTF terminals extend through the MLPWB backplane above and below the 947-type receptacle connector area. The CTF plastic strip acts as a spacer between the MLPWB backplane and the mounting plate, and is used for this purpose independently of the need for CTFs. The CTF terminal designations and location, with respect to the 947-type receptacle connector terminals, are shown in Figure 24.

Unit Intraconnections

8.14 The majority of interconnections between circuit packs on the same unit are made by automatic wire-wraps using plastic insulated 30 AWG wire. Where more stringent cross-talk requirements must be met, tight-twisted pair and miniature coax are used. These wires are usually semiautomatically applied. The coax, because of the extra preparation required, costs significantly more and is used only where necessary. Signal leads implemented with solid wire and tight-twisted pair are routed in rectilinear paths (Manhattan Geometry) and are termed surface wiring. Power, ground, and some signal distribution are provided to the circuit packs by the MLPWB backplane.

G. Connections Between Units and Frames

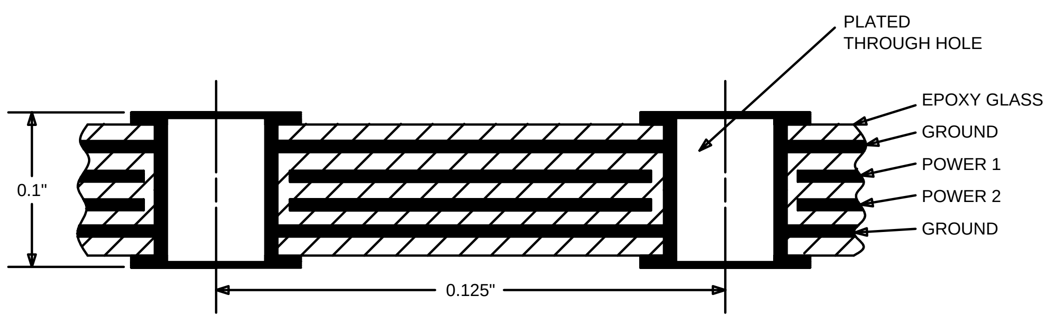
General

8.15 One of the objectives of 1A technology is to facilitate factory unit and frame testing, field installation, unit replacement, and growth tasks. This is done by connectorizing, as opposed to hard-wiring, interunit/intraframe, and interunit/interframe connections. The basic 1A technology hardware component used to meet this objective is the connectorized cable assembly. Connectorized cable assemblies are constructed using flat, flexible cable, standard 8-pair switchboard cable, coax cable, and discrete wire attached to backplane connectors (Figure 26). The backplane connectors (942-, 943-type) are designed to plug directly into the backplane terminals of the 947-type receptacle connectors. Thus, connectorization requires no additional frame hardware.

Backplane Connectors

8.16 Backplane connectors (942- and 943-type) are built up from either a 1-inch by 1.25-inch or a 1.25-inch by 1.50-inch printed circuit board. One or two plastic contact housings, each having ten box-type socket terminals, are attached to the circuit board. Contact tabs from the terminals extend beyond the back of the contact housing and are soldered to the printed circuit board. Cable leads are soldered to the appropriate electrical paths on the opposite side of the printed circuit board. The cable is then mechanically fastened to the circuit board with a strain relief device. Backplane connectors containing 16 or 20 terminals are designed to mate with one quadrant of a 947C-type receptacle connector. The contact housing limits terminal pin penetration to 0.25 inches. This allows the use of wire-wrap connections (two maximum) under the backplane connector. These wire-wrap connections are mechanically protected by the 82- or 83-type apparatus mounting.

8.17 Backplane connectors are held in place on the 947-type terminals with 82- and 83-type apparatus mountings which fit over the 947-type terminal field. These apparatus mountings provide for the alignment of the terminal pins and for guidance and locking of the backplane connector into its mating position.



TYPICAL CROSS-SECTIONS		
GRD	GRD	GRD
PWR	PWR	PWR
GRD	PWR	GRD
	GRD	PWR
		GRD

Figure 25. Multilayer Printed Wiring Board Backplane — Typical Cross Sections

Cable Types

8.18 **Flat, flexible cable** is used because of its controlled electrical properties and the low cost at which it can be terminated (many wires handled at one time). The flat cable used consists of either 24 or 31 *TEFLON** insulated 32-AWG parallel conductors. The cable is usually used as 100-ohm unbalanced transmission lines for interunit connections. This application provides excellent cross-talk performance. Flat, flexible cable can provide 8, 10, or 16 signal leads. These leads are configured with alternate signal leads surrounded by multiple shield ground leads.

8.19 **Standard eight-pair switchboard cable** is used for balanced interunit connections. Though this cable is low in cost, it is more costly to terminate than flat-flexible cable. Therefore, it is used for long runs, runs where the required fold structure of flat-flexible cable would be too complex or where the superior performance of a twisted-pair wire is needed for balanced transmission.

8.20 Other types of cable such as local cables—discrete wire or coax—and power cables are also connectorized. These cable assemblies usually do not provide the cost advantages of the other two cable types.

Cable Routing

8.21 Intraunit/intraframe cables originate at the 947-type receptacle connector terminal fields on one unit and usually run horizontally to the frame sides. The cables then run vertically through the cable guides to the terminating level. They again run horizontally to the proper terminating point.

8.22 Interunit/interframe cables originate at the 947-type receptacle connector terminal field and run horizontally to the frame sides. The cables then run vertically through the cable guides to the interframe cable racks above the frame. Different classes of interframe cables are segregated by compartmentalized cable racks (Figure 27).

H. Coordinate Numbering Plan

General

8.23 The coordinate numbering plan is used to identify the location of equipment and apparatus on units and frames. These locations are termed equipment locations (EQLs) in the frame coordinate numbering grid (Figure 28). Typically, equipment locations (EQLs) consist of a frame bay identifier, a vertical equipment location, and a horizontal equipment location (Figure 29).

8.24 Equipment locations (EQLs) are converted to **x** and **y** dimensions and combined with component terminal coordinates to generate automatic and semiautomatic wiring data.

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* Registered trademark of E.I. DU Pont de Nemous and Company.

Frame Vertical Positions

8.25 Frame vertical positions are numbered from 00 through 83 in 1-inch center line increments starting at the base of the frame (Figure 28). Vertical position numbers are stamped on the mounting bars in the front and rear of single-, double-, and triple-bay frames.

8.26 The location of a unit in a frame bay is identified by the vertical position number of the bottom edge of the unit. When equipment is mounted between two vertical position numbers, the equipment is identified by the lower position number. The bay identifier (0, 1, or 2) precedes the vertical position number for double- and triple-bay frames.

Frame Horizontal Positions

8.27 Frame horizontal positions are numbered in 1/2-inch center line increments with position 00 beginning 1.75 inches to the right of the left bay upright (Figure 27). Frame bays 2-feet 2-inches wide have horizontal positions ranging from 00 to 44 and 3-foot 3-inch wide bays have horizontal positions ranging from 00 to 70.

8.28 Frame horizontal positions are subdivided for locating components (circuit packs) which are mounted on wider than 1/2-inch center lines. The suffix **P (plus)** is added to the horizontal equipment position number to indicate **plus one-half of a division** (0.25 inches) to the right of the base position number.

EQL Application to Circuit Pack Identification

8.29 The EQLs for circuit packs are based on the location of the 947-type connector. Hinged designation strips, which are attached to the circuit pack apparatus mounting, are stamped on both sides with the applicable vertical and horizontal position numbers. Also stamped on the designation strip are circuit pack type designations, the unit identifier, and functional designation. Space is provided for stamping cautions regarding circuit pack removal and replacement.

EQL Application to 947-Type Receptacle Connector and CTF Terminal Pin Identification

8.30 The location of a 947-type receptacle connector terminal field is identified by the nearest vertical and horizontal EQLs with respect to the center lines of the terminal pin fields (Figure 30). A particular pin within a terminal field is identified by combining the pin coordinates (three digits) with the vertical and horizontal EQLs of the terminal field.

8.31 The location of a CTF, top and bottom, is identified by the nearest horizontal EQL with respect to the center line of the terminal field—same as 947-type horizontal EQL. The top CTF associated with the 947-type terminal field is identified by the 947-type terminal field vertical EQL plus one division (1-inch). The bottom CTF is identified by the 947-type terminal field vertical EQL minus one division (1-inch). A particular pin within a CTF is identified by combining the pin coordinate (two digits) with the vertical and horizontal EQLs of the CTF.

I. Power

DC-to-DC Converters

8.32 Frame dedicated DC-to-DC converters are used for changing –48, +24, and –24 V to precision DC voltages. The converters are located as close as possible to the circuitry which they are associated. In 1A technology, the converters are mounted in the associated equipment frame in the same manner as circuit packs. Associated with each converter are voltage and current monitoring circuits which produce a power alarm signal when an out-of-tolerance condition exists. The high-voltage input side of each converter is fused on a separate frame-mounted fuse panel. Overcurrent shutdown is provided on all converters to protect the backplane wiring. The types of various power converters used by the 1B Processor are listed in Table J.

Frame Filter Units

8.33 Frame filter units, located in the base of a frame, are used where necessary to isolate each frame from the +24, –24, and –48 V power bus. Filters are not used in frames that meet the feeder rate of change requirements of 0.1 ampere (maximum) per microsecond and can tolerate noise levels of 1 V peak-to-peak.

Power Control

8.34 The power switch provides a craft-machine interface for power control at the frame level. Controls and indicators associated with this switch are described in Table K.

Miscellaneous Power Associated Hardware

8.35 Adjacent unit mounting plates are connected using ground clips. The clips provide continuous frame grounding. When power is supplied to a multilayer printed wiring board (MLPWB) backplane by a means other than backplane connectors, power lugs are used to make the connection. The power lugs are soldered to the MLPWB. Spade-lug prepared power leads are connected to the screw terminals provided by the power lugs.

9. References

9.01 234-000-000, *4ESS Switch—Numerical Index* 234 contains a detailed list of all Lucent Technologies Practices relevant to the 1B Processor.

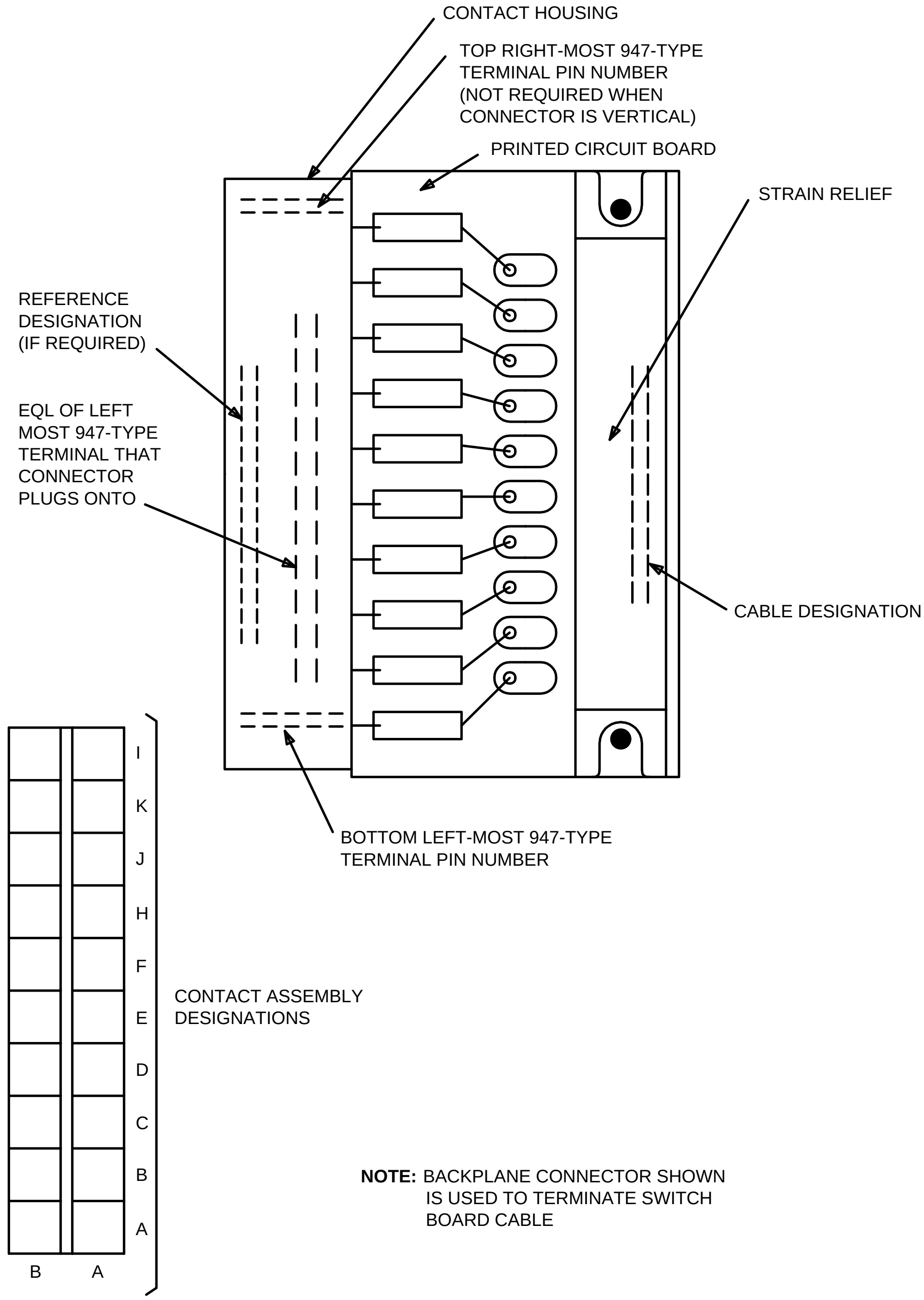
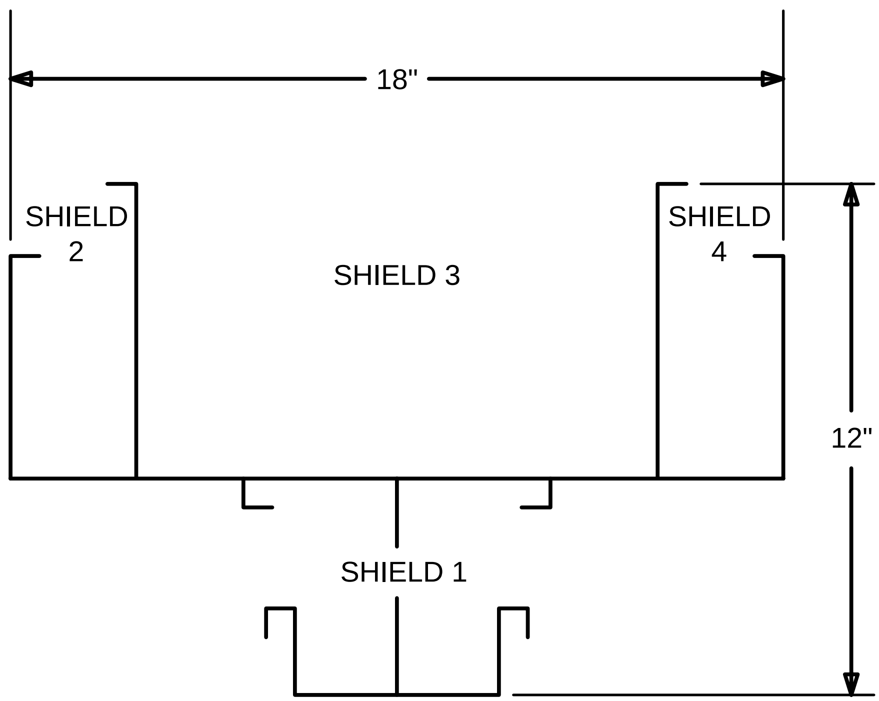


Figure 26. Typical Backplane Connector



LEGEND:
SHIELD 1 - BUS
SHIELD 2 - SCANNER
SHIELD 3 - TIP AND RING
SHIELD 4 - POWER

NOTE:
ONLY SHIELDS 1 AND 4 ARE USED
BY THE 1A PROCESSOR.

Figure 27. Compartmentize Cable Rack — Typical Cross-Section

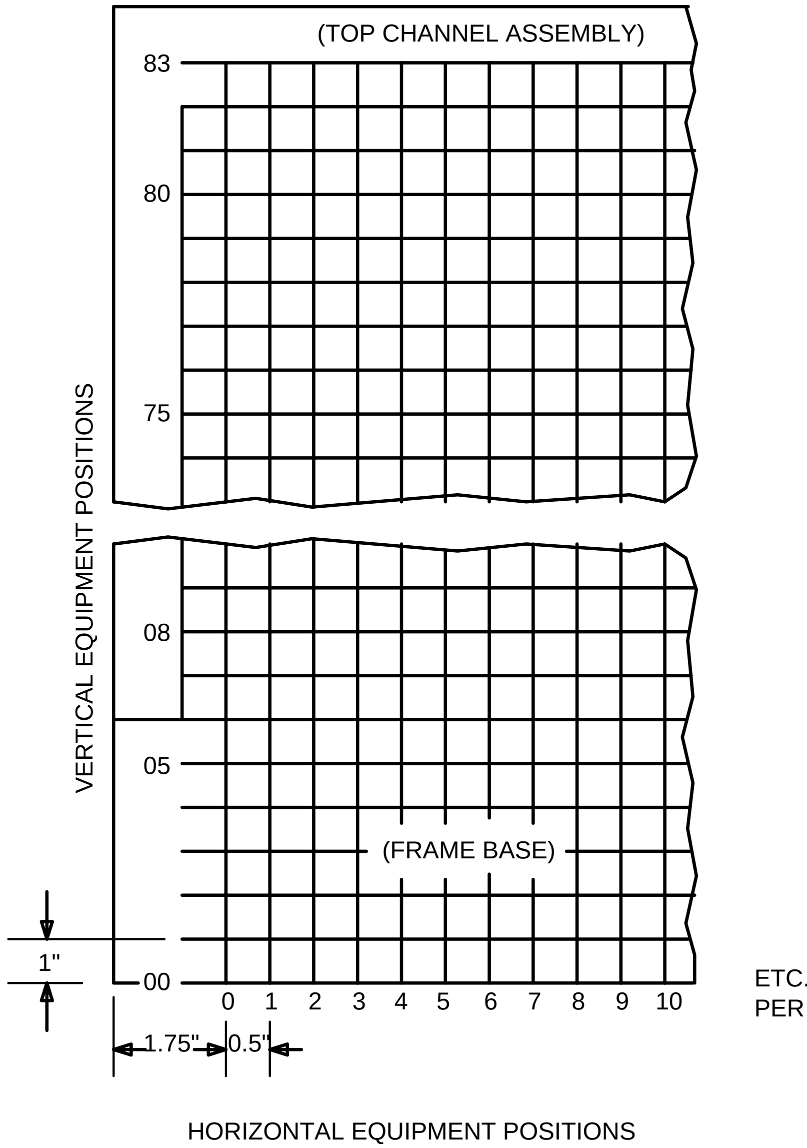


Figure 28. Frame Bay Coordinate Numbering Grid

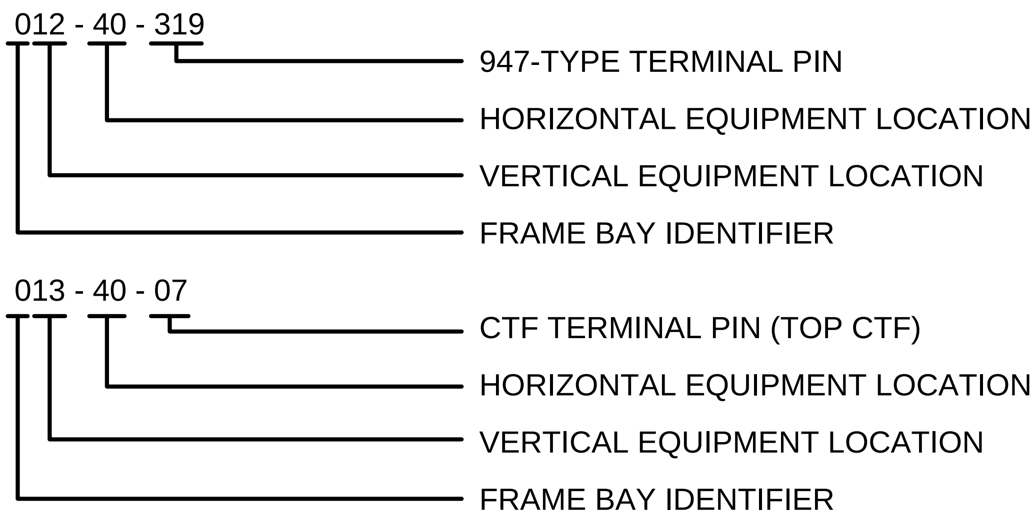


Figure 29. Typical EQL Expressions

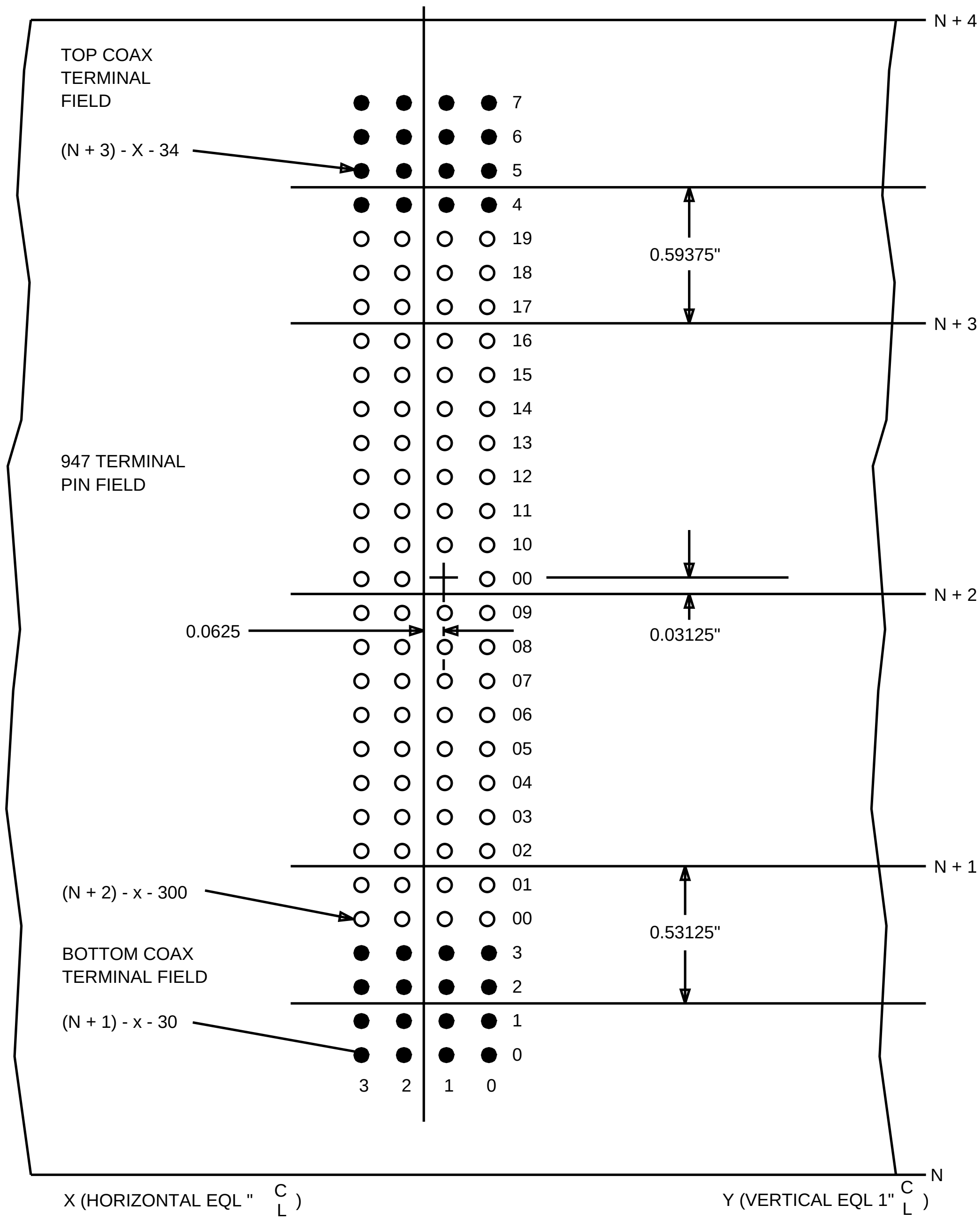


Figure 30. 947-Type Receptacle Connector and CTF Terminal Pin Identification

Table J. 1A Processor DC-to-DC Converters and Power Units

<table>
<tr><th rowspan="2">Number</th><th rowspan="2">Type</th><th colspan="2">Voltage</th><th rowspan="2">Current (Amperes)</th></tr>
<tr><th>In</th><th>Out</th></tr>
<tr><td>J87380-2*</td><td rowspan="8">DC-to-DC Converter</td><td>-48</td><td>+3</td><td>8</td></tr>
<tr><td>J87389E*</td><td>-48</td><td>+3 or -3</td><td>4</td></tr>
<tr><td>J87389H*</td><td>-48</td><td>+6</td><td>3</td></tr>
<tr><td>J87389J*</td><td>-48</td><td>+5</td><td>4</td></tr>
<tr><td>J87389M2*</td><td>+24</td><td>+3 or -3</td><td>2</td></tr>
<tr><td>J87389N*</td><td>+8 or -8</td><td>1.5</td><td></td></tr>
<tr><td>J87389S*</td><td>+24</td><td>+5</td><td>2.5</td></tr>
<tr><td>J87411A*</td><td>-48</td><td>+3
-3
+6
+12
-12</td><td>17
10
8.5
10
10.5</td></tr>
<tr><td>71G*</td><td rowspan="2">Power Unit</td><td>-48</td><td>+24 or -24
+28 or -28</td><td>3
3</td></tr>
<tr><td>106A*</td><td>+24</td><td>+19</td><td>1</td></tr>
<tr><td>130J†</td><td rowspan="10">DC-to-DC Converter</td><td>-48</td><td>+28 or -28</td><td>1</td></tr>
<tr><td>136D†</td><td>-48</td><td>-9
+5</td><td>0.15
11</td></tr>
<tr><td>136E†</td><td>-48</td><td>+12</td><td>4</td></tr>
<tr><td>136L†</td><td>-48</td><td>+12</td><td>4</td></tr>
<tr><td>136G†</td><td>-48</td><td>+5</td><td>17.5</td></tr>
<tr><td>136H†</td><td>-48</td><td>+5
+12
-12</td><td>15
1
1</td></tr>
<tr><td>136J†</td><td>-48</td><td>-9
+5</td><td>0.7
16</td></tr>
<tr><td>235A†</td><td>-48</td><td>+12
-12</td><td>0.2
0.2</td></tr>
<tr><td>236A†</td><td>+24</td><td>+5</td><td>2</td></tr>
<tr><td>244A†</td><td>Bulk DC-to-DC Converter</td><td>-48</td><td>+3</td><td>100</td></tr>
</table>

* 1A Technology converters which used 946-type plug connectors.

† Other than 1A Technology converters which used printed-wiring board-edge connectors.

Table K. Power Switch Controls and Indicators

Control/ Indicator	Type	Function
OFF NORM	From frame Lamp (White or Green)	When lighted, indicates that request has been made to take frame or unit out of service. **PWR OFF** and **OFF NORM** both lighted indicates power has been removed manually
ACK	From frame Lamp (White or Green)	When lighted, indicates program has recognized request for out-of-service or that diagnostic tests made following request for frame or unit restore-to-service are in progress
OS	Lamp (Yellow or Amber)	When lighted, indicates program has taken frame or unit out of service
PWR OFF	Lamp (Red)	When lighted, indicates power removed from frame. If **PWR OFF** is lighted and **OFF NORM** is extinguished, power removed from frame or unit under fuse alarm (FA) conditions
OFF *	Rotary/Pushbutton Switch	When rotated clockwise (**OFF** on face of switch is horizontal), request is made to program to remove frame or unit from service. If **OS** lamp lights, **OFF** may be pressed to remove power from frame or unit on which switch is mounted.
ON *	Rotary/Pushbutton Switch	When pressed, turns on power to frame or unit. A request to program is made to diagnose frame or unit if **OFF** switch is rotated counterclockwise; frame or unit is restored to service at end of diagnosis. **ON** switch also clears power alarm test circuitry if power alarm test has been performed.
TEST	Pushbutton Switch	When pressed, provides lamp test. If **Off** switch is rotated clockwise and TEST is pressed, power alarm test is performed. Exception is 256K store for which lamp test is performed regardless of normal/ROS state.

* **OFF** and **ON** pushbuttons are part of same switch.

Abbreviations and Acronyms

A

AC
Advance CMOS

ADS
Auxiliary Data System

AMASE
Automatic Message Accounting Standard Entries

API
Attached Processor Interface

APS
Attached Processor System

APU
Autonomous Peripheral Unit

ASW
All Seems Well

ASWF
All Seems Well Failure

AU
Auxiliary Unit

AUB
Auxiliary Unit Bus

AUI
Auxiliary Unit Interface

C

CC
Central Control

CM
Circuit Module

CMOS
Complementary Symmetry Metal Oxide Semiconductors

CS
Call Store

CSB
Call Store Bus

CTF
Coax Terminal Field

D

DFA
Design For Assembly

DMA
Direct Memory Access

DPF
Data Parity Failure

DUS
Data Unit Selector

E

EAI
Emergency Action Interface

ECL
Emitter Coupled Logic

EIA
Electronic Industries Association

EMI
Electromagnetic Interference

EQL
Equipment Location

ESD
Electrostatic Discharged

F

FAST
Fairchild Advance Schottky

FEM
Finite Element Method

FIT
Failure in Time

G

GCP
Generated Control Pulse

H

HIC
Hybrid Integrated Circuit

I

I/O
Input/Output

IFB
Interface Bus

IGFET
Insulated Gate Field Effect Transistor

INJ
Interject

IOP
Input/Output Processor

L

LEC
Local Exchange Carrier

LPA
Lower Protection Area

LS
Low-Power Schottky

LSI
Large-Scale Integration

LSS
Laboratory Support System

M

MCC
Maintenance Control Center or
Master Control Console

MLPWB
Multilayer Printed Wiring Board

MMIO
Memory Mapped Input/Output

MUP
MCC and Utility Processor

P

PC
Processor Configuration

PCD
Power Conversion and Distribution

PCRV
Processor Configuration Recovery

PLD
Programmable Logic Devices

PORTS
Portable Recovery Test Set

PPI
Processor Peripheral Interface

PS
Program Store

PSB
Program Store Bus

PSE
Program Store Extended

PUB
Peripheral Unit Bus

PUBB
Peripheral Unit Bus Branching

PUEA
Peripheral Unit Enable Address

PUR
Peripheral Unit Reply Bus

PUW
Peripheral Unit Write

R

ROM
Read-Only Memory

RTV
Room Temperature Vulcanized

S

S
Store

SC
Stack Counter

SD
Signal Distributor

SIC
Silicon Intergrated Circuit

SMT
Surface Mount Technology

SS
Store Secure

SSD
Scanner and Signal Distributor

T

TAPF
Trap Address Parity Fail

TAR
Transition Address Register

TASWF
Trap All Seems Well Failure

TDPF
Trap Data Parity Fail

TH
Through-Hole

TIRM
Technical Information Resource Management

TLCN
Thermal-Compression

TME
Trap Mode Error

TU
Tape Unit

TUC
Tape Unit Controller

U

UPA
Upper Protected Area

UPD
Update Bit

V

VDT
Video Display Terminal

W

WSF
Water Soluble Flux

X

XM
Extended Memory Mapped Input/Output

XS
Extended Call Store

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Document No.: 234-301-001 Issue 6 Date: December 1998

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